Turtle logic: Novel IC digital probabilistic design methodology

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I. Introduction

With the progress on VLSI process technology, the design complexity and the transistor density in system increases rapidly, causing that the power consumption and power density in system rise with the same trend. The size of CMOS devices is scaled down to the nanoscale level where interferences (soft-errors), becoming significant, affect the VLSI circuit performance [1]. Future electronic devices are expected to operate at lower voltage supply to save power, especially in ultimate and new technologies. The resulting reduction of logic levels approaches the thermal noise limit, and consequently signal to noise margins are reduced, exposing computations to higher soft-error rates [1]. In other words, the future circuits will be in a scenario where all devices may fail due to soft-error produced by trend of low SNR.

In order to design reliable circuits with unreliable components, novel design techniques have been introduced. The problem of designing reliable systems with unreliable components traces back to Von Neumann, who proposed the N-tuple Modular Redundancy (NMR) technique [2]. Additional proposals have appeared in the literature addressing the problem from the point of view of noise tolerance. For instance, the approach based on Markov Random Field theory (MRF) [3]. [4] Take in account the Hamming distance for build basic logic gates focus to high noise and low voltage scenarios.

Therefore, our proposal is based on the assumption that the devices in new and future technologies will be not perfect, noisy and hence they might fail.

II. Probabilistic formulation

In low power supply scenario and future technology, the noise margin will be too small, and therefore soft errors due to all kinds of noise sources become crucial.

In our proposal, the technology independent has been considered, and only we take into account noise level and duration which propagate through logical primitives [5] with probability P_e. For simplicity, and without loss of generality, the signals may be modeled as two-logic level, with additive white Gaussian noise $f(x)$, no correlated, with mean μ, standard deviation σ and variance σ^2.

II.A. Error caused by noise in one digital node

Figure 1 shows the voltage probability distribution in a noisy digital node. It can be described as two Gaussian distributions centered on low and high voltages (0 and V_{DD} respectively). An error can be produced when logic 1 is interpreted as logic 0 and vice versa. The respective probabilities of such cases are denoted as P_{e1} and P_{e0}.

Assuming that logic 1 and logic 0 are equally probable, the probability that the data in a node is incorrect P_e is given by the addition of P_{e1} plus P_{e0} divided by two.

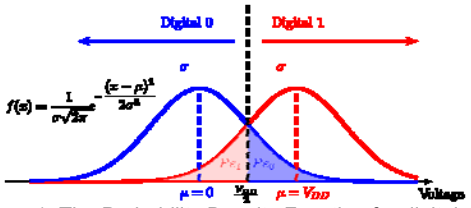

Figure 1. The Probability Density Function for digital values with $\mu = 0$ (V) and $\mu = V_{DD}$ (V) in a digital node, under influence of White Gaussian Noise.

III. Port redundancy

In this section, the improvement of reliability of digital modules using ports redundancy (PR) is presented. The Figure 2 shows how a module with one input and one output may have $(n - 1)$ replicated ports, and where the conventional differential logic is a particular case $(n = 2)$. The respective replicated ports can be either equal or complementary to the original port as can be seen in the Figure 2(b).

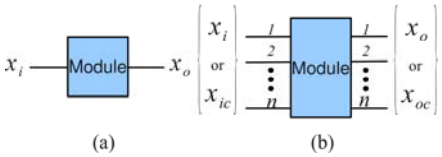

Figure 2. Port redundancy. (a) Module with one input and one output port (for instance, a traditional NOT gate), (b) Module with $(n - 1)$ replicated ports.

In general, a port redundancy has three different scenarios, with probabilities defined as:

1. Correct scenario: the values of all logic inputs are interpreted correctly. The probability is $(1-Pe)^n$.
2. Discrepant scenario: One or several ports have Voltage values which causes an incorrect interpretation (logic 0 instead of intended logic 1 or vice versa). The probability is given by the permutation sum of Pe and $(1-Pe)$.
3. Error scenario: All the ports are misinterpreted and it has a probability of P_e^n.

III.A. Analysis of error reduction with port redundancy

The error probability (P_{emi}) depends exponentially on the number of replicated ports. The Figure 3 shows the results of error probability for a single gate with redundancies from 0 to 9, for a SNR from 1 to 20 dB. As expected, if the number of replicate ports is increased, the error probability is reduced. For the specific case of Redundancy of 1 with SNR=1dB, the decrease in error probability is of 20.44%. When further increasing the in 2, 3 and 4 times, the corresponding decrease in error probability is smaller each time, with decrements respect to before redundancies of 8.26%, 5.9%, 1.68%, 0.49%, respectively, so for redundancies beyond of 4 times gives a negligible decrement in error probability. For SNR greater than 1dB, the advantage of redundancy one over redundancy two, three, etc. is lower every time. Inversely, the cost in hardware of a

digital circuit with port redundancies is higher every time. Therefore, a redundancy of one is appropriated tradeoff between reliability and overhead.

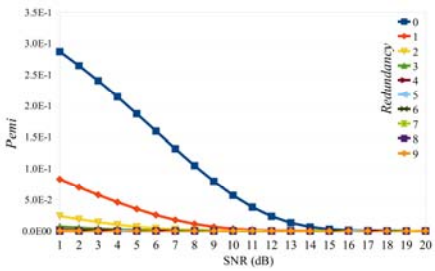

Figure 3. Error probability for a single gate with 0-9 port redundancies.

IV. Turtle Logic: redundant digital design for ICs

The design proposal presented in this work consists in replicate the ports one time using the complementary data for the devices has to reject noise in common mode. The logic functions are implemented such that the consistency of all redundant inputs is checked. In case of discrepancy, the output of the gate holds its previous values, hence avoiding the propagation of incorrect inputs to the outputs. We call this concept Turtle Logic (TL) because the circuit mimic the behavior of the turtles in the nature, for example, when it is in danger environment (noise for the circuits), it is remain in standby but does not died, and when the danger disappear the turtle continue with its normal live (for the case of the circuits, they continue with the correct functionality). To show the operating of TL design, we use a NOT gate with port redundancy of 1 and complementary data.

The circuit obtained at gate level is shown in Figure. 4 which has two possible cases:

- When the input ports have complementary values ($x_i != x_{ic}$), then, the TL NOT identifies the inputs as correct values and forces the complementary output ports driving the appropriate values according to the NOT function $x_o = not(x_i)$, and $x_{oc} = not(x_{ic})$.
- When the inputs have the same value ($x_i = x_{ic}$), TL NOT gate detects these values as an error. Thereby, the output ports of the system are forced to hold their previous correct values.

It has to be noted that when both inputs take simultaneously an incorrect value due to noise, the TL gate admits them as correct values, thus yielding an incorrect output. Nevertheless, the probability of this simultaneous event is very low when there is a statistical independence of the noise in redundant ports, as must been deduced of the Figure. 3.

V. Simulation results

In order to validate the improved robustness of the TL proposal Figure 3(b), was implemented a NOT gate with three methods: standard CMOS, MRF [3] and TL. The results shown in Table I are the result of SPICE simulations, using 90nm technology device models with a V_{DD} of 0.5V at temperature of 100°C. Thermal noise and flicker noise was generated in each transistor, as well as, shot noise in the power supply at each time step. All kind of noise generated were amplified 100 times respect to intrinsic noise of the 90nm technology, in order to emulate the behaviour of future technology with very noisy components.

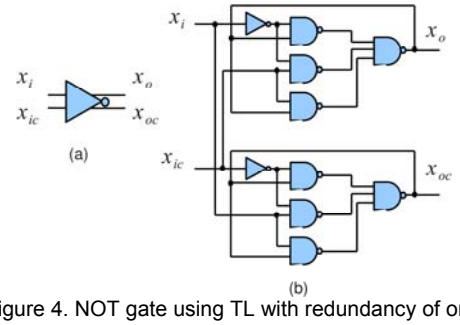

Figure 4. NOT gate using TL with redundancy of one as well as complementary data. (a) Symbol, and (b) Schematic view.

As reliability parameter to measure and compare the noise error robustness of these approaches is used the spurious signal (SS) factor [5], obtained better result than previous approaches as is shown in the SS column of Table I.

Logic		Port Redun.	# Gates	SS	
				x_o	x_{oc}
NOT	CMOS	0	1	8298	N. A.
	MRF	1	8	1580	2850
	Turtle L.	1	10	71	73

Table I. Comparative CMOS, MRF and Turtle Logic techniques for a NOT gate, using alternating 5,000 1's and 0's, with a period of 4ns.

VI. Conclusions

The reliability of a circuit might be improvement respect to the increment of redundancy of ports combined with Turtle Logic (TL) methodology. TL has higher overhead that conventional and MRF [2] approaches, but much better reliability. It requires additional settling time and may be slower than other techniques.

VII. Acknowledgments

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VIII. References

[1] International Technology Roadmap for Semiconductors, online. Available http://public.itrs.net.

[2] J. Von Neumann, "Probabilistic logics the Synthesis of Reliable Organisms from Unreliable Components", Automata Studies, C. E. Shannon and J. McCarthy, eds., Princeton Univ. Press, 1956, pp. 43-98.

[3] . Nepal, R. I. Bahar, J. Mundy, W. R. Patterson, and A. Zaslavsky, "Designing logic circuits for probabilistic computation in the presence of noise," DAC 2005, June 13-17, 2005, Anaheim, California, USA.

[4] . Garcia, A. Calomarde, F. Moll and A. Rubio "New redundant logic function design method for extremely high noise and low-voltage scenarios", DCIS2009, Zaragoza, Spain.

[5] F Moll and A. Rubio, "Spurious signals in digital CMOS VLSI circuits: a propagation analysis," Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on, vol. 39, no. 10, pp. 749–752, Oct 1992.