A Photovoltaic Three-Phase Topology to Reduce Common Mode Voltage

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***Abstract.*- At the present time most of the photovoltaic (PV) applications require to be integrated to the electrical grid. There are mainly two types of PV systems: with galvanic isolation (transformer) and transformerless. PV systems with low frequency transformer provide galvanic isolation from the grid. However, this transformer increases the losses, size and cost. On the other side, when the transformer is not included, the system can generate strong ground currents which are a function of the stray elements (capacitances). In this sense reducing the Common Mode Voltage (CMV), is an important issue in the design of power electronics converters for transformerless PV applications. In this paper a three-phase transformerless PV inverter with reduce common mode voltage is introduced. CMV is analyzed under different modulation schemes and an analysis of losses using a real model of the IGBT´s is included**

I. INTRODUCTION

At the beginning PV inverters were developed using three main stages: dc source (PV panels), converter (inverter) and grid connection (transformer and filter) [1]. The operation frequency of this transformer was around 50 or 60 Hz and provided galvanic isolation between the inverter and the electrical grid. Due its operation frequency, the transformer was expensive, big and heavy. In recent years transformerless PV inverters are becoming more and more widespread within the PV market. For this reason some researchers are every day more interested in to developing new systems that do not include transformer. This means that these new systems permits obtain best efficiency, a reduce size, good modularity and a reduced cost.

II. COMMON MODE VOLTAGE PROBLEM

PV panels are typically manufactured in layers involving glass, silicon semiconductor and backplane. The junction of these layers is covered by a grounded metallic frame in USA and only under certain conditions in Europe [2]. A PV inverter typically operates with a switching frequency around 7-15Khz, this high frequency can be reflected to the dc bus and produce leakage currents which flow through the frame and the stray capacitances [3]. These stray capacitances are between the earth and the metallic frame as can be seen in Fig. 1. The stray capacitances become an element of a resonant circuitry which consists of the PV panels, the ac filter elements and the grid impedance. The value of these capacitances depends on weather conditions, PV topology, PWM pattern, the material used in the metallic frame and the values in the passive elements of the converters. Some experiments have been done in order to determine approximately the value of these parasitic elements (under certain conditions) which is between 50-150 nF/Kw according with [4].

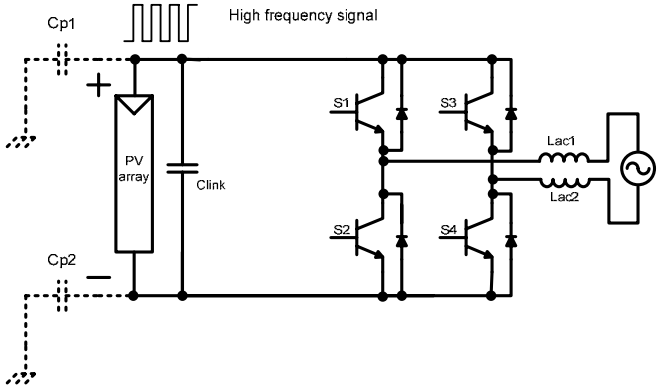

Fig. 1. Stray capacitances in a full-bridge single-phase PV inverter connected to the grid.

When leakage currents appear at the PV terminals (positive and negative) it comes up a problem related to the personal security. In this sense some standards have been established in Germany by DIN (Deutsches Institut für Normung e. V.). One of this standards is DIN VDE 0126-1-1: in this standard is established that the maximum leakage ground current should be 300 mA [5].

III. FULL-BRIDGE THREE PHASE INVERTER

In the case of single-phase PV systems, the output is an ac pulsating signal and in the input side is a smooth dc signal, this system can reach a power rate around 5 kWp [6]. Due this characteristic large dc capacitors are required which can reduce the lifetime and reliability of the system. On the other side, three-phase inverters have at the output a constant ac signal, this means that dc large capacitors are not needed. As an additional characteristic, the total power of the system can be increased, reaching values around 15kWp in the case of rooftop applications [6].

The most widely and simplest topology used in three phase systems is the full-bridge inverter, which consist in three legs, each leg with two transistors (IGBT`s). This topology is commonly used in applications like drivers for ac machines, filter equipments in the electrical grid, etc. The structure of this topology is shown in Fig. 2.

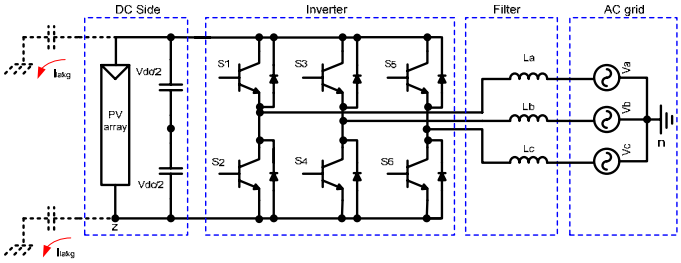

Fig. 2. Three-Phase Full-Bridge Inverter.

The performance of this inverter has been evaluated in different applications [7]-[9]. As aforementioned PV system can be designed using galvanic isolation or connecting the system directly to the electrical grid. This three-phase full-bridge inverter was evaluated in [10] for both cases. The results clearly show that this system is not suitable for transformerless PV applications. But in the case of [10] a specific modulation scheme was used. In order to understand how can affect the modulation scheme to the common mode voltage (CMV), some PWM (Pulse Width Modulation) techniques based on space Vector Modulation (SVM) have been proposed and analyzed in [11]-[12].

In the case of the topology shown in Fig. 2 which is the conventional two-level three-phase inverter, it is possible to obtain eight vectors by combining the state of the six switches of which six are the active vectors and two are the null vectors. As has been demonstrated in [13] the three phase system can be represented in the alpha-beta plane. Therefore, the eight vectors generated by the two-level three-phase inverter can be represented in the same way, as show in Fig. 3.

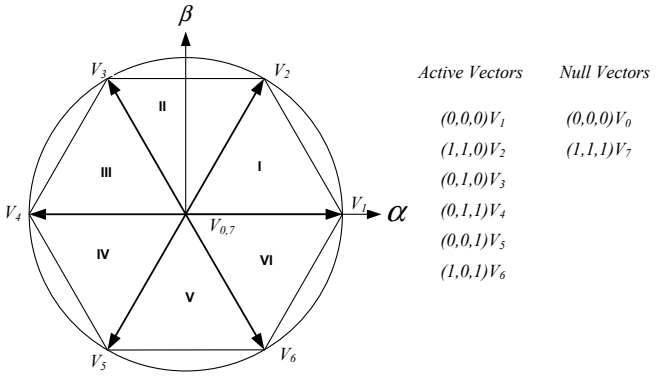

Fig. 3. .General Space Vector Modulation for three-phase inverters.

In the standard three-phase two-level inverter shown in Fig. 2, the CMV is defining as the average of the sum of voltages between the outputs and a common reference. In this case, the potential between the star point in the load and the "z" common reference for the three outputs, is the CMV which can be expressed by equation (1) [14]:

$$V_{nz} = \frac{v_{az} + v_{bz} + v_{cz}}{3} \qquad (1)$$

In this way, taking into account the equation (1), it is possible to obtain the common mode voltage generated by each space vector in Fig. 3. Table 1 shows the CMV generated by the eight space vectors.

TABLE 1
CMV GENERATED BY THE SPACE VECTORS IN A TWO LEVEL THREE-PHASE FULL-BRIDGE INVERTER

Vector	*CMV*
V_0 (0,0,0)	0
V_1 (1,0,0)	1/3 Vdc
V_2 (1,1,0)	2/3 Vdc
V_3 (0,1,0)	1/3 Vdc
V_4 (0,1,1)	2/3 Vdc
V_5 (0,0,1)	1/3 Vdc
V_6 (1,0,1)	2/3 Vdc
V_7 (1,1,1)	+Vdc

The common mode voltage is always jumping between 0 Vdc, 1/3Vdc, 2/3Vdc and Vdc at the switching frequency, this means that the ground leakage currents can appear at the PV terminals. In order to overcome this problem some SVPWM (Space Vector Pulse Width Modulation) strategies have been investigated and analyzed [12].

The idea in [12] is to evaluate the performance of this three-phase two-level inverter under different modulation strategies based on SVPWM. Some of these strategies have good performance regarding the CMV but on the other side, present some problems regarding voltage linearity, harmonic distortion factor and simultaneous switching. Some of these PWM techniques are shown in Fig. 4.

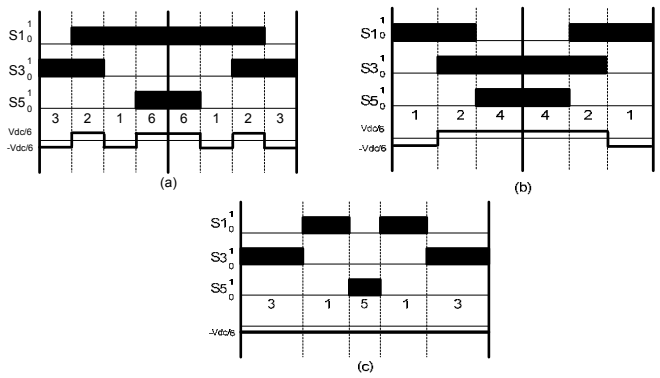

Fig. 4. Reduced Common Mode Voltage Space Vector Modulations, (a) AZSPWM1, (b) AZSPWM2, (c) RSPWM3 [12].

As a result of the evaluation in [12], it is possible to mention some well-defined characteristics of these strategies. For example, in the case of AZSPWM1 and AZPWM2 the CMV magnitude is reduced but the CMV frequency is high and also present high harmonic distortion factor. On the other case, the RSPWM has low CMV magnitude and the frequency is also low (around three times the grid frequency) but the modulation index is very low and the harmonic distortion is high. In order to attempt to improve the performance of two-level three-phase inverter, a new topology will be present in the next section.

IV. Proposed Topology

In this section, a new topology based on the full-bridge three-phase inverter is proposed. The inverter in Fig. 2, can be divided in two circuits, one to set the active vectors and another one to set the zero vectors. With this new characteristic a good performance regarding CMV has been obtained. The proposed topology can be seen in Fig. 5.

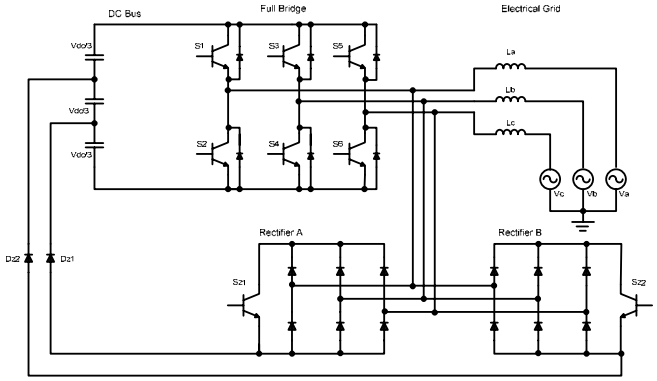

Fig. 5. Two-level Three-phase PV inverter topology.

In Fig. 5, *Rectifier A* introduces the null vectors when active vectors V_1, V_3 and V_5 are used. On the contrary, when active vectors V_2, V_4 and V_6 are used, the zero vectors are generated by *Rectifier B*. The aforementioned modulation strategy has been done by taking into account that the active vectors V_1, V_3 and V_5 and *Rectifier A* generate $1/3V_{dc}$ of CMV, and on the other hand the active vectors V_2, V_4 and V_6 and *Rectifier B* generate $2/3V_{dc}$ of CMV. The switching modulation sequence used in order to reduce the CMV magnitude is shown in Fig. 6 for sector I and sector II shown in Fig. 3.

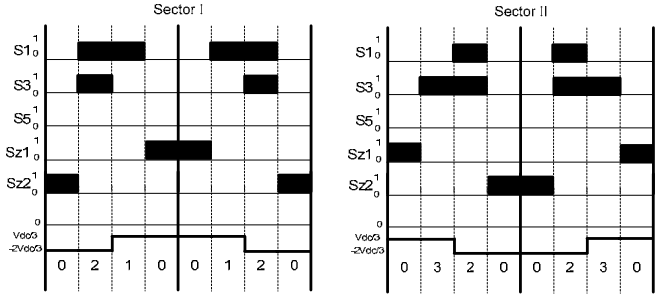

Fig. 6. Modulation strategy for FBTP ZVR (Full-Bridge Three-Phase Zero Voltage Rectifier) topology.

As can be seen in Fig 6, the space vector modulation is the commonly used strategy, but with the difference that the zero vectors are applied by means of the three-phase rectifiers. With this topology the modulation index can be maintained as in the conventional SVM. The dc bus is divided using three capacitors (or using three photovoltaic panels), in this way, a three-phase rectifier (rectifier A) can be connected to $1/3V_{dc}$ and the other one (rectifier B) can be connected to $2/3V_{dc}$. The modulation sequence is as follows: in sector I, when V_0 is applied to the load, all the switches in the full-bridge inverter are in the OFF state and the switch Sz2 is turn on, the CMV in this case is $2/3V_{dc}$. In the next step, in order to apply V_2 to the load, Sz2 should be turnoff and then S1 an S3 can be set to ON state and the rest of the switches in the full-bridge inverter are OFF, this situation keeps the CMV in $2/3V_{dc}$, after that in order to get a high modulation index, V_1 should be applied to the load. Here there is a change in the magnitude of the CMV from $2/3V_{dc}$ to $1/3V_{dc}$. Now a null vector should be applied, in this case all the transistors in the full-bridge should be turn off again, but now the zero voltage vector is applied using Sz1 which is connected to $1/3V_{dc}$, as a consequence the CMV is maintained in $1/3V_{dc}$. Until here the first half of the switching period is modulated, the other half should be modulated with the same idea. This idea can be extended to the rest of the sectors with the same results.

One thing that should be taken into account is that a short dead time should be introduced during the transition between the active vectors and the zero vectors in order to avoid a short circuit in the lower capacitors of the dc-link. Actually diodes Dz1 and Dz2 are used to prevent this kind of short circuits. The situation in which a short circuit can appear is depicted in Fig. 7, Fig. 8 and Fig. 9.

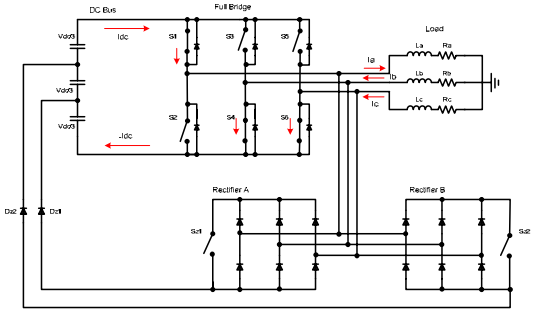

Fig. 7. State in which V_1 (1,0,0) is applied to the load.

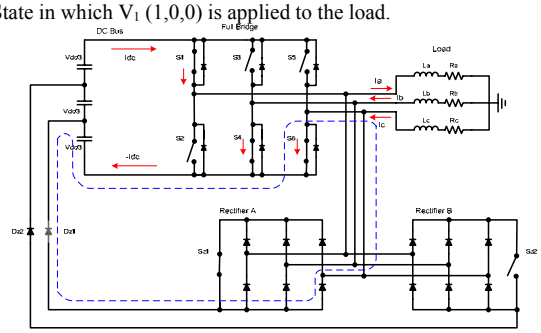

Fig. 8. State in which V_1 (1,0,0) and V_0 can appear at the same time (transitory).

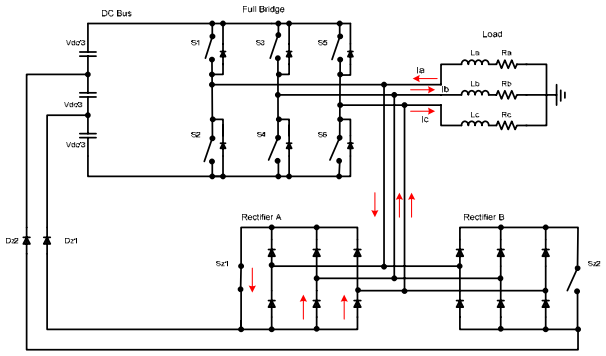

Fig. 9. State in which V_0 is applied to the load (free wheeling situation).

As can be seen, Fig. 7 in the normal operation as in two-level full-bridge inverter when V_1 is active, in this case the current is increasing in phase **a** and is decreasing in the other two phases, **b** and **c**, also this current comes from S1 and returns through S4 and S6. Fig. 8 shows the case in which a transient between V_1 and V_0 can produce a short circuit in the terminals of the lower capacitor of the dc-link. This is the case in which Dz1 is not considered and as a consequence, in order to avoid this short circuit it is necessary to use it, additionally as mentioned above, a short dead time between the turn off of the active vector and the turn on of the null vector should be included. Finally Fig. 9 shows the situation when V_0 is active, in this case current flows through the three-phase full-bridge rectifier and Sz1. As a conclusion of this analysis, all the switches in the three-phase full-bridge inverter should be opened before closing Sz1 and the same idea is applied when an even vector and Sz2 are used.

V. Simulation Results

The above topology was simulated and compared to the conventional two-level three-phase full-bridge inverter both under the same conditions. The parameters used in the simulations are listed in Table 2. All the simulations were performed using a RL load and in general under the same conditions in order to do an effective comparison.

TABLE 2
Simulation Parameters

Parameter	*Value*
V_{DC}	600V
Switching Frequency	5 Khz
R	15Ω
L	2 mH
Power	5kW
Output Current	12 Amp
$C_{P1.2}$	150nF

The simulations for the two-level three-phase full-bridge inverter were performed using a conventional space vector modulation. The results of these simulations regarding the output current, CMV and leakage current are shown in Fig. 10.

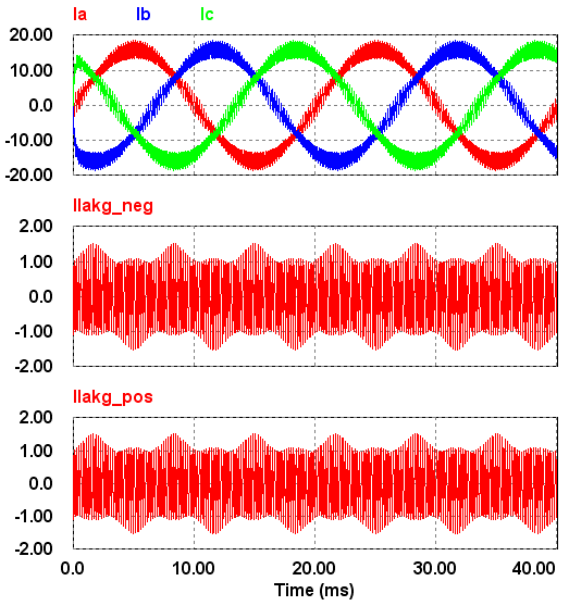

Fig. 10. Leakage ground current through parasitic capacitance in the two-level three-phase full-bridge transformerless inverter.

Fig. 10 shows the waveforms of the output current in the RL load for the three phases, also the leakage ground current in both terminals in the dc-bus. In order to see clearly the rms value of the leakage current, the FFT of these current was obtained. The frequency spectrum is shown in Fig. 11. As can be seen in this figure, the leakage ground current level is very high regarding to the standard DIN VDE 0126-1-1 which establishes the maximum limit in 300 mA. This means that this inverter is not suitable for transformerless applications

Simulation results for the proposed topology are shown in Fig 12 in which the output current for the three phases and the leakage current in both terminal of the dc-bus are depicted.

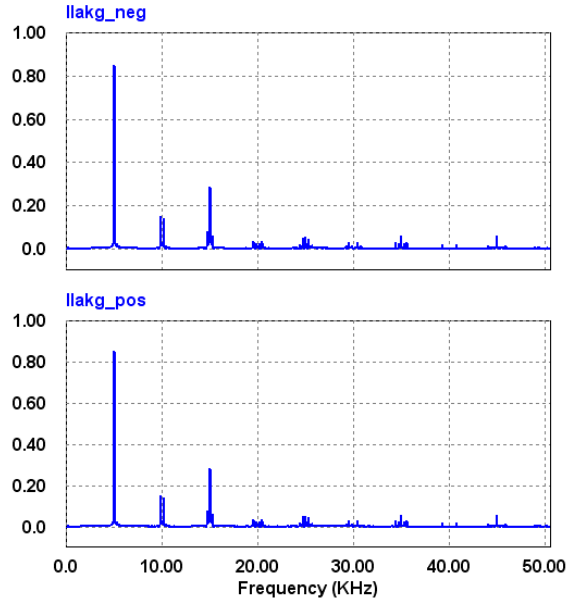

Fig. 11. Leakage ground current through parasitic capacitance in the two-level three-phase full-bridge transformerless inverter.

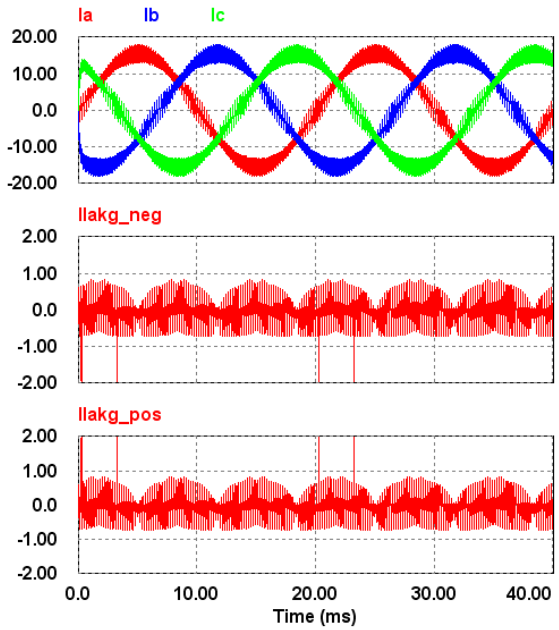

Fig. 12. Leakage ground current through parasitic capacitance in the proposed transformerless inverter.

As can be seen in Fig. 13 the frequency spectrum shows that the magnitude of the leakage current at the switching frequency is around 280 mA which is below the limit established by DIN VDE 0126-1-1 standard. This means that this three-phase transformerless inverter can be considered in grid connected PV applications. In the case of the efficiency of this proposed topology it is clear that the number of the components was increased, this means that the conduction and switching losses are higher than in the conventional two-level three-phase inverter, as a consequence the efficiency will be lowest.

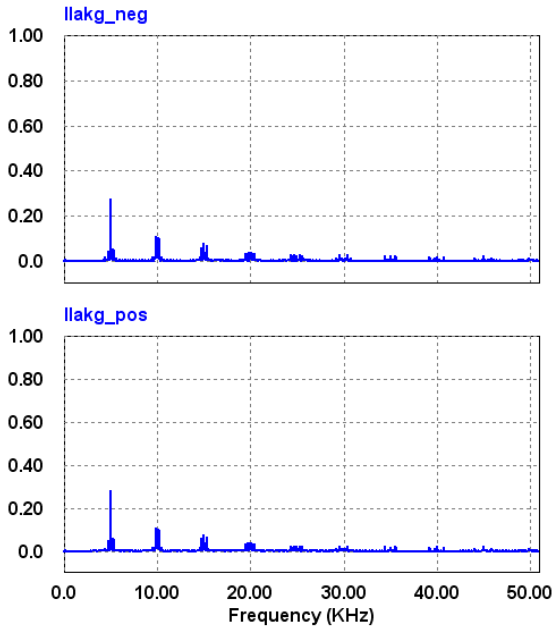

Fig. 13. Leakage ground current through parasitic capacitance in the proposed transformerless inverter.

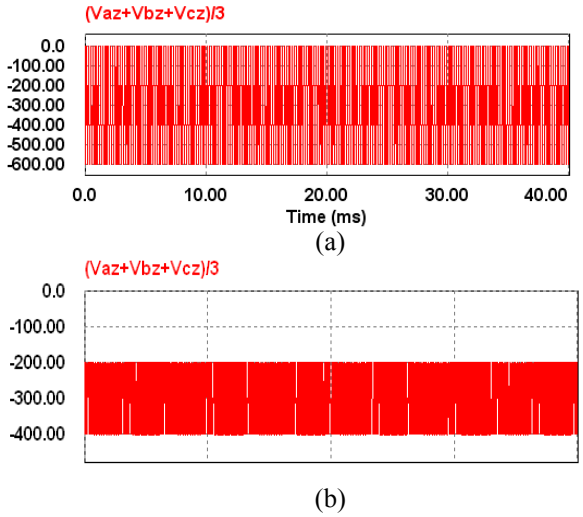

Fig. 14. Common mode voltage in both transformerless inverters: (a) Conventional two-level three-phase inverter, (b) proposed topology.

Fig. 14 shows the behavior of the CMV in both transformerless inverters, it can be seen that in the first case, the common mode voltage goes from 0 Vdc to -600 Vdc, while in the case of the proposed topology the dc voltage is changing only between -200 and -400.

As can be seen in Fig. 14(b), some glitches appear in some states during the simulations, thus the frequency seems to be higher than the first one.

Some simulations using the Thermal Module from PSIM were performed. In these simulations a real model of the IGBT's has been used. From the simulation results it can be said that the difference regarding the efficiency between these two inverters is around 2 to 3%, taking into account the switching and conduction losses in all switches and diodes.

VI. Conclusions

Renewable energy sources are becoming more and more widespread around the world, including solar energy. PV applications in the range of 5-15kW are of great interest in the case of three-phase grid connection. The present and the future in this kind of applications are transformerless inverters. In this paper an alternative solution for three-phase transformerless applications has been carried out.

A comparison regarding CMV and losses has been done based on which it can be concluded that the conventional three-phase full-bridge inverter is not suitable for transformerless applications due to its high leakage current. This converter is only functional in PV applications if there is a galvanic isolation between the grid and the inverter (low frequency transformer) or if the isolation is located between the dc-bus and the inverter (high frequency transformer). The problem is that the transformer increases the losses, cost and size.

The alternative topology proposed in this paper, reduce the CMV magnitude and as a consequence reduce also the leakage current magnitude whereas the modulation index can be equal

as in the conventional three-phase inverter. The main disadvantage is the increase in the number of active components (diodes and switches), these additional active elements introduce new switching and conduction losses, as a consequence the efficiency is lower than in the conventional three-phase inverter. In spite of these disadvantages it can be concluded that this topology is a good alternative in the case of the transformerless PV applications.

As an additional conclusion it can be said that the SVM is a versatile modulation technique, therefore some other modulations strategies will be explored in a future paper.

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