Grid Synchronization for Advanced Power Processing and FACTS in Wind Power Systems

A. Luna*, J. Rocabert*, G. Vazquez*, P. Rodríguez*, R. Teodorescu** and F. Corcoles*
*Technical University of Catalonia, ** Aalborg University
luna@ee.upc.edu

***Abstract* – The high penetration of wind power systems in the electrical network has introduced new issues in the stability and transient operation of the grid. By means of providing advanced functionalities to the existing power converters of such power plants it is possible to enhance their performance and also to support the grid operation, as the new grid codes demand. The connection of FACTS based on power converters, such as STATCOMs, are also contributing to the integration of renewable energies improving their behavior under contingencies. However, in both cases it is needed to have a grid voltage synchronization system, able to work under unbalanced and distorted conditions. This paper presents the discrete representation and performance of three PLL's structures, designed to work in that kind of situations. Their synchronization capability will be tested in different scenarios and their performance constraints will be established according to the Grid Code Requirements (GCRs)**

I. INTRODUCTION

The classical electricity infrastructure is moving towards a distributed power generation system, where the renewable energies, especially wind energy, are becoming important players. The increasing heterogeneity of the network has reinforced the already existing concern about power quality and the grid stability. As a consequence, the grid connection standards are becoming more restrictive in response to the transmission system operators (TSO) demands, that ask for more reliability [1].

In the challenge of integrating such different technologies the inclusion of power electronics converters, as an interface between the generator systems and the net, has permitted the development of power control strategies that extends their capability to interact with the grid under faulty scenarios [2].

For instance when FACT's functionalities are implemented at the grid side converters of wind turbines, taking advantage of the existing power converters, the generation system is able to support the grid voltage in case of sags. Moreover, an improvement of the Fault Ride Through (FRT) capability can be also reached in such systems with these functionalities. The installation of STATCOMs, devoted to support the grid and to enhance the FRT of entire wind farms, is also a good example of the improvements that advanced power processing is providing to the integration of renewable energies.

In all these applications the grid voltage synchronization capability has gained lately a great importance, as a good synchronization under balanced and unbalanced is needed [3]-[4].

Nevertheless, having a good synchronization permits not only a good monitoring of the grid voltage phase and amplitude, or enhancing the capability of injecting power into the grid. A good PLL can provide further advanced functionalities to the control system, as it is the case of the islanding detection mode for wind farms [5] or, as it is mentioned in [6], for getting the current harmonic reference for active filtering applications. In a nutshell, the possibilities that an accurate grid synchronization method offers are summarized in Fig. 1.

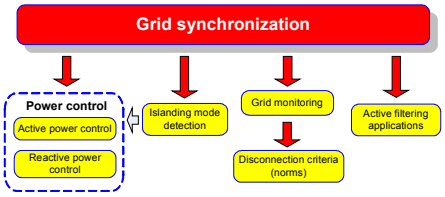

Fig. 1.- Grid synchronization applications

In this paper three solutions for that topic, based on the following advanced PLL's topologies will be tested and compared: Double synchronous reference frame PLL (DSRF PLL), Dual Sogi PLL (DSOGI PLL) and Three Phase Enhanced PLL (3PH EPLL PLL).

This analysis will be focused on their application for wind power systems or FACTS equipments devoted to support the operation of wind farms in case of grid faults. Hence, their performance in the estimation of the positive sequence variables in different scenarios will be discussed [7]-[9].

I. GRID SYNCHRONIZATION TARGETS OF GCR

In order to evaluate the response of the grid synchronization topologies under test a common performance requirement for all the structures have been established considering the implicit needs that can be derived from the GCR.

In the German standard it is stated that the voltage control must take place within 20 ms after the fault recognition by providing a reactive current on the low voltage side of the generator transformer to at least 2% of the rated current for each percent of the voltage dip, even the 100% of reactive power delivery must be possible if necessary.

A similar condition is given in the Spanish grid code, where the wind power plants are required to stop drawing inductive reactive power within 100 ms of a voltage drop and to be able to inject reactive power after 150 ms. Moreover the Spanish TSO requires also the injection of reactive power during 150ms after the clearance of the fault. Considering the aforementioned demands, in this work it will be considered

that the estimation of the voltage conditions shall be carried out within 20-25 ms.

II. DESCRIPTION OF THE THREE SYNCHRONIZATION SYSTEMS

Despite Synchronous reference frame PLL´s (SRF PLL) have a good response under balanced conditions their performance become insufficient in faulty grids and their good operation is highly conditioned to the frequency stability [10]. The topologies analyzed as follows are able to overcome the problems of the classical PLL, by means of building frequency, and amplitude adaptive structures, able to withstand in case of unbalanced systems, faulty and harmonic polluted grids.

A.- Double synchronous reference frame PLL (DSRF PLL)

The DSRF PLL (Fig. 2) is broadly discussed in [11] and [12]. In short, this algorithm enhances the dynamical response of a classical SRF PLL system, reinforcing its performance under unbalanced, and polluted conditions.

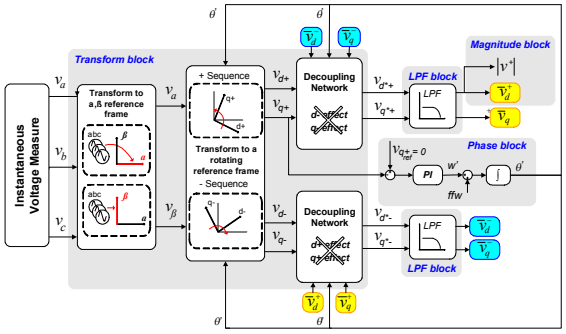

Fig. 2.- DSRF PLL block diagram

Its operation principle is based on the idea of subtracting the homopolar and the estimated negative sequence from the input, leaving just the positive sequence to the SRF PLL.

B.- Dual SOGI PLL (DSOGI PLL)

This synchronization system, presented in [13], is based on the implementation of two parallel SOGI [14]-[16].

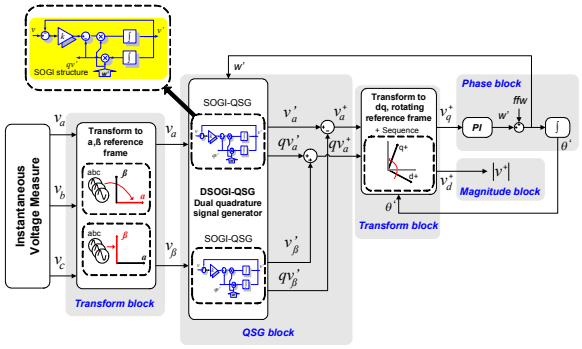

Fig. 3.- DSOGI PLL block diagram

This structure, depicted in Fig. 3, permits a good filtering of the input signal and, at the same time, behaves as a quadrature signal generator (QSG), something that facilitates the phase and magnitude detection of the positive sequence using a PI control block. This concept of PLL, based on second order integrators, has been implemented before for one phase systems, achieving satisfactory results [14] –[15].

C.- Three phase enhanced PLL(3phEPLL PLL)

This PLL (Fig. 4) is an extension of the one phase EPLL [17], a synchronization tool based also on the adaptive bandpass filter idea, for the three phase case [18].

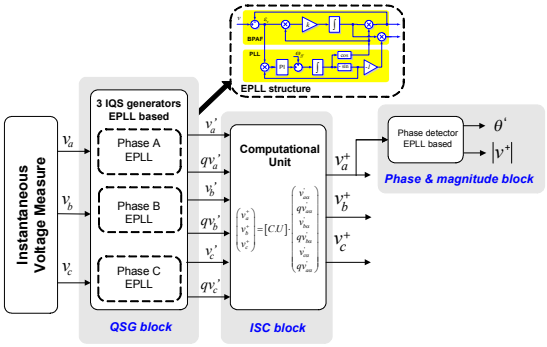

Fig. 4.- 3 ph EPLL PLL diagram block

The author adapts the solution for that topology implementing "the computational unit" [18] block, something that finally permits the positive sequence detection by using another EPLL.

III. DISCRETE IMPLEMENTATION

The discretization process will be described for the different building blocks presented previously, nevertheless those whose discrete equations are equal to its continuous representation, as the $\alpha\beta$ or $dq0$ transform, will not be discussed here.

A.- DSRF PLL discretization

This section will be more concerned about the phase locked loop and the lowpass filter discretization, whose representation are not direct in the discrete domain. As far as the DSOGI-PLL is using analogous blocks for detecting the phase and the amplitude the results obtained here will be considered also a part of the DSOGI discretization.

Phase block discretization

In the DSRF PLL the estimation of the angle comes from the integration of the estimated frequency, which corresponds to the output of a PI, as shown in Fig. 5.

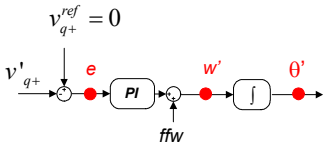

Fig. 5.- Angle estimation

The discrete representation of the PI can be divided in two parts, the proportional and the integral part. The first one is directly implemented by (1) & (2):

$$e[n] = v_{q+}^{ref} - v'_{q+}[n-1] \quad (1)$$

$$w'_{prop}[n] = k_p \cdot e[n] \quad (2)$$

While the integral part can be calculated as:

$$w'_{\text{int}}[n] = w'_{\text{int}}[n-1] + \frac{k_i T_s e[n]}{2} + \frac{k_i T_s e[n-1]}{2} \quad (3)$$

The total output of the controller is the addition of (2) & (3), as well as the feedforward signal (4):

$$w'[n] = w'_{prop}[n] + w'_{\text{int}}[n] + ffw \quad (4)$$

where $k_p = 4.44$ and $k_i = 246.74$.
Once the output of the PI gives the estimated frequency value the angle is obtained using another integrator

.

$$\theta'[n] = x[n] + \frac{T_s}{2}\omega'[n] \quad (5)$$

$$x[n+1] = \theta'[n] + \frac{T_s}{2}\omega'[n] \quad (6)$$

The resulting phase (5) is needed then at the 'dq' transform blocks and at the decoupling networks, something that justifies the one sample delay in the error estimation (2).

Lowpass filter block discretization

An IIR filter extracts the low frequency ripple from the *dq* positive and negative sequence estimation. The author [11] proposes a first order filter with a cutoff frequency, w_f, equal to the half of the grid one. As good results are obtained the same transfer function has been discretized to be implemented in the real setup (7) & (8).

$$y[n] = x[n] + \frac{T_s \cdot w_f}{2 + T_s \cdot w_f} \cdot u[n] \quad (7)$$

$$x[n+1] = \frac{2 - T_s \cdot w_f}{2 + T_s \cdot w_f} \cdot y[n] + \frac{T_s \cdot w_f}{2 + T_s \cdot w_f} \cdot u[n] \quad (8)$$

A generic notation in (7) & (8) is used due to the fact that four different filters are needed (Fig. 2), in any case '*y*' represents the filter output while '*x*' is the state and '*u*' the input.

B.- DSOGI PLL discretization

The referenced *Transform blocks* won't be analyzed in this section as again its discrete and continuous implementation are equal and it's available in further bibliography [13]-[21]. Further attention has to be paid at the *QSG block* and phase *Phase block* discretization.
QSG block discretization

The QSG in this PLL is based on two independent SOGI. This structure (Fig. 6) results in a linear system, so its discrete representation can be quite systematic once the state space is deducted.

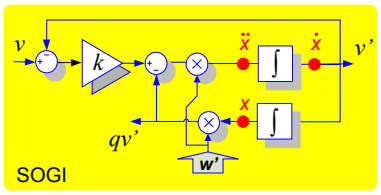

Fig. 6.- QSG based on a SOGI structure

The loop is described using two state variables, and its state space representation (9) has been built for offering the two in quadrature signals as the outputs.

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix} = \begin{bmatrix}0 & 1\\ -w'^2 & -k\cdot w'\end{bmatrix}\cdot\begin{bmatrix}x_1\\ x_2\end{bmatrix} + \begin{bmatrix}0\\ k\cdot w'\end{bmatrix}\cdot v \quad ; \quad \begin{matrix}x = x_1\\ \dot{x} = x_2\end{matrix} \quad (9)$$
$$\begin{bmatrix}v'\\ qv'\end{bmatrix} = \begin{bmatrix}0 & 1\\ w' & 0\end{bmatrix}\cdot\begin{bmatrix}x_1\\ x_2\end{bmatrix}$$

With a trapezoidal integrator the following discrete state space is obtained (10) - (11).

$$x[n+1] = A'\cdot x[n] + B'\cdot v[n]$$
$$y[n] = C'\cdot x[n] + D'\cdot v[n] \quad (10)$$

The T_s variable represents the sampling time of the discrete system while the value of *w'[n]* comes from the estimation made at the PLL block in each computation step, finally the value for the *k* gain is equal to $\sqrt{2}$ [13].

Phase block discretization

The frequency and phase detection are obtained in the same way as in the DSRF PLL case, something that stands out if the block diagrams of Fig. 2 and Fig. 3 are compared. However the PI parameters changes between both models, in this case $k_p = 2.22$ and k_i is equal to 61.68.

C.- 3phEPLL PLL discretization

This PLL uses another kind of QSG, not based on two $\alpha\beta$ components but on the three phase measurements, each one processed by an EPLL. The same structure is repeated later at the magnitude and phase block.

$$x_1[n+1]=\frac{\left(4+2\cdot Ts\cdot k\cdot w'[n]-Ts^2\cdot w'[n]^2\right)\cdot x_1[n]+(4\cdot Ts)\cdot x_2[n]+(2\cdot Ts\cdot k\cdot w'[n])\cdot v[n]}{4+2\cdot Ts\cdot k\cdot w'[n]+Ts^2\cdot w'[n]^2} \quad (11a)$$

$$x_2[n+1]=\frac{\left(-4\cdot Ts\cdot w'[n]^2\right)\cdot x_1[n]+\left(4-2\cdot Ts\cdot k\cdot w[n]'-Ts^2\cdot w'[n]^2\right)\cdot x_2[n]+(4\cdot k\cdot w[n]')\cdot v[n]}{4+2\cdot Ts\cdot k\cdot w'[n]+Ts^2\cdot w'[n]^2} \quad (11b)$$

$$v'[n]=\frac{\left(-2\cdot Ts^2\cdot w'[n]^2\right)\cdot x_1[n]+(4\cdot Ts)\cdot x_2[n]+(2\cdot k\cdot Ts\cdot w'[n])\cdot v[n]}{4+2\cdot Ts\cdot k\cdot w'[n]+Ts^2\cdot w'[n]^2} \quad (11c)$$

$$qv'[n]=\frac{2\cdot w'\cdot Ts\cdot(2+Ts\cdot k\cdot w[n]')\cdot x_1[n]+(2\cdot Ts^2\cdot w')\cdot x_2[n]+(k\cdot Ts^2\cdot w'[n]^2)\cdot v[n]}{4+2\cdot Ts\cdot k\cdot w'[n]+Ts^2\cdot w'[n]^2} \quad (11d)$$

QSG block - EPLL discretization

The EPLL presented in
Fig. 7, is slightly different from the original one [6], however the presented modifications permit a better computation, something reflected in [18] where Karimi-Ghartemani et al. are using this method to describe the state space variables.

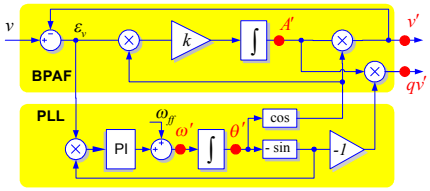

Fig. 7.- QSG based on a EPLL

It is worth to notice that an EPLL results in a nonlinear system [18], as can be demonstrated in (12)-(14), for this reason it is discretized in a different way than the previous DSOGI PLL.

$$\dot{A}'(t)=k\cdot e(t)\cdot\cos\theta'(t) \quad (12)$$

$$\dot{w}'(t)=-k_i\cdot e(t)\cdot\sin\theta'(t) \quad (13)$$

$$\dot{\theta}'(t)=w'(t)+\frac{k_p}{k_i}\cdot\dot{w}'(t) \quad (14)$$

The discrete representation of (15)-(18) gives the updates of the discrete states.

$$e[n+1]=u[n+1]-v'[n] \quad (15)$$

$$w'[n+1]=w'[n]-\frac{T_s\cdot k_i}{2}\cdot\left(e[n+1]\cdot\sin\left(\theta'[n]\right)\right)+\frac{T_s\cdot k_i}{2}\cdot e[n]\cdot\sin\left(\theta'[n-1]\right) \quad (16)$$

$$\theta'[n+1]=\theta'[n]+\frac{T_s}{2}\cdot\left(w'[n+1]+w'[n]\right)-\frac{T_s\cdot k_p}{2}\cdot\left(e[n+1]\cdot\sin\left(\theta'[n]\right)+e[n]\cdot\sin\left(\theta'[n-1]\right)\right) \quad (17)$$

$$A'[n+1]=A'[n]+\frac{T_s\cdot k}{2}\cdot e[n+1]\cdot\cos\left(\theta'[n+1]\right)+e[n]\cdot\cos\left(\theta'[n]\right) \quad (18)$$

To obtain the sinusoidal outputs of the EPLL, (19) and (20), operations are necessary. By means of these products two in quadrature signals are generated.

$$v'[n]=A'[n]\cdot\cos\left(\theta'[n]\right) \quad (19)$$

$$qv'[n]=A'[n]\cdot\sin\left(\theta'[n]\right) \quad (20)$$

In the EPLL studied in this paper the different parameters have been set to: $k_p = 5$, $k_i = 450$ & $k = 500$.

Computational unit block

As there are little changes, related to notation, regarding the genuine one it is worth to mention the specific equations used (21) - (23).

$$v_a^+=\frac{1}{3}v_a'-\frac{1}{6}\left(v_b'+v_c'\right)-\frac{1}{2\sqrt{3}}\left(qv_b'-qv_c'\right) \quad (21)$$

$$v_c^+=\frac{1}{3}v_c'-\frac{1}{6}\left(v_a'-v_b'\right)-\frac{1}{2\sqrt{3}}\left(qv_a'-qv_b'\right) \quad (22)$$

$$v_b^+=-\left(v_a^+ + v_c^+\right) \quad (23)$$

These operations are computed using each discrete state of the input variables, therefore its discrete representation is equal to the continuous, and though (21) - (23) can be directly implemented by code.

Phase and magnitude block

(15)

This element is another EPLL that estimates the phase and the magnitude of the fundamental component. Its discretization is equal to the last one, but the outputs, are the positive sequence magnitude and phase, that corresponds directly with the states θ' and A'.

IV. PERFORMANCE EVALUATION

Six representative faulty and have been presented to the DSRF PLL, DSOGI PLL and 3phEPLL PLL according to the experimental fault patterns extracted from [8]-[9].
In all tests the same pre-fault component has been used:

$$V^+=100\angle 0^\circ;\quad V^-=0\angle 0^\circ;\quad V^0=0\angle 0^\circ \quad (24)$$

TABLE I
PROPERTIES OF THE TESTING VOLTAGE SAGS

A Sag	B Sag	C Sag	D Sag
$\begin{cases} V^+ = 40\angle -40^\circ \\ V^- = 0\angle 0^\circ \\ V^0 = 0\angle 0^\circ \end{cases}$	$\begin{cases} V^+ = 73.\widehat{3}\angle -10^\circ \\ V^- = 26.\widehat{6}\angle 170^\circ \\ V^0 = 26.\widehat{6}\angle 170^\circ \end{cases}$	$\begin{cases} V^+ = 67.37\angle -5.7^\circ \\ V^- = 27.81\angle 2.2^\circ \\ V^0 = 0\angle 0^\circ \end{cases}$	$\begin{cases} V^+ = 67.37\angle -5.7^\circ \\ V^- = 27.81\angle -177.8^\circ \\ V^0 = 0\angle 0^\circ \end{cases}$

Positive, negative and homopolar sequence vectors during the fault conditions for the different sags

The fact that the power source is not generating exactly three shifted sinewaves, something comprehensible, will produce also some negative sequence component in the input signal. However this little unbalance also appears in real power systems, so this is not hindering the reliability of the test.

V. EXPERIMENTAL RESULTS

'A' Type Sag test

This kind of distortion usually appears when a three phase fault occurs. The high currents generate a great drop in all voltage values, as well as phase jumps due to the change in the line impedance. This phenomenon can be also found when high power machines are suddenly connected to weak grids. In any case either the DSRF PLL or the DSOGI PLL perform great results (8.e & 8.i) as both permit a very fast detection of the positive sequence (less than two cycles). This is not the same for the 3phEPLL that experiments great overshooting in

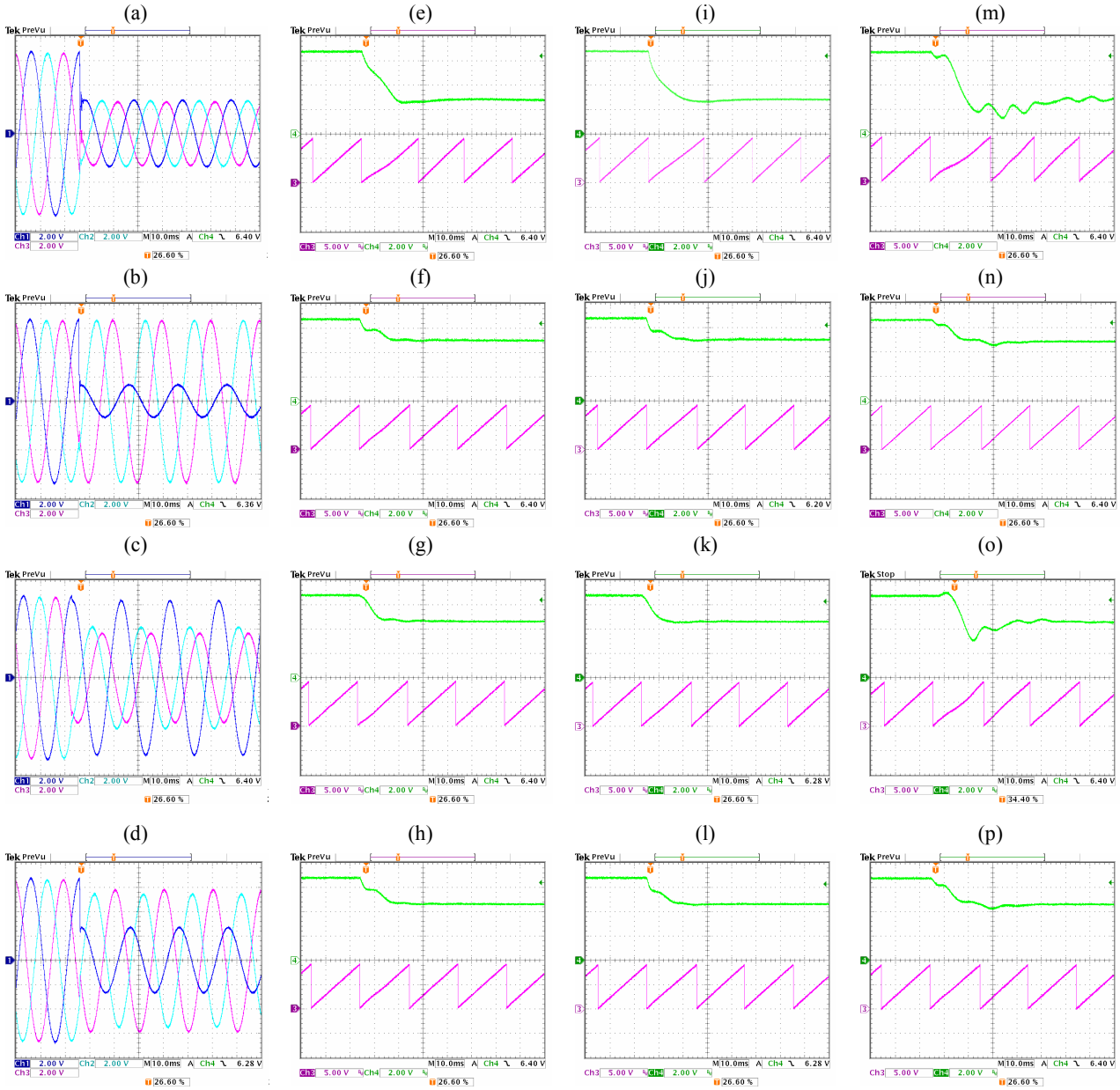

Fig. 8.- Amplitude and phase estimation of the 3 tested PLL's in case of 4 type of sags. (a) – (d) Input signal (V) ; (e) – (h) Amplitude (V) and phase (rad) detection for the DSRF PLL; (i) – (l) Amplitude (V) and phase (rad) detection for the DSOGI PLL; (m) – (o) Amplitude (V) and phase (rad) detection for the 3phEPLL PLL. Scaling factors: Amplitude = 1:150; Phase = 1:7.

the amplitude (8.m), also affecting deeply the phase detection, which was already trying to follow the 40º of phase jump.

'B' Type Sag test

As the DSOGI PLL and the DSRF PLL are using $\alpha\beta$ components the dynamics of the positive sequence detection is not influenced by the homopolar one, even though in the 3ph EPLL this value is affecting the positive component estimation, so its dynamic is slower. However, this effect is attenuated by the 'computational unit' so finally the steady state is reached with no great delay.

'C'& 'D' Type Sag test

These sags represent phase to ground and a phase to phase shortcircuits, depending on the transformer configuration. This kind of distortions are more common than the previous, because they are the typical grid faults caused by lightning storms. Again good results are achieved overall, nevertheless the nonlinear QSG is playing against the 3phEPLL, as a slower stabilization stands out (8.o and 8..p). This is even more noticeable with the 'C' sag where the combination of the phase jump and the magnitude change of two phases introduce a more severe transient period. For each PLL the execution time of one cycle and the update time between each step have been indicated at
TABLE **II**, where the total time column corresponds to the addition of both magnitudes.

TABLE II
COMPUTATIONAL COST EVALUATION

Structure	*Execution Time*	*Update Time*	*Total Time*
DSOGI PLL	1.20μs	90 ns	1.29μs
DSRF PLL	2.01μs	120 ns	2.13μs
3phEPLL PLL	2.75μs	90 ns	2.86μs

Global burden time of one cycle of instructions for each PLL, considering execution and refresh time

VII. CONCLUSIONS

The results of this paper demonstrate how the $\alpha\beta$ transform and the bandpass filtering characteristic affect to the performance of the studied PLL's as it permits isolating the system from the influence of the homopolar component. This feature is available in the DSRF and in the DSOGI. On the other hand, the bandpass filtering feature, that the DSOGI and the 3phEPLL present, improve the results in polluted grids, besides a proper structure can act as a good QSG as well, something that enhances the general performance of the system.
Only the DSOGI is combining both functionalities, something that guarantees a better positive sequence synchronization. From this work it can be concluded that all the analyzed systems are able to comply with the requirements of the codes, in terms of dynamical response, however the DSOGI PLL is offering the best compromise between accuracy and computational cost.

ACKNOWLEDGEMENTS

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