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Electro-thermal coupling analysis methodology for RF circuits

Dídac Gómez*, Diego Mateo and Josep Altet
Electronic Engineering Department
Universitat Politècnica de Catalunya
Jordi Girona 1-3. Edifici C4 Campus Nord UPC
08034 Barcelona – Spain
*dgomez@eel.upc.edu

Abstract- In this paper we present an electro-thermal coupling simulation technique for RF circuits. The proposed methodology takes advantage of well established tools for frequency translating circuits in order to significantly reduce the computational resources needed when frequencies of interest are separated by orders of magnitude.

I. INTRODUCTION

The scaling down of CMOS technologies has enabled a whole system to be integrated on a single silicon chip (System on Chip, SoC), where digital and analogue parts coexist. Regarding the analogue section, manufacturing advances have allowed building Radio-Frequency (RF) systems with low cost CMOS technologies, e.g [1] implements a tri-band SAW-less WCDMA/HSPA transceiver in a 0.13µm CMOS technology working at about 2GHz.

On the other hand, thermal coupling mechanisms between devices and blocks in integrated circuits are known to happen at low frequencies: the bandwidth of the thermal signals is about 100kHz-1MHz, depending on the particular layout configuration [2]. Regardless of the frequency, thermal effects are of importance in both optimizing the performances and enhancing the characterization of RF circuits.

The first source of thermal interference between RF circuits is generated by the electrical DC biasing. Electrical DC signals generate DC temperature gradients on the silicon surface, being cause of device mismatch and performance degradation [3].

In addition to this, electrical AC signals also produce thermal increases that couple between blocks, generating performance degradation. This latter case is produced by the non-linear nature of the Joule effect: dissipated power is expressed as the product of voltage and current; and in terms of frequency, multiplying signals is equivalent to performing frequency mixing [4]. If we compare the spectrum of the electrical RF signals that a circuit processes with the spectrum of the power dissipated by its devices, a frequency mixing operation has been performed. E.g., experimental results are reported in [5], where a linear resistor within an Integrated Circuit (IC) is driven only with a sinusoidal signal of frequency *f*. In comparison, by using laser techniques, heat flux on the silicon substrate is also measured in [5] at two frequencies: DC and *2·f*. Thus, when a RF circuit processes a single-tone electrical signal, a DC temperature increase is generated, assuming that the *2f* component of the dissipated power is much beyond the cut-off frequency of the thermal coupling mechanism.

The situation is more complicated when the RF circuit is driven by a two-tone (or multi-tone) electrical signal. In this circumstance, intermodulation products appear and the dissipated power has spectral components at frequencies equal to the difference of the frequencies of the electrical signals that the RF circuit processes. When these intermodulating frequencies are inside the thermal coupling mechanism band, they generate low-frequency AC temperature signals [6], which couple to nearby blocks. E.g., [7] reports an example of narrow-band systems in EDGE/GSM bands (channel separation can be as small as 25kHz). In this situation, the low-frequency power dissipation generates AC temperature signals at frequency multiples of 25kHz that affect the dynamic electrical behaviour of the blocks on the chip.

This circumstance is also reported in [8]. In this work, RF circuits (1GHz) are driven with a two-tone electrical signal in order to generate a temperature increase at the difference of frequencies of the applied signals. As the power dissipated at low frequencies depends on the high-frequency electrical signals, the low-frequency temperature increase measurement is used to characterize and to obtain electrical figures of merit of the RF circuit. This fact is utilized in [8] to design a built-in non-invasive mechanism to characterize RF circuit through low-frequency temperature measurements performed by temperature sensors embedded in the same silicon die.

In this context, the goal of this paper is to describe a procedure suitable to perform electro-thermal analysis of RF and high-frequency circuits.

The description of the simulation procedure we have used is in Section 2, and an example is shown in Section 3. Section 4 presents some considerations about the presented technique and finally conclusions are given in Section 5.

II. PROBLEM STATEMENT AND PROPOSED TECHNIQUE

Traditionally, when the dynamic electro-thermal simulations of a circuit have been performed, transient spice-like tools were employed (e.g. [3]). Pure transient simulations have been extensively used to predict the dynamic thermal behaviour of circuits, either to obtain thermal settling times [3] or to estimate the circuit performance degradation for low-frequency analog circuits [9].

In RF circuits, electrical signals and thermal signals are at frequencies separated by several orders of magnitude from each other. This imposes the necessity of choosing a simulation time long enough to capture the lowest frequency of interest (probably the lowest AC components of the temperature). On the other hand, the simulation time step must be small enough to capture the highest frequency present in the system (the highest electrical frequency tone applied to the circuit). The combination of long simulation times and fine time steps leads to a significant computational cost in terms of memory and run times.

Furthermore, since we are interested in knowing the different spectral components of the temperature in order to feed-back its effect in nearby circuits, transient simulation requires the use of the FFT. Low numerical error is also required, which is difficult to achieve when there is a big magnitude difference between the harmonic components. Moreover, samples may require uniform temporal spacing. Altogether, the need for FFTs forces additional constraints to the transient simulation that lead to long simulation times or considerable numerical error [4].

The analysis of the thermal increases (DC and low-frequency signals) and its co-simulation with high-frequency electrical circuitry benefits from the use of advanced simulation techniques. The specific procedure must suit the underlying physics of the thermal coupling mechanism: As it is explained in the introduction, when the RF circuit is driven with a single-tone electrical signal, the temperature increase is the result of a direct down-conversion of the incoming RF signal to DC. This down-conversion mechanism is equivalent to the operating principle of a direct-conversion RF receiver [4].

Similarly, when the RF circuit is driven with a two tone electrical signals, DC and low frequency temperature increases are generated [10]. The spectral components of the temperature are at frequencies equal to multiples of the difference of frequency of the two electrical RF tones. This down-conversion mechanism is equivalent to that a low-intermediate frequency (Low-IF) receiver [4].

The description of phenomena in the thermal domain is mathematically equivalent to the well-known mixing mechanism used in electrical RF receivers, where both electrical signals at very high frequency and electrical signals at very low or even DC frequencies must be considered and simulated at the same time. Therefore, the co-simulation required in the thermal analysis case can be performed with an electrical simulator that uses the specific analysis developed for RF circuits to reduce computational resources (memory and running times).

Two techniques that can be applied for analysing a RF circuit are: shooting-methods and Harmonic-Balanced (HB) methods [10]. Both techniques are available in a variety of commercial simulators. In a shooting method, the simulator first searches for a periodic electrical behaviour of the circuit. Then, it computes the periodic response of the system. Its main advantage is that it can work with highly non-linear circuits and with circuits having sharp signal transitions (as digital gates). On the other hand, harmonic-balanced methods work directly in the steady-state frequency domain. It has been reported that this method is more adequate for weakly to moderate non-linear circuits and for circuits with distributed components [10].

The aforementioned tools have been developed for simulations in the electrical domain. In order to perform electro-thermal simulations and to extract the power dissipated by the different blocks and devices, we have adapted the procedure reported in [11]. Thus, we ensure that the power dissipation is obtained from the product of voltages and currents in the time domain (convolution in the frequency domain) and that the coupling from the electrical to thermal domain does not alter the electrical performances of the RF circuit due to the simulation test-bench.

III. EXAMPLE

We have designed an IC in a 65nm CMOS technology with a Low Noise Amplifier (LNA) operating at 2.45 GHz and a differential temperature sensor. The purpose of this design is to experimentally characterize the low-frequency thermal couplings that a RF amplifier generates [12].

As a proof of concept of the simulation strategy, we have constructed a simulation test-bench to predict the low-frequency sensor output voltage variation due to the thermal coupling generated by the high-frequency performance of the LNA. The block diagram of this co-simulation test bench is in Fig. 1.

The LNA is a low-power current-reuse topology suitable for wireless sensor networks, and its main specifications are listed in Table 1.

The differential temperature sensor is an adaptation of a classical Operational Transconductance Amplifier [13]. The core of the sensor is formed by two emitter coupled parasitic bipolar NPN transistors biased with the same collector current. Temperature gradients generated by the nearby active RF circuit imbalances their operating points. By processing the difference of the generated collector currents, the sensor's output voltage is designed to be proportional to the difference of temperature at the bipolar transistors locations. The main specifications for the differential temperature sensor are listed in Table 2.

The electro-thermal model used in this analysis comprises: i) the dummy circuitry used to extract the power dissipated by each LNA device as a result of mixing both the DC and AC (in this case RF) voltages and currents driving each device [11]. ii) a classical RC electrical model of the substrate thermal coupling. And iii), the dummy circuitry that couples the temperature increase to the temperature sensor. In this particular example, the temperature change of the bipolar transistor used as temperature transducer is obtained by coupling the voltage that models the temperature increase to

the NPN device through an ideal voltage-controlled voltage source (V_{offset}) to modulate the base-emitter voltage (V_{be}) of the NPN transistor according to its temperature sensitivity [13].

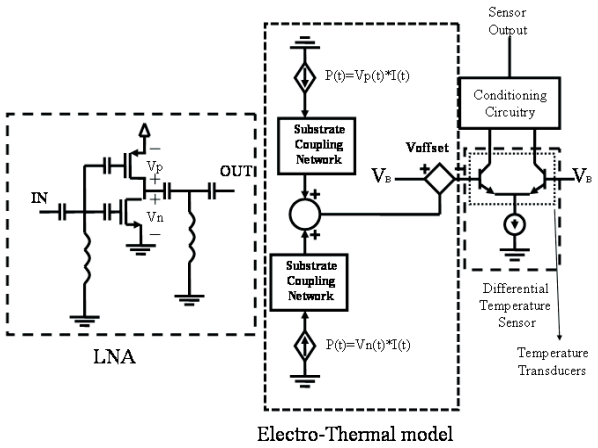

Fig1. Electro-thermal co-simulation testbench

Spec@2.45GHz	
Gv (dB)	21.22
S11 (dB)	-31
NF (dB)	4.80
CP1dB (dBm)	-18.12
IIP3 (dBm)	-8.13
PDC@1.2V (μW)	313.56
Technology	CMOS 65nm LP RF

Table 1. Summary of LNA specifications

Sensitivity (V/ºC)	0.89
Bandwidth-3dB (kHz)	38.37
PDC@1.2V (μW)	12.87
Technology	CMOS 65nm LP RF

Table 2. Summary of temperature sensor specifications

The simulator used was the commercially available SPECTRE RF. We have applied two tones with -18dBm power at the input of the LNA, spaced 10 kHz. We have preferred the Harmonic-Balance method as simulation engine over the shooting method. This circumvents the settling times of the electrical circuits during co-simulation, reducing the required computational resources even more.

Figures 2 to 5 show the result of a simulation. The first graph shows the spectrum of the LNA output voltage. The two main tones are at the same frequency as the ones applied to the LNA input. The other tones with lower amplitude are due to the non-linearities of the amplifier, which are situated 10 and 20 kHz away from the main ones. Fig. 3 displays the spectrum of the power dissipated by the NMOS transistor. It can be described with a Fourier Series whose fundamental frequency is 10 kHz (the difference of the two tones applied to the LNA input). These frequencies are the result of the down-conversion mixing of the high-frequency electrical signals present in the LNA. Fig. 4 shows the spectrum of the temperature increase at the temperature transducer location (the bipolar transistor). This temperature increase is computed from the thermal coupling of both LNA MOS transistors (we have neglected sensor self-heating) and it is a low-pass version of its dissipated power. Finally, Fig. 5 shows the spectrum of the temperature sensor output voltage.

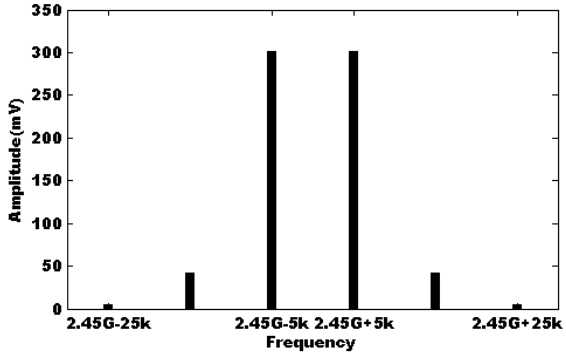

Fig 2. Spectrum at LNA output

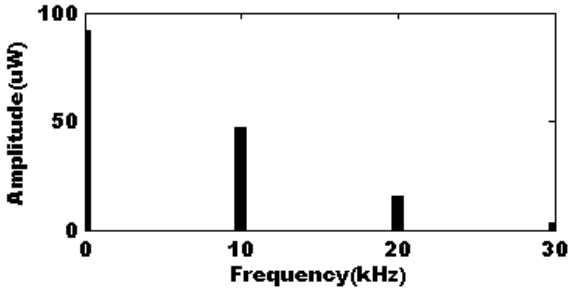

Fig 3. Spectrum of dissipated power at the NMOS transistor

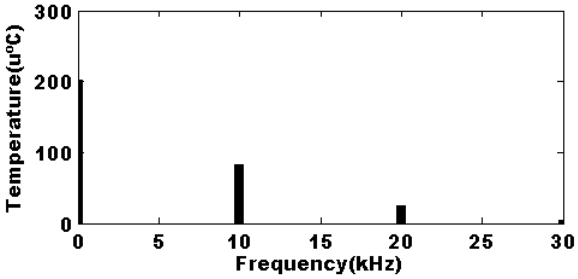

Fig 4. Spectrum at the transducer

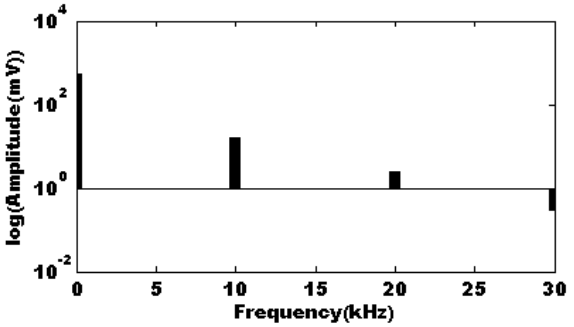

Fig 5. Spectrum at sensor output

The simulation time of the testbench (including the biasing circuitry for the LNA and sensor) is 1:05 minutes using single-thread capability. For benchmarking purposes, transient simulations were performed with input tones spaced 10MHz, 1MHz and 100kHz apart. For each one of those simulations a stop time equal to ten times the period of the spacing frequency was used ($T_{stoptime}=10/f_{spacing}$). The transient simulation times obtained are summarized in Table 3 in comparison with Harmonic-Balance simulation times. The lowest frequency spacing for the Harmonic-Balance simulations (10kHz) was

not considered during the transient simulations because the extrapolated simulation time is nearly two days.

Spacing frequency	Simulation Time with HB	Simulation Time Transient
10kHz	1m5s	----------
100kHz	1m5s	4h17m9s
1MHz	1m5s	27m48s
10MHz	1m5s	2m48s

Table 3. Comparison of simulation times for various frequencies

With the same testbench we could also analyze the sensor output voltage as a function of the power level of the two applied tones. The goal of this analysis is to study if high-frequency electrical figures of merit of the LNA (e.g. the 1dB compression point) can be extracted from the sensor low-frequency voltage variation (as reported in [8]).

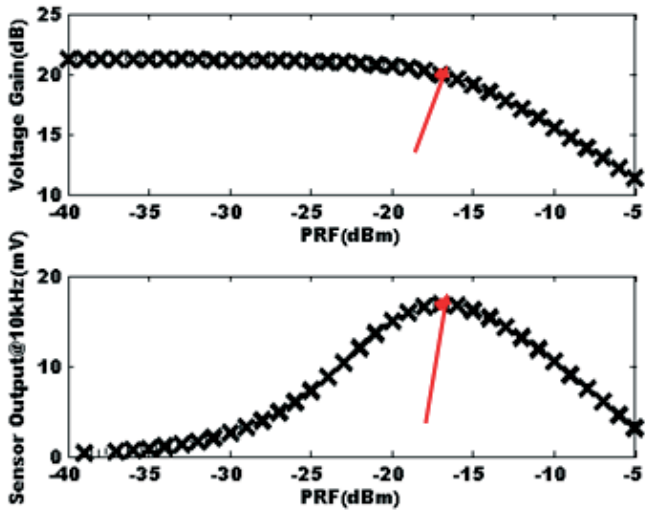

Fig 6. Top: Voltage gain of the LNA vs. input power, Bottom: Amplitude of the spectral component of the sensor output voltage at f=10kHz as a function of the power of the two tones applied to the LNA. (f_1=2.45GHz-5kHz, f_2 = 2.45GHz+5kHz)

The results are shown in Fig. 6. In this figure, the amplitude of the spectral component of the sensor's output voltage at f=10kHz is plotted as a function of the power level of the two tones (f_1=2.45GHz-5kHz, f_2=2.45GHz+5kHz) applied to the LNA input. As can be observed , there is a positive slope in the function that relates the amplitude of the sensor's output voltage with the LNA input power level. This relation is oberved until the LNA reaches saturation (maximum thermal coupling, marked with a red arrow in Fig. 6). This particular point can be related to the LNA 1dB compression point [8]. From there on, the LNA gain reduction and strongly non-linear operation provoke a negative slope in the function that relates the amplitude of the sensor output voltage with the LNA input power. The simulation time of Fig. 6 was just 40m 32s, which demonstrates an almost linear increase of simulation time with the number of simulation points.

IV. CONSIDERATIONS ON EXTRACTING THE POWER

In this section we analyze the error committed depending on the procedure used to obtain the power dissipated by the devices. Let us consider the small-signal model of a MOS transistor represented in Fig. 7. This simplified model considers the transconductance (g_m), the drain-source capacitance (C_{eq}) and the drain-source resistance (R_{eq}). For simplicity, the source is connected to a virtual ground.

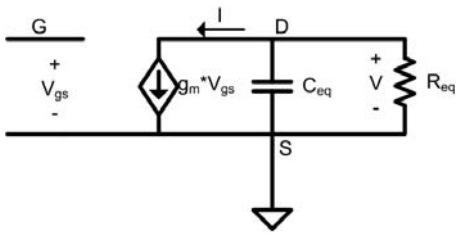

Fig 7. Small-signal model for error estimation

Only the active power dissipated by the MOS transistor will produce changes in the silicon surface thermal map, and it can be theoretically calculated as:

$$P_{real} = real(V \times I^*) \text{ (1)},$$

$$P_{real} = |g_m|^2 |V_{gs}|^2 real\left(\left(\frac{R_{eq}}{sR_{eq}C_{eq}+1}\right)^*\right), \text{ (2)}$$

where symbol "*" represents the complex conjugate. On the other hand, using the procedure indicated in Fig. 1, the dissipated power is estimated as:

$$P_{estimated} = V \times I \text{ (3)},$$

$$P_{estimated} = g_m{}^2 V_{gs}{}^2 \frac{R_{eq}}{sR_{eq}C_{eq}+1}. \text{ (4)}$$

Comparing (2) and (4), an error exists due to the difference in the last term, which is a first-order low-pass function. Thus, if the operating frequency ensures that $R_{eq}C_{eq}$<<1, equations (2) and (4) match with negligible error (the capacitance of the small-signal model can be neglected).

To analyze the dependence of the error as a function of frequency, let us consider the common source cascode amplifier with resistive loading represented in Fig. 8.

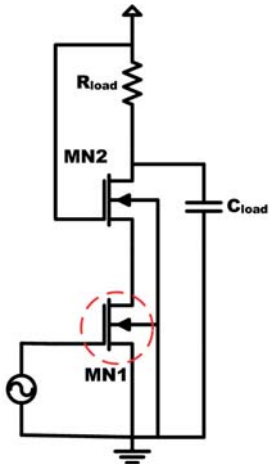

Fig 8. Testbench for error simulation

Fig. 9 shows the small-signal voltage gain of the amplifier versus frequency. As can be seen, it is a broadband design with a -3dB bandwidth of 2.9 GHz.

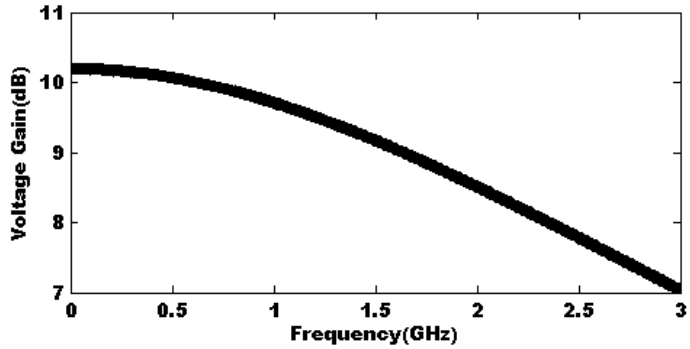

Fig 9. Small Signal Voltage Gain

Fig. 10 shows the magnitude of the power dissipated by the transconductor transistor (circled one in Fig. 8) obtained with the Harmonic-Balance engine and calculated either as V×I (red continuous curve in Fig. 9) and as Real(V×I*) (dashed black curve). As expected, both magnitudes are almost equal at low frequencies and they start to depart as the frequency increases beyond the cut-off frequency.

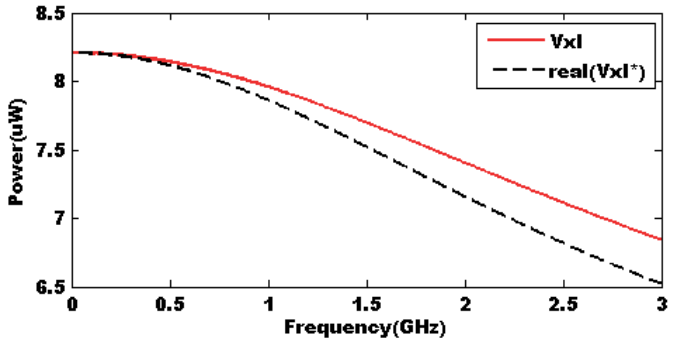

Fig 10. True dissipated power (black) and estimated dissipated power (red)

Fig 11, shows the percentage error between the true dissipated power and the estimation. The error increases as the frequency increases, but it is below 5% for the -3dB electrical bandwidth of the amplifier.

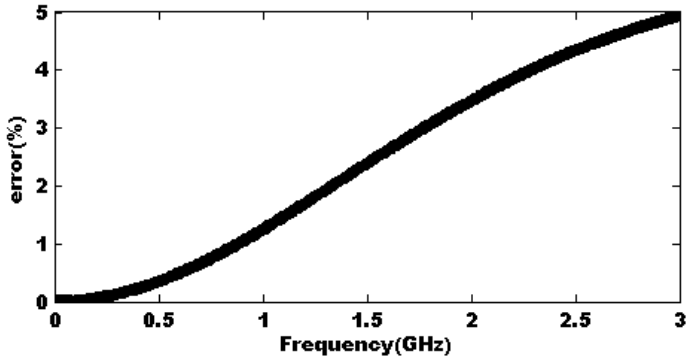

Fig 11. Error between power dissipations against frequency

One of the advantages of working with pure frequency domain simulation tools is that some of them allow calculating only the active power. Representing the complex voltage and current in rectangular form:

$$P = real(V \times I^*) \quad (5)$$

$$V = a + jb \quad (6)$$

$$V^* = a - jb \quad (7)$$

$$I = c + jd \quad (8)$$

$$I^* = c - jd \quad (9)$$

The real component of the dissipated power can be calculated as:

$$V \times I^* = ac - adj + cbj + bd \quad (10)$$

$$V^* \times I = ac + bd + adj - cbj + bd \quad (11)$$

$$real(V \times I^*) = 0.5 * (V \times I^* + V^* \times I) = ac + bd \quad (12)$$

This mathematical operation can be implemented conceptually with the block diagram of Fig. 12.

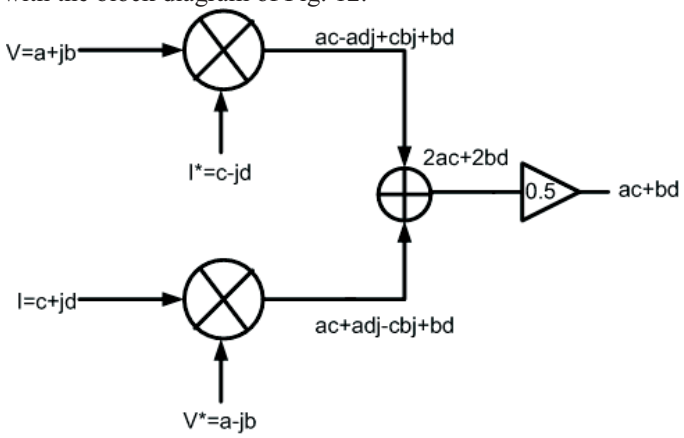

Fig 12. Conceptual block diagram of true power dissipation extraction

The block diagram of Fig 12 can be implemented in a pure frequency domain simulator since it is able to distinguish magnitude and phase components of a signal (or equivalently real and imaginary parts). The conjugation of waveforms can be done with an ideal 90º Hybrid [14] that is provided as behavioral block in certain design environments (e.g. Agilent ADS [15]). Figure 13 shows the percentage error between the true dissipated power and the estimation of the power with the block diagram of Fig. 12 applied to the circuit of Fig. 8 in the Agilent ADS environment. As can be seen, the error is practically negligible, and it is mainly caused by the numerical error of the simulator.

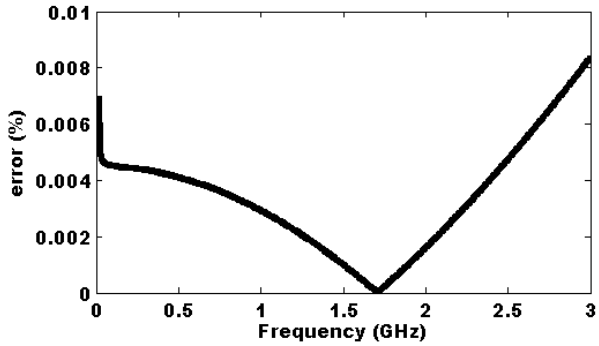

Fig 13.Error between power dissipations against frequency in ADS environment

V. CONCLUSIONS

In this paper we have presented a methodology for electro-thermal co-simulation of RF circuits. The methodology presented takes advantage of the simulation engines developed for RF design simulation. The proposed technique shows significant computational resources savings compared against traditional transient SPICE tools. Additionally, the cause of simulation error was demonstrated, and it has been proven that this error is sufficiently low within the frequency range of interest. It was also shown how in a pure frequency domain environment it is possible to reduce the simulation error to almost zero.

VI. ACKNOWLEDGMENT

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