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High-power Test Device for Package Thermal Assessment and Validation of Thermal Measurement Techniques

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Abstract—This paper describes the structure and thermal behavior of a high-power thermal test chip (up to 200 W/cm²) designed for power electronics package assessment, which has also been used for the validation of thermal measurement techniques. In particular, we show two application examples where the proposed device allowed the assessment of different power substrate technologies, and the validation of temperature measurement techniques used to characterize the high frequency behavior of circuits and devices in the frequency domain using the heterodyne technique.

I. INTRODUCTION

Among the electronic devices specifically designed for assessment purposes, thermal test chips (TTC) have been used as thermal validation tools in the field of thermal management from many years [1-7]. Basically, TTCs are devices with decoupled integrated heat sources and temperature sensors. They allow the evaluation of thermal resistance, thermal impedance, as well as package thermal design qualification. The basic principle of operation consists in applying a dissipated power (in the heat sources) and simultaneously measuring the associated temperature increase (using the temperature sensors). Different designs have been reported, containing different kinds and distributions of heat sources and sensors. Nevertheless, it is difficult to obtain detailed technical information about particular devices due to confidentiality reasons, because TTCs are in many cases devoted to the internal use of semiconductor companies. Due to the increase of the dissipated power densities in sophisticated ICs and packages, the importance of TTCs has also increased. In order to allow the comparison of the results obtained with different TTCs, industrial standards appeared and new designs tend to follow them, one of the most used being the JEDEC JESD 51-4 [8]. However, almost all the reported TTCs are devoted to the thermal characterization of packages for ICs. Consequently they reproduce the behavior of ICs, in particular in terms of maximum dissipated power, which is usually lower than that of typical power devices. One exception is presented in [9] where a thermal tester developed around a TTC working in the 100-200 W/cm² range is described and applied in the

processors packaging framework. Only a few references concern specific TTCs for the assessment of power electronics packages. These TTCs are based on active power transistors, such as the BJT used in the P432 test die and the VDMOS FET of the H029, both from ST-Microelectronics [10]. The absolute maximum DC dissipated power of both references is 40 W and 300 W respectively, but their fabrication process is relatively complex and expensive, as it is for functional power devices.

This work describes a high-power and low-cost thermal test chip specifically designed for the power electronics needs. It thermally behaves like typical vertical power devices (IGBTs, MOSFETs, fast recovery diodes, etc.), showing a high value of dissipated power on top, being the main heat extraction mechanism the conduction towards a heat-sink through the package or substrate. Section II describes the structure and fabrication details of the test chip. The versatility of the proposed TTC design is presented in Section III with two application examples of very different research fields: the thermal evaluation of power substrates and the validation of frequency-domain thermal measurement techniques.

II. THERMAL TEST CHIP STRUCTURE

The design of the proposed TTC follows the JEDEC JESD 51-4 guidelines. It has been implemented in standard 525 μm thick Silicon CMOS substrates (both, P and N type), and the chip lateral dimensions are 6 mm x 6 mm. Basically, it integrates a poly-Silicon heating resistor and a Platinum resistance temperature detector (RTD) using a low cost fabrication technology. The simultaneous implementation of heating and sensing resistors on top of the TTC requires an insulation mechanism to avoid electrical coupling between them. The best choice has been the deposition of a thin (35 nm) SiO₂ layer on top of the Si substrate (see Fig. 1). Both resistors are then deposited over this insulating layer. For simplicity reasons, all the tracks and pads are at the same level, avoiding multi-level metallization steps.

The heating resistor (R_H) is based on uniformly distributed poly-Silicon stripes. The stripes are defined by photolithography of the 350 nm poly-Silicon layer deposited over the thin SiO₂.

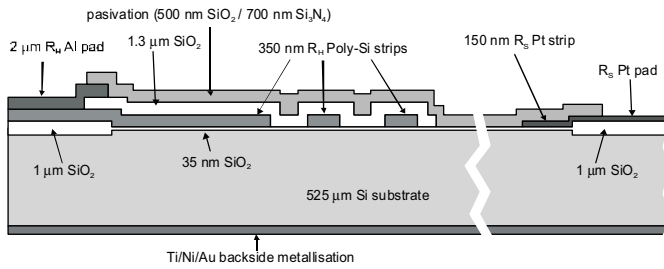


Fig. 1. TTC cross section scheme.

Their width is $20\ \mu\text{m}$ and the distance between stripes is $17.2\ \mu\text{m}$. All the stripes are connected in parallel and the total resistance value is around $60\ \Omega$. This technological solution avoids critical fabrication technology steps such as implantations, diffusions or gate oxides growth. In addition, though the heat is generated by individual poly-Silicon stripes distributed on the surface of the die, the heat-spreading inside the Si bulk allows considering an equivalent homogeneous distributed heat source on the top surface. This feature is very useful in order to develop simple analytical thermal models of the TTC for each particular application. In order to easily fix predictable power dissipation values, it is interesting to have a low R_H variation with temperature or, at least, to easily predict this dependence. In the present case, the measured R_H dependence with temperature is linear in a wide temperature range (up to 150°C), with a slope of $0.05\ \Omega/^\circ\text{C}$.

The definition of the sensing resistor (R_S) in the central part of the chip is based on the deposition of a $150\ \text{nm}$ thick Pt layer. The Pt layer is patterned by lift-off and its layout consists basically on a folded Pt track. The resistance value can be accurately measured using the 4-wire technique through the corresponding $120\ \mu\text{m} \times 120\ \mu\text{m}$ Pt pads. The R_S dispersion at ambient temperature is between $630\ \Omega$ and $775\ \Omega$, but the R_S sensitivity with temperature is very stable from one device to another ($0.95\ ^\circ\text{C}/\Omega$). In fact, the integration of RTD sensors has been reported as the best option for TTC applications [11]. The proposed device has been used in the standard temperature range of application up to 150°C . Nevertheless, it can also be used at high temperatures, up to 200°C , but in this extended operation range, a second order calibration of R_S with temperature must be used, instead of a simple linear fit. The total area taken by the RTD on the top surface is $0.7 \times 0.7\ \text{mm}^2$. This is a relevant fact, because in the central area of the die will not appear any dissipation. Consequently, the hottest area of the die is not located in the center and, for example, a difference of 2.5°C must be computed between the center and maximum chip temperatures, for a $50\ \text{W}$ dissipation. Nevertheless, for the most relevant applications this behavior does not represent a problem. Another deviation from the ideal behavior is related with the SiO_2 layer. This material shows a low thermal conductivity ($1.3\ \text{W/m.K}$), but its final thermal effect can be neglected due to its very low thickness (thermal resistance of the layer $7.5 \times 10^{-4}\ \text{K/W}$).

Fig. 1 depicts a cross-section of the TTC where all the elements described above are highlighted. Fig. 2 shows a top-view picture of a TTC soldered on a substrate under test. The Al wire-bonds of the resistors are clearly visible.

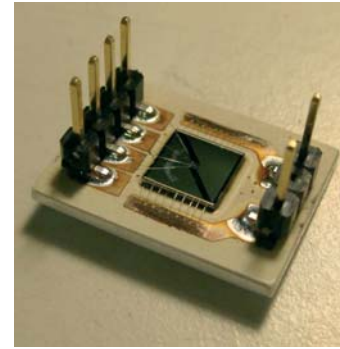


Fig. 2. Top view of a TTC assembled on an IMS substrate.

Notice that for accurate temperature determination, 4-wire measurements of the sensing resistor are imperative.

Although the proposed TTC was mainly designed for steady state analysis, in some applications it has also been used in transient operation. The dynamic limits of the device are mainly linked with the parasitic capacitance between R_H and R_S , showing typical values between $50\ \text{pF}$ and $100\ \text{pF}$.

III. APPLICATION EXAMPLES

As it was stated above, the proposed TTC can be used in a wide variety of research and engineering fields, including thermal characterization of packaging materials, validation of thermal models and simulations, thermal parameters extraction, thermometric calibrations, validation of thermal measurement techniques, etc. In this paper we present 2 different application examples of very different fields: characterization of power substrates and validation of temperature measurement techniques used to characterize the high frequency behavior of circuits and devices.

A. Thermal Evaluation of Power Substrates

Power substrates are critical elements of power modules, ensuring interconnection of the semiconductor devices, mechanical robustness and heat extraction capability. Depending on the power levels, several power substrate technologies are available, showing different thermal capabilities and cost [12]. Fig. 3 shows the schematic drawing of 3 test vehicles developed by assembling a TTC on 3 different kinds of power substrates: a standard FR4 PCB board, two kinds of Insulated Metal Substrates (IMS) and an Alumina (Al_2O_3) Direct Copper Bonding (DCB) ceramic substrate. The TTC is always soldered on a Copper pad using standard die-attach processes (SnAg solder alloy). This Cu layer shows a very low thermal influence (thickness between $70\ \mu\text{m}$ and $200\ \mu\text{m}$ depending on each substrate type). Below the Cu pad, there is a dielectric layer which is in fact the most critical material from the heat extraction point of view. The thermal conductivity value of the FR4 composite is around $0.4\ \text{W/m.K}$. The same parameter for the dielectric layer of the IMS shows values between $1\text{-}3\ \text{W/m.K}$ while for the ceramics of DCBs it can be between 15 and $200\ \text{W/m.K}$. Nevertheless, it is very difficult finding reliable and accurate values allowing the thermal assessment of different substrates, and direct measurement is imperative. The test vehicles of Fig. 3 allow a direct thermal comparison among different materials at exactly the same experimental

conditions. In addition, the thermal resistance between the chip and the backside of the substrate can be easily derived using standard electrical instrumentation. Fig. 4 summarizes the results corresponding to the quantitative thermal study of 4 power substrates: 1 FR4 PCB, 2 IMSs and an Al_2O_3 DCB. Continuous power values up to 67 W (187 W/cm^2) are injected in the TTCs, although the same tests have been also performed in transient conditions with 2.5 s power pulses. Fig. 4 shows the plots of the temperature increment (taken the reference at the substrate backside) versus dissipated power. As it can be appreciated, the curves are very linear, allowing an easy and direct analysis. The slope of these curves gives the chip-to-backside thermal resistance (R_{TH}). This value is basically related with the thickness and thermal conductivity of the different materials making up the substrate stack. As it can be appreciated, the best IMS power dissipation capability ($R_{\text{TH}}=1.94 \text{ K/W}$) is more than 2.5 times lower than that of alumina DCB substrates ($R_{\text{TH}}=0.77 \text{ K/W}$). PCB substrates are clearly restricted to low power applications ($R_{\text{TH}}=12.52 \text{ K/W}$). Direct evaluation and comparison between similar IMS technologies is also very straight forward. In this case, for example, IMS-2 shows a thermal resistance 0.42 K/W higher than IMS-1.

Similar analysis have been undertaken using the TTC, including the evaluation of multi-chip power modules with 2 TTCs on each test vehicle [13], identification of thermal conductivities [14] and specific heats [15], and validation of thermal simulations [16] and compact thermal models [17].

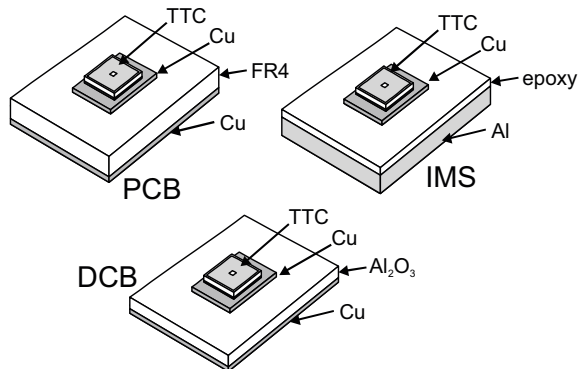


Fig. 3. Schematic drawings of the 3 kinds of substrates thermally assessed using the proposed TTC.

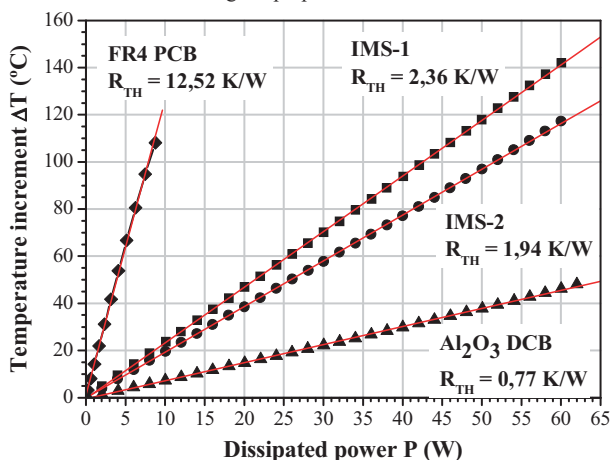


Fig. 4. Power substrates thermal characterization curves.

B. Validation of Thermal Measurement Techniques

A second application example, concerns the validation of temperature measurement techniques used to characterize the high frequency behavior of circuits and devices. An example is the named heterodyne characterization method [18-19]: If a linear circuit is biased with two electrical tones of frequencies f_1 and f_2 , due to the non linear nature of the Joule effect, power is dissipated at the frequency f_2-f_1 (named heterodyne frequency) even when no electrical signals are presented in the circuit at this frequency. The advantage of this biasing is that f_2-f_1 can generate a measurable temperature increase even when f_1 and f_2 are much larger than the cut off frequency of the thermal coupling in integrated circuits (e.g. Radio Frequency signals). The goal of the technique is to infer the electrical behavior of the circuit at the high frequencies f_2 and f_1 , by measuring the temperature increase generated near the linear circuit at the low frequency f_2-f_1 with a lock-in amplifier. The method was validated using the proposed TTC, where the frequency dependence of R_{H} was observed. The required temperature measurement was provided by an internal IR laser deflection (IIR-LD) thermometric set-up [20]. Basically, the amplitude of the output signal of this equipment is proportional to the temperature gradient inside the device under test.

In this example, the heating resistor was activated by the superposition of two sinusoidal voltages of frequencies f_1 and f_2 . The frequency f_1 was swept from 1 kHz up to 2 MHz, while the value of f_2 verified during all the measurement processes that $f_1-f_2 = 316 \text{ Hz}$. With this set-up, the temperature increase generated at 316 Hz depends on the real part of R_{H} at f_1 . Therefore, temperature measurements at 316 Hz are an observable of the frequency response of this device. Figure 5 compares the evolution of the amplitude measured at f_1-f_2 (square dots) as a function of the frequency f_1 with the frequency response of the resistance measured with a LRC meter (red line). Notice that the temperature-based measurement is expressed as $1/\text{Amplitude}$, where Amplitude is proportional to the IIR-LD set-up output voltage. As it can be seen, good agreement is observed between the low frequency temperature measurements and the frequency response of R_{H} .

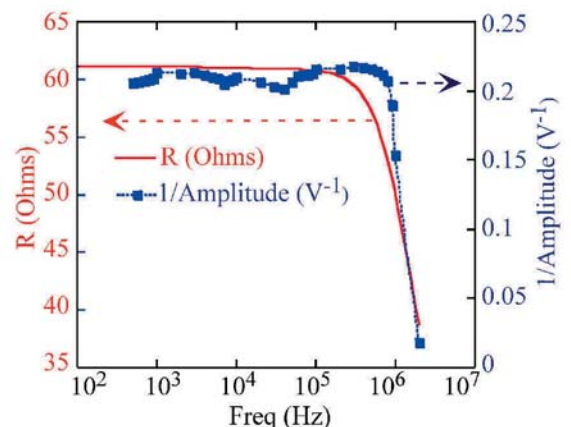


Fig. 5. Validation of a heterodyne characterization method. Thermally (dots) and electrically (line) measured frequency response of R_{H} .



V. CONCLUSIONS

The design and fabrication details of a low-cost and versatile thermal test chip have been described. The proposed device thermally behaves like typical power devices, with a power generation area on the top-side and heat dissipation towards the back-side by conduction. It allows dissipating high power densities (almost 200 W/cm²) using a poly-Silicon heating resistor distributed on the top surface. Simultaneously, the temperature on the centre of the top surface can be continuously measured using a calibrated Platinum resistor. The dissipation and temperature measurement circuits are decoupled and the thermal response of the device can be achieved with standard equipment (voltage and current sources or multimeters). The internal structure of the TTC is based on two consecutive deposition steps. In the first one the parallel poly-silicon strips along the top surface are defined by photolithography. A second deposition of Platinum defines the central sensing resistor by lift-off. As any critical diffusion or gate-oxide process is involved in the fabrication process, the device is relatively low cost, showing high fabrication yields. The versatility of the proposed TTC has been demonstrated in two application fields. First, the behavior of 3 kinds of power substrates (PCB, IMS and DCB) is quantitatively evaluated thanks to TTCs assembled on the substrates. Second, a temperature measurement techniques used to characterize the high frequency behavior of circuits and devices, based on the frequency-domain heterodyne method, has been validated using the TTC, as well as an IIR-LD equipment.

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