Design of Injection-Locked Frequency Divider in 65 nm CMOS Technology for mm-W applications

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Abstract—**In this paper, an Injection Locking Frequency Divider (ILFD) in 65 nm RF CMOS Technology for applications in millimeter-wave (mm-W) band is presented. The proposed circuit achieves 12.69% of locking range without any tuning mechanism and it can cover the entire mm-W band in presence of Process, Voltage and Temperature (PVT) variations by changing the Injection Locking Oscillator (ILO) voltage control. A design methodology flow is proposed for ILFD design and an overview regarding CMOS capabilities and opportunities for mm-W transceiver implementation is also exposed.**

Keywords: mm-W; prescaler; frequency divider; injection locking; locking range;

I. INTRODUCTION

Increasing memory capacity in mobile devices, together with the transition to wireless connections for consumer electronics and PC products, is driving the need for wireless equipment with data rates of up to 10 Gbits/sec. The worldwide 9 GHz mm-W unlicensed band (57 to 66 GHz) provides the opportunity for multi-gigabit wireless communication and it is a real opportunity for developing next generation Wireless High-Definition Multimedia Interfaces (WHDMIs).

The allocated bandwidth at 60 GHz varies from country to country as shown in Fig. 1. Mass production requirements coupled with the cost constraints of mobile devices result in a need to identify an alternative to existing, expensive Gallium Arsenide (GaAs) and Indium Phosphide (InP) technologies, currently used widely in mm-W Microwave Monolithic Integrated Circuit (MMIC) fabrication. RF CMOS 65 nm technology currently show very attractive performance for mm-W MMIC design [1]-[2], even if the technology environment is a critical issue in the design of frequency synthesizers operating at mm-W frequencies.

Recent developments in mm-W CMOS systems have begun to address the integration of building blocks to form transceivers. In addition to generic challenges such as high-frequency operation and low-noise design, the implementation of transceivers at these frequencies must deal with three critical issues related to the frequency synthesis, that are generation, division and distribution [3].

Millimeter wave frequencies have historically been costly to utilize. Recent advances in semiconductor technology provide an opportunity for this spectrum to become useable for broadband consumer applications within the next 2-3 years.

The aim of this work is to design a frequency divider for a PLL of a transceiver operating at mm-W frequencies in 65 nm RF CMOS technology; several issues will be faced, like Process, Voltage and Temperature (PVT) variations and power consumption, in order to select and design a frequency divider with high locking-range.

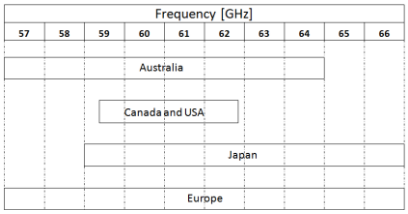

Figure 1. Spectrum available around 60 GHz

II. ARCHITECTURES FOR TRANSCEIVERS

In this section different transceiver architecture topologies are explored, from the frequency synthesis point of view.

A. Heterodyne Transceiver Architecture

In heterodyne architecture, the signal band is translated to "much lower" frequencies. The frequency translation is carried by means of a mixer which could be viewed also as a simple analog multiplier. The problems that affect heterodyne architecture are the "image-frequency" and the channel selection. Also, the effect of the half IF in a heterodyne receiver must be considered [4]. The trade off between sensitivity and selectivity in the basic heterodyne architecture often proves quite difficult to optimize with a single conversion stage. To resolve this issue, the concept of heterodyne can be extended to multiple down/up-conversions. The second down-conversion typically comprises both in-phase (I) and quadrature (Q) components of the signal. This technique allows skipping a second intermediate frequency stage. In Fig. 2, the heterodyne receiver architecture with double conversion is shown. Two LO signals at different frequencies are required, obtained, in this case, by frequency multiplication and division from a single VCO:

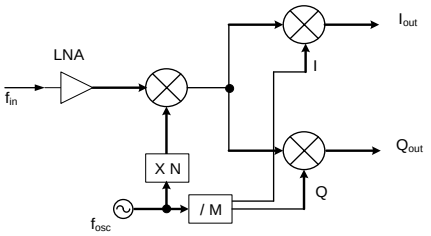

Figure 2. Heterodyne receiver

This architecture [3] must deal with the losses of the frequency multiplier. Depending on the choose of f_0, N and M, for a mm-W signal f_{in} = 64 GHz, the image lies at 45.7 GHz, experiencing only some attenuation if the front end must accommodate frequencies as low as 57 GHz [5]. The receiver in [6] uses f_0 = 29 GHz and N = 2, thereby suffering from an in-band image. For the receiver in [3] the image is suppressed by the selectivity of the antenna and the RF front end. Nevertheless, f_0 is still relatively high.

B. Homodyne Transceiver Architecture

In the direct-conversion or zero-IF architecture, the RF spectrum is simply translated to the baseband in the first down-conversion; important constraints related to this architecture consists in the channel selection (1) before the analog-to-digital conversion and, due to the noise-linearity-power trade-offs, the DC-Offset (2), because since the down-converted band extends to zero-frequency, extraneous offset voltages can corrupt the signal and saturate the following stages; 2nd and 3rd Order Distortion (3) that implies the need of high-linear LNA to attenuate RF mixer behaviour, Flicker Noise (4), that may be lowered by using active mixers and LO Leakage (5). In the simple zero-IF architecture, the LO frequency is equal to the input RF frequency. For frequency and phase modulated signals, the down-conversion must provide quadrature output, like the architecture shown in Fig. 3 [3], so as to avoid loss of information. The generation of I and Q phases of the LO at 60 GHz entails basically two issues: (a) quadrature operation typically degrades the phase noise considerably (because two core oscillators consume power and they do not improve each other's phase noise) and (b) the comparatively low tank results in serious design trade-off (phase-noise and wide tuning range).

LO frequency division also proves problematic in this architecture. Injection-locked and Miller dividers typically suffer from a narrow lock range if designed for 60 GHz. LO frequency division, also proves problematic in this architecture. ILFD and Miller dividers typically suffer, at the state-of-art, from a narrow lock range if designed for 60 GHz. It is important to note that a direct conversion is certainly the most convenient and simple conversion topology but at mm-W frequency it implies, along other challenges, that the frequency synthesizers needs frequency dividers that must operate at frequencies where the speed, sensitivity and selectivity, in terms of wide locking-range, are severe requirements, and where the PVT variations have a tremendous impact.

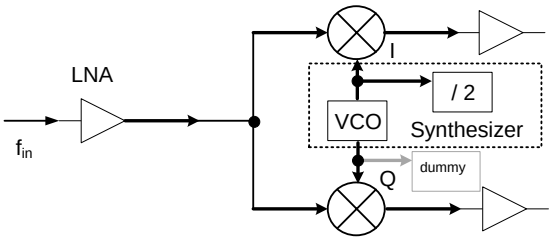

Figure 3. Direct Conversion Architecture

Heterodyne receiver architecture will be chosen, instead of direct-conversion one, if no other solution could be more feasible and commercially interesting at 60 GHz; but the aim of this work is pushing on this direction and contributing to implement frequency synthesizer (FS) for direct-conversion transceiver operating in mm-W band.

III. FREQUENCY SYNTHESIZERS IN MM-W BAND

FSs are essential part of wireless transceivers and often consume a large percentage (20–30%) of the total power [7]. A typical PLL-based FS comprises both high and low frequency blocks. The high frequency blocks, mainly the VCO and first stage of the frequency dividers, are the main power consuming blocks.

Up to now, other technologies have often been chosen over CMOS for designing the high frequency blocks in the 60 GHz band, while the low frequency blocks are commonly implemented by using CMOS technologies.

The typical FSs issues are frequency accuracy and stability, channel spacing, phase noise, sidebands (i. e., spurs) and lock time. Fig. 4 shows a basic FS architecture operating at mm-W frequency; it is very similar, as architecture, to lower FSs, except for the frequency divider, or prescaler.

The Voltage Controlled Oscillator (VCO) is the FS block in charge of the frequency generation. The VCO output frequency is:

$$f_{out} = f_0 + K_{VCO} \cdot V_C \qquad (1)$$

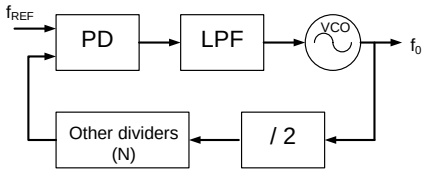

Figure 4. mm-W band PLL Arquitecture

where f_0 is the self-oscillating frequency of the VCO, i. e. the free-running frequency, K_{VCO} is the VCO gain and V_C is the VCO control voltage. The fundamental critical points in designing VCOs are to achieve a wide tuning range and as low as possible phase noise. At mm-W frequencies, reaching these requirements is a big challenge, due to the high operating frequencies and the PVT impact. It is possible to find in literature many papers regarding VCO

design in CMOS technologies for 60 GHz applications [8]-[9].

The remaining blocks of a FS are: the Phase Detector (PD) that works as an "error detector" in the feedback loop, the Low-Pass Filter (LPF) that suppresses high component frequencies of the phase detector output, allowing the DC value to control the VCO frequency and the frequency divider, which first stage, the divide-by-two divider or prescaler is the subject of this work

IV. CMOS Frequency Divider Issues in mm-W

When operating at mm-W, the most critical block in a PLL is the first frequency divider, which is usually a divide-by-two divider. The most critical requirement for this block in FS for mm-W transceiver is to ensure a wide locking range that covers properly the VCO tuning range, with the lowest possible power consumption. To cover the required VCO frequency range and PVT variations, the divider locking-range needs to be maximized. Usually this operation results in higher power consumption and larger VCO load [10]. The frequency divider has to work with the maximum operating frequency; it is possible to say that the fundamental task of a frequency divider is to "relax" the operating frequency of the following blocks, by lowering it; therefore, the first stage of the frequency divider chain is the critical design in a typical mm-W PLL system, because of its high-speed operation.

At high operating frequency, the trade-off between operating frequency and locking range of frequency dividers becomes more important. For mm-W broadband communication systems, by now it is clear that there is the need of wide locking range at high locking frequencies.

The RF frequency dividers can be categorized into digital and analog circuit implementations. The digital implementation of frequency dividers is based on flip-flop logic circuits [11]–[12]. The analog implementation of frequency dividers includes ring-oscillator-based injection locking [13]-[14], frequency regeneration [15]–[16], and resonator- based injection locking [17]–[18].

The flip-flop-based frequency dividers have the advantages of wide locking range and various division ratios, but usually suffer from high power consumption and low operation frequency. On the contrary, the analog frequency dividers are capable of high-frequency operation with low power consumption, but they usually suffer from small locking ranges. Lately, Injection-Locked Frequency Dividers (ILFDs) are very popular for mm-W applications because they feature the highest operation frequency and lowest consumption; the drawback is the limited locking range.

A. Frequency Dividers Topologies

Common Mode Logic (CML) frequency dividers have been quite used for frequency division in FSs, due to the wide locking range provided. But for high operation frequencies they show a limit due to the speed requirements. Furthermore, CML frequency dividers could be defined as "power-hungry", since its sample and hold stages require high power consumption. CML latch was first introduced in [19] and some modified latches can be found in [20]-[21]. The CML latches exhibit better performance than other latch structures. In general, a CML circuit consists of three main components, as shown in Fig. 5, which includes a pull-up load, the pull-down network (PDN) and a constant current source. CML is a completely differential and static logic. Due to its differential nature, it is highly immune to common mode noise and speed optimization in CML frequency dividers is a critical issue.

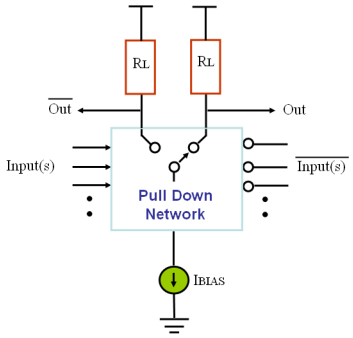

Figure 5. Generic CML Structure

ILFDs have captured the interest, for short-range high speed data communications around 60 GHz, mostly for its low power consumption, if compared to CML and Miller topologies, and for its high operation frequency. The big drawback of ILFD structure, when working at 60 GHz, is the limited bandwidth. Therefore it is imperative, at mm-W, to maximize the locking range of such ILFD divider, ideally to expand the 7 GHz of the WHDMI band (57 to 64 GHz). But, in reality, the locking range has to be higher than 7 GHz, in order to cover properly the required VCO frequency range and to overcome PVT variations. A possible solution could be increasing the amplitude of the injected signal; but this means increasing the power consumption, as well as the VCO load. Also, it could be possible to realize a ring-oscillator based ILFD, at expenses of a higher power consumption. Also, a series inductive peacking technique has been implemented [22], but at expenses of increasing critically the chip area.

B. PVT impact in sub-130 nm RF CMOS Technology

Regarding process variations, we must consider active and passive devices. Because unavoidable uncertainties during manufacturing process, integrated circuit suffer deviations from their nominal characteristic due to inter-die and intra-die variations. Inter-die variations affect all the devices of the same die simultaneously. Intra-die variations consist of both random and deterministic variations and cause a *non*-uniform distribution of the devices electrical characteristics. They are very critical in analog design, since they affect the matching between two nominally identical devices, leading to errors in differential structures. Usually, when designing a tuned circuit, like LC-VCO and ILFD as well, process variations of passive devices have a critical impact. PVT variations have a big impact in the behaviour of the VCO and the prescaler in sub-130 nm CMOS

technology. The inter-die variation patterns can be very systematic [23]: the cross correlation between different wavers can be more than 90% on average. In [24] has been demonstrated that the VCO tuning range variation is mainly caused by the variation in the MOS varactor.

V. Injection Locking Frequency Divider Design

In this section, ILFD topology will be studied and analyzed and a design is proposed. ILFDs have captured the interest of the designers for application in mm-W band, mostly for its lower power consumption and for its higher operation frequency, if compared to static CML topology. The big trade-off for ILFD at 60 GHz is the limited bandwidth, i. e. the locking range: this way the goal of this section is to introduce an improved ILFD topology that maximizes its locking range.

A. ILFD Design

Fig. 6 shows the schematic of the proposed ILFD in a 65 nm RF CMOS process. The bias transistor M_{bias}, i. e. the ILFD input stage, is used to provide both an input signal path and a dc bias path. If there is no input signal or if its amplitude (resulting in the injection current I_{inj}) is not large enough, the ILFD oscillates at its self-resonance frequency. This frequency may be changed by means of the varactor capacitance (C_v) that is changed through the control voltage (V_c). If the circuit of Fig. 6 divides correctly, transistors M_1 and M_2 switch at a rate of $f_{in}/2$ while M_{bias} injects a current at f_{in} with enough amplitude to inject-locking the ILFD.

Thus, in a manner similar to a single-balanced mixer, M_1 and M_2 translate the input to $f_{in} \pm f_{in}/2$, injecting the result into the tanks. This translation is accompanied by a conversion factor of $2/\pi$ [17] if the cross-coupled pair switches abruptly and the capacitance at node P is neglected.

As a result, the current injected into the tank at $f_{in}/2$ has a peak value of $(2/\pi) \cdot I_{inj}$, allowing to find an expression for the locking range of the oscillator in Fig. 6:

$$\Delta\omega_{f_{in}/_2} = \frac{\omega_n}{2Q}\eta\frac{2}{\pi} \qquad (2)$$

where η is the injection ratio equal to I_{inj}/I_{osc}, I_{osc} is the oscillation current, approximately equal to the tail current, ω_n is the resonant angular frequency of the tank and equal to $2\pi \cdot (f_{in}/2)$ when the circuit works properly. Q is the quality factor of the tank.

The continuous fine tuning varactor C_V is designed for the selected inductance value of the differential inductor L of 243.5 pH (DC value); the tank is sized to resonate at the self-oscillation frequency of the ILFD. The ILFD self-resonance frequency can be changed through the varactor control voltage. As a result of the analysis of the ILO steady-state, Fig. 7 shows how the ILFD self-oscillation frequency changes by means of a V_C sweep. The varactor has been sized to cover the overall band in presence of PVT variations:

$$\Delta C \geq 4\frac{f_{max}-f_{min}}{L\pi^2(f_{max}+f_{min})^3} \qquad (3)$$

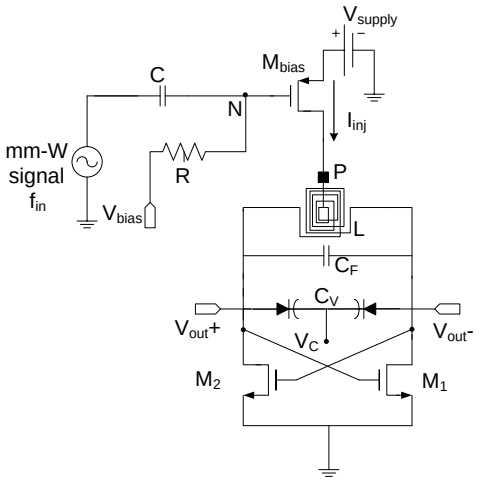

Figure 6. Proposed ILFD schematic circuit

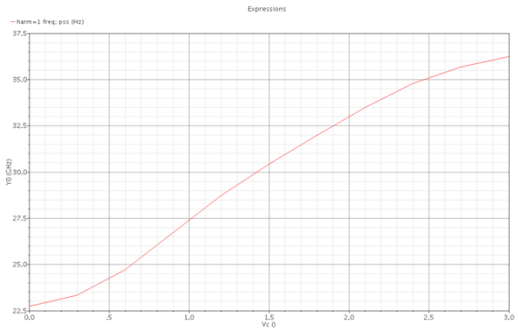

Figure 7. ILFD self-oscillation frequency range

where $\Delta C = C_{v,max} - C_{v,min}$; in this design, f_{max} = 35 GHz and f_{min} = 24 GHz. The selected varactor has a capacitance change ratio $C_{v,max}/C_{v,min} \approx 3$; so, the varactor has been sized in order that $C_{v,max} \approx 2\Delta C/3$; an additional ideal fixed capacitance C_F has been added in the schematic to take into account the parasitic effects of inductor, MOS transistors, interconnections and output buffer loading effect and to set the lower bound of the frequency range:

$$f_{min} = \frac{1}{2\pi\sqrt{L(C_{v,max}+C_F)}} \qquad (4)$$

L and varactor sizing have been done in order to achieve an optimal R_{pe} (parallel equivalent resistance of the tank) value: the value of R_{pe} is essential in order to get the parallel equivalent losses of the tank to design the cross-coupled NMOS pairs, determining its required transconductance g_m to guarantee the start-up oscillation. The worst case for start-up oscillation is the lowest value of R_{pe}, corresponding to the lowest ILFD self-oscillation frequency; this value is $\approx$ 100 Ω at 24 GHz, while at 35 GHz is around 600 Ω. There is a big trade-off between power consumption and locking range in a frequency divider design based on injection locked topology, i. e. related to the quality factor of the tank: in fact, it is possible to say that the power consumption is dominated by the losses of the VCO tank:

$$P_{loss} = \frac{R_S}{2\omega_0^2 L^2} V_0^2 \qquad (5)$$

where R_s is the series resistance of the inductor L and V_0 is the tank voltage swing. So, from (5), a low power consumption could be achieved by using small coil series resistances and/or large tank inductances. But it means achieving high Q. The locking range of the direct-locking scheme has been treated by many studies of injection locking of oscillators that have been published in the literature, leading to the conclusion that for larger locking ranges Q should be minimized (maximal R_s, minimal as possible R_{pe}, minimal L, consistent with (2)). For the proposed ILFD the value of Q at 35 GHz is 9.8, quite low, with the goal of maximize the locking range.

The ILFD design is completed with the sizing and biasing of the active section. The design process follows the same criteria presented in [25]. The PMOS bias transistor sizing is a key issue when the mm-W frequency is injected into it; in fact, in this ILFD topology the transistor acts also as a mixer (converting the injection signal to a signal at half/frequency) and it has not only bias functions. An optimal M_{bias} fine tuned size is W = 180 µm with minimum channel length. This size has been selected in order to maximize I_{inj}, i.e. the locking range, while keeping the bias function of M_{bias}. An optimal V_{bias} value is found around 0.75 V; it means a g_m = 23 mS.

B. ILFD locking range and sensitivity curves simulation

The injection locking simulation has been done in the time domain by calculating the ILFD output frequency corresponding to the positive zero volt crossings of the ILFD output signal. The proper setting of the transient analysis numerical control parameters is critical, in order to get convergence, accuracy and repetitibility of the results. In order to run a better simulation, in terms of accuracy, an ideal switch has been added in schematic of Fig. 6 between node N and decoupling capacitor C, in order that when the 60 GHz input signal is injected, the circuit has already achieved surely its steady-state oscillating and the self-oscillation frequency. In Fig. 8 the ILFD output frequency is reported for an input amplitude signal of 0.6 V (≈ 0 dBm) at 65 GHz and for a tuning Voltage Control V_C of 1.2V. Before the switch is closed, the ILFD frequency is set to its self-oscillation value (≈ 30.6 GHz); once the 65 GHz signal is injected, the ILFD output frequency changes to 32.5 GHz, which is exactly the divided-by-two input frequency. If the ILFD is not locking, when the input power is too weak and/or if the ILFD self-oscillation frequency is too far from the divided-by-two input frequency to get injection-locking, the ILFD output frequency is not constant in time, showing the behavior as reported in Fig. 9. By analyzing the amplitudes of the injected signal and the ILFD output after locking occurs it is possible to evaluate the conversion gain of the M_{bias} transistor that acts also as a mixer:

$$CG = 20dB\left[\frac{V_{out}(32{,}5\ GHz)}{V_{inj}(65\ GHz)}\right] \approx 15\ dB \qquad (6)$$

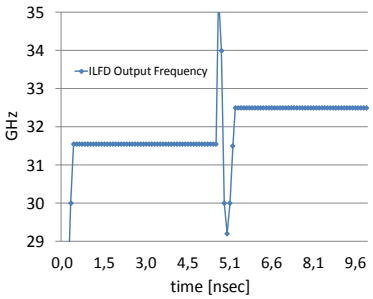

Figure 8. ILFD Output Frequency: input amplitude 0.6V (≈ 0 dBm) at 65 GHz, V_C = 1.2V

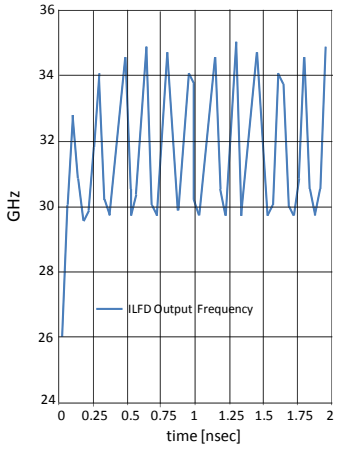

Figure 9. ILFD Output Frequency; no injection-locking state

C. ILFD Results

The ILFD drives a DC current corresponding to 6.3 mA for each cross-coupled transistor at 1.2V voltage supply. A locking range of 12.69% is achieved, around 60 GHz and without any tuning mechanism, since V_C is kept constant, for an input power of 0 dBm. The locking range is calculated as:

$$LR = \frac{f_{max} - f_{min}}{\frac{f_{max} + f_{min}}{2}} \qquad (7)$$

Generally, as seen in other works but as proved in simulation as well, the ILFD is hard to be locked for frequencies down to its self-oscillating frequency. This is a recurrent behavior of an ILFD.

As already mentioned, setting transient analysis simulation is not trivial. In order to show how much is influential the set-up of the transient analysis, in particular the time step parameter (t_s), two cases are reported: the first one regarding a sensitivity curve built by transient simulation with a lower t_s (10^{-6} psec.), the second one with an higher t_s (10^{-3} psec.). As reported in Fig. 10, two different transient simulation set-up provide different values for the self-oscillation frequency and for the sensitivity curves. The correct result corresponds to the smallest t_s value, even that this set-up results in longer simulation times.

Finally, the sensitivity curves of the proposed ILFD are calculated, through a parametric analysis by sweeping the amplitude of the injected signal and its frequency, by means

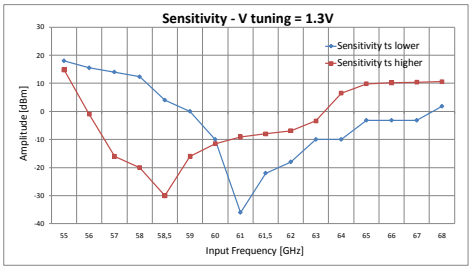

Figure 10. ILFD Sensitivity curves with higher and lower time step.

of changing the value of V_C, the overall mm-W band can be covered in presence of PVT variations, since the proposed ILFD can be locked from 47 GHz to 74 GHz for input power < 0 dBm, by setting properly V_C, as shown in Fig. 11, where the sensitivity curves for the V_C lowest and highest values are reported.

VI. CONCLUSIONS

In this work, a continuous tuning ILFD has been proposed for mm-W applications as well as a design methodology in order to maximize the locking range. The proposed ILFD achieves 12.69% of locking range around 60 GHz without any tuning mechanism, for 0 dBm input power. Also, by means of the continuous tuning varactor, it can cover the overall unlicensed mm-W in presence of PVT variations, by changing properly V_C, as shown in Fig. 11. An optimized ILFD arquitecture with discrete tuning varactors bank for PVT calibrations, based on the proposed ILFD scheme, is currently under simulations to be on silicon implemented in 65 nm CMOS technology next months.

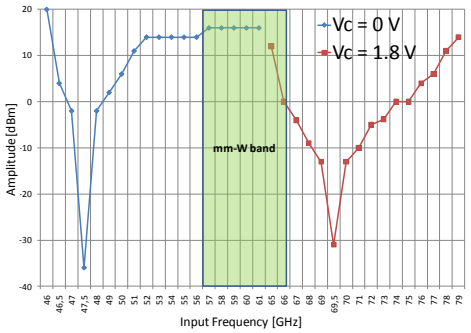

Figure 11. Sensitivity curves at the limits of the Voltage Control range.

VII. ACKNOWLEDGMENT

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