Experimental Demonstration of Heterodyne Phase-Locked Loop for Optical Homodyne PSK Receivers in PONs

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ABSTRACT

Experimental demonstration of heterodyne optical Phase-Locked Loop (oPLL), using simplest optics, is carried out. For the first time, the effect of loop delay has been experimentally characterized and compared directly to the most significant oPLL configurations. It demonstrates a linewidth tolerance of 6.5 MHz if FEC codes are used.

Keywords: Optical Communications, coherent systems, homodyne reception.

1. INTRODUCTION

Homodyne coherent optical reception is considered the ideal method to detect ultra-dense wavelength division multiplexing (udWDM) optical signals, because of its excellent wavelength selectivity, low sensitivity and tunability. However, its implementation has not been commercially deployed because of its stringent requirements in terms of laser spectral linewidth, tuning bandwidth and delay [1]. In the past, several optical Phase-Locked Loop (oPLL) architectures based on well known radio frequency applications were proposed and studied [2-3]. From them, the optical phase-locking technique that requires less complex optics (namely it avoids 90º hybrid quadruple balanced photodetectors) is the balanced oPLL [3]. On the other hand, the architecture with better performances in loop delay terms is the Costas loop [4]. Afterwards, more advanced schemes, as the subcarrier modulated loop [5], were proposed, with some improvements. In any case, to our knowledge, they were never compared in terms of laser linewidth and loop delay.

Along a different line, homodyne systems were mainly focused toward long-haul WDM applications but were not seriously considered for use in access passive optical networks (PON). As these networks have multiple low capacity channels, a major concern is the use of optical filters in order to delimitate these channels in direct-detection based systems, mainly because of the filter's low selectivity. Thus, if users demand increases, a coherent receiver using electrical filtering is a good way to solve this problem. An example of this is shown in Fig.1. Thus, for upgrading an existing WDM-PON, only is needed to replace Central Office (CO) and Customer Premises Equipments (CPE). Then the operator is able to route more than a single wavelength into one WDM standard channel, increasing the network performances [6]. Heterodyne optical receivers could be a first approach, but due to its inherent image frequency problems, a better solution would be homodyne reception.

Since the critical components used in optical homodyne reception (local laser, standard coupler and reception electronics) can be semiconductor integrated, it may constitute a good candidate to be used in future udWDM PON solutions. Also, as demonstrated in this paper, we can use standard DFB/DBR lasers, of relative low linewidth. Consequently, a PON solution based on homodyne reception can potentially be envisaged for deployment after integration development of its optoelectronics.

In this paper, new results are presented for a promising but somewhat forgotten PLL architecture. Since it uses an electrical lock-in amplifier, it is known as lock-in amplifier oPLL based. But another common name is heterodyne oPLL. It was presented in [7-9] in similar schemes. For the first time, a more complete characterization, in terms of linewidth and loop delay, of the heterodyne oPLL is presented and experimentally verified. Also it is compared to the balanced, Costas and subcarrier modulated loops.

2. SYSTEM MODEL

In a RF heterodyne loop, the main idea is dither the local laser phase sinusoidally by a small amount (e.g. 10 mrad). It is done at a frequency above the loop bandwidth. Using this technique, an increase of the loop SNR in front of the additive noise is reported [10].

The phase-locked loop model scheme is depicted in Fig. 1. It is a homodyne balanced receiver with a Proportional-Integral (PI) loop filter. Dithering is introduced after the PI filter. This leads to an amplitude modulated error phase after photodetection, which is filtered and synchronously demodulated [9].

Thus, while the local laser is controlled in low-pass, the deviation measure signal is in band-pass. Since a sine wave is needed to control the laser, a precise design of the parameters of such a pure tone is required. Small amplitude is desired in order not to distort much the detected phase.

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As shown in [9], when using PSK modulated data, in order to avoid data to phase-lock crosstalk, a full wave rectifier is placed between the balanced receiver and the band-pass filter. Hence, the differential equation that characterizes the loop leads to:

$$\frac{d\phi_C(t)}{dt} = K\sin(\omega_c t)\left[\cos\left(\phi_S - \phi_C - \frac{AK}{\omega_c}\sin\left(\omega_c t\right)\right) * h_{f1}(t)\right] * h_{f2}(t) * f(t) \tag{1}$$

where $\phi_S(t)$ is the input generic phase (including phase noise); $\phi_C(t)$ is the phase introduced by the local laser (phase noise + control loop filter output); $h_{f1}(t)$ and $h_{f2}(t)$ are the impulse response of the bandpass and the low-pass filters, respectively; and $f(t)$ is the PI filter impulse response. Assuming that the loop is in tracking mode, this equation can be linearized like for the typical PLLs. A detailed explanation of how to linearize it, can be found in [9]. If we assume only additive noise, an improvement is made by playing with band-pass and low-pass filters bandwidth relationship [10]. So making a proper parameters design, phase noise will be the predominant noise.

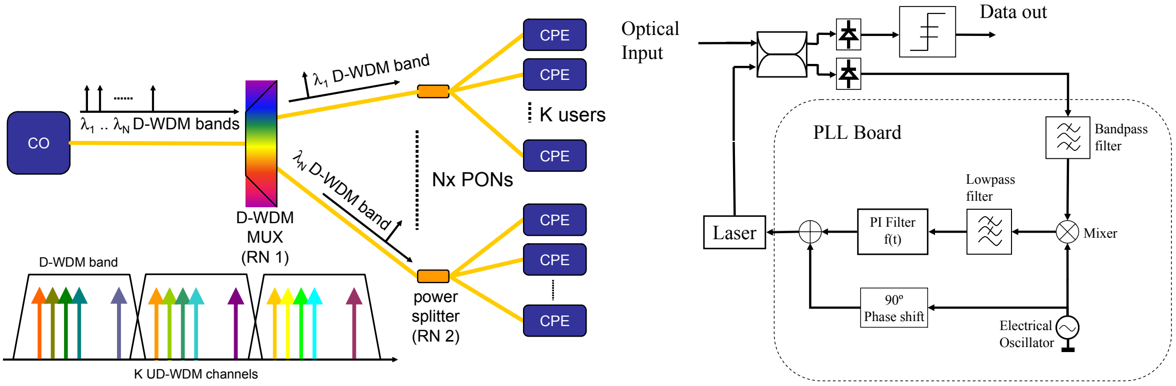

Figure 1. Example of upgrading an existing WDM-PON (left), and heterodyne oPLL schematic (right).

3. SIMULATIONS

The heterodyne oPLL performances were evaluated by means of computer simulations, and it was compared to other oPLL architectures: Balanced, Costas, and Sub-Carrier Modulated loops.

Concerning the heterodyne loop, the system was designed to operate at a dithering frequency of 700 MHz assuming a maximum error phase bandwidth of 200 MHz. Also the amplitude used was of 10 mrad, introducing an additional error phase standard deviation of 5.5º.

Heterodyne loop filters were 4th order Bessel approximations. Since they have a relatively large transition band, they introduce a certain fix delay (near 3 ns) at the pass band, in addition to the loop delay.

We simulated the four oPLL configurations and estimated the phase noise cancellation. Several configurations of damping factor, natural frequency and dithering amplitude have been simulated in order to determine the loop limitations when cancelling the phase noise. Precisely, for each loop, the damping factor was set to 9, assuring an overdamped performance, since it has been demonstrated to be optimum when designing loops with large delay [11]. In each case, the loop natural frequency was optimized in terms of output phase error. These simulations determined the optimal designs for each loop type. So, we made several sweeps of damping factor and natural frequency for different loop delays and laser linewidths. Since 10 ns is an easily implementable delay when regarding a laboratory prototype, results for optimal configurations at 10 ns loop delay are shown in Fig. 2.

From the results, it is shown that at low linewidths (below 1 MHz at 10 ns loop delay), the heterodyne loop mostly has an intermediate performance between the Costas loop and the balanced loop. Thus when using the heterodyne loop, for a 12º maximum phase error deviation we are limited at working at a maximum linewidth of 525 kHz, near the balanced loop limit. When using PSK modulation, that phase error of 12° limits to operate at a BER-floor of 10^{-9} [12]. On the other hand, if FEC codes are used, a BER-floor of 10^{-3} is operable, and a maximum phase error deviation of about 28º is allowed, leading to a maximum linewidth of 6.5 MHz per 10 ns loop delay tolerance. In this case, the heterodyne loop clearly outperforms in a 30% the most advanced loops, such as the sub-carrier modulated loop.

This behaviour is due to the unique architecture of the heterodyne loop. At low linewidths, it is mostly limited by the dithering amplitude, so its performances are near the balanced loop. However, at high linewidths, when the dithering amplitude is negligible, the loop performances are improved by the lock-in amplifier, that ensures a better phase ranging.

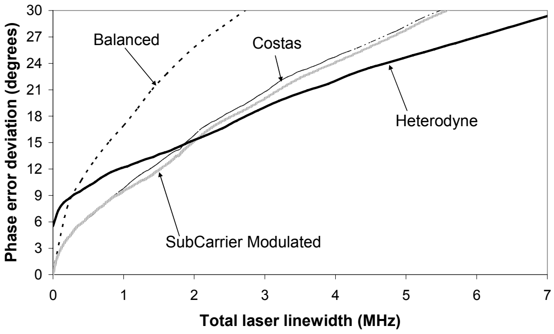

Figure 2. Phase error deviation evaluated at a loop delay of 10 ns.

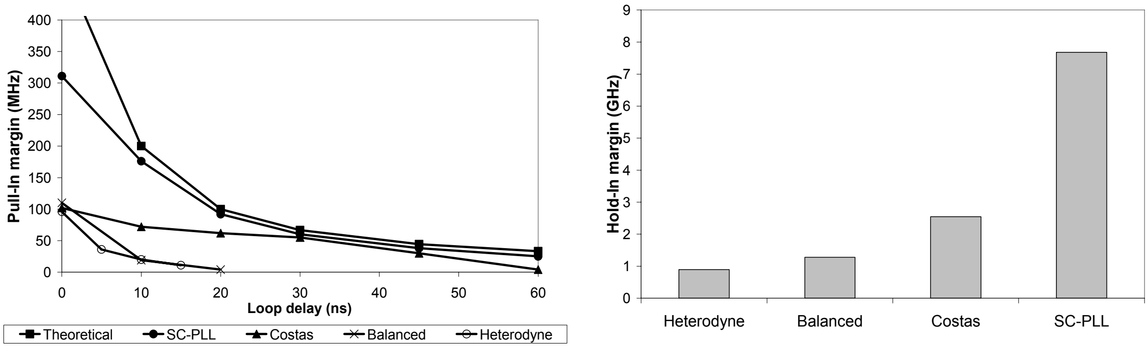

Figure 3. Pull-In margins (left) and Hold-In margins (right) of the simulated oPLL architectures.

After phase noise cancellation simulations, other important parameters were also evaluated: Hold-In and Pull-In margins. The results are shown in Fig. 3. In these figures, we can see that the heterodyne loop has low Pull-In and Hold-In margins. This is its main drawback. Precisely, at 10 ns loop delay, the Pull-In margin is found to be around 20 MHz in front of the 176 MHz achieved by the subcarrier architecture. Concerning the Hold-In margin, the exact data is 896 MHz for the heterodyne loop, and up to 7.68 GHz for the subcarrier.

Table 1. Table summarizing results at 10 ns delay.
Note that when using FEC a BER of 10^{-3} is operable.

	Balanced	**Costas**	**SCM**	**Heterodyne**
Linewidth tolerance BER 1E-9 (10º)	400 kHz	1.05 MHz	1.15 MHz	525 kHz
Linewidth tolerance BER 1E-3 (28º)	2.4 MHz	4.9 MHz	5.1 MHz	6.5 MHz
Pull-In Margin	19 MHz	72 MHz	176 MHz	20 MHz
Hold-In Margin	1.28 GHz	2.55 GHz	7.68 GHz	896 MHz

4. EXPERIMENTS AND DISCUSSION

Once foreseen those improvements, a laboratory prototype of the proposed PLL was developed and assembled into an experimental setup (Fig. 4).

An external cavity tuneable laser was placed at the transmitter (Tx) side, while at the receiver (Rx) side we had a standard DFB laser running at 1544.07 nm. The total laser linewidth was measured by using a self-homodyne technique and found to be 960 kHz. The Rx laser output was fusion spliced with the optical coupler and the photodetector. The balanced detector was substituted by a single photodetector because we had to monitor optical signals, and also achieve relative low loop delay. The parameters for the heterodyne loop prototype were optimized for the 700 MHz dithering frequency. Filters placed inside PLL board were designed and implemented to introduce the same delay as in simulations (around 3 ns). Finally, the total loop delay was measured using a vectorial network analyzer, and found to be 10 ns.

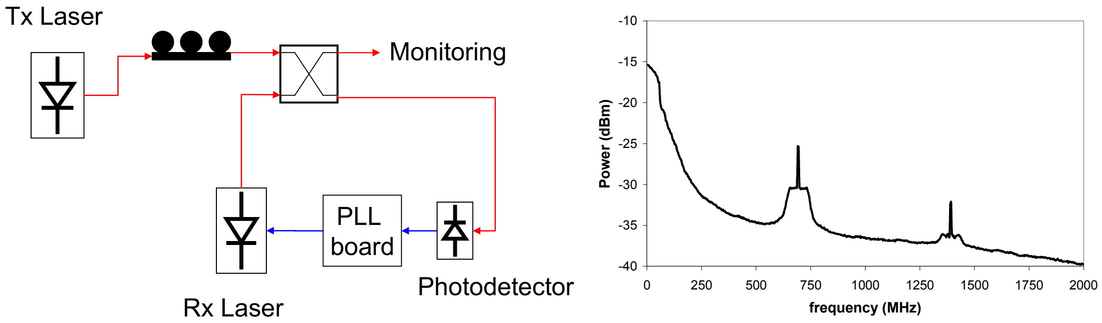

Figure 4. Experimental Setup(left) and electrical power spectrum after photodetection (right).

Locking was observed by tuning one of the lasers until the main beat signal was about 20 MHz, agreeing the Pull-In margin simulation results. Concerning the Hold-In margin, it was found to be 868.24 MHz, also in agreement with the simulations.

Fig. 4 shows the spectrum at the output of the photodetector when locking is achieved. From this spectrum the phase error standard deviation was calculated to be 11.49º for a measurement bandwidth of 200 MHz. This value fits perfectly into the heterodyne loop curve of Fig. 2, confirming again the theoretical calculations. So a maximum BER of 10^{-9} could be achieved when working with this configuration. However, the unique characteristics of such loop, make easy to embed it onto an integrated semiconductor optical circuit. In that case, the loop delay can be dramatically reduced, thus improving oPLL performances.

5. CONCLUSIONS

We have demonstrated that phase noise tolerance performances of heterodyne oPLL are better than the balanced optical PLL. In our case, with a loop delay of 10 ns, a 10^{-9} BER cannot be achieved if we have a linewidth larger than 1 MHz. When using FEC codes the heterodyne architecture outperforms clearly the most advanced oPLLs, and requires much simpler optics.

This architecture uses simple optical components, being specially indicated for low linewidth DFB commercial lasers, and avoiding the use of the phase-critical optical 0/90º hybrids.

REFERENCES

[1] L. G. Kazovsky, G. Kalogerakis and W. T. Shaw: Homodyne Phase-Shift-Keying Systems: Past Challenges and Future Opportunities, *Journal of Lightwave Technology*, vol. 24, no. 12, Dec. 2006.

[2] L. G. Kazovsky: Decision-Driven Phase-Locked Loop for optical homodyne receivers: performance analysis and laser linewidth requirements, *Journal of Lightwave Technology*, vol. 3, no. 6, Dec. 1985.

[3] L. G. Kazovsky: Balanced PLL for optical homodyne receivers: performance analysis, design considerations, and laser linewidth requirements, *Journal of Lightwave Technology*, vol. 4, no. 2, Feb. 1986.

[4] S. Norimatsu, K. Iwashita and K. Sato: PSK optical homodyne detection using external cavity laser diodes in Costas loop, *Photonics Technology Letters*, vol. 2, no. 5, May 1990.

[5] S. Camatel, V. Ferrero, P. Poggiolini: 2-PSK homodyne receiver based on a decision driven architecture and a sub-carrier optical PLL, in *Proc. OFC 2006*, 2006, paper OTuI3.

[6] C. Bock, *et al.*: Ultra-Dense WDM PON based on Homodyne Detection and Local Oscillator Reuse for Upstream Transmission, in *Proc. ECOC 2006*, Cannes, France, Sept. 2006, paper We3.P.168.

[7] R. T. Ramos and A. J. Seeds: Fast heterodyne optical phase-lock loop using double quantum well laser diodes, *Electronics Letters*, vol. 28, no. 1, Jan. 1992.

[8] K. H. Kudielka and W. Klaus: Optical homodyne PSK receiver: Phase synchronization by maximizing baseband signal power, in *Proc. LEOS 1999*, 1999, paper TuU2.

[9] J. M. Fabrega and J. Prat: Optimization of Heterodyne Optical Phase-Locked Loops in Homodyne PSK Detection, in *Proc. ICT 2006*, 2006, paper ThuOS2.

[10] R. W. Smith, *et al.*: Design of a phase-sensitive detector to maximize signal-to-noise ratio in the presence of gaussian wideband noise, *Measurement Science Technology,* vol. 3, Aug. 1992, pp 1052-1062.

[11] S. Norimatsu and K. Iwashita: Damping Factor Influence on Linewidth Requirements for Optical PSK Coherent Detection, *Journal of Lightwave Technology*, vol. 11, no. 7, Jul. 1993

[12] K. Kikuchi, *et al.*: Degradation of Bit-Error Rate in Coherent Optical Communications Due to Spectral Spread of the Transmitter and the Local Oscillator, *Journal of Lightwave Technology*, vol. 2, no. 6, Dec. 1984.