Current Balancing Strategy in Parallel-Connected Legs of Power Inverters

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Abstract

The parallel connection of inverter legs is a way to increase the output currents and thus the converter rated power. The connection is made by inductors and a critical issue is to achieve balanced currents among the legs. Circulating currents produce additional losses and stress to the power devices of the converter. Therefore, they should be controlled and minimized. An efficient technique to achieve such a balance is presented in this paper. The proposed strategy does not include proportional-integral (PI) controllers and parameter tuning is not required. The exact control action to achieve current balance is straightforward calculated and applied. Simulation and experimental results are shown in this paper to verify efficiency of the proposed balancing method.

Introduction

Multilevel converters are extensively used in high power systems. The main reason for this is because they can deal with high voltages. However, in some fields such as wind generation, high power is sometimes achieved by increasing the output current levels and not the voltage levels [1]. Consequently, they are kept in the low-voltage range and, therefore, under the low-voltage regulations, which are less demanding than mid-voltage regulations. Furthermore, the cost of low-voltage maneuver devices is much cheaper under such conditions.

Parallel connected legs of a voltage-source inverter (VSI) require the use of inductors to obtain a single output voltage from several input legs. It would be optimal if current sharing among the legs was balanced; however, there is no guaranty for this unless a proper control is used [2]-[4].

Several techniques can be applied to achieve current balance among the legs. Quick response of the balancing control is crucial to avoid long transitory overcurrents on specific legs which might be destructive. In this sense, balancing methods based on PI controllers might not provide an optimal balancing response. The balancing strategy proposed in this paper can achieve current balance very quickly. The exact modification of the modulation signals is calculated and applied without distorting the output voltages and currents.

Parallel-Connected Legs

VSI's legs cannot be directly connected in parallel in order to avoid shortcircuits. Inductors are the optimal passive components to achieve the following benefits; (1) averaging voltages of several legs for each output phase and (2) limiting circulating currents among the legs. Fig. 1 shows an example of parallel-connected legs. There are n legs in parallel and the output of this scheme corresponds to one single phase of the converter (phase a, for instance).
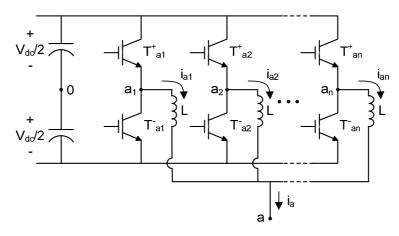

Fig. 1: A single phase of a VSI integrated by n legs connected in parallel

Current Balancing Method

In this study, no magnetic coupling among the inductors is assumed, although the analysis could be extrapolated to magnetically-coupled inductors such as the configurations presented in [5]. However, in those coupling solutions, the equivalent inductance of the output phase is very small, which might not be interesting for grid-connected applications, for instance. On the other hand, if there is not magnetic coupling between the inductors, the equivalent output inductance is L/n, where n is the number of parallel legs. Consequently, the same inductances used for the parallel connection among the legs contribute to the output inductance of the phase needed in grid-connected applications.

The following expression describes relationship between voltages and currents in each leg of the system in Fig. 1.

$$L\frac{di_{aj}}{dt} = v_{aj} - v_{a0} \qquad \text{for} \quad j = \{1, 2, \dots, n\} \qquad (1)$$

Adding up all the terms:

$$\sum_{j=1}^{n} L \frac{di_{aj}}{dt} = \sum_{j=1}^{n} \left(v_{aj} - v_{a0} \right), \tag{2}$$

and taking into account that $\sum_{j=1}^{n} i_{aj} = i_a$, (2) becomes:

$$L \frac{di_a}{dt} = \left(\sum_{j=1}^{n} v_{aj} \right) - n v_{a0}, \tag{3}$$

or:

$$L_n \frac{di_a}{dt} = v_{aCOM} - v_{a0}; \quad \text{where} \quad L_n = \frac{L}{n} \quad \text{and} \quad v_{aCOM} = \frac{1}{n} \sum_{j=1}^{n} v_{aj}. \tag{4}$$

The common voltage v_{aCOM} would be the voltage generated from an equivalent single leg.

The locally-averaged operator is defined as follows:

$$\overline{x}(t) = \frac{1}{T_w} \int_{t-T_w}^{t} x(\tau) d\tau. \tag{5}$$

If the window-width (T_w) used in this operator is defined to be the same as the converter switching period, switching frequency ripples in the voltages and currents are completely filtered and cancelled. Consequently, the variables become continuous. Applying this operator to (4), and considering that the locally-averaged variable $\overline{v}_{aCOM}$ becomes the global reference voltage of the phase $\overline{v}_{aCOM} = v_{aREF}$, this equation becomes as follows:

$$L_n \frac{d\overline{i}_a}{dt} = v_{aREF} - \overline{v}_{a0}; \quad \text{where} \quad L_n = \frac{L}{n} \quad \text{and} \quad v_{aREF} = \overline{v}_{aCOM} = \frac{1}{n} \sum_{j=1}^{n} \overline{v}_{aj}. \tag{6}$$

From (6), the averaged equivalent leg of the whole phase can be deduced, as it is shown in Fig. 2.
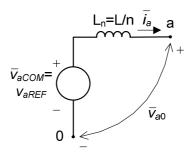

Fig. 2: Averaged equivalent leg

If there were no current balancing control in the system, the voltage reference provided to each leg and the global reference of the phase, that is $\overline{v}_{aj} = v_{aREF}$ for $j = \{1, 2, ..., n\}$, would be the same.

However, in order to provide a control law for each leg current, each individual voltage is modified as follows:

$$\bar{v}_{aj} = v_{aREF} + \Delta \bar{v}_{aj} \quad \text{for} \quad j = \{1, 2, ..., n\}. \tag{7}$$

Adding the control variables $\Delta \bar{v}_{aj}$ into the expression of $\bar{v}_{aCOM}$ in (6), the following relationship is obtained:

$$\bar{v}_{aCOM} = \frac{1}{n} \sum_{j=1}^{n} \left(\bar{v}_{aj} + \Delta \bar{v}_{aj} \right) = \frac{1}{n} \sum_{j=1}^{n} \bar{v}_{aj} + \frac{1}{n} \sum_{j=1}^{n} \Delta \bar{v}_{aj}. \tag{8}$$

Taking into account that the control variables should not affect the output voltage generated by the leg ($\bar{v}_{aCOM} = v_{aREF}$), from (6) and (8) one can conclude that the control voltages have to meet the following condition:

$$\sum_{j=1}^{n} \Delta \bar{v}_{aj} = 0 . \tag{9}$$

Since $\bar{v}_{aCOM}$ becomes unaltered if restriction (9) is applied, from (6) and its equivalent circuit in Fig. 2, one can deduce that $\bar{i}_a$ and $\bar{v}_{a0}$ will also be unaffected by the control variables.

On the other hand, applying the locally-averaged operator given in (5) to (1):

$$L \frac{d\bar{i}_{aj}}{dt} = \bar{v}_{aj} - \bar{v}_{a0} \quad \text{for} \quad j = \{1, 2, ..., n\}, \tag{10}$$

and adding the effect of the control variables, the following relationship is obtained:

$$L \frac{d\left(\bar{i}_{aj} + \Delta \bar{i}_{aj} \right)}{dt} = \bar{v}_{aj} + \Delta \bar{v}_{aj} - \bar{v}_{a0} - \Delta \bar{v}_{a0} \quad \text{in which} \quad \Delta \bar{i}_{aj} = \bar{i}_{aj} - \frac{\bar{i}_a}{n}, \text{ for } j = \{1, 2, ..., n\}., \tag{11}$$

Comparing (10) and (11), and considering that $\Delta \bar{v}_{a0} = 0$ as a consequence of the control restriction given in (9):

$$L \frac{d\Delta \bar{i}_{aj}}{dt} = \Delta \bar{v}_{aj} . \tag{12}$$

Assuming a current imbalance $\Delta \bar{i}_{aj}(k)$ at the instant kT_s, the necessary voltage to achieve the reference current $\frac{\bar{i}_a}{n}$ can be calculated imposing the condition $\Delta i_{aj}(k+1) = 0$ to the discrete representation of (12), as follows:

$$L \frac{\Delta \bar{i}_{aj}(k+1) - \Delta \bar{i}_{aj}(k)}{T_s} = \Delta \bar{v}_{aj}(k) \quad \text{with} \quad \Delta i_{aj}(k+1) = 0; \quad \Delta \bar{v}_{aj}(k) = -\frac{L}{T_s} \Delta \bar{i}_{aj}(k) . \tag{13}$$

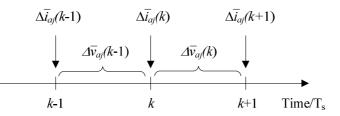Fig. 3 shows a timing diagram for this on-line process.

Fig. 3: Time sequence of the sampling process for current balancing

If it is not possible to achieve current balance in a single sampling period because of a large value required to $\Delta \bar{v}_{aj}$, this control voltage should be limited to its maximum value to avoid overmodulation. When implementing this restriction, still condition (9) has to be satisfied to avoid distortion in the global output voltage phase.

The Interleaving Technique

The interleaving technique is applied to the system shown in Fig. 1 to achieve an apparent switching frequency n times higher that the individual switching frequency of each leg ($f_s = n \cdot f_{sw} = n/T_{sw}$).

Operating with a carrier-based modulation strategy, this is achieved by using an n number of shifted carriers. Fig. 4 shows the general n-case carriers' disposition.
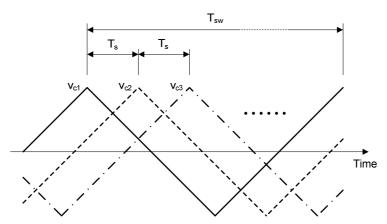

Fig. 4: Phase shift disposition of the carriers for interleaving operation mode

The output current ($\bar{i}_a$) and the individual current of each leg ($\bar{i}_{aj}$) are sensed at the maximum (or minimum) peak of the corresponding carrier (v_{cj}). The value of the variable $\Delta \bar{v}_{aj}$ is calculated at any sampling period and applied to the particular modulation signal of each leg. Subsequently, the balancing dynamic is as fast as the apparent switching frequency ($f_s = 1/T_s$).

Simulation and Experimental Results

The proposed balancing strategy has been simulated by Matlab-Simulink. A single phase converter with three parallel-connected legs has been considered. The load is resistive and connected between the output ("a") and the dc neutral point ("0"). The main data for the simulation are: V_{dc}=1 kV, m_a=0.8, fundamental frequency f=50 Hz, carrier frequency f_{sw}=2 kHz, sampling frequency f_s=6 kHz, L=5 mH with a parasitic resistance of R_p=50 mΩ, and R_{load}=5 Ω.
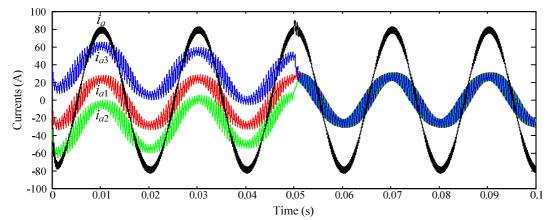
Fig. 5: Simulation results for an initial current imbalance. The balancing control is activated at the time 50 ms
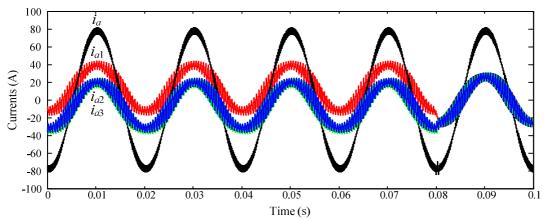

Fig. 6: Simulation results assuming different voltage drops on the power devices. The balancing control is activated at the time 80 ms

Fig. 5 shows the system starting with the balancing control disconnected. An initial current imbalance has been provoked at the beginning of the process. Observe that the currents tend to be naturally balanced; however, the balancing dynamic is very slow. Since the three currents are significantly different for some time, the consequences might be critical for the legs that carry more current. The balancing control is activated at the instant t=50 ms. Observe that the three currents are quickly balanced and the legs carry similar current values henceforth. Thus, similar power losses would be produced in all the transistors of the converter.

Permanent current imbalances are produced due to different voltage drops on the power devices of the legs. Even a small difference in the transistor voltage drops can produce large currents imbalances, since they depend mostly on the inductance parasitic resistor value, which is usually very small.

In Fig. 6, an additional voltage drop on the lower transistor of the leg "a1" is assumed. The system starts with a permanent current imbalance due to this voltage drop. The balancing control is activated a t=80 ms, again quickly compensating for such imbalance. It should be remarked that these kinds of permanent imbalances are much more dangerous for the legs than those produced by transitory processes. Nevertheless, when the controller is activated the currents become balanced very quickly no matter what the reason for imbalance is.

A single-phase laboratory prototype has been built to verify the proposed current balancing strategy. The converter has two parallel-connected legs and operates over a resistive load. The main parameters

are: V_{dc}=50 V, m_a=0.7, f=50 Hz, f_{sw}=5 kHz, f_s=10 kHz, L=6 mH with a parasitic resistance of R_p=0.54 Ω, and R_{load}=10 Ω.

All the figures presented henceforth include experimental and simulation results. In Fig. 7, a disturbance is introduced to produce current imbalance. The current compensator is not activated in this experiment. Although the two leg currents are naturally balanced, they remain unbalanced for some time related to the time constant $\tau = L/R_p$. The time constant value is much larger in real high power systems because resistors associated to huge power inductors are very small. Hence, transitory imbalances will produce significant stress to the power semiconductors of the legs.
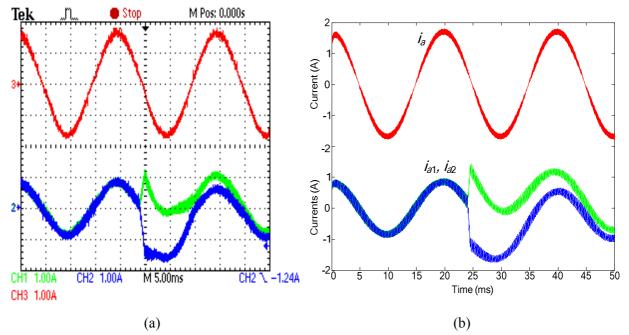

(a)   (b)

Fig. 7: Two parallel legs operating without the balance compensator: (a) experimental and (b) simulation results

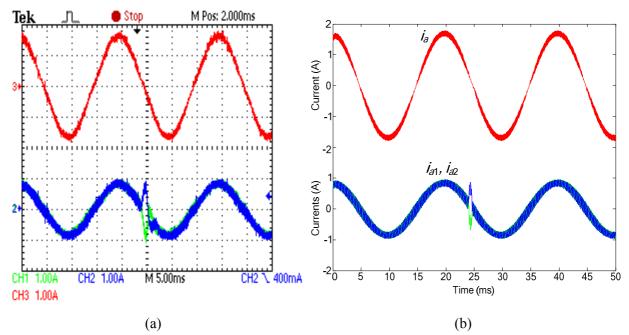(a)   (b)

Fig. 8: Two parallel legs operating with the balance compensator activated: (a) experimental and (b) simulation results

(a)   (b)
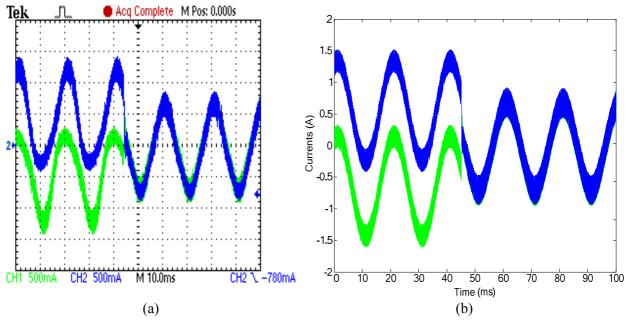
Fig. 9: Current imbalance produced by a small dc voltage difference between the legs and activation of the compensator: (a) experimental and (b) simulation results

A similar process is presented in Fig. 8 with the compensator activated. Observe how the proposed compensator can balance currents very quickly. Notice that the output current has practically no distortion due to compensation. This is because the controller only produces differential voltage for current compensation, but it does change the global output voltage generated by the phase.

Fig. 9 shows an example in which a small dc-voltage has been added to the output voltage of one leg. This process emulates the case of different voltage drops in the transistors of the legs. The system starts with a permanent current imbalance. When the balancing control is activated, the currents are balanced almost instantaneously.

Conclusion

An important challenge for parallel-connected converter legs is to achieve evenly shared currents among the legs. The current control strategy presented in this paper can achieve such balance with very fast dynamics. It is based on calculating the exact control actuation needed for current balance; therefore, it avoids the use of any PI controller.

Simulation and experimental results are provided to validate the behavior of the proposed compensator. The currents are quickly balanced no matter what the reason for imbalance is. Permanent current imbalances are the most dangerous and can be produced by slight differences in the power semiconductors voltage drops. Furthermore, the proposed balancing strategy can be applied to converters with any number of legs connected in parallel.

Motor drives and grid-connected converters are some application fields in which VSIs with parallel legs are applied, especially for high power systems such as those used in wind generation. The main benefit is that the low-voltage regulations have to be met instead of the highly demanding mid-voltage regulations. Furthermore, for very high power systems, multilevel converters with parallel legs can be considered.

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