Diagnosis of Full Open Defects in Interconnecting Lines

R. Rodríguez-Montañés, D. Arumí, J. Figueras

Universitat Politècnica de Catalunya,
Departament d'Enginyeria Electrònica
Diagonal, 647, P9, 08028 Barcelona, SPAIN
Phone: 34 93 4016650; FAX: 34 93 4017784
{rosa;arumi;figueras}@eel.upc.edu

S. Einchenberger, C. Hora, B. Kruseman, M. Lousberg, A.K. Majhi

NXP Semiconductors
THE NETHERLANDS
{stefan.eichenberger;camelia.hora;
bram.kruseman;maurice.lousberg;ananta.majhi}@nxp.com

***Abstract*— A proposal for enhancing the diagnosis of full open defects in interconnecting lines of CMOS circuits is presented. The defective line is first classified as fully opened by means of a logic-based diagnosis tool (Faloc). The proposal is based on the division of the defective line into a number of segments. The selected group of segments is derived from the topology of the line and its surrounding circuitry. The logical information related to the neighbouring metal lines for each considered test pattern is taken into account. With the proposed diagnosis methodology, a set of likely locations for the open defect on the line is obtained. A ranking between the set of possible locations is presented based on the analysis of the quiescent current consumption of the circuit under test. Examples are presented in which the use of the diagnosis methodology is shown to discriminate between different locations of the full open defect.**

***Index Terms*—Defect Diagnosis, Full Open Defect, Interconnecting Line, CMOS.**

I. INTRODUCTION

OPEN defects are frequently occurring in nowadays CMOS technologies [1][2]. They have been traditionally modelled as a resistance inserted between the two disconnected physical points in the line having the defect. The value of this resistance can range from a few kΩ (weak open defect) up to tens of GΩ (complete disconnection or full open defect) [3].

In the presence of a full open defect, the downstream gates of the defective line are in a floating state since they are disconnected from their driver. The voltage value of the floating wire depends strongly on the layout of the defective line and on the surrounding circuitry as well as it depends on the capacitances inside the driven gates and on the initial trapped charge as reported in previous works [4]-[12]. Moreover, the logic response of the circuit to the floating voltage depends on the logic input threshold voltage of the downstream gates for each particular test pattern. If the floating node voltage is larger than the logic input threshold of the next gate it will be interpreted as logic one at its output, otherwise a logic zero will be generated. This behaviour is known as the Byzantine effect [13].

The diagnosis of open defects has been addressed in a number of previous works. However, insufficient layout information from the circuit is taken into account [14]-[17] making the diagnosis of the defect difficult. For diagnosis tools using only logic information and gate level description of the circuit, a non-negligible amount of equivalent physical locations can be found for each given suspicious signal. A work focussed on pinpointing the faulty segment, instead of just diagnosing the defective signal, was presented by Huang [18]. Going towards the use of the information obtained from the physical layout, Sato et al. [19] proposed a segment model that considers the coupling capacitors between the floating node and the adjacent nodes and power and ground rails. However, only vias were assumed to be able to fail.

In this work, the full open defect is assumed to be located in any point in the interconnect architecture between the output of the driver and the input of any of the downstream gates. Thus, vias and interconnecting metal lines are considered. Furthermore, the information obtained from the quiescent current consumption is used to rank the diagnosis results in the case of more than one possible locations.

The paper is organised as follows. Section II presents the full open segment model. The calculation of the voltage at the failing node is shown in Section III. The proposed diagnosis methodology is presented in Section IV and some application examples are illustrated in Section V. In the last Section conclusions of the work are presented.

II. FULL OPEN SEGMENT MODEL

In this section, a proposal for dividing the defective line into a set of segments is presented. This full open segment (FOS) model is derived from the topology of the circuit and will be used for the computation of the floating node voltage.

In order to proceed to the division of the defective line, the topological information of the line itself and of the surrounding signals have to be extracted from the physical design. The required data relates to the dimensions and relative location between the wires in order to compute the coupling capacitances [20]. The physical topology determines

25th IEEE VLSI Test Symmposium (VTS'07)
0-7695-2812-0/07 $20.00 © 2007 IEEE

the partition of the defective line into segments. Within a given segment, the relative distances between wires and their dimensions are kept constant.

In order to illustrate the full open segment model used in this work, let us assume the floating line shown in Figure 1. According to its topology, it is made up of different pieces of metal layers having different distances (height) to substrate or well. In this example, three metal layers going from the lowest metal level (M1) up to the third layer (M3) are shown. In order to compute the coupling (parasitic) capacitances of the line to substrate or well, four parameters for each piece of metal composing the line need to be computed, namely, the length of the piece of wire (L), the thickness (th) and the width (W) at each metal level and the height of the dielectric for each metal level (h).

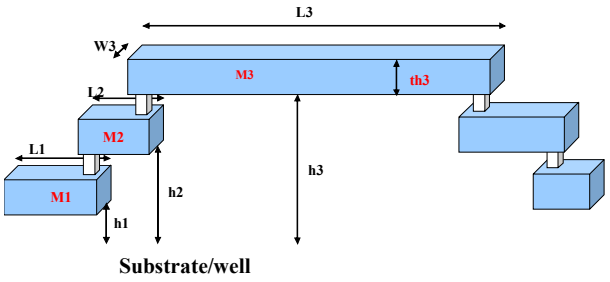

Figure 1: Part of the Layout of a generic interconnecting line.

Figure 2 shows an example of the top-view of the surrounding interconnecting lines for the target/floating node. In the figure, four different neighbours are drawn. Neighbour 1 (labelled N1) is made of metal 1 level (as labelled M1 on the target line). It is placed at a distance d1 from the floating node and has a length LN1. Neighbour N3 is made of a unique metal level but it is composed of two pieces of wire located at different distances, d3 and d3', from the floating node. On the other hand, neighbour 4 (N4) is made of 3 different metal layers, namely, M3, M2 and M1. No vias are depicted in the figure since their contribution to the electrical behaviour of the floating line is negligible (low resistance). Only neighbours made of the same metal layer as the target line are drawn for this example, although the methodology can be applied to coupling between different metal levels provided the coupling information is available.

According to the topological information shown in Figure 1 and Figure 2, the electrical behaviour of the floating node can be evaluated since the coupling capacitances to the neighbouring lines and to substrate and well can be easily computed. Notice that the trapped charge is also referenced in Figure 2 as well as the capacitances added by the next gate(s) placed at the end of the line. This information is determinant in the resulting voltage of the floating line in the case of short lines or open defects located at the far end of the line.

The target node is proposed to be divided into several segments as illustrated in Figure 3. Segment breaks are caused by a change in the neighbourhood. Examples of these changes are the discontinuation of a neighbouring line (breaks segment 1 and 2), or a change in distance to a neighbouring line (break segment 5 and 6) or a change in the coupling area due to a change in the thickness of the coupled lines (break segment 7 and 8). Hence, the coupling capacitance per unit length is constant within a segment. Moreover, we only consider as neighbouring lines, those lines that are in the same metal layer and at a distance less than 5 times the minimal spacing, although this distance boundary can be adapted to each particular design. Hence, each segment consists of the target line and zero to two neighbouring lines. In Figure 3, nine segments have been obtained.

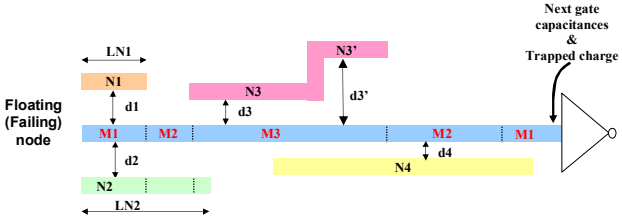

Figure 2: Top-view of the layout of a target/floating interconnecting line and its surrounding (neighbouring) lines. As an example, neighbour *N1*, which is made of M1, is located at a distance (spacing) *d1* from the target line over a length *LN1*. The target line drives an inverter, in this example.

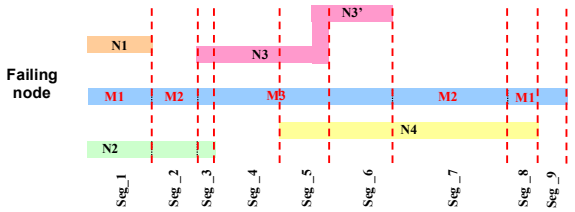

Figure 3: Proposed division of the floating node into different segments depending on the topology of the surrounding circuitry.

Once the floating node has been divided into the appropriate set of segments, the two resulting coupling capacitances to the power rails are extracted in order to compute the node voltage for each particular test pattern. Notice that depending on the logical value of the neighbouring lines and on the type of substrate of well area over which lies the line in a particular segment *k*, the coupling capacitance can have only contribution to V_{DD} (Cup), only to gnd (Cdown) or, most probably, it can have contributions of both signs. The procedure is illustrated in the next section.

III. FLOATING NODE VOLTAGE

For floating nodes the voltage at the end of the line is not controlled by the previous gates but by the neighbouring lines. As a result one does not have consistent fail behaviour, which makes these defects hard to analyse with electrical failure localisation tools. To determine the logic interpretation of the floating line, i.e. if we expect a 0 or a 1, we have to calculate this voltage. The actual voltage depends on the capacitive divider made up of the capacitances lying between the location of the full open and the end of the line. Note that the capacitive divider includes the capacitances generated by tree-like (fanout) lines connected to the floating line. Hence, we can construct a function for this floating line voltage in which

we need to take into account the logical state of the neighbours for a particular test pattern and the location of the open denoted by the segment.

Let us assume a defective line with extracted coupling capacitances as shown in Figure 4 and with a full open defect located in segment *k*. Each segment can be described with one resulting coupling capacitance connected to VDD and one to ground as presented in the previous section. The terms in the capacitance divider consists of the contribution of the next segments after the open (segment *i*, with $i > k$) and the defective segment (*k*) itself. The contribution of the next segments is a constant figure determined by Cup and Cdown and the state of the neighbouring lines, while the contribution of the segment containing the defect depends on the internal location (x) of the open in the segment. The defect location can range between the beginning (x = 0) of the segment up to its end (x = Lk). Since it is a linear dependence it is sufficient to only calculate the values at the begin and end of the segment and perform an interpolation of these results for all other positions. Hence, we can determine Vline (voltage of the floating line) with a open at the end of segment *k* and for test pattern (TP) by:

$$Vline(k,TP) = \frac{\sum_{i=k+1}^{N} Cup\_i}{\sum_{i=k+1}^{N} Cup\_i + \sum_{i=k+1}^{N} Cdown\_i} \qquad \text{eq(1)}$$

while if the open is not at the end of segment *k* we use the linear dependence and obtain:

$$Vline(x,k,TP) = Vline(k-1,TP) + \frac{x}{Lk} \cdot (Vline(k,TP) - Vline(k-1,TP)) \qquad \text{eq(2)}$$

where x is the location of the open defect in segment *k*, going from 0 up to its total segment length (Lk). This equation enables us to calculate the voltage of the floating line and to predict the observed logic value by the receiving gates. Hence, solving the problem of the inconsistent fail for fault localisation.

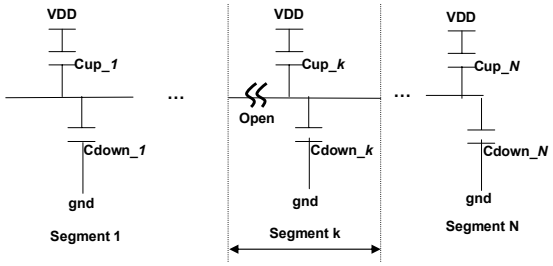

Figure 4: General case for a full open located in segment *k* of an interconnecting line divided into N segments.

IV. Diagnosis of Full Open Defects

With the use of the previously presented full open segment (FOS) model, diagnosis of full open defects can be performed on interconnecting lines. For this analysis one needs a line suspected to contain an open, e.g. determined with a fault localization tool, and the fail results of a voltage test (or, as we show in Section V.B, an IDDQ test).

The information given by the voltage test allows to know which logic level on the target floating line has been interpreted by the rest of the circuit, for each applied test pattern TP. The matching between this measured logic value and the computed Vline(k, TP) is the basis of the proposal for the diagnosis of the full open defect.

As an example, let us assume a circuit with 3 applied test patterns, namely, TP1, TP2 and TP3. The results for the calculated Vline(TP) are depicted in Figure 5 for the whole set of segments (9, in this example). From the applied voltage test we determined that TP1 and TP3 caused the logic value of the floating node to be interpreted as a high value, while TP2 caused the logic value to be interpreted as a low value. In the figure, test patterns with a logic 1 result (line with dots) and the test pattern with a logic 0 result (solid line) are drawn. To explain the observed logic results we need to determine a location in which the expected voltage of the floating line for logic 1 results is always above those of the logic 0 results. In other words, we need a location in which the voltage for TP1 and TP3 is above TP2. In Figure 5 the only locations that fulfil this requirement are between segments 2 and 4, which is therefore the most likely location of the open defect.

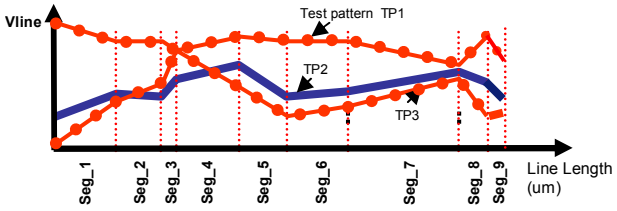

Figure 5: Example of voltage at the floating line (Vline) obtained with the Full Open Segment Model for three different test patterns (TP1, TP2 and TP3). Test patterns with a logic 1 result have been drawn in lines with dots while test patterns with a logic 0 result is drawn solid.

The logic threshold on the downstream gates are usually not predictable since they depend on the trapped charge, on the temperature and on the process parameters which may have a wide variability. Only the relative values of the Vline lines are important since they are insensitive to the the common contributions mentioned above. In this direction, the contribution of the trapped charge does not change the relative position of the target/floating line voltages and hence is eliminated from the voltage computation.

V. Application Examples

In this section, some results obtained from the application of the proposed diagnosis methodology to a CMOS 0.18µm NXP Semiconductors circuit are presented.

A. Example 1

A failing net has been found by the NXP Semiconductors diagnosis tool Faloc [22][23] with a total metal length L=178µm as illustrated in Figure 6 (the floating node is the

thickest line in the figure) and it is made of metal layers M1, M2 and M3 (not indicated in the figure). The number of neighbouring lines depicted correspond to 88 signals although more than half of them are shielded by others being closer to the failing net. In the procedure only the (38) non-shielded signals have been considered. The failing net has two downstream gates G1 and G2. After applying the FOS model, the line has been divided into 124 segments and the open has been predicted to be located at the branch connected to gate G1 as derived from the floating voltage Vline (Figure 7) computed for the Test Patterns that detected a logic 1 (lines with dots) or a logic 0 (solid lines) on the defective node.

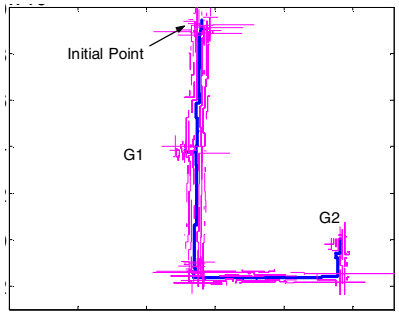

Figure 6: a) Layout of the failing net of example1 and 88 neighbouring lines.

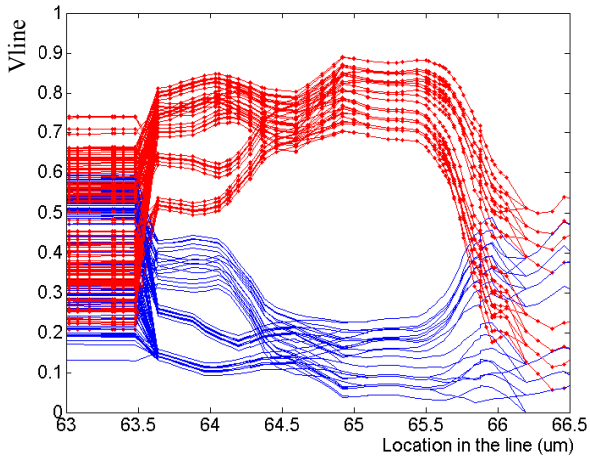

Figure 7: Predicted normalized voltage at the failing net, according to the FOS model, for example 1. The location shown in the figure corresponds to the branch of gate G1.

Notice the reduction of the length of the possible defect locations from 178µm to 2.5µm. However, in this particular case, since the open has been diagnosed in a short branch, the reduction of the length should be related to the length of the branch which is around 4µm.

Quiescent current measurements have been done on the defective circuit and no high current has been measured. The diagnosed open result is consistent with the negligible quiescent current measured since the predicted voltages have no intermediate values and no high current is expected under these circumstances.

B. *Example 2*

The diagnosis methodology has been applied to another failing net detected by Faloc in an interconnecting line with a total metal length L=250µm. The line goes from metal M1 to M5 and the floating line has 31 neighbouring lines. Figure 8 illustrates the layout of the line and its neighbours. After the use the FOS model, the line has been divided into 420 segments.

From the data obtained by the ATE, only one test pattern makes the floating line to have a voltage value interpreted as a logic 1 (line with dots in Figure 9). There are two possible zones where the full open can be located (A and B, in Figure 9) since, in these zones, the "line with dots" (voltage predicted for the test pattern causing a logic 1 on the floating line) has higher values than all the "solid" lines (voltage predicted for the test patterns causing a logic 0 on the floating line).

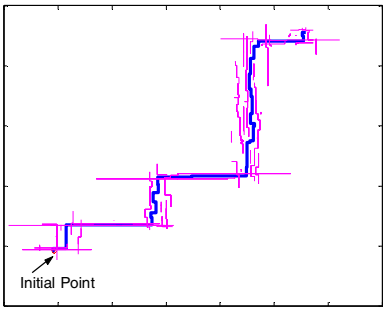

Figure 8: Layout of the failing net of example 2 and 31 neighbouring lines.

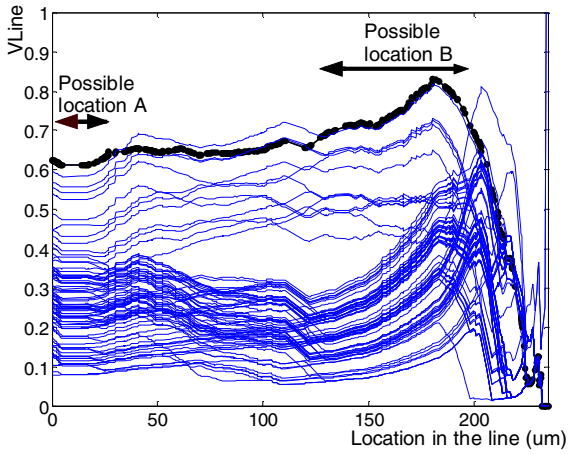

Figure 9: Predicted normalized voltage at the failing net, according to the FOS model, for example 2.

In order to discriminate between the two possible locations of the open defect (A and B in the figure), the information related to the quiescent current consumption has been taken into account. Knowing the downstream gate (4-input OR) and the input driven by the defective node (input B), an electrical simulation has been done in order to compute the current vs. input voltage relationship as illustrated in Figure 10. For each given segment and test pattern, the Vline has been computed and, according to Figure 10, the expected current has been

obtained (IDDQ predicted) and compared to the measured value (IDDQ measured, in Figure 11) for that particular test pattern. For each of the segments we can plot the expected and measured IDDQ for a specific test pattern and determine the correlation coefficient between these values. Examples of these plots are shown in Figure 12 a,b, and c for segment 1 which belongs to zone A, segment 250 which belongs to zone B, and segment 400 which belongs to a different arbitrary zone, respectively. If we calculate the correlation coefficient for all (420) segments we obtain Figure 13 which shows this correlation coefficient as a function of segment number.

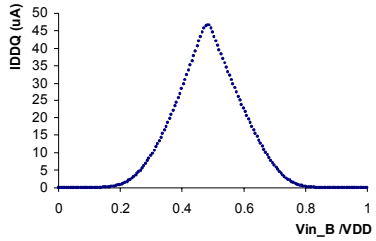

Figure 10: Simulated (SPICE) current consumption of the gate (4-input OR) connected at the floating line.

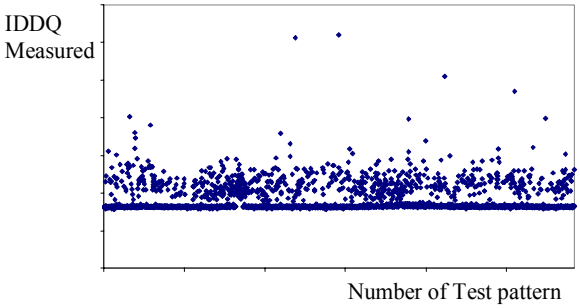

Figure 11: : IDDQ measurements for the defective device.

According to the correlation coefficient, one of the two possible locations (A) is more likely to have the defect. Based on this information, some extra test patterns have been added to the analysis which are those that have caused a high quiescent current consumption although they are not useful in terms of voltage testing (they do not make observable the failing net). Since the only test pattern causing a high logic value on the failing net (line with dots in Figure 9) has also caused a high current consumption on the defective device, it is assumed that, for this test pattern, the voltage value at the floating node has an intermediate value that makes the next gate have both n-network and p-network in an on-state. The selected (four) extra test patterns have also caused a high current consumption in the circuit. Taking this into account, the predicted voltage at the floating node for the four extra test patterns should also lie around intermediate values close to the obtained with the test pattern causing a high logic value on the failing net (line with dots in Figure 9). The predicted voltage for the extra test patterns has been added to the Vline graph with thick solid lines (see Figure 14). The close position between the four extra lines at location A agrees with the expected behaviour.

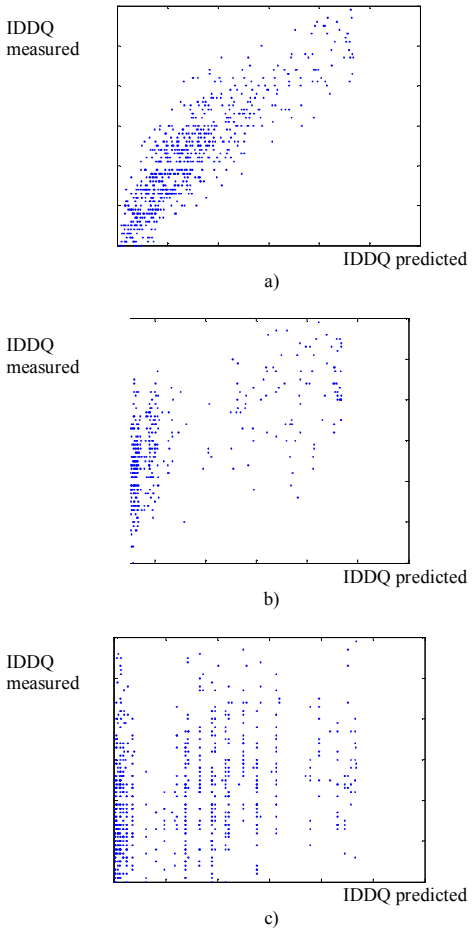

Figure 12: IDDQ measured (y-axis) versus IDDQ predicted (x-axis), for a) segment 1 located in zone A of Figure 9, b) segment 250 located in zone B of Figure 9 and c) segment 400 located in a different arbitrary zone of Figure 9.

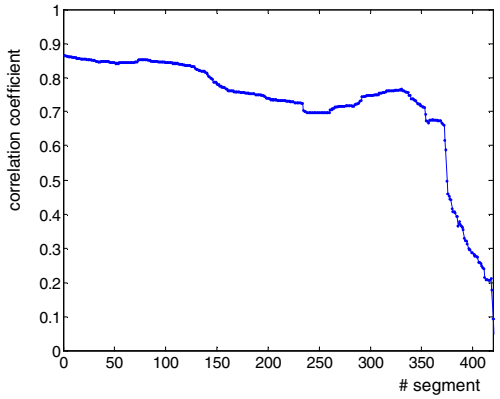

Figure 13: Correlation coefficient between the measured IDDQ and the predicted IDDQ derived from Vline.

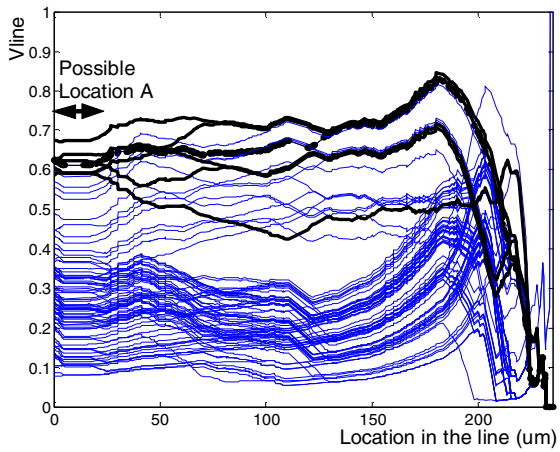

Figure 14: Prediction of the voltage at the floating line, Vline, with the inclusion of four extra test patterns (thick solid lines) that have the property of having caused a high current consumption (IDDQ) in the defective device.

VI. Conclusion

A diagnosis methodology of full open defects in interconnecting lines has been presented. The target defective line is selected with the use of an existing logic diagnosis tool (Faloc [22]). The proposal is based on the division of the defective line into a set of segments. The selected group of segments is derived from the topology of the line and its neighbouring elements. The logical information related to the neighbouring metal lines for each considered test pattern is taken into account. With the proposed diagnosis methodology, a set of likely locations for the open defect on the line is obtained and any point in the line is considered as candidate. A ranking between the set of possible locations has been presented based on the data gathered from the quiescent current consumption of the circuit under test. Examples obtained from a circuit manufactured in a 0.18µm NXP Semiconductors technology have been used to illustrate the methodology.

Acknowledgment

This work has been supported by NXP Semiconductors-UPC project C05746 and MCyT-FEDER projects TEC2004-02625 and TEC2005-01027.

References

[1] Hawkins, C.F.; Soden, J.M.; Righter, A.W.; Ferguson, F.J.; "Defect classes-an overdue paradigm for CMOS IC testing", Proceedings of the International Test Conference, pp.413-425, 1994.

[2] Needham, W.; Prunty, C.; Eng Hong Yeoh; "High volume microprocessor test escapes, an analysis of defects our tests are missing", Proceedings of the International Test Conference, pp.25–34, 1998.

[3] R. Rodríguez-Montañés, P. Volf and J. Pineda de Gyvez, "Resistance characterization for weak open defects", IEEE Design & Test of Computers, Vol. 19, N.5, pp.18-26, 2002.

[4] M. Renovell, G. Cambon, "Topology Dependence of Floating Gate Faults in MOS Integrated Circuits," Electronics Letters, Vol. 22, No. 3, pp. 152-153, 1986.

[5] C.L. Henderson, J.M. Soden and C.F. Hawkins, "The Behavior and Testing Implications of CMOS IC Open Circuits", Proceedings of the International Test Conference, pp.302-3, 1991.

[6] H. Sue, C. Di and J.A.G. Jess, "Probability analysis for CMOS floating gate faults", Proceedings of the European Design and Test Conference, pp. 443-448, 1994.

[7] H. Konuk, "Voltage and current-based fault simulation for interconnect open defects", IEEE Transactions on Computed Aided Design of integrated circuits and systems, Volume 18, Number 12, pp. 1768-1779, 1999.

[8] U. Choudhury, A. Sangiovanni-Vincentelli, "Automatic generation of analytical models for interconnect capacitances", Transactions on Computed Aided Design of Integrated Circuits and Systems, Vol. 14, Is: 4, pp. 470–480, 1995.

[9] Champac, V.H.; Rubio, A.; Figueras, J., "Electrical model of the floating gate defect in CMOS ICs: implications on I_{DDQ} testing", Transactions on Computed Aided Design of Integrated Circuits and Syst, Vol. 13, Is 3, pp.359-369, 1994.

[10] Konuk, H.; Ferguson, F.J.;, "An unexpected factor in testing for CMOS opens: the die surface", Proceedings of the VLSI Test Symposium, pp. 422-429, 1996.

[11] S. Johnson, "Residual charge on the faulty floating gate CMOS transistor", Proceedings of the International Test Conference, pp. 555–561, 1994.

[12] Rafiq, S.; Ivanov, A.; Tabatabaei, S.; Renovell, M.; "Testing for floating gates defects in CMOS circuits", Proceedings of the Asian Test Sympos., pp.228-236, 1998.

[13] Lavo, D.B.; Larrabee, T.; Chess, B.; "Beyond the byzantine generals: unexpected behavior and bridging fault diagnosis", Proceedings of the International Test Conference, pp. 611-619, 1996.

[14] Venkataraman, S.; Drummonds, S.B.; "Poirot: applications of a logic fault diagnosis tool", IEEE Design & Test of Computers, Vol 18, Is. 1, Jan.-Feb. pp.19-30, 2001.

[15] Bartenstein, T.; Heaberlin, D.; Huisman, L.; Sliwinski, D.; "Diagnosing combinational logic designs using the single location at-a-time (SLAT) paradigm", Proceedings of the International Test Conference,. pp.287-296, 2001.

[16] Zhiyuan Wang; Marek-Sadowska, M.; Tsai, K.-H.; Rajski, J.;, "Analysis and methodology for multiple-fault diagnosis", IEEE Transactions on Computed Aided Design of Integr Circuits and Syst, Vol 25, Is 3, pp.558-575, 2006.

[17] Lavo, D.B.; Hartanto, I.; Larrabee, T.; "Multiplets, models, and the search for meaning: improving per-test fault diagnosis", Proceedings of the International Test Conference, pp.250-259, 2002.

[18] Shi-Yu Huang; "Diagnosis of Byzantine open-segment faults [scan testing]", Proceedings of the Asian Test Symposium, pp.248-253, 2002.

[19] Sato, Y.; Yamazaki, L.; Yamanaka, H.; Ikeda, T.; Takakura, M.;, 'A Persistent Diagnostic Technique for Unstable Defects', Proceedings of the International Test Conference, pp.242-249, 2002.

[20] Chern, J.-H.; Huang, J.; Arledge, L.; Li, P.-C.; Yang, P.; 'Multilevel metal capacitance models for CAD design synthesis systems', Electron Device Letters, Vol 13, Is 1, pp.32-34, 1992.

[21] Johnson, S.;, "Residual charge on the faulty floating gate CMOS transistor", Proceedings of the International Test Conference, pp. 555–561, 1994.

[22] "Faloc Reference Manual 3.9", NXP Semiconductors, 2004.

[23] C. Hora, "On Diagnosing Faults in Digital Circuits", Ph.D. dissertation, Technische Universiteit Eindhoven, 2002.