# A $75\,pJ/bit$ All-Digital Quadrature Coherent IR-UWB Transceiver in $0.18\,\mu m$ CMOS

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*Abstract*— In this paper a $75\,pJ_b$ all-digital quadrature coherent impulse radio ultra-wideband transceiver in $0.18\,\mu m$ CMOS is presented. It consumes $42\,mW$ operating at a $560\,Mbps$ datarate. The receiver and transmitter share most of the components reducing the area. This design is optimal for low-power low-cost short-range high-speed communications.

*Index Terms*— Ultra-wideband (UWB), Impulse Radio (IR), Short Range, Low Power, All digital

## I. INTRODUCTION

Although ultra-wideband technology (UWB) has lately been prone to criticism, it still has its niche applications: pulse-based UWB can be successfully used in short-range high datarate communications [1]–[3]. The compromise in terms of power consumption, datarate and distance can be conveniently exploited to achieve at the same time low power consumption and high datarate at the expense of range [1], [4]. The transceiver presented in this paper was designed taking into account these bound conditions (datarate, power and range), resulting in a IR-UWB transceiver with the best performance compared with previous works, to best of the knowledge of the authors.

The receiver and transmitter architectures are described in section II while the measurements are presented in section III. In section IV a comparative with previous works is carried out. Finally the conclusions are summarized in section V.

## II. TRANSCEIVER ARCHITECTURE

IR-UWB transceivers can be implemented with a coherent or non-coherent architecture. The coherent architecture, such as that shown in Fig. 1, was chosen for the transceiver because it's more appropriate for noisy or interference-rich environments. The FCC part 15 [5] defines several frequency bands. The $3$–$5\,GHz$ band was selected as a compromise between available bandwidth and center frequency.

In order to reduce area occupancy as well as complexity the transceiver architecture presented in this work shares
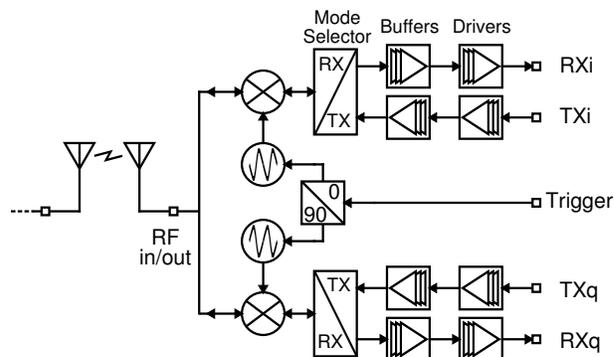


Fig. 1.   Quadrature transceiver architecture.

as much components as possible between the receiver and the transmitter. To achieve this functionality the unilateral blocks of the RF front-end are suppressed based on two inherent properties of impulse-radio ultra-wideband (IR-UWB). In the first place, receivers are not noise limited but rather interference limited, thus the LNA is not required [4]. In the second place, to conform to the tight power spectral density specifications, the transmitted power is so limited that it can be achieved without the need of a PA. Besides suppressing these blocks, a quadrature topology is used, only possible in coherent receivers, not only to improve spectral efficiency but also to ease signal tracking and synchronization [6]. The whole transceiver is implemented in a pure digital CMOS technology; this yields to reduced cost and area (no inductances are used), at the expense of some performance lose, though.

### A. Receiver Mode

IR-UWB coherent receivers are usually built upon a correlator or a matched filter [7]. This architecture can be implemented in analog receivers by combining a mixer, a template generator and an integrator [7]. The receiver full differential topology proposed in this work is depicted in Fig. 2. The common gate input stage (M1–M2), shared between the I and Q branches, is not matched to $50\,\Omega$
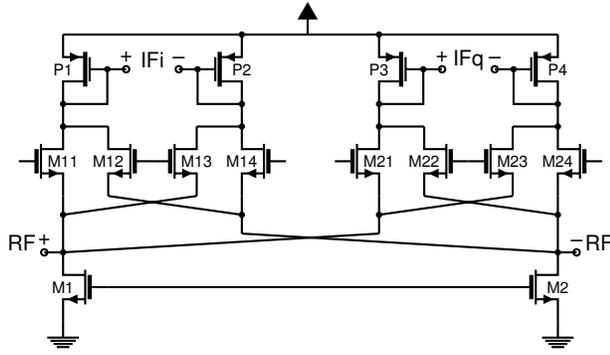
Fig. 2. Quadrature receiver mode schematic.



Fig. 4. Simplified transmitter mode schematics for amplitude modulation. (a) Transmission of "0", (b) transmission of "1".

to obtain UWB operation [4]. The Gilbert cell of the I branch (M11–M14) is connected to active loads (P1–P2) to obtain the demodulated IF signal. This signal is then amplified by the baseband buffers shown in Fig. 1 and finally connected to a driver to drive the $50\,\Omega$ input of the oscilloscope. For the sake of simplicity the connections to the template generator (gates of transistors M11–M14) are not shown. The Q branch (M21–M24 and P3–P4) is connected in a similar way.

Post-layout transistor level simulations of the signals involved in the receiver are depicted in Fig. 3. The upper panel represents the RF input signal. The signal in the middle panel is the output at the active load in Fig. 2. Finally the last panel shows the signal amplified by the baseband buffers in Fig. 1, just before the driver.

### B. Transmitter Mode

There are different modulations schemes for IR-UWB communications (PPM, PAM, . . . ). An amplitude modulation (PAM) is easily implemented in this circuit unbalanc-
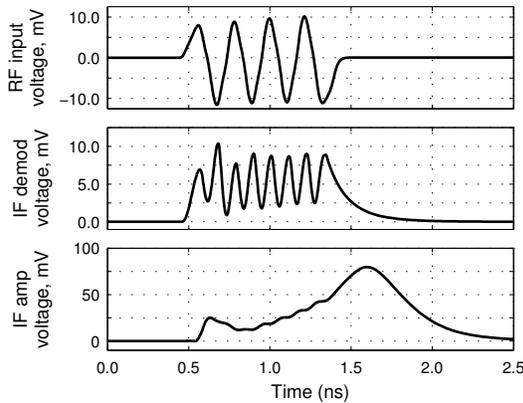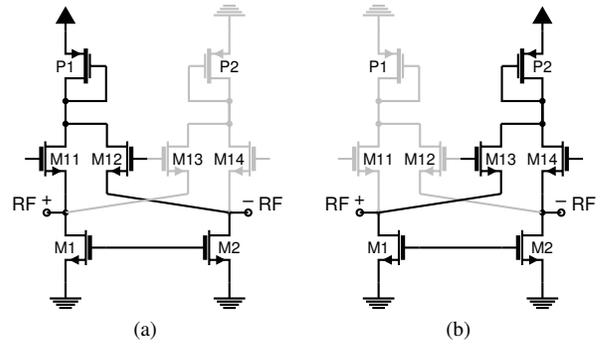
ing the Gilbert cell by connecting one active load source to the positive supply and the other to ground for a "0" pulse, or vice versa for a "1" pulse. A simplified non-quadrature version of the transceiver is shown in Fig. 4a while generating a "0" pulse and alternatively generating a "1" signal in Fig. 4b. It's worth noting that to achieve dynamic operation an inverter (with complementary outputs) must be connected to the sources of transistors P1–P2. Also a driver to adapt the signals to the $50\,\Omega$ signal generator output is implemented, as shown in Fig. 1. The IR-UWB transmitted signal for the IQ transceiver operating as a transmitter is represented in Fig. 5.

### C. Mode selection, frequency control and synchronization

We have introduced a transceiver that can operate with the same basic blocks either as receiver or transmitter. However, this can be only achieved in half-duplex, as the receiver and transmitter share most of the components and area.

The receiver synchronization is performed by measuring the detected energy at the outputs of the IQ branches. The frequency of the template generator and the delay between each IQ branch are controlled externally. These two controls together with the external trigger are used in coarse synchronization and tracking.
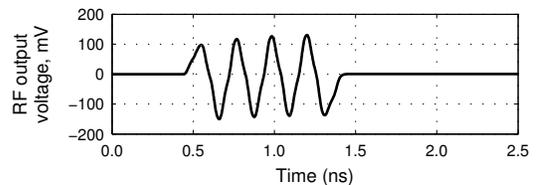


Fig. 3. Receiver transistor level simulation.
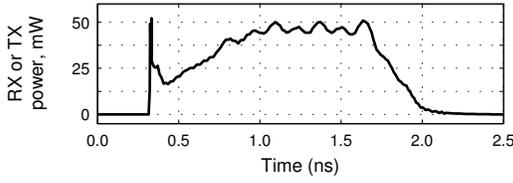


Fig. 5. Transmitter transistor level simulation.

Fig. 6. Receiver or transmitter power consumption transistor level simulation.

### D. Power consumption

IR-UWB transceivers can operate in a very low duty cycle, thus only the instantaneous power consumption during the transmitter and receiver operation time window is shown in Fig. 6. Non optimized systems usually have RF front-end blocks such as the LNA always on, which yields to higher power consumption specially in low duty cycle operation. There exist some techniques to switch these blocks off [8], but they need extra control. Due to the fact that the actual transmitted power is very low and the power consumption is dominated by the template generator and buffers, the power consumption in both the receiver and transmitter mode is the same. The power consumption of the transceiver for either receiving or transmitting mode is represented in Fig. 6.

### III. MEASUREMENTS

The transceiver was fabricated in a $0.18\mu m$ 1P6M CMOS technology. A microphotography of the chip is shown in Fig. 7a. The layout of the transceiver core is depicted in Fig. 7b, covering an area of $0.11\,mm^2$. The complete system was characterized at different datarates with a pair of UWB antennas at $30\,cm$ distance.

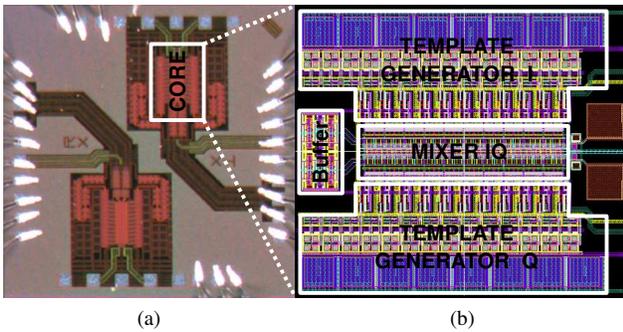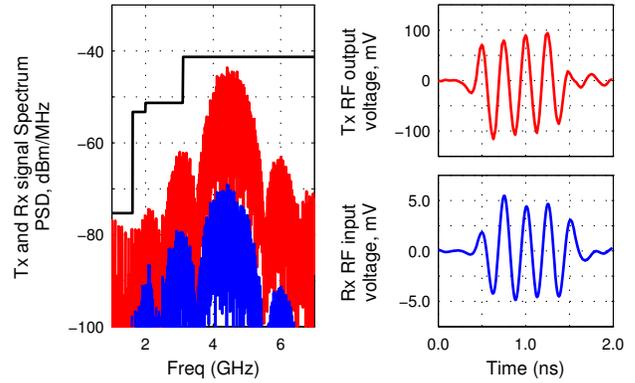Measurements of the power spectral density and time domain measurements of the transmitted and received



Fig. 8. Measurements of transmitted and received (a) PSD and (b) time domain waveforms.

pulses —at a center frequency of $4.48\,GHz$— are represented in Fig. 8a and Fig. 8b, respectively. The link attenuation is measured to be around $28\,dB$ in the whole band.

The datagram of the transmitted bits and demodulated pulses is shown in Fig. 9. The datarate is $560\,Mbps$ in IQ modulation, with an overall power consumption for the receiver and transmitter of $42\,mW$. This yields to an energy per bit of $75\,pJ/s$. The BER is better than $10^{-4}$. The system was tested up to $1.2\,Gbps$ using a cable and a $12\,dB$ attenuator between the transmitter and the receiver. The power consumption of the transceiver was also measured for different datarates, as shown in Fig. 10. The center frequency can be swept from $3$–$5\,GHz$ to accommodate different bands of operation and compensate for PVT effects.



(a)          (b)

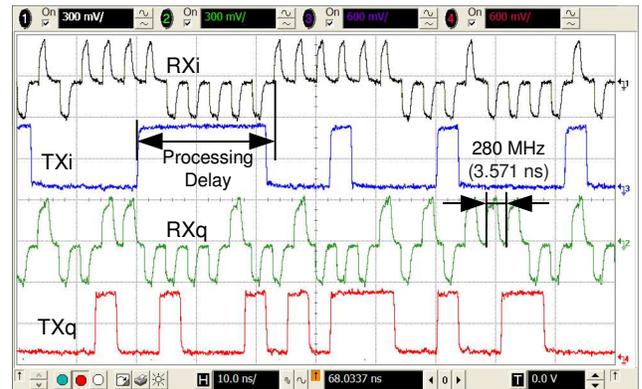Fig. 7. Chip microphotography and core layout.



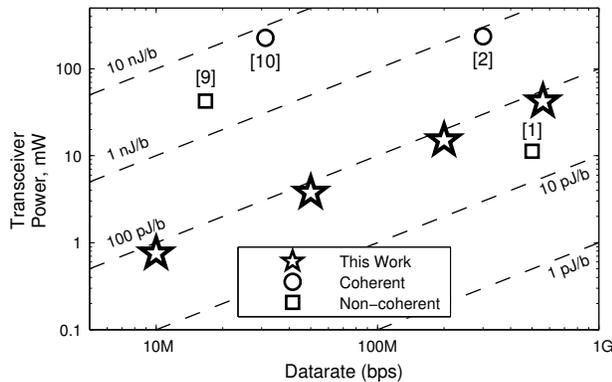Fig. 9. Datagram measurements of the transmitted bits and demodulated signals for IQ modulation.

Fig. 10. Power, datarate and energy per bit comparative

## IV. COMPARATIVE

As explained in section II there are several IR-UWB architectures proposed in the literature with significant differences. When compared to low speed transceivers the circuit proposed in this work performs much better in terms of efficiency even whether they're coherent [2] or not [9]. When compared to medium to high speed IR-UWB transceivers it's clearly better than any other coherent systems [10] and only a non-coherent system such as the one presented in [1] has better energy per bit figures. This comparative is illustrated in Fig. 10.

Besides a lower power, the presented transceiver has also a smaller area, mostly due to the fact that all the other transceiver use inductances. Moreover, the system in [1] lacks any frequency tuning control, making it difficult to calibrate or compensate for PVT effects. This comparative is summarized in Table I.

TABLE I
COMPARATIVE

| Reference | [10] | [9] | [2] | [1] | This |
|---|---|---|---|---|---|
| Energy/bit $(pJ/b)$ | 7240 | 2540 | 787 | 22.6 | **75.0** |
| Datarate $(Mbps)$ | 31.2 | 16.7 | 300 | 500 | **560** |
| Power $(mW)^a$ | 226 | 42.5 | 236 | 11.3 | **42** |
| Freq. $(GHz)$ | 3–9 | 3–5 | 4&8 | 1–2 | **3–5** |
| Coherent | Yes | No | Yes | No | **Yes** |
| Area $(mm^2)^b$ | 4.50 | 2.28 | 16.7 | 0.36 | **0.11** |
| Inductors | Yes | Yes | Yes | Yes | **No** |
| Freq Tuning | Yes | Yes | Yes | No | **Yes** |
| CMOS $(nm)$ | 180 | 90 | 180 | 180 | **180** |
| Year | 2008 | 2008 | 2007 | 2008 | **2009** |

$^a$ Excluding buffers and post processing logic.
$^b$ For half-duplex operation whenever possible.

## V. CONCLUSION

We have presented a quadrature all-digital coherent IR-UWB transceiver in $0.18\,\mu m$ CMOS which can operate up to $560\,Mbps$ with an energy efficiency of just $75\,pJ/s$. It is based on a novel architecture that shares most of the RF front-end between the receiver and the transmitter resulting in a smaller area. The system performs better than any IR-UWB coherent transceiver found in the literature and only some non-coherent systems have lower energy per bit, but at the expense of performance.

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