Modelling and experimental verification of the impact of negative bias temperature instability on CMOS inverter

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Abstract

The effects of negative bias temperature instability (NBTI) on the performance of a CMOS inverter have been investigated by means of both simulation and experimental methods. The simulation of NBTI effects on CMOS inverter has been done by shifting the pFET V_{tho} BSIM parameter. The results show that NBTI shifts the inverter transfer curve, reduces the low noise margin and current consumption but increases the high noise margin. A good agreement between simulation and experimental results has been obtained. Therefore, it can be assumed that the effect of NBTI on CMOS circuits can be mainly predicted by shifting the V_{tho} pFET parameter.

1. Introduction

The impact of negative bias temperature Instability (NBTI) on MOS devices and circuits is one of the most critical issues of present CMOS reliability problems, which can limit the IC dimensions reduction. It is mainly accepted that NBTI is ascribed to the formation of Si/SiO_2 interface states and the oxide positive charge [1]. Regarding to this problem, the dominating work has been concentrated on discrete transistor parameter shift, rather than on circuit performance. At device level, it has been demonstrated that NBTI effect on pFET is manifested in increasing the threshold voltage (V_{tho}). Therefore the drive current is reduced [2]. The NBTI effect on static and dynamic stress has been also reported. These investigations show that the voltage threshold shift (ΔV_{th}) under dynamic stress is almost half of DC case, due to the recovery properties of NBTI [3]. At circuit level, the NBTI effects have not been deeply investigated. However, some works

have pointed out that NBTI provoke a signal noise margin (SNM) reduction on SRAM cell [4] and a frequency reduction in case of CMOS ring oscillator [5].
In order to improve the understanding of the effects on digital circuits during the design phase, SPICE reliability models of wearout mechanisms are required. In this paper, the impact of NBTI on the performance of CMOS inverter has been modelled and verified experimentally. Specifically, the impact of NBTI in the voltage transfer curve, noise margin and current consumption has been analyzed.

2. Experimental

The samples under test correspond to pFET with aspect ratio 2 μm/0.13 μm and CMOS inverters with aspect ratios of 3 μm/0.13 μm and 6 μm/0.13 μm, for the nFET and pFET, respectively. Fig.1 depicts the stress setup. A stress–measure–stress sequence has been followed in the experiment, with exponentially increasing periods of time. During the measurement phase, the I_D–V_G pFET characteristic/inverter voltage transfer curve (VTC) for CMOS inverter has been measured. During the NBTI stress phase, a constant voltage of 0 V has been applied to the pFET gate/inverter input and the rest of the terminals have been biased at 2 V. In order to accelerate the NBTI effects the experiments have been done at 125 °C.

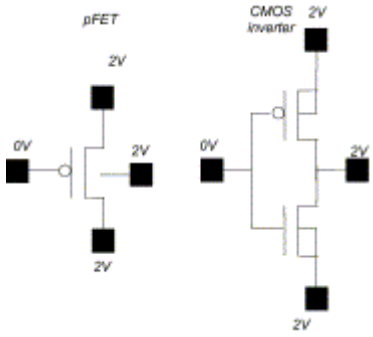

Fig. 1. Voltage applied in each terminal during the NBTI stress.

3. Results

3.1. Getting ΔV_{th} in a single pFET

The starting point of the experiment consists of measuring the ΔV_{th} due to NBTI on a single pFET. In Fig. 2 the ΔV_{th} time dependence is shown. A power law dependence

with slope 1/6 has been obtained experimentally, according the theoretical prediction [1]. This time dependence behaviour has been included in an SPICE simulator with the purpose of predicting the effects of NBTI on CMOS inverter. In order to do that, the pFET and nFET have been modelled with BSIM3 model [6] and a shift on the V_{tho} parameter of pFET has been included according with the data set obtained in Fig. 2.

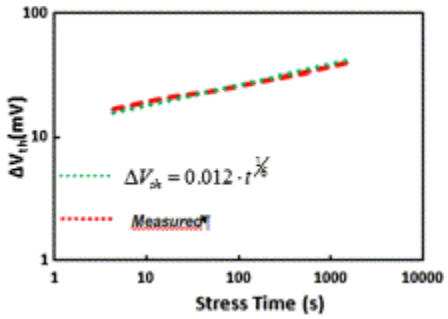

Fig. 2. ΔV_{th} of single pFET as a function of stress time for NBTI stress. The data sets are fitted with a power law with exponents 1/6.

3.2. Impact on VTC

Once the voltage threshold shift in a single pFET has been obtained, the inverter VTC for different stress time has been simulated and measured. In order to quantify the VTC shift, the maximum gain point shift (ΔV_M) of VTC is considered as a reference.
The theoretical relationship between ΔV_M and the inverter pFET ΔV_{th} is given by

(1)

$$\Delta V_M = \frac{\Delta V_{th}}{1 + \sqrt{\frac{\mu_N (W/L)_N}{\mu_P (W/L)_P}}}$$

where μ denote the carrier mobility and W/L the transistor aspect ratio. The subindex N and P denote the nFET and pFET channel, respectively. The CMOS inverter under test has been designed in order to achieve the maximum gain point at $V_{DD}/2$, thus $\mu_N(W/L)_N = \mu_P(W/L)_P$. Forcing this condition, the ratio between ΔV_{th} and ΔV_M is given by

(2)

$$\Delta V_M = \frac{\Delta V_{th}}{2}$$

In Fig.3 the measured VTC for different stress times are plotted. As it has been expected theoretically, the NBTI provokes a VTC shift to the left, which indicates the increasing of voltage threshold of the pFET transistor. Fig. 4 shows the experimental and simulation results of the ΔV_M versus stress time. As it can observed, the simulation data predict correctly the measurement behaviour. It is observed that ΔV_M increases with the time stress with a power law dependence. Moreover, if both ΔV_M and ΔV_{th} are compared, a similar power law dependence, with exponent of 1/6 is achieved. Therefore, ΔV_M is half of ΔV_{th}, which is predicted theoretically by [2].

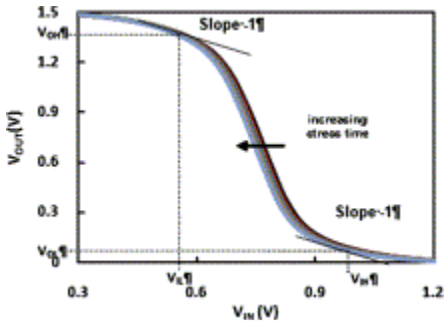

Fig. 3. Experimental transfer curve of an inverter for different stress times. The noise margin are defined when the slope of VTC is equal −1.

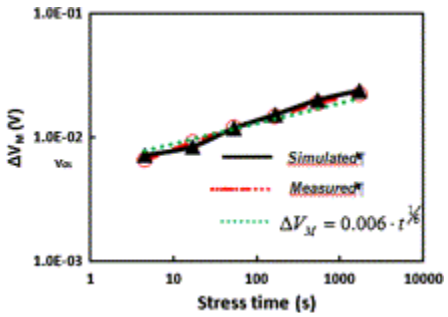

Fig. 4. Measured and simulated ΔV_M as a function of time stress. The time dependence follows a power law with exponent of 1/6.

3.3. Impact on noise margin

The robustness of a CMOS inverter can be expressed in terms of immunity to noise. The most common way to express this immunity is the noise margin. Two types of noise margin can be differentiated; low noise margin (NML) and high noise margin

(NMH), which correspond with the minimum noise level signal to switch the CMOS inverter from low to high and from high to low, respectively. The NML and NMH are defined by

(3)

$$\mathrm{NML} = V_{IL} - V_{OL}$$
$$\mathrm{NMH} = V_{OH} - V_{IH}$$

where V_{IL}, V_{OL}, V_{OH}, V_{IH} are obtained when the slope of VTC equals −1 (Fig. 3). Ideally, noise margin should be symmetrical and as large as possible. Using the LEVEL1 MOSFET model the noise margin has been obtained analytically (see Appendix A). The inverter transfer curves measured and simulated have been processed in order to evaluate the impact of NBTI on NML and NMH and compared with the analytical solution. Fig. 5 shows the NMH and NML against the stress time. It is interesting to observe that NMH and NML have a different stress time evolution; the NMH increases with the stress time whereas the NML is reduced. In both cases, the simulation results fit the measurement results. It is also interesting to note that similar trend are obtained analytically, by shifting the voltage threshold following the power law corresponding to Fig. 2. Therefore, It confirms that NBTI mainly has effect on pFET threshold voltage.

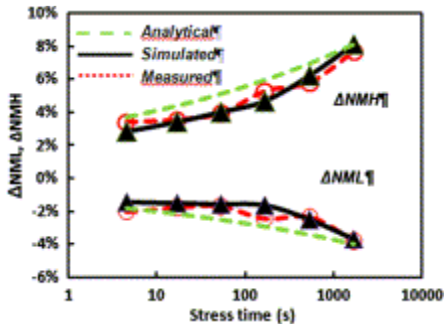

Fig. 5. Measured, simulated and analytical ΔNML and ΔNMH as a function of stress time. ΔNMH increase with stress time whereas ΔNML is reduced.

Usually, it is accepted that the noise margin is defined by the minimum value between NML and NMH. Taking this approach our results show that NBTI reduces the noise margin, since NML is decreased. However, it should be pointed out that NMH increases with NBTI.

3.4. Power consumption

Finally, the current consumption of CMOS inverter has been analysed. In Fig. 6 the CMOS current consumption versus the voltage input, which has been namely as short circuit current (I_{SC}) consumption, is plotted for different stress times.

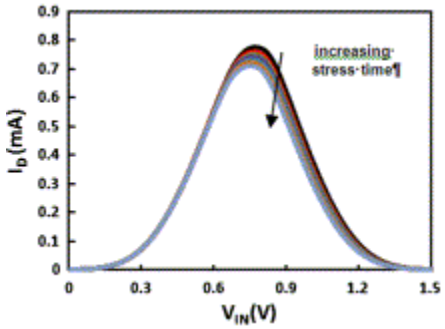

Fig. 6. Experimental current consumption for different stress time.

In Fig. 7, the measured and simulated maximum short circuit current shift (Δ_{ISCmax}) versus stress are shown. In order to quantify the drain current (I_D) reduction, the maximum short circuit current shift has been used. In Fig. 7, the measured and simulated maximum current shift against the stress time is shown. It is observed a reduction about 100 μA after 1650s, and a power law dependence of 0.2.

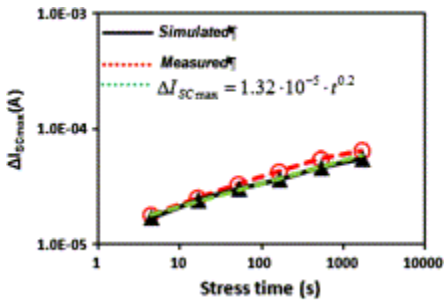

Fig. 7. Measured and simulated maximum current consumption shift as a function of stress time. The time dependence follows a power law with exponent of 0.2.

4. Conclusions

In this paper the impact of NBTI on CMOS inverter has been simulated and experimentally analyzed. The simulation of NBTI effects on CMOS inverter has been done by shifting the pFET V_{tho} BSIM parameter. The results show that NBTI provokes a shift in the VTC to the right side, reduces the low noise margin but increases the high noise margin. Also it has been observed that NBTI reduces the current consumption. Moreover, a good matching between simulations, experimental and analytical results have been obtained. Therefore, NBTI effects on CMOS inverter circuits can be mainly predicted by shifting the V_{tho} parameter of pFET.

Acknowledgments

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Appendix A

The inverter noise margin has been obtained analytically. In order to obtain V_{IL}, V_{OH} the LEVEL1 nFET drain current in saturation region [4] and pFET drain current in triode region [5] has been equalized

(4)

$$I_{Dn}=K_N\cdot(V_I-V_{Tn})^2$$

(5)

$$I_{Dp}=K_P\cdot[2\cdot(V_{DD}-V_I-|V_{Tp}|)\cdot(V_{DD}-V_{OUT})-(V_{DD}-V_{OUT})^2]$$

where K denote the transconductance factor and V_T the threshold voltage. The subindex n and p denote the nFET and pFET channel, respectively.

Eqs.[4] and [5], the output voltage has been obtained[6]:

(6)

$$V_{OUT}=(V_I+|V_{Tp}|)+\sqrt{(V_{DD}-V_I-|V_{Tp}|)^2-\frac{K_N}{K_P}\cdot(V_I-V_{Tn})^2}$$

As we have show in Fig. 3, the V_{IL} and V_{OH} are defined from equating slope of VTC to −1, so, calculation the derivative of expression [6] we obtain

(7)

$$\frac{\partial V_{OUT}}{\partial V_I}=1-\frac{(V_{DD}-V_I-|V_{Tp}|)+\frac{K_N}{K_P}\cdot(V_I-V_{Tn})}{\sqrt{(V_{DD}-V_I-|V_{Tp}|)^2-\frac{K_N}{K_P}\cdot(V_I-V_{Tn})^2}}=-1$$

Clearing V_I from [7] the V_{IL} is obtained [8]. The V_{OH} is calculated by substituting [8] on [6].

(8)

$$V_{IL} = \frac{(3 \cdot K_P + K_N) \cdot [(V_{Tp} - V_{DD}) \cdot K_P + V_{Tn} \cdot K_N]}{K_N^2 + 2 \cdot K_N \cdot K_P - 3 \cdot K_P^2} + \frac{2 \cdot K_P \cdot (V_{Tn} + V_{Tp} - V_{DD}) \sqrt{K_N \cdot (3 \cdot K_P + K_N)}}{K_N^2 + 2 \cdot K_N \cdot K_P - 3 \cdot K_P^2}$$

The same process has been follow in order to obtain V_{IH} and V_{OL}. However, in this case, the nFET is in triode region and pFET is in saturation region.