A Regenerative Active Clamp Circuit for DC/AC Converters with High-Frequency Isolation in Photovoltaic Systems

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Abstract— **DC/AC converters with high-frequency isolation and bidirectional power flow are extensively used in photovoltaic power systems and small isolated power converters at low and medium power ranges.**

The main disadvantages of these circuits are: high freewheeling loss of the primary leakage current, limited ZVS range for the lagging leg switches, the effects of the parasitic elements of the systems and others. To avoid these losses an energy recovery circuit based on an active voltage clamper is presented.

The control circuit is designed having a number of soft switching transitions. The system has been verified by simulation and a prototype is being tested. In this paper we present an energy recovery system and a modulation sequence for the cycloconverter. The energy recovery system is based on an active voltage clamper; the voltage peaks energy is returned to the source. Furthermore, the presented modulation sequence is designed to have a maximum number of soft-switching transitions independent of the electric variables; which means minimum losses and independence on measurement systems limitations for modulation.

I. INTRODUCTION

High frequency power conversion started to become popular during the 80's and 90's. [1] – [3]. In those years, different high-frequency switching techniques were introduced together with the concept of soft-switching. Nowadays, those designs are feasible due to the improvement in the devices and control performance [4].

For the transformation of DC to AC a number of topologies have been proposed, that comply with the basic requirements. These topologies have the drawback that they whether work in low-frequency or do not have isolation between the input and the output.

The advantages of high-frequency isolation is an important reduction of the weight, volume and cost of the reactive components.

Among the topologies to obtain DC to AC conversion with isolation, the one in Fig. 1 is especially interesting since the number of conversion and filtering stages is minimized. This converter also allows bidirectional power flow. However, critical parasitic elements can significantly affect the performance of this converter when operated at high frequencies. In particular, overvoltages in the transformer secondary are especially noticeable. In this paper, the addition of an energy recovery system is proposed in order to control these negative effects and optimize the overall converter performance.

The control of the energy recovery system is designed to obtain zero-current-switching (ZCS) and zero-voltage-switching (ZVS) in all the converters switches, thus increasing the computer efficiency.

II. TOPOLOGY.

The power converter includes a first stage of a four quadrant full bridge inverter working at 20 kHz. Then a high frequency transformer rises the voltage up to 400 V and provides isolation. A high-frequency bidirectional cycloconverter with an output low pass filter provides the line frequency output. Fig. 1 shows the schematic of this circuit [5]. In parallel with the high-frequency cycloconverter there is an regenerative bi-directional voltage clamper taking up the energy stored in the parasitic elements of the high frequency transformer, as in [6] and [7].

This stored energy will be processed and returned to the main circuit in the inverter stages. The bi-directional active clamp circuit consists of four active switches with an anti-parallel diode, $Sc_1 - Sc_4$, a full bridge rectifier, $D_1 - D_4$, and a clamp capacitor, C_{store}. For the design of the capacitance of the clamp capacitor, an energy balance between the energy stored in the transformer leakage inductor and the energy stored in the clamp capacitor has been made.

Equation (1) describes the residual energy stored in the leakage inductor.

$$E_{ds} = \frac{1}{2} L_{leakage} I_{\max}^2 . \quad (1)$$

The voltage across C_{staore} is approximately constant, with

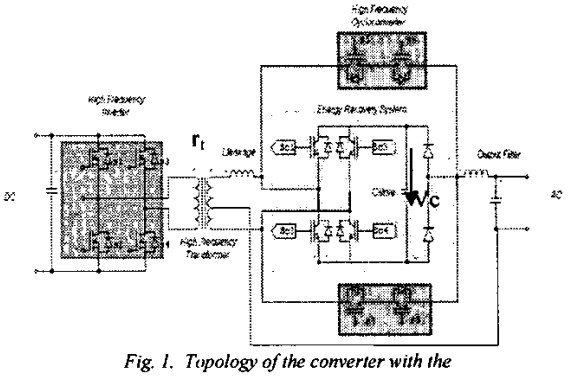

Fig. 1. Topology of the converter with the Regenerative Active Clamp

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a low AC component ($k*V_{c,av}$) because of the charge and discharge of the stored energy in the parasitic elements. This variable is a design parameter of the voltage clamper described by (2) and (3).

$$E_{ds} = \frac{1}{2} C_{store}\left(V_{c,\max}^2 - V_{c,av}^2\right), \quad \text{where} \quad V_{c,av} \cong V_{bat} r_t \tag{2}$$

$$V_{c,\max} = V_{c,av} + kV_{c,av} \tag{3}$$

where 'k' is equivalent to the maximum ripple admitted.

Combining expressions (2) and (3), the value of C_{store} can be found.

$$C_{store} = \frac{2E_{ds}}{V_{c,avg}^2(k^2 + 2k)} \tag{4}$$

An important factor in the design is the high values of di/dt circulating through the capacitor (snubber capacitor types are recommended).

III. Modulation Description

Usually this type of converters can be applied in isolated photovoltaic applications, where a high efficiency level is required to compensate the low efficiency of the photovoltaic panels. To achieve this point, soft-switching techniques are recommendable. A ZVS commutation is applied in the transitions of the inverter while in the transistors of the high frequency cycloconverter a ZCS technique is applied.

Different modulations of the transistors of the first stage exist [8], [9]. In our case, we have applied a modulation sequence based on a sine Pulse Width Modulation (sPWM) with step for zero. This modulation pattern presents the great advantage that reduces the number of commutations of the transistors in the high frequency cycloconverter, with some dependence of the inductive characteristic of the load.

The modulation of the first-stage high-frequency inverter is explained in Fig. 2. The sPWM signal is created comparing a high frequency sawtooth signal with a low frequency sine. With this sPWM signal the different modulation signals of the transistors of the first stage are generated. Later on, a blanking time is added to these signals.

For the modulation of the transistors of the full bridge, the previous signal is combined with another square signal of fixed duty (0.5), synchronous with the previous one, called *ClkInv*. The *sPWM* signal transmits the required pulse width for each instant of time in a leg; for the other leg the square signal connects alternatively to the positive or negative point of the battery at switching frequency. In this form the low frequency component can be eliminated, leaving alone the high-frequency components. The low frequency component (line frequency) will be easily reconstructed with the cycloconverter operating as a diode bridge, in the case of positive rectification. In the case of being in the negative half cycle, the cycloconverter operates in negative rectification mode. In this way, the transformer saturation is avoided without the necessity of increasing the volume of the transformer. Eqs. (5)-(8) describe the modulation of the transistors.

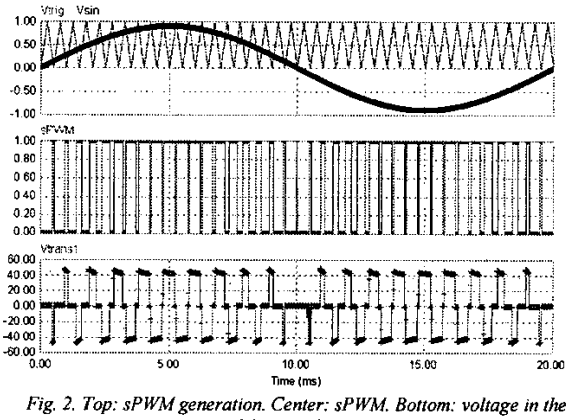


Fig. 2. Top: sPWM generation. Center: sPWM. Bottom: voltage in the input of the transformer, Vtr1.

$$S1 = \overline{ClkInv} * \overline{sPWM} + ClkInv * sPWM \tag{5}$$

$$S2 = \overline{S1} = ClkInv * \overline{sPWM} + \overline{ClkInv} * sPWM \tag{6}$$

$$S3 = \overline{ClkInv} \tag{7}$$

$$S4 = \overline{S3} = ClkInv \tag{8}$$

For the generation of the modulation signs there is a series of restrictions to avoid the converter failure. The operation principle is very simple. First, the high-frequency inverter legs cannot be short-circuited. Second, all inductors, especially the output inductor in our case, can never be in open circuit. These rules can be translated into logic expressions as:

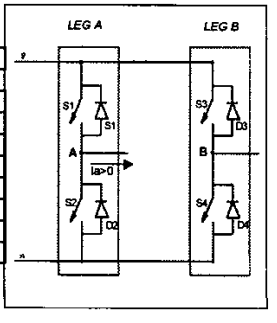
$$\left.\begin{array}{l} S1 + S2 = 0 \\ S3 + S4 = 0 \end{array}\right\} \quad \text{where} \quad \left.\begin{array}{l} Si = 1 \rightarrow on \\ Si = 0 \rightarrow off \end{array}\right\} \tag{9}$$

The operation principle in the generic case, in a leg, is described in Table I.

From Table I it follows that the voltage in point A, V_A, is not only a function of the transistors state, but also fro m the sign of the current, I_A. Then:

TABLE I: TRUTH TABLE OF THE LEG A

S1	S2	sgn (Ia)	Va	Cond
0	0	+	n	D2
0	1	+	n	D2
1	0	+	p	Q1
1	1	+	s.c.!	X
0	0	-	p	D1
0	1	-	n	Q2
1	0	-	p	D1
1	1	-	s.c.!	X



$$V_A = S_1 + \overline{S_2} \bullet \overline{I_A} \tag{10}$$

where I_A is positive when the current go out of the leg. In a analog form the voltage in the middle point of the other leg can be expressed:

$$V_B = S_3 + \overline{S_4} \bullet I_A \quad \text{where} \quad I_A = -I_B \tag{11}$$

In the ideal case, starting from the two previous expressions, (10)-(11), the input voltage in the high frequency transformer can be described in (12).

$$V_{AB} = \left\{ (S_1 + \overline{S_2} \bullet \overline{I_A}) - (S_3 + \overline{S_4} \bullet I_A) \right\} \cdot V_{BATT} = V_{tr1} \tag{12}$$

A. First Stage Modulation and Blanking Time

In the commutation of the switches of the first stage, a transition is carried out between the conduction of the upper transistor and the conduction of the lower transistor. During this transition it is mandatory that the two transistors of one leg are never driven at the same time.

To guarantee this restriction, a blanking time is used. In this period of time the elements that entered in conduction will be the MOSFET of a leg and the diode of the other one. Therefore, the voltage across the terminals of the high frequency transformer will be lower. This voltage can be determined by (13):

$$\langle \Delta V \rangle = \frac{t_{blanking}}{T_s} (r_{on} I_{rms} + v_{diode}) \tag{13}$$

The sequence utilized can be seen in Fig. 3. The first interval corresponds the one when the transformer input voltage equals the input voltage. This interval is characterized by the sequence (S1,S2,S3,S4)=(1,0,0,1), and marked as "+". The current flows through r_{ON} of S1 and S4.

The next step is to turn off S4; then the gate signals of the inverter are (1,0,0,0), interval 2. When S4 is turned off the energy stored in the inductive load and in the inductive parasitic elements causes terminal B to swing towards the DC power rail, through the anti-parallel diode of the transistor S3. This interval is marked as "*", and the current through transistor S4 will be extinguished.

The third interval is defined when the voltage on terminal B reaches the DC power rail, S3 is turned on and the H–bridge enters in interval 3. The load current circulates through switches S1 and S3 and the gate signals are (1,0,1,0). This interval is marked as "0".

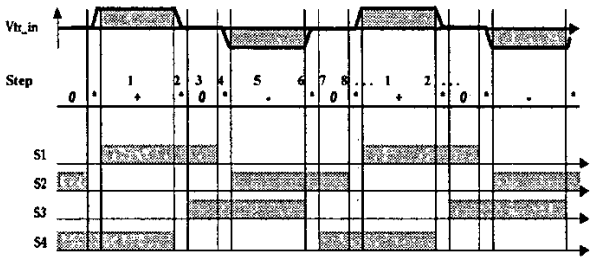


Fig. 3. Temporally sequence of the gate transistors signals

Interval 3 ends when S1 is turned off. Then, the gate signals of the H-bridge are (0,0,1,0) and the current flows through D2 and D3. This interval is called "*" too, interval 4.

When the voltage on load terminal A reaches ground, S2 is turned on, and the H–bridge enters interval 5. This is the reverse conduction state and the gate signals are (0,1,1,0). Current flows through the load from right to left until another direction change is initiated.

Then, another transient step will be in the sequence, in the interval 6. This one has the sequence (0,1,0,0).

Finally, there is another transition step, interval 7, then in interval 8 the voltage seen by the transformer will be zero, and later on the commutation sequence repeats again.

The switches in the inverter should have a small blanking time so that there is no reduction in the maximum value of the output voltage [10]. This minimum blanking time is expressed by (14).

$$t_{blanking} \geq \frac{2 V_{bat} C_{switch}}{I_o} \tag{14}$$

A simple method to get ZVS consists in adding a polypropylene capacitor that presents a fast dynamic to high frequencies, coupled with C_{OSS}, the parasitic capacitor of the transistor [11]. In this way, previously to the turn-on of the transistor, the capacitor in parallel with the transistor will be discharged. When the discharge is completed, the voltage across the transistor is practically null and then the current starts to circulate.

This effect decreases the switching losses of the transistors of the first stage; nevertheless, a slightly higher switching time is required in comparison with the hard-switching operation time of the transistor.

B. Second Stage Modulation and Overlapping Time

Similarly to the modulation of the first stage, there is a series of forbidden gate signals for the modulation of the second stage.

One of the main conditions is that the output inductance could never be in open-circuit, since a surge would be capable to destroy the transistors of the circuit. Another point is never short-circuiting the secondary of the transformer when there is voltage across it.

In Table II the acceptable states among the 16 possible for the modulation of the cycloconverter are detailed. In Table II the schematic of the half bridge cycloconverter is attached to clarify the terminology. Table II shows, in function of the gate signals of the transistors S5-S8, the sign of the input voltage of the transformer sgn(Vtr1)=sgn(Vtr2) and the current through the inductance of the output filter, the point where the half point of the second power stage "M" is connected. In the table, "o.c." stands for open-circuit in the output filter, and "s.c." stands for short-circuit in the transformer.

As a result of the analysis of the different states of the second power stage, the conditions that the gate signals must verify in any time, included in the transients, are given

TABLE II
MODULATION TABLE OF THE CYCLOCONVERTER GATE SIGNALS

s5	s6	s7	s8	M: Vtr2>0 iL<0	M: Vtr2>0 iL>0	M: Vtr2<0 iL<0	M: Vtr2<0 iL>0
0	0	0	0	o.c.	o.c.	o.c.	o.c.
0	0	0	1	o.c.	Y	o.c.	Y
0	0	1	0	Y	o.c.	Y	o.c.
0	0	1	1	Y	Y	Y	Y
0	1	0	0	o.c.	X	o.c.	X
0	1	0	1	o.c.	Y	o.c.	X
0	1	1	0	Y	X	s.c.	s.c.
0	1	1	1	Y	Y	s.c.	s.c.
1	0	0	0	X	o.c.	X	o.c.
1	0	0	1	s.c.	s.c.	X	Y
1	0	1	0	X	o.c.	Y	o.c.
1	0	1	1	s.c.	s.c.	Y	Y
1	1	0	0	X	X	X	X
1	1	0	1	s.c.	s.c.	X	X
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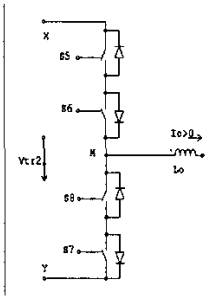

by (15)

$$\left.\begin{aligned} S5+S7=0 \\ S6+S8=0 \end{aligned}\right\} \quad \text{where} \quad \left.\begin{aligned} Si=1\rightarrow on \\ Si=0\rightarrow off \end{aligned}\right\} \tag{15}$$

As it has been previously mentioned, the modulation of the second stage, the cycloconverter stage, rectifies the output voltage of the transformer. This is equivalent to a positive rectification when $V_{OUT}>0$ and $I_{OUT}>0$, and a negative rectification when $V_{OUT} < 0$ and $I_{OUT}<0$. This simplifies the modulation pattern, whenever the sign of the output current is, this pattern is in phase with the sign of the output voltage and the state of the transistors will be stable. In these two modes the commutation of the cycloconverter can be simplified as in Fig. 4.

Additionally, the cycloconverter switches should have an overlapping time determined by (16):

$$t_{overlap} \geq \frac{2I_{out}L_{leak}}{V_{tr1}\cdot r_T} \tag{16}$$

If the sign of the output voltage is different than the output current sign, the commutation of the transistors of the cycloconverter will be as it is explained now.

This delay can be implemented by a compensation of the PWM waveform. The presented modulation has the advantage that the sign of the current circulating through the output filter is not required. In this way all the output inductor current sensors can be removed reducing the complexity and cost of the final system. The modulation proposed requires the sign of the transformer output voltage, but that is previously established by the modulation signals of the high frequency inverter. So there is not any additional sensor required to calculate the modulation sequence.

The cycloconverter modulation depends on the input voltage polarity as input signal to create the reference signal sPWM. The example of the sequence signals for one leg of the cycloconverter in the voltage mode reference is shown in Fig. 5 at Vtr2>0 and iL>0. In the other cases the sequence to apply can see in the Fig. 6.

Interval 0 The current flows through Q_{11} and the diode D_{12}. This state is bi-directional and does not depend on the current sign.

Interval 1 The transistor Q_{22} is turned on. The commutation of the transistor Q_{22} is ZCS. Then, there is a soft switching with a significant loss reduction

Interval 2. Q_{11} is turned off, the current changes the path under a hard switching, limited by the parasitic inductances of the leg.

Interval 3. In this point the current flows through Q_{22} and diode D_{21}. So the transistor Q_{12} can be turned off under ZCS.

Interval 4 Finally, all the commutations are finished.

The rest of the cases can be analyzed in a similar way. It is important to note that the presented sequence is the same for Io>0 than for Io<0.

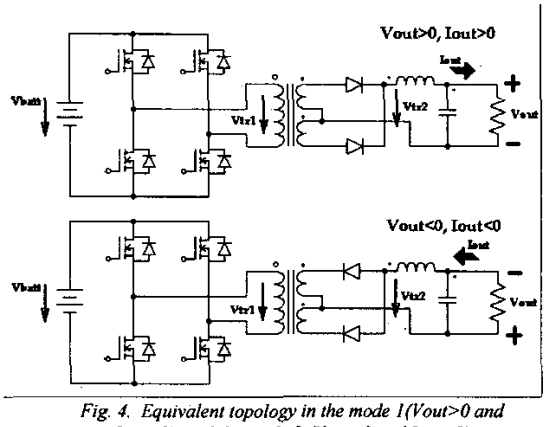

Fig. 4. Equivalent topology in the mode 1(Vout>0 and Iout>0) and the mode 3 (Vout<0 and Iout<0)

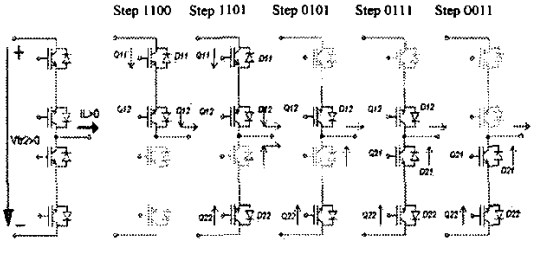

Fig. 5. Equivalent intervals in a transition in the mode 1

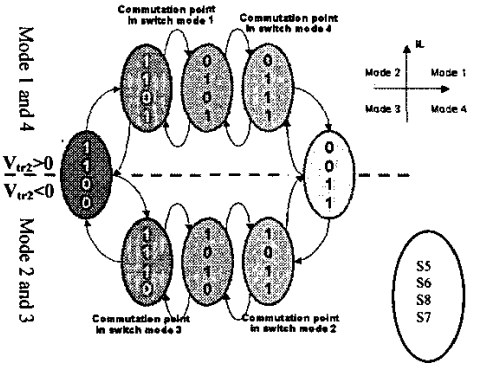

Fig. 6. Transition of the modulation state in the gate signals of the transistors in the cycloconverter

IV. SELECTION OF THE SWITCHES

For the selection of the switches in the power converter the following selection criteria have been developed. As it is well known, MOSFETs are faster than IGBTs, however, both devices are available for the selected frequency. Therefore this is not a good selection criterium [12] and [13].

IGBTs are well suited to applications which take advantage of their ability to switch high voltages and low currents, where the conduction loss incurred by the $V_{ce(sat)}$ of the device is usually lower than the forward conduction loss of a MOSFET with a equivalent voltage rating (if such a MOSFET even exists). On the other hand MOSFETs is well suited to switch high currents and low voltages. Consequently we will use MOSFETs for the commutation in the high frequency inverter and IGBTs for the commutation in the high frequency cycloconverter.

Equations (17)-(18) determine the conduction losses of the transistor and the diode, assuming sine current waveforms [14].

$$P_{cond} = \frac{1}{2}\left(\frac{V_{CE0}}{\pi}\hat{i} + \frac{r_{ce}}{4}\hat{i}^2\right) + m\cdot\cos\varphi\cdot\left(\frac{V_{CE0}}{8}\hat{i} + \frac{r_{ce}}{3\pi}\hat{i}^2\right) \quad (17)$$

$$P_{diode} = \frac{1}{2}\left(\frac{V_{F0}}{\pi}\hat{i} + \frac{r_f}{4}\hat{i}^2\right) - m\cdot\cos\varphi\cdot\left(\frac{V_{F0}}{8}\hat{i} + \frac{r_f}{3\pi}\hat{i}^2\right) \quad (18)$$

Where V_{CE0} is equal to threshold voltage of the output characteristic with i_C=0, r_{CE} is equal to on-state resistance of the IGBT, V_{F0} equivalent to threshold voltage of the forward characteristic with i_F=0 and r_F is the dynamic on resistance. These equations are formulated for the calculation of the losses in an IGBT, but are extrapolables to the case of a MOSFET. The product m·cos(φ) determines how the total power dissipation is divided up between IGBT or MOSFET and the diode

V. HIGH FREQUENCY TRANSFORMER

One of the most important elements in the power converter is high frequency transformer. A good transformer design is important to minimize the parasitic components.

One of the more dangerous parasitic elements is the leakage inductance. This parasitic can cause that the second stage has to commutate a current source in both sides, instead of a voltage source in one side (the transformer) and a current source in the other one (the filter inductor). So if any residual current is circulating through the leakage inductances and the circuit is in open circuit an over voltage is generated. Therefore, a good commutation strategy must never leave the transformer secondary in open circuit. Another important factor is reseting the residual current in the leakage inductances.

For the design of the power transformer, the selection of the core material is the first step, as described in [15]. In the market, different advanced compounds that assure some good working conditions are available and with very low power/mass ratios. PERMALLOY80 has one of the best ratios, with a low resistance in continuous and in alternating regimes. This compound has the drawback that is not used extensively what implies a relatively high cost. Inside those made up with a better performance is FERRITE PC40, this compound presents similar (but lower) characteristics to the previous one. Nevertheless, their price and their availability makes it a good choice.

The second point to reduce the leakage flux of the high frequency transformer is in the winding layout. Not only it is looked for eliminating the leakage flux but also reducing skin effect that increases the alternating resistance. With the objective of minimizing the previously described parasites a good technique consists in making a sandwich of the secondary winding with the primary winding. This layout eliminates the circulation through the air and consequently the leakage flux.

VI. VOLTAGE ACTIVE CLAMPER MODULATION

With this topology the major disadvantage is that the transformer leakage inductance causes high transient voltage across the bridge switches, which increases the switching rating and decreases the reliability.

The proposed soft switching circuit clamps the voltage across the high frequency output through a full bridge diodes and store the energy in a capacitor, transfering later on the energy in the leakage inductance to the load.

The operation of this subcircuit will be described. When the current path is cut and the diodes change to a state conduction, a resonance period between leakage inductor and C_{store} will occur. It must be larger than the energy transferring period. With this method the energy stored in the transformer and other parasitics will be absorbed by C_{store}. Then, when the main circuit returns to a conduction stage, C_{store} discharges through the transistors of the active voltage clamper to the load. Then, this circuit only works when the freewheeling path of the cycloconverter is closed. Then, a low overvoltage may occur. When the transformer voltage is higher than the voltage across C_{store} the diodes of the voltage clamper are turned on.

The voltage across the points called 'p' and 'n' is always positive, then to discharge the capacitor the transistors that will be active must be *Sc1* and *Sc4* when the voltage at high frequency transformer is positive. The opposite transistors conduct, *Sc2* and *Sc3*, when the voltage across the transformer is negative, see Fig. 7.

This subcircuit has the advantage that increases the global efficiency of the system and eliminates the overvoltage across the switches and other devices of the power converter. On the other hand, this system increases the cost and the complexity of the converter. In order to reduce the cost, the driver circuits can be replaced by a simple pulse transformer as shown in Fig. 7. Additionally the control waveforms can be obtained directly from Vtr2, with an additional cost reduction.

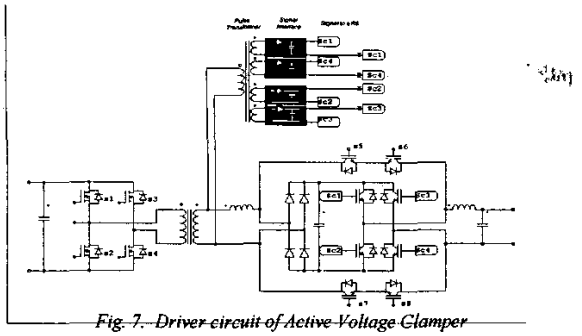

Fig. 7. Driver circuit of Active Voltage Clamper

The required transformer consists in a high frequency pulse transformer with a primary to an input of Vbat*rt ac Volts, while the secondaries must must work to the voltage required by the transistor of the energy recovery system, usually 15 Vac.

For the cost reduction of the final prototype, this pulse transformer can be added to the main power transformer.

VII. SIMULATIONS

To show the effectivity of the modulation and the clamper circuit some simulations have been done. The conditions of the simulations are the same of the actual case: V_{in}=48V, $V_{out,rms}$=230V, P_{out}=2kW, f_s=20kHz, f_{out}=50Hz, L_{out}=3mH, C_{out}=10uF, r_T=10 and r_{LOAD}=35Ω. In the results, a good performance of the modulation applied at the converter at nominal power is observed. First, the output voltage in a full period is shown in Fig. 8. Additionally, the high frequency cycloconverter voltage is shown. The elimination of any overvoltage is verified. The second representation shows the waveforms of the currents through the output filter.

The Fig. 9 shows all currents and voltages relationed with the performance of the Active Voltage Clamper as well as the transformer output voltage.

The waveforms that are observed in Fig. 9 show the charge and discharge cycle of the campling capacitor. The energy storing phase from the leakage inductances and the later recovery to the load are observed.

To verify the correct operation of the voltage clamper system, a prototipe has been constructed as seen in Fig. 10. The experimental results are shown in Fig. 11. The experiments have been done with a resistive load of 35Ω. The waveforms in Fig.11 show how the output voltage of the high frequency transformer has no overvoltages (CH1). This waveform has been acquired with the same reference as the voltage across C_{store} (CH3). The cycloconverter output voltage is shown (CH2), together with the load current, for comparison purposes. It is clear that the output distortion is minimal.

VIII. CONCLUSION

One of the most important problems in the high-frequency converters consists in the absence of freewheeling paths to discharge the leakage inductances of the high-frequency transformer. This fact not only reduces the efficiency of the converter, but also produces overvoltages that can destroy the switches. To avoid this, it is necessary to assure a permanent path to discharge the energy stored in the parasitics of the transformer. An active regenerative clamp circuit to return this energy to the load in a secure way is presented, as well as the design of the control circuit. To increment the efficiency in the converter, soft-switching techniques are used. The clamp circuit is specially interesting when working at high frequency.

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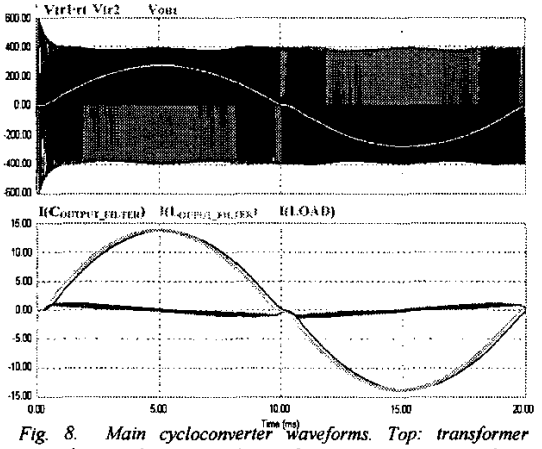

Fig. 8. Main cycloconverter waveforms. Top: transformer secondary voltage (Vtr2), cycloconverter output voltage (Vpwmout), output voltage (Vout). Bottom: filter inductor current (iLout), filter capacitor voltage (iCout), load current (iR9).

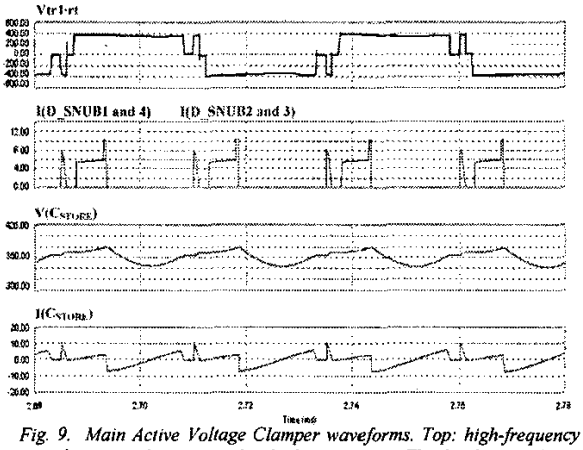

Fig. 9. Main Active Voltage Clamper waveforms. Top: high-frequency transformer voltage.Second: diodes current. Third: C_{store} voltage. Bottom: C_{store} current, showing energy recovery.

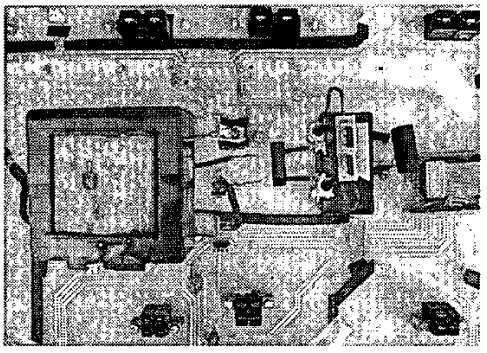

Fig 10 Detail of the high-frequency transformer and the active clamp circuit.

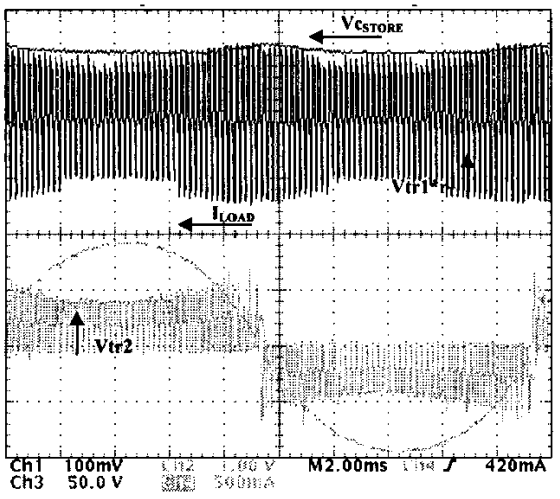

*Fig 11 Experimental results: CH1 50V/div Vtr1*r_T, CH2 50V/div Vtr2, CH3 50V/div V_{CSTORE}, CH4 500mA/div*

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