Experimental characterization of NBTI effect on pMOSFET and CMOS inverter

R. Fernández[a]*, B. Kaczer[b], J. Gago[a], R. Rodriguez[c], M. Nafría[c]
[a]*Dept. d'Enginyeria Electrònica, Universitat Politècnica de Catalunya, Colom 1 E-08222-Terrassa*
[b]*IMEC, Kapeldreef 75, B-3001 Leuven, Belgium*
[c]*Dept. d'Enginyeria Electrònica. Universitat Autònoma de Barcelona, Edifici Q, E-08193 Bellaterra*
[*] *Corresponding author*: +34 93 739 80 89; Fax: +34 93 739 80 16; e-mail: rfernan@eel.upc.edu

***Abstract*— In this paper, an experimental characterization of Negative Bias Temperature Instability (NBTI) effects on a single pMOSFET and CMOS inverter is done. The characterization has been performed for static and dynamic stresses with frequencies ranging from DC to GHz. The results show that NBTI produces a threshold voltage shift (ΔV_T) on pMOSFETs, which is frequency independent. For DC stress, this ΔV_T is double than in the AC case. In a CMOS inverter, NBTI produces a voltage transfer curve shift which is expected theoretically. As ΔV_T, in a single pMOSFET, the voltage transfer curve shift in a CMOS inverter is frequency independent and almost double for DC stress in comparison to the AC case.**

I. Introduction

The Negative Bias Temperature Instability (NBTI) is one of the main present and future reliability problems [1]. Nowadays, CMOS circuits are working from DC up to the GHz range, but not many dynamic NBTI (AC-NBTI) works have been reported [2]-[4] and are always focused on frequencies below a few MHz. In this paper, the NBTI effects on pMOSFET and CMOS inverter are experimentally investigated from DC to GHz. In order to do that, on-chip circuits have been fabricated [5].

II. Experimental

The samples under test are pMOSFETs with an aspect ratio of 2µm/0.13µm and CMOS inverters with aspect ratios of 3µm/0.13µm and 6µm/0.13µm, for the nMOSFET and pMOSFET respectively. Fig. 1 depicts the stress setup. A constant voltage of 0V or a square signal from 0-2V were applied to the gate/inverter input for the static (DC) and dynamic (AC) stresses, respectively. In both cases, 2V were applied to the rest of terminals, Depending on the stress frequency, an external pulse generator (DC-MHz) or on-chip stress circuits (MHz-GHz) have been used to provide the AC stress waveform. All the measurement have been done at 125°C at exponentially increasing periods of time.

The stress-measurement sequence is shown in Fig.2. First of all, the I_D-V_G pMOSFET characteristic is measured (the Voltage Transfer Curve, VTC, in case of CMOS inverter), the data are saved and the stress is applied. After stress, the I_D-V_G transistor curve (or the VTC of the inverters) are again measured and the data saved. If the sequence is not finished the stress time is exponentially increased and the stress is again applied. If the stress-measurement is finished the data are analysed and the threshold voltage shift (ΔV_T)is obtained.

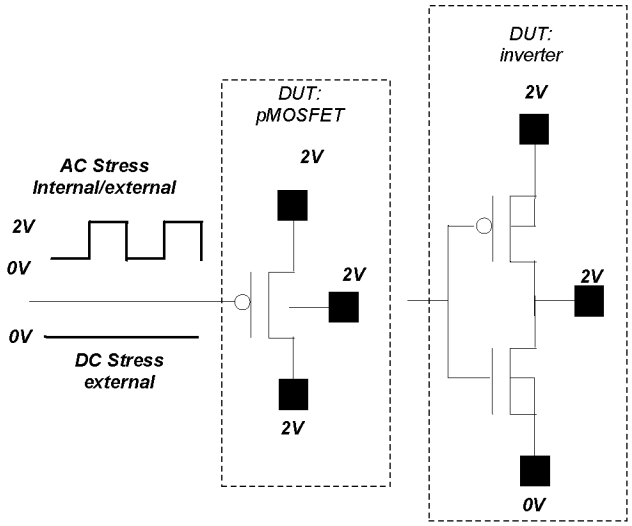

Fig. 1: Stress setup for static and dynamic NBTI measurement. Depending on the AC stress frequency, the stress signal is externally or on-wafer generated.

III. Results

Fig. 3 shows the I_D-V_G curve of a fresh and stressed pMOSFET. From these characteristics, ΔV_T has been obtained for a constant current of 10µA. For the stressed transistors the I_D-V_G curve is shifted and therefore, $|V_T|$ increases,

Fig. 4 represents ΔV_T as a function of the stress time of pMOSFETs subjected to DC and AC (7.4MHz) NBTI stresses. In both cases, ΔV_T follows a power law dependence with the stress time and an exponent around 0.20 is obtained. However, in the case of AC stress, ΔV_T is almost half of the one obtained for the DC case. For instance,, for 1000s stress (125°C and 2V) the ΔV_T is around 40mV and 20mV for the DC and AC stresses respectively. .

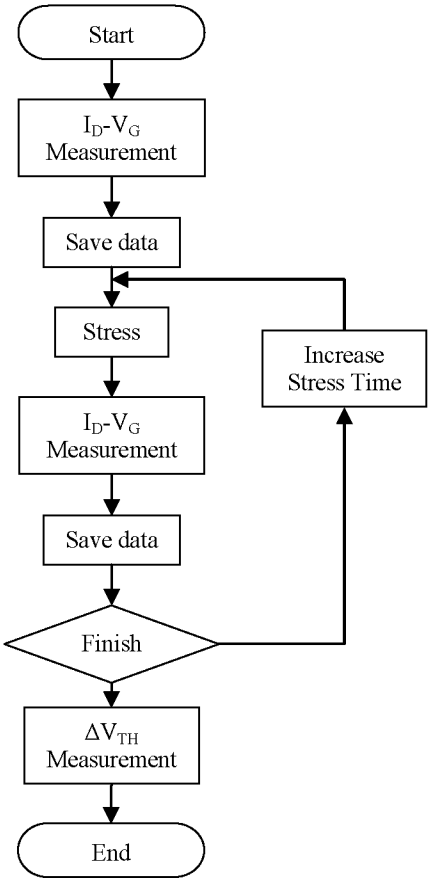

Fig. 2: Stress-measurement sequence.

In order to evaluate the ΔV_T dependence with the stress frequency, an AC stress swept has been applied to the gate. For frequencies from 1Hz to 1MHz an external pulse generator was used. The AC stress voltages from 1MHz - 2GHz were obtained from a on-wafer pulse generator [5]. Fig. 5 shows the ΔV_T frequency dependence for 1000s stress (125°C, 2V). The plot confirms that ΔV_T is independent of frequency in the wide range of 1 Hz – 2 GHz and the ΔV_T value obtained under AC stress is almost the half of the DC case. However, a low ΔV_T measured at 1MHz (the highest frequency measured using an external pulse generator) is observed. This lower value of ΔV_T can be attributed to the loss of the stress signal integrity due to a setup parasitic effect, which, on the other hand, could explain the frequency dependency reported in other works and demonstrates the need of on-chip NBTI characterizations.

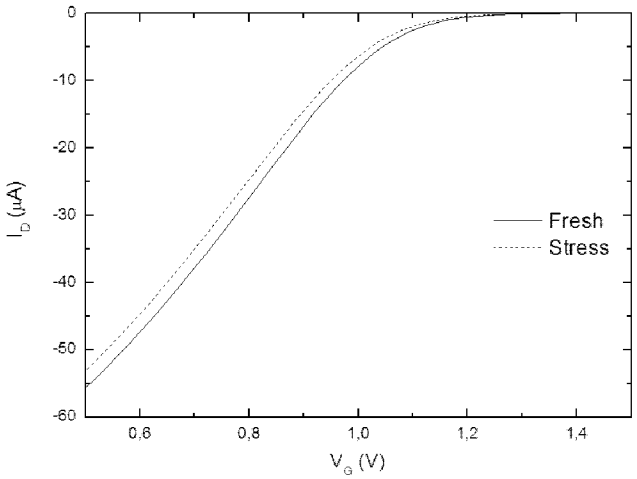

Fig. 3: I_D-V_G characteristic of a fresh pMOSFET and after 1000s NBTI stress (125ºC, 2V).

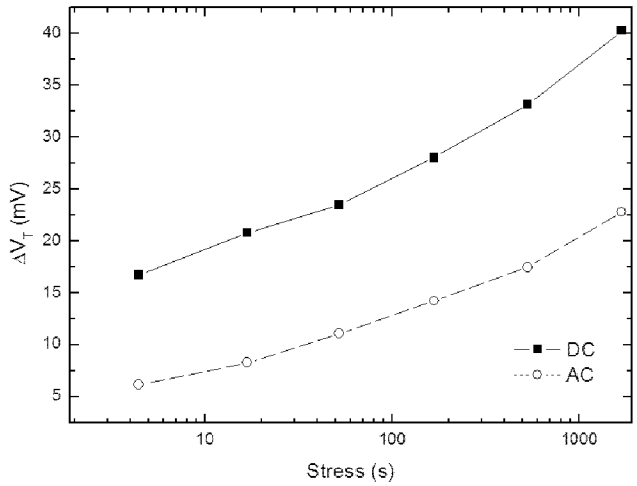

Fig. 4: ΔV_T as a function of t_{stress} for DC and AC NBTI stress conditions. In both cases ΔV_T follows a power law with exponents around 0.20.

CMOS inverters have also been subjected to DC and AC stresses. In order to quantify the NBTI effects, the maximum gain point shift of the inverter voltage transfer curve has been used (ΔV_{IN}). The theoretical relationship between ΔV_{IN} and the inverter pMOSFET ΔV_{TP} is given by equation (1).

$$\Delta V_{IN} = \frac{\Delta V_{TP}}{1+\sqrt{\frac{\mu_N (W/L)_N}{\mu_P (W/L)_P}}} \qquad (1)$$

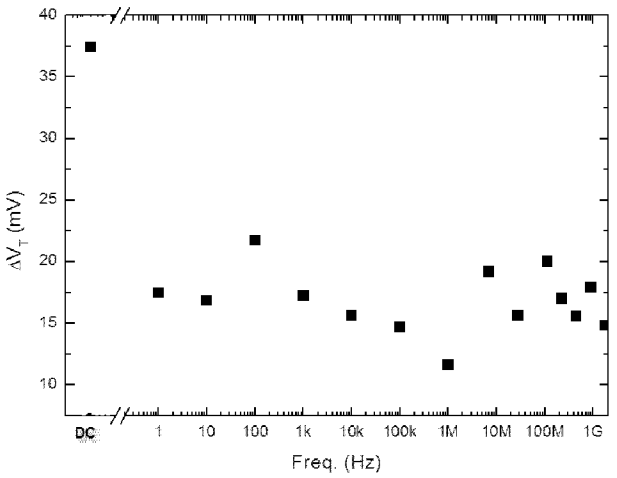

Fig. 5: Frequency dependence of V_T shifts due to AC NBTI stress in a single pMOSFET

μ denote the carrier mobility and W/L the transistor aspect ratio. The CMOS inverter under test has been designed in order to achieve the maximum gain point at $V_{DD}/2$, so $\mu_N(W/L)_N = \mu_P(W/L)_P$. Forcing this condition, the ratio between ΔV_{TP} and ΔV_{IN} is given by equation (2).

$$\Delta V_{IN} = \frac{\Delta V_{TP}}{2} \qquad (2)$$

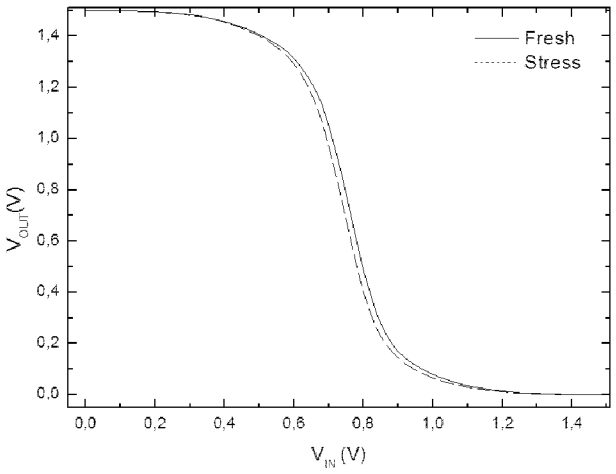

Fig. 6: The inverter voltage transfer curve before and after 1000s NBTI stress (125ºC, 2V).

In Fig. 6 the inverter voltage transfer curve before and after NBTI stress is plotted. A voltage transfer curve shift is produced after NBTI stress. Fig. 7 shows the ΔV_{IN} frequency dependence. Again the shift produced due to AC stress is almost half of the DC case. Moreover, if ΔV_T of a pMOS transistor (Fig.5) is compared with ΔV_{IN} of the inverter (Fig.7), it is observed that ΔV_{IN} is almost half of ΔV_T, which is predicted theoretically by equation (2). This result confirms that the NBTI impact on CMOS inverter functionality is only due to the NBTI effect on the single inverter pMOSFET.

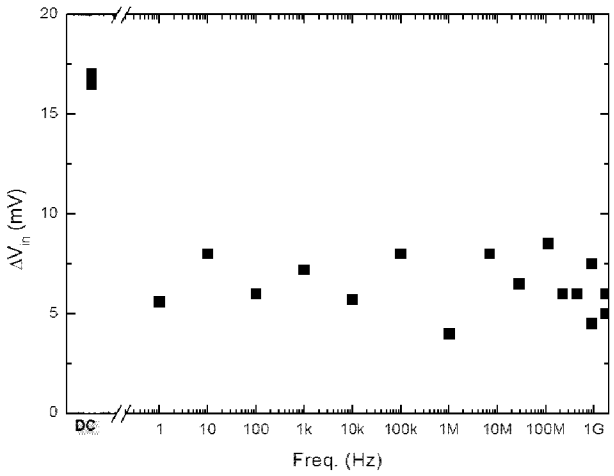

Fig. 7: Frequency dependence of the inverter maximum gain point shift, ΔV_{IN} ,due to AC NBTI stress.

IV. Conclusion

Experimental characterization of NBTI effect on single pMOSFETs and CMOS inverters has been done. The results indicate that i) the NBTI impact on transistor performance subjected to AC stress is almost half of the DC case. ii) AC NBTI is independent of frequency in the entire 1 Hz – 2 GHz range iii) the effect of NBTI in the CMOS inverter functionality is only due to NBTI effects on the inverter pMOSFET.

Acknowledgment

This work has been partially supported by the Spanish Government (TEC2004-00798/MIC and TEC2007-61582), the European Commission (Marie Curie Actions, APROTHIN Project) and the Generalitat de Catalunya (2005SGR-00061).

References

[1] Reddy, V.; Krishnan, A.T.; Marshall, A.; Rodriguez, J.; Natarajan, S.; Rost, T.; Krishnan, S.; Impact of negative bias temperature instability on digital circuit reliability, Proc. IRPS, p. 248 (2002).

[2] Abadeer, W.; Ellis, W.; Behavior of NBTI under AC dynamic circuit conditions, Proc. IRPS, p. 17 (2003).

[3] Chakravarthi, S.; Krishnan, A.; Reddy, V.; Machala, C.F.; Krishnan, S.; A comprehensive framework for predictive modeling of negative bias temperature instability, Proc. IRPS, p. 273 (2004).

[4] Alam, M.A.; A critical examination of the mechanics of dynamic NBTI for PMOSFETs, IEDM Tech. Digest, p. 345 (2003).

[5] Fernandez, R.; Kaczer, B.; Nackaerts, A.; Demuynck, S.; Rodriguez, R.; Nafria, M.; Groeseneken, G.; AC NBTI studied in the 1 Hz ý 2 GHz range on dedicated on-chip CMOS circuits, IEDM Tech. Digest, p. 1 (2006).