A new switching frequency modulation scheme for EMI reduction in multiconverter topology

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Acknowledgements

This research is supported by "Ministerio de Ciencia e Innovación de España", in the frame of the project TEC2007-61582.

Keywords

EMC/EMI, Interleaved Converters, Power supply, Switched-mode power supply.

Abstract

This paper presents a modulation scheme in order to reduce conducted Electromagnetic Interference (EMI) generated by modular power converters with parallel topology. The proposed scheme is based on a combination of interleaving and Switching Frequency Modulation (SFM) techniques. The objective of this modulation scheme is to cancel certain harmonics of EMI and to reduce the amplitude of the remaining harmonics. The proposed scheme has been implemented in a field programmable gate array and a four channel parallel buck converter has been used in order to verify it. A significant EMI reduction has been obtained in comparison to use the interleaving and Switching Frequency Modulation separately.

Introduction

Power converters operate with switching signals which present high currents and voltages in periods of few microseconds. As a result, these kind of systems generate conducted Electromagnetic Interferences (EMI) in the power lines that can affect other circuits or devices. These interferences can be propagated through power and signal wires or coupling paths by electric and/or magnetic field. Consequently, the reduction of conducted EMI generated by power converters has become an important issue to study. In order to reduce conducted EMI several methods have been proposed in literature. The Switching Frequency Modulation (SFM) technique is a well-known method for conducted EMI reduction in power converters [1-6]. This technique consists of varying the switching frequency in order to generate a distribution of the energy of the interference harmonics in side-bands. This effect reduces the amplitude of each interference harmonics. In the last years, the SFM technique has been studied in different kind of centralized power systems, such as switching mode power supplies (SMPS) [1,2], resonant ballast [3], domestic induction cooking appliances [4], active filters [5] or drive motor [6]. However, according author's knowledge, in modular or distributed power systems (Fig. 1) the Switching Frequency Modulation technique has not been deeply evaluated.

The modular or distributed power systems present several advantages in comparison with centralized power systems, such as redundancy, better sharing of load currents and dynamic behaviour [7]. On the other hand, these kinds of systems have an important relevance in power supply industry. The modular power supplies with parallel topology (Fig. 1) are used in microprocessors powers supplies, which require high current level with low voltage level [7].

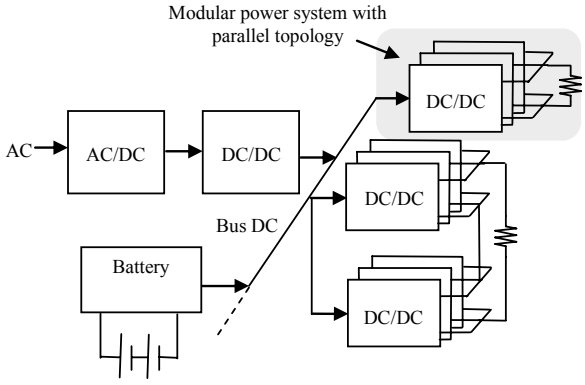


Fig. 1: Distributed power supply system.

In this work, a new switching frequency modulation scheme is proposed in order to reduce the conducted EMI in modular power supplies with parallel topology. In this type of systems is commonly used the interleaving technique as a good solution to reduce output voltage ripple [8,9] and conducted EMI [10,11]. The modulation scheme proposed, called switching frequency modulation with variable delay (VDFM), combines the interleaving and SFM techniques. The goal of this new modulation scheme is to cancel certain harmonics of EMI and to reduce the amplitude of the remaining harmonics.

The paper is organized as follows. First of all, the new modulation scheme (VDFM) is analysed. In the next section, the practical implementation used is described, paying special attention to the implementation of the modulation scheme in a field programmable gate array (FPGA). In order to verify the advantages of the proposed modulation scheme, the VDFM is compared with interleaving technique and standard Switching Frequency Modulation scheme in a four channel parallel buck converter. Finally, the main conclusions are summarized and some future works are pointed out.

Analysis of Switching Frequency Modulation with Variable Delay

The Switching Frequency Modulation with Variable Delay (VDFM) consists of combining the interleaving and SFM techniques. In the interleaving technique all converters operate with the same switching period (T_c) but a shift delay equal to T_c/N is introduced in the switching pattern ($c_i(t)$) of each converter, where N is the number of converters, as shown in Fig. 2a. From the point of view of noise generation, the equivalent source of noise pattern ($s(t)$) can be estimated by the addition of all single switching patterns. Consequently, the $s(t)$ pattern is equivalent to the noise generated by a single converter switching at a constant period N times below (T_c/N). However when the SFM technique is applied, the switching period is not constant. Therefore, in order to modulate in frequency each switching pattern and to apply the interleaving concept at same time, it is necessary to introduce a variable delay of pulse position, ε_k, in each instantaneous switching period (T_k). Figure 2b shows the switching patterns and the equivalent source of noise corresponding to N=4. The ε_k is constant and equal to 0 for the first switching pattern ($c_1(t)$), but it varies in the next switching patterns, depending on T_k. The delay of pulse position inside an instantaneous switching period is given by (1), where i identifies the converter ($i=1,2,...,N$).

$$\varepsilon_{k,i} = \frac{T_k}{N} \cdot (i-1) \tag{1}$$

When VDFM is applied, the equivalent source of noise corresponds to a switching frequency modulated pattern with a central frequency N times higher than the central frequency of each converter, as shows Fig. 2b. Theoretically, it is expected a cancelation of certain harmonics and amplitude reduction of the remaining harmonics.

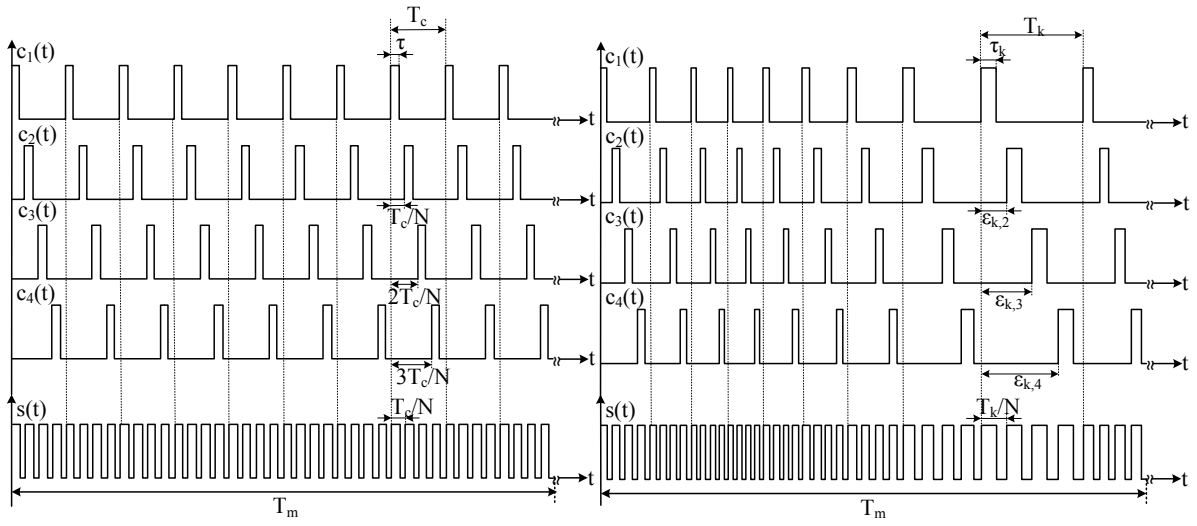


Fig. 2: Switching pattern and equivalent source of noise pattern for N=4. (a) Interleaving. (b) VDFM.

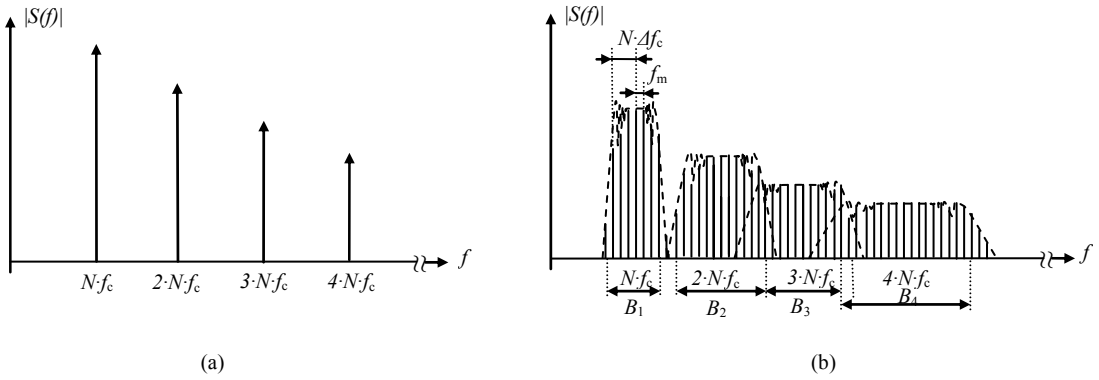


Fig. 3: Equivalent source of noise pattern spectrum. (a) Interleaving. (b) VDFM.

In Fig. 3a and Fig. 3b, the theoretical EMI spectrum for interleaving and VDFM is depicted. When the interleaving technique is applied, the shift delay introduced in each switching pattern does not change the amplitude of interference harmonics, but it modifies the harmonic phases. This effect produces a suppression of harmonics whose frequency is not multiple of N, only interference harmonics at frequency multiple of N appears, as demonstrates in [9]. Nevertheless, when each switching pattern is modulated in frequency and a variable delay of pulse position is introduced, the energy of each harmonics that have not been cancelled by means of interleaving technique is spread into side-bands harmonics.

The amplitude reduction of each interference harmonics improves as the modulation index (m_f) increases when the standard SFM method with a periodic modulation profile is applied [1,2]. The m_f depends on the maximum frequency deviation (Δf_c) and the modulation profile (f_m), as show in (2). However, the maximum value of Δf_c is limited by the operation of converter. Notice, that by using VDFM, the maximum frequency deviation corresponding to the equivalent source of noise pattern is N times higher than the maximum frequency deviation of each switching pattern. Therefore, the amplitude reduction of each interference harmonics that have not been cancelled by the interleaving technique also depends on the number of converters.

$$m_f = \frac{\Delta f_C}{f_m} \tag{2}$$

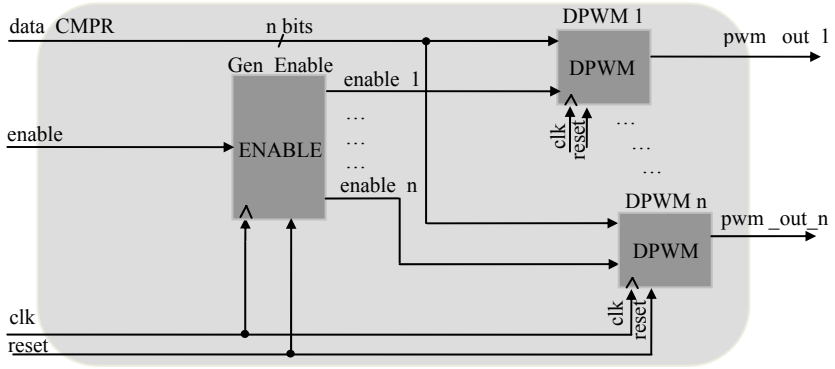
 ISBN: 9789075815009

Implementation

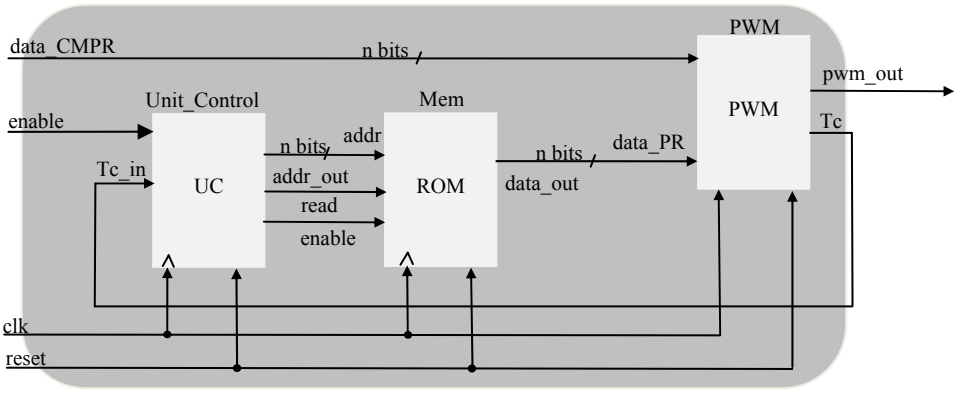
The switching pattern signals have been generated by means of several digital pulse width modulators (DPWM) that have been implemented in a field programmable gate array (FPGA). Figure 4a shows the block diagram which generates the *N* switching patterns. The value of node port *data_CMPR* adjusts the duty cycle and the *Gen_Enable* block allows introducing a shift delay between PWM signals. In order to implement the modulation scheme proposed, the initial delay of pulse position ($\varepsilon_{1,i}$) of each switching patterns is introduced as a shift delay between PWM signals by means of *Gen_Enable* block, and the next delays of pulse position are introduced modifying the instantaneous switching period of each PWM signals, as show in (3), where *i* identifies the converter ($i=1,2,...,N$), $T'_{k,i}$ indentifies the switching period corresponding at the *k* switching cycle for each converter and *L* is the number of switching cycles contained in a period of the modulation profile (T_m). In Fig. 5 the generating PWM signals is depicted.

$$T'_{k,i} = T_{k,1} + \frac{T_{k+1,1}}{N}\cdot(i-1) - \frac{T_{k,1}}{N}\cdot(i-1) \qquad for \quad k = \{1,2,...,L-1\}$$
$$T'_{L,i} = T_{L,1} + \frac{T_{1,1}}{N}\cdot(i-1) - \frac{T_{L,1}}{N}\cdot(i-1) \qquad for \quad k = L \tag{3}$$

The values of each instantaneous switching periods ($T'_{k,i}$) are used to calculated the clock cycles necessaries to generated the PWM signals. The values of these clock cycles are stored in a lockup table (*Mem* block), present in the block diagram of DPWM (Fig. 4b). In this case, the duty cycle are determined by comparing the counters implemented in each *PWM* block with the value of node port *data_CMPR*. The control signals in the DPWM unit are generated using a finite state machine (*Unit_Control* block).



(a)



(b)

Fig. 4: Block Diagram. (a) Generation of switching patterns. (b) DPWM with variable frequency.

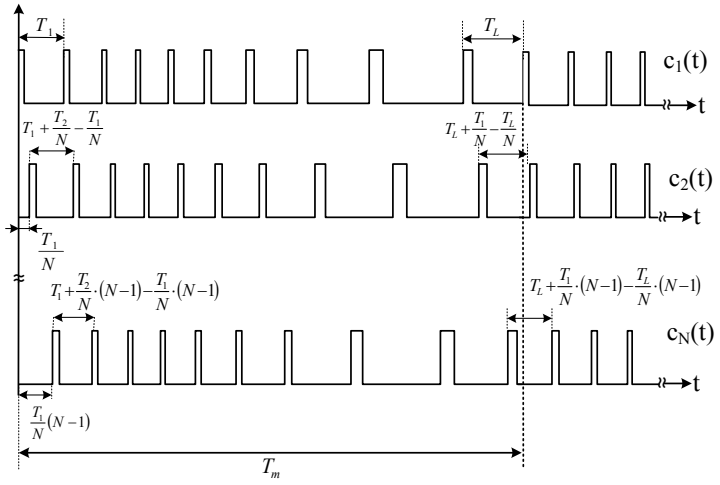


Fig. 5: PWM signals used by VDFM.

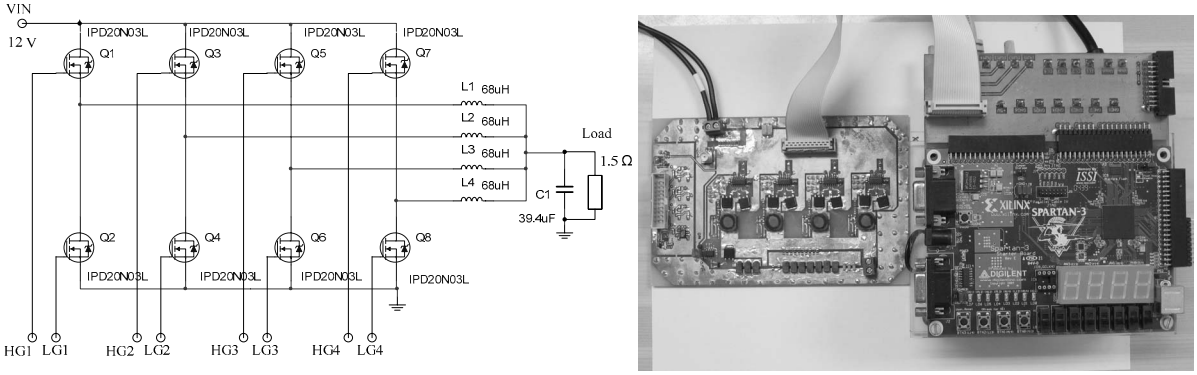
Experimental Results

The new modulation scheme, VDFM, have been validated in a four channel parallel buck converter, which is shown in Fig. 6. The operating conditions of each singular converter are summarized in Table I.

Table I: Main features of buck converters

Nominal Input Voltage	Nominal Output Voltage	Power	Switching Frequency
12 V_{DC}	1.5 V_{DC}	0.5 W	400 kHz

In order to evaluate the benefits of the modulation scheme proposed, the noise spectrum of parallel converter has been measured with a spectrum analyzer using a RBW equal to 9 kHz through a monophase line impedance stabilization network (LISN) in order to meet the criteria imposed by CISPR 16-1 [12]. The measurement setup is depicted on Fig. 7.



(a) (b)

Fig. 6: Four channel parallel buck converter prototype. (a) Schematic. (b) Full view prototype.

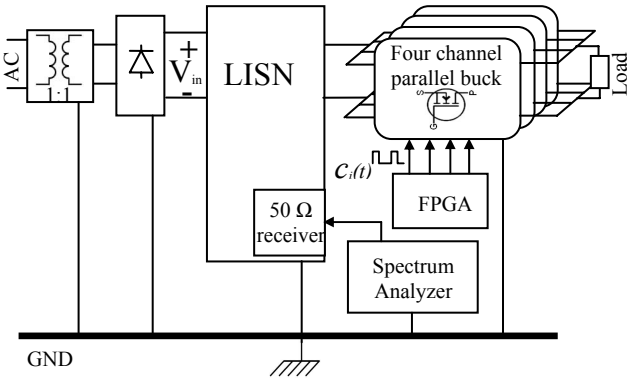


Fig. 7: Measurement setup.

First of all, the EMI spectrum of parallel buck converter obtained when the Switching Frequency Modulation and interleaving techniques are applied has been compared with the proposal modulation scheme. All alternatives have been measured in the following conditions: duty cycle D=0.15 %, central switching frequency f_c= 400 kHz, a triangular as modulation profile, $V_m(t)$, with a modulation frequency f_m= 10 kHz and a maximum frequency deviation Δf_c= 40 kHz.

Figure 8 shows the comparison between the EMI spectrum for the standard Switching Frequency Modulation scheme and Switching Frequency Modulation with Variable Delay scheme. The experimental results obtained demonstrate the effectiveness of this new modulation scheme presented. The VDFM provides an additional attenuation for frequencies lower than 4 times central switching frequency (f_c), only side-bands harmonics around at frequency multiple of 4 times central switching frequency appears. The side-bands harmonics around at switching frequency, two times switching frequency, three times switching frequency, etc, has been cancelled.

Figure 9 shows the comparison between the EMI spectrum for interleaving technique and Switching Frequency Modulation with Variable Delay scheme. When VDFM is applied, it is observed an additional amplitude reduction about 12 dB for the fundamental harmonic ($4 \cdot f_c$). This result confirms the theoretically expected result illustrated in Fig. 3b.

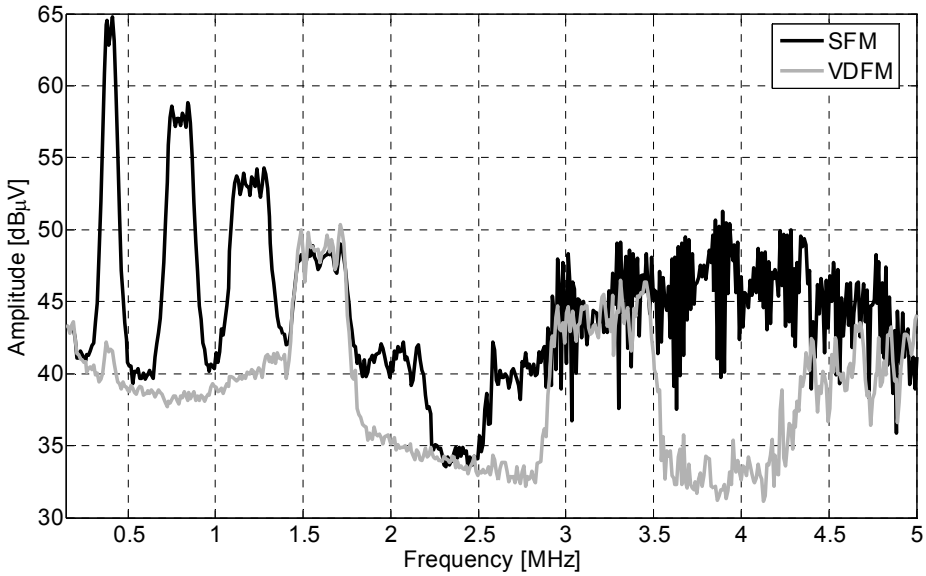


Fig. 8: Experimental EMI spectrum SFM vs VDFM.

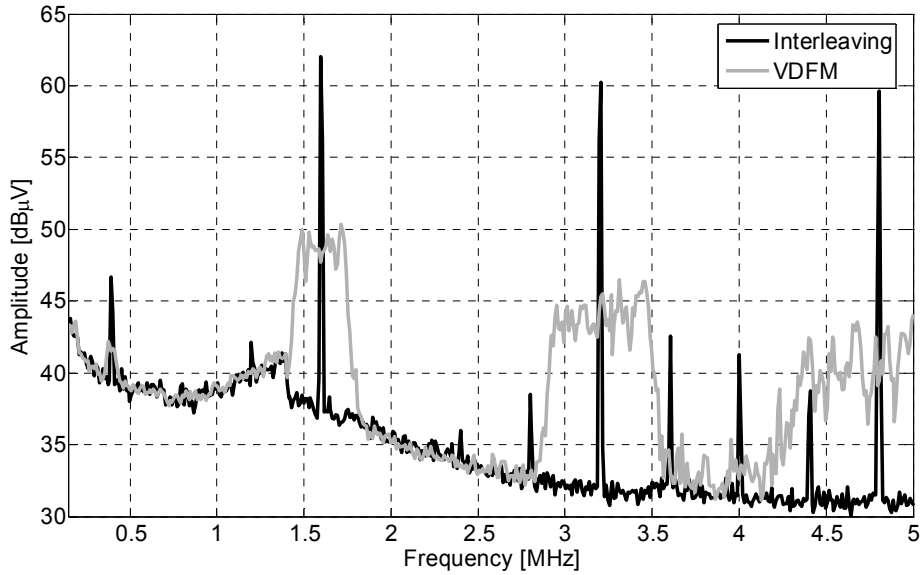


Fig. 9: Experimental EMI spectrum Interleaving vs VDFM.

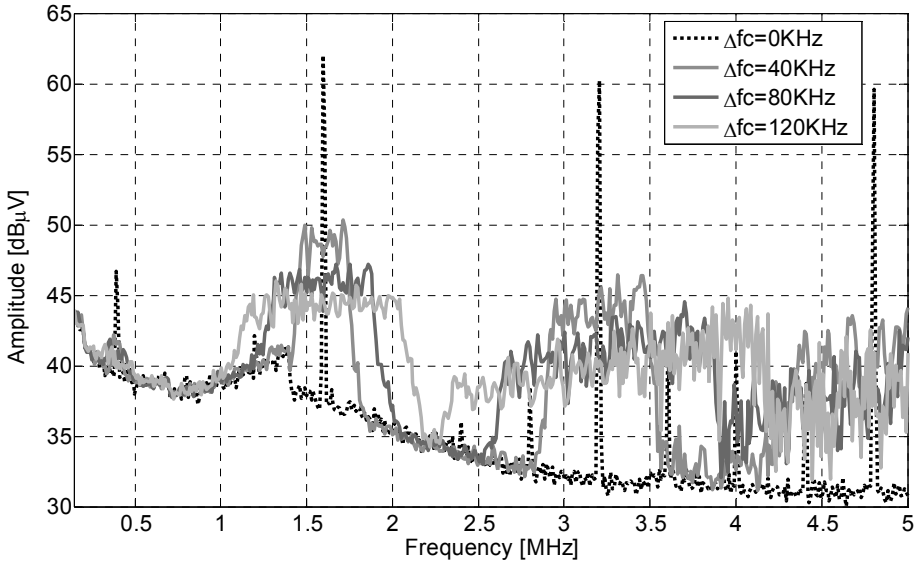


Fig. 10: Experimental EMI spectrum for cases: Δf_c=0 KHz, Δf_c =40 KHz, Δf_c =80 KHz and Δf_c =120 KHz.

Finally, in Fig. 10 the EMI spectrum is depicted for different values of Δf_c when VDFM technique is applied in a four channel parallel buck converter. For Δf_c =0KHz, the EMI spectrum corresponds to apply only the interleaving technique. A strong reduction, on all harmonics not multiple of $4 \cdot f_c$ is observed, approximately, only appears harmonics at frequencies $4 \cdot f_c$, $8 \cdot f_c$, $12 \cdot f_c$. Notice that, for Δf_c >0 the energy of harmonics at frequencies multiple of $4 \cdot f_c$ has been distributed into side-bands whose amplitude decreases when Δf_c increases. It is possible to obtain an amplitude reduction about 17 dB for the fundamental harmonic ($4 \cdot f_c$), when Δf_c =120 KHz.

Conclusion

The main contribution of this work has been to present a new modulation scheme in order to reduce the conducted EMI in modular power supplies with parallel topology. From the point of view of EMI, the VDFM scheme combines the benefits of the interleaving and SFM techniques, such as harmonic cancelation effect and distributed the harmonics energy.

The results show the influence of the maximum frequency deviation in the amplitude reduction of the non-cancelled interference harmonics. With a switching frequency variation about 10 % regarding the central switching frequency (Δf_c =40 KHz), it is possible to obtain an amplitude reduction about 12 dB for fundamental harmonic ($4 \cdot f_c$).

In future works, the impact of the modulation index and the number of converters in the amplitude reduction will be deeply analysed when VDFM is applied.

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