Process and Temperature Compensation for RF Low-Noise Amplifiers and Mixers

Didac Gómez, Milosz Sroka, and José Luis González Jiménez, *Member, IEEE*

***Abstract*—Temperature and process variations have become key issues in the design of integrated circuits using deep submicron technologies. In RF front-end circuitry, many characteristics must be compensated in order to maintain acceptable performance across all process corners and throughout the temperature range. This paper proposes a new technique consisting of a compensation circuit that adapts and generates the appropriate bias voltage for LNAs and mixers so that the variability with temperature and process corners of their main performance metrics (S-parameters, gain, noise figure, etc.) is minimized.**

***Index Terms*—Low-noise amplifier (LNA), mixer, process compensation, RF integrated circuits, temperature compensation.**

I. Introduction

MODERN CMOS manufacturing technologies show large process variations. This makes circuit design an increasingly complicated challenge, as circuit performance has to be maintained in all possible manufacturing and environmental situations [1]. Traditionally, temperature (T) and process variability have been addressed separately during the design process. Temperature variations are compensated using temperature-independent biasing circuits that provide a nearly constant voltage, current or transconductance (g_m) within the specified temperature range [2], [3]. The compensation of process variations in RF and analog integrated circuits (ICs) usually requires trimming [4], calibration and/or self-tuning [5]–[8]. Recently, some techniques have been proposed for generating bias currents with a constant value that is independent of temperature and process [9], [10]. Although these circuits may prove effective in generating a constant voltage or current by themselves, there is no *a priori* guarantee than once connected to the biased circuit this latter will have constant behavior. In this work, we focus on obtaining nearly constant circuit performance using adaptive biasing (not necessarily a constant magnitude) in such a way that the biasing voltage/current variation with temperature and process compensates for variations in some of the biased circuit's parameters of interest. This technique is especially appealing for RF circuitry, in which the variability of transistors and passives has a significant impact on the final circuit behavior. The proposed technique uses conventional constant $-g_m$ voltage references by exploiting complementary temperature and process effects on its components. It is shown how these circuits can be sized to generate a desired voltage versus temperature and process characteristic that, when applied to the biased circuit, counteracts the effects of process and temperature variations.

To demonstrate the proposed technique, it is applied to a RF LNA and a double-balanced mixer with bleeding current sources, but it can be applied as well to other circuits, especially those having a transconductor as the main stage. The LNA has single-ended topology with an inductively degenerated source and a cascode transistor [see Fig. 1(a)]. The mixer uses bleeding current sources. The LNA and mixer are part of an RF front-end for low-power radios operating in the 2.5-GHz ISM band [11] and were designed and implemented with a 2P6M 0.18-μm RF CMOS process. The circuits have been fabricated and tested. Simulation results reasonably match experimental measurements for typical temperature and process conditions, as shown in [12]. The technique presented in this work is validated using the process corners and Monte Carlo simulation models provided by the manufacturer, as it is difficult for academic research institutions to access a representative number of samples for any of the corners of the process.

The rest of the paper is organized as follows. Section II briefly reviews temperature and process effects on MOS transistors and passives found in RFICs. Section III presents the proposed technique, and its application to the LNA and mixer circuits. Section IV presents the simulation results. Finally, Section V contains the conclusions.

II. Temperature and Process Effects on CMOS ICs

A. Temperature Effects

The two most important parameters that determine the temperature behavior of *I–V* characteristics of MOS-FETs are threshold voltage (V_T) and mobility (μ_n). Both decrease with increasing temperature according to the following expressions [1]:

$$V_T(T) = V_T(T_0) - \alpha_{V_T}\Delta T$$
$$\mu_n(T) = \mu_n(T_0)\left(\frac{T}{T_0}\right)^{\alpha_\mu}. \quad (1)$$

Here, $\Delta T = T - T_0$, T_0 is the reference temperature, α_{V_T} lies in the range 0.5–4 mV/ K, and α_μ lies in the range 1.5–2. The

Manuscript received October 09, 2008; revised March 16, 2009 and June 23, 2009. This work was supported in part by the Spanish Ministry of Science and Innovation (MICINN) and EU FEDER funds under projects TEC2008-01856 and AGAUR SGR 1497 funds. The wrok of D. Gómez was supported by AGAUR FI2009 scholarship. This paper was recommended by Associate Editor B. Bakkaloglu.

D. Gómez and J. L. González Jiménez are with the Electronic Engineering Department, Universitat Politècnica de Catalunya, Barcelona 08034, Spain (e-mail: dgomez@eel.upc.edu, jl.gonzalez@upc.edu).

M. Sroka is with the Digital Media SoC Department, Center for Semiconductor Research & Development, Toshiba Corporation, Kawasaki 212-8520, Japan.

Digital Object Identifier 10.1109/TCSI.2009.2031707

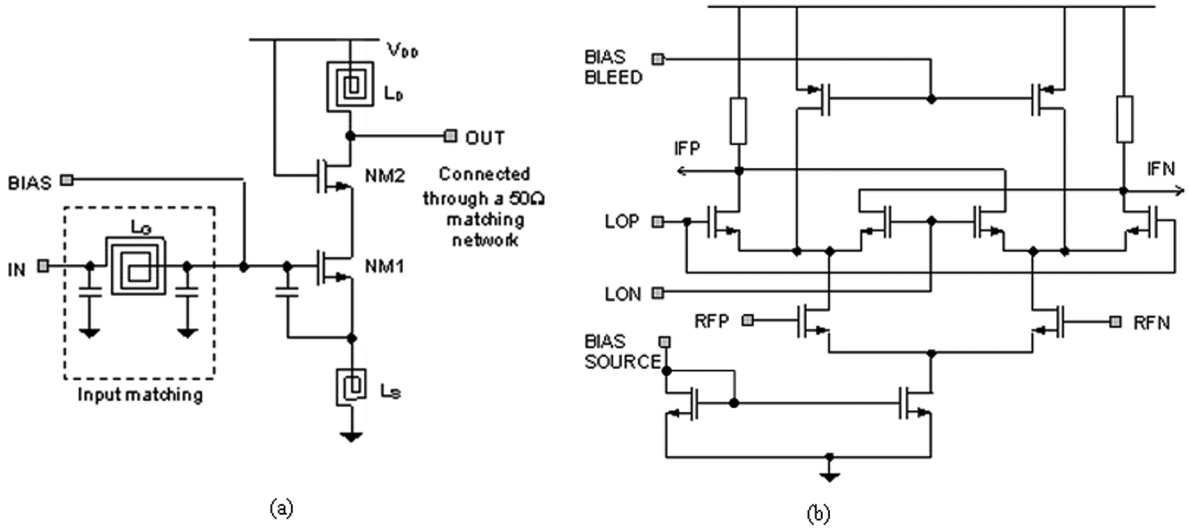

Fig. 1. Simplified LNA and mixer schematics.

TABLE I
TEMPERATURE COEFFICIENT OF THE VARIOUS RESISTORS AVAILABLE IN THE PROCESS

Resistor type	Temperature coefficient
N+ POLY resistor	- 250 ppm/ºC
P+ POLY resistor	-225 ppm/ºC
P- POLY resistor	-1800 ppm/ºC
N+ diffusion resistor	1411 ppm/ºC
P+ diffusion resistor	1405 ppm/ºC

temperature dependences of V_T and μ_n have an opposite effect on the drain current. This has been used to propose temperature-stable biasing points for CMOS circuits [15]. Passive elements are also affected by temperature. In the modern CMOS manufacturing process, both positive and negative temperature coefficient resistors can be found that are made up of n^+ or p^+ diffusion and of doped polysilicon, respectively (see Table I). Different resistor types can be combined to obtain a temperature independent resistor or to tune its resistance versus temperature characteristic as desired.

The temperature and process compensation circuit used in this work is based on a classical constant $-g_m$ circuit [13], [14] containing a self-biased quad of transistors and a resistor [see Fig. 2(a)]. For this circuit it can be shown that

$$g_{mNM1} = \frac{2\left(1 - m^{-0.5}\right)}{R} \tag{2}$$

where m is the ratio between NM_1 and NM2. If R is made constant with temperature, a stable g_m value is provided for NM_1, NM_2, and for the slave transistor in the biased circuit.

B. Process Effects

Inter-die variations produce a dispersion of the values of manufactured transistors and passives in comparison with the typical expected value. However, all the devices in the same chip suffer the same variations. This is the type of process variation that is compensated by the biasing circuit proposed in this work. Manufacturing variability that affects devices on the same chip causes intra-die variations (mismatching), which is usually solved by layout techniques and proper sizing of paired devices.

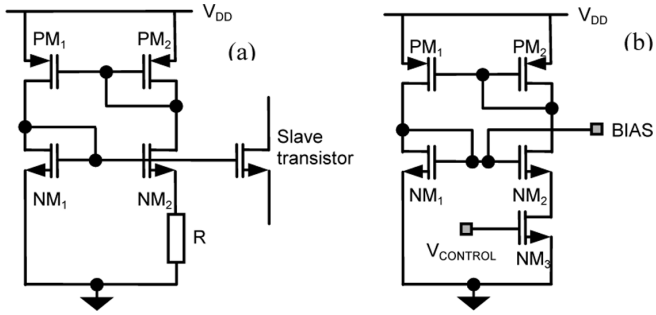

Fig. 2. Schematics of constant $-gm$ bias generators.

The impact of mismatching on the proposed technique is addressed at the end of Section III and in the results for the differential mixer shown in Section IV.

Inter-die variations are modeled as worst-case process corners and through the use of statistical device models that allow Monte Carlo simulations to be performed on the whole circuit. In the technology used in our work, passive elements suffer from larger process variations than active devices. Therefore, it is a good idea to reduce the variability of the biasing characteristic of the circuit of Fig. 2(a) by replacing the resistor with an NMOS transistor biased in the ohmic region using an identical circuit as shown in Fig. 4.

In CMOS manufacturing processes, four corners are usually defined in addition to the typical case (TT), i.e., SS, SF, FS, and FF. They correspond to all the combinations between a fast or slow PMOS and NMOS transistor model. The slow corner implies a thicker gate oxide (C_{ox}), a reduced mobility (μ) and a larger threshold voltage (V_T), which results in a reduced drain current density for the same gate voltage. The fast corner is just the complementary one. Passive component variation is traditionally modeled using just two corners in addition to the typical one, namely MAX and MIN, which refer to the maximum and minimum values that the passive component (resistor, inductor or capacitor) may achieve due to inter-die process variations. The two corners of passive elements are associated with the transistor corner to obtain useful worst cases. For example,

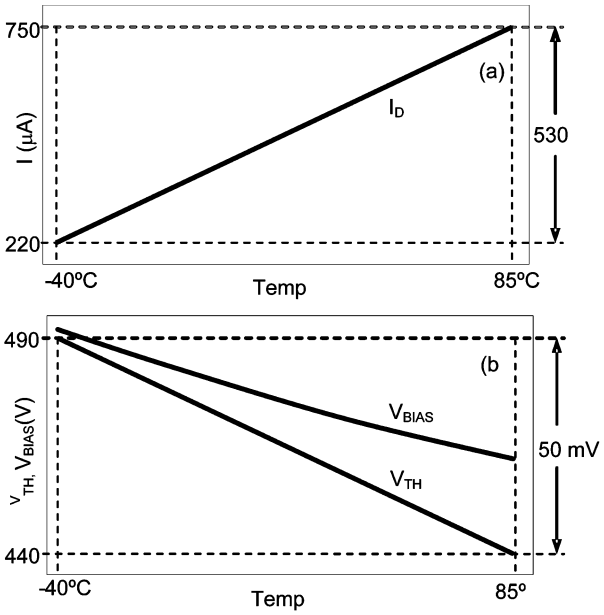

Fig. 3. DCcurent of : (a) LNA and (b) threshold and bias voltages variation with temperature for the biased and the biasing circuits, repectively.

the MIN corner of resistors is considered when the FF corner is used, since smaller resistors produce larger currents. Similarly, the MAX corner model for capacitors or inductors is considered together with the SS corner, since it produces slower operation and smaller currents.

In [9] it is shown that the combined impact of variations in V_T and $K' = \mu C_{\rm ox}$ on the drain current is

$$\frac{\Delta I}{I} \approx \frac{\Delta K'}{K'} + \frac{2\Delta V_T}{(V_T + V_{DS\_SAT})} \tag{3}$$

where V_{DS_SAT} is the saturation voltage. Since $\Delta K'$ and ΔV_T have an opposite sign in fast and slow corners (for both PMOS and NMOS transistors) [9], it is possible to get zero current variation by properly adjusting the constant magnitudes of the two summands of (3). Indeed, it is also possible to adjust them to obtain a variation in the drain current that counteracts the variability due to the process of the biased circuit. This is the approach used in this work.

III. Process and Temperature Compensation

The initial values of bias voltages are provided by the RF designers in the typical temperature and process corner. The goal of the proposed technique is to provide an adaptive bias that preserves the same performance at other process corners and temperatures. It is implemented in a two-step process. First, a circuit based on Fig. 2(b) is sized in order to achieve a bias voltage versus temperature characteristic that once applied to the biased circuit produces a temperature independent behavior for typical process corner. Next, the bias generator circuit is resized in order to tune the process variation effects on the bias voltage in the direction that counteracts the impact of process variations on the biased circuit. A complete example of this process is presented for the LNA circuit. The same technique is applied to the mixer, but only the final results will be shown here, due to the limited space available.

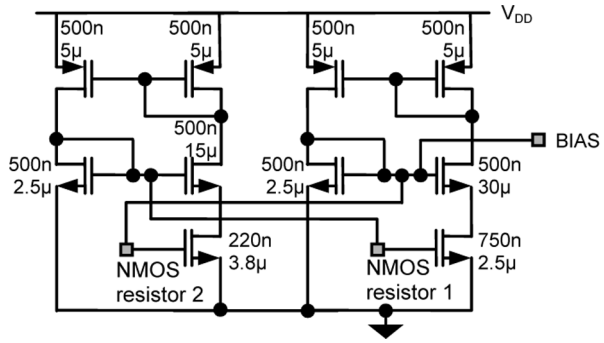

Fig. 4. Biasing circuit for the LNA (sizes correspond to the final version that compensates both temperature and process variations).

TABLE II
LNA Characteristics at 2.34 GHz for $-40°\mathrm{C} < \mathrm{T} < 80°\mathrm{C}$

LNA parameter	Value at T_{TYP}=27ºC	Max. variation with temperature, constant V_{BIASs}	Max. variation with temperature using bias generator
S21	4.52 dB	4.60 dB	0.14 dB
S11	-15.31 dB	1.23 dB	0.61 dB
S22	-23.32 dB	12.3 dB	7.51 dB
S12	-39.13 dB	0.06 dB	0.33 dB
NF	3.50 dB	0.56 dB	0.93 dB
Gain	4.49 dB	4.85 dB	0.14 dB

A. Compensation of the LNA Thermal Variability

Fig. 3(a) shows the LNA DC current versus . temperature when a constant bias voltage ($V_{\rm BIAS}$) is used. With this constant biasing, the voltage gain varies more than 4 dB inside the temperature range (see Table II). Then, the circuit of Fig. 4 is sized to generate a $V_{\rm BIAS}(T)$ characteristic as shown in Fig. 3(b). The optimization process that is run on the bias + LNA circuit has the goal of minimizing (within a margin of 1dB around the typical value) the variability of the LNA gain and other relevant parameters along the temperature range by adjusting the relative size of the NMOS resistor and the NM_1 NM_2 pairs. As a consequence, the LNA voltage gain variability with temperature is reduced to less than 0.2 dB and other parameters improve as well, as shown in Table II.

B. Compensation of the LNA Process Variability

The process of sizing the biasing circuit to simultaneously compensate process and temperature variations is summarized in the flowchart of Fig. 5. The process starts with the bias circuit (BIAS) obtained in a previous step that stabilizes in temperature the behavior of the BIAS + DUT circuits. The DUT is the LNA amplifier in this case. Next, the DUT alone is simulated at various corners. At each corner the VBIAS is swept till the selected parameter matches the same value than at TT. For the LNA this requires increasing the bias voltage by 55 mV in the SS corner and decreasing it by 60 mV in the FF corner respect the value at TT. In this example the optimization goal parameter is the gain, but any other parameter or combination of parameter in the form of a figure-of-merit could be used.

Next, the BIAS circuit alone is sized inside an optimization loop to generate the $V_{\rm BIAS}$ at each corner that was obtained in

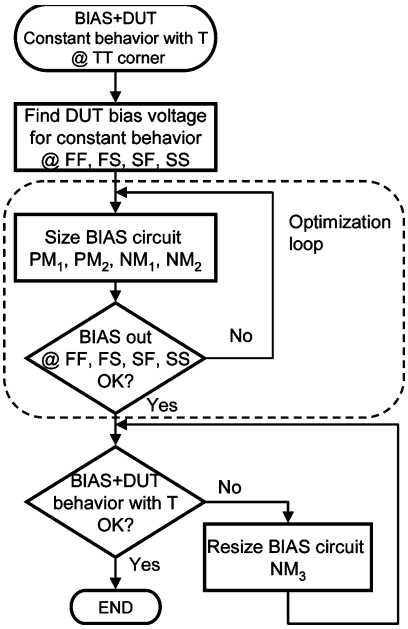

Fig. 5. Bias circuit sizing for process variability compensation workflow.

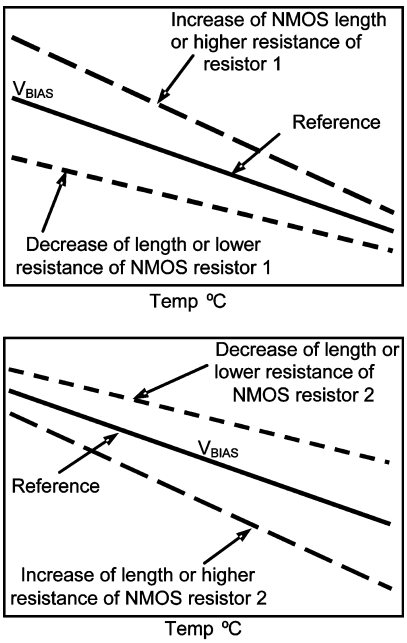

Fig. 6. Variability of the slope of biasing characteristic for the LNA with temperature and varying length of NMOS resistors (NM3).

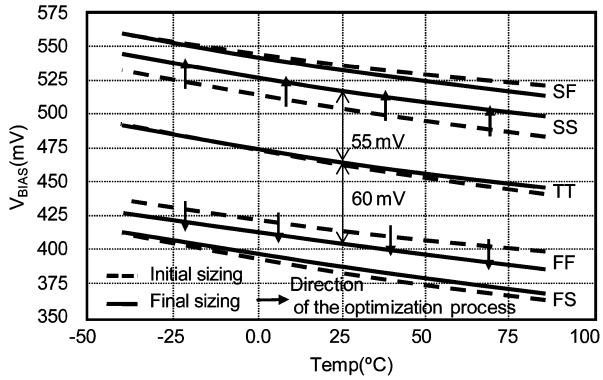

Fig. 7. Biasing voltage characteristics for the LNA with temperature and the four process corners (TT, FF, FS, SS, and SF).

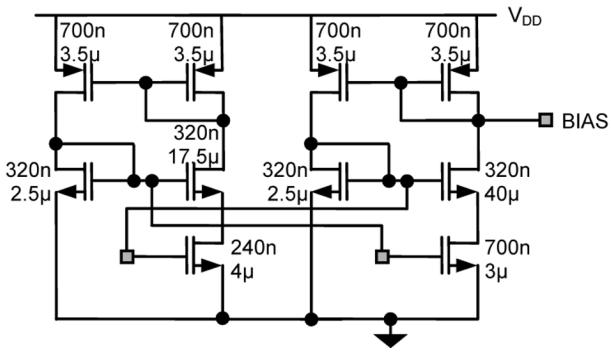

Fig. 8. Double-stage biasing and compensation circuit for the Mixer.

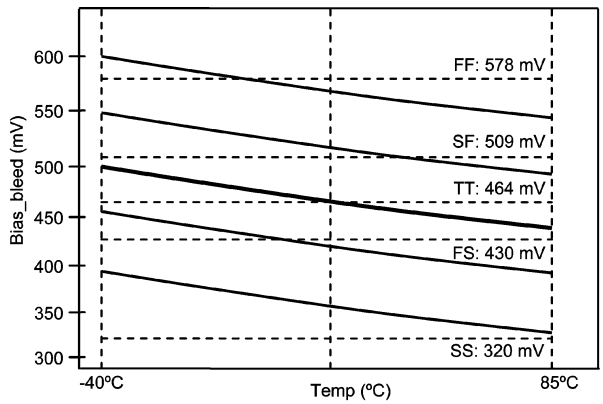

Fig. 9. Bias voltage of Mixer bleeding transistors from the circuit of Fig. 8.

the previous step. The optimizer tool available in the commercial simulator was used. Some constraints are added to preserve the temperature compensation by maintaining the original ratio between the quad of transistors (PM_1, PM_2, NM_1 and NM_2) and the NMOS resistors (NM_3) in both instances of the basic bias cell of Fig. 4. The resulting BIAS + DUT circuit is simulated to check temperature behavior, which can be improved if required by resizing the NMOS resistors $(NM)_3$ using a sweep analysis. Actually, there is a trade-off between preserving the temperature variation slope in all corners and maintaining the offsets of the bias voltage achieved in all corners.

The dependence of $V_{\rm BIAS}(T)$ curve on the sizing of the bias circuit is illustrated in Fig. 6. The slope and separation from the reference $V_{\rm BIAS}(T)$ curve obtained in step 1 of the sizing algorithm are adjusted during the optimization loop for the different corners to compensate process variations and preserve the temperature compensation of the original circuit.

Fig. 7 shows the behavior of the circuit of Fig. 4 with temperature and process. Such behavior has been optimized to counteract the impact of process and temperature on the LNA of Fig. 1(a). The dashed lines correspond to an intermediate value

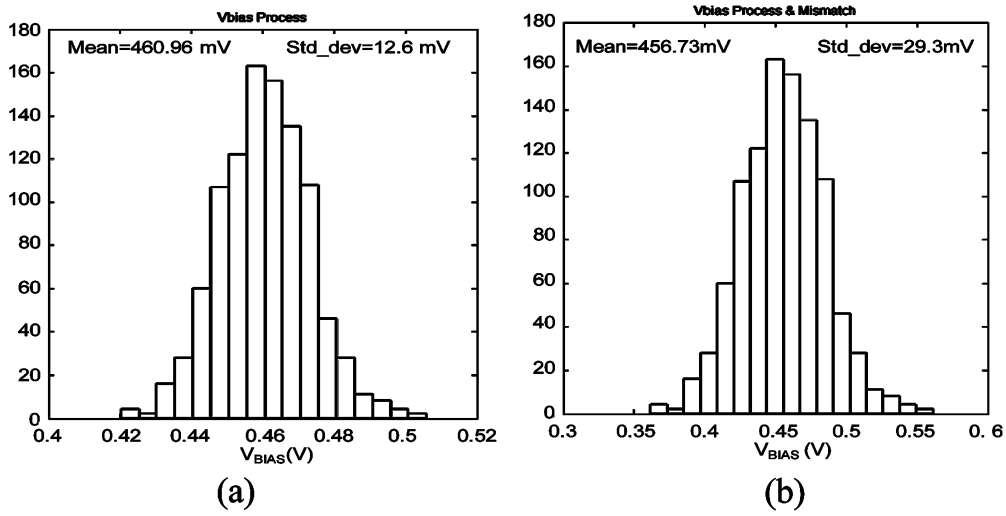

Fig. 10. (a) Process only and (b) Process + mismatch Monte Carlo simulation of the bias generator circuit for the mixer.

of the bias voltage that is found at the beginning of the optimization loop, and the direction of the optimization process is illustrated by the arrows.

C. Process and Temperature Compensation for the Mixer

The double-balanced mixer circuit of Fig. 1(b) requires several different biasing voltages and a constant current source. In addition to the bleeding PMOS transistors, the RF and LO ports also require DC bias voltages [not shown in Fig. 1(b)]. Indeed, due to the strong influence of the bleeding current on the mixer DC operating point and voltage gain an adaptive bias voltage that sets such current may be used for compensating the effects of temperature and process variations on the mixer devices. The other bias voltages are obtained from the power supply using voltage dividers made by combining two types of resistor with opposite temperature coefficients: diffusion resistors and poly resistors (see Table I). The same technique is used for the resistive loads of the mixer that set the voltage gain. Fig. 8 shows the biasing circuit used to generate the adaptive bias voltage that sets the bleeding current. It has the same topology used in the circuit of Fig. 4. In this case, the bias voltage is generated at the gate of the PM_1, PM_2 transistors, as the bleeding current sources of the mixer are implemented with PMOS transistors. The behavior of this bias voltage with process corners must be just the opposite of that in the case of the LNA. This is easily achieved with the proposed bias generator circuit sizing technique, by balancing the two summands of (3) in the opposite direction to in the LNA. Final transistor sizes are shown in Fig. 8, and the achieved behavior is shown in Fig. 9, where the dashed lines show the optimal bias voltage values for each corner found in step 1 of the sizing algorithm shown in Fig. 5, and the solid line show the final behavior of the biasing circuit with temperature and process corners.

D. Mismatching Effects

The operation of the bias circuit is affected by its symmetry. Intra-die variations affect this symmetry by introducing mismatching between the pair of transistors that ideally must be equal or have proportional sizes. However, since mismatch is inversely proportional to the device area, its impact can be reduced by increasing the device sizes.

Intra-die variations are modeled by adding random variables to the parameters of a primary device model, particularly those that determine the threshold voltage and the mobility. In this way, every transistor in the circuit is affected by a different random variation using the statistical simulation analysis. Fig. 10 shows the result of 1,000 runs of the Monte Carlo analysis of the bias generator circuit shown in Fig. 8 at $T = 27°\mathrm{C}$. The left graph corresponds to a simulation set-up in which only process variations (inter-die) are taken into account. The right graph shows the same type of simulation when both inter-die and intra-die variations are considered. The random intra-die process variations increase the standard deviation of the bias voltage value from ± 12.6 mV to ± 29.3 mV for an average value of 460 mV. This means that mismatching is responsible for a random variation of the bias voltage with a $\sigma = \pm 16.7$ mV. As shown in the next section, this variation does not significantly affect the effectiveness of the inter-die process compensation technique.

IV. Results

The proposed adaptive biasing technique is checked using SPICE simulations of the extracted netlist of the LNA and mixer circuits, including all the parasitics.

A. LNA Circuit Results

Process variation simulations are performed with corner analysis and Monte Carlo analysis. S parameter, noise figure (*NF*) and voltage gain (G_v) results at 2.45 GHz and $T = 27°\mathrm{C}$ for corner process variations are shown in Table III, and their characteristics are depicted in Fig. 11. The LNA simulation results when using a constant V_{BIAS} voltage are shown in the top section of the figure. Since the circuit has only NMOS transistors, only three corners are shown (NMOS fast, NMOS slow, and NMOS typical). Corner models for passives are associated to fast/slow transistor corners as described in Section II-B. The bottom section of the figure shows the results once the process and temperature compensation V_{BIAS} generator circuit is used.

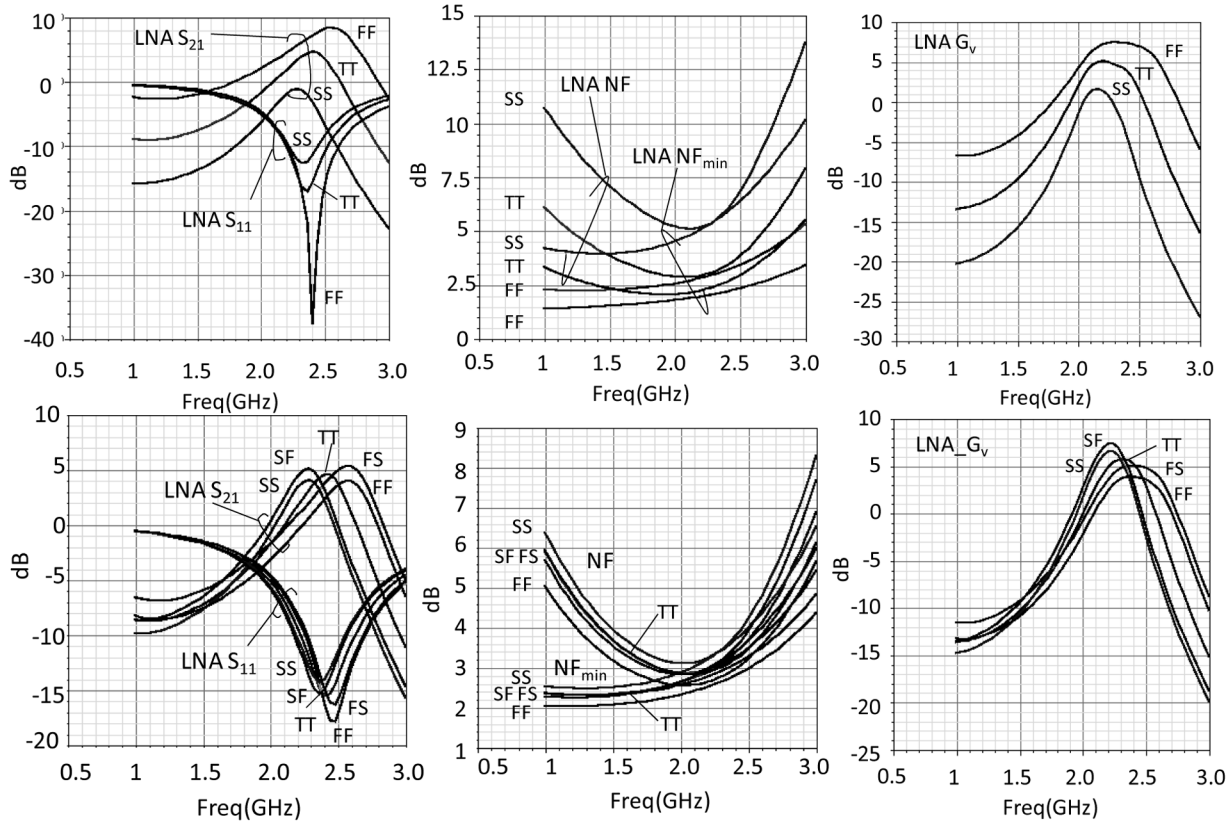

Fig. 11. LNA S-parameters, NF and NFmin, and voltage gain for process corners process (top) without (and (bottom) with the compensation circuit.

TABLE III
LNA CHARACTERISTICS SPREAD AT 2.45 GHZ, $T = 27$ °C FOR PROCESS VARIATIONS (CONSIDERING ALL CORNERS). IN BRACKETS: VALUES WHEN INPUT RESONANT FREQUENCY IS CALIBRATED

LNA Para-meter	Value at TT corner	Max. variation with process, constant bias.	Max. variation with process using bias generator
S21	4.52 dB	12.10 dB	3.65 (1.31) dB
S11	-15.31 dB	15.21 dB	4.72 (1.37) dB
S22	-23.32 dB	19.18 dB	19.46 (1.08) dB
S12	-39.13 dB	7.05 dB	5.53 (3.60) dB
NF	3.50 dB	3.58 dB	0.88 (0.64) dB
Gain	4.49 dB	12.77 dB	3.79 (1.60) dB

TABLE IV
LNA MONTE CARLO SIMULATION RESULTS (1000 RUNS) FOR INTER-DIE PROCESS VARIATIONS AT $T = 27$ °C (ALL UNITS ARE IN DB)

Para-meter:	Const. bias (no compens.)			Bias compensation circuit		
	Mean	σ	3σ	Mean	σ	3σ
S21	4.83	1.216	3.648	4.76	0.642	1.926
S11	-16.04	1.384	4.152	-15.79	0.724	2.172
S22	-18.70	7.40	22.20	-18.73	7.46	22.38
S12	-39.13	0.833	2.499	-39.16	0.795	2.385
NF	3.42	0.281	0.843	3.419	0.131	0.393
NF_{min}	3.26	0.319	0.957	3.268	0.148	0.444
Gain	4.80	1.178	3.535	4.73	0.671	2.014

TABLE V
MAXIMUM VARIATION IN LNA GAIN IN ALL THE PROCESS CORNERS FOR TEMPERATURE VARIATIONS FROM -40 °C TO 80 °C

	TT	FF	SS	SS	SF
ΔGain	0.16 dB	1.5 dB	1.9 dB	0.83 dB	0.82 dB

In this case, there are five corners since the biasing circuit has PMOS transistor as well. The results of Monte Carlo analysis using 1,000 runs are presented in Table IV, showing a clear improvement in the dispersion of the various performance parameters when the compensation circuit is used. Furthermore, the results in Table V show that the temperature compensation is maintained across all process corners.

The variability of inductors in the LNA, which is much smaller than that of other passive components, mainly affects the input resonant frequency at which matching is achieved (which is also affected, to a lesser extent, by the variability of on-chip and passive capacitors, as seen in Fig. 11). However, this variability cannot be compensated for with adaptive biasing: a self-calibration technique such as [16] is required. The last column of Table III includes the improvement that would be achieved if such a calibration technique for input matching was used along with the compensation circuit proposed in this work.

B. Mixer Circuit Results

Process variations effects in the Mixer circuit are catastrophic, especially in the SS corner, as can be observed in the left graph of Fig. 12. The compensation circuit effectively provides an adaptive bias voltage for the bleeding transistors that, in combination with the other biasing techniques described in Section III-C, reduces process variability to acceptable levels, as shown in the right graph of Fig. 12. The variability of the

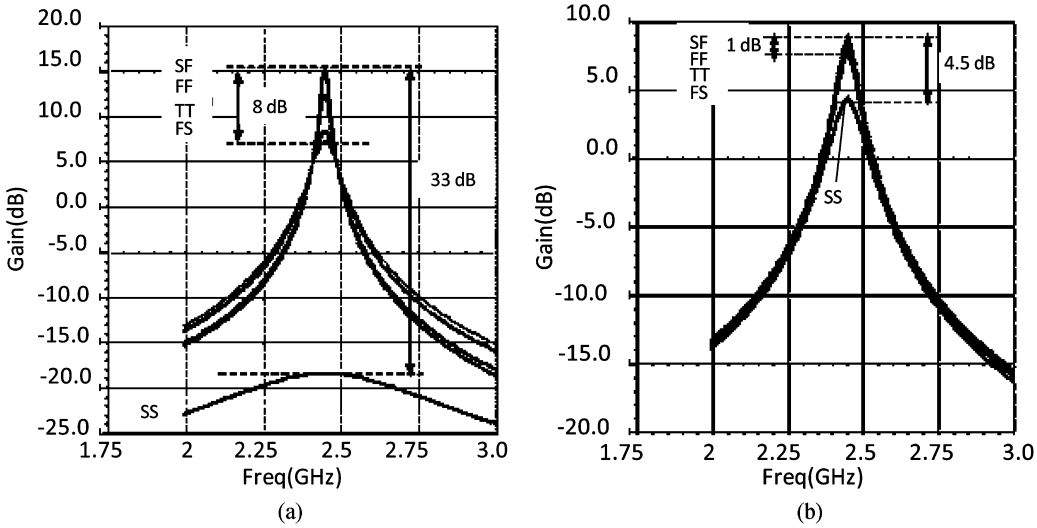

Fig. 12. Mixer voltage gain for process corners process without (left) and with the compensation circuit (right).

TABLE VI
MONTE CARLO SIMULATION RESULTS (1000 RUNS) OF MIXER VOLTAGE GAIN AT $T = 27$ °C.

Constant bias Inter-die variations		Proposed bias circ. Inter-die variations		Proposed bias circ. Inter-die + Intra-die	
Mean	σ	Mean	σ	Mean	σ
9.8 dB	2.7 dB	10.5 dB	1.9 dB	10.4 dB	2.14 dB

mixer gain is reduced from 8 dB to less than 1 dB for all the corners except SS.

The impact of intra-die variations on the compensation technique is analyzed by running 1000 Monte Carlo simulations at $T = 27$ °C. In a first experiment, the mixer circuit is simulated with constant biasing voltages and only inter-die process variations are considered. In a second experiment, the bias circuit + mixer circuit are simulated and only inter-die process variations are considered. Next, both inter-die and intra-die (mismatching) process variations are considered together. The results are shown in Table VI. The effectiveness of the proposed inter-die process compensation technique is verified by comparing the standard deviation of the mixer voltage gain (G_v) obtained in both experiments. The G_v of the mixer with constant biasing voltages shows an inter-die variation with a $\sigma = 2.7$ dB, whereas the mixer using the bias voltage generated by the circuit of Fig. 8 shows an inter-die variation with a $\sigma = 1.9$ dB. When inter-die and intra-die variations are both considered, the BIAS + mixer G_v variations show a $\sigma = 2.14$ dB. Therefore, mismatching does not significantly affect the operation of the proposed technique.

The variations of the supply voltage affect the compensation circuit and the LNA and mixer circuits in a similar way. Negligible effects are observed if these variations are kept below ± 50 mV (for a supply voltage of 1.2 V), which usually require an appropriate supply voltage regulation.

V. CONCLUSIONS

This paper presents a simple biasing circuit structure and its sizing technique that allows compensation of both the effects of temperature and process variation. The proposed technique is applied to an RF LNA and mixer circuits, but it can be extended to other circuits. It is particularly suited to generate the gate bias voltage of the gain transistors in RF building blocks or any other circuit (such as active filters, output drivers, etc.) using a transconductor as the main stage. The structure of the circuit is derived from classic temperature compensation circuits, which, with proper redesign, also become compensation circuits for inter-die process variations.

The results shown in this paper demonstrate that performance variability with temperature was accurately compensated. Concerning inter-die process variations, the application of the proposed biasing technique provides a significant reduction of variability. For the LNA, the S_{11}, S_{22} and gain variation with process corners is reduced by a factor larger than 3 and NF variation is reduced by a factor larger than 4. Monte Carlo simulations indicate a reduction in the sigma of the distribution of LNA parameters by a factor of two. The application of the same technique to the mixer by using the bleeding bias voltage (in addition to other, simpler techniques) provides a reduction in the variability of the mixer gain from 8 dB to less than 1 dB for all the corners except SS. For that corner, the compensation circuit brings the mixer gain from a catastrophic fault to a value just 4.5 dB below the typical corner. Additionally, it has been shown that intra-die variations (mismatching) do not significantly affect the effectiveness of the proposed inter-die process and temperature compensation technique.

REFERENCES

[1] P. Lall, M. G. Pecht, and E. B. Hakim, *Influence of Temperature on Microelectronics and System Reliability*. Boca Raton, FL: CRC Press LLC, 1997.

[2] Y. L. Theng, Y. S. Hwa, L. B. Poh, T. H. Kwang, S. Tachi, K. L. Soo, T. Murakami, S. H. Jin, L. T. Choon, T. C. Lin, W. K. Wing, X. J. Qi, L. M. Chiao, L. H. Shio, X. Wei, and M. Itoh, "Design techniques to combat process, temperature and supply variations in Bluetooth RFIC," in *IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 8–10, 2003, pp. 551–554.

[3] J. Chen and B. Shi, "Design of an on-chip temperature-compensated constant transconductance reference," *Analog Integr. Circuits and Signal Process.*, vol. 37, no. 3, pp. 215–222, Dec. 2003.

[4] D. Marche, Y. Savaria, and Y. Gagnon, "Laser fine-tuneable deep-sub-micrometer CMOS 14-bit DAC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 8, pp. 2157–2165, Sep. 2008.
[5] F. Cheng and R. J. Weber, "A novel process-variation insensitive network for on-chip impedance matching," in *Int. Symp. on Commun. and Inf. Technol.*, Oct. 2004, vol. 1, pp. 43–46.
[6] T. Das, A. Gopalan, C. Washburn, and P. R. Mukund, "Self-calibration of input-match in RF front-end circuitry," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 52, no. 12, pp. 821–825, Dec. 2005.
[7] P. Vänänen, N. Mikkola, and P. Heliö, "VCO design with on-chip calibration system," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 10, pp. 2157–2166, Oct. 2006.
[8] F. Bahman, T. Serrano-Gotarredona, and E. Sánchez-Sinencio, "An accurate automatic quality factor tuning scheme for second-order LC filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 4, pp. 745–756, Apr. 2007.
[9] S. Sengupta, K. Saurabh, and P. E. Allen, in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2004, pp. 23–26.
[10] A. M. Pappu, X. Zhang, A. V. Harrison, and A. B. Apsel, "Process-invariant current source design: Methodology and examples," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2293–2302, Oct. 2007.
[11] *Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (WPANs)*, IEEE Std 802.15.4, IEEE, 2006.
[12] L. Moreno, D. Gómez, J. L. González, D. Mateo, X. Aragonès, R. Berenguer, and H. Solar, "A low-power RF front-end for 2.5 GHz receivers," in *IEEE Int. Symp. Circuits Syst.*, May 2008, pp. 976–979.
[13] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Second ed. Cambridge, U.K.: Cambridge Univ. Press, 2003.
[14] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*. New York: Wiley, 1997.
[15] I. M. Filanosvsky, in *IEEE Int. Symp. on Circuits Syst.*, May 2000, pp. V-197–V-200.
[16] T. Das, A. Gopalan, C. Washburn, and P. R. Mukund, "Self-Calibration of input-match in RF front-end circuitry," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 52, no. 12, pp. 821–825, Dec. 2005.

Didac Gómez received the M.S. degree in telecommunications engineering from the Universitat Politècnica de Catalunya (UPC), Barcelona, Spain, in 2007. He is currently working toward the Ph.D. degree at the UPC's Department of Electronic Engineering.

He is the author of three conference papers. His research interests include UWB impulse-radio circuits, robust RF integrated circuit design and process variability in CMOS technologies.

Milosz Sroka received the M.S. degree in electrical engineering from the Institut National des Sciences Appliquées de Lyon (INSA), France, in 2007 and the MS degree in telecommunication engineering from the Universitat Politècnica de Catalunya (UPC), Barcelona, Spain, in 2007.

In October 2007 he joined Toshiba Corporation, Kawasaki, Japan, where he works on the development of Digital Media SoC in the Center for Semiconductor Research and Development. From September 2004 to February 2005 he participated in an internship in system modeling and simulation in the Korea Advanced Institute of Science and Technology (KAIST) in Daejeon. During the summer of 2005 he worked in the R&D Dept. of Ficosa International in Barcelona (Spain), where he developed embedded systems for automotive applications. From July 2006 to December 2006 he participated in an internship in video processors in the Multimedia Laboratory in Toshiba R&D Center in Kawasaki, Japan. His research interests include RF integrated circuits, VLSI design and video processors.

José Luis González Jiménez (M'99) received the Diploma in telecommunication engineering from the Ramon Llull University (URL), Barcelona, Spain, in 1992, and both the M.S. degree in telecommunications engineering and Ph.D. degree (with honors) in electronic engineering from the Universitat Politècnica de Catalunya (UPC), Barcelona, in 1994 and 1998, respectively.

He is currently a full-time Associate Professor at the Department of Electronic Engineering of the UPC's School of Telecommunications Engineering of Barcelona. He was granted a Fulbright Fellowship from January to July 1999 to work as a guest researcher at the University of Arizona, Tucson (USA), where he collaborated with Motorola in the design of high-speed D/A converters. From September 2007 to August 2008 he was a visiting researcher at STMicroelectronics/CEA-Leti joint Advanced Research Laboratory in Minatec, Grenoble (France), working on the design of mmW oscillators and substrate noise coupling in mmW CMOS ICs. He is the author of 2 books, a book chapter, 10 international journal papers and more than 40 conference papers. He holds seven patents. His research interests include VLSI design, mixed-signal/RF integrated circuits and noise problems in SoC integration.