Improved current-source sizing for high-speed high-accuracy current steering D/A converters

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ABSTRACT

This paper describes a design methodology for the basic current source cell circuit of high-speed high-accuracy current steering D/A converters taking into account mismatching in all the transistors of the cell. Previous works consider arbitrary safety margins in the sizing process. The presented approach allows a more accurate selection of the optimal design point. The design methodology is illustrated for a particular design of a 0.35μm CMOS 12-bit 400 MHz current-steering segmented D/A converter.

1. INTRODUCTION

High-accuracy (≥ 12 bits) and high-speed (from tens up to several hundreds of MHz) D/A converters (DAC) are required by modern telecommunication systems [1]. A CMOS current-steering DAC is the usual choice for this type of applications since this topology best suits those requirements. In this architecture the b significant bits are used to switch a binary weighted array of b current sources and the m most significant bits, from a total of $n = m + b$ bits, are thermometer decoded and used to switch an array of 2^m-1 unary current sources. The addition of currents generated by the two arrays represents the analog output value. The performance of the DAC is specified through static parameters (Integral Non Linearity or INL, Differential Non Linearity or DNL, and parametric yield) and dynamic parameters (glitch energy, settling time and SFDR) [2]. Static performance is mainly dominated by systematic and random errors. Systematic errors caused by process, temperature and electrical slow variation gradients are almost cancelled by proper layout techniques [3]. Random errors are determined solely by mismatch due to fast variation gradients. The design of current-steering DAC starts with an architectural selection to find the optimum segmentation ratio (m over n) that minimizes the overall digital and analog area [4,5,6]. The INL is independent of the segmentation ratio and depends only on mismatching if the output impedance is made large enough [7]. The DNL specification depends on the segmentation ratio but it is always satisfied provided that the INL is below 0.5 LSB for reasonable segmentation ratios. The glitch energy is determined by the number of binary bits b, being the optimum architecture in this sense a totally unary DAC. However this is unfeasible in practice due to the large area and delay that the thermometer decoder would exhibit. The minimization of the glitch energy is then bypassed to the circuit level design of the switch & latch array and current source cell. After the architecture level optimization, the LSB current source cell must be optimally sized at circuit level taking into account the INL specification and trying to minimize settling time and to maximize output impedance. The other current sources are scaled from it accordingly to its weight. In this paper an optimum sizing strategy for the current source cell is presented that complements previous approaches by taking into account matching errors not only in the current source transistor but in the rest of transistors of the cell as well.

2. SIZING STRATEGY

The two usual topologies for the basic current source are shown in Fig. 1. Topology (a) consists of a current source (CS) transistor and two complementary switch (SW) transistors. Topology (b) includes an additional cascode transistor (CAS) that increases the output impedance to fulfil the SFDR specification for resolutions ≥ 12 bits [8]. This later topology reduces the clock feedthrough from the switches to the drain of the CS thus reducing the glitch energy. A driver circuit with a reduced swing placed between the latch and the switch reduces the clock feedthrough to the output node as well. The latch circuit complementary output levels and crossing point are designed to minimize glitches [9]. Table 1 shows the circuit level parameters (size and gate voltage) to be found by means of the optimization process for the more general topology (b) in Fig. 1. The aspect ratio W/L fixes the overdrive voltage (V_{gs}-V_T), and viceversa, for each transistor once the LSB current I is fixed. The same aspect ratio can be obtained for different areas $W \times L$, except for the CS transistor, because the usual INL-mismatch specification eliminates one degree of freedom.

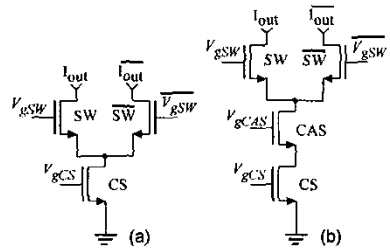

Figure 1. Current source cell topologies

Current source (CS)	Switch (SW)	Cascode (CAS)
W_{CS}, L_{CS}, V_{gCS}	W_{SW}, L_{SW}, V_{gSW}	$W_{CAS}, L_{CAS}, V_{gCAS}$

Table 1. Current source cell transistor parameters.

The relative standard deviation of a unit current source $\sigma(I)/I$ has to be small enough to fulfil the INL < 0.5 LSB specification given a parametric *yield* [10]:

$$\frac{\sigma(I)}{I} \le \frac{1}{2C\sqrt{2^{n-1}}}, \text{ with } C = \mathbf{inv\_norm}\left(0.5 + \frac{yield}{2}\right) \qquad (1)$$

where **inv_norm** is the inverse cumulative normal distribution. The CS transistor size is found as:

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$$W_{CS}^2 = \frac{I}{K'\left(\frac{\sigma(I)}{I}\right)^2}\left[\frac{A_\beta^2}{(V_{gs}-V_T)_{CS}^2}+\frac{4A_{VT}^2}{(V_{gs}-V_T)_{CS}^4}\right]$$
$$L_{CS}^2 = \frac{K'}{4I\left(\frac{\sigma(I)}{I}\right)^2}\left[A_\beta^2(V_{gs}-V_T)_{CS}^2+4A_{VT}^2\right] \quad (2)$$

where K' is the MOS transistor gain factor, V_T the threshold voltage, and A_β and A_{VT} are their technology matching parameters, respectively.

2.1 Basic current cell (CS+SW) sizing

The overdrive voltage $(V_{gs}-V_T)_{CS}$ in (2) has to be maximized to minimize the CS area, but has to be small enough to allow the SW transistor to operate in saturation in any situation to obtain the highest possible output impedance. For the current source in Fig. 2(a), the condition for the gate voltages of the transistors that guarantees that both operate in saturation is:

$$\underbrace{V_{OD}^{CS}+V_{OD}^{SW}+V_T^{SW}}_{V_{gSW}^{min}} < V_{gSW} < \underbrace{V_{DD}-\Delta V_o^{max}+V_T^{SW}}_{V_{gSW}^{max}} \quad (3)$$

where V_{OD} are the overdrive voltages for the different transistors, V_{DD} is the power supply voltage and ΔV_o^{max} is the maximum output voltage swing. A solution exists in eq. (3) if and only if the difference between the upper and lower bounds is positive. This determines an upper bound for the addition of the overdrive voltages in the worst case when $I_{out}R_L = V_o = V_{DD}-\Delta V_o^{max}$:

$$V_{OD}^{CS}+V_{OD}^{SW} \le V_{DD}-\Delta V_o^{max} \quad (4)$$

from which the minimum area will be found when the left part is equal to the right part. The two last expressions relate the SW and the CS transistors bias voltages in such a way that if one of them is fixed, the other one is derived using eq. (4). The CS transistor is the larger of the two, so its overdrive voltage is always fixed to the highest possible value fulfilling eq. (4). By doing this, the overdrive voltage of the SW transistors is found just at the limit between the triode and the saturation regions. In the sizing procedure previously reported [9,11] only the mismatch error of the current source transistor is considered and an arbitrary safety margin is introduced in eq. (4) to prevent the transistors to enter triode region due to process variations: $V_{OD}^{CS}+V_{OD}^{SW} = V_{DD}-\Delta V_o^{max}-\Delta V_{safe}$.

The CS gate voltage is intrinsically determined by its overdrive voltage. It can be easily shown that the maximum of the DC output impedance when channel length modulation is taken into account is found when the SW gate voltage is:

$$V_{gSW} = V_T^{SW}+\frac{1}{2}\left(V_{DD}-\Delta V_o^{max}+V_{OD}^{CS}+V_{OD}^{SW}\right) = \frac{V_{gSW}^{max}+V_{gSW}^{min}}{2} \quad (5)$$

If the mismatch error of the switches and additional cascode transistors is taken into account the overall basic current cell circuit can be optimised without introducing the arbitrary safety margin (ΔV_{safe}) as is shown in the following.

In the proposed sizing procedure the whole range of possible CS and SW overdrive voltages that verify (4) is explored including process variations. For each pair $\left(V_{OD}^{CS},V_{OD}^{SW}\right)$ the minimum area and aspect ratio of the CS transistor is found using eq. (2). If the length of the SW transistor is chosen to be minimum (this maximizes the transconductance of the SW transistor and minimizes the clock feedthrough) the area and aspect ratio of the SW transistor are found from the SW overdrive voltage and the I current value. The settling time in this type of converters can be approximated by the time constant of the lower frequency of one of two real poles, the first corresponding to the output node and the second corresponding to the internal node. The pole frequencies can be represented against $\left(V_{OD}^{CS},V_{OD}^{SW}\right)$ or other equivalent transistor parameters to choose the optimum sizing if settling time is the most important concern, as it is shown in the next section. Indeed, other parameters (output impedance, total area) may be used instead as the optimization goal depending on the system requirements.

In order to include in the previous analysis the effect of process variations in the SW transistor, the statistical variation of the two bounds for the SW gate voltage in eq. (3) is modeled by means of a Gaussian distribution. The variance of the upper bound is found by expressing ΔV_o^{max} as a function of the LSB current I and the load resistance R_L and taking partial derivatives:

$$\sigma_{V_{gSW}^{max}}^2 \approx \left(\frac{\partial V_{gSW}^{max}}{\partial I}\right)^2\sigma_I^2+\left(\frac{\partial V_{gSW}^{max}}{\partial V_T^{SW}}\right)^2\sigma_{V_T^{SW}}^2+\left(\frac{\partial V_{gSW}^{max}}{\partial R_L}\right)^2\sigma_{R_L}^2 =$$
$$= \frac{A_{VT}^2}{W_{SW}L_{SW}}+\Delta V_o^{max\,2}\left(\frac{\sigma_I^2}{I^2}+\frac{\sigma_{R_L}^2}{R_L}\right) \quad (6)$$

Similarly, the variance of the lower bound yields:

$$\sigma_{V_{gSW}^{min}}^2 \approx \frac{A_{VT}^2}{W_{CS}L_{CS}}+\frac{A_{VT}^2}{W_{SW}L_{SW}}+\frac{V_{OD}^{SW\,2}}{4}\left(\frac{\sigma_I^2}{I^2}+\frac{A_\beta^2}{W_{SW}L_{SW}K'^2}\right) \quad (7)$$

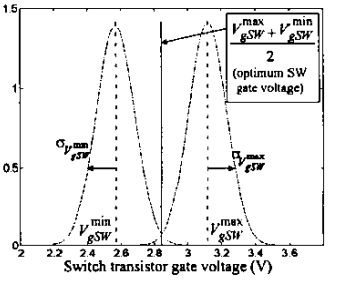

Figure 1b. Illustration of equation (8).

To find an appropriate value for the SW gate voltage, the upper bound must be larger than the lower bound in a given percentage of the cases expressed by *yield_SW*. If this is accomplished, the optimum of the SW gate voltage found in (5) has to verify that:

$$p\left(\left[V_{gSW}^{max}-\frac{V_{gSW}^{max}+V_{gSW}^{min}}{2}\right]>0\right) \ge yield\_SW \text{ and}$$
$$p\left(\left[\frac{V_{gSW}^{max}+V_{gSW}^{min}}{2}-V_{gSW}^{min}\right]>0\right) \ge yield\_SW \quad (8)$$

conditions which are illustrated in figure 1b and that can be expressed also as:

$$\frac{V_{gSW}^{max}-V_{gSW}^{min}}{2} \ge S\max\left[\sigma_{V_{gSW}^{max}},\sigma_{V_{gSW}^{min}}\right] \quad ;(9)$$

here, since only one half of the Gaussian distribution has to be considered, $S = \mathbf{inv\_norm}(yield\_SW)$ where $yield\_SW$ is related to the INL $yield$ by:

$$yield = yield\_SW^2 \tag{10}$$

because the LSB current cell is the worst case of the bounds variance (its area is the smallest of all the current sources) and its two complementary SW transistors must be both inside the bounds with the same probability. The expression of eq. (9) represents a saturation constraint more realistic than eq. (4) where an arbitrary safety margin has to be included.

2.2 Cascoded current cell (CS+CAS+SW) sizing

If an additional cascode transistor is inserted, as shown in Fig. 2(b), the previous analysis is applied to both the SW and CAS transistors. The optimum of the DC output impedance is found in this case when the SW and CAS gate voltages are:

$$\begin{aligned} V_{gCAS} &= V_T^{CAS} + \frac{1}{3}\left[V_{DD} - \Delta V_o^{\max} + 2V_{OD}^{CS} + 2V_{OD}^{CAS} - V_{OD}^{SW}\right] \\ V_{gSW} &= V_T^{SW} + \frac{1}{3}\left[2\left(V_{DD} - \Delta V_o^{\max}\right) + V_{OD}^{CS} + V_{OD}^{CAS} + V_{OD}^{SW}\right] \end{aligned} \tag{11}$$

The CAS transistor introduces two new degrees of freedom: its overdrive voltage and its area (or channel length). One of these two degrees of freedom can be eliminated as discussed in [8] using an output impedance/bandwidth criterion by relating the sizes of the SW and the CAS transistors. Another possible criterion is to choose the minimum width for the CAS transistor which, in addition to minimise the CAS transistor area, also minimises the parasitic capacitance at the source of the SW transistors thus yielding a reduced settling time (assuming that the pole due to this node is the limiting one). Therefore, the area (or dimensions) of the CAS transistor is univocally determined by its overdrive voltage and the current I. In this case the range of SW and CAS overdrive voltages that guarantee saturation is found by solving (9) for the two transistors, where the SW and CAS gate voltage bounds statistical variances due to process variations are given by:

$$\begin{aligned} \sigma^2_{V_{gSW}^{\max}} &\approx \frac{A_{VT}^2}{W_{SW}L_{SW}} + \Delta V_o^{\max 2}\left(\frac{\sigma_I^2}{I^2} + \frac{\sigma_{R_L}^2}{R_L}\right) \\ \sigma^2_{V_{gSW}^{\min}} &\approx \frac{A_{VT}^2}{W_{SW}L_{SW}} + \frac{A_{VT}^2}{W_{CAS}L_{CAS}} + \frac{V_{OD}^{SW2}}{4}\left(\frac{\sigma_I^2}{I^2} + \frac{A_\beta^2}{W_{SW}L_{SW}K'^2}\right) \\ \sigma^2_{V_{gCAS}^{\max}} &\approx \frac{A_{VT}^2}{W_{SW}L_{SW}} + \frac{A_{VT}^2}{W_{CAS}L_{CAS}} + \frac{V_{OD}^{SW2}}{4}\left(\frac{\sigma_I^2}{I^2} + \frac{A_\beta^2}{W_{SW}L_{SW}K'^2}\right) \\ \sigma^2_{V_{gCAS}^{\min}} &\approx \frac{A_{VT}^2}{W_{CS}L_{CS}} + \frac{A_{VT}^2}{W_{CAS}L_{CAS}} + \frac{V_{OD}^{CAS2}}{4}\left(\frac{\sigma_I^2}{I^2} + \frac{A_\beta^2}{W_{CAS}L_{CAS}K'^2}\right) \end{aligned} \tag{12}$$

and the saturation condition is given by two equations:

$$\begin{aligned} \frac{V_{gSW}^{\max} - V_{gSW}^{\min}}{2} &\geq S\max\left[\sigma_{V_{gSW}^{\max}}, \sigma_{V_{gSW}^{\min}}\right] \\ \frac{V_{gCAS}^{\max} - V_{gCAS}^{\min}}{2} &\geq S\max\left[\sigma_{V_{gCAS}^{\max}}, \sigma_{V_{gCAS}^{\min}}\right] \end{aligned} \tag{13}$$

3. OPTIMUM SIZING OF A 12 BITS CURRENT-STEERING DAC

The optimization process described in the above section has been implemented in MATLAB and applied to the design of a 12 bits DAC. The target technology is a 0.35μm CMOS process. The segmentation has been set to b= 4 and m = 8 bits, V_{DD} = 3.3V, $\Delta V_o^{\max} = 1$ V and $R_L = 50\Omega$. The internal node interconnection capacitance has been estimated to be 100 fF, and the output capacitance 2 pF.

If the basic current source topology is chosen (CS+SW transistors) any optimization parameter can be represented against the two degrees of freedom available (for example, the two transistors overdrive voltage, or alternatively their corresponding area). Fig. 2 shows graphs representing optimum sizing for two criteria (area and settling time). The upper graph represents the two pole frequencies against the area of the CS and SW transistors, whilst the lower graph shows the minimum of the pole frequency against CS and SW overdrive voltages and the same optimum design points. The first pole (p_1) is due to the output load and the parasitic capacitance at the drain of all the switch transistors connected to the output (that will increase with its width). The second pole (p_2), due to the internal node, has contributions of both the parasitic capacitance of the CS drain and the SW source, and depends on the SW transistor small signal trasconductance and body effect parameters, as presented in [9]. In p_2 the interconnection capacitance between the switch & latch and the current source arrays C_{int} is taken into account [8]. The small signal parameters and parasitic capacitances determining the poles are known once the sizes of the transistors are found. The only degrees of freedom are the two transistors overdrive voltages, which univocally determine the transistor sizes, as discussed in section 2. Not all the combinations are possible, however, due to the constraint set by the saturation condition of eq. (9) that limits a region of the $\left(V_{OD}^{CS}, V_{OD}^{SW}\right)$ plane where the optimum design point should be found. For maximum speed the optimal design point is found where the minimum of the two pole frequencies is maximised. If a minimum area is the preferred goal, the point in the $\left(V_{OD}^{CS}, V_{OD}^{SW}\right)$ plane inside the saturation condition constrained region with the lowest possible $Area^{CS} + Area^{SW}$ value should be chosen, which will minimize the total area taking into account the matching constraint of eqs. (1) and (2). The saturation conditions previously used in the literature are also shown in Fig. 2 for comparison purposes. The use of an arbitrary safety margin leads to inefficient solutions as shown in the figure. For example, the optimum design point for settling time would produce larger CS transistors using the saturation condition of eq. (4) instead of the one of eq. (9). In the other hand, the optimum design point for minimum area found using eq. (4) would be out of the realistic safety design region found by eq. (9), indicating that for that case, the 0.5 V safety margin is too optimistic.

The SW+CS topology does not provide enough output impedance for a 12-bit DAC and a cascode transistor has to be added. It is cumbersome to represent the optimization parameter (for example pole frequencies) for the SW+CAS+CS topology, since a 4th dimension is required, so only the bounds for the overdrive voltages have been plotted in Fig. 3 for that topology. The design space that guarantees that all the transistors operate in saturation found by using eq. (13) is the volume under the surface. The

bounds set by the equivalent to eq. (4) for this circuit are also shown for comparison.

The final layout of the designed and implemented 12-bits DAC core is shown in Fig. 4. Simulation results at transistor level including all the parasitics extracted from the layout indicate an SFDR of 65dB for a sinusoidal input of 53MHz sampled at 300MHz. The settling time for a full scale differential output swing is 2.5ns, as shown in the transient simulation result of fig. 5, allowing operation of the DAC up to 400 Msamples/s.

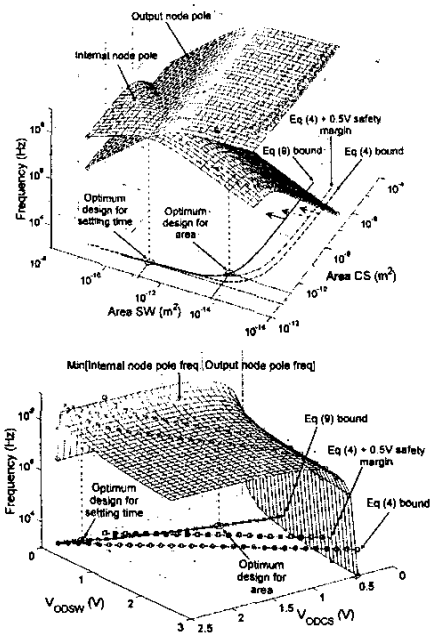

Figure 2. Optimization graphs for the SW+CS topology for a 12 bits DAC

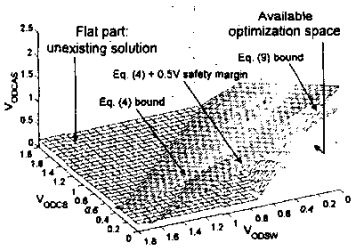

Figure 3. Design space for the SW+CAS+CS topology for a 12-bit DAC

4. CONCLUSIONS

This work presents a sizing and design sequence for high-speed high-accuracy current steering DACs that avoids the introduction of an arbitrary safety margin for the overdrive voltages by analyzing the effects of process variations in the operating conditions of all the transistors of the current cell. The design procedure allows further minimization of the total DAC area. The presented approach takes into account the mismatching effects to find a safe design space for the two most usual topologies of the current cell. As an illustrative case, the design procedure has been succesfully applied for the implementation of a 12-bit 0.35μm CMOS current-steering DAC.

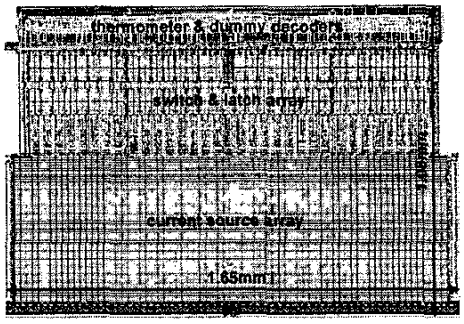

Figure 4. Layout of the designed 12-bit DAC

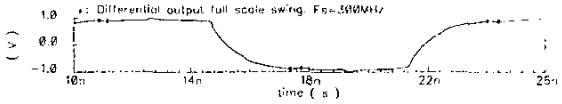

Figure 5. Transient simulation results of the DAC

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5. REFERENCES

[1] M. Gustavsson, J.J. Wikner, N.N. Tan, *CMOS Data Converters for Communications*, Kluwer Academic Publishers, Boston, 2000.

[2] Paul Hendriks, "Specifying Communication DACs", *IEEE Spectrum*, July 1997, pp. 58-69.

[3] Y. Cong, R.L. Geiger, "Switching Sequence Optimization for Gradient Error Compensation in Thermometer-Decoded DAC Arrays", *IEEE Tr. on Circuits and Systems-II*, Vol. 47, No. 7, 2000, pp. 585-595.

[4] J. Vandenbussche, G. Van der Plas, W. Daems, A. Van den Bosch, G. Gielen, M. Steyaert, W. Sansen, "Systematic Design of High-Accuracy Current-Steering D/A Converter Macrocell for Integrated VLSI Systems", *IEEE Tr. on Circuits and Systems-II*, Vol. 48, No. 3, 2001, pp. 300-309.

[5] C.H. Lin, K. Bult, "A 10.b, 500-Msample/s CMOS DAC in 0.6 mm^2", *IEEE J. of Solid-State Circuits*, Vol. 33, No. 2, 1998, pp. 1948-1958.

[6] JL González, E. Alarcón, "Clock-Jitter Induced Distortion in High-Speed CMOS Switched-Current Segmented Digital-to-Analog Converters", in *Proc. of IEEE Intl. Symposium on Circuits and Systems (ISCAS'01)*, May 2001, pp. I512-I515.

[7] B. Razavi, *Principles of Data Conversion Systems*, IEEE Press, New Jersey, 1995.

[8] A. Van den Bosch, M. Staeyaert, W. Sansen, "SFDR-Bandwidth Limitations for High Speed High Resolution Current Steering CMOS D/A Converters", *Proc. IEEE Int. Conf. Electronics, Circuits ans Systems (ICECS)*, 1999, pp. 1193-1196.

[9] J. Bastos, A.M. Marques, M.S.J. Steyaert, W. Sansen, "A 12-Bit Intrinsic Accuracy High-Speed CMOS DAC", *IEEE J. of Solid-State Circuits*, Vol. 33, No. 12, 1998, pp. 1959-1969.

[10] A. Van den Bosch, M.A.F. Borremans, M.S.J. Steyaert, W. Sansen, "A 10-bit 1-Gaample/s Nyquist Current-Steering CMOS D/A Converter", *IEEE J. of Solid-State Circuits*, Vol. 36, No. 3, 2001, pp. 315-324.

[11] A. Van den Bosch, M. Steyaert, W. Sansen, "Design Techniques for High Accuracy, Current-Steering CMOS D/A Converters", *3rd Workshop on ADC Modelling and Testing*, 1998, pp. 861-866.