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CATRENE-PANAMA
WP1: Integrated PA Milestone M1.3
Technology, approach & system choice for Home Networking

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Revision history:

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I – Overview

Specifications provided by Gigle for the coax-communications pre-Power Amplifier (pre-PA) are presented in section II.

The ST CMOS045 technology is firstly summarised in section III. The list found in that section contains all options available for the normal process and for the RF extension. There are also some figures to evaluate quickly voltage and current limitations of the devices.

All transistors that could be used in the design are evaluated in the next sections. Their Figure of Merit and their gain are plotted in order to compare each transistor type.

Finally, a first and second draft of the pre-PA circuit in CMOS045 technology are briefly presented. External components selection is given in this part. Inductors and capacitors come from muRata catalogue available on its website. Then, the final design of the pre-PA is done in CMOS65 due to un-availability of the 45nm process in CMP runs during 2009. The behaviour of the circuit is simulated with the focus set on power consumption and linearity.

II – Specifications

Specifications provided by Gigle.

	Min	Typ	Max	Comment
Gain		16dB		Over the whole band of signal
MTPR			-36dBc	
Frequency Band A range	800MHz		1.5GHz	
Frequency Band B range	1.5GHz		2GHz	
Frequency Band C range	2GHz		2.5GHz	
Frequency Band D range	300MHz		800MHz	Internally the four bands should be handled by the PA without any change. Externally each band will require different impedance matching networks.
Signal bandwidth	50MHz		250MHz	
Output power			0dBm	PSD is -70dBm/Hz over 100MHz on the physical medium.
Power control	-10dBm	-5dBm	0dBm	This control should be possible in the pre-amp.
Input impedance		50ohm		
Output impedance		50ohm		
Power Added Efficiency	10%	20%		

Table 1: Power Amplifier specifications

III – Summary of the Design Rules Manual (DRM)

Process supported:

CMOS045 Standard Process:

- CMOS045_LP:
- both of LVT (low Vt) and SVT (standard Vt) on the same die
- 1.8V or 2.5V for IO devices
- metallization: 7M-4X-0Y-2Z
- low leakage SRAM (high density) using LP core oxide

Technology option:

- **LP HS SRAM:** CMOS045_LP + High-Speed SRAM
- **HVT:** CMOS045_LP + HVT (high Vt)
- **GP:** CMOS045_LP + GP-SVT (standard Vt) and GP-HVT (high Vt)
- **GP HS SRAM:** GP + High-Speed GP SRAM

CMOS045 AMS Standard Process:

- **inductors** (indsym_hq_7m4x0y2z, inddif_hq_7m4x0y2z)
- **RF-MOM** (cfrstack_rf_7m4x0y2z, cfrstack_rf_7m4x0y2z_sh, cfrstack_rf_7m4x0y2z_2p)
- **varactors** (cpo11nw_var, cpo11nw_diff_var)
- **RF-MOS** (nsvtlp_rf, psvtlp_rf, nlvtlp_rf, plvtlp_rf, nsvt18_rf, psvt18_rf)

CMOS045 AMS Technology option:

- **XHPA:** CMOS045_LP + Free High-Performance Analog core MOSFETs

Warning: 2.5V transistors *for IO are NOT supported on AMS model*

Technology limitations:

Supply voltage:

- **LP:** 1.1V ±10%
- **GP:** 0.9V ±10%
- **1.8V IO:** 1.8V ±10%
- **2.5V IO:** 2.5V ±10%
- **RF-MOM:** 3.3V ±10%

Current limitations:

- **NLVTLP:** 765µA/µm Ldrawn=0.040 µm
- **PLVTLP:** 370 µA/µm

- **NSVTLP:** 620 µA/µm Ldrawn=0.040 µm
- **PSVTLP:** 300 µA/µm

- **NSVT18:** 680 µA/µm Ldrawn=0.150 µm
- **PSVT18:** 300 µA/µm

- **NSVT25:** 600 µA/µm Ldrawn=0.270 µm
- **PSVT25:** 350 µA/µm

- **M1:** Idc=0.095 mA and Irms=1.2mA for W=0.070 µm @ 105ºC
  Idc=0.005 mA and Irms=1.15mA for W=0.070 µm @ 150ºC

- **MiX:** Idc=0.103 mA and Irms=0.97mA for W=0.070 µm @ 105ºC
  Idc=0.005 mA and Irms=0.93mA for W=0.070 µm @ 150ºC

- **MiZ:** Idc=4.414 mA and Irms=10.17mA for W=0.400 µm @ 105ºC
  Idc=0.234 mA and Irms=9.60mA for W=0.400 µm @ 150ºC

- **AP:** Idc=15.96 mA and Irms=29.68mA for W=2.000 µm @ 105ºC
  Idc=4.320 mA and Irms=27.56mA for W=2.000 µm @ 150ºC

Voltage limitations:

Maximum DC Gate Oxide Voltage

- **LP NMOS:** 1.5V @ 125ºC

- **LP PMOS:** 1.25V @ 125ºC

- **OD18 NMOS:** 2.36V @ 125ºC
- **OD18 PMOS:** 2.46V @ 125ºC

IV – Performances of the Design Kit (DK)

These evaluations are made with the minimal length for each transistor and a width set at 10µm with 10 fingers.

IV.1 – Figure of merit (Ft)

An evaluation of the technology was made with NLVTLP, NSVT18 and NSVT25 transistors. The Figure of merit (Ft) is the frequency where the current gain of the MOS is equal to the unity. In fact, this is only a theoretical value which is a way to compare different transistors. This evaluation depends on the polarisation point of the transistor; Ft depends on both Vgs and Vds.

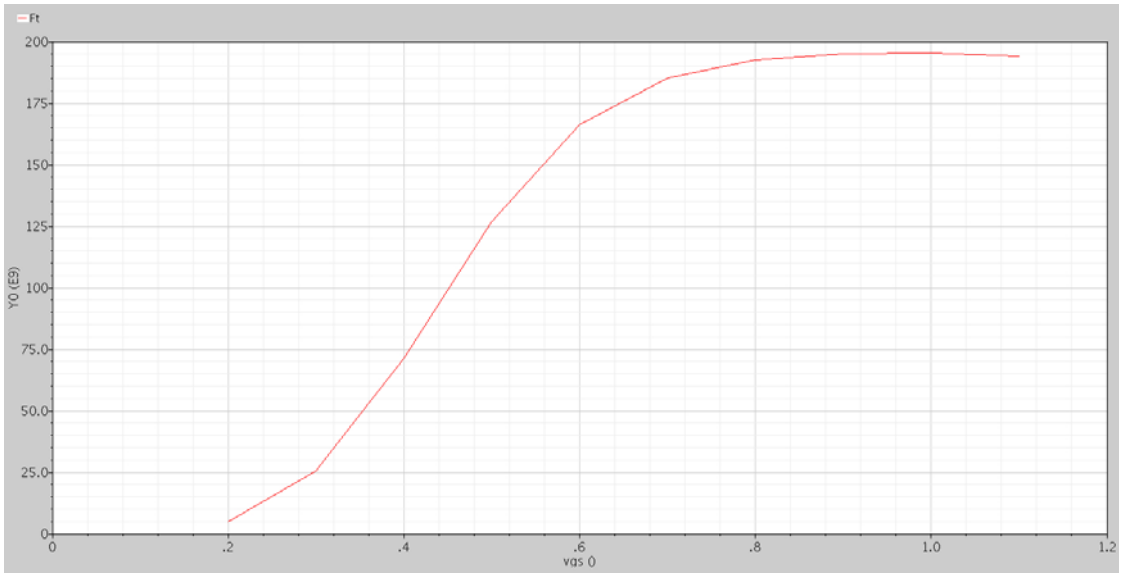

Figure 1: Ft versus Vgs in GHz at Vds=0.6V (NLVTLP)

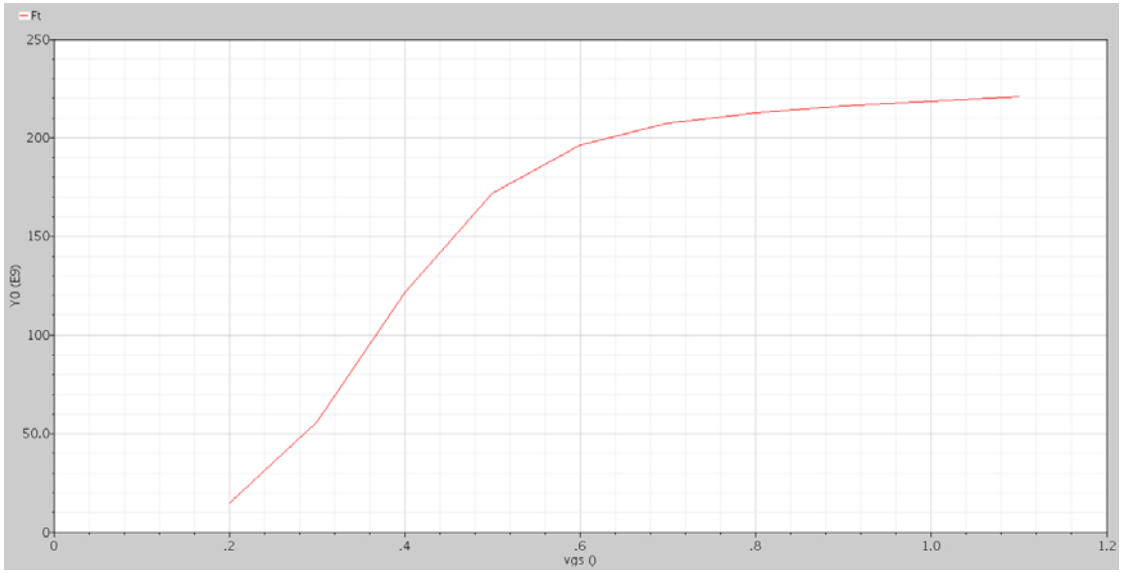

Figure 2: Ft versus Vgs in GHz at Vds=1.1V (NLVTLP)

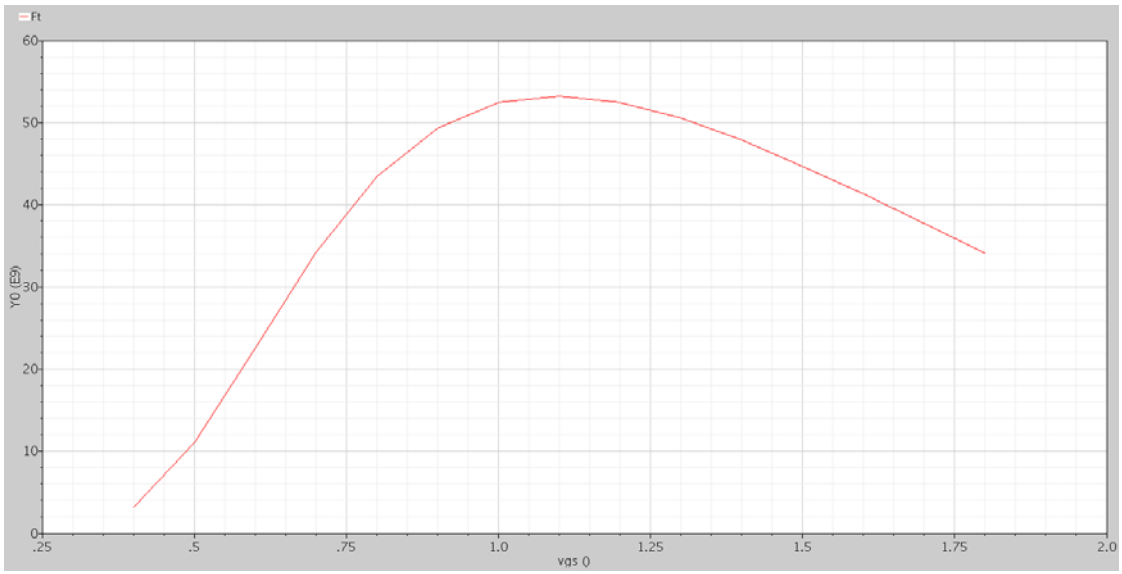

Figure 3: Ft versus Vgs in GHz at Vds=0.6V (NSVT18)

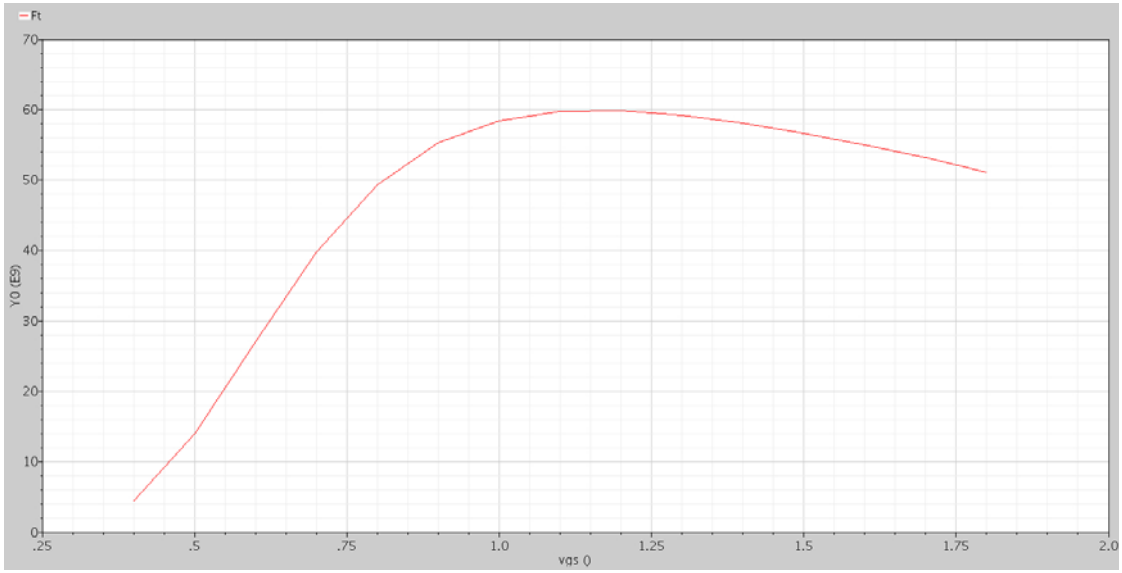

Figure 4: Ft versus Vgs in GHz at Vds=1.1V (NSVT18)

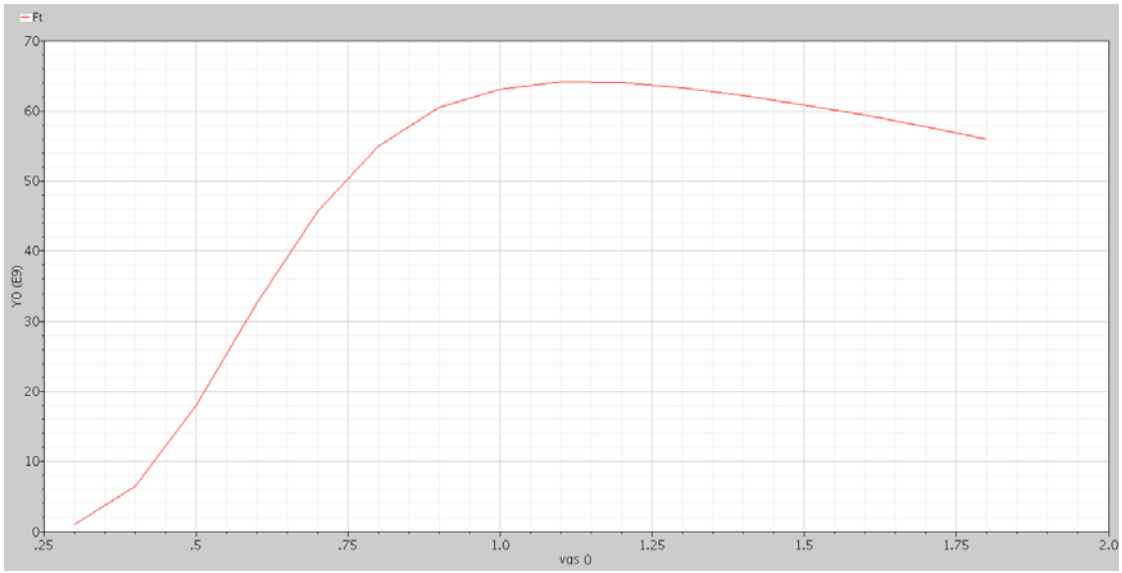

Figure 5: Ft versus Vgs in GHz at Vds=1.8V (NSVT18)

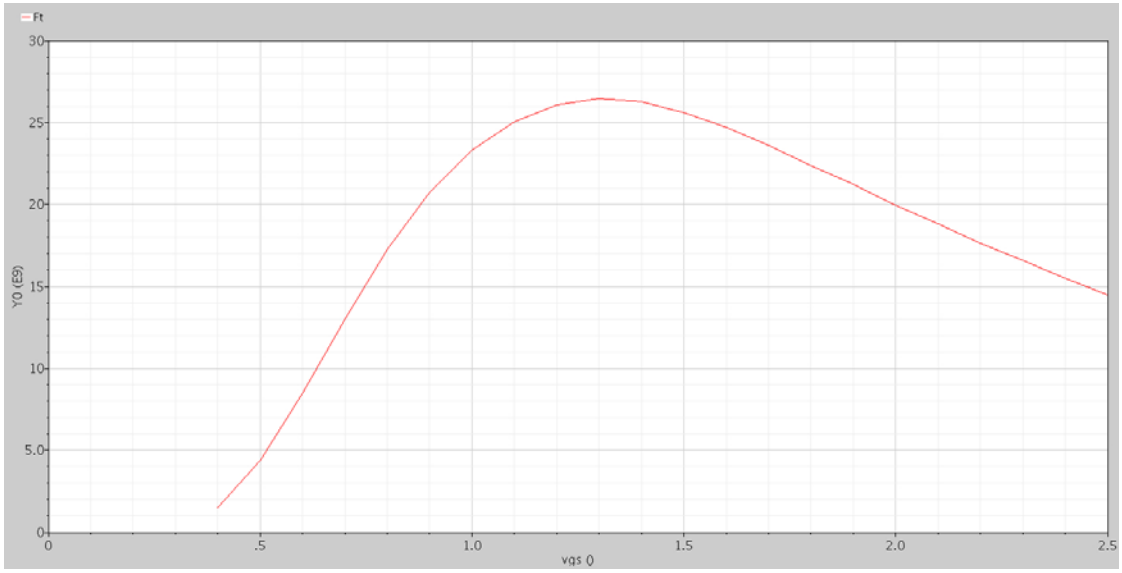

Figure 6: Ft versus Vgs in GHz at Vds=0.6V (NSVT25)

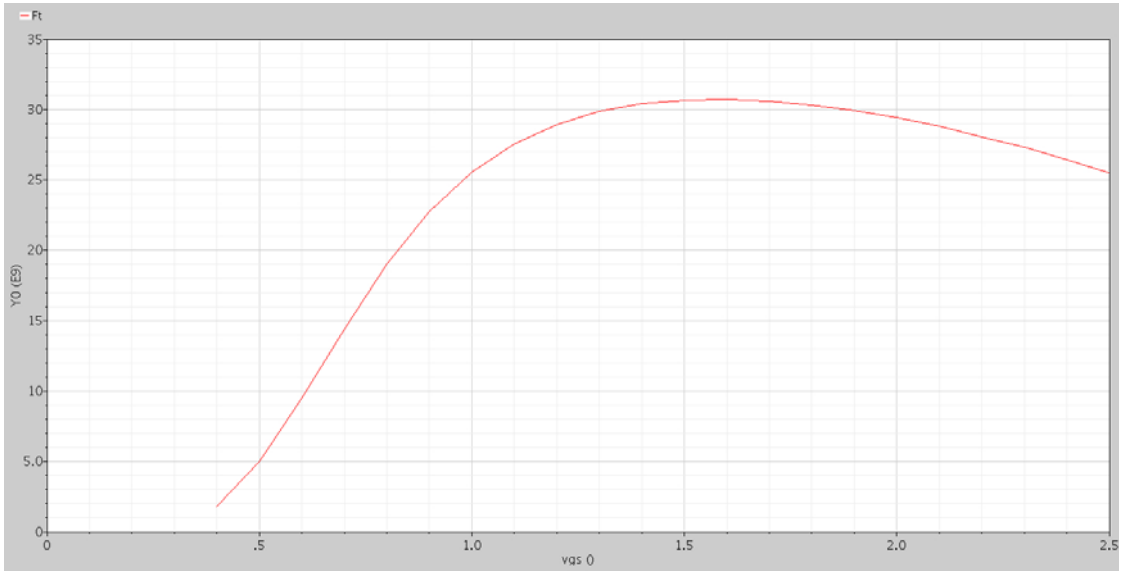

Figure 7: Ft versus Vgs in GHz at Vds=1.1V (NSVT25)

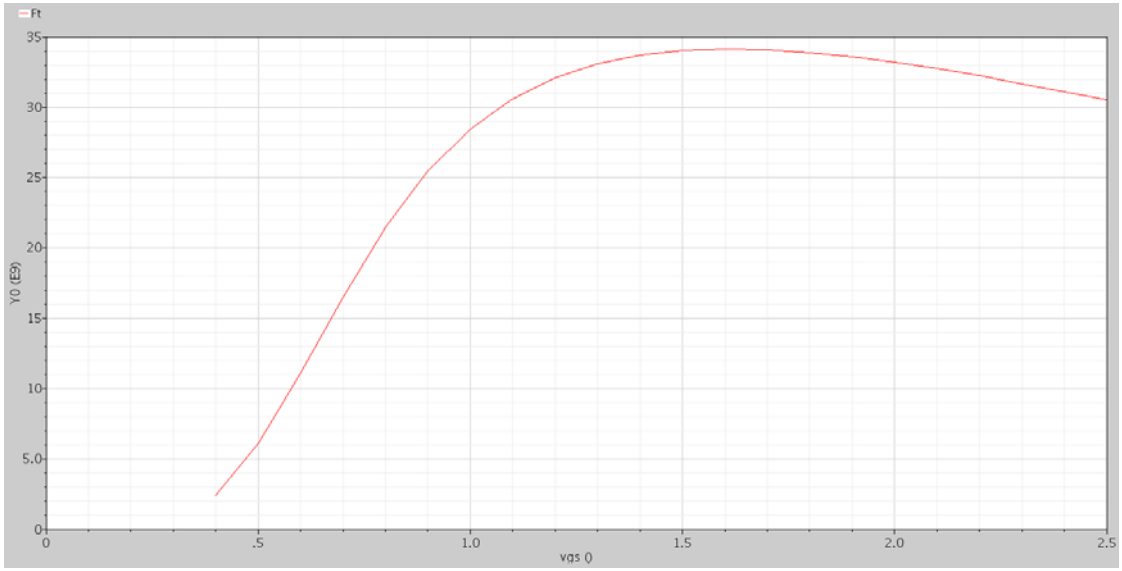

Figure 8: Ft versus Vgs in GHz at Vds=2.5V (NSVT25)

IV.2 – Gain of the transistor (Gm)

Gain of a transistor is also important to be compared. More than the lat one, this test is highly dependant on the size of the transistor.

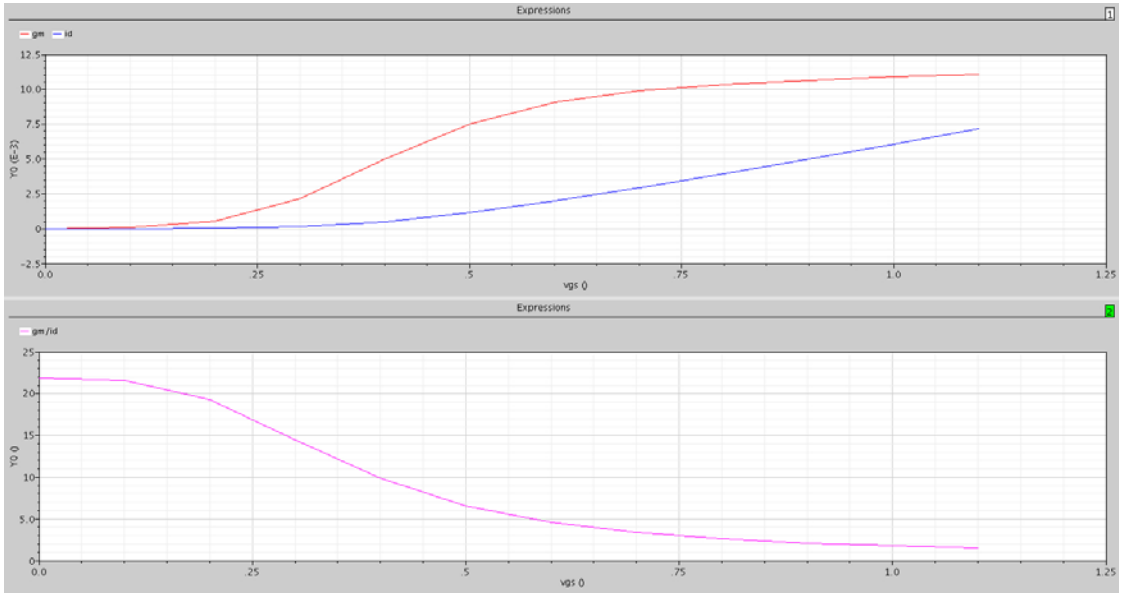

Figure 9: gm, id and gm/id versus Vgs in GHz (NLVTLP)

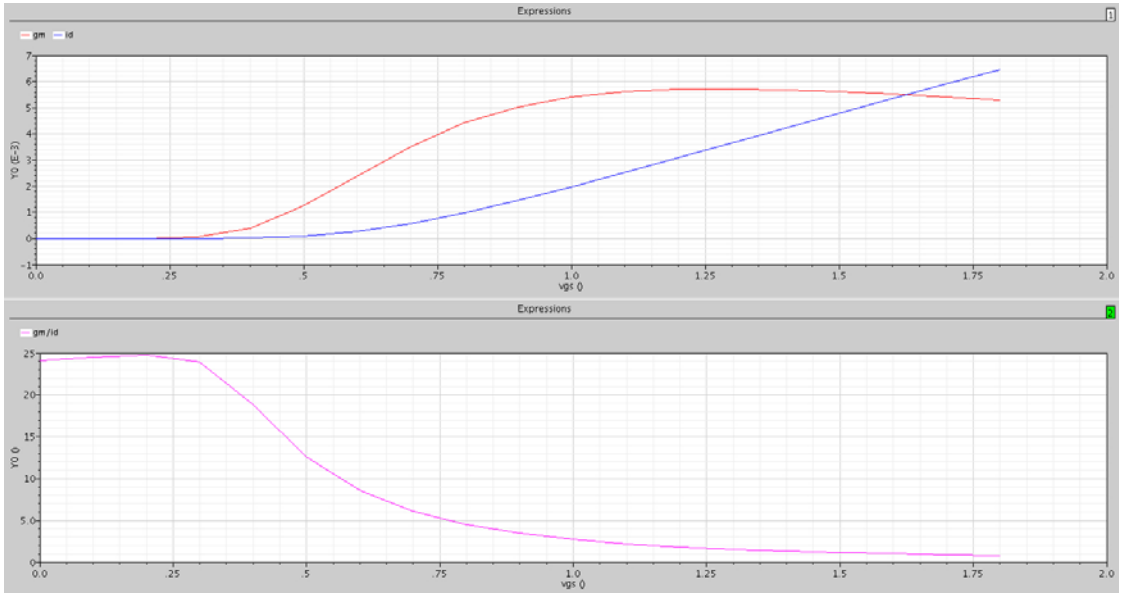

Figure 10: gm, id and gm/id versus Vgs in GHz (NSVT18)

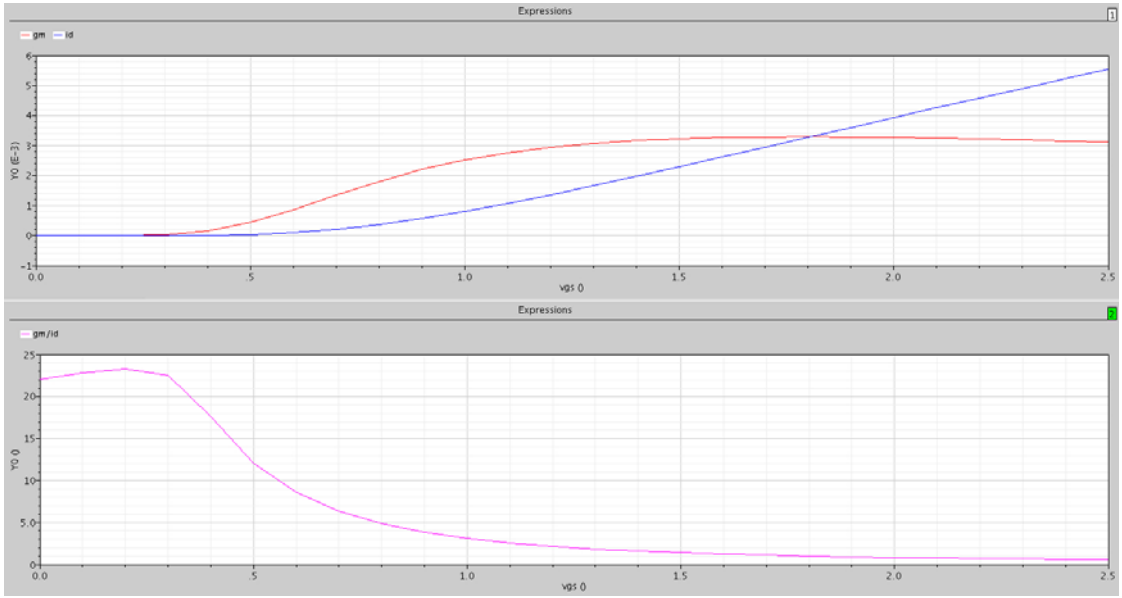

Figure 11: gm, id and gm/id versus Vgs in GHz (NSVT25)

V – Design review

V.1 – First draft

The first design was made by a single transistor. This topology with an inductor load (RFC) implies a voltage supply lower than the maximum Vds voltage supported by the transistor. Considering this, the NSVT25 has been chosen to have the higher voltage supply.
This solution showed its limits quickly due to its incapacity to have a high gain with reasonable size for the transistor.
That leads us up to the second draft.

V.2 – Second draft

In this version, a cascode topology was selected. Cascode topology brings good behaviour in lot of parts of the design. Using a NLVTLP for the cascoded transistor (at the bottom) and a NSVT25 for the cascoding one (at the up) we have the benefit of each one. The NLVTLP has a higher gain for the same width than the NSVT25 but a Vds maximum voltage below. With the cascode the gain AND the high Vds are possible. Moreover, it increases the isolation between the output and the input.
Figure 12 shows the core of the circuit.

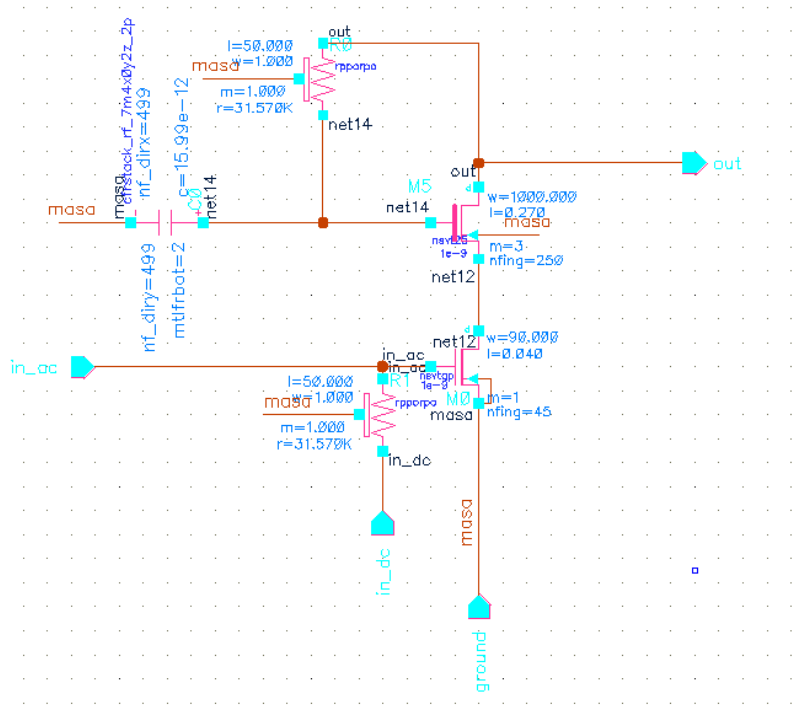

Figure 12: Core CMOS045

This power amplifier needs external components which can be different for each frequency band. To do this, components from the muRata's library has been chosen.

The components chosen are the followings:

Capacitor1: GQM1885C1H101JB01 for D frequency band (490MHz)
Capacitor2: GQM1875C2E470JB12 for A frequency band (1.09GHz)
Capacitor3: GQM1885C1H130JB01 for B frequency band (1.73GHz)

Capacitor4: GQM1875C2E100JB12 for C frequency band (2.24GHz)

Models RLC series:

490MHz: R=56mΩ; L=0.59nH; C=100pF
1.09GHz: R=115mΩ; L=0.49nH; C=47.12pF
1.73GHz: R=125mΩ; L=0.65nH; C=13.05pF
2.24GHz: R=176mΩ; L=0.48nH; C=10.1pF

Inductor1: LQW15AN91NJ00 for D frequency band (490MHz)
Inductor2: LQW15AN43NH00 for A frequency band (1.09GHz)
Inductor3: LQW15AN20NH00 for B and C frequency band (1.73GHz and 2.24GHz)

Models RL series C parallel:

490MHz: R=6.416Ω; L=87.43nH; 30fF
DC: R=784mΩ; L=94.51nH; C=30fF

1.09GHz: R=4.21Ω; L=41.59nH; C=30fF
DC: R=0.394Ω; L=45.25nH; C=30fF

1.73GHz: R=2.638Ω; L=19.23nH; C=30fF
DC: R=155mΩ; L=20.99nH; C=30fF

2.24GHz: R=3.041Ω; L=19.15nH; C=30fF
DC: R=155mΩ; L=20.99nH; C=30fF

Two models for the inductor are used in order to take into account frequency dependent resistance and inductance. The first one at the central frequency of the band and the other one at DC because they have a serial resistance very different who could change the biasing point.

The complete design of this circuit (on chip and external components) is presented on Figure 13. As said before, there are two models of the inductor to have the good DC operating point (model connected to the 1H-inductor) and the good behaviour at high frequency (model connected to the 1F-capacitor).

The load, which is not represented here, is a 50Ω-load.

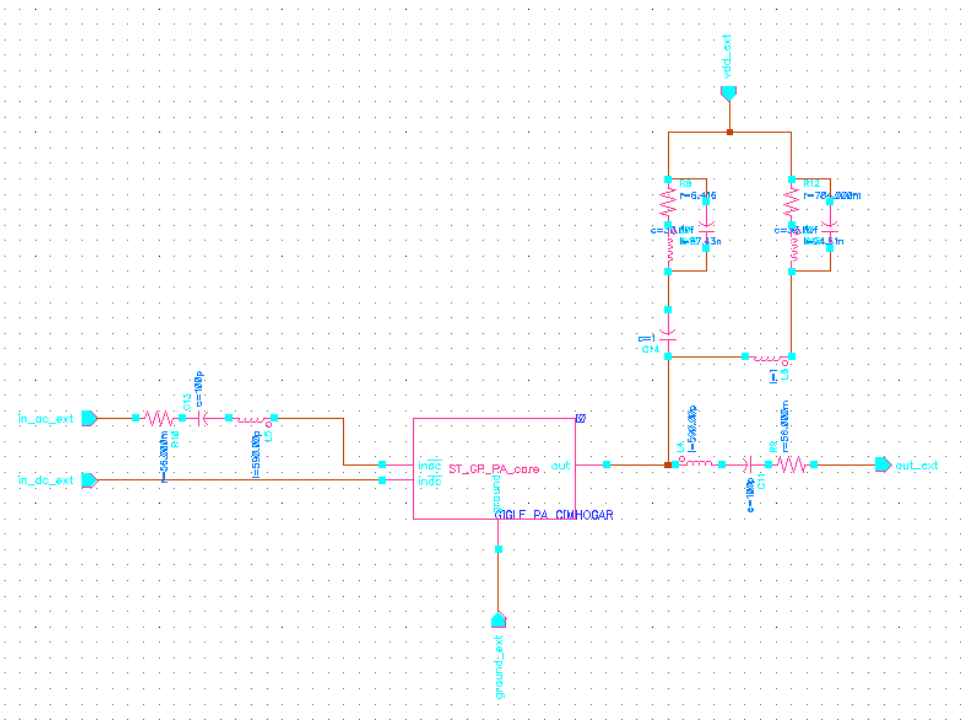

Figure 13: Complete design

V.3 – Linearity

Linearity is measured with an OFDM signal. The input signal has a very high MTPR (limited by the numerical floor noise); the output must reach a MTPR better than -36dB for all the notches present in the band.

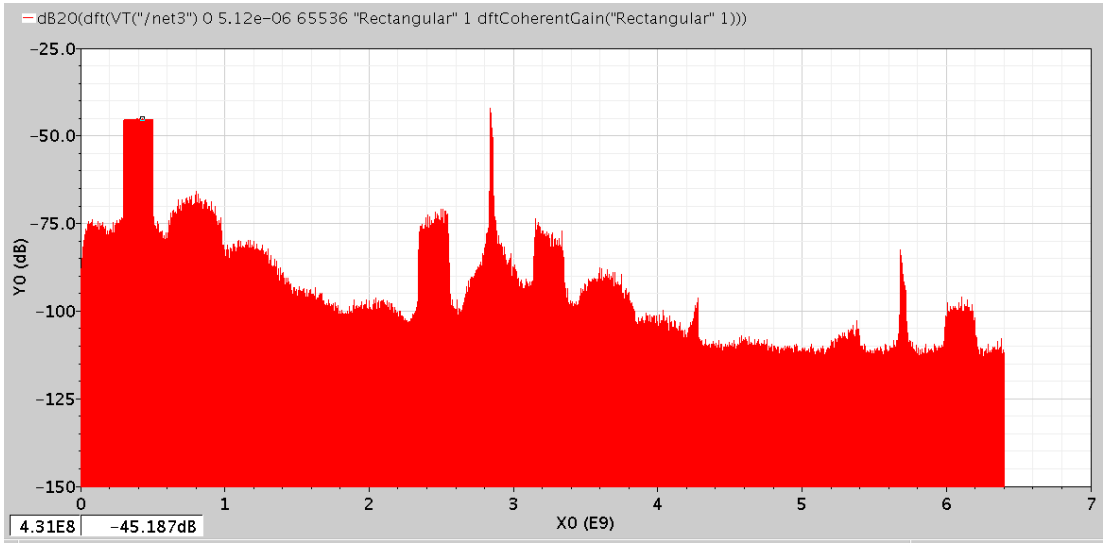

Figure 14: FFT for CMOS045 single-ended @400MHz

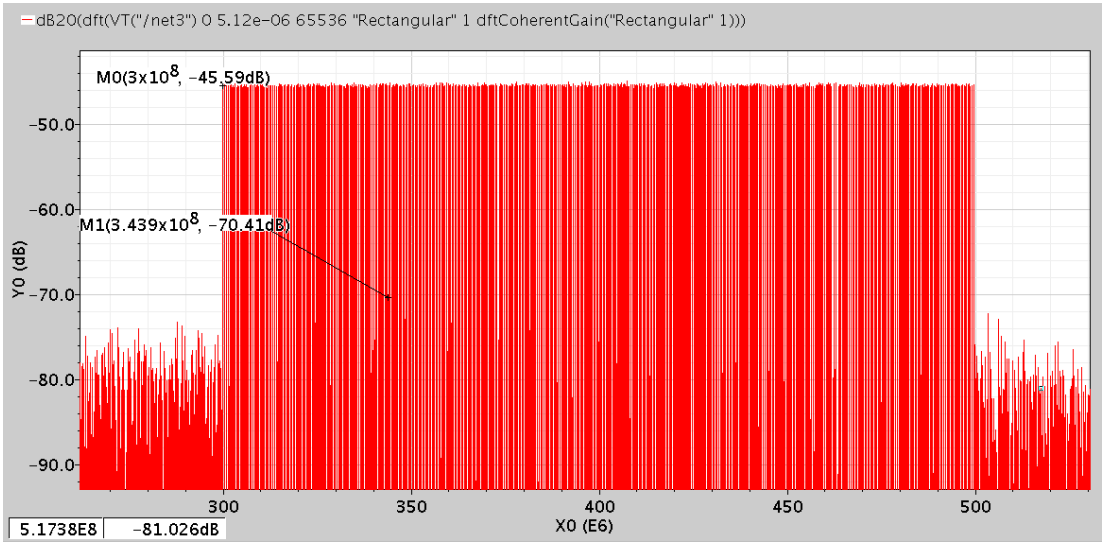

Figure 15: Zoom to the MTPR for the CMOS045 single-ended @400MHz

According to the last FFT, the linearity constraint is too high for this design with a MTPR of -25dB is reached.

Next step is to try differential topology to see whether linearity could be improved.

VI – Changing of technology and pre-PA topology

As Gigle asks us, a migration from CMOS045 to CMOS065 was made. This migration was made by changing the topology too. The new differential topology provides a better rejection of the second order intermodulation products. The topology is given in Figure 16. Transistors used are low power ones (nlvtlp) at the bottom and 1V8 IO ones (nsvt18) for the cascode. This combination allows high gain with the nsvtlp (which have a 60nm-length gate) and a quite large signal output who can reach up to 1.8V.

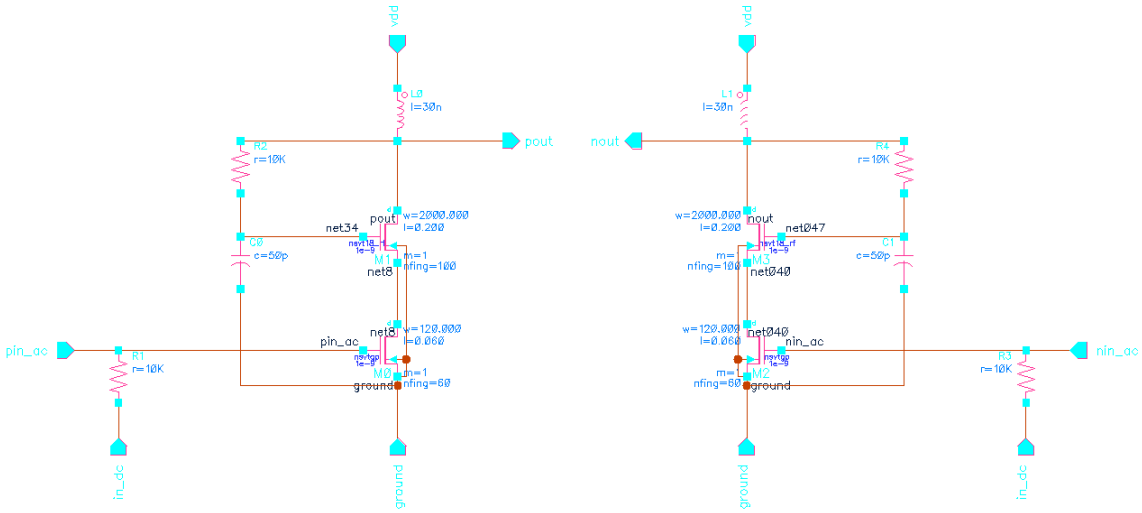

Figure 16: Topology of the pseudo-differential design in 65nm

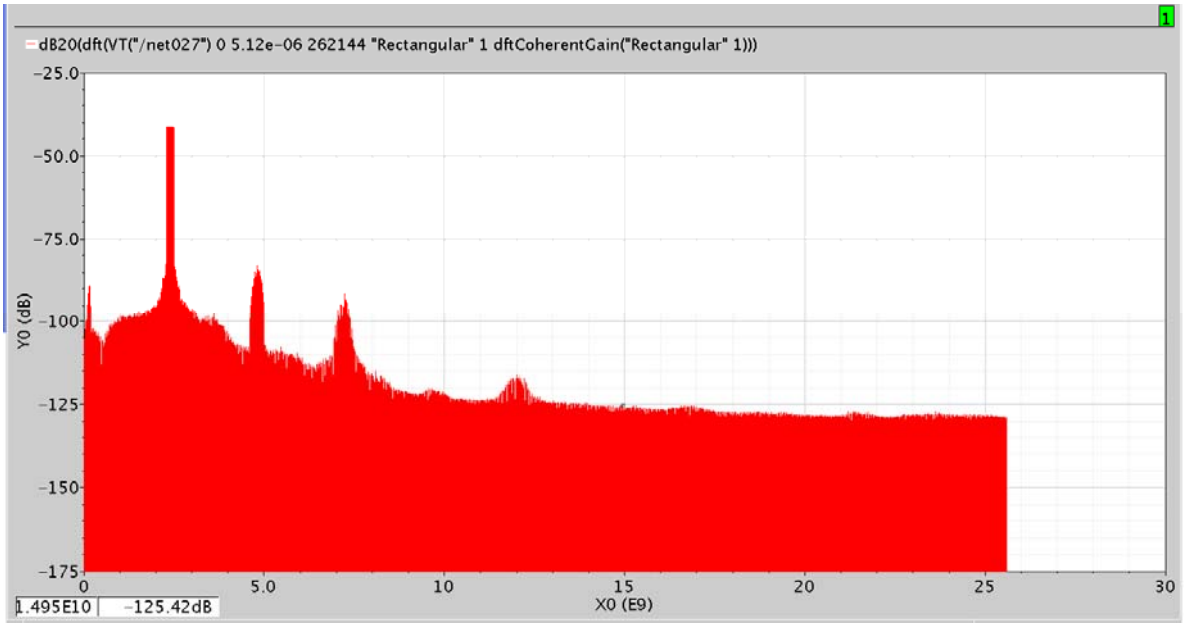

Figure 17: FFT for CMOS065 differential @2.4GHz

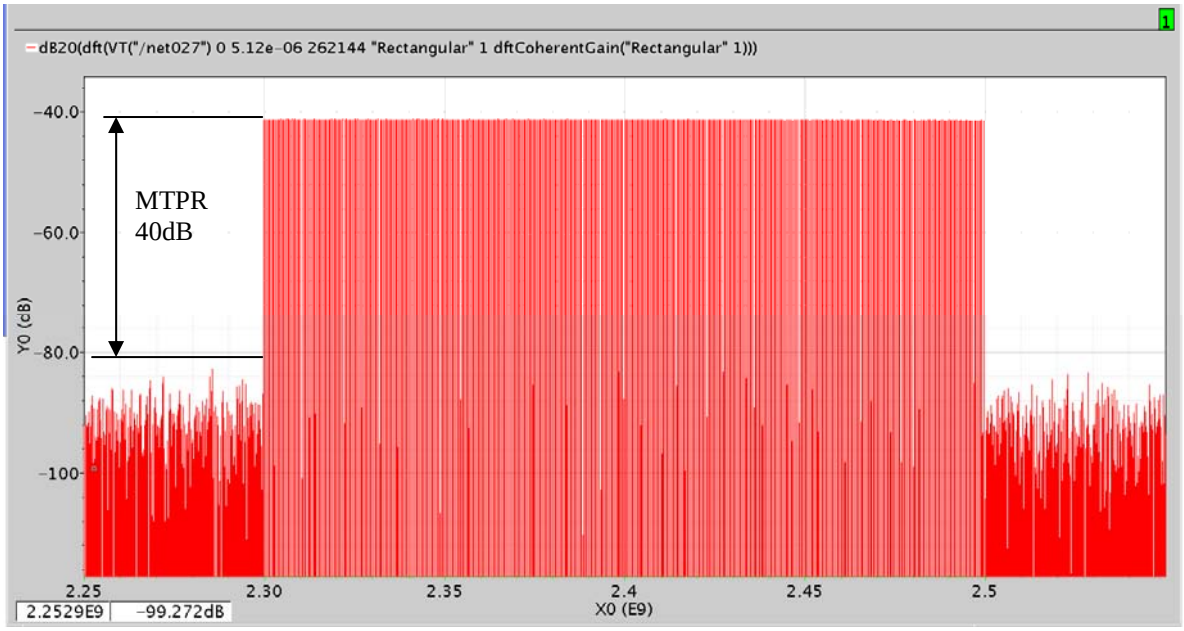

Figure 18: Zoom to the MTPR for the CMOS065 differential @2.4GHz

As the Figure 17 and Figure 18 show, the pseudo-differential topology gives a better linearity, a -40dB of MTPR is reached. The consumption is 95mW with a 1.1V voltage supply. The layout of the only PA is 450*250µm^2 and the maximum output power is nearly 11dBm at -1dB compression point.

VII – Conclusion

Next step is the fabrication of the prototype to validate the choices. The chip will be embedded in a QFN24 package to be mounted on a board. Because the main area is occupied by capacitors, the changing of technology will not change drastically the size of the chip. The benefit of 45nm or beyond should be seen in the power consumption and gain.
These CMOS technologies allow fabrication of analog component and digital ones on the same die and tend to introduce system on chip. The next challenge is to unify the technology of the PA to the technology of the digital part.