Digital Signature Generator for Mixed-Signal Testing

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Abstract—**A novel Digital Signature Generator to monitor two analog signals is proposed. The X-Y plane is divided by non linear boundaries into zones in order to generate the digital output for each analog (x,y) location. The circuit is based on a differential amplifier input stage modified by splitting the input MOSFETs. In this way two input signals are provided on each side of the differential stage. The output stage is based on a differential comparator with digital single ended output. The location and slope of the zone boundary depend on the relative sizes of the input transistors. The proposed signature generator is designed to be integrated in Built-In M-S testing and diagnosis circuits. Each monitor only requires 8 transistors for the input stage and 12 transistors for the digital output generator. The CUT intrusion on each monitored signal is reduced to the capacitive load of a single MOSFET. A STM 65 nm technology implementation is presented to demonstrate the viability of the proposal.**

Index Terms— **M-S Test, Digital signature generation, X-Y zoning, Multi-input comparator.**

I. INTRODUCTION

Monitoring internal signals of digital and mixed-signal circuits is becoming a widely used strategy in production testing and verification to increase the observability of the internal performance.

Built-in techniques for testing, signal integrity analysis and correlation of noisy signals are direct areas of application for such monitors. Internal monitors are widely used to increase the observability of signals embedded in large ICs, not easily accessed by primary I/Os.

Oscillation-test method [1], [2] current monitoring [3], [4] and Zoning [5], [6], have been used in the past for these purposes with good results in digital and mixed-signal applications. For testing purposes, X-Y Zoning, using straight lines to cut the plane into zones to monitor signal compositions (Lissajous curves), has been proposed [7], [8]. In the X-Y zone testing method, the monitoring of signals is based on the composition of two signals of the circuit, *x(t)* and *y(t)*, in a similar way that an oscilloscope in X-Y mode represents the evolution of two signals on the screen. If the composed signals are periodic with rational ratio of periods, the resultant curves are also periodic becoming the well-known Lissajous curves. The implementation of a straight line in the X-Y plane can be accomplished with the use of weighted adders and comparators. Several monitors have been proposed in the past for this purpose [10], [11], [12]. In these techniques, the Lissajous shape was used to select X-Y partitions delimited with straight lines. Recently, a generalization of the monitoring method for multiple variables using several hyperplanes has been proposed based on Lissajous compositions on a CUT with multitone excitation [9]. The method has been applied to verify parameter shifts in a physically programmable band-pass filter with selectable natural frequency. The experimental results showed a good prediction of the actual natural frequency with 0.34% error in the range of ±10% frequency shifts.

In this paper we investigate the possibilities of partitioning the X-Y plane using non-straight lines by taking advantage of the non-linear dependence of the nMOS transistor drain current I_D as a function of its gate-source voltage V_{GS}. The benefits of the proposal are the monitor small size and its low loading impact on monitored signals.

The paper is organized as follows. Section II is devoted to present the X-Y zoning method and the possible partition of the plane for testing purposes. A simplified mathematical model to analyze the possible lines, their shape and position are presented. Section III introduces the new structure of the signature generator, its on-chip implementation and performance evaluation using extensive electrical simulations. In section IV a summary of the work and conclusions about the results are presented.

II. CURRENT COMPARISON APPROACH.

Previous work on monitoring signals in the X-Y plane is based on dividing the X-Y plane by straight control lines that delimit the zones where the curve have points and the zones where the curve points are not expected. In this way, a large set of parametric and catastrophic defects can be detected by just checking whether the Lissajous curve remains in the specified zone or not. Figure 1 shows a Lissajous composition of a multitone input signal and the Low-Pass output of a Biquad filter. The the nominal shape is presented in Fig.1 a and the modified shape for 10% shift in the natural frequency of the filter is shown in Fig.1 b.. Monitoring is implemented using several control lines which divide the X-Y plane in multiple zones. The digital codes of the zones traversed by the Lissajous curve become the digital signature of the circuit. Digital signatures are efficiently accessed and

internally/externally processed. In this way the Mixed-Signal CUT test and parameter verification are facilitated.

Current comparison is a straightforward way to implement control lines composing two or more voltage signals. In contrast with voltage comparison, the easy way to add and subtract currents on nodes (Kirchorff's law) imply very simple structures. Furthermore, in CMOS applications, the quasi-quadratic current-voltage characteristic of MOS transistors, in saturation, enables the implementation of non linear curves to delimit zones in the X-Y plane. These characteristics facilitate the generation of efficient zone boundaries with low area overhead.

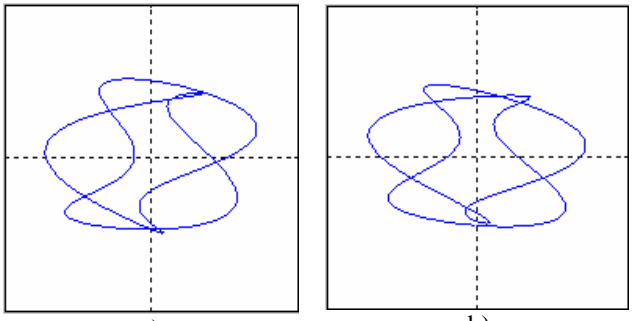

Figure 1. Lissajous composition of a multitone input signal and the Low-Pass output of a Biquad filter: a) Nominal shape, b) shape for 10% shift in the natural frequency of the filter.

In following paragraphs, we present a simplified model showing the principle of functionality of the proposed monitor.

A. Current Comparison Model

In order to illustrate the principle of operation of the monitor we will consider four voltage input signals V_1, V_2, V_3 and V_4, without loss of generality. As it will be discussed later, the number of monitored signals can be modified using the same principle of operation.

The basic architecture is similar to a source grounded differential pair or pseudo differential pair with two input transistors in each side [15], [16]. The input stage of the monitor is a differential-input differential-output stage with four input signals obtained splitting the input transistors in each side as indicated in Figure 2. The four-input monitor compares two currents generated by four voltages through the gate of nMOS transistors (transistors *M1*, *M2*, *M3* and *M4*) which deliver the current to be added at each branch of the differential input stage. Since the circuit is balanced, the output voltage will compare the currents of both branches of the monitor. Assuming equal transistor sizes, *M5* and *M8*, the switching point ($V_{out1} = V_{out2}$) will occur when:

$$I_5 = I_8 \tag{1}$$

where I_i denotes the current of transistor M_i, in Figure 2.

Using Kirchorff's law in the output nodes:

$$\begin{aligned} I_5 &= I_1 + I_2 - I_7 \\ I_8 &= I_3 + I_4 - I_6 \end{aligned} \tag{2}$$

due to the current mirroring of transistors (*M6, M5*) and (*M7, M8*) with a β ratio of their widths (0.9 in this design):

$$\begin{aligned} I_6 &= \beta I_5 \\ I_7 &= \beta I_8 \end{aligned} \tag{3}$$

Combining (1) with expressions (2) and (3):

$$(I_1 + I_2) - (I_3 + I_4) = (I_5 + \beta I_8) - (I_8 + \beta I_5) = 0 \tag{4}$$

From where we get,

$$I_1 + I_2 = I_3 + I_4 \tag{5}$$

In order to perform the current comparison analysis between both branches, the unified MOSFET model is used [13].

$$I_D = K\left(V_{GT}V_{MIN} - \frac{V_{MIN}^2}{2}\right)(1 + \lambda V_{DS}) \tag{6}$$

Where K is the product of the process transconductance and the MOS aspect ratio, V_{GT} stands for the difference, ($V_{GS} - V_{TH}$) being V_{TH} the threshold voltage. V_{MIN} is defined as:

$$V_{MIN} = \min\{V_{GT}, V_{DS}, V_{DSAT}\} \tag{7}$$

In the condition (5) and assuming all transistors working in saturation, the previous model takes the form,

$$I_D = \frac{K}{2}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{8}$$

The gate-source voltage V_{GS}, is related with the input signal V_i in the way, $V_{GS} = V_i$, then

$$I_i = \frac{K_i}{2}(V_i - V_{THi})^2(1 + \lambda V_{DS}) \tag{9}$$

Combining (5) and (9) we obtain the commutation points that define the control line. Now, we consider four different transistor sizes, $K_1 \neq K_2 \neq K_3 \neq K_4$, identical threshold voltage $V_{TH1} = V_{TH2} = V_{TH3} = V_{TH4} = V_{THn}$, and constant parameter λ. As a result, we obtain a theoretical simplified expression for the current comparator as a function of the four input voltages:

$$K_1(V_1 - V_{THn})^2 + K_2(V_2 - V_{THn})^2 = K_3(V_3 - V_{THn})^2 + K_4(V_4 - V_{THn})^2 \tag{10}$$

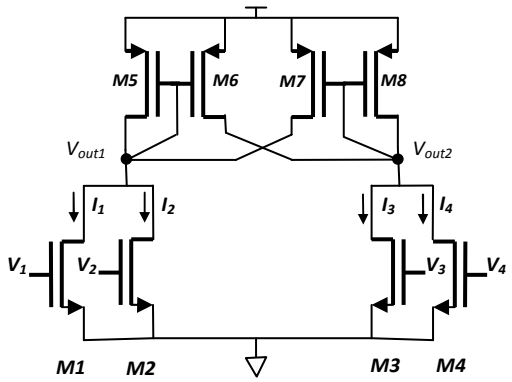

Figure 2. Four input current addition stage

The combination of transistor sizes with an adequate selection of input voltages allows controlling the position and shape of the control lines on the X-Y plane.

B. Curvature and position Control

To implement curves with different slopes and curvature in different positions of the X-Y plane two input voltages can act as the composed X-Y signals while the other two inputs act as positioning control signals. If the two composed signals are at the same side in (10) (V_1, V_2 or V_3, V_4), and the other two inputs are constant DC voltages, the curve has the general form:

$$a(x-h)^2 + b(y-h)^2 - c = 0 \qquad (11)$$

which is the equation of an ellipse centered in (*h, h);* in our case *(V_{THn}, V_{THn})*.

If the two composed signals are in opposite sides of the equality in (10) (V_1, V_3 / V_1, V_4 / V_2, V_3 or V_2, V_4 pairs), a hyperbola centered in (*h, h)* is obtained:

$$a(x-h)^2 - b(y-h)^2 - c = 0 \qquad (12)$$

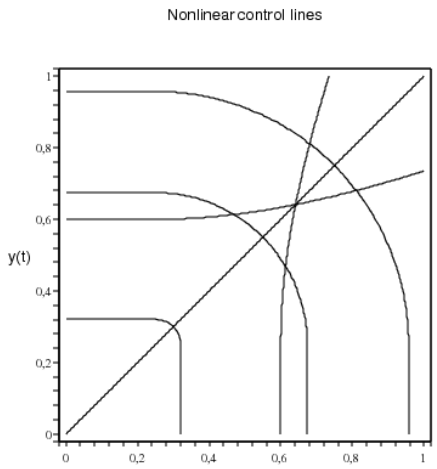

Figure 3. Mathematical model control lines for different parameters

In Figure 3 several theoretical ellipse and hyperbola segments are presented in the X-Y plane.

III. SIGNATURE GENERATOR IMPLEMENTATION

In order to implement the current comparison based monitor, with single ended digital output, we propose a circuit with the input stage shown in Figure 2 followed by the output stage circuit of Figure 4.

A. Monitor input stage

Based on the structure and analysis previously presented, this section is devoted to the generation of non linear control lines implemented in a 65nm CMOS technology. The position and shape of the control line is selected by choosing the input transistors and adequately sizing the input transistor dimensions (*W/L*). To maintain the balance of the active load, PMOS transistors, *M5* and *M8,* are equal sized transistors as well as *M6* and *M7*. In our design $W_{M6} = \beta W_{M5}$ and $W_{M7} = \beta W_{M8}$ with a width ratio of β =0.9. This feedback will improve the gain of the stage with no disturbance in the expected curves.

Table I summarizes the specific monitor configuration which defines de curves: transistor dimensions, applied (*x*, *y*) input signals and constant voltages at each comparator input. The sequence of digital outputs of the monitor generates the digital signature of the CUT.

B. Monitor Output stage

The output stage of the Monitor is a differential amplifier with single-ended output that digitalizes the differential output of the input stage. The main desired characteristics are simplicity, speed and wide common mode input range, thus, a simple sense amplifier structure has been chosen for the design. Three identical stages perform the final comparator function [14] as shown in Figure 4b.

The crossed inputs at the two first stages unbalance the voltage seen by the third stage which properly performs the comparison. The three modules are identical. Aspect ratio is 2000nm/180nm for the PMOS transistors and 1800nm/180nm for the NMOS ones.

The layout of the proposed signature generator implemented in STMicroelectronics 65nm-CMOS technology is depicted in Figure 5. In order to minimize mismatch effects, everyone transistor in Figure 2 has been split in four to balance the structure following two-dimension common-centroide design strategies [17]. According to the layout of Figure 5, distributions of NMOS and PMOS transistors are:

M1 M1 M4 M4	*M8 M8 M5 M5*
M3 M3 M2 M2	*M6 M6 M7 M7*
M2 M2 M3 M3	*M7 M7 M6 M6*
M4 M4 M1 M1	*M5 M5 M8 M8*

The area for the input stage is 53.54 μm^2 (11.64 µm × 4.6 µm) and for the output stage, 62.57 μm^2 (8.32 µm × 7.52 µm), summing a total of 116.1 μm^2 per monitor.

TABLE. 1. Input stage transistor dimensions W (nm) and applied voltages (V) for the curves depicted in Figure 6. All transistors with L=180 nm

	Transistor dimensions W/L (nm/180nm)				Applied input voltages (V)			
CURVE	M1	M2	M3	M4	V1	V2	V3	V4
1	3000	600	600	3000	Y axis	0.2	X axis	0.6
2	3000	600	600	3000	0.6	Y axis	0.2	X axis
3	1800	1800	1800	1800	Y axis	X axis	0.55	0.55
4	1800	1800	1800	1800	Y axis	X axis	0.3	0.3
5	1800	1800	1800	1800	Y axis	X axis	0.75	0.75
6	1800	1800	1800	1800	Y axis	0.5	X axis	0.5

.

C. *Simulation results*

As can be observed in Table I, changing the positions of the four input voltages, modifies curve shape and position. Figure 6 shows the layout simulation results of curves in Table I.

Comparing V_1 and V_3 voltages (one signal in each side of the differential pair) and setting V_2 and V_4 to a DC level, the resulting curves are segments of hyperboles (curves 1 and 2 of Figure 6). If both sides are symmetrical (transistor aspect ratio and constant voltages) we obtain a degenerated hyperbole that becomes a straight line cutting the plane at 45 degrees (curve 6 in Figure 6).

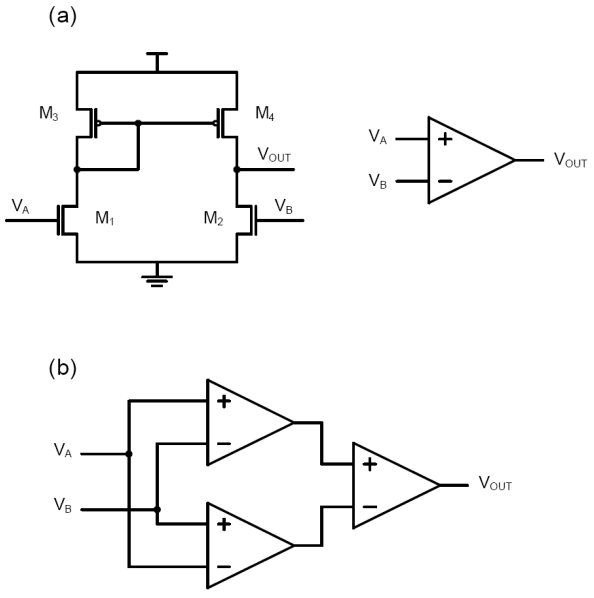

Figure.4 Output stage (a) One stage schematic and symbol (b) wiring of the three stages

On the other hand, we use both voltages in one branch of the differential pair (V_3, V_4), to control the line position, connecting two DC levels. With this configuration the quadratic addition of V_1 and V_2 happens and segments of ellipses are obtained as can be seen in curves 3 to 5, for different DC input voltages. Ellipses become a straight line for V_1 voltages below threshold voltage because M_1 transistor does not deliver current to the addition. Symmetrical straight line appears when V_2 voltage is below V_{TH}, then the ellipsis (curves 3 to 5) end with a straight line when reaching each axis.

Simulation results agree with the expected curves obtained through the mathematical model presented in Section II, considering the transistors working in saturation for the entire common mode range. Actual common mode input range is reduced by the V_{TH} of the input transistors. Below this voltage, *Mi* transistors enter the subthreshold region and, even

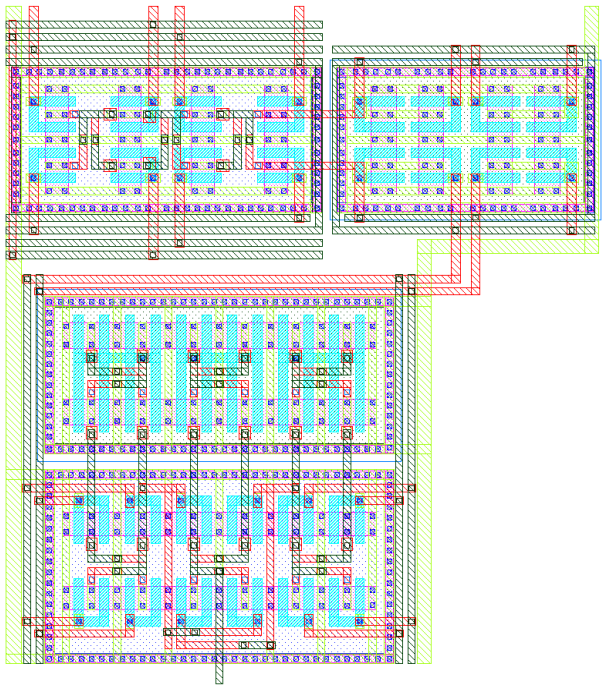

Figure 5. Digital Signature Generator Layout

though subthreshold currents are properly compared with the expected DC results, transient analysis reflects reduced timing parameters.

In the case study presented in Figure 6 with the monitor configurations in Table I we need six monitors one for each control line. Only two types of monitor circuit sizes are needed in order to cover the X-Y plane: One monitor with all four input transistor dimensions set to 1800nm/180nm (W/L); the second monitor with two transistors set to 600nm/180nm while the rest are 3000nm/180nm. Because the relation 600+3000 equals 1800+1800 the same load transistors (*M5, M6, M7 and M8*) are required.

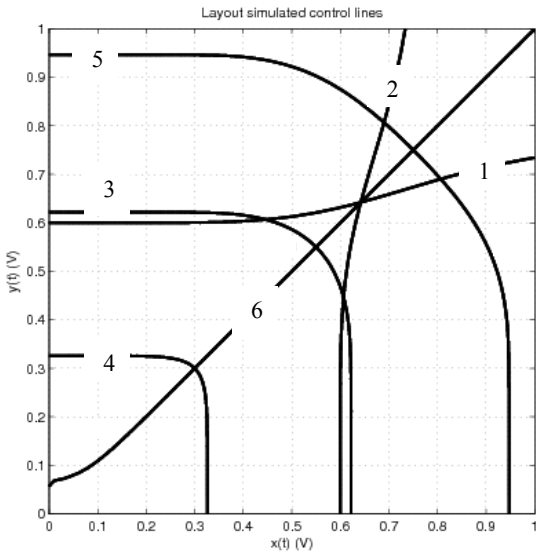

Figure 6. Layout simulated control lines of Table I.

D. Signature generation

The use of the proposed method for testing or parameter validation requires the use of several monitors, one for each curve cutting the X-Y plane. Depending on the Lissajous curve to be monitored the designer develops the adequate zones in the X-Y plane and then the specific monitors. The output of the monitors, sampled asynchronously during the evolution of the Lissajous cycle, represent the digital signature of the circuit. Using as example the control curves of Figure 6 combined with the nominal and the 10% parameter shift Lissajous curves of Figure 1 we obtain the composition represented graphically in Figure 7. The zones are codified in such a way that every monitor codifies a digital "1" when Lissajous curve is above the control line, or digital "0" when Lissajous curve is bellow the boundary. The outputs of the monitors processed by an asynchronous sampler, as indicated in Figure 8, deliver the periodic signatures shown in Table 2.

Due to the shape change of the Lissajous curve, and its position in the X-Y plane, in this example, there is a difference in the sequence length of the periodic output, as well as the zone codes reflecting different zone crossings.

The use of regression techniques as used in [9] will solve, in a general case, the mapping between measured signal (digital signature) and circuit parameter sets.

TABLE. 2. Digital Signatures of nominal and 10% natural frequency parametric variation in the case study of Figure 1 and Figure 6 for one period of the Lissajous curve.

Nominal
101010
101011
101111
101101
101111
101110
001110
001100
001000
001010
000010
100010
101010
101011
101111
101101
001101
001100
001000
001010

10% shift
101010
101011
101111
101101
001101
001100
001000
001010
101010
101011
101111
101101
101111
101110
001110
001100
001000
001010

IV. CONCLUSIONS

A low cost X-Y zoning Digital Signature generator has been proposed, based on a current comparator input stage followed by a differential voltage comparator output stage. The proposal converts the output differences of the input stage into binary signals used as digital signature of the monitor.

With a simple design, splitting the transistors of the input stage, only two different circuits are needed to cover adequately the X-Y plane. Zone boundaries are set by changing the input DC biasing voltages and/or the aspect ratio of the input transistors. Every monitor requires only 8 transistors for the input stage and 12 transistors for the digital output stage. The monitor area overhead is limited to 116,1 μm^2 which is an important reduction over voltage comparison alternatives. The loading on each monitored signals is limited to the capacitive load of the NMOS input transistors. With these monitors and fixed input biasing voltages the X-Y plane is partitioned into zones with non linear boundaries allowing effective monitoring of the Lissajous curves. The sequence of digital outputs of the monitor during one period of the Lissajous curve constitutes the digital signature of the CUT.

ACKNOWLEDGEMENTS

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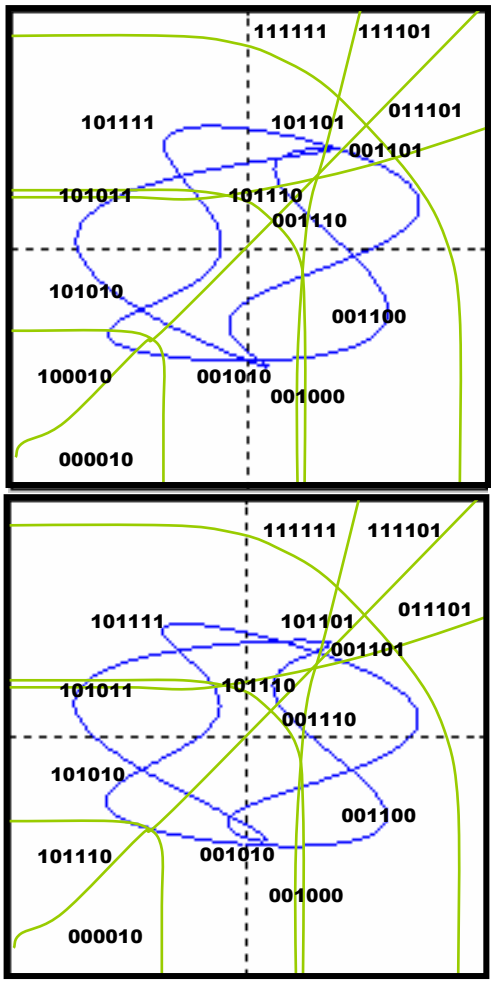

Figure 7 Lissajous curves evolving through control lines represented in Figure 6. Top curve represents the composition of multitone input voltage and nominal Low Pass output of a Biquad filter. Bottom curve is the same composition with a 10% parametric variation in the nominal frequency of the filter.

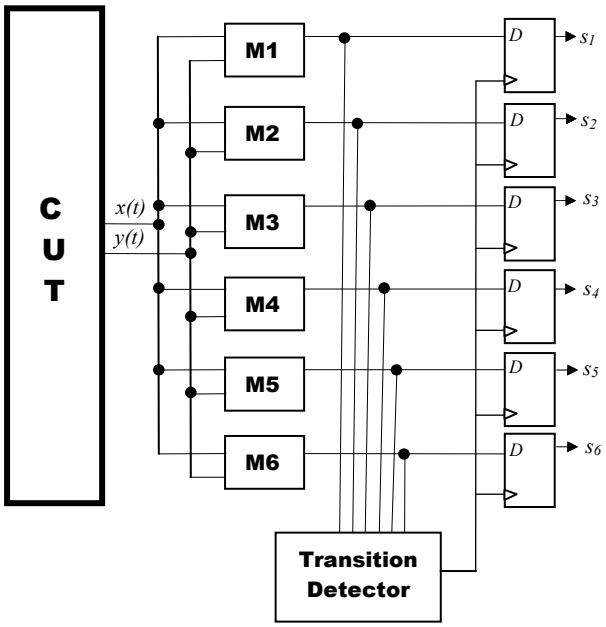

Figure 8. Asynchronous sampling of Digital signatures of the example in Figure 7

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