Digital Repetitive Control of a Three-Phase Four-Wire Shunt Active Filter

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***Abstract*—Shunt active power filters have been proved as useful elements to correct distorted currents caused by nonlinear loads in power distribution systems. This paper presents an all-digital approach based on a particular repetitive control technique for their control. Specifically, a digital repetitive plug-in controller for odd-harmonic discrete-time periodic references and disturbances is used for the current control loops of the active filter. This approach does not introduce a high gain at those frequencies for which it is not needed and, thus, improves robustness of the controlled system. The active power balance of the whole system is assured by an outer control loop, which is designed from an energy-balancing perspective. The design is performed for a three-phase four-wire shunt active filter with a full-bridge boost topology. Several experimental results are also presented to show the good behavior of the closed-loop system.**

***Index Terms*—Active power filters, digital repetitive control, three-phase four-wire power distribution systems, unbalanced systems.**

I. Introduction

ELECTRICAL power quality has been, in recent years, an important and growing problem because of the proliferation of nonlinear loads such as power electronic converters in typical power distribution systems. Particularly, voltage harmonics and power distribution equipment problems result from current harmonics produced by nonlinear loads. This fact has led to the proposal of more stringent requirements regarding power quality like those specifically collected in the standards IEC-61000-3-{2,4} and IEEE-519.

Much work has been done in the area of active filter control [1]–[7]. Nevertheless, it seems that, as a conclusion, the main point is the need for high-gain current control loops [2], [5], [7]. Perhaps, the easiest way to obtain them is to use some kind of hysteresis controller (or relay controller) [8]. However, this controller has the disadvantage of a varying switching frequency, which produces a continuous harmonic spectrum. This problem is not present in fixed-frequency pulsewidth-modulated schemes that have their high-frequency content around switching frequency harmonics. Therefore, it would be interesting to develop digital controllers with pulsewidth modulators (PWMs) for the active filter system. Fulfilling these requirements, there is a technique, called repetitive control, that allows control loops to be designed with a high gain at the harmonic frequencies of a fundamental one. This methodology arose from the Internal Model Principle (IMP) [5], [9] in control theory and is particularly suitable for periodic-signal tracking problems and periodic-signal disturbance rejection problems. Therefore, the necessary high-gain requirements of current control loops in active filters can be met with this approach. Particularly, this paper uses the repetitive control technique to design high-gain digital controllers for the current loops of the three-phase four-wire active filter.

The repetitive control concept and technique has been largely used in different control areas such as compact disk and hard disk arm actuators [10], [11], robotics [12], electro-hydraulics [13], torque vibration suppression in motor control [14] and power electronics applications like, for example, unity power factor rectifiers [15], pulsewidth-modulated inverters [16]–[19] and uninterruptible power supply (UPS) systems [20].

Normally, in power electronic systems, the reference and disturbance signals appearing in control loops (in this case, source and load currents, respectively) are, in steady state, periodic signals with only odd harmonics in their Fourier series expansion. If the usual repetitive control methodology is used in these systems, the open-loop transfer function includes a high gain in all the harmonic frequencies [21]. However, it is not necessary to include a high gain at even-harmonic frequencies; it only means a waste of control effort and a reduction of system robustness without improving system performance. Besides, the introduction of a high gain at even-harmonic frequencies generally implies that the open-loop transfer function includes an integral term that corresponds to zero frequency harmonic. This fact, together with the inclusion of sensors that use transformers[1] in the loop, gives closed loops that are not internally stable. Hence, traditional repetitive controllers must be precluded in systems with pure derivative terms in order to obtain internally stable closed-loop systems.

This paper designs and implements odd-harmonic digital repetitive current controllers [22] for a three-phase shunt active filter that only introduces a high gain where it is needed, i.e., at odd-harmonic frequencies. Furthermore, an outer voltage control loop that assures the active power balance of the whole system is designed from an energy-balancing point of view, and the zero dynamics of the system is characterized. It is important to emphasize that the designed control architecture

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[1]The dynamic model of the transformer has a pure derivative term, i.e., a transmission zero in $s = 0$.

only uses three sensors for source currents, unlike the usual control schemes that double this number, sensing the load currents and the active filter input currents. Then, the task of the current loops is to maintain sinusoidal-shape source currents in phase with the line-to-neutral voltages in spite of the corresponding load currents. From a control theory point of view, this approach matches a disturbance attenuation problem, and from this perspective, the current controllers are designed using the aforementioned linear control design technique. In addition, the computational cost of the overall controller is reduced in front of the usual six current sensors architecture because the proposed controller structure does not need a load current analysis module.

This paper is organized as follows. Section II introduces the problem, the control objectives, and the model of the system. Section III shows the multiloop controller design with the underlying theoretical aspects and the steady-state analysis. Section IV describes the experimental setup and gives some implementation issues. Section V presents some selected experimental results that show the good behavior of the whole system. Finally, Section VI summarizes the results of this paper.

II. Problem Formulation

A. Physical Model of the Boost Converter

Fig. 1 presents the complete system architecture. A three-phase mixed linear and nonlinear load is connected to the power source; in parallel, a three-phase four-wire active filter is applied in order to fulfill the desired behavior, i.e., to guarantee a unity power factor and a three-phase balanced current set in the network side. A three-leg boost converter with an ac neutral wire connected directly to the midpoint of the dc-bus is used as the active filter. The averaged (at the switching frequency) model of the boost converter is given by

$$L_k \frac{di_{f,k}}{dt} = -r_{L,k} i_{f,k} - v_1 d_k - v_2(d_k - 1) + v_{s,k} \quad (1)$$

$$C_1 \frac{dv_1}{dt} = -r_{C,1} v_1 + \sum_k i_{f,k} d_k \quad (2)$$

$$C_2 \frac{dv_2}{dt} = -r_{C,2} v_2 + \sum_k i_{f,k} (d_k - 1) \quad (3)$$

where d_k is the duty ratio of the k-phase,[2] $i_{f,k}$ are the inductor currents, v_1 and v_2 are the dc capacitor voltages, $v_{s,k} = V_s\sqrt{2}\sin(\omega_r t + \phi_k)$ are the voltage sources that represent the three-phase ac-line source with $\phi_a = 0$, $\phi_b = -2\pi/3$, and $\phi_c = -4\pi/3$, L_k are the converter inductors, $r_{L,k}$ are the inductor parasitic resistances, C_1 and C_2 are the converter capacitors, and $r_{C,1}$ and $r_{C,2}$ are the parasitic resistances of the capacitors. The control variables d_k take their values in the closed real interval [0, 1] and represent the averaged value of the pulsewidth-modulated control signal injected to the actual system.

[2] $k \in \{a, b, c\}$.

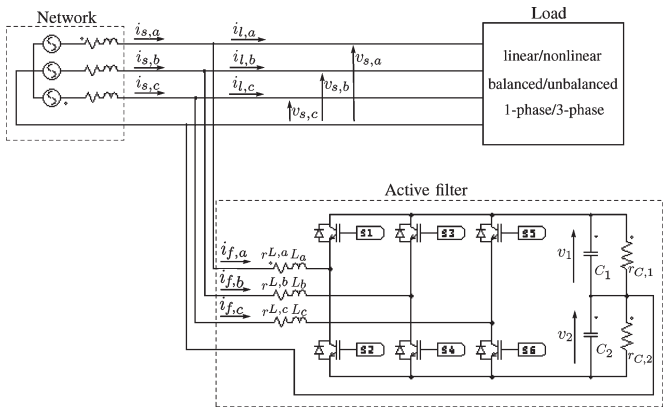

Fig. 1. Three-phase four-wire parallel active filter connected to the network-load system.

B. Load Description

The load current, in steady state, is usually a periodic signal with only odd harmonics in its Fourier series expansion, so the current in each phase can be written as

$$i_{l,k} = \sum_n a_{n,k} \sin(\omega_r(2 \cdot n + 1)t + \phi_k) + b_{n,k} \cos(\omega_r(2 \cdot n + 1)t + \phi_k) \quad (4)$$

where $a_{n,k}, b_{n,k} \in \mathbb{R}$ are the real Fourier series coefficients of the k-phase current.[3]

C. Control Objectives

The active filter goals are to assure that the load is seen as a resistive one and to balance the load current set. These goals can be stated[4] as $i^*_{s,k} = I^*_d \sin(\omega_r t + \phi_k)$, i.e., all the source currents have a sinusoidal shape in phase with the corresponding line-to-neutral voltage and the same amplitude. Another collateral goal that is necessary for a correct operation of the converter is to assure a constant average value of the dc-bus voltage,[5] i.e., $\langle v_1 + v_2 \rangle^*_0 = V_d$, where V_d must fulfill the boost condition. It would also be desirable that this voltage would be almost equally distributed among both capacitors ($v_1 \approx v_2$).

These two objectives define a nonstandard control problem: the second one is a regulation objective for the mean value of $v_1 + v_2$, but the first one is not a tracking specification because only a shape and not a signal is defined, that is, I^*_d is not known *a priori*, and it must take the adequate value to maintain the power balance of the whole system. This special form of the problem specifications implies the particular structure of the controller loops described in the next section.

D. Rewriting the Equations

It is a standard for this kind of systems to linearize the current dynamics by the state feedback $\alpha_k = v_1 d_k + v_2(d_k - 1)$.

[3] In a balanced load, $a_{n,k} = a_{n,j}$ and $b_{n,k} = b_{n,j}$ $\forall k \neq j$; $k, j \in \{a, b, c\}$.

[4] x^* represents the steady-state value of signal $x(t)$.

[5] $\langle x \rangle_0$ means the dc value, or mean value, of signal $x(t)$.

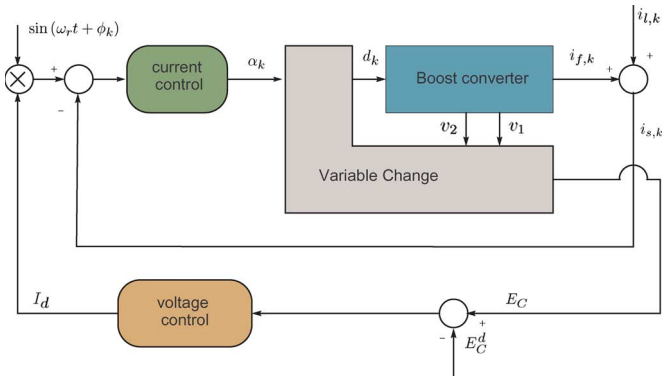

Fig. 2. Controller scheme showing one of the current control loops (inner) and the voltage (or energy) control loop (outer).

Moreover, the change of variables $i_{f,k} = i_{f,k}$, $E_C = 1/2(C_1 v_1^2 + C_2 v_2^2)$, $D = C_1 v_1 - C_2 v_2$ yields two more meaningful variables, namely: E_C, which is the energy stored in the converter capacitors, and D, which is the charge unbalance between them. Assuming that the two dc-bus capacitors are equal ($C = C_1 = C_2, r_C = r_{C,1} = r_{C,2}$), the system dynamics in the new variables results in

$$L_k \frac{di_{f,k}}{dt} = -r_{L,k} i_{f,k} + v_{s,k} - \alpha_k \tag{5}$$

$$\frac{dE_c}{dt} = -\frac{2r_C E_c}{C} + \frac{1}{C}\sum_k i_{f,k}\alpha_k \tag{6}$$

$$\frac{dD}{dt} = -\frac{r_C}{C} D + \frac{1}{C}\sum_k i_{f,k}. \tag{7}$$

It is important to note that the state feedback, together with the change of variables, results in a state and input diffeomorphism, provided that $v_1 + v_2 \neq 0$. In addition, (7) is also linear. Taking benefit from the fact that current equations (5) are linear and decoupled, a linear controller is designed for each one to force a sinusoidal shape in the network current (see Fig. 2). The sine-wave amplitude is given by an outer digital control loop to fulfill the appropriate active power balance for the whole system. This balance is achieved if the energy[6] stored in the active filter capacitors E_c is equal to its reference value E_c^d. The full control scheme for one phase current is depicted in Fig. 2. The specific controller designs will be presented in Sections III-A and B. It is worth remarking that, under the fulfillment of current specifications, (7) is decoupled as well. The corresponding zero dynamics is studied in Section III-C.

III. Control Design

A. Current Loop

The dynamics of (5) can also be described by

$$G_p(s) = \frac{Y_k(s)}{\alpha_k(s)} = \frac{-1/r}{\frac{L}{r}s + 1}. \tag{8}$$

[6]A similar reasoning can be done with the dc-bus capacitor voltages, as it is implied by the change of the variables used.

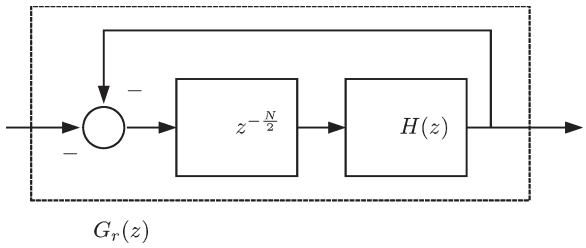

Fig. 3. Basic block diagram of the digital repetitive control loop.

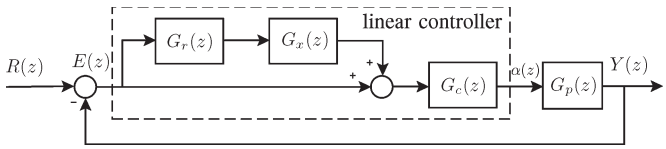

Fig. 4. Digital repetitive current control loop.

This continuous-time transfer function is sampled with a zero-order hold at a sampling frequency equal to the switching frequency of the converter giving, as a result, $G_p(z)$, and then this function is taken as a plant for the digital current controller design, as can be seen in Fig. 4. An odd-harmonic digital repetitive controller [22] is designed for tracking and disturbance rejection purposes.

Odd-harmonic repetitive control consists of placing a basic block (internal model) into the loop (Fig. 3), which introduces an infinite gain at a certain frequency and all its odd harmonics. This basic block is used as a basis to feed back a delay of $N/2 \in \mathbb{N}$ sampling periods, where $N = T_r/T_s$, T_r is the period of the periodic signal to be tracked or rejected, and T_s is the sampling period. It can be proven that this internal model has poles at the fundamental frequency and at its odd-harmonic frequencies [22].

Repetitive controllers are usually implemented in a "plug-in" fashion, i.e., the repetitive compensator is used to augment an existing nominal controller $G_c(z)$ (Fig. 4). This nominal compensator is designed to stabilize the plant $G_p(z)$ and provides disturbance attenuation across a broad frequency spectrum. This scheme was first introduced by Inoue *et al.* [23]. The controller is composed of the internal model and a linear system $G_x(z)$, which is designed to ensure closed-loop stability. In practical implementations, a null-phase finite-impulse response (FIR) low-pass filter $H(z)$ is introduced into the basic block in order to reduce the gain at those frequencies where system behavior is not properly modeled (Fig. 3). It is important to emphasize that the FIR filter $H(z)$ reduces the repetitive loop gain to finite values for all the frequencies, giving it a general low-pass shape.

The closed-loop system of Fig. 4 is stable if the following conditions are fulfilled [22].

1) The closed-loop system without the repetitive controller is stable, i.e., $G_o(z) = G_c(z)G_p(z)/(1 + G_c(z)G_p(z))$ is stable.
2) $\|H(z)\|_\infty < 1$.
3) $\|1 - G_o(z)G_x(z)\|_\infty < 1$, where G_x is a design filter to be chosen.

These conditions are fulfilled by a proper design of $G_c(z)$ and $G_x(z)$, which is described as follows.

- *Condition 1:* It is advisable to design the controller $G_c(z)$ with a high-enough robustness margin.
- *Condition 2:* There is no problem with the causality of $H(z)$ because it is series connected with the delay $z^{-N/2}$ and the repetitive loop will be executed as a whole in a controller real-time operation.
- *Condition 3:* A trivial structure that is often used is [24] $G_x(z) = k_r G_o(z)^{-1}$. This structure can only be used if G_o is a minimum-phase transfer function. Otherwise, other techniques should be applied in order to avoid closed-RHS plane zero–pole cancellations [24]. Moreover, as said before, there is no problem with the no causality of $G_x(z)$.

  As argued in [25], k_r must be designed while looking for a tradeoff between robustness and transient response.

B. Energy Shaping (Voltage Loop)

Without taking into account the active filter losses, all the power obtained from the net is due to load requirements, and under this ideal assumption, the following constraint holds:

$$P_{\text{net}} = \sum_k I_d \sqrt{2} V_s \sin^2(\omega_r t + \phi_k) = \sum_k v_{s,k} i^{l,k} = P_{\text{load}}. \tag{9}$$

However, as I_d is designed locally constant in order to fulfill the harmonic requirements, it is not possible to satisfy this requirement instantaneously. What can be achieved is an energy compensation within one period

$$\int_{t-T_r}^{t} P_{\text{net}} = \int_{t-T_r}^{t} P_{\text{load}} \tag{10}$$

that yields the I_d ideal value.

From the power flow point of view, the converter redistributes the power flow within one period in order to assure the stated power balance. Hence, the total energy stored in the converter (E_T) does not suffer variations within a period, i.e.,

$$\int_{t-T_r}^{t} \dot{E}_T = 0. \tag{11}$$

The stored energy in the converter can be decomposed into the energy stored in the inductors $(E_L = \sum_k (1/2) L_k (i_{f,k})^2)$ and the energy stored in the capacitors (E_c). Additionally, it is important to note that some energy is lost in the parasitic resistors of the inductors and the capacitors.

Presuming the currents' steady state and discarding the parasitic resistance of the inductors and capacitors, it can be easily proven that independent of the value of I_d and the load currents, the variation of energy in the inductors in one period is zero. Thus,

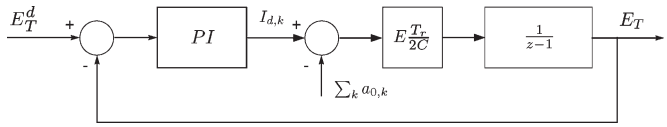

Fig. 5. Simplified 50-Hz model with a PI controller.

$$\int_{t-T_r}^{t} \dot{E}_T = \int_{t-T_r}^{t} \dot{E}_c. \tag{12}$$

Using (6) and (12) results in

$$\int_{t-T_r}^{t} \dot{E}_T = E_T(t) - E_T(t-T_r) = \sum_k \frac{\sqrt{2} V_s \pi (I_d - a_{0,k})}{\omega}.$$

This energy balance can be seen as a linear discrete-time system (with the sample time T_r) with an input I_d and a constant disturbance $a_{0,k}$, i.e.,

$$E_T(z) = \frac{1}{z-1} \frac{\sqrt{2} V_s \pi}{\omega} \left(3Id(z) - \sum_k a_{0,k} \right). \tag{13}$$

As the value of $a_{0,k}$ is usually unknown but constant in steady state, it can be considered as a step disturbance in the closed-loop system (see Fig. 5). Thus, a classical PI controller will regulate E_T to the desired value E_T^d without steady-state error, i.e.,

$$I_d(z) = \left(k_p + k_I \frac{z+1}{z-1} \right) \left(E_T^d(z) - E_T(z) \right). \tag{14}$$

The losses in the inductor and capacitor parasitic resistances can be considered as an additive complex-dynamics disturbance in the voltage closed-loop system. However, as the experimental results will show, it is not worth taking these losses into account in the design of the voltage loop.

It is important to note that, from (12), the control defined for E_T can be applied to E_c. From the practical point of view, this is of great relevance because E_c can be directly calculated by means of measuring the dc-bus voltage $(v^1 + v^2)$. If this assumption is used, the voltage loop design uses a steady-state condition in the current loop.

C. Zero Dynamics

In this section, the complete system zero dynamics is characterized while assuming that $i_{s,k} \simeq I_d^* \sin(\omega_r t + \phi_k)$.

The charge unbalance is described in (7). This equation is a linear differential equation with an unknown input $\sum_k i_{f,k}$. As $\gamma \stackrel{\triangle}{=} (r_C/C) > 0$, the system is stable, and if $\sum_k i_{f,k} = 0$

(balanced load), then it tends to zero in steady state. Otherwise, as the input is a periodic signal, the output is also periodic. Then,

$$D^*(t) = \frac{1}{C}\sum_k\sum_n -\frac{a_{n,k}}{\varsigma_n}\sin\left(\omega_r(2\cdot n+1)t+\phi_k+\delta_n\right) - \frac{b_{n,k}}{\varsigma_n}\cos\left(\omega_r(2\cdot n+1)t+\phi_k+\delta_n-\frac{\pi}{2}\right) \quad (15)$$

where $\varsigma_n = \sqrt{\gamma^2+((2\cdot n+1)\omega_r)^2}$, and $\delta_n \triangleq -\tan^{-1}(\gamma/(2\cdot n+1)\omega_r)$.

As ς_n increases with the frequency, and assuming that, as usual, higher harmonics have lower amplitudes than the ones near the fundamental, the contribution of these harmonics to the evolution of $D^*(t)$ may be neglected in most cases.

As a conclusion, in the particular case of balanced loads, D is identically zero due to the fact that load currents will compensate among them. Otherwise, D^* presents an intrinsic oscillatory behavior with a zero-mean value. If these intrinsic oscillations are seen from the voltage point of view, then it can also be seen that their amplitude is proportional to the capacitance inverse; thus, increasing the capacitance will reduce their amplitude.

The other important variable that should be analyzed is the energy stored in the capacitors (E_c); the evolution of this variable is described in (6). This equation describes a stable linear system with an exogenous input. This input is $i_{f,k}\cdot\alpha_k$, where $i^*_{f,k}$ is an odd-harmonic periodic signal, and it is easy to prove that α^*_k is also an odd-harmonic periodic signal. Consequently, $i^*_{f,k}\cdot\alpha^*_k$ will be an even-harmonic periodic signal. Hence, E^*_c will also be an even-harmonic periodic signal. These oscillations are the same ones as that in $i^*_{f,k}\cdot\alpha^*_k$ but are filtered by a first-order filter $1/s+2\gamma$.

The voltage loop (Section III-B) will assure that the first harmonic of these intrinsic oscillations will be regulated to the desired value (E^d_C). As a conclusion, E^*_C presents an intrinsic oscillatory behavior with a mean value that can be regulated by the energy (voltage) loop. Its amplitude, from the voltage point of view, is proportional to the inverse of the capacitance C; hence, the amplitude of the voltage oscillations can be reduced by increasing the capacitance.

IV. Experimental Setup and Implementation Issues

A. Experimental Setup

The experimental setup used to test the designed controller has the following parts:

1) *Active filter:* This is the full-bridge (three-legged) boost converter with insulated gate bipolar transistor (IGBT) switches (nominal current 100 A) and the following parameters: $r = 0.034\ \Omega$, $L_1 = L_2 = L_3 = 1$ mH, and $C_1 = C_2 = 6600\ \mu$F. The switching frequency of the converter is 20 kHz and a synchronous (regularly) centered-pulse single-update PWM strategy is used to map the controller's output to the IGBT gate signals.

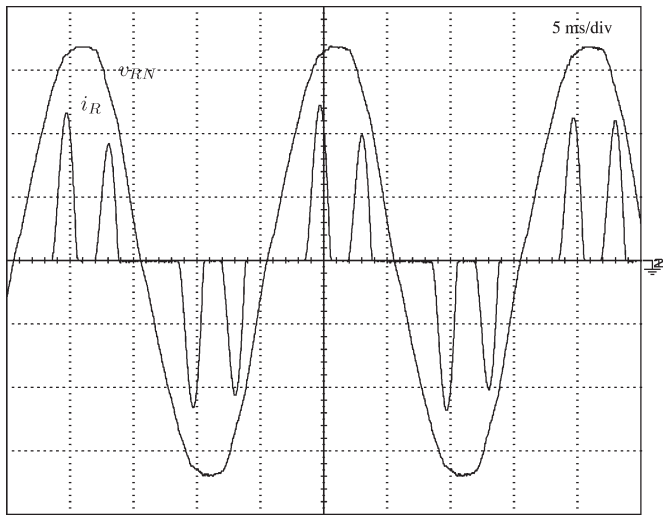

Fig. 6. Three-phase nonlinear load: mains voltage (phase R) and current from phase R (90 V/div and 12.5 A/div, respectively).

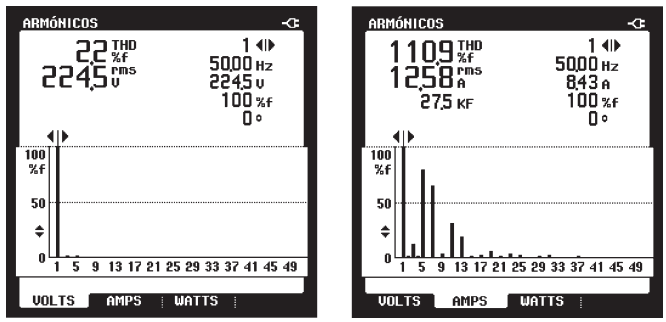

Fig. 7. Three-phase nonlinear load: mains voltage (phase R) and load current from phase R (rms and THD).

2) *Rectifier (nonlinear load):* This is the three-phase full-wave diode rectifier with $C = 1500\ \mu$F. The active power with nominal dc resistor is $P = 5.6$ kW, and its reactive power is approximately zero. The rectifier also includes three series inductors (0.2 mH) in its ac side to limit the derivative of its inputs currents. Fig. 6 shows the shape of the ac mains voltage and current for phase R, and Fig. 7 shows the harmonic content of the phase R ac mains line-to-neutral voltage and current for the rectifier with the nominal dc resistor. It is worth remarking that the total harmonic distortion[7] (THD) of this current is about 110%, and its maximum derivative is about 70 kA/s.
3) *Single-phase linear load:* The resistive load of 1.9 kW is connected between phase R and the neutral wires. It is used experimentally to unbalance the load and to make up a mixed load together with the three-phase nonlinear load.
4) *Analog circuitry of feedback channels:* The three ac mains line-to-neutral voltages, the three ac mains currents, and the dc-bus voltage are sensed with voltage transformers, Hall-effect sensors, and an isolation amplifier, respectively. All the signals from the sensors pass through the corresponding gain conditioning stages to

[7]In this paper, the THD figures and the harmonic content are always taken with respect to the fundamental harmonic (50 Hz), and they have been obtained using a Power Quality Analyzer Fluke 43 instrument.

adapt their values to an A/D converter input, taking advantage of their full dynamic range. In addition, all the feedback channels include a first-order low-pass filter with a unity dc gain and a 4.3-kHz cutoff frequency.[8]

5) *Control hardware and DSP implementation:* The control board has been internally developed and is based on an ADSP-21161 floating-point DSP processor with an ADSP-21990 fixed-point mixed-signal DSP processor that acts as coprocessor, both from Analog Devices. The DSP-21161 and the ADSP-21990 communicate with each other using a high-speed synchronous serial channel in the direct memory access mode. The ADSP-21990 deals with the three-phase PWM generation and the A/D conversions with its integrated eight 14-bit high-speed A/D channels.
6) *Voltage and frequency:* The nominal line-to-neutral voltage of the ac three-phase mains is $V_s = 220$ Vrms, and its nominal frequency is 50 Hz.

B. Implementation Issues

Some implementation issues that are worth remarking are listed as follows.

1) The sampling rate of the A/D channels and the current loop is $F_s = 20$ kHz, which is the same as the switching frequency of the active filter. Because the sampling rate of the ac mains voltages and currents is the same as the converter switching frequency, some aliasing problems can arise. Particularly, the switching ripple appears as a dc component on the discrete-time side (after A/D conversion). This fact has proved especially critical in ac mains line-to-neutral voltage sensing because these signals are used as the carrier signals in the controller. To solve this problem, the sampled ac voltages are passed through parametric equalizer filters that include a zero in $z = 1$ to reject, in steady state, the dc component of the signals. In the ac mains currents, the problem is not very important because the open-loop dc gain of the current loops is low, and the current loops are hardly affected by the fictitious current dc component.
2) The controller and its related code (communications, alarm supervision, data collection routines, etc.) are coded in the C programming language without an underlying real-time operating system. Only a few of the lowest level procedures are coded in assembler for efficiency reasons. The available computing power of the floating-point DSP processor allows the controller operations to be calculated in about two-thirds of the current loops' sampling period. Thus, it is only necessary to force one period of computing delay; in any case, this delay would be necessary due to the hardware PWM unit peculiarities. It is worth noting that the one-period computing delay has been included in the plant model $G_p(z)$ to take it into account in the current controller design process.
3) In this paper, the current loop plants $G_p(z)$ (one for each phase) have no zeros, and the designed controllers $G_c(z)$ are minimum-phase first-order lag controllers, specifically $G_c(z) = -[(0.0135z - 0.01)/(z - 0.905)]$. Then, the closed-loop functions $G_o(z)$ are minimum-phase functions, and there is no problem choosing $G_x(z) = k_r G_o(z)^{-1}$. The assigned value for k_r is 0.2, and the null-phase low-pass FIR filter selected is $H(z) = 1/4z + 1/2 + 1/4z^{-1}$. It is worth stressing that the digital repetitive current controller designed for one phase is repeated for the other two.
4) The outer dc-bus voltage (energy) control loop needs to feed back the dc-bus voltage sampled at 50 Hz. However, direct sampling of this signal at 50 Hz sampling rate is not a reliable option because of inherent noise and synchronization issues when the dc-bus voltage oscillates. Therefore, to alleviate this problem, the dc-bus voltage is sampled at a sampling rate of 20 kHz, and after that, it is passed through a comb filter tuned to the even-harmonic values of the fundamental frequency (with the exception of zero frequency). The output of the comb filter is decimated to a 50-Hz sampling rate, and after a low-order low-pass filtering, it is compared to the desired value to generate the error signal for the voltage (energy) loop controller.

V. Experimental Results

This section shows some of the experimental results obtained for the active filter operation with the designed all-digital controller. The results are presented by means of an oscilloscope and power analyzer screen dumps of the ac mains electrical variables and, when it is necessary, the active filter semibus dc voltages.

Apart from the selected experiments collected in this section, a lot of numerical simulations, including mainly capacitive or inductive loads, have been carried out, showing the same good performance as it will be shown later in this paper. Furthermore, it is worth noting that several numerical simulations, including loads that work as generators at some periods[9] (thus imposing a negative active power flow to the source), have been carried out without problems. The voltage loop of the overall controller assures the active power balance, and after a transient, in steady state, the inputs to the AM modulators are negative, giving current references shifted π rad from corresponding line-to-neutral voltages that the current loops track without difficulty.

A. Active Filter Operation With No Load

This section presents some results of the no-load operation of the active filter. Fig. 8 shows the line-to-neutral voltage and current for phase R. The rms value of the current is about 1 A, and its THD value is 6%. Then, the resulting active power consumed by the filter to cover its losses without compensating any load is about 720 W. It is worth noting that the fundamental component of the current is in phase with the voltage ($\cos\phi = 1$;

[8]The oscilloscope screens in the figures cited in this section and the following show the voltages and currents after the corresponding low-pass filters.

[9]This problem was established as a hard one by Depenbrock and Staudt [26].

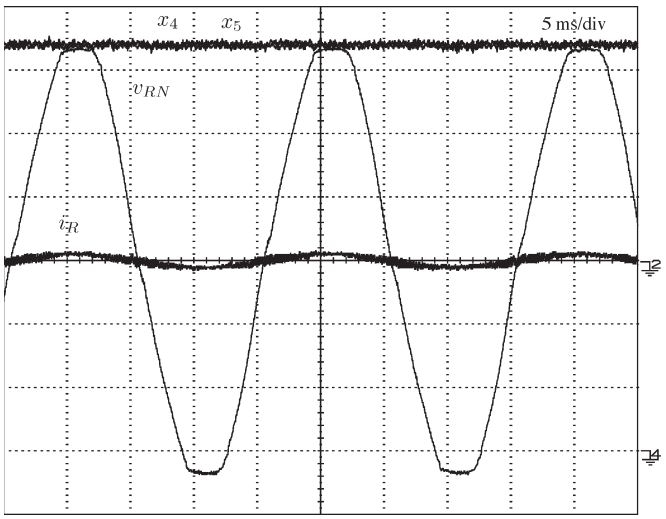

Fig. 8. Active filter with no load: mains voltage (phase R) (90 V/div), current from phase R (12.5 A/div) and semibus dc voltage (65 V/div), respectively.

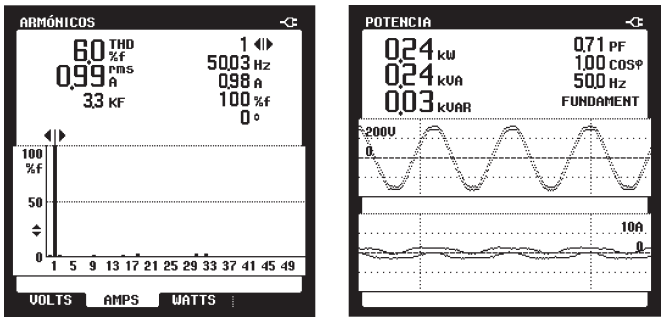

Fig. 9. Active filter with no load: rms and THD values of the mains current $i_R(t)$ and P, Q, $\cos\phi$, and PF for phase R.

see Fig. 9). Therefore, almost no reactive power is consumed by the filter. The low figure of the power factor (PF $= 0.71$) is owed to the high value of the switching ripple with respect to the fundamental component of the current.

B. Active Filter Operation With the Three-Phase Nonlinear Load

In this experiment, the three-phase diode rectifier described in Section IV-A is connected to the network. This nonlinear load is balanced and has no reactive power at the fundamental frequency; however, the active filter must work to compensate all the generated higher order harmonics. Fig. 10 shows the current for phase R, which appears with a good sinusoidal shape and in phase with the grid voltage. This figure also shows the values of each semibus of the active filter dc-bus. It is important to remark that there are no oscillation, aside from the switching ripple, in these variables because the load is a balanced one. As shown in Fig. 11, the THD of the current is very low (0.9%), and the power factor is very close to 1. Obviously, although not shown, the results for the other two phases (S and T) are quite similar, and the three currents form a balanced set in the grid side, thus giving a neutral current with only high-frequency components and very low rms values.

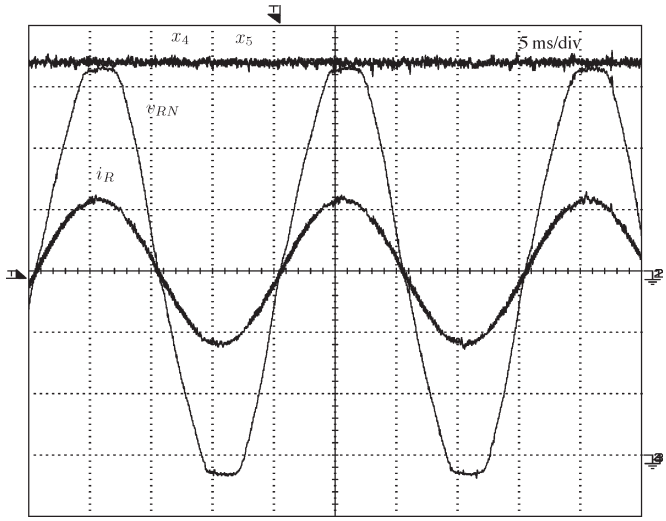

Fig. 10. Active filter with the three-phase nonlinear load: mains voltage (phase R) (90 V/div), current from phase R (12.5 A/div), and semibus dc voltages (65 V/div), respectively.

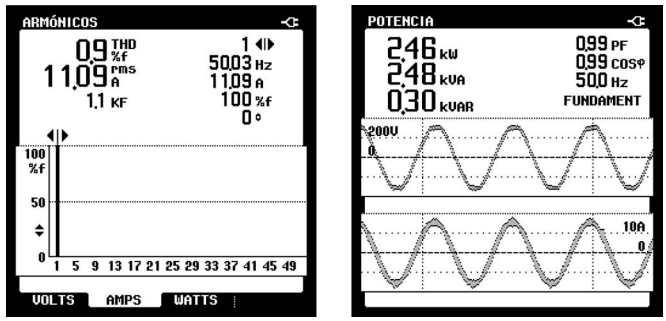

Fig. 11. Active filter with the three-phase nonlinear load: rms and THD values of the mains current $i_R(t)$ and P, Q, $\cos\phi$, and PF for phase R.

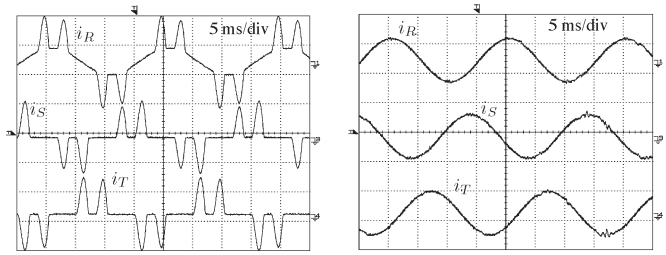

Fig. 12. Active filter with the three-phase nonlinear load plus a single-phase (R) resistive load: (left) $i_{R,\mathrm{load}}(t)$, $i_{S,\mathrm{load}}(t)$, $i_{T,\mathrm{load}}(t)$ and (right) $i_{R,\mathrm{source}}(t)$, $i_{S,\mathrm{source}}(t)$, $i_{T,\mathrm{source}}(t)$ (12.5 A/div).

C. Active Filter Operation With the Three-Phase Nonlinear Load Plus a Single-Phase Resistive Load

In this case, the single-phase resistive load described in Section IV-A is connected between phase R and neutral wires to create and unbalanced mixed (linear and nonlinear) load. Fig. 12 (left) shows the three load currents that are clearly unbalanced. The figure on the right shows the three grid currents forming a sinusoidal balanced set.

Fig. 13 (left) details the phase R current, which is in phase with the corresponding line-to-neutral voltage and shows the

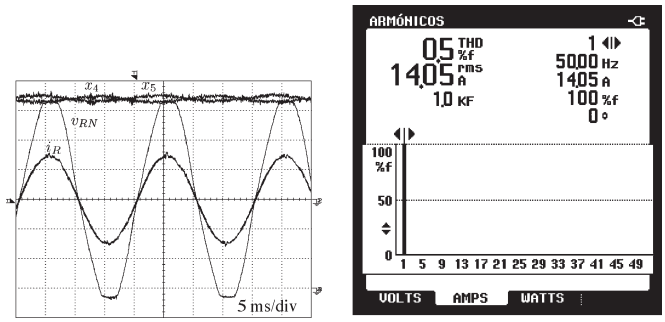

Fig. 13. Active filter with the three-phase nonlinear load plus a single-phase (R) resistive load: mains voltage (phase R) (90 V/div), current from phase R (12.5 A/div), and semibus dc voltages (65 V/div), respectively, and rms and THD values of the mains current $i_R(t)$.

semibus dc voltages. As theoretically predicted, these voltages present an intrinsic oscillatory behavior because of the unbalanced characteristic of the load to compensate. In the power analyzer screen dump of this figure, it can be observed that the phase R current THD is 0.5%, which is a very low value, thus confirming the sinusoidal shape of the current. The THD for the current has a lower value than that in Section V-B case due to the fact that its rms value is higher; hence, the current switching ripple is comparatively lower.

VI. Conclusion

This paper has shown the design and implementation of an all-digital linear controller for a three-phase four-wire current active filter. The controller consists of three inner current control loops and an outer dc-bus voltage control loop. The current references for the inner control loops are created, passing the output of the voltage controller through AM modulators that use as a carrier a filtered version of the corresponding line-to-neutral voltage. The inner current control loops that, as the experimental results show, perfectly shape the grid currents are designed using a digital repetitive control approach. The high loop gain injected by the repetitive controllers at the fundamental and harmonic frequencies of the network frequency guarantees good tracking of the reference current and rejection of the high-order harmonics of the load current. It is important to remark that, because the current sensors have been placed on the network side, the control problem for the current loops can be discussed from a disturbance rejection point of view. This approach allows for obtaining a controller with half the usual current sensors, thus reducing the hardware cost, and a lower computational cost due to the load current analysis module is unnecessary. In addition, the external slow dynamics voltage loop ensures the active power balance of the whole system, adequately rejecting the load variations and providing the inner current control loops with the correct current rms references.

The paper also discussed the steady-state behavior of the active filter in order to characterize the dc-bus voltage oscillations that appear during the controlled-system operation, especially under the unbalanced load condition. Additionally, some relevant practical implementation issues were commented upon, and a selection of the obtained experimental results was included, which shows that the closed-loop performance of the designed system is good, with low THD values for the network currents and a near-unity power factor at network terminals in front of linear and nonlinear, balanced or unbalanced, loads.

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