Sliding-Mode Control Design of a Boost–Buck Switching Converter for AC Signal Generation

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***Abstract*—This paper presents a sliding-mode control design of a boost–buck switching converter for a voltage step-up dc–ac conversion without the use of any transformer. This approach combines the step-up/step-down conversion ratio capability of the converter with the robustness properties of sliding-mode control. The proposed control strategy is based on the design of two sliding-control laws, one ensuring the control of a full-bridge buck converter for proper dc–ac conversion, and the other one the control a boost converter for guaranteeing a global dc-to-ac voltage step-up ratio. A set of design criteria and a complete design procedure of the sliding-control laws are derived from small-signal analysis and large-signal considerations. The experimental results presented in the paper evidence both the achievement of step-up dc–ac conversion with good accuracy and robustness in front of input voltage and load perturbations, thus validating the proposed approach.**

***Index Terms*—boost–buck switching converter, dc–ac step-up conversion, sliding-mode control.**

I. Introduction

UNINTERRUPTIBLE power supplies (UPS) or ac power sources constitute the most classical applications of power conditioning systems designed to supply an ac load from a dc source. The design of these systems involves the design of both a high-efficiency switching power stage circuit and a control subsystem in order to achieve a suitable dc–ac conversion in the desired output frequency range. Concerning the generated output voltage, low harmonic distortion, and robustness in front of input voltage and load perturbations (evaluated in terms of fast transient behavior and steady-state accuracy) are commonly requested features.

Usually, the power stage circuits in charge of performing the dc–ac conversion are based on a full-bridge buck switching converter topology. Regarding the control subsystem, several control schemes oriented to ensure a proper tracking of an external sinusoidal reference have been suggested. For instance, many tracking control techniques based on high-frequency pulsewidth modulation (PWM) have been proposed in the past for buck-based dc–ac converters [1]–[5]. However, these control strategies are designed by means of a power-stage model, thus leading to output waveforms being sensitive to power stage parameter variations, such as the output load. On the other hand, sliding-mode control techniques have been proposed as an alternative to PWM control strategies in dc–dc switching regulators since they make these systems highly robust to perturbations, namely variations of the input voltage and/or in the load [6]–[8]. Taking advantage of these properties, sliding-mode control has also been applied to the design of high-efficiency buck-based dc–ac converters, where a switching dc–dc converter is forced to track, by means of an appropriate sliding-mode control action, an external sinusoidal [12]–[18]. Nevertheless, the full-bridge buck converter topology limits the ac output voltage amplitude to values lower than the dc input voltage, except in the vicinity of the output filter resonant frequency [19].

When ac amplitudes higher than the dc input voltage are required, the classical design combines a step-up turns ratio transformer and a buck converter in the dc–ac conversion circuit. However, this approach entails some drawbacks related to the transformer nonidealities (leakage inductances, limited bandwidth,…) and increases the weight and size of the converter circuit. Alternatively, transformerless step-up conversion topologies could be considered. Nonetheless, although sliding-mode control has been successfully applied to switching dc–dc converters exhibiting a step-up voltage conversion ratio such as the boost converter [8], [22], the coupled-inductor Čuk converter [9] and the boost–buck converter [10], [11], preliminary studies have shown the analytical difficulties in applying sliding-mode control techniques to these power stages for a dc–ac step-up conversion ratio [20], [21].

In order to overcome the drawbacks exposed above, this work focuses on a sliding-mode control design for a cascade connection between a boost dc–dc converter with a full-bridge buck inverter, as a transformerless power stage for a dc–ac step-up conversion, this being referred as a boost–buck dc–ac converter. Starting from the sliding-control-law design proposed by Carpita *et al.* [12] for a full-bridge buck-based dc–ac conversion, the work here reported presents how a well-known linear sliding-control law for a single boost dc–dc converter has to be designed when the previous cascade connection conversion is considered. Therefore, by properly combining the step-up/step-down conversion ratio of the boost–buck dc–ac converter with the robustness properties of sliding-mode control, a step-up dc–ac voltage conversion robust in front of input voltage and/or load perturbations can be generated in a large frequency range without the use of any transformer.

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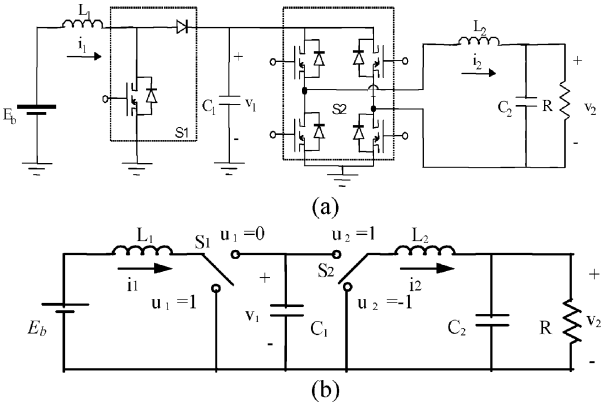


Fig. 1. (a) Cascade connection of a boost converter with a full-bridge buck inverter. (b) Circuit model.

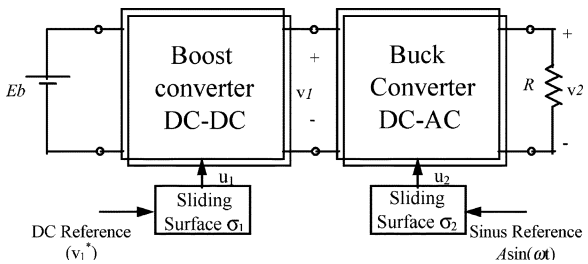


Fig. 2. Block diagram of a boost–buck dc–ac converter.

The paper is organized as follows. The next section presents the boost–buck dc–ac converter sliding-control strategy. Collecting the results of previous studies [12]–[19], Section III designs a sliding-control law of the buck stage, whereas Section IV focuses on a complete design procedure for the boost one. Finally, the last two sections present both simulation and experimental results validating the approach, and the conclusions of this work.

II. Boost–Buck Sliding-Control Strategy

Fig. 1(a) shows the boost–buck dc–ac converter circuit consisting in the cascade connection of a boost dc–dc converter with a full-bridge buck inverter. For analysis purposes, the converter can be represented by the circuit model shown in Fig. 1(b), where S1 is a conventional power switch and S2, corresponds to the full bridge switch to ensure the bipolarity of the ac output.

If u_1 and u_2 stand for the control signals of S1 and S2, respectively, the system can be represented by the following set of differential equations:

$$\begin{cases} L_1 \frac{di_1}{dt} = E_b - v_1 \cdot (1 - u_1) \\ C_1 \frac{dv_1}{dt} = i_1 \cdot (1 - u_1) - i_2 \cdot u_2 \\ L_2 \frac{di_2}{dt} = v_1 \cdot u_2 - v_2 \\ C_2 \frac{dv_2}{dt} = i_2 - \frac{v_2}{R} \end{cases} \tag{1}$$

where $u_1 \in \{0, 1\}$ and $u_2 \in \{-1, 1\}$. As shown in Fig. 2, this work considers the design of two sliding-mode control laws for the u_1 and u_2 variables.

Recalling the results of previous studies [10]–[17], a first sliding-control law will be designed to control the full bridge switch of the buck stage (control variable u_2) for tracking an external sinusoidal reference, thus providing a dc–ac conversion. A second law will be designed to control the dc–dc boost stage (control variable u_1) in order to set the intermediate voltage v_1 at a large enough value to ensure a global ac output voltage amplitude to dc input voltage step-up ratio.

The design of the sliding-control laws will be carried out by applying the equivalent control concept [6], [7]. This technique can be summarized in the following three steps for the case of one control variable u.

- The first step is the choice of a switching surface $\sigma(x, t) = 0$ (where x is the system state vector) that provides the desired asymptotic behavior.
- Obtaining the equivalent control u_{eq} by applying the invariance condition $(d\sigma/dt)\big|_{\substack{\sigma=0 \\ u=u_{\text{eq}}}} = 0$ constitutes the second step. The existence of the equivalent control u_{eq} assures the feasibility of a sliding motion over the switching surface $\sigma(x, t) = 0$. On the other hand, besides describing the averaged dynamic behavior of the power stage over the switching surface, the equivalent control enables obtaining the sliding domain, given by

$$\min\{u^-, u^+\} < u_{\text{eq}} < \max\{u^-, u^+\}$$

where u^- and u^+ are the control values for $\sigma < 0$ and $\sigma > 0$ respectively. The sliding domain is the state plane region where the sliding motion is ensured.
- Finally, the control law is obtained by guaranteeing the Lyapunov stability criteria, i.e., $d\sigma^2/dt < 0$.

According to the aforementioned three steps, the design procedure of the two sliding-control laws is given in the following sections.

III. DC–AC Buck Stage Sliding-Control Design

There are several works reported in the literature dealing with sliding control of buck-based dc–ac converters [12]–[19]. In order to track a user-defined sinusoidal voltage reference $V_{\text{ref}}(t) = A \cdot \sin(\omega t)$ at the buck stage output, i.e. $v_2 = V_{\text{ref}}(t)$, the following switching surface and the corresponding control law proposed by Carpita *et al.* [15] is adopted in this paper:

$$\sigma_2(v_2, t) = a_1 \cdot (V_{\text{ref}}(t) - v_2) + a_2 \cdot \left(\frac{dV_{\text{ref}}(t)}{dt} - \frac{dv_2}{dt} \right) \tag{2}$$

where $a_1 > 0$ and $a_2 > 0$ are the design parameters. The sliding motion over the switching surface is given by

$$\sigma_2(v_2, t) = 0 \Rightarrow v_2(t) = V_{\text{ref}}(t) + \mu \cdot e^{-a_1 \cdot t / a_2} \tag{3}$$

thus leading to the desired steady-state behavior. As (3) points out, the sliding-mode dynamic behavior depends on the a_2/a_1 time constant, which has to be as low as possible; however, as it is reported by the authors, if the time constant is too low, the state vector can leave the switching surface due to the bounds on control. A complete set of design considerations of these switching surface parameters can be found in [15].

The corresponding equivalent control resulting from the application of the invariance condition to $\sigma_2(v_2, t)$ is given by

$$\frac{d\sigma_2}{dt} = 0 \Rightarrow u_{2\text{eq}} = \frac{L_2C_2}{v_1}\left[\frac{a_1}{a_2}\left(\frac{dV_{\text{ref}}}{dt} - \frac{dv_2}{dt}\right) + \frac{d^2V_{\text{ref}}}{dt^2} + \frac{v_2}{L_2C_2} + \frac{1}{RC_2}\frac{dv_2}{dt}\right] \quad (4)$$

whereas the sliding domain can be obtained by imposing $\min\{u^-, u^+\} < u_{2\text{eq}} < \max\{u^-, u^+\}$, or equivalently

$$-1 < u_{2\text{eq}} < 1. \quad (5)$$

Finally, the power converter will reach the sliding surface if $d\sigma_2^2/dt < 0$, this leading to the following switching control law:

$$u_2 = \begin{cases} +1, & \text{if } \sigma_2 > 0 \\ -1, & \text{if } \sigma_2 < 0. \end{cases} \quad (6)$$

A. Steady-State Design Constraints

In the subsequent developments the sub-index "ss" stands for steady-state variables. In accordance to the sliding-mode control theory, if the sliding domain is preserved the previous control law will lead the buck stage to the desired steady-state sliding motion, where the following relation holds:

$$v_{2\text{ss}}(t) = V_{\text{ref}}(t) = A \cdot \sin(\omega t). \quad (7)$$

The design must evidently preserve the steady-state sliding domain of the buck power stage which can be deduced by restricting expressions (4) and (5) to the steady-state behavior given by (7). Accordingly, (4) can be written as

$$u_{2\text{eqss}} = \frac{L_2C_2}{v_{1\text{ss}}}\left[\frac{d^2V_{\text{ref}}}{dt^2} + \frac{1}{RC_2}\frac{dV_{\text{ref}}}{dt} + \frac{V_{\text{ref}}}{L_2C_2}\right]. \quad (8)$$

From (5), (7), and (8), it can be easily proved that the steady-state sliding domain of the buck power stage is given by [17]

$$-v_{1\text{ss}} < \frac{L_2}{R} \cdot \frac{dv_{2\text{ss}}}{dt} + (1 - L_2 \cdot C_2 \cdot \omega^2) \cdot v_{2\text{ss}} < v_{1\text{ss}} \quad (9)$$

or equivalently, according to (7)

$$\frac{A}{v_{1\text{ss}}} < \gamma(\omega) \quad (10)$$

where

$$\gamma(\omega) = \frac{1}{L_2 \cdot C_2} \cdot \frac{1}{\sqrt{\frac{\omega^2}{(R \cdot C_2)^2} + \left(\omega^2 - \frac{1}{L_2 \cdot C_2}\right)^2}} \quad (11)$$

is the frequency response of the buck converter output filter, being ω the desired output frequency. Fig. 3 shows the plot of the steady-state sliding domain boundary given by (10)–(11) for fixed values of L_2, C_2 and R.

From this plot, the following conclusions can be drawn:

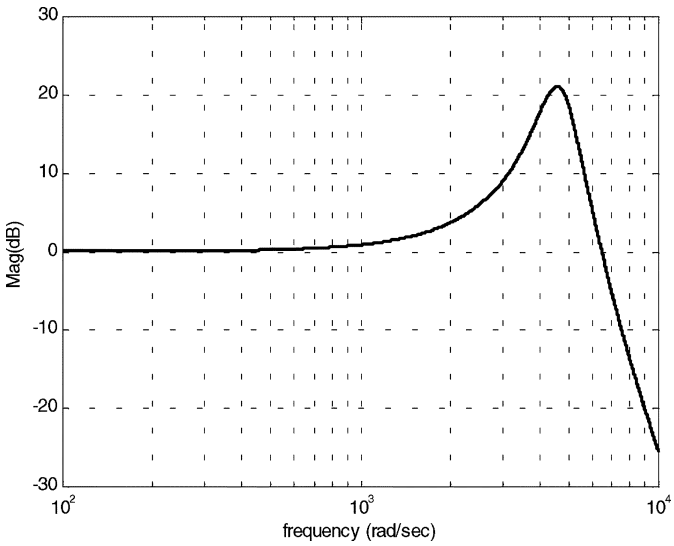


Fig. 3. Gain Bode diagram of $\gamma(\omega)$. Parameters: $L_2 = 750\,\mu$H, $C_2 = 60\,\mu$F and $R = 10\,\Omega$.

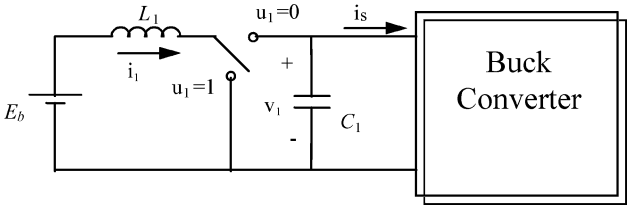


Fig. 4. Definition of the current i_S.

- The steady-state sliding regime is ensured for the values of $A/v_{1\text{ss}}$ lying below the plot of the frequency response of the buck converter output filter. It can be noticed that below the resonant frequency the ratio $A/v_{1\text{ss}}$ must verify $A/v_{1\text{ss}} \leq 1$, in agreement with the step-down characteristic of the buck switched converter.
- If load variations are considered, the design has to take into account the most restrictive sliding domain that corresponds, according to (11), to the minimum load value [19].

It can be pointed out that the steady-state average value of the boost output voltage, $v_{1\text{ss}}$, must be time-varying. This statement can be proved by analyzing the boost output current (or, equivalently, the buck input one), referred as i_S and defined as shown in Fig. 4.

According to (1), this current is given by

$$i_S = u_2 \cdot i_2. \quad (12)$$

Therefore, provided that the buck converter has reached its corresponding steady-state sliding motion, the steady-state boost output current can be written as

$$i_{\text{ss}} = u_{2\text{eqss}} \cdot i_{2\text{ss}}. \quad (13)$$

On the other hand, from (1), the following relation can be easily deduced assuming that the converter has reached the steady state:

$$i_{1\mathrm{ss}} \cdot \left[E_b - L_1 \cdot \frac{di_{1\mathrm{ss}}}{dt} \right] = v_{1\mathrm{ss}} \cdot \left[C_1 \cdot \frac{dv_{1\mathrm{ss}}}{dt} + i_{\mathrm{ss}} \right]. \quad (14)$$

If $v_{1\mathrm{ss}}$ is a constant value, then, $i_{1\mathrm{ss}}$ will be unbounded and the system will become unstable [21]. As a consequence, for the case of a design requiring $A/v_{1\mathrm{ss}} \leq 1$, two main constraints affecting the boost output voltage $v_{1\mathrm{ss}}$ can be highlighted from the previous steady-state analysis, namely, the following.

- Referring to Fig. 1, if an amplitude A higher than the dc input voltage E_b is desired, the boost stage would carry out a large enough step-up voltage ratio v_1/E_b.
- Since the voltage $v_{1\mathrm{ss}}$ is time varying so is the ratio $A/v_{1\mathrm{ss}}$. This ratio must be kept into the boundaries of the buck stage sliding domain, thus overcoming the loss of the buck stage sliding motion.

As a result, the boost stage sliding control will be designed in compliance with these constraints, as it is developed in the following section.

IV. Boost Stage Sliding-Control Design

A. Switching Surface, Sliding Domain and Control Law

Referring to Fig. 4 and according to (1), the boost stage dynamics can be modeled by the following set of differential equations:

$$\begin{cases} L_1 \frac{di_1}{dt} = E_b - v_1 \cdot (1 - u_1) \\ C_1 \frac{dv_1}{dt} = i_1 \cdot (1 - u_1) - i_S \end{cases} \quad (15)$$

where the current i_S is given by (12).

The following switching surface, previously reported in the literature for controlling the dc–dc boost stages [8], [22], is adopted in this paper:

$$\sigma_1(i_1, v_1, t) = \alpha \cdot i_1 + \beta \cdot v_1 - \delta \cdot v_a - K = 0 \quad (16)$$

where $dv_a/dt = v_1^* - v_1$, v_1^* is the desired dc steady-state value of the voltage v_1 for a global A/E_b step-up conversion and $(\alpha, \beta, \delta, \mathrm{K})$ are the sliding surface design parameters. The corresponding sliding motion is given by $\sigma_1(i_1, v_1, t) = 0$.

The equivalent control $u_{1\mathrm{eq}}$ is obtained by applying the invariance condition, and can be expressed as

$$u_{1\mathrm{eq}} = \frac{\alpha C_1 (v_1 - E_b) - \beta L_1 (i_1 - i_S) + L_1 C_1 \delta (v_1^* - v_1)}{\alpha C_1 v_1 - \beta L_1 i_1} \quad (17)$$

whereas the sliding domain can be deduced by imposing $\min\{u^-, u^+\} < u_{1\mathrm{eq}} < \max\{u^-, u^+\}$, or equivalently in this case $0 < u_{1\mathrm{eq}} < 1$, this leading to the following restrictions:

A.

$$\mathrm{sgn}\left[\alpha C_1 v_1 - \beta L_1 i_1\right] \cdot \left[\alpha C_1 (v_1 - E_b) - \beta L_1 (i_1 - i_s) + L_1 C_1 \delta (v_1^* - v_1)\right] > 0.$$

B.

$$\mathrm{sgn}\left[\alpha C_1 v_1 - \beta L_1 i_1\right] \cdot \left[\alpha C_1 E_b - \beta L_1 i_S - L_1 C_1 \delta (v_1^* - v_1)\right] > 0.$$

Finally, the switching control law can be derived applying $d\sigma_1^2/dt < 0$, this resulting in

$$u_1 = \begin{cases} +1, & \text{if } \sigma_1 \cdot \left[\frac{\alpha}{L_1} \cdot v_1 - \frac{\beta}{C_1} \cdot i_1 \right] < 0 \\ 0, & \text{if } \sigma_1 \cdot \left[\frac{\alpha}{L_1} \cdot v_1 - \frac{\beta}{C_1} \cdot i_1 \right] > 0. \end{cases} \quad (18)$$

The parameters $(\alpha, \beta, \delta, K)$ must be designed at least to keep the ratio A/v_1 into the buck stage steady-state sliding domain given by (10)–(11). Since the output voltage amplitude A is fixed by the user, an analysis of the intermediate voltage v_1 dynamic behavior in front of input voltage and load perturbations is mandatory. Accordingly, the following sections are oriented to deduce several design criteria for the parameters $(\alpha, \beta, \delta, K)$ by considering the influence of small and large perturbations of either the input voltage or the load over voltage v_1.

B. Design Criteria According to Small-Signal Dynamics Analysis

This case analyzes the dynamic behavior of the intermediate voltage v_1 in front of small perturbations of the input voltage and the load, under the following assumptions.

- The power system dynamics remains on the sliding surfaces given by (2) and (16), therefore the expressions (4) and (17) corresponding to the equivalent controls prevail.
- The amplitude of the perturbations is small enough to approximate the dynamic behavior of the voltage v_1 by a linear model.

Under these assumptions, the equivalent dynamics of the closed-loop boost stage can be described by

$$\begin{cases} L_1 \frac{di_1}{dt} = E_b - v_1 \cdot (1 - u_{1\mathrm{eq}}) \\ C_1 \frac{dv_1}{dt} = i_1 \cdot (1 - u_{1\mathrm{eq}}) - i_S \\ \sigma_1(i_1, v_1, t) = \alpha \cdot i_1 + \beta \cdot v_1 - \delta \cdot v_a - K = 0 \end{cases} \quad (19)$$

where $u_{1\mathrm{eq}}$ is given by (17), and in this case $i_S = u_{2\mathrm{eq}} \cdot i_2$, since the power system remains on the sliding surfaces. The small signal analysis is carried out in a conventional way, by splitting the variables into their dc–dc steady-state and their perturbed counterparts. In this sense, the small signal analysis corresponding to load perturbations can be carried out in terms of the buck input current i_S, since a load perturbation results in an input current one. Therefore, the variables of (19) can be written as

$$\begin{aligned} E_b &= E_b^* + \hat{E}_b \\ i_s &= i_s^* + \hat{i}_s \\ i_1 &= i_1^* + \hat{i}_1 \\ v_1 &= v_1^* + \hat{v}_1 \\ v_a &= v_a^* + \hat{v}_a \\ u_{1\mathrm{eq}} &= u_{1\mathrm{eq}}^* + \hat{u}_{1\mathrm{eq}} \end{aligned} \quad (20)$$

where, for any variable x, x^* and $\hat{x}$ stands for the dc steady-state and the perturbed values of x respectively. The steady-state values can be deduced taking into account that both E_b^* and v_1^* as well as the load R and the desired sinusoidal output amplitude A are user-defined parameters. Accordingly, the dc steady-state

value of $u^*_{1\mathrm{eq}}$ corresponds to the equivalent steady-state duty-cycle of a boost converter and can be expressed as

$$u^*_{1\mathrm{eq}} = \frac{v_1^* - E_b}{v_1^*} \tag{21}$$

whereas, according to (14), i_S^* is given by

$$i_S^* = \frac{A^2}{2Rv_1^*}. \tag{22}$$

At last, i_1^* can be deduced assuming no losses in the boost stage, i.e,

$$i_1^* = \frac{v_1^*}{E_b} i_S^* \quad \Leftrightarrow \quad i_1^* = \frac{A^2}{2RE_b}. \tag{23}$$

Finally, by replacing (20) into (19) and neglecting higher order terms of perturbed variables, the closed-loop system defined by (19) can be represented by the following linear one:

$$\begin{cases} L_1 \frac{d\hat{i}_1}{dt} = \hat{E}_b - \hat{v}_1 + v_1^* \cdot \hat{u}_{1\mathrm{eq}} + \hat{v}_1 \cdot u^*_{1\mathrm{eq}} \\ C_1 \frac{d\hat{v}_1}{dt} = \hat{i}_1 - i_1^* \cdot \hat{u}_{1\mathrm{eq}} - \hat{i}_1 \cdot u^*_{1\mathrm{eq}} - \hat{i}_S \\ \frac{d\hat{v}_a}{dt} = -\hat{v}_1 \\ \alpha \cdot \hat{i}_1 + \beta \cdot \hat{v}_1 - \delta \cdot \hat{v}_a = 0. \end{cases} \tag{24}$$

The dynamic behavior of $\hat{v}_1$ with respect to input voltage and load perturbations can be inferred from (21)–(24) and can be expressed in the form of the following closed-loop transfer functions:

$$G_i(s) = \frac{\hat{V}_1(s)}{\hat{I}_S(s)} = \frac{-2RE_b\alpha v_1^* s}{\Delta(s)} \tag{25a}$$

$$G_E(s) = \frac{\hat{V}_1(s)}{\hat{E}_b(s)} = \frac{\alpha A^2 s}{\Delta(s)} \tag{25b}$$

where

$$\Delta(s) = \left(2RE_b\alpha C_1 v_1^* - \beta L_1 A^2\right) s^2 + \left(2RE_b^2\beta + \frac{\alpha A^2 E_b}{v_1^*}\right) s + 2RE_b^2\delta. \tag{26}$$

As can be seen, these transfer functions exhibit one closed-loop zero at the origin, thus confirming the robustness of the sliding-control law in front of input voltage and current (i.e output load) step perturbations. Furthermore, these transfer functions can be used to derive the following design restrictions.

1) Small-Signal Stability: The poles must be located in the left-half plane, this leading to the following constraint:

$$\frac{A^2}{2RE_b^2 v_1^*} \cdot (\delta \cdot L_1 \cdot v_1^* - \alpha \cdot E_b) < \beta < \alpha \cdot \frac{2RC_1 \cdot E_b \cdot v_1^*}{L_1 \cdot A^2}. \tag{27}$$

2) Overdamped Small-Signal Dynamics: In order to preserve the buck inverter steady-state sliding domain given by (10), it would be desirable to guarantee a slightly overdamped dynamics of v_1 in front of input voltage and load perturbations. This design criterion requires the poles of the closed-loop transfer functions (25a) and (25b) to be real, whatever the values of R and E_b are. According to (25a)–(25b) these poles are the roots of

$$\left[2RE_b\alpha C_1 v_1^* - \beta L_1 A^2\right] s^2 + \left[2RE_b^2\beta + \frac{\alpha A^2 E_b}{v_1^*} - \delta L_1 A^2\right] s + 2RE_b^2\delta = 0 \tag{28}$$

which can be rewritten as $1 + F(s) = 0$ where

$$F(s) = R \cdot \frac{\left[2E_b\alpha C_1 v_1^*\right] \cdot s^2 + \left[2E_b^2\beta\right] \cdot s + 2E_b^2\delta}{\left[-\beta L_1 A^2\right] \cdot s^2 + \left[\frac{\alpha A^2 E_b}{v_1^*} - \delta L_1 A^2\right] \cdot s} \tag{29}$$

therefore the root locus of $F(s)$ in terms of the load parameter R will correspond to the roots of (28). Since the poles of $F(s)$ given by $s = 0$ and $s = [(\alpha \cdot E_b)/(\beta \cdot L_1 \cdot v_1^*) - \delta/\beta]$ are real, the root locus will lie on the real left-half plane axis (thus leading to an overdamped response) for any value of R if the zeros of $F(s)$ are real as well. This condition can be accomplished if the design verifies

$$\beta^2 \geq \frac{4 \cdot \alpha \cdot C_1 \cdot v_1^* \cdot \delta}{E_b}. \tag{30}$$

3) Steady-State Design: The previous small-signal analysis can also be applied to infer additional design criteria when the power converter operates in steady-state. When the buck converter is in steady-state sliding motion, the output boost stage current i_{SS} is given by (13), which can be written from (1), (7)–(8), assuming that $\hat{v}_{1\mathrm{ss}} \ll v_1^*$, in terms of its dc and ac counterparts as

$$i_{\mathrm{ss}} = i^*_{\mathrm{ss}} + \hat{i}_{\mathrm{ss}}$$

where

$$\begin{aligned} i^*_{\mathrm{ss}} &= \frac{A^2}{2v_1^* R} \\ \hat{i}_{\mathrm{ss}} &= K(\omega) \cdot \sin(2\omega t + \theta) \\ K(\omega) &= \frac{A^2}{2v_1^* R}\left[(L_2C_2\omega)^2 + \left(\frac{L_2\omega}{R}\right)^2 + \left(L_2C_2\omega^2 - 1\right)^2\left(1 + R^2C_2^2\omega^2\right)\right]^{1/2} \end{aligned} \tag{31}$$

therefore i_{ss} is sinusoidal time-dependent and exhibits a ripple at twice the desired output frequency, thus leading to a ripple of the voltage $\mathrm{v}_{1\mathrm{ss}}$ at the same frequency given by (25a), namely

$$\left|\hat{V}_{1\mathrm{ss}}(2j\omega)\right| = |G_i(2j\omega)| \cdot K(\omega) \tag{32}$$

thus evidencing the time dependence of the intermediate steady-state voltage $v_{1\mathrm{ss}}$ pointed out in Section III. This voltage ripple amplitude can lead the ratio $A/v_{1\mathrm{ss}}$ beyond the steady-state sliding domain boundary of the buck dc–ac converter given by (10), thus leading to a loss of sliding motion. Therefore, in order to counteract this possibility, a proper attenuation of $|G_i(2j\omega)|$

has to be designed, this involving according to (25a) the surface parameters (α, β, δ) as well as the boost converter components L_1 and C_1. The following design procedure is suggested assuming that the next parameters are known.

The desired output voltage amplitude and frequency noted as A_d and ω_d, respectively.

The input voltage E_b, the buck inductor and capacitor values L_2 and C_2 and the dc steady-state boost output voltage v_1^*.

The minimum load value, noted as $R_{\min}$.

Taking into account these previous assumptions, the maximum current ripple is also known from (31), namely

$$K(\omega_d) = \frac{A_d^2}{2v_1^* R_{\min}} \left[(L_2 C_2 \omega_d)^2 + \left(\frac{L_2 \omega_d}{R_{\min}} \right)^2 + \left(L_2 C_2 \omega_d^2 - 1 \right)^2 \left(1 + R_{\min}^2 C_2^2 \omega_d^2 \right) \right]^{1/2} \quad (33)$$

from which the corresponding voltage amplitude can be deduced according to (32), i.e.,

$$\left| \hat{V}_{1\mathrm{ss}}(2j\omega_d) \right| = |G_i(2j\omega_d)| \cdot K(\omega_d). \quad (34)$$

The design procedure starts by fixing a desired value of $\left| \hat{V}_{1\mathrm{ss}}(2j\omega_d) \right|$ such that

- $\left| \hat{V}_{1\mathrm{ss}}(2j\omega_d) \right|$ is in compliance with the small-signal analysis validity range. Regarding the voltage ripple as a steady-state perturbation, this constraint can be usually satisfied by fixing a perturbation level at most of 10% of the dc steady-state value, therefore

$$\left| \hat{V}_{1\mathrm{ss}}(2j\omega_d) \right| = \lambda \cdot v_1^* \qquad \text{where} \quad \lambda \leq 0,1. \quad (35)$$

- The sliding domain of the buck inverter is preserved, *i.e.* $A_d/v_1 < 1$, this leading to:

$$v_1^* - \left| \hat{V}_{1\mathrm{ss}}(2j\omega_d) \right| > A_d \quad (36)$$

or, equivalently according to (35)

$$\lambda < 1 - \frac{A_d}{v_1^*}. \quad (37)$$

Consequently, λ is selected to verify the most restrictive of the constraints (35) and (37). Subsequently, the value of the desired attenuation can be known from (34) and (35), i.e.,

$$|G_i(2j\omega_d)| = \frac{\lambda v_1^*}{K(\omega_d)}. \quad (38)$$

Accordingly, the unknown parameters of the transfer function $G_i(s)$ given in (25a) must be designed to fulfill (38). In order to simplify the design, this transfer function is rewritten in a normalized form as follows:

$$G_i(s) = \frac{-G_1 \cdot s}{s^2 + 2\xi\omega_n \cdot s + \omega_n^2} \quad (39)$$

$$\text{where} \quad G_1 = \frac{2R_{\min} E_b \alpha v_1^*}{(2 \cdot R_{\min} E_b \alpha C_1 v_1^* - \beta L_1 A_d^2)} \quad (40)$$

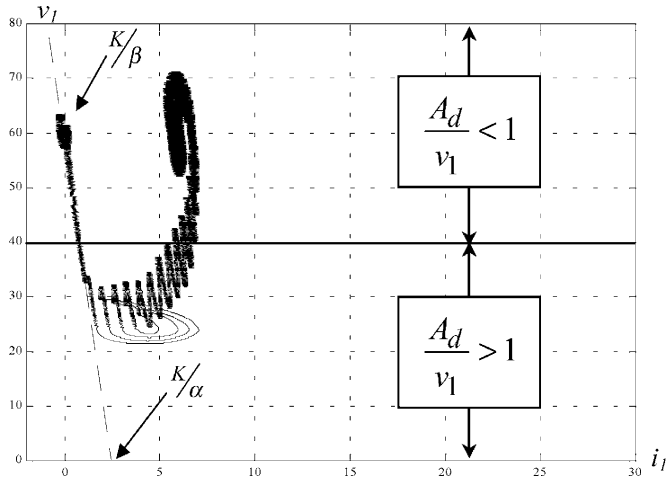


Fig. 5. Simulation of a load step change from open circuit to $R = 5\,\Omega$. Parameters: $L_1 = 1$ mH, $C_1 = 1000\,\mu$F, $L_2 = 750\,\mu$H, $C_2 = 60\,\mu$F, $E_b = 24$ V, A = 40 V, $\omega = 2\pi 50$ rad/s, $\alpha = 0.8$, $\beta = 0.0228$, $\delta = 1.573$, $K = 1$, $a_1 = 2000$, $a_2 = 1$, and $v_1^* = 60$ V.

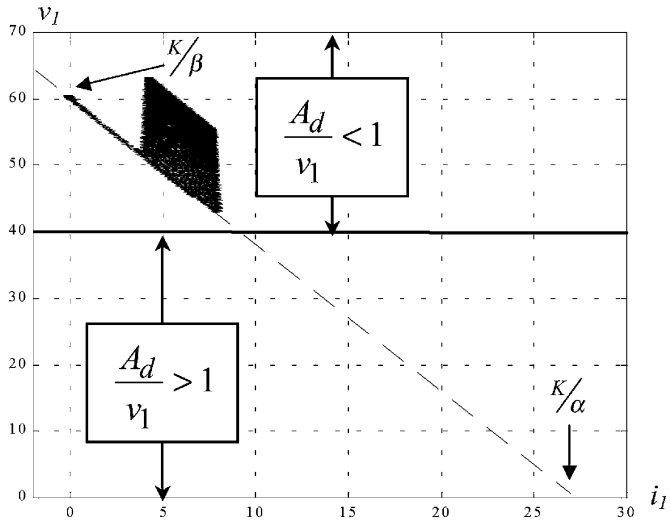


Fig. 6. Simulation of a load step change from open circuit to $R = 5\,\Omega$. Parameters: $L_1 = 1$ mH, $C_1 = 1000\mu$F, $L_2 = 750\mu$H, $C_2 = 60\,\mu$F, $E_b = 24$ V, $A = 40$ V, $\omega = 2\pi 50$ rad/s, $\alpha = 0.8$, $\beta = 0.35$, $\delta = 1.573$, $K = 21$, $a_1 = 2000$, $a_2 = 1$, and $v_1^* = 60$ V.

$$\omega_n^2 = \frac{2R_{\min} E_b^2 \delta}{(2 \cdot R_{\min} E_b \alpha C_1 v_1^* - \beta L_1 A_d^2)} \quad (41)$$

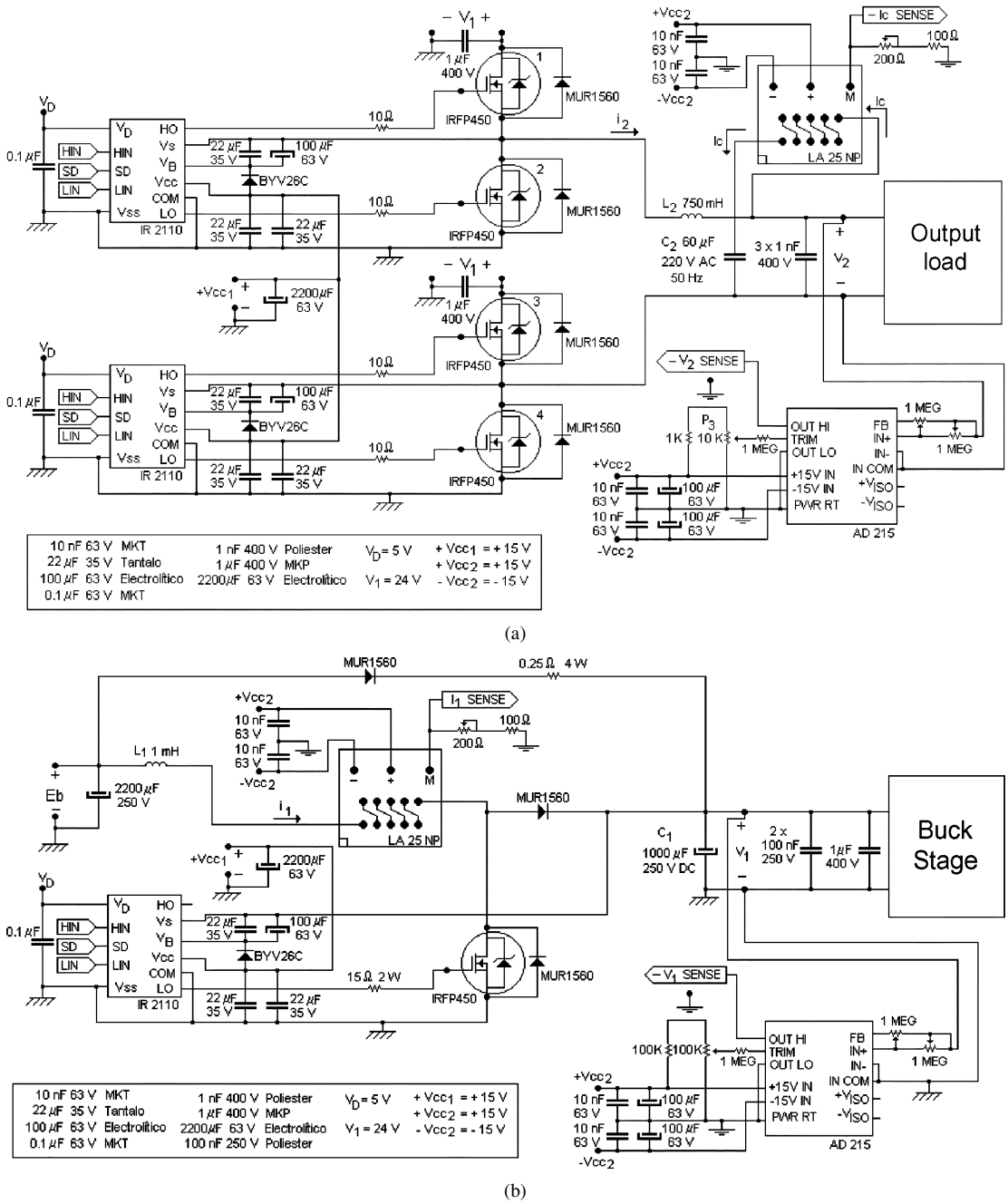
$$2\xi\omega_n = \frac{\left(2R_{\min} E_b^2 \beta + \frac{\alpha A_d^2 E_b}{v_1^*} - \delta L_1 A_d^2 \right)}{(2 \cdot R_{\min} E_b \alpha C_1 v_1^* - \beta L_1 A_d^2)}. \quad (42)$$

Therefore, from (39), the attenuation $|G_i(2j\omega_d)|$ satisfies

$$|G_i(2j\omega_d)| = \frac{2\omega_d G_1}{|-4\omega_d^2 + 4\xi j\omega_n \omega_d + \omega_n^2|}. \quad (43)$$

The design is simplified by assuming that the ripple frequency $2\omega_d$ lies on the high frequency attenuation range of $|G_i(j\omega)|$. In this case, (43) can be approximated by

$$|G_i(2j\omega_d)| \cong \frac{G_1}{2\omega_d}. \quad (44)$$



(a)

(b)

Fig. 7. (a) Buck inverter power stage circuit. (b) Boost converter power stage circuit.

According to this assumption, the following value of ω_n has been arbitrarily selected:

$$\omega_n = \frac{\omega_d}{5} \tag{45}$$

this enabling the design of real poles (i.e, an overdamped response) with a damping factor ξ such that $\xi \cong 1$ in order to fulfill the approximation given in (44). Therefore, from (38) and (44), the value of G_1 can be deduced as

$$G_1 = \frac{2\omega_d \lambda v_1^*}{K(\omega_d)} \tag{46}$$

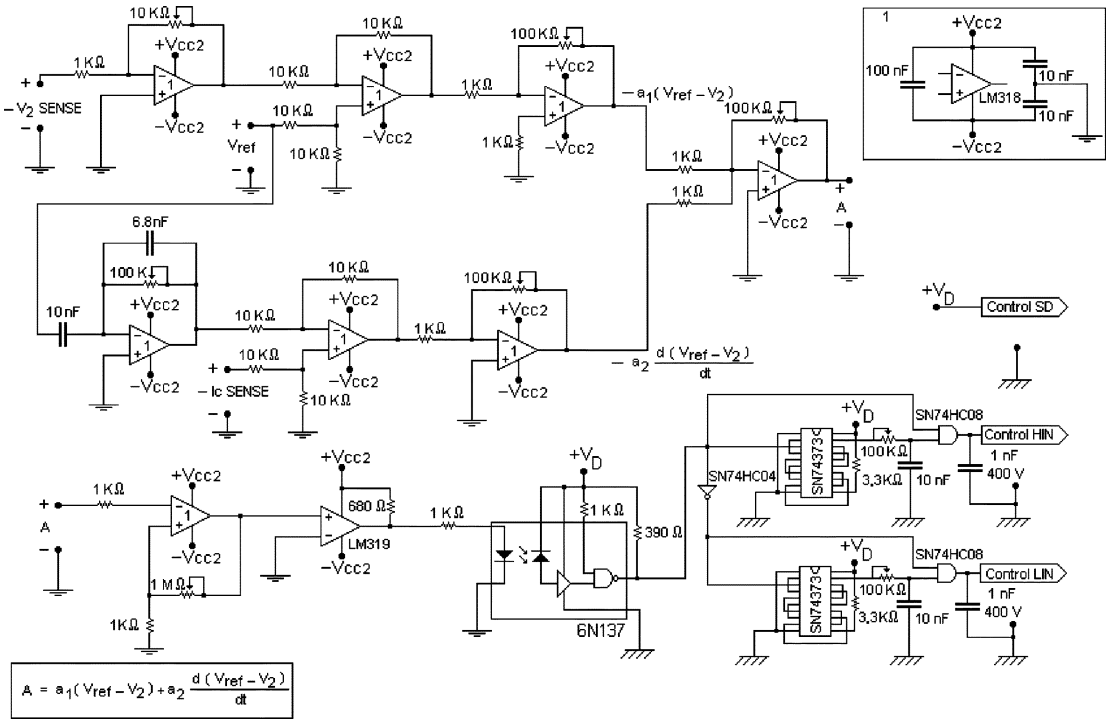
whereas, according to (40), (41), and (45), the following design relations holds:

$$\delta = \frac{\alpha v_1^* \omega_n^2}{E_b G_1} = \frac{\alpha v_1^* \omega_d^2}{25 E_b G_1} \qquad C_1 = \frac{1}{G_1} + \frac{\beta \cdot L_1 \cdot A_d^2}{2RE_b \alpha v_1^*}. \tag{47}$$

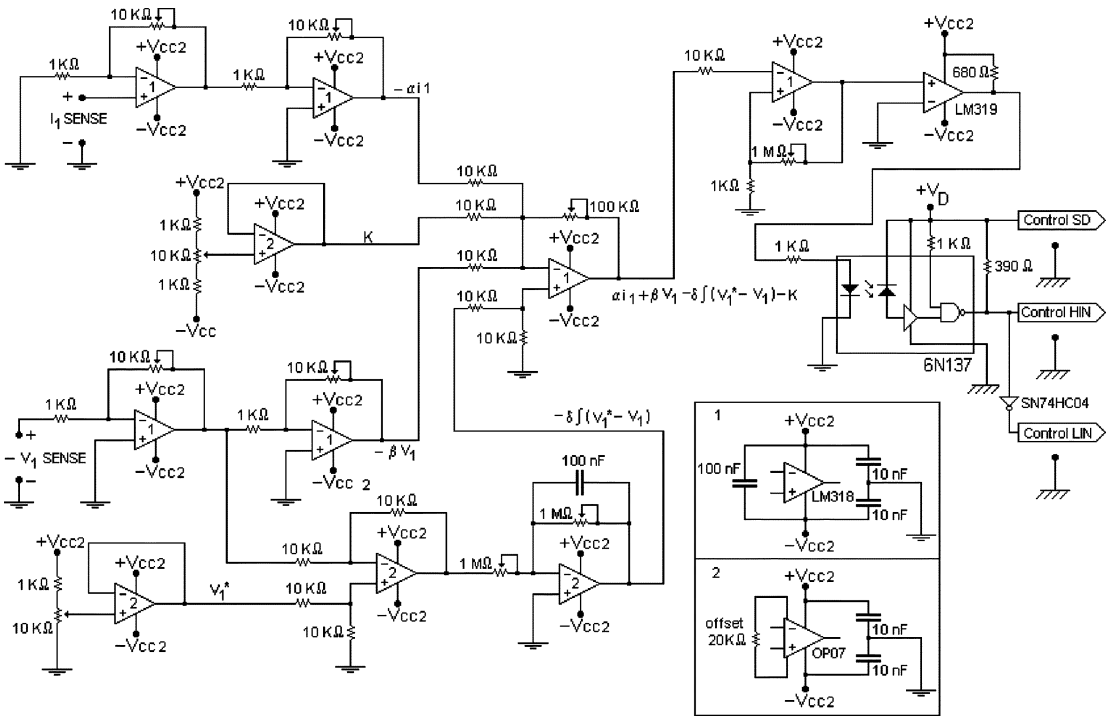
These design relationships can be applied only under small-signal perturbation assumptions. When large-signal perturbations are considered, other design criteria complementing the previous ones arise, as it is highlighted in the next section.

C. Design Criteria According to the Large-Signal Transient Response

In order to infer additional design criteria, the following example is presented to illustrate the large-signal behavior of the power stage in the state plane under the sliding-control laws given in (6) and (18). This example considers a boost–buck dc–ac power stage with the following parameter values: $L_1 = 1$ mH, $C_1 = 1000$ μF, $L_2 = 750$ μH, $C_2 = 60$ μF, $R = 1000$ Ω (i.e, open circuit) and $E_b = 24$ V; the desired output



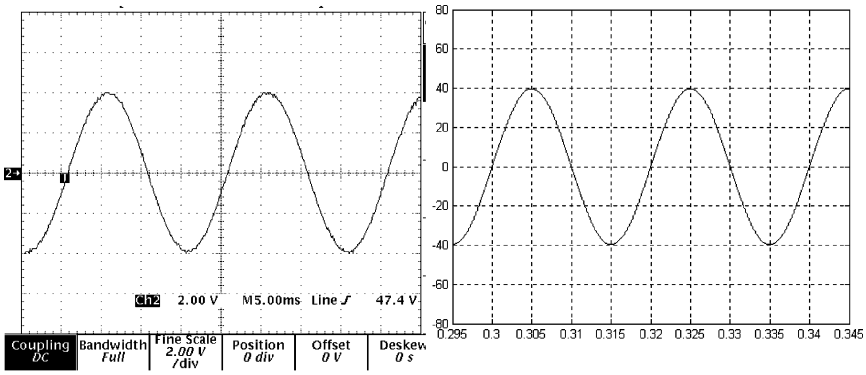
(c)



(d)

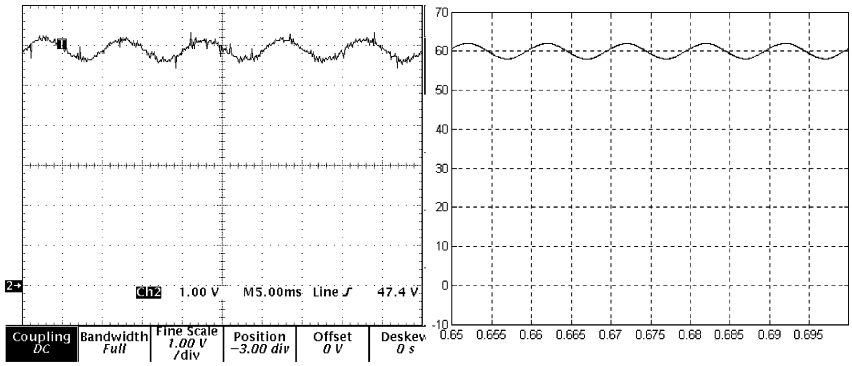
Fig. 7 *(Coninued.)* (c) Buck inverter control circuit. (d) Boost converter control circuit.

signal parameters are fixed to $A_d = 40$ V (this corresponding to a global voltage step-up dc–ac conversion from a 24-V dc to 80 Vpp) and $\omega_d = 2\pi 50$ rad/s, being the dc component of the boost output voltage set to $v_1^* = 60$ V. Additionally, the buck switching surface parameters are $a_1 = 2000$, $a_2 = 1$ whereas those corresponding to the boost one have been deliberately selected to hold a pair of conjugate poles according to (30), namely $\alpha = 0.8$, $\beta = 0.0228$, $\delta = 1.573$, $K = 1$. Fig. 5 shows the Matlab® simulation of he boost converter state variables (i_1, v_1) when, starting from the open circuit steady-state defined by ($i_1^* = 0$ A; $v_1^* = 60$ V), a load step change from open circuit to $R = 5\ \Omega$ is applied at $t = t_0$.



(a) (b)

Fig. 8. (a) Measured and (b) Matlab simulation of the steady-state output voltage v_2. Scaling factor $K = 0.1$.



(a) (b)

Fig. 9. (a) Measured and (b) Matlab simulation of the steady-state intermediate voltage v_1. Scaling factor $K = 0.1$.

Although a full analytical description is extremely cumbersome, the dynamic behavior shown in Fig. 5 can be interpreted by initially neglecting the state variables ripple as follows.

- $t = t_0^-$: prior to the load step change, the boost converter is in the steady state corresponding to open circuit; therefore, according to (16), the following relation holds:

$$S_1(i_1, v_1, t_0^-) = \alpha \cdot i_1 + \beta \cdot v_1 - \delta \cdot \int_0^{t_0^-} (v_1^* - v_1)dt - K = 0 \quad (48)$$

and particularly, for the open-circuit steady state (namely, $i_1^* = 0$ A; $v_1 = v_1^*$)

$$\beta \cdot v_1^* - \delta \cdot \int_0^{t_0^-} (v_1^* - v_1)dt - K = 0. \quad (49)$$

- $t_0 < t \leq t_1$: after the load step and during a time-interval $\Delta t = t_1 - t_0$ the state trajectory remains on the switching surface $S_1(i_1, v_1, t_0^-) = 0$. The main reasons for this behavior are as follows.
  a) The boost converter quickly recovers the switching surface $S_1(i_1, v_1, t_0^-) = 0$ due to the sliding-control action.
  b) The integrative term does not change significantly and can be approximated by its steady-state value, namely

$$\int_0^{t_0+\Delta t} (v_1^* - v_1)dt \cong \int_0^{t_0^-} (v_1^* - v_1)dt. \quad (50)$$

Since the relation (48) holds, the state plane trajectory can be written, according to (49), as

$$v_1 \cong -\frac{\alpha}{\beta} \cdot i_1 + v_1^* \quad (51)$$

this corresponding to the equation of a straight line in the plane (i_1, v_1) with a slope of $-\alpha/\beta$ and a constant term given by v_1^*.

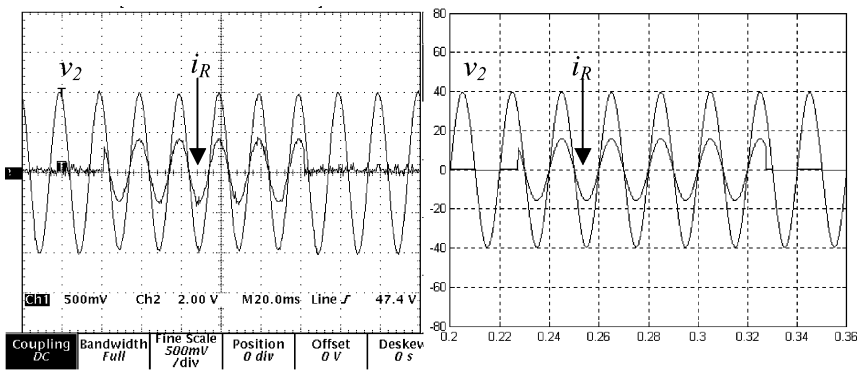
- For $t \geq t_1$ the integrative term increases and the system leaves the straight line given in (51) evolving with a second order underdamped dynamics, according to the complex poles location, to the new equilibrium point.

Fig. 5 also shows how, even remaining on the straight line defined in (51), the boost output voltage v_1 falls below the level of the sinusoidal amplitude A_d, thus leading to a buck sliding motion loss since in this case $A_d/v_1 > 1$. This behavior suggests that the absolute value of the slope must be as low as possible to overcome this possibility. In accordance with this qualitative analysis, the values of α and β are designed so that

$$\beta = \frac{\alpha \cdot i_1^*|_{R=R\min}}{v_1^* - A_d - |\hat{v}_1|_{\max}} \quad (52)$$

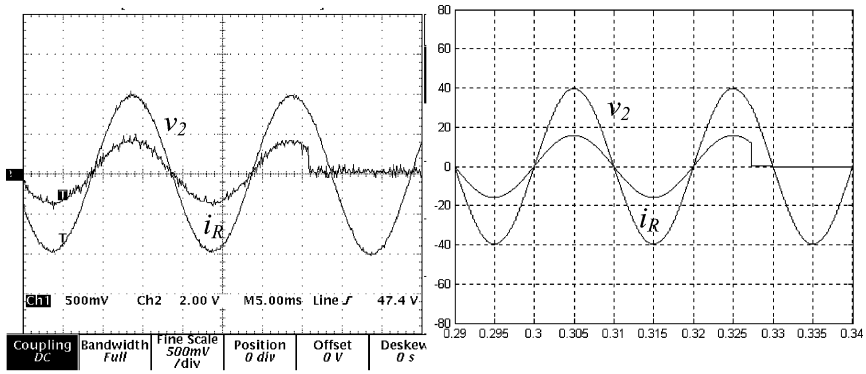
thus corresponding to a straight line in the plane (v_1, i_1) defined by the points according to the open circuit and the $R_{\min}$ load values, thus preserving the buck converter sliding domain in the worst case. On the other hand, the value of K has been rbitrarily fixed to set the integrative term value to zero in open circuit steady-state operation; therefore, from (49)

$$K = \beta \cdot v_1^*. \quad (53)$$



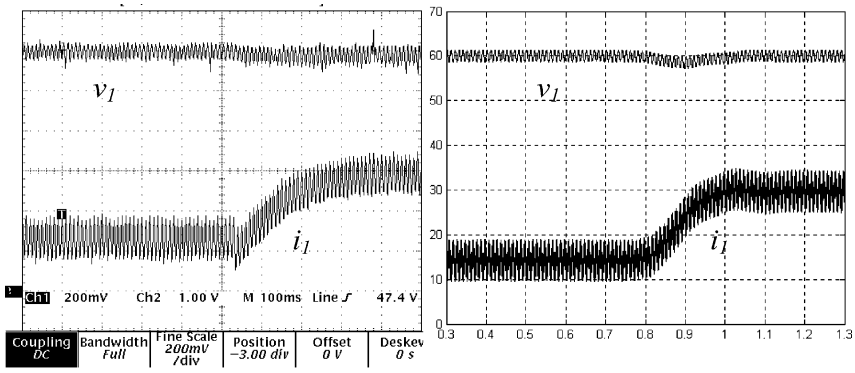
(a) (b)

Fig. 11.(a) Measured and (b) Matlab simulation of the output signal v_2 and the load current i_R for a load step change (open circuit – $R = 10\ \Omega$ – open circuit). Voltage scaling factor $K = 0.1$, current scaling factor $K = 100$ mV/A.



(a) (b)

Fig. 12. Zoom of the (a) measured and (b) Matlab simulation of the output voltage v_2 and load current i_R for a load step change ($R = 10\ \Omega$–open circuit). Voltage scaling factor $K = 0.1$, current scaling factor $K = 0.1$ V/A.



(a) (b)

Fig. 13. (a) Measured and (b) Matlab simulation of the intermediate voltage v_1 and the converter input current i_1 for an input voltage step from 50 to 24 V. Voltage scaling factor $K = 0.1$, current scaling factor $K = 0.1$ V/A. Transient dynamics of the power supply have been included in the Matlab® simulations.

In order to validate this design criteria, Fig. 6 shows the Matlab simulation of (i_1, v_1) for a new set of values of K and β modified according to (52) and (53), in front of the same load perturbation. As can be seen, the buck sliding domain is preserved, whereas the boost dynamics exhibits the expected overdamped behavior and reaches the new equilibrium point $(v_1^*, i_1^* = A_d^2/2RE_b)$.

D. Suggested Design Procedure

Provided that the values of the following parameters are known: $A_d, \omega_d, R_{\min}, E_b, v_1^*, C_2, L_2$, and collecting the results of the previous sections, the following design procedure is proposed.

– Fix α and L_1
– Determine λ and $\hat{v}_{1\max}$ according to **(35)** and **(37)**
– Determine K and β according to **(52)** and **(53)**
– Determine $K(\omega_d)$ and G_1 according to **(33)** and **(46)**
– Determine δ and C_1 according to **(47)**.

V. Simulation and Experimental Results

The proposed design has been tested by means of both Matlab® simulations and measurements carried out on a

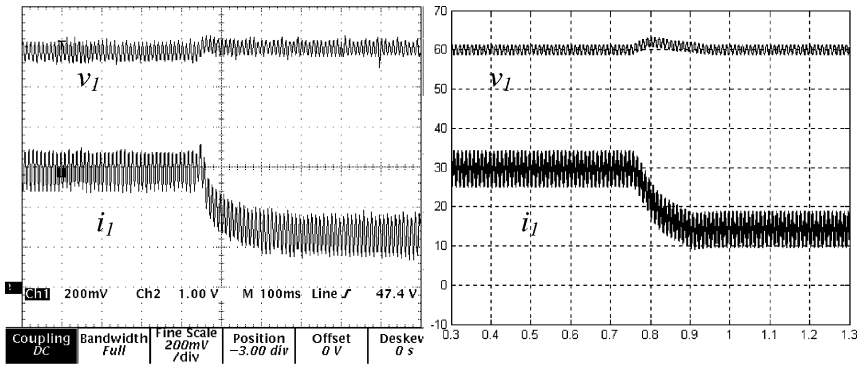


Fig. 14. (a) Measured and (b) Matlab simulation of the intermediate voltage v_1 and the converter input current i_1 for an input voltage step from 24 to 50 V. Voltage scaling factor $K = 0.1$, current scaling factor $K = 0,1$ V/A. Transient dynamics of the power supply have been included in the Matlab simulations.

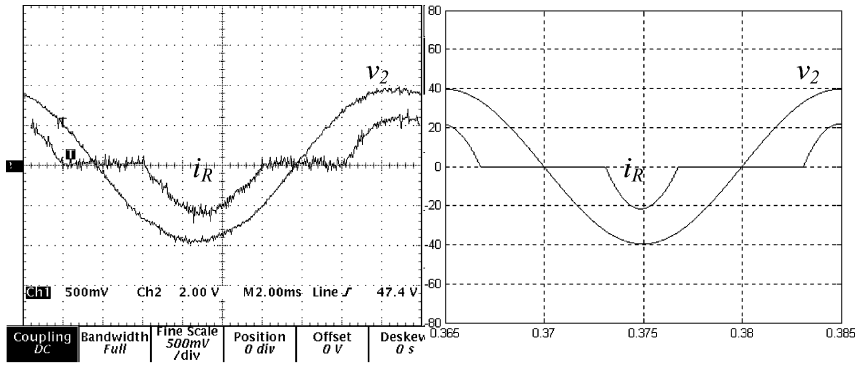


Fig. 15. (a) Measured and (b) Matlab simulation of the output voltage v_2 and the output current i_R when the converter is loaded with a full-wave rectifier. Voltage scaling factor $\mathrm{K} = 0.1$, current scaling factor $K = 0.1$ V/A.

laboratory prototype which experimental set-up is shown in Fig. 7(a)–(d). The circuit parameters have been fixed in accordance with the design procedure exposed in the paper, and are as follows.

- Output signal and minimum load: $A_d = 40$ V and $\omega_d = 2\pi 50$ rad/s, $R_{\min} = 10\ \Omega$.
- Input voltage and intermediate voltage: $E_b = 24$ V, $v_1^* = 60$ V.
- Steady-state intermediate voltage ripple $\hat{v}_{1\mathrm{SSpp}} = 4{,}8\ \mathrm{V_{pp}}$ (*i.e*, $\lambda = 4\%$)
- boost–buck power stage: $L_1 = 1$ mH, $C_1 = \mu 1000$ F, $L_2 = \mu 750$ H, $C_2 = \mu 60$ F,
- Sliding surfaces parameters: $\alpha = 0.8$, $\beta = 0.1515$, $\delta = 7$, $K = 9$, $a_1 = 12$, $a_2 = 0.005$

Fig. 8 shows the measured and the simulation of the steady-state dc–ac converter output voltage v_2 , which confirms the achievement of a step-up conversion from 24 V dc to (80 $\mathrm{V_{pp}}$, 50 Hz) ac with good accuracy. Similarly, Fig. 9 shows the measured and the simulation of the intermediate steady-state voltage v_{1SS} which can be approximated by $v_{1SS} \approx 60 + 2{,}3\sin(2\pi \cdot 100 \cdot t)$, thus exhibiting as expected the desired ripple amplitude at twice the output frequency. As far as the transient dynamics in front of load perturbations is concerned, Figs. 10–12 show the measured and the simulation of the converter response in front of a load step change from open circuit to 10 Ω and back to open circuit. Particularly, Fig. 10 shows both the input current i_1 and the intermediate voltage v_1 which does not exhibit any overshoot. Fig. 11 corresponds to the measured and the simulation of the output voltage v_2 and the load current in front of the same load perturbation profile, whereas Fig. 12 shows a zoom of these output variables evidencing the robustness of the output voltage in front of load perturbations. On the other hand, Figs. 13 and 14 show the intermediate voltage v_1 and the input current i_1 for a input voltage step from 50 to 24 V and from 24 to 50 V, respectively, where the dynamics of the power supply transients has been included in the simulations.

As it can be seen, the input voltage step does not modify significantly the intermediate voltage v_1, thus preserving the sliding domain of the buck converter. Finally, Fig. 15 shows the output voltage and the output current when the boost–buck dc–ac converter is loaded with a full-wave rectifier, highlighting the robustness of the output voltage in front of nonlinear loads as well. In this sense, a total harmonic distortion (THD) of 0.5% for the resistive load and of 1.8% for the full wave rectifier have been also measured. Finally, it can be pointed out that all the simulation results are close to the measured ones, thus confirming the usefulness of the presented analytical approach.

VI. Conclusion

This paper has presented a sliding-mode control design of a boost–buck dc–ac switching converter for a voltage step-up dc–ac conversion without the use of any transformer. The proposed approach has been based on the design of two sliding-con-

trol laws, one ensuring the control of the full-bridge buck converter for a proper dc–ac conversion, and the other one to control the boost converter for guaranteeing a global dc–ac voltage step-up ratio. Taking advantage of previous results for the buck sliding-mode control design, the work has been mainly focused on the design of a sliding-control law for the boost converter, which has been oriented to preserve the buck sliding motion. This design has been performed through a small-signal dynamic analysis and has taken into account the large-signal behavior of the boost stage in the state plane. As a result, a set of design criteria and a complete design procedure have been suggested. Furthermore, the simulation and experimental results presented in the paper are in close agreement and have shown the achievement of a step-up conversion from 24 V dc to (80 V_{pp}, 50 Hz) ac with a good accuracy and low THD for both resistive and nonlinear loads, as well as robustness in front of input voltage and load perturbations, thus validating the proposed design. In this sense, the approach presented in the paper can be applied for a robust and accurate dc–ac step-up transformerless conversion involving other output voltage amplitudes and frequencies by applying the design procedure exposed in the paper, and changing accordingly the buck converter sinusoidal voltage reference.

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