Odd-Harmonic Digital Repetitive Control of a Single-Phase Current Active Filter

Ramon Costa-Castelló, *Member, IEEE*, Robert Griñó, *Member, IEEE*, and Enric Fossas

***Abstract*—Shunt active power filters have been proved as useful elements to correct distorted currents caused by nonlinear loads in power distribution systems. This work presents an all-digital approach, based on the repetitive control technique, for their control. In particular, a special digital repetitive plug-in controller for odd-harmonic discrete-time periodic references and disturbances is used. This approach does not introduce high gain at those frequencies for which it is not needed, and thus it improves robustness. Additionally, the necessary data memory capacity is lower than in traditional repetitive controllers.**

The design is performed for the particular case of single-phase shunt active filter with a full-bridge boost topology. Several experimental results are also presented to show the good behavior of the closed-loop system.

***Index Terms*—Current harmonics compensation, digital repetitive control, PWM converters, sampled-data control, shunt active filters.**

I. Introduction

In RECENT years, there has been a proliferation of nonlinear loads such as power electronic converters in typical power distribution systems. This fact has reduced the power quality of electric power systems. In particular, voltage harmonics and power distribution equipment problems result from current harmonics produced by nonlinear loads. This fact has led to the proposal of more stringent requirements regarding power quality like those collected in the standards IEC-61 000-3-$\{2, 4\}$ and IEEE-519.

Much work has been done in the area of active filter control; [1]–[6] can be cited, among others. Nevertheless it seems that, as a conclusion, the critical point is the need for high gain current control loops [4]. Perhaps the easiest way to obtain them is to use some kind of hysteresis controller (or relay controller) [7]. However, there is a technique, called repetitive control, that allows control loops to be designed with high gain at the harmonic frequencies of a fundamental one. This methodology arose from the internal model principle (IMP) [8] of control theory and is particularly suitable for periodic-signal tracking problems and periodic-signal disturbance rejection problems. Therefore, the necessary high-gain requirements of current control loops in active filters can be met with this approach. Particularly, this work uses the repetitive control technique to design a high-gain digital control current loop for a single-phase shunt active filter.

The concept of repetitive control has been largely used in different control areas such as CD and hard disk arm actuators [9]–[11], robotics [12], [13], machining [14], electro-hydraulics [15], torque vibration suppression in motor control [16], [17], power electronic converters [18], unity power factor rectifiers [19], pulse-width modulated (PWM) inverters [20]–[24] and uninterruptible power supply (UPS) systems [25], [26].

Normally, in power electronic systems, the reference and disturbance signals appearing in control loops, in steady-state, are periodic signals with only odd harmonics in their Fourier series expansion. If the usual repetitive control methodology is used in these systems, the open-loop transfer function includes high gain in all the harmonic frequencies [27]. However, it is not necessary to include high gain at even harmonic frequencies and, what is worse, it means a waste of control effort and a reduction of system robustness without improving system performance. In addition, the introduction of high gain at even harmonic frequencies, generally, implies that the open-loop transfer function includes an integral term. This fact, together with the inclusion of sensors that use transformers[1] in the loop, gives closed loops that are not internally stable. Hence, any controller with integral action, like PID controllers or traditional repetitive controllers, must be precluded in systems with pure derivative terms in order to obtain an internally stable closed-loop system. This work designs and implements an odd-harmonic digital repetitive current controller for a single-phase shunt active filter and, as aforementioned, the controller only introduces high gain at odd harmonic frequencies, i.e., it only introduces high gain where it is needed [28].

The paper is organized as follows. Section II introduces the problem and its specifications. Section III shows the multiloop controller design and the underlying theoretical aspects. Section IV describes the experimental setup and some implementation issues. Section V presents several experimental results that show the good behavior of the whole system. Finally, Section VI summarizes the results of this work.

II. Problem Statement and Specifications

Fig. 1 shows the layout of the system under study: a mixed linear and nonlinear load connected to a power source with an internal impedance. The nonlinear load draws a distorted current waveform (nonsinusoidal shape) with the same fundamental period as voltage but with high order harmonic content. In addi-

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[1]The dynamic model of the transformer has a pure derivative term, i.e., a transmission zero in $s = 0$.

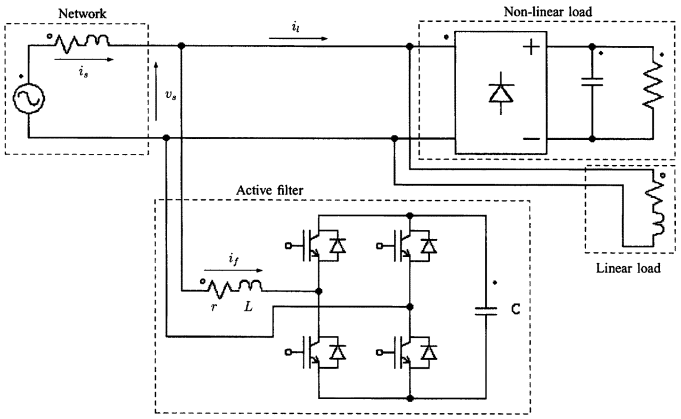

Fig. 1. Single-phase parallel active filter connected to a network with a linear and a nonlinear load.

tion, the linear load can demand some reactive power from the source and, in consequence, its sinusoidal current has a lag with respect to the voltage waveform.

The averaged (at the switching frequency) model of the full-bridge boost active filter is given by

$$L\dot{x}_1 = -rx_1 - x_2u + v_s \tag{1}$$

$$C\dot{x}_2 = x_1u \tag{2}$$

where x_1 is the inductor current (i_f) and x_2 is the dc capacitor voltage; $v_s = E\sin(\omega_r t)$ is the voltage at the network terminals; r sums up the parasitic resistance of all the converter elements, and L and C stand for the inductor and the capacitor of the converter, respectively. The control variable u takes its value in the closed real interval $[-1, 1]$ and represents the averaged value of the pulse-width modulated (PWM) control signal injected to the real system. As can be seen in Fig. 1, $x_1 = i_f = i_s - i_l$. The control objectives are[2]:

1) constant average value of the voltage at the dc bus capacitor, i.e., $\langle x_2\rangle_0^* = V_d$, where V_d must fulfill the boost condition $V_d > E$;
2) sinusoidal source current in phase with the voltage waveform, i.e., $i_s^* = I_d^*\sin(\omega_r t)$.

These two objectives define a nonstandard control problem: the first one is a regulation objective as for the mean value of x_2, but the second one is not a tracking specification because only a shape and not a function is desired, that is I_d^* is not known a priori and it must take the adequate value to maintain the power balance of the whole system. This special form for the problem specifications implies the particular structure of the controller loops described in Section III.

III. Controller Structure

Defining $v = ux_2$ and $\mathbf{y} = [x_1, (1/2)x_2^2]'$, (1) and (2) can be restated as

$$L\dot{y}_1 = -ry_1 - v + v_s \tag{3}$$

$$C\dot{y}_2 = y_1v \tag{4}$$

[2]In this work $\langle x\rangle_0$ means the dc value, or mean value, of signal $x(t)$ and x^* represents the steady-state value of signal $x(t)$.

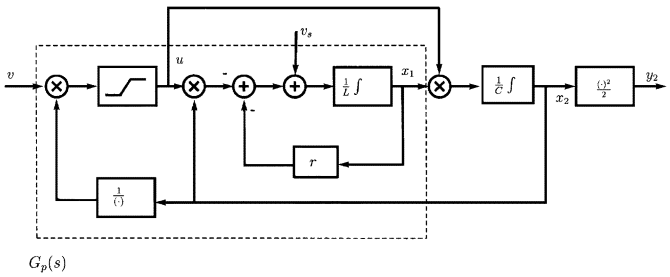

Fig. 2. System block diagram showing the linearizing change of variables.

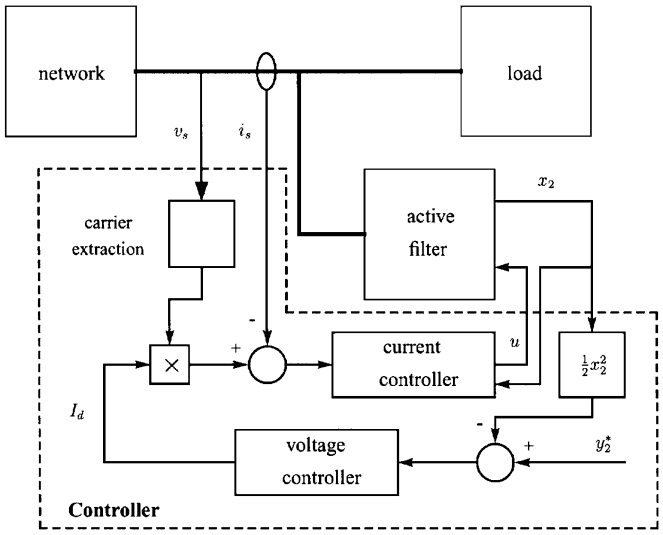

Fig. 3. Controller block diagram showing the current and voltage loops.

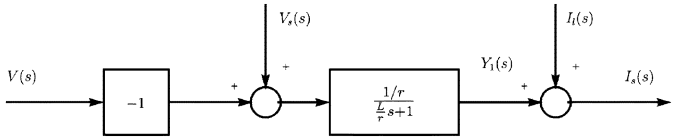

Fig. 4. Block diagram for (3).

where y_1, y_2 are the inductor current and the dc bus capacitor voltage squared and divided by 2, respectively. The new input variable for the plant is v. As can be observed, (3) is now linear in v and y_1 whereas (4) is not. Fig. 2 shows the system block diagram after applying the linearizing change of variables.

The proposed controller is composed of two digital control loops (Fig. 3). The inner loop is the current control loop. Its function is to shape the source current i_s into a sinusoidal in phase with the voltage source v_s. To this end, a current sensor is placed at the network terminals and this current is used as the feedback signal in the current control loop. It is worth mentioning that neither current sensors are necessary at the load terminals nor in the active filter inductor. In this case, the load current is seen as a disturbance signal for the source current control loop, as shown in Fig. 4. So, if the current control loop is properly designed to attenuate its output disturbance (in a sufficiently large frequency band) then the performance specification will be achieved in spite of the disturbance phase characteristic. However, this approach has a drawback, namely that the active filter and control loop dynamics affect the active power flow from the source to the load, and consequently, the outer voltage loop must

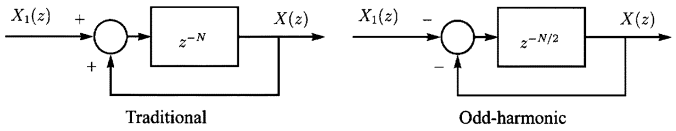

Fig. 5. Traditional and odd-harmonic repetitive basic cells.

be slightly faster in order to cope with this problem. The current control loop works at a sampling frequency $(F_s = 1/T_s)$ equal to the switching frequency of the active filter.

The outer control loop is the voltage loop. Its main function is to maintain the dc bus voltage close to the reference value in spite of load changes in the system. Since the inner current loop controls the source current and its reference is the output of the voltage controller multiplied by a sinusoidal carrier signal in phase with the source voltage, keeping the dc bus voltage close to the reference value can be seen as a way to ensure the power balance of the active filter and the load set. In this manner, it is not necessary to include in the control algorithm any active power calculation because maintaining the dc bus voltage level is equivalent to perform an active power balance for the whole system.

A. Current Loop

1) Equation Linealization: The continuous time transfer function that describes the unperturbed dynamic behavior of (3) is

$$G_p(s) = \frac{Y_1(s)}{V(s)} = \frac{\frac{-1}{r}}{\frac{L}{r}s + 1}. \tag{5}$$

In steady state, x_2 will be around V_d. Although (5) is independent of V_d, it is important to note that the control action, u, can only take values in $[-1, 1]$. As v is divided by x_2 to obtain u (Fig. 2), it is desirable that V_d is as high as possible since this will keep the control action far from saturation limits.

This transfer function is sampled with a zero-order hold at a sampling frequency equal to the switching frequency of the converter, resulting in $G_p(z)$. This function is then taken as a plant for the digital controller of the current loop.

2) Odd-Harmonic Repetitive Controller: Repetitive control consists in placing a basic cell into the loop (Fig. 5) which introduces infinite gain at a certain frequency and all its harmonics, including dc frequency. This basic cell is based on a positive feedback of a delay of $N \in \mathbb{N}$ sampling periods where $N = T_r/T_s$, T_r being the period of the periodic signal to be tracked or rejected and T_s the sampling period. It can be shown that this cell has poles at the desired frequencies [29]. Odd-harmonic repetitive control [28] is based on introducing a different cell (Fig. 5) which consists of a negative feedback of a delay of $N/2$ sampling periods. It can be proven that this cell has poles at fundamental frequency and its odd-harmonic frequencies [28]. As mentioned in Section I, this fact is of great interest for most power electronic systems.

Repetitive controllers are usually implemented in a "plug-in" fashion, i.e., the repetitive compensator is used to augment an existing nominal controller, $G_c(z)$ (Fig. 6). This nominal compensator is designed to stabilize the plant, $G_p(z)$, and provides disturbance attenuation across a broad frequency spectrum. This scheme was first introduced by Inoue *et al.* [29]. The controller is composed of the basic cell and a linear system $G_x(z)$ which is designed to ensure closed-loop stability. In practical implementations, a null-phase FIR low pass filter $F(z)$ is introduced into the basic cell in order to reduce gain at those frequencies where system behavior is not properly modeled. It is important to emphasize that the FIR filter $F(z)$ reduces the repetitive loop gain to finite values for all the frequencies, giving it a general low-pass shape. In order to obtain a stable closed-loop system, the sufficient conditions of Proposition 1 can be used.

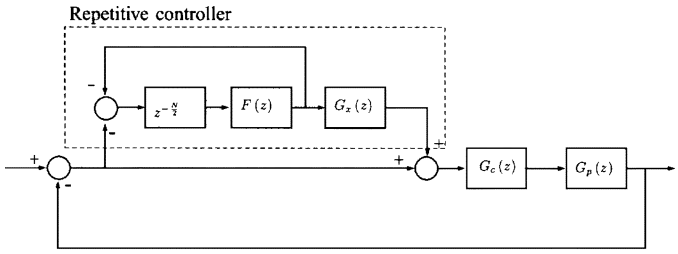

Fig. 6. Digital repetitive controller scheme for the source current (i_s) loop.

Proposition 1 ([28]): The closed-loop system of Fig. 6 is stable if the following conditions are fulfilled.

1) The closed loop system without the repetitive controller is stable, i.e., $G_o(z) = (G_c(z)\,G_p(z)/1 + G_c(z)\,G_p(z))$ is stable.
2) $\|F(z)\|_\infty < 1$.
3) $\|1 - G_o(z)\,G_x(z)\|_\infty < 1$, where G_x is a design filter to be chosen.

These conditions are fulfilled by a proper design of $G_c(z)$ and $G_x(z)$.

1) *Cond. 1*: It is advisable to design the controller $G_c(z)$ with a high enough robustness margin.
2) *Cond. 2*: There is no problem with the causality of $F(z)$ because it is series connected with the delay $z^{-(N/2)}$ and the repetitive loop will be executed as a whole in controller real-time operation.
3) *Cond. 3*: A trivial structure which is often used is [30]: $G_x(z) = k_r G_o(z)^{-1}$. This structure can only be used if G_o is a minimum-phase transfer function. Otherwise, other techniques should be applied in order to avoid closed-RHS plane zero-pole cancellations [30]. Moreover, as said before there is no problem with the no causality of $G_x(z)$.

   As argued in [31], k_r must be designed looking for a tradeoff between robustness and transient response.

B. Voltage Loop

1) Steady-State Behavior: In this section, the steady-state behavior is analyzed. Steady-state controls $I_d = I_d^*$ and $u = u^*(t)$ such that the specifications hold are assumed. Then, the dynamics of x_2 is proved to be periodic and the value of I_d^* is obtained. It will be assumed for x_1 to hold equation $x_1 = i_s^* - i_l = I_d^* \sin(\omega_r t) - i_l(t)$ throughout the section.

Proposition 2: Let $x_1 = i_s^* - i_l = I_d^* \sin(\omega_r t) - i_l(t)$ where $i_l(t)$ is a periodic signal with period $T_r = 2\pi/\omega_r$; then

$$\begin{aligned} Cy_2\big|_{t_0}^{t_0+T_r} &= \frac{Cx_2^2}{2}\bigg|_{t_0}^{t_0+T_r} \\ &= \int_{t_0}^{t_0+T_r} E\sin(\omega_r t)(I_d^*\sin(\omega_r t) - i_l(t))dt \\ &\quad - \int_{t_0}^{t_0+T_r} r(I_d^*\sin(\omega_r t) - i_l(t))^2 dt. \end{aligned}$$

Proof: Solving for ux_2 in (1) yields

$$ux_2 = v_s(t) - L\frac{dx_1}{dt} - rx_1$$

then

$$\frac{Cx_2 dx_2}{dt} = x_2 u x_1 = \left(v_s(t) - L\frac{dx_1}{dt} - rx_1\right)x_1.$$

Integrating the latter equation in $[t_0, t_0 + T_r]$ and noting that $v_s = E\sin(\omega_r t)$ and that x_1 is T_r-periodic, the result is obtained. ∎

Proposition 3: The following statements are equivalent.

1) $x_2(t)$ is T_r-periodic.
2) $\int_{t_0}^{t_0+T_r} E\sin(\omega_r t)(I_d^*\sin(\omega_r t) - i_l(t))dt - \int_{t_0}^{t_0+T_r} r(I_d^*\sin(\omega_r t) - i_l(t))^2 dt = 0.$
3) $x_2((k+1)T_r) = x_2(kT_r)$.

Proof: It is straightforward from the previous proposition. ∎

As a conclusion, let us assume control inputs u and I_d such that x_1 converges to $I_d^*\sin(\omega_r t) - i_l(t)$ and $\langle x_2\rangle_0 = x_2^*$. Then I_d converges to I_d^* which in turn satisfies

$$\int_{t_0}^{t_0+T_r} E\sin(\omega_r t)(I_d^*\sin(\omega_r t) - i_l(t))dt - \int_{t_0}^{t_0+T_r} r(I_d^*\sin(\omega_r t) - i_l(t))^2 dt = 0$$

and x_2 converges to a periodic function of the same fundamental frequency as x_1.

2) Voltage Controller: Assuming the system is in steady state, the net current will have the following shape:

$$x_1(t) = I_d\sin(\omega_r t) - \underbrace{\sum_{l=1,l\ \text{odd}}^{\infty}(a_l\cos(l\omega_r t) + b_l\sin(l\omega_r t))}_{i_{load}} \tag{6}$$

where a_l and b_l are the load current Fourier series coefficients. By applying proposition 2 and (6), one can obtain the following expression:

$$y_2\big|_{kT_r}^{(k+1)T_r} = -\frac{rT_r}{2C}\left[\left(I_d^k - b_1\right)^2 + \sum_{l=1,l\ \text{odd}}^{\infty} a_l^2 + b_l^2\right] + \frac{ET_r}{2C}\left(I_d^k - b_1\right) \tag{7}$$

where I_d^k stands for the desired net current amplitude in period k. This equation can be interpreted in terms of a discrete time integrator, with T_r as sampling time, which has two inputs, one which is nonlinear in I_d^k, a_l and b_l, and another which is linear in I_d^k and b_1 (Fig. 7). This nonlinear discrete time system can

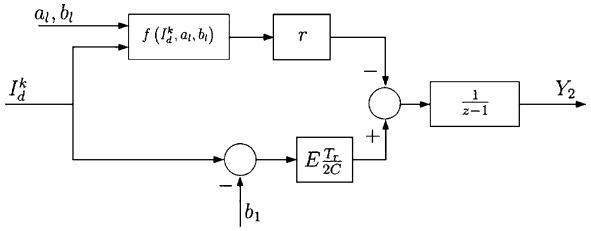

Fig. 7. Complete 50 Hz block diagram of voltage dynamics.

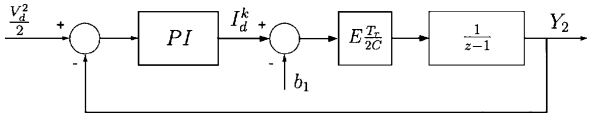

Fig. 8. simplified 50 Hz model with PI controller.

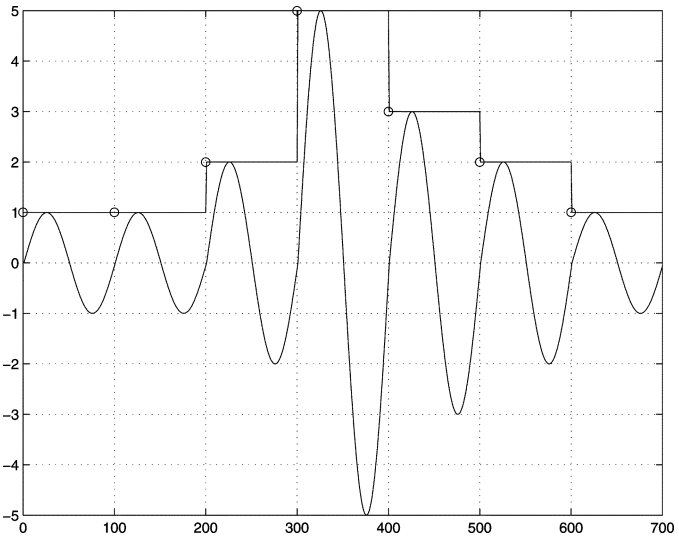

Fig. 9. AM modulator input and output signals (synchronized operation).

be linearized by introducing a new control variable J_d^k which relates to I_d^k in the following way :

$$I_d^k = \frac{E + 2b_1}{2r} \pm \sqrt{b_1^2 + \frac{E^2}{4r^2} - \frac{2CJ_d^k}{rT_r} - \sum_{\substack{l=1\\ l\ \text{odd}}}^{\infty}(a_l^2 + b_l^2)}. \tag{8}$$

Once this variable change is applied, a new linear system is obtained

$$\frac{Y_2(z)}{J_d(z)} = \frac{1}{z-1}. \tag{9}$$

Unfortunately, (8) depends on the load current Fourier coefficients, which are usually unknown.

It is important to note that higher harmonics do not contribute to the variations in voltage although they introduce energy losses due to Joule's effect.

For simplicity let us take $r = 0$ in the practical development of the voltage controller. Under this assumption the relation between Y_2 and I_d can be stated as

$$C(z-1)Y_2(z) = \frac{ET_r}{2}\left(I_d(z) - b_1\right).$$

As the value of b_1 is usually unknown but constant in steady state, it can be considered as a step disturbance in the

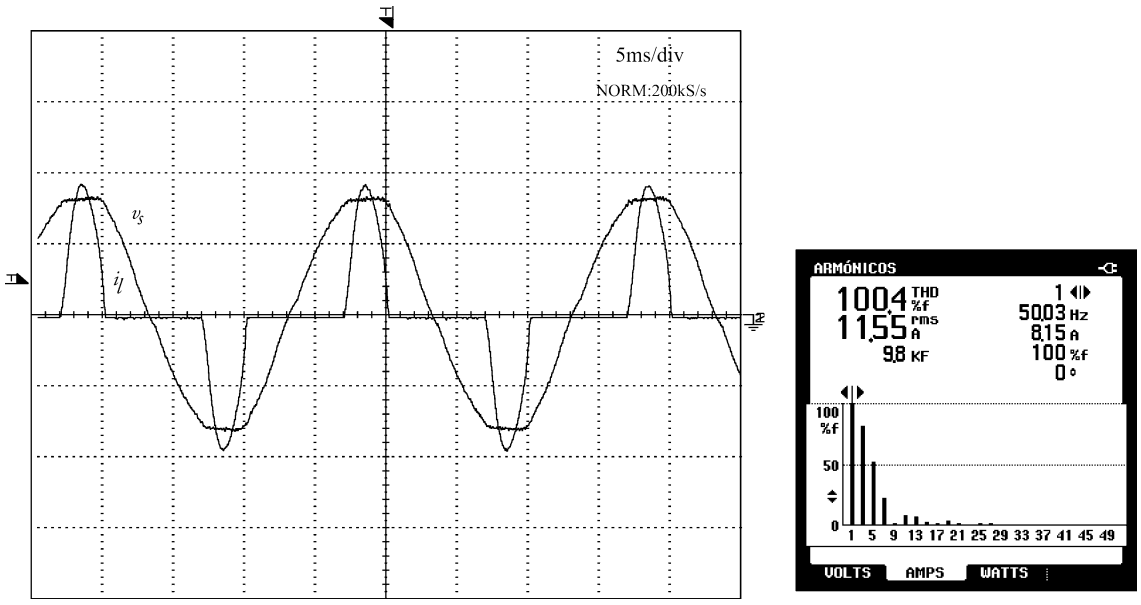

Fig. 10. Non-linear load: ac mains voltage (v_s) and nonlinear load current (i_l) (180 V/div and 15 A/div, respectively) (top) and harmonic content of nonlinear load current (bottom).

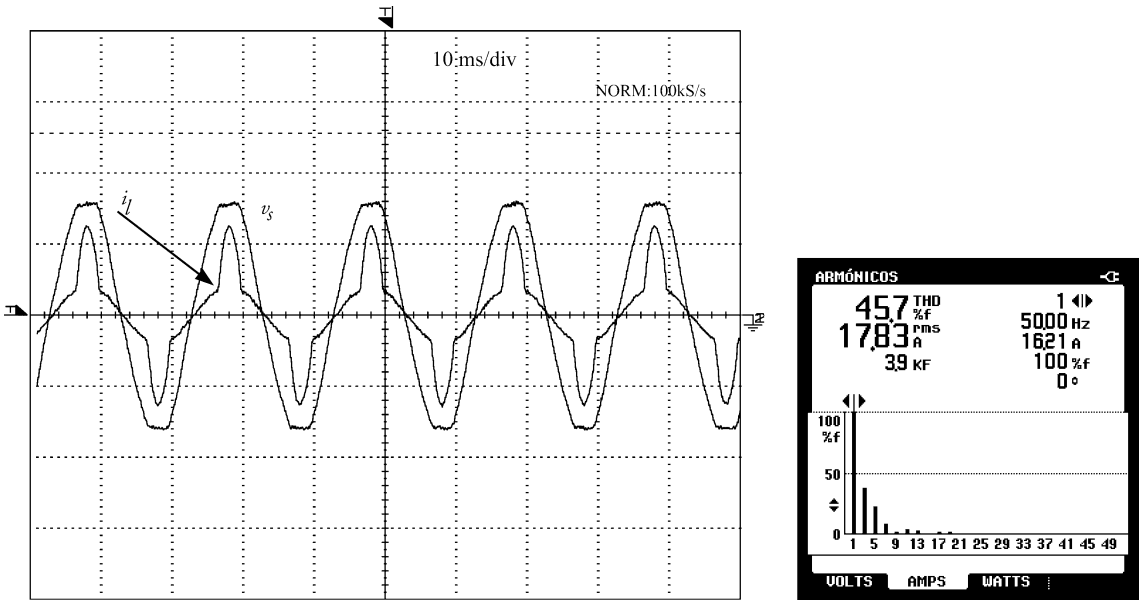

Fig. 11. Mixed linear and nonlinear load: ac mains voltage (v_s) and nonlinear load current (i_l) (180 V/div and 15 A/div, respectively) (top) and harmonic content of nonlinear load current (bottom).

closed-loop system (see Fig. 8). Thus, a classical PI controller will regulate y_2 to the desired value y_2^* without steady-state error, i.e.,

$$I_d(z) = k_p(Y_2^*(z) - Y_2(z)) + k_I \frac{z+1}{z-1}(Y_2^*(z) - Y_2(z)).$$

The losses in the inductor, represented by $r \neq 0$, can be considered as an additive complex-dynamics disturbance in the voltage closed-loop system. However, as the experimental results will show, it is not worth taking these losses into account in the design of the voltage loop.

In order to reduce high frequency disturbances in the whole control system, the outer discrete-time voltage loop has its sampling time (T_r) synchronized with the positive derivative zero crossing of the carrier signal. Thus, the current reference signal of the inner loop changes its amplitude I_d maintaining the sinusoidal shape within the natural period of the signal. Fig. 9 shows the input and the output of the AM modulator: the input signal (I_d) has the same period as the carrier signal, and is synchronized with the carrier.

It is important to emphasize that although the voltage is kept under control at sampling instants, it presents oscillations within each sampling period (period T_r). In steady state, these oscillations could be analyzed from (4) under zero dynamics conditions, i.e., under strict compliance of control objectives. Unfortunately, this analysis depends on the load current harmonic content which, a priori, is not known. Obviously, the amplitude of the intra-sample oscillations is proportional to

$1/C$. Therefore, from a practical point of view, this amplitude can be reduced by using a bigger capacitor if it pose a problem.

The multiloop discrete-time controller developed in this work is designed in an outward way: first, the inner current loop with fast dynamic response (large bandwidth, high sampling rate) and second, the outer voltage loop with slow dynamic response (small bandwidth, low sampling rate). This approach assumes a decoupling in response time between the two loops in the sense that larger is better. Moreover, the design of the outer loop assumes a perfect behavior for the inner loop. Obviously, in spite of the good behavior of the current loop, this assumption is only approximate. Nevertheless, the experimental results confirm the goodness of this control engineering design methodology.

IV. Experimental Setup

The experimental setup used to test the designed controller has the following parts.

1) Active filter: full-bridge boost converter with IGBT switches (nominal current 100 A) and the following parameters: $r = 0.034\ \Omega$, $L = 1$ mH, $C = 6600\ \mu$F. The switching frequency of the converter is 20 kHz and a synchronous centered-pulse single-update pulse-width modulation strategy is used to map the controller's output to the IGBT gate signals.

   In this work, the plant $G_p(z)$ has no zeros and the designed controller $G_c(z)$ is a minimum-phase first order lag controller, specifically $G_c(z) = -(0.0135z - 0.01/z - 0.905)$. Then, the closed-loop function $G_o(z)$ is a minimum-phase function and there is no problem choosing $G_x(z) = k_r G_o(z)^{-1}$. The assigned value for k_r is 0.2 and the null-phase low-pass FIR filter selected is $F(z) = (1/4)z + (1/2) + (1/4)z^{-1}$.
2) Rectifier (nonlinear load): full-wave diode rectifier with $C = 1500\ \mu$F. The active power with nominal dc resistor is $P = 1.81$ kW, its reactive power is approximately zero and its power factor (PF) is equal to 0.68. The rectifier also includes an inductor (0.2 mH) in its ac side to limit the derivative of its input current. Fig. 10 shows the shape of the ac mains voltage and current, and the harmonic content of the input current for the rectifier with nominal dc resistor. It is worth noting to remark that the total harmonic distortion[3] (THD) of this current is about 100% and its maximum derivative is about 80 kA/s.
3) Linear load: resistive load of 1.9 kW in parallel connection with the nonlinear load. Fig. 11 shows the same information as Fig. 10 but with the resistive load connected in parallel with the rectifier to make up a mixed load.
4) Analog circuitry of feedback channels: the ac mains voltage, ac mains current and dc bus voltage are sensed with a voltage transformer, a hall-effect sensor and an isolation amplifier, respectively. All the signals from the sensors pass through the corresponding gain conditioning stages to adapt their values to A/D converter input taking advantage of their full dynamic range. In addition, the three feedback channels include a first order low-pass filter with unity dc gain and 4.3 kHz cutoff frequency[4].
5) Control hardware and DSP implementation: the control board has been internally developed and is based on an ADSP-21 161 floating-point DSP processor with an ADMC-200 that acts as coprocessor, both from Analog Devices. The ADMC-200 deals with the PWM generation and the A/D conversions.

   The sampling rate of the A/D channels and the current loop is $F_s = 20$ kHz, the same as the switching frequency of the active filter. The voltage loop is operated at 50 Hz sampling rate. Because the sampling rate of the ac mains voltage and current is the same as the converter switching frequency, some aliasing problems can arise. Particularly, the switching ripple appears as a dc component on the discrete-time side (after A/D conversion). This fact has proved especially critical in ac mains voltage sensing because this signal is used as the carrier signal in the controller. To solve this problem, the sampled ac voltage is passed through a parametric equalizer filter that includes a zero in $z = 1$ to reject the dc component of the signal, in steady-state. In the ac mains current, the problem is not so important because the open-loop dc gain is low, and then the current loop is hardly affected by the fictitious current dc component.

   The controller and its related code (communications, alarm supervision, data collection routines, etc.) are coded in C programming language without an underlying real-time operating system. Only a few of the lowest level procedures are coded in assembler for efficiency reasons. The available computing power of the DSP processor allows the controller operations to be calculated in about one half of the current loop sampling period. Thus, it is only necessary to force one period of computing delay and, in any case, this delay would be necessary owing to hardware peculiarities. It is worth noting that the one-period computing delay has been included in the plant model $G_p(z)$ to take it into account in the controller design process.
6) The nominal RMS ac mains voltage is $V_s = 220$ V RMS and its nominal frequency is 50 Hz.

V. Experimental Results

This section shows some of the experimental results obtained with the active filter and the designed digital controller. The results are presented through oscilloscope and power analyzer screen dumps of the ac mains electrical variables and, when it would be necessary, the active filter dc bus voltage. Table I summarizes the total harmonic distortion (THD) and RMS values of the source current for the used benchmark loads. It is important to remark that the active filter can, in all cases, nearly compensate all the distorted (nonfundamental frequency components)

[3]In this work the THD figures and the harmonic content are always taken with respect to the fundamental harmonic (50 Hz) and they have been obtained using a Power Quality Analyzer Fluke 43 instrument.

[4]The oscilloscope screens in the figures of this section and the following show the voltages and currents after the corresponding low-pass filters.

TABLE I
SOURCE CURRENTS AND CORRESPONDING THD VALUES FOR THE NONLINEAR AND MIXED LINEAR-NONLINEAR LOADS WITH AND WITHOUT THE ACTIVE FILTER

	without active filter		with active filter	
Load	i_s (A)	THD (% fund.)	i_s (A)	THD (% fund.)
Nonlinear	11.55	100.4	9.09	0.5
Mixed	17.83	45.7	17.38	0.3

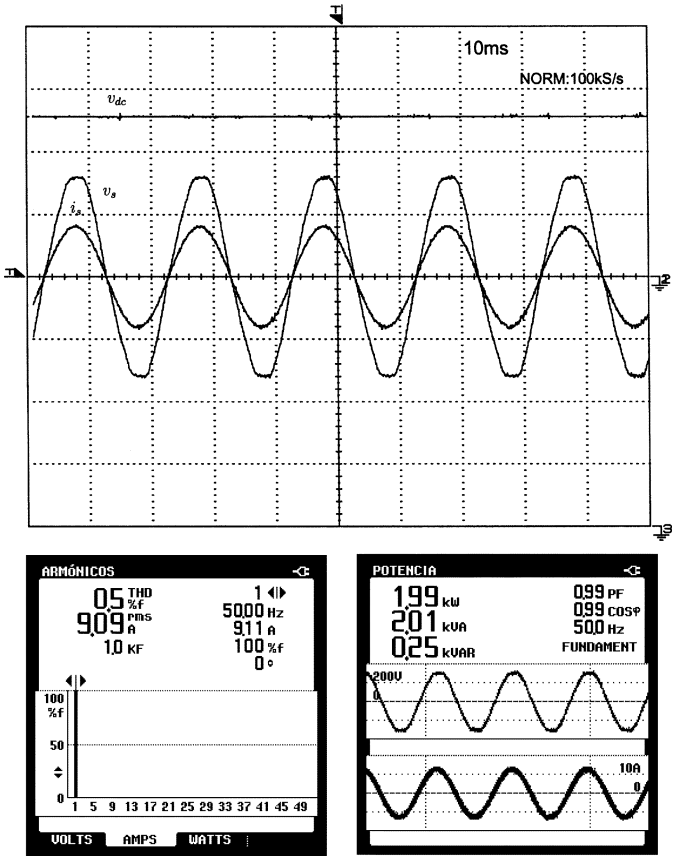

Fig. 12. Full nonlinear load: source voltage (v_s) and current (i_s), and dc bus voltage (v_{dc}) (180 V/div, 15 A/div and 65 V/div, respectively) (top); harmonic content and total harmonic distortion for source current (i_s) (bottom, left); active and reactive power and power factor in the ac mains (bottom, right).

and reactive parts of the load current. Thus, the source current appears in phase with source voltage giving a power factor close to one.

Apart from the experiments collected in this section, a lot of numerical simulations, including mainly capacitive or inductive loads, have been carried out showing the same good performance. Also, it is worth noting that several numerical simulations including loads that work as generators at some time periods[5] (thus imposing a negative active power flow to the source) have been carried out without problems. The voltage loop of the overall controller assures the active power balance and, after a transient, the current loop input is negative giving a current reference shifted π rad from the source voltage that the current loop tracks without difficulty.

[5]This problem was established as a hard one by Depenbrock and Staudt [32].

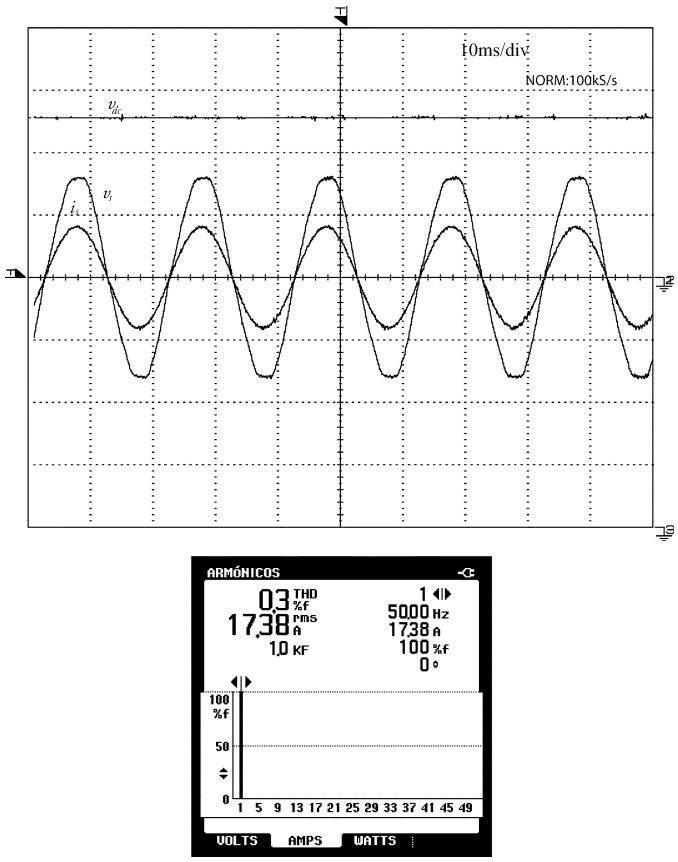

Fig. 13. Mixed linear and nonlinear full load: source voltage (v_s) and current (i_s), and dc bus voltage (v_{dc}) (180 V/div, 30 A/div and 65 V/div, respectively) (top); harmonic content and total harmonic distortion for source current (i_s) (bottom).

A. Single-Phase Nonlinear Load

This subsection presents some experimental results for the active filter working to compensate the rectifier load. Fig. 12 shows the source voltage and current, and the dc bus voltage in steady-state. It is important to stress the obtained figure for the ac mains current THD, 0.5%, because it is lower than the THD of the ac mains voltage, which is made possible by introducing a digital parametric equalizer filter in the source voltage feedback channel. This filter only outputs the fundamental component of the voltage, which is then used as a carrier signal to build the reference current for the current control loop.

The dc bus voltage tracks the reference value of 425 V with a small ripple around it of about ± 4 V. This ripple can not be seen in Fig. 12 because of the used scale.

B. Single-Phase Mixed Linear and Nonlinear Load

In this experiment, the resistive load is connected in parallel with the rectifier, thus doubling the active power of the load. Fig. 13 shows the shape of the ac mains current and its harmonic content, where it can be seen that the higher order harmonics are virtually zero. The THD for the current has a lower value, 0.3%, than in the previous case owing to the fact that its RMS value is higher; hence, the current switching ripple is comparatively lower.

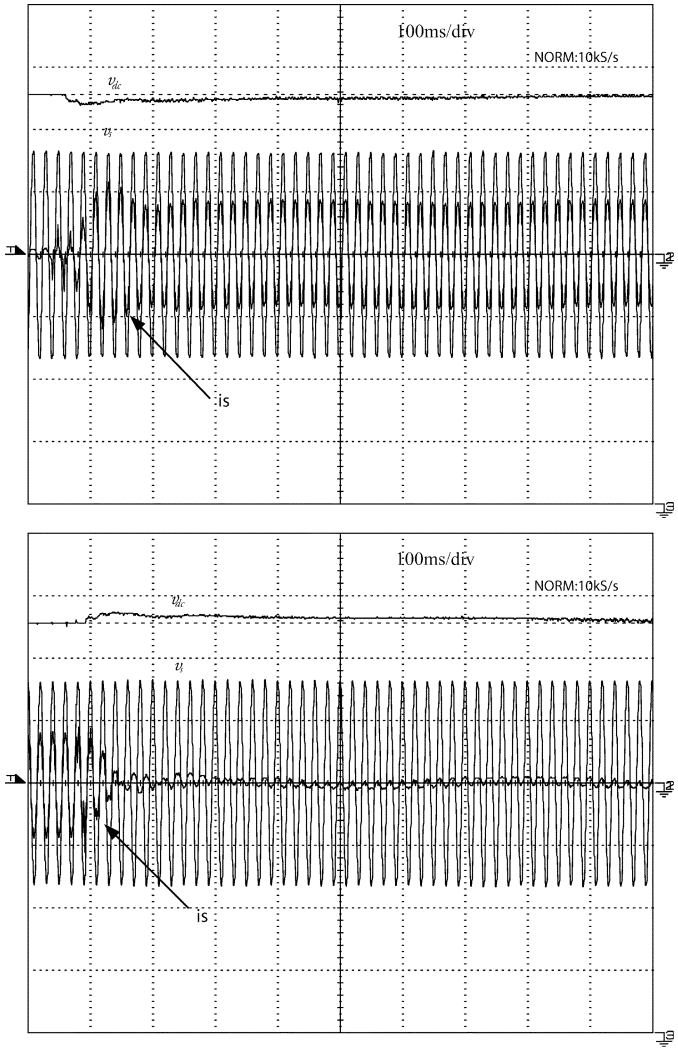

Fig. 14. Source voltage (v_s) and current (i_s), and dc bus voltage (v_{dc}) (180 V/div, 15 A/div and 65 V/div, respectively): from no-load to full nonlinear load (top) and from full nonlinear load to no-load (bottom).

C. Non-Linear Load Variations

This section presents the results for the following experiments:

1) the full nonlinear load is applied to the network with the active filter in operation (Fig. 14, top);
2) the full nonlinear load is disconnected from the ac mains with the active filter in operation (Fig. 14, bottom).

In each case, the overshoot in the dc bus voltage is under 4%; there is therefore no problem with the maximum load variations expected in the system. The mean-value low-frequency oscillations that appear in the mains current are not present in the real current signal. These oscillations arise from the aliasing of the switching ripple (20 kHz fundamental) because the oscilloscope sampling frequency for this time base is only 10 kHz.

VI. Conclusion

The paper shows the design of an all-digital controller for a parallel single-phase active filter. The inner current control loop is designed using a digital repetitive control approach that, as the experimental results show, perfectly shapes the source current. The high loop gain injected by the repetitive controller at the fundamental and harmonic frequencies of the network frequency ensures good tracking of the reference current and the rejection of the high order harmonics of the load current. It is worth emphasizing that, because the current sensor has been placed on the network side, the control problem for the current loop can be discussed from a disturbance rejection point of view. In addition, the external slow dynamics voltage loop ensures the active power balance of the whole system, adequately rejecting the load variations and providing the inner current control loop with the correct current RMS reference.

As future work, the transient behavior, or rather, the stability of the two-loop controller and the system should be theoretically studied to guarantee the performance experimentally proved. Moreover, it would be interesting to characterize the dc bus voltage oscillations that appear during the controlled-system operation in order to set the dc-bus capacitor to the lowest value without removing the system from its working range.

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