VOLTAGE FLUCTUATIONS IN IC POWER SUPPLY DISTRIBUTION NETWORKS: IMPACT ON DIGITAL PROCESSING SYSTEMS

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Abstract— *The supply voltage decrease and power consumption increase of modern ICs made the requirements for low voltage fluctuation caused by packaging and on-chip parasitic impedances more difficult to achieve. Most of the research works on the area assume that all the nodes of the chip are fed at the same voltage, in such a way that the main cause of disturbance or fluctuation is the parasitic impedance of packaging. In the paper an approach to analyze the effect of high and fast current demands on the on-chip power supply network. First an approach to model the entire network by considering a homogeneous conductive foil is presented. The modification of the timing parameters of flip-flops caused by spatial voltage drops through the IC surface are also investigated.*

Index Terms— *CMOS, integrated circuits ground bounce, power supply voltage fluctuations, noise, digital circuit performances.*

I. INTRODUCTION

Due to the rapid progress of both the electronic technology and the manufacturing semiconductor industry the requirements are becoming harder to achieve in the design and manufacturing of modern integrated circuits. CMOS digital systems evolution is characterized by a continuous increment of transistor count, shifting from hundreds to thousands of million transistors and with a prediction of following the same trend of device increase next decade (Moore's Law).

Along with the reduction of the device critical dimensions, the power supply voltage level has been reduced achieving 1V and even lower levels. The increased complexity causes an increase in the power consumption, a key problem for modern circuits due to both silicon temperature (forcing an efficient heat removal), and battery life requirements. But the noise has kept the same level making its influence on power supply voltage greater and more difficult to compensate its effects. The consequence is the need to deliver to the circuits and subsections of the system a clean and sufficient levels of energy characterized by a regulated voltage level and an abrupt shape of current requirements, all this at the very high frequency devices works.

The parasitic impedance of the real packages and the internal power supply delivery network cause fluctuations in the power supply voltages, causing perturbations into the digital circuits performance, mainly severe deviations from the nominal delay. This is one crucial problem for both technology and designers in modern systems. To deal with the impact and cost of ground bounce and power supply fluctuations is one of the most active topics currently addressed by researchers [1, 2].

Typically, in many of these research works the mechanism of the voltage fluctuations is modeled by the use of a lumped and uni-dimensional serial electric circuit as shown in Fig. 1, taken from [3]. The V_{DD} power supply package pins are modeled by an inductance and a serial resistance together with a parasitic capacitance, all lumped components. Later, the power lines are applied to the digital cells with the consideration of a parasitic resistance for the distribution network and a capacitor resulting from the parasitic and on-chip decoupling capacitances. This model explains in a first approach the two components of the voltage fluctuations: the *IR* drop caused by the current flow through the parasitic resistance of both package and power supply network and the *LdI/dt* component caused by the voltage drops in the package inductance due to the sharp and abrupt shape of the CMOS digital circuit current.

From the lumped model it could be derived that the V_{DD} and GND rails are equipotential for all the cells of the circuit. However, the real picture of the power structure clearly gives a different result. The distribution network is composed by a given number of crossed bars in one or two levels of metal, usually the upper levels, with delivering points of power supply at the crosses. The V_{DD} (and GND) level is applied to the network from a large amount of V_{DD} and GND pins located all around the package. For fast and non-homogeneous current demands both *resistive and inductive drops* inside the chip distribution network could appear caused by the distributed resistance and inductance of the network, causing the appearance of voltage drops through it ($\Delta V(x,y,t)$) and consequently through the logic system. The analysis of the voltage drop due to the distributed elements and its effects on data transmission and storing in memory elements is the objective of this work.

In this work we face the problem in two steps. First we model the *RI* and *LdI/dt* voltage drops in the internal power supply distribution network. In order to consider a general result, far from the casuistic details of real power distribution networks, we consider the network composed by two (V_{DD} and GND) foils with the area of the entire chip. In the second part of the work we present simulation results for the observation of the effect of internal voltage drops in the bus structure connecting two separated cores or functional units.

The paper is organized as follows. Section II addresses the modeling of the power supply network as a conductive

foil analyzing the resistive distribution and the effects when it is considered as a two-dimensional transmission line. In section III results of the effect of the spatial differential voltages caused in simple interconnection line connecting two distant built-in cores. Finally, section IV presents the conclusions.

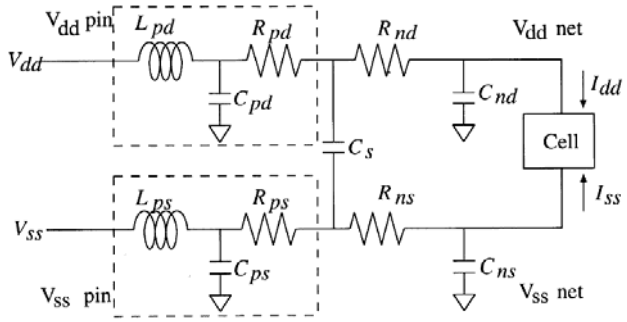

Fig. 1 Simplified model for the voltage fluctuation mechanism [3].

II. Modeling of the Power Supply Network as a Conductive Foil

Power supply networks may be considered as electromagnetic resonant cavities. Several works have the objective to model this structure [4,5,6,7,8]. The structure is formed by a finite set of lines crossing long and wide the chip and located in the upper levels of metal. Different works analyze design methodologies to deal with a good power distribution where the variables are the number of rails and its width for a given distributed current load, a distribution of capacitances and certain limiting drop requirements. In this work we try to get knowledge avoid considering the structure of the crossbars in detail assuming a generic structure. We consider the power distribution network as a single conductive foil, where the resistivity and the dielectric constant as well as the dimensions of the foils (the chip) determine the resistance distribution and the resonant frequencies (Fig. 2).

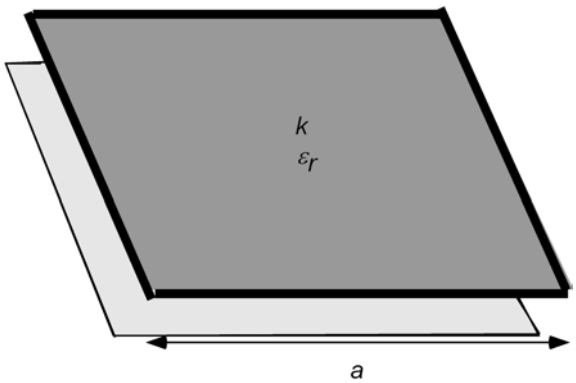

Fig. 2. Modeling of the power supply distribution network as a homogeneous conductive foil characterized by a sheet resistance and a dielectric constant.

II.1 Resistive behavior of the network.

Let us consider an isotropic and homogeneous conductive foil with a given *k* sheet resistance (Fig.2). A precedent of this models, considering only the resistive behavior, was investigated by Meindl in [4] where they present an accurate IR drop model by using Poisson equation resolution through finite elements techniques.

We evaluate the resistance distribution of the surface of the foil when all the contours are connected to GND (it is an optimistic assumption that allow a simple analytical solution). The approximation we follow allows an analytical expression that is the result of equation:

$$R(x,y) = 1/S(x,y) = 1/\left[\oint \frac{dl}{k \cdot r(x,y)}\right] \qquad (1)$$

where *R* is the distributed resistive function, *S* the distribution conductive function, *k* the sheet resistance and *r(x,y)* the distance between *(x,y)*, and the perimeter *dl*, the integration is made around all the perimeter of the chip.

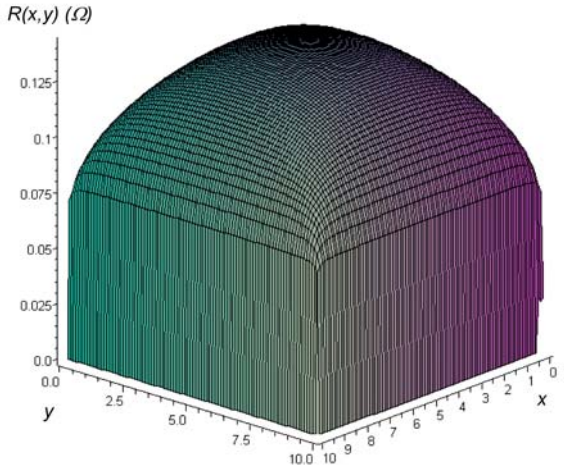

Fig. 3. Resistive distribution in the foil *R(x,y)*, when all the border is connected to ground.

The result is shown in Fig. 3, for a squared foil which sides (*a*) are 10 arbitrary units long and an unitary sheet resistance (*k=1Ω*). The resistance variation (fluctuation) in the flat part of the foil is around 0.06Ω. In [5] the authors analyze through experiments with real devices the voltage drop distribution for a PowerPC microprocessor, giving a maximum voltage variation of 100 mV at the center of the foil for a total current of 10 A, which corroborates the previous result.

II.2 Loss-less electromagnetic resonant network

The power distribution network, modeled as a conductive foil with a relative dielectric constant ε_r can be considered as an electromagnetic bidimensional structure characterized by the wave equation:

$$\frac{\partial^2 v}{\partial x^2}+\frac{\partial^2 v}{\partial y^2}=\frac{1}{c}\frac{\partial^2 v}{\partial t^2} \qquad (2)$$

Where c is the wave propagation velocity, that for the present case is given by:

$$c = c_0 / \sqrt{\varepsilon_r} \approx 0.5 c_0 \qquad (3)$$

where c_0 corresponds to the speed of light in the vacuum and a value of 3.9 was considered for ε_r. The distribution network, when excited at the resonant frequencies, causes a significant amount of noise, caused by standing waves. These resonant frequencies are determined by the mode number of the propagation wave (m,n), the dielectric constant and the physical size of the foil (squared, edge a). The resonant frequencies are given by:

$$f_r(m,n) = \frac{c}{2a}\sqrt{(m^2+n^2)} \qquad (4)$$

Table 1 shows the resonant frequencies for a set of propagation modes:

TABLE 1 Resonant frequencies (a=1 cm)

m	*n*	*fr(GHz)*	*λ(mm)*
1	1	10	14
2	1	16.7	8.8
2	2	21.2	7
3	3	31.8	4.7
3	2	27	5.54
3	1	23.7	6.2
4	4	42.4	3.52
4	3	37.5	4
4	2	33.5	4.46

For real cases the bonding inductances, the number of bonding pads and the on-chip decoupling capacitors are large and the impact on field distribution and resonant frequencies are minimal. So, the previous frequencies given for the foil model are acceptably accurate for real circuits. The amplitude of the resonant voltage wave is dictated by the losses of the foil. Usually radiation and dielectric losses can be neglected and the main reason for losses is the foil conduction losses. Fig. 4 shows a simulated view of the resonance effect for a case where modes (4,4) and (1,1) predominate the propagation (case of 2x2 cores), the boundary conditions for the perimeter of the foil are that the borders are connected to ground. Observe how it is possible to have peaks and valleys for distant points, and this is the case of the launching and receiving flip-flops of a single line bus between two cores in a 2x2 cores structure. In the case of the voltage distribution shown in Fig. 4 the maximum peak has an amplitude of 40 mV.

Effect of spatial voltage drops into the parameters of a single bit communication bus

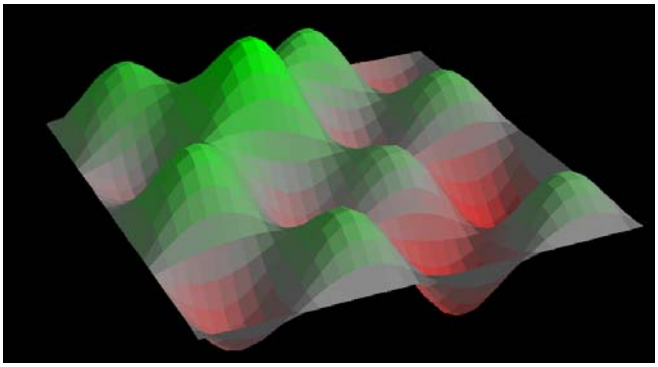

Fig. 4. Simulated voltage distribution for a resonance with (1,1) and (4,4) propagation modes.

In the previous section we have shown that spatial voltage drops may appear in the voltage power supply network of digital circuits. For short radius dominions, like functional units or even small cores the spatial voltage fluctuations may be considered negligible. This is the typical assumption in most of the research works [9,10,11,12], the voltage fluctuations are equipotential to all the digital devices of the IC. This means they consider voltage fluctuation in time, but not in space. However, from the previous section results, this assumption may not be acceptable for distant points, like, as a matter of example, the case of the two flip-flops (the emitter or launching flip-flop and the receiving flip-flop) of a bus line connecting two different and distant cores or entities with a high and fast current demand. In this paper our objective is to analyze the effect of a spatial drop (V_{DD1} for core1 and V_{DD2} for core2, see Fig. 5) in a single bit bus communication. We show the effects of the spatial drop through electrical simulations on circuits and devices of a 90nm technology. We consider moderate drop levels, understanding moderate as lower than the threshold voltages of the technology devices, in the sense that we will not observe level failures but only time delay fluctuations. In this paper we present the effect of a given pseudo-static spatial drop (V_{DD2}-V_{DD1}=ΔV_{DD}) on the propagation and setup values for flip-flops not considering, just to simplify and focus the attention on the considered problem, the propagation time through the bus line wire, just to simplify and focus the attention on the considered problem.

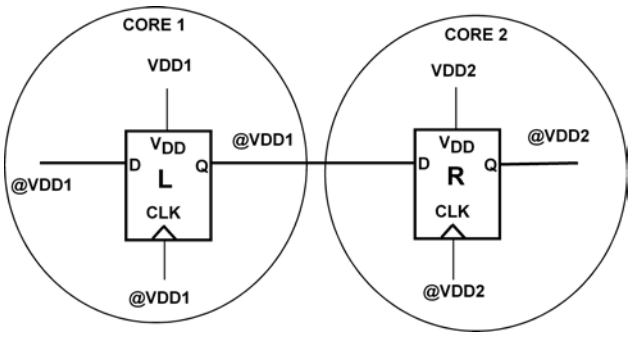

Fig. 5. The experiment: a single bit communication bus between two distant cores under differents supply voltage dominions.

To address this problem we proceed to analyze the problem in three phases: First we analyze the effect of V_{DD} fluctuations on a flip-flop (flip-flop R in Fig. 5), affecting

all power lines, input data and clock, on the propagation and setup time of the device. The second experiment presents the effect of voltage fluctuations only on the data input (D) of the flip-flop. And finally we consider the two effects combined which is the general case (flip-flop R working at V_{DD2} levels and data input coming from core1 working at V_{DD1} level). We consider a nominal voltage of V_{DD}= 1V and analyze the effect on delay time for a range of ± 0.4V, which is larger than the expected fluctuations, but is helpful to give a better idea about the parameters tendency.

III.1 Effect of fluctuations on the voltage level of all the flip-flop inputs.

The V_{DD} levels in all the flip-flop inputs (power line, D input and clock input) severely affect the device timing response of the device [11,12]. An increase of V_{DD} produces an increase of the driving voltage (V_{DD}-V_t) while the load capacitances are practically not affected. Therefore the charging and discharging time of loads by transistors is reduced and consequently the propagation time of any logic device is lower. The flip-flop is composed by two latches, each one of them by inverters driven by data levels, and a known structure of serial and feed backed transmission gates actuated by clock levels. An increase of V_{DD} reduces the propagation and setup time (time required to stabilize internal nodes for an input data change). A flip-flop circuit taken from the standard cell library of a 0.35 µm technology is analyzed, and from HSpice simulations its timing parameters are obtained. The propagation time is defined as the time between 50% of signal clock level (falling edge activation) and the 50% of the flip-flop data output (Q) level. The setup time is obtained as the time a data has to be stabilized before clock edge in order to get a sure writing process. Fig. 6 shows the results.

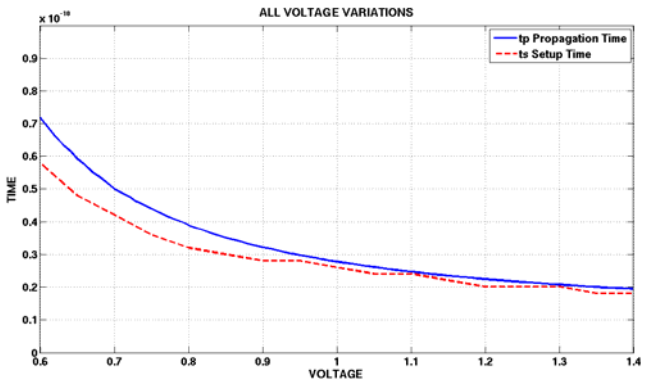

Fig. 6. Variations of propagation time (blue continuous line) and setup time (red-dotted line) for V_{DD} fluctuations.

Observe that a 40% of variation of the voltage may produce a 100% on the propagation and setup time, so the effect is worth enough to be taken into account. Observe that the propagation and setup times variations are proportional between them, so, general time parameter can be considered as affected by a factor $(1+f(\Delta V_{DD}))$ [9], where f is a non-linear function of the ΔV_{DD} level following Fig. 6.

$$t_{propagation}=t_{propagation0}\,(1+f(\Delta V_{DD})) \quad (5)$$

$$t_{setup}=t_{setup0}\,(1+f\,(\Delta V_{DD})) \quad (6)$$

III.2 Effect of input data voltage level on flip-flop delay.

In the previous section we have considered that all the voltage levels change equally. However, the problem stated in Fig. 5 has a different voltage in data input D of flip-flop R (the level is given by core1 that is V_{DD1}). In this section we consider the effect of a fluctuation on D input of a flip-flop when the rest of the inputs (power line and clock) are kept at a constant voltage. As we have mentioned in the previous section the clock signal voltage level affects the propagation of the input/latched data to the intermediate/output node of the latch. Because input data (with a voltage fluctuation) is considered stabilized before the clock edge (satisfying setup requirements) it can be derived that fluctuations on the input data node (D) do not affect the propagation time (time from clock to output).

A very different situation applies to the setup time, the required to get a correct latching of the first section. The time the input data axis (usually two inverters) needs to get a stabilized level to the latch out level is dependent of the level of the input (transistor gates) D. So, it is expected an impact on the setup time of the same level that the one shown in Fig. 6. Fig. 7 shows the experimental results using HSpice simulations. Effectively the propagation time practically kept invariant while the setup is severely affected.

The setup time in the case of the D input level fluctuation can be given by:

$$t_{setup}=t_{setup0}\,(1+g(\Delta V_{DD})) \quad (7)$$

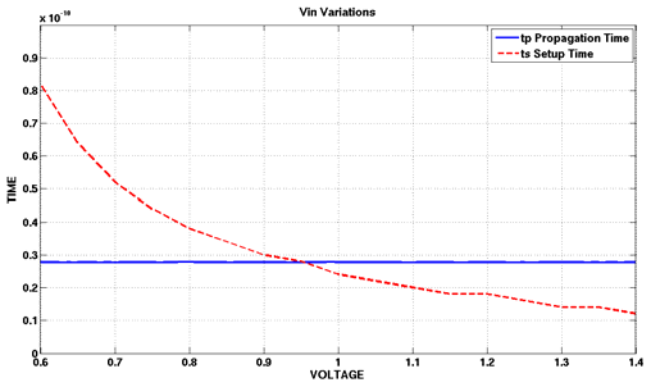

Fig. 7. Variations of propagation time (blue continuous line) and setup time (red-dotted line) for input D voltage level fluctuations.

III.3 Spatial voltage fluctuation on a flip-flop.

In this section we show the complete effect voltage drop between core1 and core2 (Fig. 5) on a data launching/receiving bit bus. For the propagation time, a power supply voltage (let's say $\Delta V_{DD2}>\Delta V_{DD1}$, in reference to the nominal value) cause a reduction of the propagation time in flip-flop R. Because the voltage drop in data input respect V_{DD2} (ΔV_{DD2}-ΔV_{DD1}=ΔV_{DD}) does not affect the propagation time (section III.2) the fluctuations on the

propagation time of flip-flop R are caused just by the fluctuation of the power rail line (=ΔV_{DD2}, III.1).

In the case of the setup parameter things are completely different and even opposite to the behavior observed before now. First the effect of the low V_{DD2} causes a decrease on setup time due to the smaller swing the inverters must perform to reach a high output within the noise margin level for enough time to latch-up the signal. On the other hand, fluctuations of the setup time (reduction). However the lower level of data D input (respect V_{DD2}) causes a fluctuations in opposite sense (increase), resulting in a compensating phenomena. Fig. 8 shows the results of a global experiment ($\Delta V_{DD}=V_{DD2}-V_{DD1}$) in the sense of Fig. 5.

III.4 Timing Relationship.

Let us imagine a circuit line like the one shown in Fig. 5, but where the two cores have the same voltage level we assume equal to nominal value (V_{DD}). We can write the following timing condition:

$$T_{CLK} \geq t_{propagation0} + t_{setup0} \qquad (8)$$

Now if we consider the case of fluctuations ΔV_{DD2} and ΔV_{DD1} we should write:

$$T_{CLK} \geq t_{propagation0}(1 + f(\Delta V_{DD1})) + \cdots$$

$$+ t_{setup0}(1 + h(\Delta V_{DD2}) - k(\Delta V_{DD2})) \qquad (9)$$

Where f is the time parameter changing factor (section III.1), h corresponds to the effect due to the data D input drop (section III.2) and k is related to the effect of V_{DD2}. Remember we are not considering line propagation time to simplify and give a clearer picture of the considered effect.

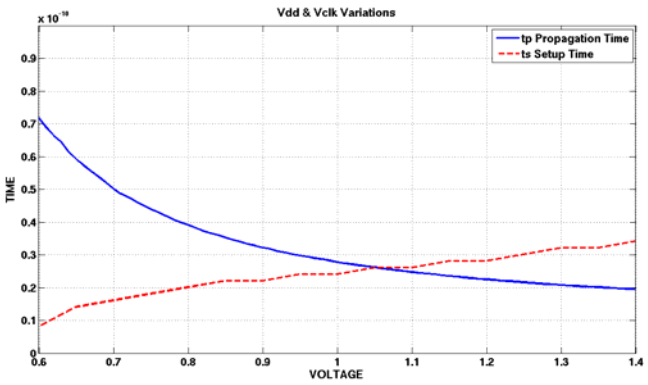

Fig. 8. Effect of a spatial voltage drop in the propagation (blue continuous line) and setup time (red dotted line).

IV. Discussion and Conclusions

In the presence of high and fast and abrupt, demands of current in circuits with a low voltage supply, causes of ground bounce and voltage fluctuations do not have to be restricted to the parasitic impedance of packaging and bounds. The internal to the chip voltage distribution network has to be taken into account. This last non-ideal network responds at very high frequencies, just the opposite to medium and low frequencies present in PCB and packaging impedances. In the paper a general model consisting of a continuous and homogeneous conductive foil is evaluated, for the resistive drops (IR) and for the dynamic and resonant response due to the electromagnetic behavior of the foil. Considering that spatial voltage drops are possible between points located at a certain distance far from each other, the effect of these drops are evaluated through electrically simulated circuits. Because the more realistic situation would be the bus lines between cores in a multi-core integrated circuit the effect of the spatial voltage drops on a single bit bus has been investigated. The results show that fluctuations cause a modification of the time requirements of the flip-flops and that the spatial could introduce some compensating effects.

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