POWER SUPPLY NOISE AND LOGIC ERROR PROBABILITY

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***Abstract*— Voltage fluctuations caused by parasitic impedances in the power supply rails of modern ICs are a major concern in nowadays ICs. The voltage fluctuations are spread out to the diverse nodes of the internal sections causing two effects: a degradation of performances mainly impacting gate delays and a noisy contamination of the quiescent levels of the logic that drives the node. Both effects are presented together, in this paper, showing than both are a cause of errors in modern and future digital circuits. The paper groups both error mechanisms and shows how the global error rate is related with the voltage deviation and the period of the clock of the digital system.**

I. INTRODUCTION

The problem of power supply voltage disturbances in the internal sections of nowadays VLSI Gigascale integrated circuits is a major bottleneck for the technological evolution of such circuits and CMOS technology in general. The supply voltage decreases at the same time, the power consumption increases as more devices are integrated in modern circuits implying a huge increase of the current levels feeding the integrated circuit. At the same time, the increment of both complexity and speed of circuits is forcing the *dI/dt* factor towards greater levels. Resistive (*IR-drop*) and inductive (*LdI/dt* noise) disturbances originated in the package and the power supply distribution network by the power supply current components are of main concern in integrated circuit design [7]. The disturbances and fluctuations of the power supply voltage of internal blocks cause noise in the quiescent levels of the logic circuits as well as gate delay variations.

In general a VLSI design objective is to keep voltage fluctuations bounded by a given limit, usually considered in between 5 and 10% [7], [3], [9] in order to limit their corresponding impact on performance. Previous works approaching the problem [8] identified voltage fluctuations as a key factor for high performance integrated circuits. Recently, a special relevance is being dedicated to the problem due to the critical impact of power supply voltage noise on circuit performances [5]. This effect is expected to be even more relevant for the next generations of Gigascale Integration multi-core processors. In [10], Zheng and Tenhunen defend the thesis that the noise peak value is the most relevant factor to investigate the impact on performances, while in [5], Saint-Laurent and Swaminathan defend that it is more general to consider the average supply voltage while a circuit is switching.

In this paper a comprehensive approach is considered based on the modeling of voltage fluctuation as a random variable with a given probabilistic distribution. The mean value is given by the average *IR-drop* and the variance is dominated by the fluctuation swing caused by *LdI/dt* noise. In complex Gigascale circuits the unpredictable nature of fluctuations is better dealt with the approach here presented and as it will be shown, this approach allows the determination of the probability of potential transient faults caused by this unpredictable voltage noise. Previous papers [2], [1], investigated the effect of power supply voltage disturbances on the appearance of transient errors, modeled as delay faults. The paper here presented gives the calculation of error probability due to such faults when caused by both delay violation and misleading of the logic values because a noise contamination of the electrical levels. From this approach, designers may take decisions about compensation techniques for a desired error level. The evaluation of the error bound can be useful for new design paradigms where retry and self-recovering techniques are applied to the design of high performance processors [6], [4].

The structure of the paper is as follows. Section II discusses the impact of voltage fluctuation on circuit path delays. Section III calculates the probability of error through a timing violation analysis, giving results about the impact of the noise mean and variance as well as the circuit designing parameters. Section IV analyses the error probability caused by the noise contamination of the logic levels. Section V groups the two mechanisms, timing violation and level contamination showing a global error rate calculation. Finally section VI presents the main conclusions of the paper.

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II. NOISE IMPACTS LOGIC DELAY

Power supply noise impacts the propagation time (ie; delay) of the logic gates and blocks. One of the main effects of power supply voltage noise in a synchronous digital circuit is to cause a timing violation in a register during a clock period when the value of V_{DD} is smaller than nominal value, becoming a permanent fault. Due to the slow variations of V_{DD} with respect to clock period, we assume that all the gates in a combinational path have the same value of V_{DD}, that will vary from period to period. In order to obtain the probabilistic distribution of gate delay due to power supply voltage noise, it is necessary to investigate the dependence of gate delay with ΔV_{DD}. This dependence can be analytically obtained only for very simple MOS models that are not accurate enough for nanometric devices. Therefore, we have obtained this dependence by HSPICE simulations for a 90-nm technology with 1V nominal voltage. We simulated a 3-stage ring oscillator structure to avoid the dependence on the delay of the input voltage waveform and obtain accurate results. Several gates are considered for the ring: NOT, NAND, NOR, and XOR. Each ring is simulated several times, each one with a different value of V_{DD}, from 1.2 V to 0.65V. This is a wide range considering that the predicted percentage power supply voltage variation for this technology is 10%, acording the ITRS [3]. Figure 1 shows the results of the delay for different gate type obtained from the delay of one period of the ring oscillator output (measured at cross by 50% of V_{DD}) as well as for the setup time of a register.

III. TIME VIOLATION ERROR PROBABILITY COMPUTATION (DELAY ERROR)

A. *Delay probability distribution function*

The objective of this section is to get the timing violation error probability for a given logic chain when a Gaussian noise in the power supply with momentums μ_{Vdd} and σ_{Vdd} respectively are assumed. The result of the previous section gives a function relating power supply voltage with gate delay. In order to obtain the desired error probability due to time violation errors, we call delay errors, it is necessary to obtain the probability density function (*pdf*) of the delay magnitude for each gate type.

As section II shows, the relation between voltage and timing characteristics is nonlinear. Therefore, the *pdf* for the timing characteristics will not be an exact gaussian as the *pdf* for power supply voltage, but must be derived from it either analytically or numerically. In our study, the voltage-delay dependence is obtained numerically, and so will be the timing *pdf*. A simple Matlab script is used to calculate numerically all the delay *pdf* of the different gates considered in this paper. Figure 2 shows the resulting *pdf*s for different basic gates and setup time of flipflops where the delay has been normalized to the mean delay.

B. *Error probability computation*

Once the delay *pdf* is calculated, the error probability of a timing violation can be calculated by numerical integration. Let us consider a typical pipeline stage, with a combinational delay chain and a latch. In this structure, a timing error occurs when the combinational delay t_G plus the setup time of the latch t_S exceeds the clock period T_{clk}. Under our approach, both t_G and t_S are random variables that have a timing distribution derived as explained in section III.A. As a first approach, we do not consider clock skew or clock period variations.

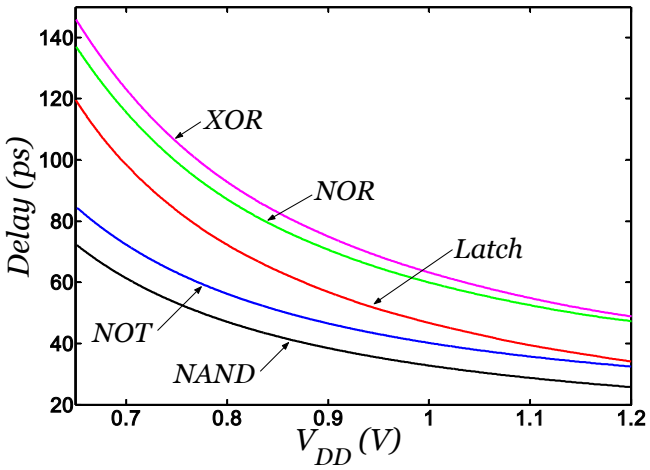

Figure 1. Delay vs. power supply voltage for different basic gates.

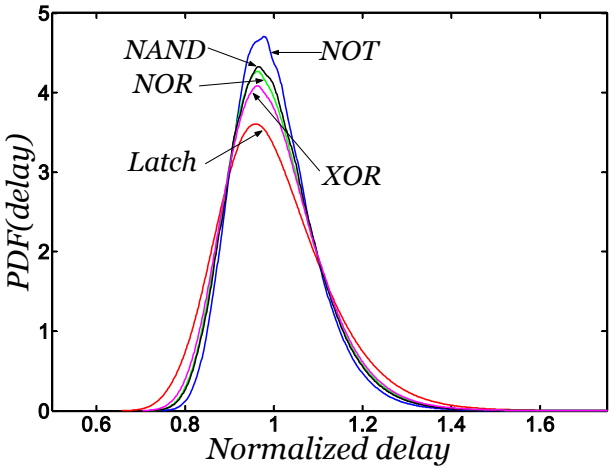

Figure 2. Normalized *pdf* for delay variable and different basic gates.

In general, calculating the error probability for a pipeline stage is a complex task as it is necessary to calculate the delay probability for each gate and then calculate the chain delay probability. However, it is possible to simplify this process if we assume two properties of these chains. First, that the normalized timing *pdf*s are practically equal, as can be observed in Figure 2. Therefore, the delay and critical setup time may be expressed for any gate with a single random variable δ as:

$$t_G = t'_G \delta$$
$$t_S = t'_S \delta \qquad (1)$$

where t'_G and t'_S are the mean values of the total gate chain delay and the latch setup time respectively. Second, the switching time for the gates are small compared to the period of the ground bounce noise. This allows considering all the gates in a chain to be affected by the same voltage noise value. Considering both facts, the condition for having a delay error caused by timing violation simplifies to

$$(t'_G + t'_S)\delta > T_{clk} \qquad (2)$$

These parameters are dependent on the delay *pdf* and therefore on the power supply voltage distribution. As discussed in section III.A, we consider Gaussian power voltage noise distributions with a given mean (μ_{vdd}) and standard deviation (σ_{vdd}). With these considerations, the error probability for a pipeline stage reads

$$p(D) = \int_{\frac{T_{clk}}{t'_G + t'_S}}^{\infty} \eta(\delta) d\delta \qquad (3)$$

where $\eta(\delta)$ is the *pdf* of the random variable δ. Numerically integrating equation 3 it is possible to calculate the error probability given a certain power supply voltage *pdf*. As a matter of illustrative example we consider a delay path composed by 5 gates (NOR, NAND, XOR and two NOTs). Adding the latch setup time the total delay under nominal conditions (V_{DD} of 1V) is 306 ps (3.27 GHz).

Figure 3 shows the Delay Error Probability versus the time security margin $T_{clk}/(t'_G+t'_S)$, defined by the designer, for the mentioned logic chain considering a mean value for the supply voltage (which considers the *IR* drop and the control actions of the supply system) μ_{VDD}=0.95V and different noise amplitudes (from 1 to 30%). Observe that in order to assure an error probability smaller than 0.2% with a 10% of noise amplitude, it is necessary to provide a time security margin larger than 22%. A trivial observation is that this model considers a null error probability for an infinite time security margin.

IV. LOGIC LEVEL CONTAMINATION ERROR

In this section we will evaluate the probability error caused by a direct effect of the noise on the electrical logic level. When the PMOS (NMOS) device is on, representing a 1 (0) logic value the noise in the VDD (GND) rail is applied directly to the output node, causing a noisy output given by $VDD + V_{noise}$ (V_{noise}). We assume power supply noise in both VDD and GND rails. Figure 4 shows the probability distribution function (Gaussian) for both rail noises on the voltage axis. We consider a contamination error when there is a misleading of the logic level, this means that the "1" voltage level crosses down the half power supply level threshold (1 is understood as 0) or that the "0" voltage level crosses up the half power supply level threshold (0 is understood as 1). The probability of (through VDD and GND) of contamination noise errors are given by:

$$p(C) = \frac{1}{2}\left[1 + erf\frac{V_{DD}}{2\sigma_{VDD}\sqrt{2}}\right] \qquad (4)$$

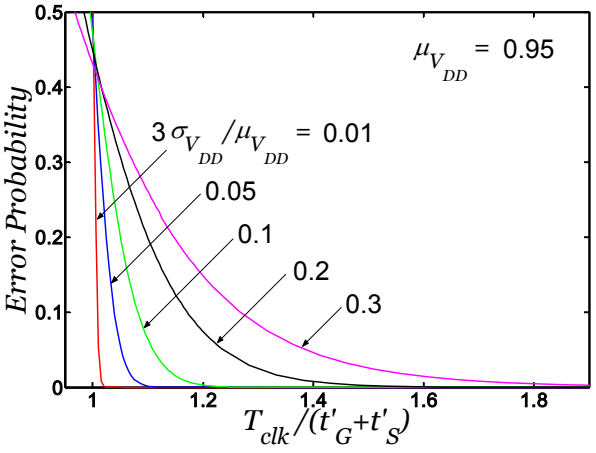

Figure 3. Delay error probaility for a 5 gate chain for different noise amplitudes and time security margins.

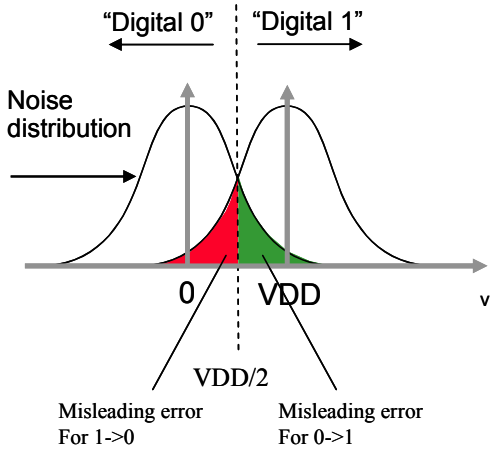

Figure 4. Misleading logic levels caused by direct logic level noise contamination.

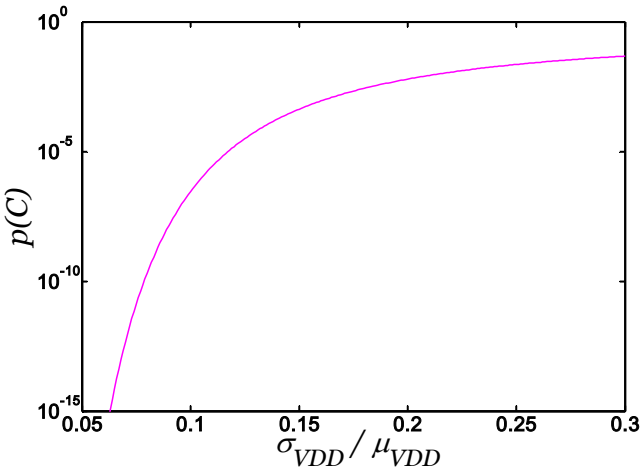

Figure 5. Contamination error for different noise levels. Vertical axis is the contamination error probability p_C and the horizontal the relation σ_{Vdd}/V_{DD}.

Similar reasoning for the level contamination error and probability calculation can be found in [11] and [12]. Figure 5

shows the representation of equation (4) for different levels of noise amplitude (typical deviation) relative to VDD, σ_{vdd}/V_{DD}. As a matter of example observe that for σ_{vdd}/V_{DD}=0.1 the contamination error probability is 10^{-7}, a moderate but not negligible rate of transient faults. The meaning of the contamination error is given by the following consideration: the noise is coupled directly to the node contaminating its value. Independently of the clock period T_{clk} (even infinite) and neglecting any type of filtering in the interconnection or devices, the data is "registered" at a given arbitrary time, resulting a sampling of the Gaussian noise.

V. GLOBAL ERROR PROBABILITY

In this section we group the two types of causes of error, delay (*p(D)*) and level contamination (*p(C)*), in order to find the global error probability. Both causes have a common source: the voltage noise, so the two probabilities are not independent. If we name D as the delay cause and C as the contamination cause, we can write:

$$p(D+C) = p(D) + p(C) - p(D \cdot C) \quad (5)$$

where in the case of a moderated error rate as the one considered for nowadays CMOS technology the third term can be neglected and (5) can be approximated to:

$$p(D+C) = p(D) + p(C) \quad (6)$$

We show in Figure 6 the resulting global error probability versus the time security margin for $3\sigma_{VDD}/\mu_{VDD}$=0.3, only. It can be observed that for high error rates *p(D)* dominates the error probability, and for $T_{clk} \Rightarrow \infty$, the error probability is asymptotic to *p(C)* and not to 0, showing that even for a widely dimensioned synchronous system there is an error rate caused by noise.

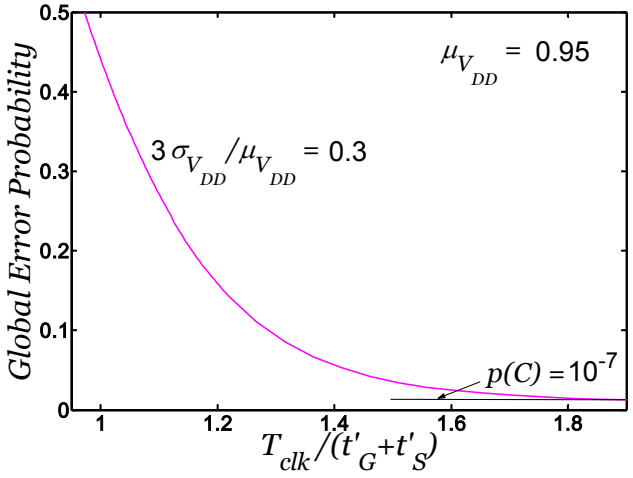

Figure 6. Global error probability due to power supply noise.

VI. CONCLUSIONS

Power supply noise is a major concern in advanced ICs because of the circuit's critical conditions. Power supply noise can be a source of errors, transient mainly but that can become permanent when stored in registers. In this paper such a class of permanent errors has been considered, showing two causes of error, time violations because enlargements of the path delay due to voltage noise and false registering caused by direct noise contamination of the logic nodes. The error probability for both causes and an approach to the global one has been derived. We have showed that the timing violation errors are a sensitive function of the timing margin policy, and that even for very relaxed time requirements there is a probability of error caused by the contamination factor.

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