Output Voltage Regulation of a High-Efficiency High Step-Up DC-DC Power Converter

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***Abstract*— Step-up dc-dc power converters are needed in many applications. Depending on the voltage conversion ratio, one or another structure should be chosen, usually leading to efficiency vs. conversion ratio trade-offs. Recently, a new class of switch-mode dc-dc power converters has been introduced into the literature. These new converters show high efficiency levels at high conversion ratios, making them attractive to applications where efficiency is a major concern. Due to the complexity of the structure, mathematical models of the system have not been developed up to now, making the closed-loop control of these devices a challenging task. In this paper, an output voltage regulation control scheme is proposed and tested in simulation. The system is decomposed in subsystems, whose models are identified within the different control stages.**

I. Introduction

Efficiency is a major concern when high conversion ratios are demanded from switch-mode power converters (SMPC). Zhao *et al.* have developed a new class of SMPC [1]-[4] capable of providing efficiencies around 90% at high conversion ratios, with a low component count. This new class of converters uses high-frequency transformers to provide a more efficient path for the energy to flow from the source to the load. Works have been done in order to analyse the different topological variations of these converters [5], in order to achieve high efficiency with a high conversion ratio, and low stress on the components. The characteristics of these converters make them attractive to applications where high output voltages are required when the voltage source can provide only low voltages. In [4] a boost converter is presented and elevation ratios of about $8:1$ are achieved, while attaining efficiencies above 90%. Although, these converters have been studied by different authors because of their appealing electrical characteristics, so far, there are no closed-loop control schemes applied to such topologies present in the literature. This makes the control of this kind of SMPC an interesting problem from the control of power electronic converters point of view.

The motivation of this work was to develop the voltage step-up stage for a 1 kW dc-ac voltage inverter fed by a PEM type fuel cell. In this case a Ballard MAN5100078 PEM fuel cell has been defined as the power source. At 1 kW output power, the MAN5100078 provides about 25 V dc according to the product specifications [6]. The step-up stage must be capable of elevating the output voltage from 25 V dc up to 400 V dc to feed the dc-ac voltage inversion stage, and therefore a voltage elevation ratio of $16:1$ is expected. The efficiency of the overall system is a major concern in this design, and thus, a highly efficient step-up stage must be considered.

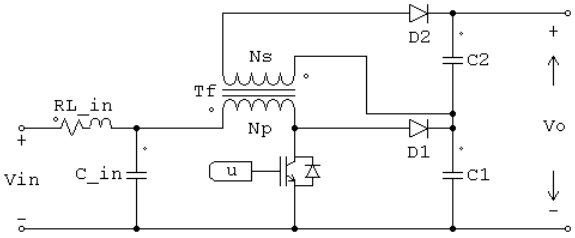

Fig. 1. Step-up SMPC Zhao *et al.* [4] and input current filter.

This work presents the development of an output voltage controller for the dc-dc SMPC of Fig. 1. This is a challenging task due to the lack of mathematical models that describe the behavior of this converter. The use of system identification techniques to obtain the nominal plant models finds applicability in the solution of this problem. The control objective is to maintain the output voltage V_o at 400 V dc under different load conditions. The converter must be able to handle up to 1 kW output power (full load).

Section II presents the values of the components and a brief description of the converter to be used. The proposed control architecture is described in section III. The nominal plant identification and controller design for the inner control loop are explained in section III-A. The nominal plant identification process and the development of the output voltage controller are presented in section III-B. The simulation results under output voltage reference changes and load disturbances are discussed in section IV. The conclusions are presented in section V.

II. System Description

Fig. 1 presents the step-up structure to be used. V_{in} is the dc voltage source (PEM type fuel cell). An input current low-pass LC filter (RL_{in} and C_{in}) has been added, in order to protect the fuel cell unit against the high-frequency, discontinuous input current shape of the converter. The boost topology used in this design was presented in [4].

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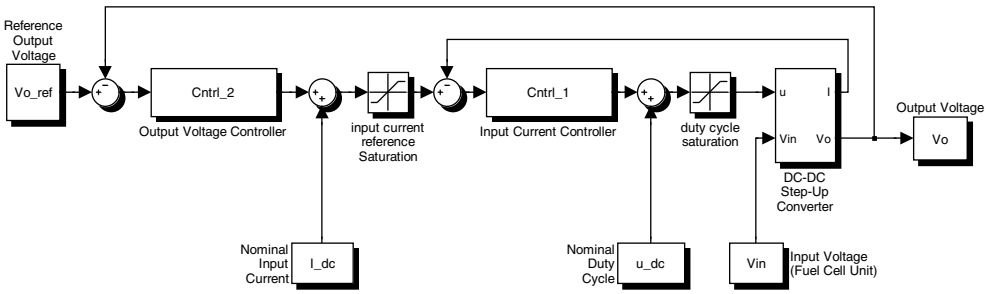

Fig. 2. Proposed dual-loop output voltage regulation control scheme.

The values of the components used in the converter of Fig. 1 are: $V_{in} = 24$ V dc, $RL_{in} = 10$ mΩ in series with a 42 μH inductance, $C_{in} = 2000$ μF, $C_1 = C_2 = 220$ μF. D_1 is a 60CPQ150 60 Amp, 150 V_{RRM} Schottky diode with 0.8 V dc forward drop from IR, D_2 is an IXYS DSEI60-10A 60 Amp, 1000 V_{RRM} FRED diode with 2 V dc forward drop. The switch is implemented by means of four IRFPS40N50L 500 V_{DSS}, 46 Amp in parallel with a total $Rds_{on} = 20$ mΩ, and 1.5 V dc forward voltage drop for the recovery diode. A RCD turn-off snubber [7], [8] has been added in parallel to the switch, its purpose is to reduce the voltage ringing between the drain and source terminals of the MOSFET array. A 60CPQ150 Schottky diode from IR, a 16 Ω 20 W resistor and a 33 pF capacitor are used in the RCD snubber. T_f is a high-frequency transformer with $N_p = 20$ turns, $N_s = 136$ turns, the leakage inductances of the primary and secondary windings are $L_{\sigma p} = L_{\sigma s} = 1.4$ μH. The resistances of the primary and secondary windings are $R_p = 3.3$ mΩ and $R_s = 1.8$ mΩ, and the magnetizing inductance is $L_m = 71$ μH. All the resistance and inductance values are referred to the primary winding. The duty cycle u is commanded by using regular centered pulse, single-update mode, pulse-width modulation (PWM) at 20 kHz. The output voltage must be maintained at $V_o = 400$ V dc and the system full-load condition is set to 1 kW output power.

III. Output Voltage Regulation Controller Design

Fig. 2 presents the proposed output voltage control scheme. A cascade control scheme is considered. The inner loop controls the current that is extracted from the fuel cell by making changes in the duty cycle u. The outer loop controls the output voltage by making changes in the current reference that must be extracted from the voltage source. This scheme offers the possibility of limiting the input current reference, and therefore, protecting the components against excessive current values.

A. Input Current Control Loop

The purpose of the inner control loop is to control the current that is provided by the voltage source V_{in}, by means of changes in the duty cycle u. In order to develop the inner-loop controller, a model of the input current response to variations on the duty cycle must be known.

The procedure followed to find a valid frequency-domain model is as follows:

- Perform small-signal swept-sine analysis for the system working at different operating points.
- Select a representative Bode (gain and phase) plot to be used as the nominal plant.
- Fit a continuous-time system to the selected Bode plot.

Fig. 3 shows the small-signal swept-sine analysis results for the system working under different load conditions. In all cases 400 V dc are provided at the output feeding a resistive load. The output power conditions considered for the test were 100 W, 600 W, 1000 W and 1500 W. The small-signal swept-sine analysis has been performed from 1 Hz up to 10 kHz.

The following stage consists in selecting a representative swept-sine analysis response to be used as nominal plant for the controller. From the Bode plots of Fig. 3, it can be seen that the 600 W plot would be a good choice, because its path remains in the middle of all other plots for the gain (magnitude) as well as for the phase.

Having selected the 600 W small-signal swept-sine analysis result as the nominal plant, in order to to be able to design the controller, it is necessary to fit a continuous-time system to this frequency-domain data. To find an estimated state-space model that fits the desired frequency-domain gain and phase data, a black-box system identification routine was used. In this case a parametric model algorithm was used to find a 4 states continuous-time model that fits the 600 W data. The resulting transfer function from the duty cycle variations U to the input current variations I takes then the form presented in Eq. (1).

$$G_1(s) = \frac{-798.6737(s+39.82)(s+1.928e^4)(s-5.538e^5)}{(s+212.5)(s+513.1)(s^2+406.9s+1.54e^7)} \quad (1)$$

The identified continuous-time nominal plant, expressed by Eq. (1) has two stable zeros at 39.82 rad/sec and $1.928e^4$ rad/sec, and a nonminimum phase zero is present at $5.538e^5$ rad/sec. Additionally, $G_1(s)$ has two stable real poles at 212.5 rad/sec and 513.1 rad/sec. Two stable complex poles are present with a natural frequency of $3.92e^3$ rad/sec and a

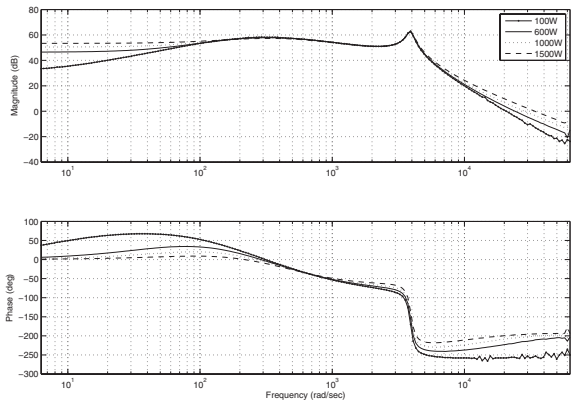

Fig. 3. Small-signal swept-sine analysis results for the system at different working points. Input variable: variations on the duty cycle u. Output variable: variations on the input current to the system.

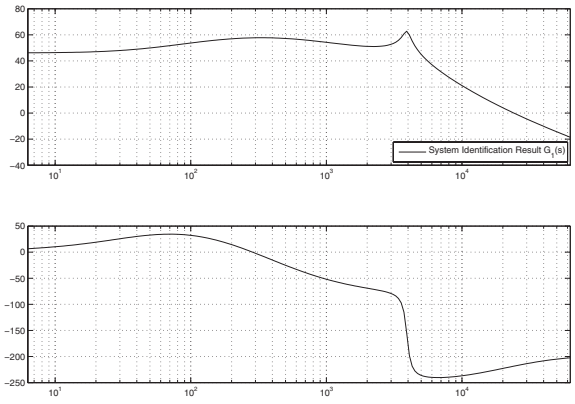

Fig. 4. Bode plot of the system identification result transfer function $G_1(s)$.

damping of 0.0517, whose effects can be seen in the resonant peak of the 600 W plot in Fig. 3.

Fig. 4 presents the Bode plot for the continuous-time system identification result, Eq. (1). By comparing the 600 W plot in Fig. 3 with the system identification result in Fig. 4, it can be seen that Eq. (1) provides a very good approximation of the behavior of the system.

As the controller is to be implemented by means of a digital computer, it would be convenient to make the controller design directly in the z-domain. The plant defined by Eq. (1) must be converted to a discrete-time model. Eq. (2) shows the conversion result of Eq. (1) into the z-domain, when using a sampling frequency of 20 kHz and a zero-order hold (ZOH) as discretization method.

$$G_1(z) = \frac{0.65858(z+1.528)(z-0.998)(z-0.379)}{z(z-0.9894)(z-0.9747)(z^2-1.94z+0.9799)} \tag{2}$$

When implementing the controller, the load of the PWM register of the microprocessor, introduces a one switching cycle delay. This delay needs to be accounted into the nominal plant in order to consider its influence into the behavior of the overall system. Eq. (3) shows the actual nominal plant to be used in the controller design process.

$$P_1(z) = \frac{1}{z} G_1(z) \tag{3}$$

Using Eq. (3) as nominal plant, a discrete-time controller has been designed. This controller must have as much bandwidth as possible while attaining good stability margins.

$$C_1(z) = \frac{0.0015594(z^2-1.942z+0.9801)}{z(z-1)} \tag{4}$$

The controller of Eq. (4) has two stable complex zeros with natural frequency of $3.92e^3$ rad/sec and a damping of 0.0517, which compensate the resonant poles at the nominal plant. Also $C_1(z)$ has a real pole at $z = 1$ which means that the closed-loop system error trends asymptotically to zero for step changes in the input current reference. An additional zero is located at $z = 0$ to add properness to the controller $C_1(z)$.

Fig. 5 shows the open-loop Bode plot for the input current control loop. This design presents good stability margins, having a phase margin of 46.9^o and a gain margin of 25.7 dB.

B. Output Voltage Control Loop

The control objective of the outer control loop is to maintain the output voltage level close to its reference value, by means of changing the input current reference to the inner control loop. In order to be able to develop a controller for this task, a model of the plant must be known. In this case the plant output is the output voltage, and the input to the plant is the input current reference to the inner loop.

The procedure followed to find a continuous-time model from the changes in the input current reference to the changes in the output voltage reference is as follows:

- Apply different step reference variations into the inner-loop current reference and normalize the results.
- Determine if the normalized output voltage responses can be approximated by a low-order continuous-time system.
- Average the dc gain, pole values, zero values for all the cases.
- The nominal plant will be the low-order system formed by the average values.
- Include the appropriate time delays into the low-order model.

Fig. 6 shows in dashed the normalized responses of V_o to different magnitude step changes in the input current reference. From Fig. 6 it can be seen that the responses can be approximated by a first-order system of the form:

$$\frac{A}{\tau s + 1} \tag{5}$$

By averaging the time constants and the DC gains of the V_o responses an average first-order system is obtained. The solid line in Fig. 6 is the resulting average first-order system defined by Eq. (6).

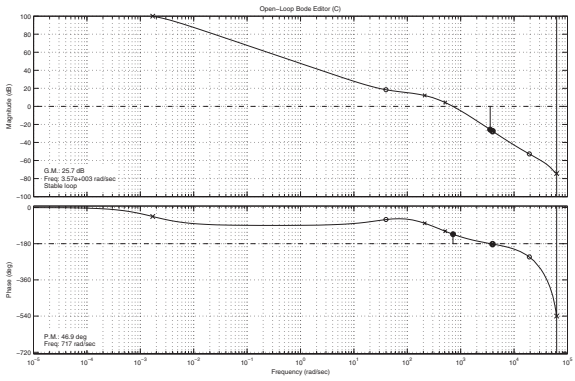

Fig. 5. Open-loop Bode plot for the inner control loop. Control of the input current.

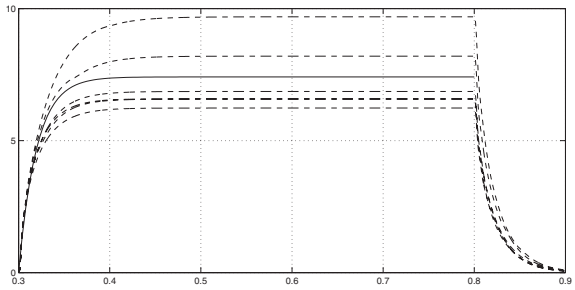

Fig. 6. V_o responses to different magnitude step changes in the input current reference around the operating point. The step change magnitudes are 1A,10A,20A,-1A,-10A,-20A. Dashed: normalized V_o responses. Solid: system average approximation.

$$G_2(s) = \frac{7.411}{1.966e^{-2}s + 1} \tag{6}$$

The output voltage controller is also to be implemented by means of a digital computer, so the continuous-time system must be discretized. Eq. (7) shows the conversion result of Eq. (6) into the z-domain. The sampling frequency is 20 kHz, and a zero-order hold (ZOH) has been used as discretization method.

$$G_2(z) = \frac{1.883e^{-2}}{z - 0.9975} \tag{7}$$

Again, intrinsic time delays need to be accounted to include their influence in the behavior of the plant. After a detailed analysis of the time responses of Fig. 6, it has been determined that it is necessary to include a 2 switching period delay, and hence the plant to be controlled becomes:

$$P_2(z) = \frac{1}{z^2} G_2(z) \tag{8}$$

Having Eq. (8) as the plant to be controlled, a discrete-time controller has been designed. The resultant controller is presented in Eq. (9).

$$C_2(z) = \frac{11.286(z - 0.9974)(z - 0.8967)}{z(z - 1)} \tag{9}$$

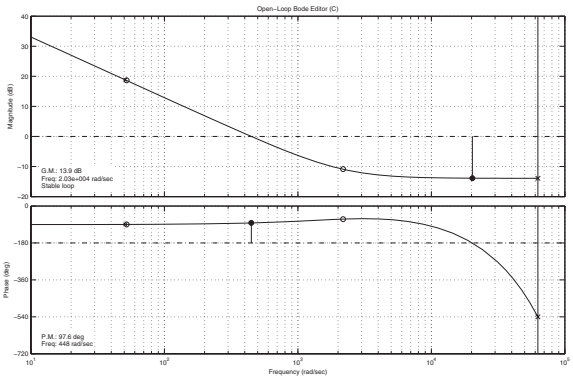

Fig. 7. Open-loop Bode plot for the outer control loop. Control of the output voltage V_o.

Eq. (9) has two real stable zeros located at 52.2 rad/sec and $2.18e^3$ rad/sec. The outer-loop controller $C_2(z)$ also has a pole located at $z = 1$ which means that the error of the closed-loop system will trend asymptotically to zero when step changes are applied to the output voltage reference. An additional zero is located at $z = 0$ to make the controller proper.

Fig. 7 shows the open-loop Bode plot for the outer control loop. This design presents good stability margins, having a phase margin of 97.6^o and a gain margin of 13.9 dB.

IV. Simulation Results

The designed controllers were tested in simulation on a 1 kW system. Fig. 8 shows the response of the system to load variations. The system has been driven to steady state at 1 kW. Load changes have been performed in the system from full-load condition (1 kW) to 200 W output power and then back to full load. The system is capable of regulating the output voltage in less than 85 msec, and the overshoot presented is less than 6.38%. The overall efficiency of the system under this circumstances is always above 93%.

Fig. 9 shows the response of the system to an output voltage reference change, from 400 V dc to 350 V dc and back to 400 V dc at full-load condition. The settling time is less than 70 msec and the overshoot is 3.95% of the steady-state value of the output voltage.

Experimentation was only accomplished by means of numerical simulation, taking into account aspects that are present in the experimental set up. The simulations have been executed under switch-mode at 20 kHz switching frequency. The MOSFET array is modeled as a 20 mΩ resistor when the switch is in conduction state. The antiparallel diode of the MOSFET array and diodes D_1 and D_2 are modeled as dc sources when they are in on state. Parasitic resistances are considered for the input inductance and for the two windings of the transformer. The leakage inductances of the transformer are considered for the two windings. The time delay due to the load of the PWM register, that usually appears in the microprocessors is considered for the controller design of the inner loop. The propagation of the time delay of the inner loop to the outer control loop is also considered.

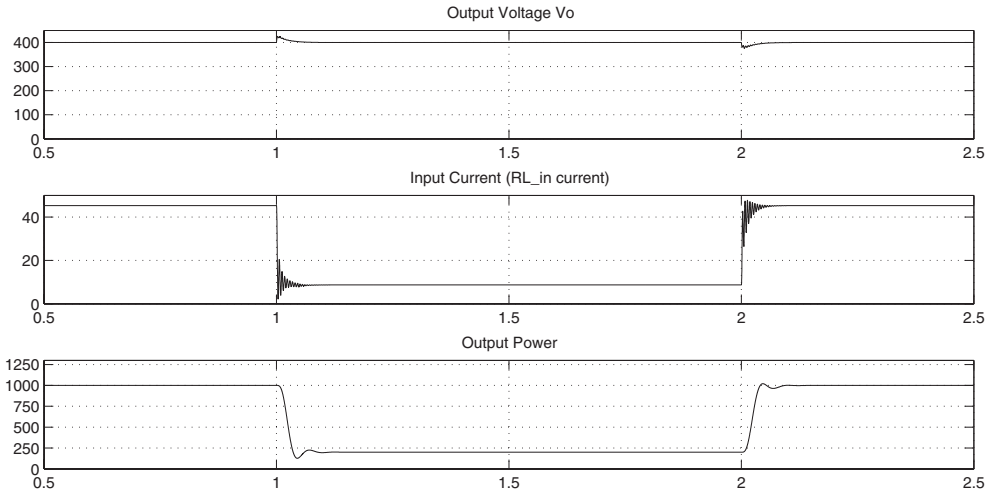

Fig. 8. Output voltage regulation under load change conditions.

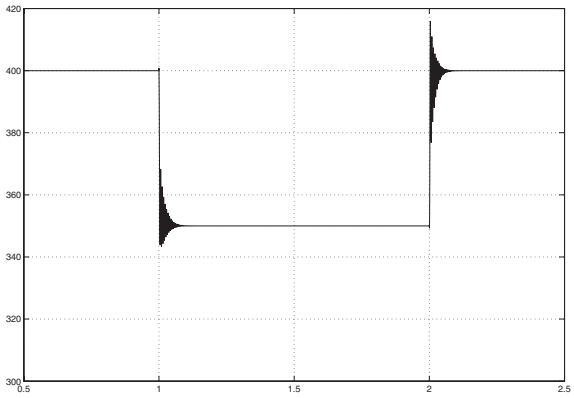

Fig. 9. Output voltage regulation under reference change from 400V dc to 350V dc and back to 400V dc.

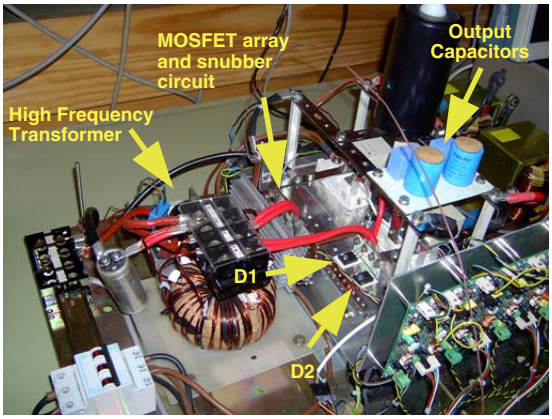

Fig. 10. Step-up SMPC Zhao *et al.* [4] experimental set up.

On the other hand, open-loop tests on the operation of the experimental set up, shown in Fig. 10, exhibit an 87% conversion efficiency at full load and a 91% at half load. These preliminary results are very promising about the operation of the system, considering the low input voltage, and the $16:1$ conversion ratio reached.

V. Conclusions

A cascade control system with a good robustness has been developed and tested for the output voltage regulation of the step-up converter presented in [4]. The dual-loop control scheme of Fig. 2 has been used to regulate the output voltage of the converter. The inner loop controls the current that is demanded from the voltage source. This control architecture allows the designer to impose a hard limit to the input current reference, and thus, the physical elements can be protected against over currents. The inclusion of the $z = 1$ poles in Eq. (4) and Eq. (2) has the effect of making the steady-state error of the closed-loop system trend asymptotically to zero for step variations in the input current and output voltage reference signals. This translates into zero steady-state error for constant references, which is the regulation problem control objective. The addition of the current filter (RL_{in} and C_{in}), the selection of the input current as the variable to be controlled, and the selection of u as control variable in the inner-control loop have made easier to find a good continuous-time approximation of the inner-loop nominal plant.

The simulation results show that the developed controllers have a good level of robustness against important reference changes and load disturbances.

Acknowledgment

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