# The Floating Capacitor as a Differential Building Block

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***Abstract*— This paper analyzes the advantages and limitations of using the floating- (or flying-) capacitor technique as a building block with differential input and either differential or single-ended output to implement voltage amplifiers, multiplexers, and coherent amplitude demodulators. Theoretical analysis, supported by experimental results, shows that the fully differential configuration has a better common-mode rejection ratio (CMRR). However, if the output signal, once amplified, must be single ended, then it may be better to have a floating capacitor with single-ended output in amplifiers and some multiplexers whereas in demodulators a floating capacitor with differential output yields a better CMRR.**

***Index Terms*— Capacitor switching, CMRR, data acquisition, differential amplifiers, multiplexing, sampling methods, synchronous detection.**

## I. Introduction

THE floating- (or flying-) capacitor technique is a common method for low-level signal amplification [1] and multiplexing [2]–[4]. Fig. 1 shows the basic floating-capacitor circuit. First, switches $S1$ and $S2$ close and $C_S$ charges to the differential input voltage $V_d$ (assumed constant). Next, $S1$ and $S2$ open and $S3$ and $S4$ close, so that, except for stray capacitances $C_{s1}$ to $C_{s4}$, the charge stored by $C_S$ is shared by $C_H$, assuming it was previously fully discharged, in accordance with

$$Q = V_d C_S = V_o(C_S + C_H). \tag{1}$$

And therefore

$$V_o = V_d \frac{C_S}{C_S + C_H}. \tag{2}$$

This means that the differential output voltage $V_o$ ideally depends only on the differential input voltage $V_d$, thus yielding a very high common mode-rejection ratio (CMRR) without the necessity of any component matching.

When the floating-capacitor technique is used for amplification [1] or demodulation [5] or multiplexing [2], the circuit output in Fig. 1 is usually grounded and connected to the input of a single-ended amplifier that provides gain and low output impedance [1], [5]. This is a considerable advantage because it allows us to use an op-amp-based amplifier, which is less expensive than an instrumentation amplifier. Furthermore, by using switches able to withstand high voltages it is possible to pick out small differential voltages superimposed on very high common-mode voltages. In multiplexers, however, sometimes none of their output terminals are grounded [3], [4] but are connected to an instrumentation amplifier.

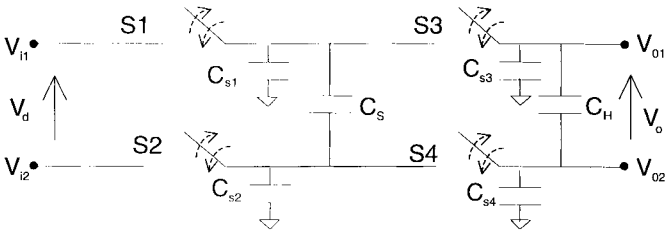


Fig. 1. Floating capacitor circuit. $C_{s1}$ to $C_{s4}$ are stray capacitances.

Therefore, the question arises as to whether it is better to use the floating capacitor as a building block with differential input but single-ended output, or as a fully differential circuit. A satisfactory answer can only be given by considering the fact that an amplifier must follow the floating capacitor.

## II. Theoretical Analysis

### A. Fully Differential Floating Capacitor

Analog switches have stray capacitances to ground, which according to switch technology can change from the ON to the OFF state. These changes are disregarded here. In Fig. 1, parallel capacitances are grouped together. Let the switches have zero ON resistance.

$Q_{i1}$ is defined as the charge on the top plates of $C_S$, $C_H$, $C_{s1}$, $C_{s3}$; and $Q_{i2}$ as the charge on the top plates of $C_{s2}$, $C_{s4}$, plus the charge on the bottom plates of $C_S$, $C_H$. At any random time period $n$, first $S1$, $S2$ are closed and $S3$, $S4$ are opened. The charge $Q_{i1}$ will result from the actual input voltages on the top plates of $C_S$, $C_{s1}$ plus the charge stored on the top plates of $C_H$, $C_{s3}$, at the previous time period $n-1$ (assuming that $C_H$ has not been reset between samples). The same will apply for $Q_{i2}$, giving

$$\begin{aligned} Q_{i1}(n) &= V_{i1}(n)C_{s1} + [V_{i1}(n) - V_{i2}(n)]C_s + V_{o1}(n-1)C_{s3} \\ &\quad + [V_{o1}(n-1) - V_{o2}(n-1)]C_H \\ Q_{i2}(n) &= V_{i2}(n)C_{s2} - [V_{i1}(n) - V_{i2}(n)]C_s + V_{o2}(n-1)C_{s4} \\ &\quad - [V_{o1}(n-1) - V_{o2}(n-1)]C_H. \end{aligned} \tag{3}$$

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When $S3$ and $S4$ close, the electric charge will quickly redistribute among capacitances. As the total charge at each side, $Q_{i1}$ and $Q_{i2}$, cannot change, we have

$$\begin{aligned} Q_{i1}(n) &= V_{o1}(n)(C_{s1}+C_{s3}) \\ &\quad + [V_{o1}(n)-V_{o2}(n)](C_S+C_H) \\ Q_{i2}(n) &= V_{o2}(n)(C_{s2}+C_{s4}) \\ &\quad - [V_{o1}(n)-V_{o2}(n)](C_S+C_H). \end{aligned} \tag{4}$$

Equating expressions (3) and (4) in the $Z$ transform domain [6] shows that after many clock cycles the voltage at each output terminal equals that at the respective input terminal, which are assumed to be constant. That is $V_{o1}=V_{i1}$, $V_{o2}=V_{i2}$.

Input and output signals can be described in terms of differential and common-mode voltages, $V_{iD}=V_{i1}-V_{i2}$, $V_{iC}=(V_{i1}+V_{i2})/2$, $V_{oD}=V_{o1}-V_{o2}$, $V_{oC}=(V_{o1}+V_{o2})/2$. Fully differential circuits can be described by four transfer functions as follows [7]:

$$\begin{aligned} V_{oD} &= G_{DD}V_{iD}+G_{DC}V_{iC} \\ V_{oC} &= G_{CD}V_{iD}+G_{CC}V_{iC}. \end{aligned} \tag{5}$$

Here, $G_{DD}=1$, $G_{DC}=0$, $G_{CD}=0$, and $G_{CC}=1$. The CMRR (CMRR $= G_{DD}/G_{DC}$) is therefore infinite because the input common mode voltage cannot produce any differential output voltage.

In practice, the input voltage will not be truly constant and when closing $S3$ and $S4$ there will be some charge redistribution to "update" the voltage across $C_H$. But if the switching rate is fast enough as compared with the rate of change of the input signal, a steady state will be reached rather quickly.

### *B. Floating Capacitor with Single-Ended Output*

In Fig. 1, if the bottom side of the output circuit is grounded, then when $S1$ and $S2$ are closed, (3) is still valid (with $V_{o2}=0$). However, when $S3$ and $S4$ close, the charge $Q_{i1}$ will remain constant, but part of $Q_{i2}$ will run to the ground. The output voltage $V_{o1}$ will then fulfill the condition

$$\begin{aligned} Q_{i1}(n) &= V_{i1}(n)C_{s1}+[V_{i1}(n)-V_{i2}(n)]C_s \\ &\quad + V_{o1}(n-1)C_{s3}+V_{o1}(n-1)C_H \\ &= V_{o1}(n)[C_{s1}+C_{s2}+C_{s3}+C_{s4}]. \end{aligned} \tag{6}$$

As before, the output voltage $V_{o1}$ after many clock cycles can be calculated by assuming the input voltages to be constant,

$$V_{o1}=V_{i1}-\frac{C_S V_{i2}}{C_S+C_{s1}}. \tag{7}$$

If the input signals are again described by differential and common mode voltages, $V_{o1}$ can be written as

$$V_{o1}=G_D V_{iD}+G_C V_{iC}. \tag{8}$$

From (7),

$$\begin{aligned} G_D &= \frac{C_S+C_{s1}/2}{C_S+C_{s1}} \\ G_C &= \frac{C_{s1}}{C_S+C_{s1}}. \end{aligned} \tag{9}$$

Therefore, the CMRR is now,

$$\text{CMRR}=\frac{G_D}{G_C}=\frac{C_S+C_{s1}/2}{C_{s1}} \tag{10}$$

which is smaller than that of a fully differential floating capacitor circuit.

### *C. Effect of Output Amplifier on the CMRR*

Both the fully differential and the single-ended circuits need an output amplifier to provide gain and low output impedance. If this amplifier has a differential input, the overall CMRR will be [7],

$$\frac{1}{\text{CMRR}_o}=\frac{1}{\text{CMRR}_{fc}}+\frac{1}{\text{CMRR}_a} \tag{11}$$

where $\text{CMRR}_{fc}$ and $\text{CMRR}_a$ are the respective CMRR's for the floating capacitor circuit and the amplifier. This means that $\text{CMRR}_o$ will be smaller than that of each stage, if they have the same sign, and will be the largest of them all, if they have opposite signs. Hence, if the fully differential floating capacitor is used because of its high CMRR, then $\text{CMRR}_a$ must be very high too, otherwise it could yield a low $\text{CMRR}_o$.

For low-frequency signal amplification, amplifiers provide a high $\text{CMRR}_a$ with differential input and differential output built from matched op amps, without requiring any matched resistor [8]. Therefore, if a fully differential amplifier with high CMRR is already available, there is no need for an input amplifier stage based on the floating capacitor. However, differential amplifiers with single-ended output have a much smaller $\text{CMRR}_a$ than that of fully differential amplifiers. In addition, $\text{CMRR}_a$ decreases for low gain. Therefore, for low-gain applications, a floating capacitor circuit with single-ended output may have a larger CMRR than a common differential amplifier.

If the floating capacitor circuit is used as a coherent amplitude demodulator [5], its switches typically operate at the carrier frequency. For frequencies about 1 kHz or higher, transients, ON resistance, and limited OFF isolation in switches can yield a $\text{CMRR}_{fc}$ that is lower than $\text{CMRR}_a$ for a differential amplifier working at low-frequency (demodulated signal). Consequently, in this case it should be advantageous to place a fully differential floating capacitor demodulator ahead of a differential amplifier, rather than using a single-ended demodulator following a differential amplifier working at the carrier frequency [5].

The floating capacitor is also used in fully differential multiplexers [3], [4]. In Fig. 2, using a floating capacitor makes it possible to simultaneously sample all input signals and then sequentially amplify each sampled signal by using a common differential (or fully differential) amplifier. Just as in low-frequency amplification, a floating capacitor with single-ended output may have a larger CMRR than a common differential amplifier but only for low-gain applications requiring a single-output.

On the other hand, if for the fully differential circuit $G_{CD}=0$ and $G_{CC}=1$, then according to (5), $V_{oC}=V_{iC}$. Therefore, the amplifier (and input switches) must withstand the input common mode voltage present at any input channel. In case

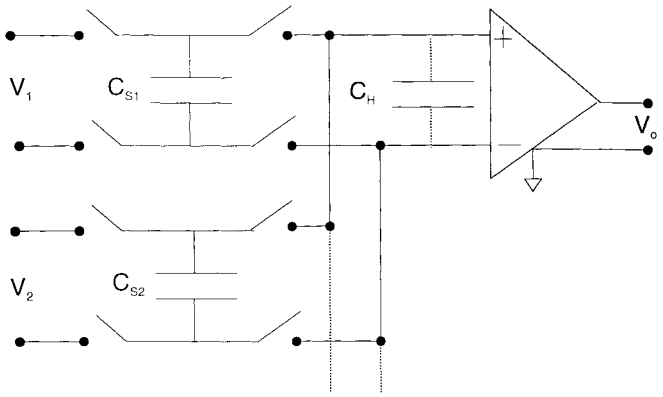


Fig. 2. Fully differential multiplexer.

TABLE I
FREQUENCY DEPENDENCE OF THE CMRR (dB) OF A COHERENT DEMODULATOR BASED ON A FLOATING CAPACITOR CIRCUIT. FD: FULLY DIFFERENTIAL FLOATING CAPACITOR; SE: FLOATING CAPACITOR WITH SINGLE-ENDED OUTPUT

| Sampling Frequency | | 10 Hz | 100 Hz | 1 kHz | 10 kHz | 100 kHz |
|---|---|---|---|---|---|---|
| Reference circuit | FD | 107 | 107 | 107 | 99 | 84 |
| | SE | 99 | 99 | 91 | 74 | 54 |
| Duty cycle=5% | FD | 106 | 107 | 105 | 95 | 79 |
| | SE | 97 | 97 | 84 | 65 | 47 |
| Reference circuit with Cs=100 nF | FD | 126/107 | 121/102 | 126/103 | 115/105 | 91 |
| | SE | 75 | 75 | 75 | 64 | 46 |
| Reference circuit with $C_{s1}$=100 pF | FD | 117/102 | 122/102 | 114/100 | 105/95 | 80 |
| | SE | 80 | 80 | 75 | 59 | 40 |
| Reference circuit with $C_{s2}$=100 pF | FD | 100/116 | 100/114 | 100/116 | 101/121 | 81 |
| | SE | 100 | 100 | 81 | 59 | 41 |

of large common-mode voltages, it may be better to use an amplifier with single-ended input after the floating capacitor circuit because this only applies the differential input voltage to the amplifier. Alternatively, if there is galvanic isolation between signal ground and amplifier ground, it is feasible to use standard switches and a differential amplifier after the floating capacitor circuit because most of the signal common mode voltage will be applied across the insulation barrier.

In summary, it is better to use a fully differential floating capacitor circuit rather than a floating capacitor with a single-ended output for coherent amplitude demodulators, and it may be even better for simultaneous multiplexing. For large common mode voltages, either in multiplexers, amplifiers or demodulators, it is better to use a floating capacitor with single-ended output.

## III. EXPERIMENTAL RESULTS AND DISCUSSION

The circuit shown in Fig. 1 was built using CMOS switches (CD4053B and MAX303). As the results were similar for both models, only those for the CD4053B are presented. The circuit output was connected to an instrumentation amplifier. The same circuit was used either as an amplifier or as a coherent demodulator. When working as an amplifier, the switching frequency must be much higher than the frequency of the (differential) input signal. When working as a coherent demodulator, the switching frequency was the carrier frequency. The reference circuit had $C_S = C_H = 1$ $\mu$F, duty cycle 10% for the clock signal (10% sample, 90% hold) and the unknown parasitic capacitances inherent to components and circuit layout. Both output configurations, fully differential and single ended, were tested for each circuit.

Table I shows the CMRR for the demodulator when the following amplifier was the INA 110 with a gain of 500 (for the fully differential demodulator) or 100 (for the demodulator with single-ended output). Here the amplifier works at DC and, from the data sheet, its typical CMRR at dc is 110 dB for gains of 100 and higher. We first measured the reference circuit. The first row in Table I shows that if the carrier frequency is low, the amplifier according to (11) limits the CMRR for the fully differential circuit. But from 10 kHz up, there is a reduction in CMRR attributable to the demodulator. Nevertheless, the CMRR is very high. When the output of the floating capacitor circuit is grounded the demodulator determines the overall CMRR. It decreases by 8 dB at 10 Hz, as predicted by (10), and 30 dB at 100 kHz.

Next, it was verified that, as predicted by the theoretical models, $C_H$ had no influence on the CMRR. A reduced duty cycle $\alpha$, however, resulted in a reduced CMRR at high frequencies. Table I shows the results for $\alpha = 5\%$. An analysis was then made of the influence of $C_S$. When $C_S$ was reduced from 1 $\mu$F to 100 nF, the low-frequency CMRR for the fully differential demodulator first increased by about 20 dB, from 107 to 126 dB. This can be explained by (11) if each stage has a CMRR with opposite sign. By the same token, if the input terminals for the amplifier are inverted, the CMRR should decrease. Effectively, it reduced to 107 dB, the same as for the reference circuit. For the single-ended demodulator, when $C_S = 100$ nF the CMRR reduced by about 20 dB, as predicted by (10).

The parasitic impedance was then increased by connecting a 100 pF capacitor, first from the top side to ground, in parallel with $C_{s1}$, and next from the bottom side to ground, in parallel with $C_{s2}$. Again, the CMRR increased (or decreased) for the fully differential demodulator and was smaller for the single-ended demodulator, as predicted by (10). Note that inverting input connections for the instrumentation amplifier works in opposite ways for $C_{s1}$ and $C_{s2}$. In addition, $C_{s2}$ should not affect the results for the single-ended circuit, but from 1 kHz up, a large $C_{s2}$ reduces the CMRR.

When the floating capacitor was used to amplify low frequency signals (0.1 Hz), the results for the frequency dependence of the CMRR (Table II) were similar to those for the demodulator, as expected. For 1 Hz and 10 Hz input signals it is necessary to increase the minimal sampling frequency, but otherwise the results are the same.

The INA114 was also used as a differential amplifier. For the fully differential circuit the CMRR increased to about 120 dB at low frequencies because the INA114 has a better CMRR at dc than the INA110. The CMRR for the fully differential circuit at higher frequencies and for the single-ended circuit was similar.

TABLE II
FREQUENCY DEPENDENCE OF THE CMRR (dB) OF AN AMPLIFIER BASED ON A FLOATING CAPACITOR CIRCUIT WHEN THE INPUT SIGNAL IS 0.1 HZ. FD: FULLY DIFFERENTIAL FLOATING CAPACITOR; SE: FLOATING CAPACITOR WITH SINGLE-ENDED OUTPUT

| Sampling Frequency | | 10 Hz | 100 Hz | 1 kHz | 10 kHz | 100 kHz |
|---|---|---|---|---|---|---|
| Reference Circuit | FD | 106 | 105 | 105 | 96 | 79 |
| | SE | 96 | 96 | 89 | 71 | 52 |
| Duty cycle=5% | FD | 105 | 104 | 104 | 92 | 74 |
| | SE | 95 | 95 | 83 | 65 | 46 |
| Reference circuit with Cs=100 nF | FD | 103 | 104 | 104 | 102 | 80 |
| | SE | 77 | 76 | 76 | 69 | 52 |
| Reference circuit with $C_{s1}$=100 pF | FD | 111 | 110 | 111 | 119 | 97 |
| | SE | 79 | 79 | 74 | 58 | 39 |
| Reference circuit with $C_{s2}$=100 pF | FD | 101 | 102 | 101 | 101 | 96 |
| | SE | 95 | 95 | 80 | 59 | 39 |

## IV. CONCLUSIONS

The floating-capacitor circuit provides an excellent CMRR when used as fully differential amplifier or demodulator. The CMRR for the floating-capacitor circuit with single-ended output, depends on the ratio between the capacitance of the sampling capacitor $C_S$ and stray capacitance from the circuit high side to ground (10). Second-order effects reduce the CMRR at frequencies above 1 kHz. This reduction is greater for the single-ended circuit.

Whatever the application, the floating-capacitor circuit requires a following amplifier providing voltage gain and low output impedance. If the signal, once amplified, must be single ended, then it may be better to have a floating capacitor with single-ended output in amplifiers and some multiplexers while in demodulators a floating capacitor with differential output yields a better CMRR. For large common mode input voltages, it is also better to use a floating capacitor with single-ended output.

## REFERENCES


[1] J. Williams, "Applications for a switched-capacitor building block," Application Note 3, Linear Technology Inc., Milpitas, CA, July 1985.

[2] R. C. Jaeger, "Tutorial: Analog data acquisition technology, Part III—Sample-and-holds, instrumentation amplifiers, and analog multiplexers," *IEEE Micro*, vol. 2, pp. 20–35, Nov. 1982.

[3] D. H. Sheingold, Ed., *Analog-Digital Conversion Handbook*, 3rd ed. Englewood Cliffs, NJ: Prentice-Hall, 1986.

[4] P. H. Garrett, *Advanced Instrumentation and Computer I/O Design.* New York: IEEE Press, 1994.

[5] R. Pallás-Areny and O. Casas, "A novel differential synchronous demodulator for ac signals," *IEEE Trans. Instrum. Meas.*, vol. 45, pp. 413–416, Apr. 1996.

[6] K. R. Laker and W. M. C. Sansen, *Design of Analog Integrated Circuits and Systems.* New York: McGraw-Hill, 1994.

[7] R. Pallás-Areny and J. G. Webster, "Common mode rejection ratio for cascaded differential amplifier stages," *IEEE Trans. Instrum. Meas.*, vol. 40, pp. 677–681, Aug. 1991.

[8] ——, "Common mode rejection ratio in differential amplifiers," *IEEE Trans. Instrum. Meas.*, vol. 40, pp. 669–676, Aug. 1991.



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