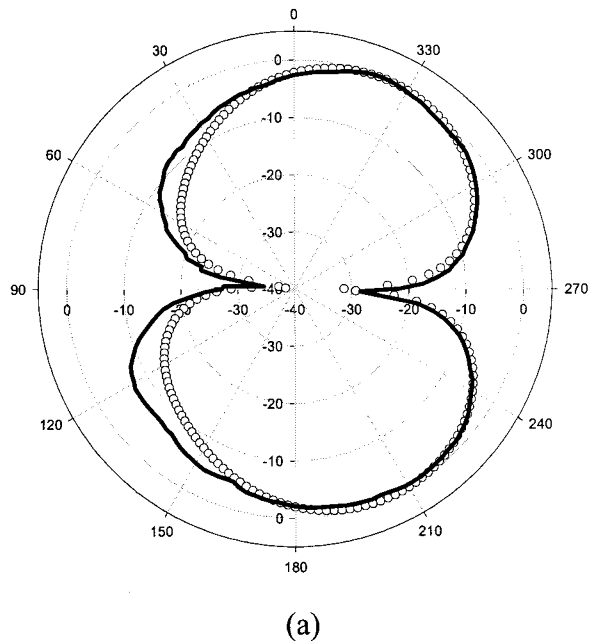

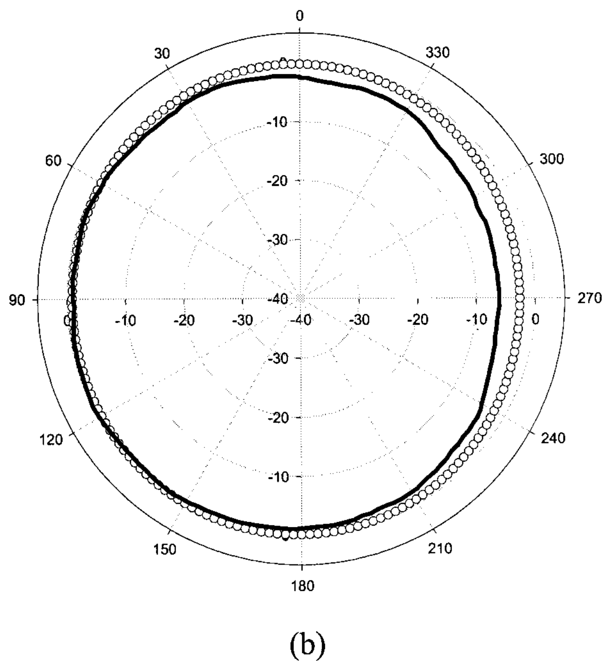

Figure 3 Radiation patterns in the (a) *x–z* and (b) *y–z* planes: ○○○ computed result; — measured result

4 mm and $L_B = 3$ mm, the first and third resonances occur at 1.82 and 2.04 GHz, respectively.

As seen in Figure 1(b) and (c), the fabricated antenna is sitting on the left upper corner of FR4 substrate ($66 \times 30 \times 1$ mm^3, $\varepsilon_r = 4.2$) in consideration of its placements in a handset. The antenna is fed by 50Ω grounded coplanar waveguide (CPW) input line.

3. RESULTS

In order to validate the behavior of the proposed antenna, numerical simulation has been carried out with Microwave Studio™ (MWS). The fabricated antenna with the selected dimensions was measured using an Agilent 8510C Network Analyzer. The measured and simulated return losses are compared in Figure 2 and are in reasonably good agreement with each other. From the measured results, it is seen that the operating frequency is in the range of 1.75–2.17 GHz with impedance bandwidth of 21.4% at VSWR $<$ 2.0. It is confirmed that the proposed antenna can be used in the KPCS/IMT-2000 dual band.

Radiation patterns have been simulated and measured at the frequency of 1.89 GHz. The simulated and measured radiation patterns of the *x–z* and *y–z* planes are shown in Figure 3(a) and (b), respectively. As seen in Figure 3, there is good agreement between the measured and simulated results. Note that the radiation patterns are approximately omnidirectional and similar to that of a monopole antenna. Both simulated and measured antenna gains in the *x–z* plane have 2.6 dBi.

4. CONCLUSION

It has been demonstrated that the proposed antenna with branch structure provides a wide impedance bandwidth of 21.4% based on VSWR $<$ 2, maximum measured gain of 2.6 dBi, and an omnidirectional radiation pattern similar to that of a monopole antenna. Its advantages in terms of the cost, size, and ease of surface-mount assembly are attractive features for KPCS/IMT-2000 applications.

ACKNOWLEDGMENT

This work was supported by the National Research Laboratory (NRL) of the Ministry of Science and Technology, Korea, under contract no. M1-0203-00-0015.

REFERENCES

1. K. Noguchi, N. Yasui, M. Mizusawa, S.I. Betsudan, and T. Katagi, Increasing the bandwidth of a two-strip meander-line antenna mounted on a conducting box, IEEE AP-S 4 (2001), 112–115.
2. M. Ali and S.S. Stuchly, A meander-line bow-tie antenna, IEEE AP-S 3 (1996), 1566–1569.
3. W. Choi, S. Kwon, and B. Lee, Ceramic chip antenna using meander conductor lines, Electron Lett 37 (2001), 933–934.
4. S.H. Sim, C.Y. Kang, S.J. Yoon, Y.J. Yoon, and H.J. Kim, Broadband multilayer Ceramic chip antenna for handsets, Electron Lett 38 (2002), 205–207.
5. J.I. Moon and S.O. Park, Dielectric resonator antenna for dual-band PCS/IMT-2000, Electron Lett 36 (2000), 1002–1003.

© 2004 Wiley Periodicals, Inc.

NOISE MODEL OF A REVERSE-BIASED COLD-FET APPLIED TO THE CHARACTERIZATION OF ITS ENR

M. C. Maya, A. Lázaro, and L. Pradell
Universitat Politècnica de Catalunya (UPC),
Dept. TSC Campus Nord UPC—Mòdul D3
08034, Barcelona, Spain

Received 29 July 2003

ABSTRACT: *This paper presents a broadband-noise circuit model for a "cold"-FET (V_{ds} = 0 V) with a reverse-biased gate. The noise model includes two intrinsic uncorrelated noise-current sources whose spectral densities are determined from measurement of the device's* S *parameters and noise powers. The model is used to characterize the device's excess*

noise ratio (ENR) for application to full receiver-noise calibration. Experimental results up to 40 GHz are given. © 2004 Wiley Periodicals, Inc. Microwave Opt Technol Lett 40: 326–330, 2004; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.11370

Key words: *on-wafer noise source; excess noise ratio; small-signal model; noise model*

1. INTRODUCTION

Noise sources based on active devices such as FETs in a one-port configuration have been proposed in the literature [1–3] as an alternative to avalanche-noise diodes (normally included in coaxial and waveguide noise sources) [4, 5] and other devices [6]. In [1], a FET is used as an equivalent "cold" source, and more recently a FET-based cold/hot noise source [2] has been proposed, where the selection between states is obtained through device-bias control and switching the device input port between the gate-source and drain-source ports, respectively. To extend the operating bandwidth, a MMIC active cold load has been proposed [3], composed of two MMIC cold-load circuits designed to cover the 2–10-GHz and 10–26-GHz ranges, respectively. While FET-based noise sources present the advantage of being easily compatible with microwave on-wafer measurement systems [7], it is necessary to know their excess noise ratio (ENR) in a wide frequency range, in order to be able to calibrate the noise receiver. To determine the noise-source ENR, usually its output-noise temperature is measured with a receiver previously calibrated, using a well-known room-temperature and/or cryogenic noise reference [1–4, 6]. In a preceding work [5], it has been shown that equivalent noise models for the noise devices are useful in the determination of their ENR, because they help to reduce measurement uncertainty, in particular, when the device's reflection-coefficient magnitude is high, as occurs in unmatched on-wafer FET or avalanche-diode-noise sources.

In this paper, a method to extract the noise circuit-model of a cold-FET ($V_{ds} = 0$) with a reverse-biased gate is presented. The cold-FET is used as an on-wafer "hot" noise source in a one-port configuration, with the gate-source port as the output noise port, while the drain-source port is loaded with an arbitrary reflection coefficient. The model is used to estimate the device noise temperature and, therefore, characterize its ENR. The noise analysis is performed from noisy networks theory in order to derive an expression for the device output's noise-current spectral density as a function of its intrinsic noise sources. Then, using broadband S parameters and noise-power experimental measurements as a function of frequency, a regression technique is applied for the best fit between the measured and estimated "multiplier" factor M associated to the noise sources, in order to "estimate" the device's ENR, thus reducing the measurement uncertainty. Experimental results of the estimated M and ENR of a 2×50 μm gate-width DPD-SQW HEMT up to 40 GHz are presented and applied to perform full receiver noise calibration.

2. NOISE MODEL FOR A REVERSE-BIASED "COLD"-FET

Figure 1 shows the small-signal equivalent circuit of a cold-FET ($V_{DS} = 0$) with the gate reverse-biased ($V_{GS} < 0$), including the noise sources associated with the passive components and two intrinsic uncorrelated noise sources associated with the gate-source and gate-drain diodes, i_{gs} and i_{gd}, respectively [7]. It is assumed that all passive components, except i_{gs} and i_{gd}, introduce thermal noise. The noise-current spectral density of the gate noise source can be expressed as [7]:

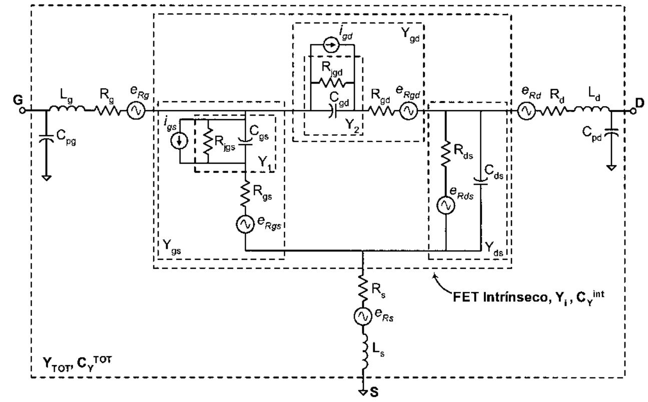

Figure 1 Equivalent circuit of a reverse-biased cold-FET, including two intrinsic noise current sources

$$\overline{i_{gs}^2} = 2qI_{GS}M^2 \tag{1}$$

where I_{GS} is the gate-source DC-bias current, q is the electron charge, and M is a breakdown multiplier factor that has a low-pass frequency dependence [9]. An analogue expression can be written for the gate-drain diode. Note that if the FET layout is symmetrical with $I_{GS} = I_{GD}$, the breakdown multiplier factors and the current spectral-densities are the same ($\overline{i_{gs}^2} = \overline{i_{gd}^2}$).

2.1. Extraction of the Small-Signal Equivalent Circuit Elements

The extrinsic elements, R_g, R_d, R_s, L_g, L_d, L_s, C_{pg}, and C_{pd}, represent the access and contact resistances and the pad effects, and they are assumed to be bias-independent. To obtain these elements, first the transistor is pinched-off, and C_{pg} and C_{pd} are computed from the imaginary part of its Y parameters using the method proposed in [10]. Then the transistor is forward-biased ($V_{GS} > 0$, $V_{DS} = 0$), and L_g, L_s, and L_d are computed from the imaginary part of its Z parameters, and R_s, R_g, and R_d from the real part of its Z parameters using a procedure similar to [11].

Once the extrinsic elements are known, the intrinsic Y matrix, Y_i (Fig. 1), is readily obtained, and the intrinsic parameters are calculated from identification with π-branch admittances Y_{gs}, Y_{gd}, and Y_{ds}. Elements R_{ds} and C_{ds} are computed from the real and imaginary parts of Y_{ds}, respectively. The junction resistances (R_{jgs}, R_{jgd}), intrinsic capacitances (C_{gs}, C_{gd}), and channel resistances (R_{gs}, R_{gd}), are estimated from admittance Y_{gs} and Y_{gd} as functions of the frequency. The frequency dependence of Y_{gs} is

$$\frac{1}{Y_{gsi}} = Z_{gsi} = \frac{(R_{gs} + R_{jgs}) + s_i(R_{gs}R_{jgs}C_{gs})}{1 + s_iR_{jgs}C_{gs}}, \tag{2}$$

where $s = j\omega$, ω is the angular frequency, i ($=1, \ldots, N$) is the frequency index, and N is the number of measured frequency points. An expression similar to Eq. (2) can be written for Y_{gd}. From Eq. (2), a linear equation system is obtained:

$$[Z_{gsi}] = [1 \quad s_i \quad -s_iZ_{gsi}] \cdot \begin{bmatrix} R_{gs} + R_{jgs} \\ R_{gs}R_{jgs}C_{gs} \\ R_{jgs}C_{gs} \end{bmatrix}. \tag{3}$$

The system of Eq. (3) is solved for $R_{gs} + R_{jgs}$, $R_{jgs}C_{gs}$, and $R_{gs}R_{jgs}C_{gs}$ using the pseudo-inverse method. The results are used as initial estimates in an iterative Newton gradient-conjugate method to obtain the final values.

2.2. Noise Model

The procedure to obtain a noise model of the reverse-biased cold-FET is based on determining its total noise correlation matrix in admittance configuration, $\mathbf{C_Y^{TOT}}$ (see Fig. 1) and its equivalent output noise current spectral density, $\overline{i_o^2}$. To obtain $\mathbf{C_Y^{TOT}}$, first the expression for the intrinsic "admittance" noise correlation matrix $\mathbf{C_Y^{int}}$ is written in terms of the gate and drain noise-current spectral densities, $\overline{i_{gs}^2}$ and $\overline{i_{gd}^2}$, respectively, and the thermal noise sources associated with the intrinsic resistances, $\overline{e_{R_{gd}}^2} = 4T_a kR_{gd}$, $\overline{e_{R_{gs}}^2} = 4T_a kR_{gs}$, and $\overline{e_{R_{ds}}^2} = 4T_a kR_{ds}$, given by

$$\mathbf{C_Y^{int}} = \mathbf{H}_0 \cdot \begin{bmatrix} \overline{i_{gs}^2} & 0 \\ 0 & \overline{i_{gd}^2} \end{bmatrix} \cdot (\mathbf{H}_0)^{\dagger} + 4kT_a(\mathbf{H}_1 \cdot \mathbf{Y}_p \cdot \mathbf{H}_1^{\dagger}), \qquad (4)$$

where the superscript † indicates the transpose-conjugate operator, k is the Boltzmann constant, T_a is the room temperature, $\mathbf{H}_0$ is a conversion matrix from an $i_{gs} - i_{gd}$ noise-source configuration (see Fig. 1) to an "admittance" noise-source configuration, and the term $4 \cdot k \cdot T_a \cdot (\mathbf{H}_1 \cdot \mathbf{Y}_p \cdot \mathbf{H}_1^{\dagger})$ is the thermal noise contribution of the intrinsic elements:

$$\mathbf{H}_0 = \begin{bmatrix} 1 & 1 \\ 0 & -1 \end{bmatrix} \cdot \begin{bmatrix} \dfrac{Y_{gs}}{Y_1} & 0 \\ 0 & \dfrac{Y_{gd}}{Y_2} \end{bmatrix}; \quad \mathbf{H}_1 = \begin{bmatrix} 1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix};$$

$$\mathbf{Y}_p = \begin{bmatrix} R_{gs}|Y_{gs}|^2 & 0 & 0 \\ 0 & R_{gd}|Y_{gd}|^2 & 0 \\ 0 & 0 & \dfrac{1}{R_{ds}} \end{bmatrix}. \qquad (5)$$

In Eq. (5), Y_{gs} and Y_{gd} are the π-branch admittances, where the former is given by Eq. (2) and a similar expression can be written for Y_{gd}, and Y_1 and Y_2 are the gate-source and drain-source diode admittances, respectively, as shown in Figure 1.

Next, the intrinsic admittance noise correlation matrix $\mathbf{C_Y^{int}}$ is transformed into the "impedance" representation and the thermal-noise sources of the parasitic resistances, $\overline{e_{R_g}^2} = 4T_a kR_g$, $\overline{e_{R_d}^2} = 4T_a kR_d$, and $\overline{e_{R_s}^2} = 4T_a kR_s$, are added [12]. The resultant correlation matrix, $\mathbf{C_Z}$, is expressed as follows:

$$\mathbf{C_Z} = \mathbf{Z}_i \cdot \mathbf{C_Y^{int}} \cdot \mathbf{Z}_i^{\dagger} + 4kT_a\mathbf{R}, \qquad (6)$$

where

$$\mathbf{R} = \begin{bmatrix} R_g + R_s & R_s \\ R_s & R_d + R_s \end{bmatrix} \qquad (7)$$

and $\mathbf{Z}_i$ $(=[\mathbf{Y}_i]^{-1})$ is the intrinsic impedance matrix (see Fig. 1). Finally, $\mathbf{C_Z}$ is transformed into the admittance configuration to obtain the total admittance noise correlation matrix $\mathbf{C_Y^{TOT}}$. The resulting expression is given by

$$\mathbf{C_Y^{TOT}} = \mathbf{Y}(\mathbf{Z}_i \cdot \mathbf{C_Y^{int}} \cdot \mathbf{Z}_i^{\dagger} + 4kT_a \cdot \mathbf{R})\mathbf{Y}^{\dagger}, \qquad (8)$$

where $\mathbf{Y}$ is the device admittance matrix.

Once $\mathbf{C_Y^{TOT}}$ has been determined, the equivalent output noise current spectral density $\overline{i_o^2}$ referred to the FET gate-source (G-S) port, can be derived. It is assumed that the drain-source (D-D) port is connected to an arbitrary admittance, Y_S. The analysis is as follows. The reverse-biased cold-FET is a noisy two-port that can be represented (see Fig. 2) as a noiseless two-port with two noise-current sources, i_{n1} and i_{n2}, connected at the G-S port (2-2′) and D-S port (1-1′), respectively (admittance configuration). The thermal noise source, i_s, associated with the Y_S admittance is also considered. From analysis of noisy two-ports in admittance representation [13], the following expression for I_1 is obtained:

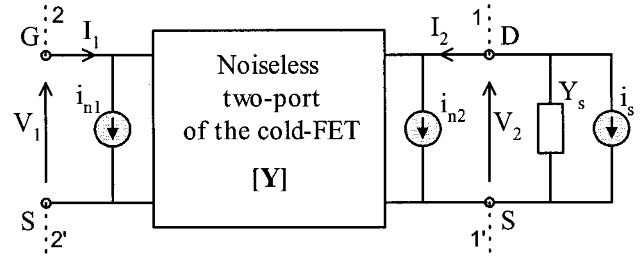

Figure 2 Noise representation of the reverse-biased cold-FET including equivalent noise current-sources at input i_{n1} and output i_{n2} (gate-source port and drain-source ports, respectively) with an arbitrary termination admittance connected to the drain-source port

$$I_1 = \left(Y_{11} - \frac{Y_{12}Y_{21}}{Y_S + Y_{22}}\right)V_1 - \frac{Y_{12}i_{n2} + Y_{12}i_s}{Y_S + Y_{22}} + i_{n1}. \qquad (9)$$

The second and third terms in Eq. (9) are the noise contribution to the total current at the gate-source port. We denote this contribution as i_o:

$$i_o = i_{n1} + P(i_{n2} + i_s), \qquad (10)$$

where

$$P = -\frac{Y_{12}}{Y_{22} + Y_S}. \qquad (11)$$

Then, assuming that i_s is not correlated with i_{n1} and i_{n2}, the output noise current spectral density $\overline{i_o^2}$ is given by

$$\overline{i_o^2} = |P|^2\overline{i_s^2} + \overline{i_{n1}^2} + |P|^2\overline{i_{n2}^2} + P^*\overline{i_{n1}i_{n2}^*} + P\overline{i_{n2}i_{n1}^*}. \qquad (12)$$

The self and cross-power spectral densities of the noise sources i_{n1} and i_{n2} [12] can be arranged in matrix form $\mathbf{C_Y^{TOT}}$, thus obtaining

$$\overline{i_o^2} = |P|^2\overline{i_s^2} + [1 \quad P] \cdot \mathbf{C_Y^{TOT}} \cdot [1 \quad P]^{\dagger}, \qquad (13)$$

where

$$\mathbf{C_Y^{TOT}} = \begin{bmatrix} \overline{i_{n1}^2} & \overline{i_{n1}i_{n2}^*} \\ \overline{i_{n2}i_{n1}^*} & \overline{i_{n2}^2} \end{bmatrix}. \qquad (14)$$

The total admittance noise-correlation matrix $\mathbf{C_Y^{TOT}}$ was obtained in Eq. (8). Substituting (8) into (14), $\overline{i_o^2}$ is written as the sum of a contribution due to the intrinsic noise sources, $\overline{i_{gs}^2}$ and $\overline{i_{gd}^2}$, and a contribution due to thermal noise $\overline{i_{oe}^2}$ (known from small-signal analysis):

$$\overline{i_o^2} = \mathbf{H}\begin{bmatrix} \overline{i_{gs}^2} & 0 \\ 0 & \overline{i_{gd}^2} \end{bmatrix} \cdot \mathbf{H}^{\dagger} + \overline{i_{oe}^2}, \qquad (15)$$

$$\overline{i_{oe}^2} = 4kT_a(\mathbf{U} \cdot \mathbf{R} \cdot \mathbf{U}^{\dagger} + (\mathbf{Q} \cdot \mathbf{H}_1) \cdot \mathbf{Y}_p \cdot (\mathbf{Q} \cdot \mathbf{H}_1)^{\dagger} + |P|^2\mathrm{Re}(Y_S)), \qquad (16)$$

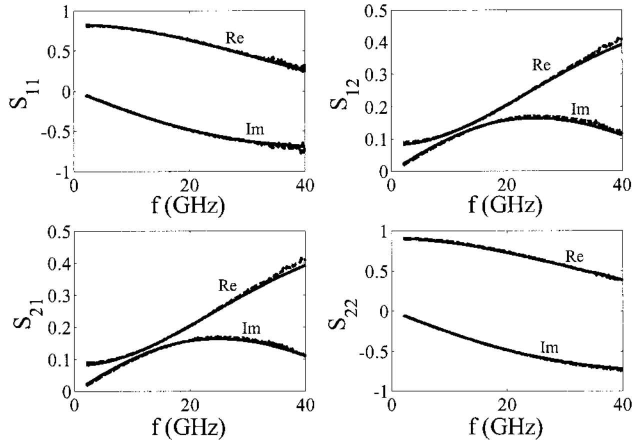

Figure 3 *S* parameters of a reverse-biased cold-FET, with $I_{GS} = 0.87$ mA, measured (– –) and estimated (–)

$$\mathbf{U} = [1 \quad P] \cdot \mathbf{Y}, \quad \mathbf{Q} = \mathbf{U} \cdot \mathbf{Z}_i, \quad \mathbf{H} = \mathbf{Q} \cdot \mathbf{H}_0. \tag{17}$$

From Eq. (15), the output current spectral density $\overline{i_o^2}$ can be computed if $\overline{i_{gs}^2}$ (or $\overline{i_{gd}^2}$ if they are assumed to be the same) are known; however, to compute these terms the multiplier factor M must be known [see Eq. (1)]. Since M depends on the reverse-biased cold-FET physical characteristics under prebreakdown conditions, that is, drift and avalanche zone width, ionization coefficient, and saturation drift velocity (which typically are not known), the calculation of M can be difficult. Alternatively, $\overline{i_o^2}$ can be expressed as a function of the device noise temperature T_d and its admittance Y_d, both measured at the gate-source port (plane 2-2′ in Fig. 2):

$$\overline{i_o^2} = 4k \cdot T_d \cdot \mathrm{Re}(Y_d). \tag{18}$$

Considering the assumption that $\overline{i_{gs}^2} = \overline{i_{gd}^2}$, substituting (18) into (15), and solving for $\overline{i_{gs}^2}$, the next expression is derived as follows:

$$\overline{i_{gs}^2} = (4k \cdot T_d \cdot \mathrm{Re}(Y_d) - \overline{i_{oe}^2}) \cdot (\mathbf{H} \cdot \mathbf{H}^{\dagger})^{-1}. \tag{19}$$

Finally, using (19) in (1), the multiplier factor M^2 is determined at each frequency:

$$M^2 = \frac{\overline{i_{gs}^2}}{2qI_{GS}}. \tag{20}$$

To measure the reverse-biased cold-FET noise temperature T_d and its gate-source admittance Y_d, an experimental on-wafer setup, and calibration and measurement procedures such as those described in [5], are used. To reduce the jitter in the computed factor M^2 (due to random measurement errors in T_d and Y_d), a simple regression technique in log scale is applied to M^2 for a sufficient number of frequency points, in a similar way as that proposed in [5]. Thus, a smooth characteristic over the frequency is obtained for M^2, in agreement to theoretical predictions [9]. Then, $\overline{i_o^2}$ is calculated again from Eqs. (1) and (15), estimated T_d (T_d^{est}) is computed from Eq. (18), and the ENR estimated of the reverse-biased cold-FET is found by using

$$ENR = 10 \cdot \log\left(\frac{T_d^{est}}{T_0} - 1\right), \tag{21}$$

where T_0 (=290°K) is the standard temperature.

TABLE 1 Values of the Equivalent-Circuit Element of a Reversed-Biased Cold-FET with I_{GS} = 0.87 mA

Extrinsic Elements		Intrinsic Elements	
C_{pg} (fF)	7.43	C_{gs} (fF)	23.74
C_{pd} (fF)	19.58	C_{gd} (fF)	25.01
L_g (pH)	34.44	C_{ds} (fF)	6.56
L_d (pH)	19.58	R_{jgs} (kΩ)	0.99
L_s (pH)	1.62	R_{jgd} (kΩ)	1.06
R_g (Ω)	2.63	R_{gs} (Ω)	2.28
R_d (Ω)	3.72	R_{gd} (Ω)	0.01
R_s (Ω)	5.16	R_{ds} (kΩ)	7.95

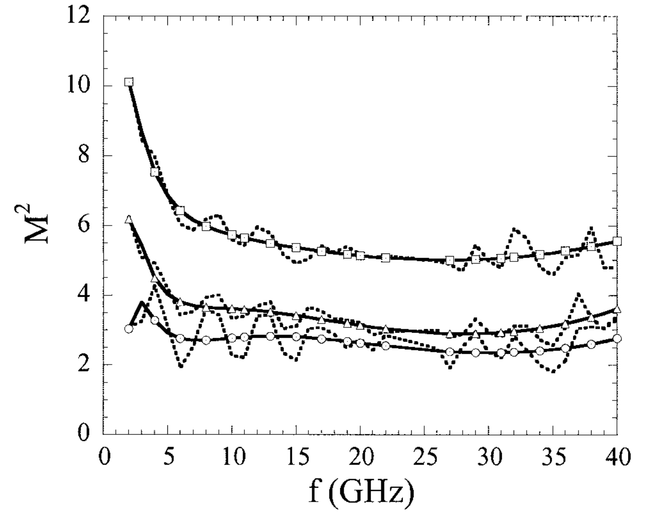

Figure 4 Frequency dependence of multiplier factor M^2 of a reverse-biased cold-FET, measured (– –) and estimated (–), at $I_{gs} = 0.87$ mA (□), $I_{gs} = 0.78$ mA (△), and $I_{gs} = 0.34$ mA (○)

3. EXPERIMENTAL RESULTS

The device characterized in this work is an on-wafer 0.5-μm gate-length, 2 × 50 μm gate-width DPD-SQW HEMT from the

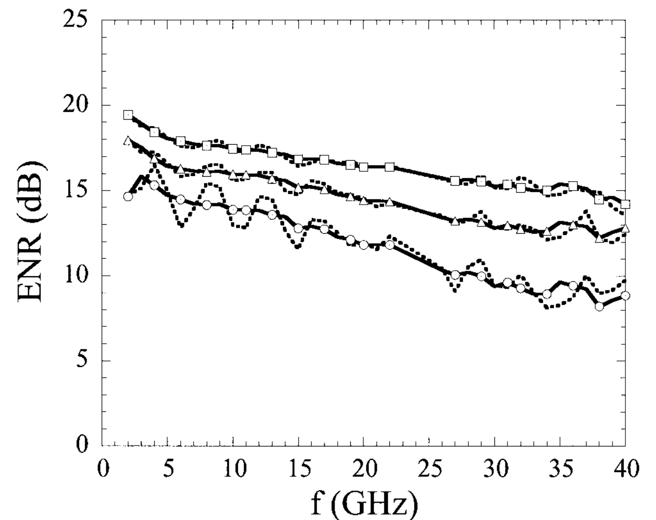

Figure 5 Reverse-biased cold-FET ENR, measured (– –) and estimated (–), at $I_{gs} = 0.87$ mA (□), $I_{gs} = 0.78$ mA (△), and $I_{gs} = 0.34$ mA (○)

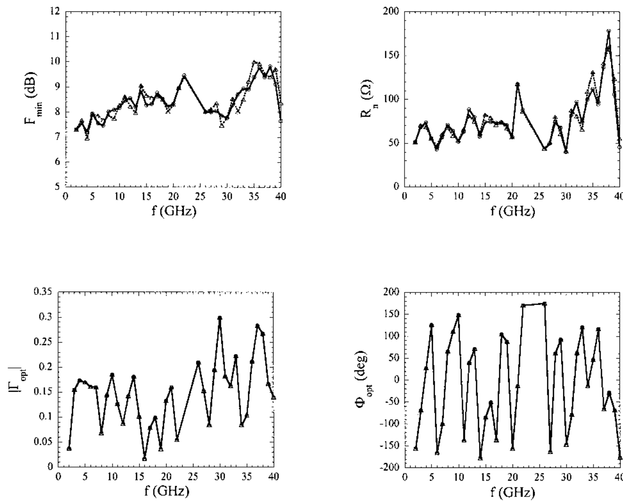

Figure 6 Receiver's noise parameters up to 40 GHz, measured with a coaxial noise-source (–○–) and with an on-wafer noise-source (reverse-biased cold-FET) (– –△– –)

Foundry of Fraunhofer Institut (FhG-IAF), Freiburg, Germany. The gate bias-point is fixed with a current source, close to the transistor breakdown point. Figure 3 plots its measured S parameters, and the estimated values computed using the procedure described in section 2.2, showing very good agreement. Table 1 shows the values obtained for the elements of the equivalent circuit.

From the measured cold-FET noise temperature T_d, the cold-FET multiplier factor M^2, computed using Eq. (20), and its ENR are plotted in Figures 4 and 5, respectively, as a function of frequency, for three bias points. Both exhibit an excessive ripple mainly produced by uncertainties in the measured T_d, due to a high reflection coefficient magnitude $|S_{11}| > 0.6$ [14]. Then, the proposed regression technique is applied for the best fit of the measured multiplier factor M^2 as a function of frequency. Using the result of the regression of M^2, T_d^{est} is estimated and the ENR is estimated from (21). The estimated values of M^2 and ENR are compared with the measurement in Figures 4 and 5. A sensible reduction in the ripples of M^2 and ENR can be observed. The slow variations of the ENR (due to variations of the device output impedance) in the computed ENR, demonstrates that the cold-FET noise model, based on extracting its internal physical noise sources, reduces the ENR measurement uncertainty.

As an application, the previously characterized reverse-biased cold-FET is used as an on-wafer noise source to measure receiver-noise parameters, using the procedure described in [14], and FET noise parameters. Figure 6 compares the receiver-noise parameters measured up to 40 GHz with a coaxial noise source, to those measured with the cold-FET noise source. Good agreement is obtained.

4. CONCLUSION

A noise model of a reverse-biased cold-FET has been presented, in which the expressions of the device output noise-current spectral density as a function of the intrinsic noise sources and their multiplier factor M^2 are determined by application of the noisy networks theory. The noise model has been applied to the characterization of the ENR of the cold-FET, using broadband S parameters and noise-power measurement. To reduce uncertainty in the measured device's ENR, a regression technique is applied to the intrinsic noise-current sources for their best fit with experimental measurements as a function of frequency, using their smooth frequency characteristic. Experimental results up to 40 GHz of the multiplier factor M^2 and the ENR are shown. Also, an application of the reverse-biased cold-FET as on-wafer noise source has been presented, where it has been used to extract the receiver's noise parameters.

ACKNOWLEDGMENTS

This work has been supported by Spanish Government under grants TIC2000-0144P4-02 and ESP2002-04141-C03-02, and a scholarship from CONACYT-Mexico.

REFERENCES

1. R.H. Frater and D.R. Williams, An active "cold" noise source, IEEE Trans Microwaves Theory Tech 29 (1981), 344–347.
2. L.P. Dunleavy, M.C. Smith, S.M. Lardizabal, A. Fejzuli, and R.S. Roeder, Design and characterization of FET based cold/hot noise sources, IEEE MTT-S Dig, Denver, CO (1997), 1293–1296.
3. P.M. Buhles and S.M. Lardizabal, Design and characterization of MMIC active cold loads, IEEE MTT-S Dig, Boston, MA (2000), 29–32.
4. L.P. Dunleavy, J. Randa, D.K. Walker, R. Billinger, and J. Rice, Characterization and applications of on-wafer diode noise, IEEE Trans Microwaves Theory Tech 46 (1998), 2620–2627.
5. M.C. Maya, A. Lázaro, and L. Pradell, Extraction of an avalanche diode noise model for its application as an on-wafer noise source, Microwave Opt Technol Lett 38 (2003), 89–92.
6. P. Béland, S. Labonté, L. Roy, and M. Stubbs, A novel on-wafer resistive source, IEEE Microwave Guided Wave Lett 9 (1999), 227–229.
7. M.C. Maya, A. Lázaro, and L. Pradell, Cold-FET ENR characterization applied to the measurement on-wafer transistor noise parameters, Euro Microwave Conf, 2002, pp. 41–44.
8. K.Y. Lee, B. Lund, T. Ytterdal, P. Robertson, E.J. Martinez, J. Robertson, and M.S. Shur, Enhanced CAD model for gate leakage current in heterostructure field effect transistors, IEEE Trans Electron Devices 43 (1996), 845–851.
9. R.H. Haitz and F.W. Voltmer, Noise of a self-sustaining avalanche discharge in silicon: studies at microwave frequencies, J Appl Phys 39 (1968), 3379–3384.
10. W. Stiebler, M. Matthes, G. Böck, T. Koppel, and A. Schäfer, Bias-dependent cold-(H)FET modeling, IEEE MTT-S Dig, San Francisco, CA (1996), 1313–1316.
11. R. Anholt and S. Swirhun, Equivalent-circuit parameter extraction for cold GaAs MESFET's, IEEE Trans Microwave Theory Tech 39 (1991), 1243–1247.
12. H. Hillbrand and P. Russer, An efficient method for computer aided noise analysis of linear amplifier networks, IEEE Trans Microwave Theory Tech 23 (1976), 235–238.
13. H. Rodhe and W. Dahlke, Theory of noisy fourpoles, Proc IRE 44 (1956), 811–818.
14. A. Lazaro, M.C. Maya, and L. Pradell, Measurement of on-wafer transistor noise parameters without a tuner using an unrestricted noise sources, Microwave J 45 (2002), 20–46.

© 2004 Wiley Periodicals, Inc.