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Schematic Method of Estimation and Increase of Radiation Hardness of the Onboard Radio-electronic Equipment for Space Applications

A. S. Bakerenkov, Y. R. Shaltaeva, A. S. Rodin, N. S. Glukhov,* and V. A. Felitsyn

National Research Nuclear University MEPhI (Moscow Engineering Physics Institute), Kashirskoe shosse 31, Moscow, 115409, Russia

Abstract

Experimental and theoretical justification of a schematic method of estimation and increase of radiation hardness of the onboard radio-electronic equipment for space applications on the example of the standard circuit of the voltage follower combining the most widespread schematic decisions: differential stage, current mirror and emitter follower.

Corresponding Author:
N. S. Glukhov
nsglukhov@gmail.com

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1. Introduction

Impact of the ionizing radiation of space leads to failures of the onboard radio-electronic equipment (REE) of spacecrafts. The problem of radiation hardness assurance of REE for space applications has both a practical and scientific significance. Integrated circuits (ICs) are used in the onboard equipment of spacecrafts for providing satellite communication in GLONASS and GPS systems. A number of projects of Roskosmos, NASA and other companies are directed to increase the radiation hardness of onboard REE. At present, the works on a research of Mars assume to use an electronic instruments for a long time during impact of the ionizing radiation of space. The investigations of deep space that are performed using space located observation equipment, communication with which is carried out with use of REE, are of great interest from the point of view of a cosmology.

Integrated microcircuits are basic elements of modern REE. Thus, the problem of radiation hardness assurance of REE is directly connected with increasing of the radiation hardness of analog and digital ICs. Now there are two approaches for solution of the problem of radiation hardness assurance: perfecting of the production technology of ICs on the basis of a research of physics of radiation effects in semiconductor devices and optimization of traditional schematic decisions. At present, the technology approach is widely used to reach the radiation hardness of modern ICs.

The increasing of the radiation hardness of ICs by technological methods requires large material inputs to improve the technology. The application of schematic methods to increase the radiation hardness allows to achieve the same results without complication of technological process and to decrease material inputs for modernization of processing equipment. Schematic approach allows to increase radiation hardness of ICs without expensive improvement of technological tools. In this work, the estimation technique of lifetime of REE in space radiation environment is based on radiation tests of standard schematic elements and corresponding schematic simulations.

2. Materials and Methods

The application of presented technique will allow to estimate the radiation hardness of REE for space applications at circuit design stage of development and to provide the possibility of choice of the optimal schematic solution from the point of view of radiation hardness. The technique was experimentally tested on the example of traditional circuits: differential stage, current mirror and emitter follower. These circuits are basic elements of schematic of the operational amplifiers (OpAmps) that are widely used in the modern REE for space applications.

The prediction technique of the radiation hardness assumes on the basis of schematic simulation in the LTSpice IV using the dependence of the value of the current gain of the bipolar transistor on the total dose level, which was obtained experimentally, to calculate the total dose dependence of the input current and to estimate the radiation induced offset of the transmitting characteristic of the standard bipolar transistor follower. The circuit of the follower was chosen for researches as it combines the most widespread schematic decisions: differential stage, current mirror and emitter follower.

3. Results

For the experimental estimation of the accuracy of the prediction of the radiation degradation with use of the described technique the circuit of the follower was developed on integral transistors of a transistor matrix 198NT1A. This chip involves five bipolar NPN transistors fabricated on the common chip to minimize the dispersion of the electrical characteristics. The impact of the ionizing radiation provides identical radiation degradation of parameters of these transistors. It allows to perform the calculation of radiation sensitive parameters of the follower circuit using the results of the measurements of current voltage characteristics of one transistor from the matrix. The use of five discrete transistors does not allow to perform the described approach because of wide technological deviation of their electrical parameters.

4. Conclusion

During experimental investigations, one transistor from the matrix was used as a control device to obtain the dependence of the current gain on total dose level. The input currents and transmitting characteristics of the follower during radiation tests were obtained using the measure equipment, developed in National Research Nuclear University. The performed research showed good correlation of the results of schematic simulations and radiation tests. Since the electrical parameters of ICs are directly connected with both temperature and total dose level we will use the temperature control devices [1, 2] in our following detailed research of this issue.

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