Structure and Optimisation of Liquid Crystal based Phase Shifter for Millimetre-wave Applications

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This dissertation is submitted for the degree of

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Under the supervision of

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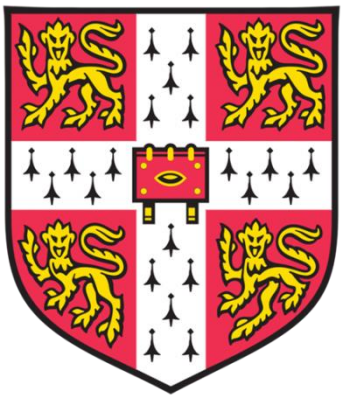

DEPARTMENT OF ENGINEERING

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I hereby declare that except where specific reference is made to the work of others, the contents of this dissertation are original and have not been submitted in whole or in part for consideration for any other degree or qualification in this, or any other University.

This dissertation is the result of my own work and includes nothing which is the outcome of work done in collaboration, except where specifically indicated in the text.

This dissertation contains less than 65,000 words including appendices, bibliography, footnotes, tables and equations and has less than 150 Figs.

Jinfeng Li

11th June. 2018

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Abstract

The delivery of tunable millimetre-wave components at 60GHz is of research and development interests with the advent of 5G era. Among applications such as high-data-rate wireless communications, high-precision automotive radars and hand-gesture sensing, variable phase shifters are vital components for antenna arrays to steer an electromagnetic beam without mechanical movement. However, present microwave technology has limited scope in meeting more and more stringent requirements in wavefront phase control and device performance for those cutting-edge applications in the millimetre-wavelength range. Although some existing microwave switchable techniques (such as RF MEMS and solid-state p-i-n diodes) can offer ultra-fast speed for phase modulation, their binary beam-steering nature is resolution-limited and thereby degrades the beam-scanning performance. In response to this, continuously-tunable phase shifting can be realised by using tunable dielectric materials such as ferroelectric BST and liquid crystals (LCs). BST thin films can offer relatively fast switching and modest tunability. However, the increased dielectric loss beyond 10GHz impedes their implementation for higher frequency applications. By comparison, liquid crystals (LCs) have drawn attention in recent years because of their continuous tunability as well as low losses especially at millimetre-wavebands. The principle of shifting the phase continuously is based on the shape anisotropy of LC molecules for variable polarizabilities and hence tunable dielectric constants, which allows wave speed to be controlled with ease by a low-frequency field of only up to 10V. However, LC-based tunable delay lines are not well established in the frequency regime of 60GHz-90GHz because of the limited status of LC microwave technology in which most of the LC based devices have been designed for below 40GHz. It is the aim of this PhD research to bridge the gap and address future societal needs based on our group's focus and experience in developing cutting-edge LC-based agile microwave components.

In this work, a liquid crystal (LC) based 0-180˚continuously-variable phase shifter is developed with insertion loss less than -4.4dB and return loss below -15dB across a wide spectrum from 54GHz to 67GHz. The device is driven by a 0-10V AC bias and structured in a novel enclosed coplanar waveguide (ECPW) including an enclosed ground plate in the design, which significantly reduces the instability due to floating effects of the transmission line. This structure screens out interference and stray modes, allowing resonance-free quasi-TEM wave

propagation up to 90GHz. The tunable ECPW is optimised by competing spatial volume distribution of the millimetre-wave signal occupying lossy tunable dielectrics versus low-loss but non-tunable dielectrics and minimising the total of dielectric volumetric loss and metal surface loss for a fixed phase-tuning range. A variety of influences affecting the actual device performance are studied, experimented and optimised. Fabricated prototypes exhibit wideband low-loss performance and 0-π continuous tuning with low power consumptions and high linearity compared with the state-of-the-arts. Potentially, the ECPW-fed phased antenna array will be incorporated with advanced beam-forming algorithms to develop compact beam-steering systems of improved performances and targeted for ultra-high-data-rate wireless communications, inter-satellite communications, current road safety improvement, futuristic autonomous driving, and other smart devices such as the hand-gesture recognition.

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Chapter 1. Millimetre-wave Beam Steering Applications and Technologies

The availability of 60GHz-90GHz spectrum space is promising in response to a rising demand for bandwidth in the context of the congested spectrum below 30GHz.

1.1 60 GHz – 90 GHz Opportunities

Historically, large electrically steered radars were deployed for military applications, such as missile detection/tracking/guidance and fire control, navigation, aircraft surveillance and homeland defence. In addition to the military sector and radio astronomy research (e.g. the Square Kilometer Array (SKA) radio telescope project), phased array antennas also exhibit immerse commercial potential in the Extremely High Frequency band (30GHz-300GHz) for civilian applications, notably the next generation of wireless communications (57GHz-66GHz), satellites communications and navigation systems (60GHz), Intelligent Transport Systems (63GHz-64GHz), as well as the 77GHz automotive multi-beam long-range radars for Adaptive (Autonomous) Cruise Control (ACC), and 79GHz mono-pulse short range radars for vehicle collision avoidance alarm and traffic monitoring functionalities.

1.1.1 Fifth Generation (5G) Mobile Communications (57GHz-66GHz)

The ratification of the IEEE 802.11ad amendment has scoped the 60GHz ISM waveband for consumer wireless communication [74]. In Europe, the frequency range from 57GHz to 66GHz provides a license-free 9GHz bandwidth that allows the possibility of high data-rate (multi-gigabit per second) Wireless Personal Area Network (WPAN) for indoor short-range communications (e.g. supplying wireless multimedia in airplane or car cabins), and other broadband last-mile applications.

In contrast to public bands (2.5GHz and 5GHz) currently deployed for WiFi, 60GHz is susceptible to the following issues that limit its usage in wireless communications.

[1] Elevated free-space path loss (increases with frequency) according to the Friis transmission formula. As compared with 5GHz, there can be an additional -22dB of signal attenuation for 60GHz at a propagation distance of 10m (a typical range suggested by the IEEE 802.11ad).

[2] Substantial atmospheric absorptions (98% of 60GHz energy is absorbed by oxygen) and severe rain attenuations in the 60GHz band, which gets more pronounced at ranges beyond 100 meters. From the isolation point of view, however, the oxygen absorption that peaks at 60GHz allows interference-free deployment of closely-spaced systems co-operating at the same frequency, and hence is beneficial for efficient frequency spectrum reuse.

[3] Struggles to penetrate walls (obstacles in line-of-sight) especially for concrete materials owing to the quasi-optical propagation characteristics and blockage effects followed by 60GHz.

[4] There are not as many mobile and static devices requiring bandwidth at present. Furthermore, devices based on classical semiconductor integrated circuits and waveguide structures struggle to scale down in size, cost, and insertion loss as required by 60GHz.

Phased array antennas can be used to address these challenges by producing a highly directive beam. Incorporated with beam forming techniques, phased array attracts considerable interests in 60GHz ultra-high-data-rate point-to-point wireless communications by orienting high-gain beams towards distant receivers/transmitters. By producing multiple beams to subdivide the cells, phased array finds its application in base stations with decent improvements without constructing new sites. The far-field radiation pattern is shaped by adjusting the phase/amplitude of the radiators or modifying the aperture distribution. The null difference-pattern offers good beam-pointing accuracy, which improves the spectral efficiency and signal-to-noise ratio. Multi-path fading, bit error rate and co-channel interferences are significantly mitigated, thereby allowing broader band operations and higher data rate delivery for modern communication systems. Undesired interference is insignificant due to the high propagation attenuation at 60GHz. Given these benefits, there is a growing progression of the trend to apply phased array technologies to electrical beam steering at 60GHz in preference to conventional mechanical ways.

1.1.2 Inter-satellite Communications (60GHz)

The atmospheric absorption at a geosynchronous altitude of 26000 miles (oxygen-free) is ignorable and hence no longer a concern for 60GHz signal propagation. The last decades have witnessed the development to an increasing extent of terrestrial and satellite services for mobile terminals, airborne and space-based communications. 60GHz inter-satellite communication linking is expected to take advantage of the large bandwidth availability to accommodate the high data-rate capacity required by user satellites (NASA, 1986), and even the emerging multi-spacecraft phase-array communications [8] for deep-space explorations. To track the communication partner between a faster-moving low-earth-orbiting (LEO) satellite and a geostationary orbit (GEO) relay satellite (or between multiple space crafts), electronically steerable phased array antennas play a dominant role in the relay links.

1.1.3 Automotive Radar (76GHz-81GHz)

Performing as eyes and ears of a vehicle, radar is arguably a key component of future generation intelligent cars with fully self-driving functions. Superior over light and acoustic sensing technologies, radar offers many advantages, particularly the sustainability in severe weather or lighting conditions. For device size consideration, 60GHz-90GHz is a suitable frequency range to realise a compact car radar system with improved spatial resolution due to the shorter wavelengths. There are increasing incentives towards a worldwide harmonised frequency allocation for car radars in the 76GHz - 81GHz band (3.7mm<λ<3.9mm) in place of the current 24GHz one (λ=1.25cm), as higher frequency radars enable antenna array size miniaturisation along with weight reduction. Assuming a 64 by 64 antenna array with a pixel pitch of 2 wavelengths, the dimension of a 24GHz radar will be $(2 \times 0.0125 \times 64)^2$=1.6m$\times$1.6m, whereas a 79GHz one by comparison can be scaled to $(2 \times 0.0038 \times 64)^2$=48cm$\times$48cm.

Vehicular radar units have already been commercially exploited in modern upper-class models largely for road safety and comfort purposes, such as 24GHz system (resolution in cm level) for pre-crash and lane departure warning, blind spot surveillance and parking assistance, automatic braking and adaptive cruise control (ACC), etc. Radars exhibit several unique

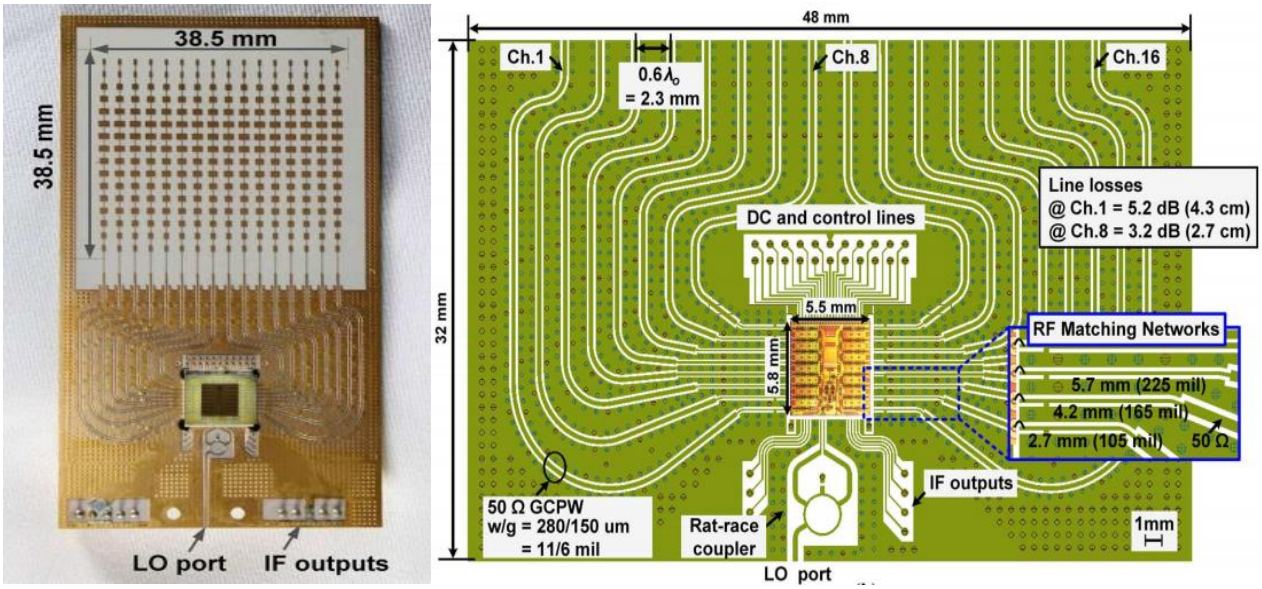
properties when compared with competing/complementing technologies, e.g. ultrasound, video cameras and lidar (Light Detection and Ranging).

Ultrasound sensors (relying on reflected acoustic waves) have limited field of detection and limited resolution by comparison with radar, and hence they are only widely used for parking aid. By contrast with visual observation (optical imaging cameras) and laser-based systems (lidar), radar exhibits robustness to lighting conditions, allowing day and night operations under low visibility and adverse weather conditions (fog, rain, snow, spray). High cost lidar fails to reliably track extremely dirty (non-reflective) vehicles. Furthermore, extreme sunlight and mis-alignment might cause malfunction. It was reported that Google's latest prototype of a driver-free robotic car (based on lidar and video camera) has yet to be tested in snow or heavy rain out of safety concerns [36]. Another technology reported by [12] is the Night Vision system featuring far-infrared thermal imaging cameras, which rely on temperature differences of objects to function, but the image quality problem is still of customer concern. From the aesthetic point of view, lidar, ultrasound and cameras must be mounted outside (e.g. installed in the bumper), whereas radar can conform into the rooftop or body/glass of the car without extra maintenance.

There has recently been a growing interest in fully self-driving cars, i.e. the vehicle performs all safety-critical functions for the entire trip, with the driver anticipated not to get involved in any control [53]. Intelligent combination of smart radars with camera technology would reliably approach tomorrow's driverless challenge [82]. There is enormous opportunity towards a growth in the automation level, i.e. a leap for semi-automated to truly autonomous, as evidenced by the emerging innovation by sensor fusion (i.e. stereo camera, thermal imaging camera and multi-stage radar sensors) in Mercedes-Benz's Intelligent Drive [51].

Current commercially available electronically-scanned multi-ranging car radars (e.g. DENSO 77GHz and Delphi ESR 2.5 SAR) are mostly based on Monolithic GaAs p-i-n diodes or Field Effect Transistors (FET) switches. The state-of-the-art includes a 77GHz-81GHz 16×16 phased array receiver chip with $\pm 50^{\circ}$ horizontal field of view for car radar, as demonstrated by the UC San Diego research team [27]. Fig.1 below shows the standard microstrip antenna array and the controller (i.e. their proposed SiGe BiCMOS phased array chip). The overall

dimension of the radar sensor is only 9.2×4.8cm². The phase modulation is still achieved by active switches-based digital phase shifters (5-bit).



(a) Fully Assembled Antenna Array (b) Control Network

Fig.1 A 77GHz-81GHz Microstrip Antenna Array and Control Network [27]

Note that multiple grounded coplanar waveguides (GCPW with vias) in bended configuration were used for the connection between the SiGe chip and the series-fed microstrip antenna array. The GCPW distributed network causes an average line loss of -3.2dB at the interior and -5.2dB at the periphery of the board due to different line lengths (mostly>3cm).

1.1.4 Gesture Sensing (60GHz)

Besides being compact, millimetre-wave radars also significantly improve the spatial resolution, allowing more accurate object distinction. For instance, a 60GHz-90GHz (3mm<λ<5mm) radar exhibits a very high positional accuracy inherently suitable for capturing tiny motions of human hands. Based on physical principles of 60GHz radiation that were unexplored in interactive applications, [49] presents a millimetre-wave radar prototype built for driver's hand-gesture sensing, which not only enhances convenience, but also the driving safety.

Furthermore, Google's Advanced Technology and Projects group (ATAP) recently launched *Soli* (Fig.2), an interactive computer graphics technology bringing touchless gesture sensing to wearables like a smartwatch and other consumer mobile devices. The demo is essentially a 60GHz radar-on-chip (10mm²), allowing users to intuitively interact with their small-screened

devices by a range of gestures or finger motions, by contrast with traditionally touch-based interface or voice recognition.

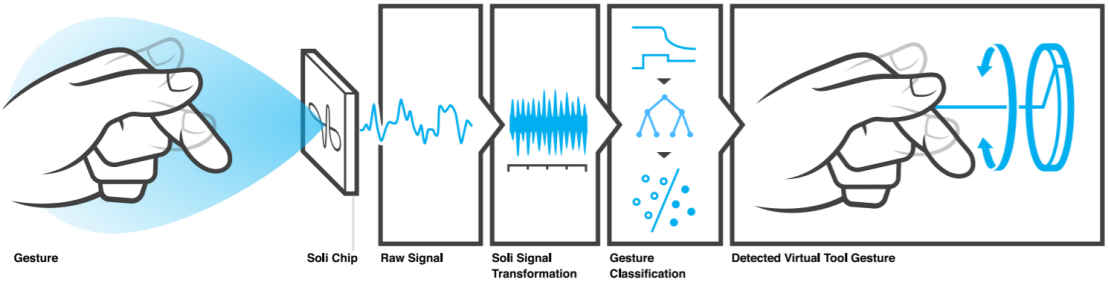


Fig.2 An End-to-end 60GHz Phased Array Radar for Fine Gesture Sensing [33]

This is the first time that ubiquitous gesture interaction is realised by an end-to-end millimetre-wave radar sensing system that incorporates electrically steered antenna arrays with advanced signal processing and machine learning. Such innovation could help to significantly improve user engagement, and presumably revolutionise the smartphone industry.

1.2 Millimetre-wave Beaming Steering Technologies

1.2.1 Conventional Beam Scanning by Mechanically Rotating

Conventional beam scanning technology (by parabolic reflector antennas, satellite dishes and previous automotive radars) has long relied on mechanically rotating (motor-driven) antennas to achieve beam redirecting. Fig.3 shows a parabolic antenna for satellite communications, and a radar dish already decommissioned for air traffic control at London Heathrow Airport.

(a) Satellite Dish in Germany (b) Surveillance Radar (London Heathrow Airport)

Fig.3 Traditional Beam Steering by Mechanically Rotating Antenna

This method is inherently slow, clunky, power-consuming, and difficult in responding rapidly enough to track large numbers of fast-maneuvering targets. Moreover, the large and bulky mechanically controlled parts are susceptible to inertia and vibration of mechanical systems, resulting in poor reliability and high maintenance costs. By contrast with a standard single-pixel rotating parabolic dish antenna, there is an increasing demand for electronic beam steering by phased array antennas as discussed below.

1.2.2 Electrically Steerable Phased Array Antenna

Adaptive phased antenna array is a key technology for 60GHz wireless communications. The future of beam-steerable systems lies in the implementation of electronically steerable phased array technology, with the advantages and limitations outlined below.

1.2.2.1 Advantages of Electronic Beam Steering by Phased Array

As an evolutionary radar technique, the delivery of a phased array antenna is of research and development interests because of the following features. Firstly, adaptive array smart antennas allow steering the beam to a given direction of focus whilst nulling interfering signals. Without resorting to mechanical rotation, the main beam (maximum energy) of a phased array antenna is electrically steered in one or more dimensions by varying the excitation phases of each radiating element, as interpreted in Fig.4 below.

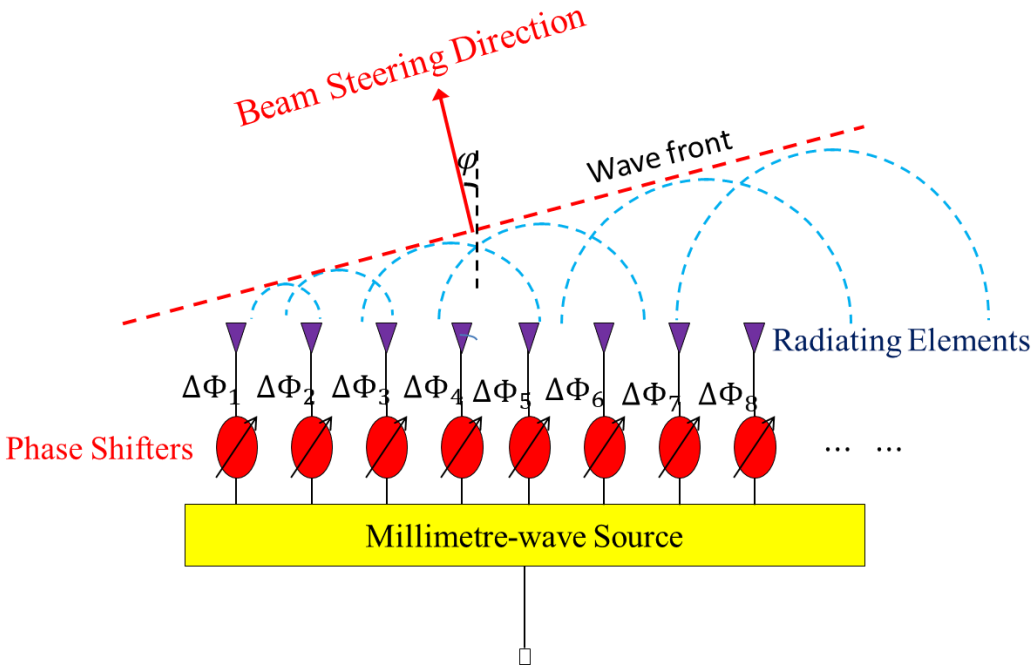


Fig.4 Electronic Beam Steering by Multiple Phase Shifters-Fed Antenna Array (Static)

The inertia-less beam switching rate falls within the order of ~1 μs for certain phased array architectures based on ferroelectrics phase shifters, which outperforms recent advances in mechanical scanning antennas based on RF MEMS. Phased-array based weather-sensing radar would complete a whole-space scanning within 30 seconds, which is far superior to the 4 to 5 minutes required by current mechanical radar systems.

The instantaneous slewing and accurately switching beam-pointing capability allows adaptively programmed multi-mode operations to be performed simultaneously, e.g. multi-target tracking and multi-point communications. Phased arrays also feature far more appreciable reliability and less maintenance costs. Pixel failure with as many as 10% of all the components leads to a loss in gain of only 1 dB, while the system remains operational, and the degradation is graceful. The simultaneous multifunction capability, reconfigurability, and the fault tolerance would contribute to significant cost-effectiveness.

1.2.2.2 Challenges in Phased Array based Electronic Beam Steering System

In the domain of radar and communication systems, the behaviour of a phased array is however far more complex than a passive, mechanically positioned antenna. Apart from the benefits as mentioned, current phased-array technique is still subjected to a range of constraints.

First, the performance characteristics of a phased array antenna are scanning angle dependent. Sensitivity is also a function of beam steering direction and fluctuates across the array field of view. For planar arrays, the maximum useful scanning angle is limited to 60° from broadside. When the beam direction moves away from the broadside, there is a slump in the gain of the array. On the contrary, a mechanical driven antenna can steer a beam with a constant gain at any scanning angle.

Second, radiation pattern is strongly affected by mutual coupling effect, causing significant impedance variations with the scanning angle. Taking phased array vehicular radar for an example, the RF interference (RFI) from on-coming vehicles warrants careful consideration.

The third limitation concerns packaging. For aesthetic reasons in the automotive industry, a phased antennas array to be mounted on a car should be light-weight and low-profile. However, reducing the antenna size would increase the beam width and reduce the angular resolution. Solutions of angular resolution improvement can rely on special signal processing techniques, such as Multiple Signal Classification (MUSIC).

Finally, the quest for decent performance with lower side lobes and wider bandwidth keeps the array costs high. If radiating elements are grouped into several sub-arrays (each equipped with a single delay line as depicted in Fig. 5 below), the required number of phase shifters can be reduced for lower costs, however, the beam scanning range degrades due to the increased side lobes and grating lobes [16].

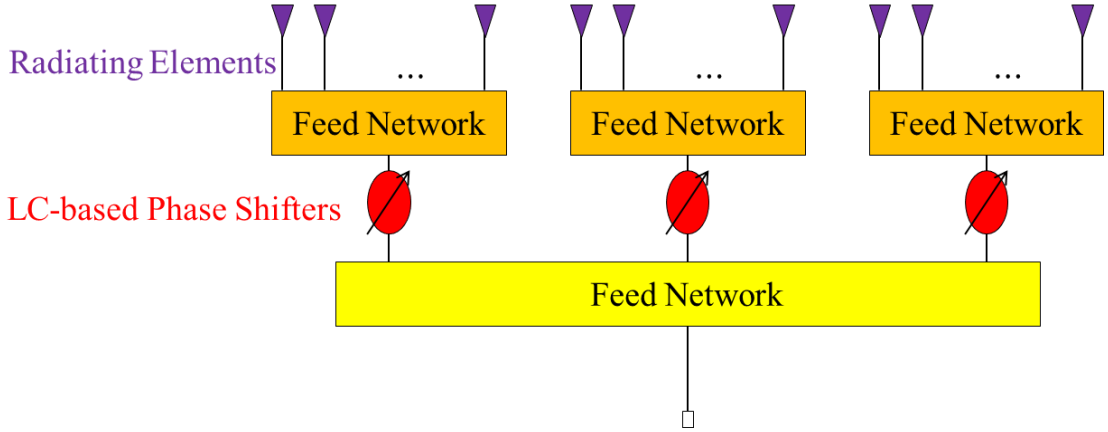


Fig.5 Primary and Secondary Feeding Networks with the Sub-array Concept

For these reasons, commercialised phased arrays have not yet been in widespread use. Automotive radars based on phased array systems are still limited to being equipped in high-end luxury cars such as Mercedes-Benz S-Class [44]. The TracVision A7 antenna system available in the market could provide live satellite television for moving vehicles, but the scanning still partially requires mechanical parts, and the entire hybrid phased array system is still costly, with the retail price reaching $3995. Whereas for mechanically rotating antennas, the absence of multiple phase shifters and amplifiers (even at large scan angles) drives the cost down. In summary, to commercialise the phased array technology, seeking for millimetre-wave phased shifters with improved performance and lower cost is of paramount importance.

1.2.3 Phase Shifting Devices as Key Components in a Phased Array System

As a key component of the phased array antenna system, the phase shifter is of research importance for low-loss beam steering or scanning. In particular, phase shift and insertion loss require a balance of the following performance specifications.

(1) Millimetre-wave 0-360° or 0-180° phase shift, without breaching the constraint placed on insertion loss (e.g. -4dB).

(2) Low variation in insertion loss for the full range of phase shift over the required frequency band, i.e. low insertion loss variation with the biasing control. This is aimed at minimising the beam distortion while steering. As the signal combining and null forming at undesired directions is significantly affected by the amplitude of the signal at each channel, the phase shifters are required to not just exhibit a low insertion loss but also maintain a constant loss within their phase tuning range.

(3) High phase shifting resolution (analogue functionality).

(4) Ease of control (e.g. low frequency bias), linear phase shift-voltage response, low power consumptions (e.g. bias voltage <10V).

(5) Fast response (e.g. ferroelectrics can achieve μs switching).

(6) Robust, reliable (e.g. can work at humid environments and temperature variations).

(7) High power handling capability (required by low-loss high-power transmitter).

(8) Compact for integration.

We can envision the use of this low-loss high-tuning-range phase shifter technology in a phased array transceiver to realise certain function as mentioned above, e.g. 5G mobile communications (57GHz-66GHz in Europe), satellite communications (60GHz), gesture sensing (60GHz), and car radar (76GHz-81GHz), etc. Among all these possibilities, we centre attention around the 5G mobile and satellite communications (57GHz-66GHz).

1.3 Survey of Current Millimetre-wave Phase Shifters and Their Limitations

Electronically beam-steerable phased array antennas rely on efficient wavefront phase control to produce a desirable rapid-moving radiation pattern with single-radar-based high angular resolution without mechanically sweeping the direction of the antenna in space. There have been various attempts to realise phase modulation in the microwave regime, either by using functional materials (e.g. magnetically or electronically tunable materials), or by switching the antenna elements/transmission lines of different lengths.

1.3.1 Ferrites

Conventional delay lines feeding phased-array antenna systems were implemented with ferrite materials by altering the magnetic bias field. These phase shifters have advantages in terms of high power-handling capacity, decent reliability, radiation tolerance, and thus suitability for high-power applications. However, the tuning is based on the generation of strong magnetic fields, requiring coils biased with hundreds or even thousands of volts. For these reasons, they are bulky, less integratable, slow in response (requiring long tuning times), expensive (not amenable to mass production methods), and have significant power consumptions [38]. Ferrite-based phased array is by no means cost-effective for modern terrestrial applications.

1.3.2 p-i-n diodes, Varactors

Current phased array antennas are mostly based on phase shifters implemented in multiple switches, routing the microwave signal through various physical delay lengths to achieve different phase delay for different radiating elements as presented in Fig.6 below.

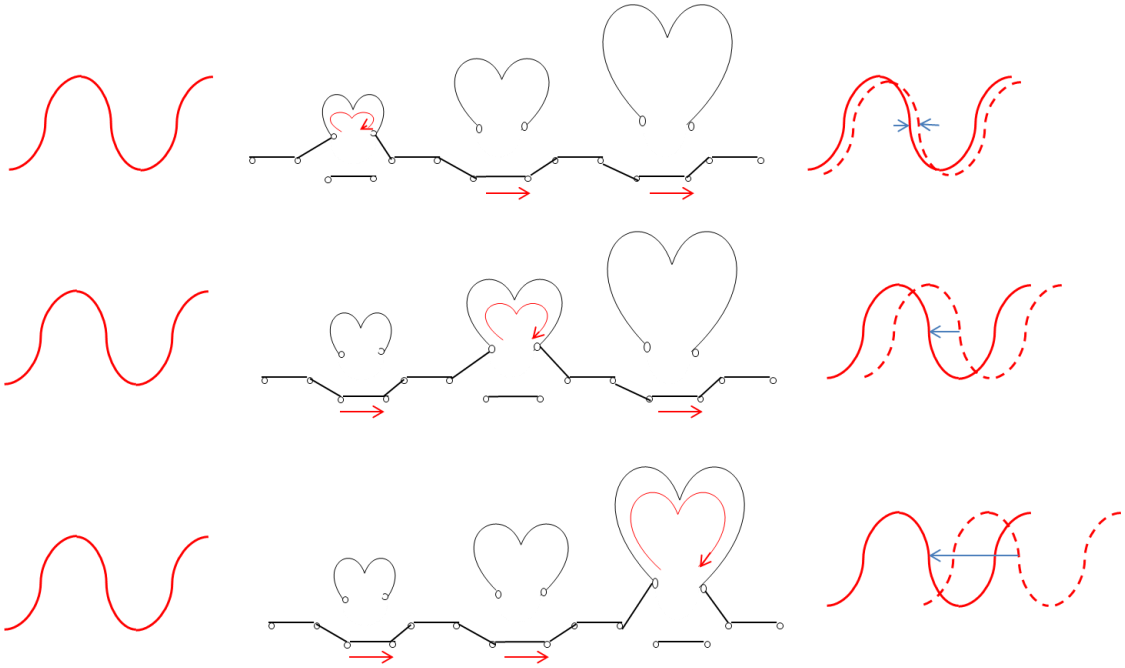


Fig.6 Principle of Multiple Switchable Delay Lines with Phase Shifts of 45°, 90°, 180°

Such switch-based philosophy has been implemented in different ways, such as GaAs or GaN based p-i-n diodes/Schottky diodes/FETs. The major drawback of these methods is the severely limited phase-shift resolution, predominately limited by control bits, i.e. the number of transmission lines to be switched. According to the nature of discrete tuning in n-bit operation, the phase shift resolution of a 4-bit digital delay line is limited to only $\frac{360^\circ}{2^4}$ =22.5°. Furthermore, solid-state phased arrays based on GaAs monolithic microwave integrated circuit (MMIC) exhibit unacceptably high losses in the millimetre-wave band due to high dissipation factors of the materials.

1.3.3 MEMS

State-of-the-art MEMS technology with microsecond switching speeds seems best suited to a switching function, as it offers a much lower insertion loss, higher linearity over a large bandwidth, and lower power consumptions than the solid-state technology.

However, commercially available MEMS switches are still limited by the maximum operational frequency of up to 40GHz. They are challenged by reliability issues and the drastically rising insertion loss in the millimetre-wave bands when integrating MEMS switches and transmission lines on a substrate. A MEMS-based digital phase shifter (3 bit, 15μs

switching time) was reported to exhibit an insertion loss of -5.7 dB for achieving a 180˚ phase shift at 76.5GHz [9]. The inherent digital resolution problem as mentioned above finally limits their applicability for the future high-performance phased antenna array beam steering applications.

1.3.4 Tunable Dielectrics Methods

Passively controllable microwave components based on continuously tunable dielectrics offer promising alternatives to switch-based topologies (i.e. active semiconductor devices and MEMS as mentioned above).

The permittivity of microwave dielectric materials is a complex value, i.e.

$$\varepsilon = \varepsilon' - j\varepsilon'' = \varepsilon'(1 - j\frac{\varepsilon''}{\varepsilon'}) \quad \ldots\ldots\ldots\ldots\ldots\ldots(1)$$

where $\varepsilon' = \varepsilon_r\varepsilon_0$ is the real relative permittivity (dielectric constant), and $\frac{\varepsilon''}{\varepsilon'}$ is the loss tangent. The imaginary part ε'' accounts for power dissipation in the medium (heat) due to damping of the vibrating dipole moments (polarisation induced by an external AC field cannot follow the field anymore). Electrical tunability implies that the permittivity of the interlayer substrate of a device can be modified by an external applied voltage, i.e.

$$\textit{Tunability (E)} = \frac{\varepsilon_r(E) - \varepsilon_r(0)}{\varepsilon_r(0)} \times 100\% \quad \ldots\ldots\ldots\ldots\ldots\ldots..(2)$$

where $\varepsilon_r(0)$ and $\varepsilon_r(E)$ denote the un-tuned and tuned dielectric constants, respectively. Modulation of the real/imaginary part of the relative permittivity of tunable materials could achieve phase modulation of an input signal and hence the control of millimetre-wave transmission properties.

Note that for anisotropic materials, their characteristics variance with directions can be described by anisotropy tensors, i.e. 3 diagonals each for anisotropic permittivity, electric loss tangent, conductivity, permeability, and magnetic loss tangent. Each diagonal represents a tensor of the model along an axis. The permittivity tensor for an anisotropic material is described by

$$\varepsilon = \begin{pmatrix} \varepsilon_1\varepsilon_0 & 0 & 0 \\ 0 & \varepsilon_2\varepsilon_0 & 0 \\ 0 & 0 & \varepsilon_3\varepsilon_0 \end{pmatrix} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

where ε_1 is the relative permittivity of the material along one tensor axis, ε_2 is the relative permittivity along the second axis, and ε_3 is the relative permittivity along the third axis, ε_0 is the permittivity of the free space.

Fig.7 below shows the different polarisation mechanisms occurring in the frequency domain. Up to the microwave region, ion and dipole polarisations dominate. These polarisation types can be described by the Debye's relaxation polarisation model:

$$\varepsilon_{r,\ complex} = \varepsilon_{r,\ optical} + \frac{\varepsilon_{r,\ static} - \varepsilon_{r,\ optical}}{1 + j\omega\tau} \quad \text{..... (4)}$$

where ω is the angular frequency, τ is the relaxation time (i.e. the characteristic time that the orientational polarisation or average dipole orientation takes to adjust in a switching field), $\varepsilon_{r,\ static}$ and $\varepsilon_{r,\ optical}$ are the static and high frequency permittivity, respectively.

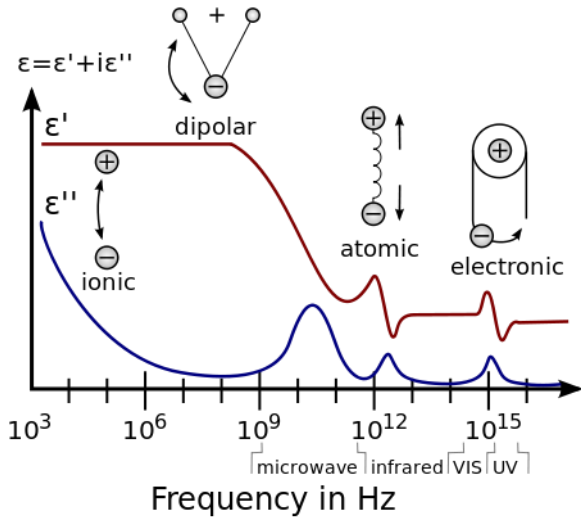


Fig.7 Dielectric Responses in the Electromagnetic Spectrum [50]

As frequency increases, the material's net polarisation drops as each polarisation mechanism ceases to contribute, and hence its dielectric constant. From a certain frequency onwards (>10^{15}Hz), the movement of charge cannot remain in step with the alternating field, and all the polarisation mechanisms cease to contribute to the polarisation of the dielectric. The dielectric constant drops to 1, the same as that of a vacuum. Relaxations and resonance processes determine the characteristic of the dielectric constant. Governed by a linear second order ordinary differential equation, the resonance processes are atomic in nature, but out of the scope of this research because they only occur at 10THz onwards. Described by a linear first-order ordinary differential equation, the relaxation processes indicate that the polarisation follows the electric field but is hindered by dissipations [22]. Dielectric loss is especially high around the

relaxation or resonance frequencies of the polarisation mechanisms as the polarisation lags the applied field, causing an interaction between the field and the dielectric's polarisation that results in heating.

However, only a handful of tunable microwave dielectrics have thus far been identified with high tunability and low loss, among them, ferroelectric material barium strontium titanate (BST) and liquid crystal (LC) in nematic phase which are of research and development interests.

1.4 Exploring Liquid Crystal based Phase Shifters for 60GHz-90GHz Applications

1.4.1 Ferroelectric Barium Strontium Titanate (BST)

As promising candidates for microwave tunable delay lines, BST and LC both exhibit tuning-voltage dependent and temperature dependent electromagnetic properties with different degrees of field-dependent nonlinearity and frequency-dependent dielectric loss. Since tunability and losses of different dielectrics might differ appreciably depending considerably upon the operating frequency, BST and LC operating in different frequency ranges are identified below.

Ferroelectric BST thin films do exhibit decent performance below 10GHz-15GHz (depending on applications), with figure-of-merit in terms of phase shift per loss reaching 50-100º/dB at 1GHz. However, the tunability is counterbalanced by considerably increasing dielectric loss beyond 10GHz. For this reason, there is a slump in the figure-of-merit, dropping down towards only 25º/dB at 10GHz. The high dielectric loss at millimetre-wave bands severely restricts their application potential. The intrinsic loss originates from collisions with thermal phonons, while charged defects, the universal relaxation law, and quasi-Debye contribution account for the extrinsic loss.

Recent efforts in loss reduction rely on doping ferroelectric materials with oxides, e.g. MgO, Al_2O_3, and ZrO_2. However, the reduction in loss tangent (as low as 0.004 reported at 10 GHz by adding MgO and Mg_2TiO_4 to a 50/50 BST) is at the cost of reduced tunability [1], and hence only a minor improvement in figure-of-merit.

1.4.2 LC's Advantages over BST for Millimetre-wave Applications

More recently, liquid crystal (LC) in nematic phase has been reported in electrically tuned microwave devices (e.g. resonators, filters, phase shifters, antennas, frequency-selective surfaces) that are essential components of a phased antenna array system. Working as tuning dielectric materials based on molecular shape anisotropy (explained in Chapter 2.1), liquid crystals offer highly attractive properties over competing technologies.

(1) First and foremost, continuous tunability (0-2π analogue phase shifting capability). With LC-based phase shifters, appreciable resolution of beam scanning is achievable to outperform digital resolutions.

(2) Very low-loss dielectric properties (almost transparent) above 10GHz up to 1THz, as evidenced by the dielectric spectroscopy as shown in Fig.8 below. The dispersion of the permittivity is associated with the dipolar relaxation behavior due to molecular dynamics. For this work, the targeted frequency band is sufficiently higher than the dielectric relaxation absorption bands of liquid crystals, and hence enables low-loss performance. Using a V-band (50GHz - 75GHz) rectangular waveguide test cell, it was reported that nematic LC is transparent in the millimetre-wavelength range [76].

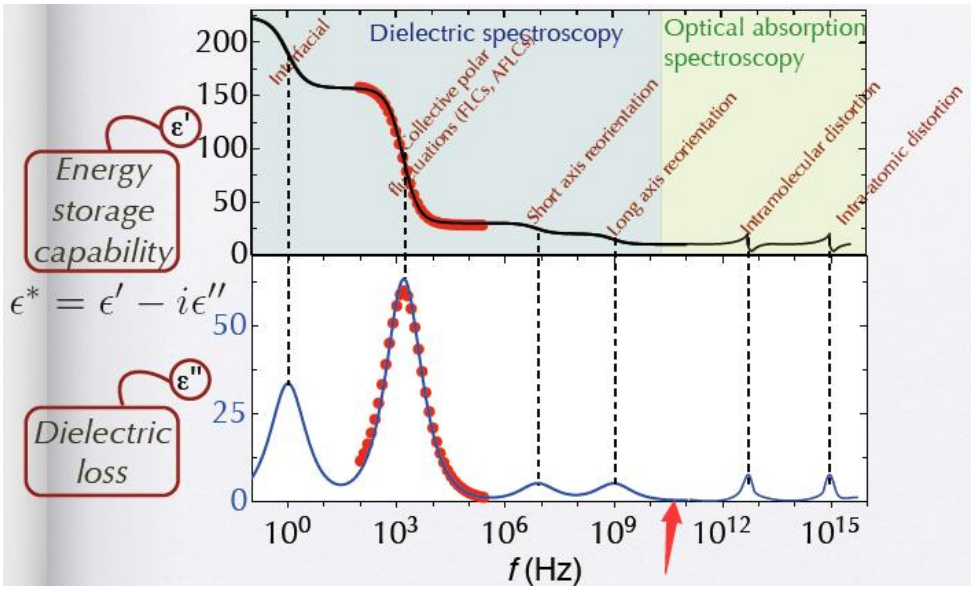


Fig.8 Broadband Characterisation of Liquid Crystals [37]

As observed from Fig.8 above, although the tunability of nematic LC between 10GHz and 100GHz is not exceptionally large (almost a constant permittivity as there is no dielectric relaxation in this interval), the low loss tangent (no strong absorption band around this region) tips the balance. The dielectric properties (particularly the low loss tangent) of LC are most favourable at millimetre-wave bands (>30GHz). By contrast with BST thin films, the dielectric loss of LC above 10GHz decreases with frequency. Figure-of-merit (defined as the ratio of phase tunability to insertion loss) of LC rises with millimetre-wave frequency and thus, making it the most competitive low-loss tuning material in the millimetre-wave bands.

(3) Ease of control. Very low control voltage (~10V), low power consumptions (E < 0.2V/μm to drive the LC in comparison with BST (30V/μm to obtain a reasonable tunability, depending on the structure). Under a higher biasing field, ferroelectric devices are more prone to sample aging, polarisation fatigue and hence a degradation of the tunability.

(4) Good temperature stability. LC-produced phase delay is less sensitive to temperature variation (within ±20˚C). Measurement conducted by [70] shows a minor temperature dependence of LC in tunability at –10˚C, 24˚C, and 50˚C.

To recapitulate, the potential of liquid crystals as reconfigurable materials arises from their appreciable tunability, low polarisation loss (especially above 10GHz), ease of control (continuous tuning with low power consumptions), transparency, and possible integration with printed and flexible circuit technologies. The continuous tunability (i.e. analog functionality) is especially useful in beam-scanning applications for improving the beam-pointing accuracy and compensating for temperature or aging drift. In this context, there is a momentum towards the combination of LCs and the phased array antenna technology in preparation for futuristic millimetre-wave applications.

1.4.3 Limitations of Nematic Liquid Crystal

However, nematic liquid crystals (NLC) do exhibit three main limitations.

First, the switching speed ranges from ~ms to ~s (depending on operating wavelength, type of LCs and the layer thickness), which is far slower than that of BST thin films (~μs). Although the increase of applied driving voltage or a decrease of the threshold voltage could effectively reduce the rise time, the tuning speed of a microstrip type NLC cell is predominately limited by the undesirably large decay time (slow reorientations). A diversity of methods has been suggested to alleviate this problem, including a π-cell configuration, membrane impregnated with NLC, dual-frequency switching-mode NLC [6], etc. However, they exhibit different degrees of problems, such as a rise in insertion losses, a decrease in tunability and hence a degradation of the achievable phase shifts.

Second, field-dependent nonlinearity. The effective working range is limited by two threshold voltages, i.e. the Fredericks transition voltage and a saturated voltage. The initial threshold voltage can be lowered by increasing the dielectric anisotropy, reducing the elastic constant, as well as reducing the flow viscosity. However, reducing the elastic constant may weaken the restoring torque, and hence slowing down the response time to post-removal of the bias field.

Third, the fluidic nature limits the device topology. LCs must be enclosed and sealed inside a sandwich structure. Making LCs surrounding a core line in a cylindrical way (coaxial) or strip line presumably achieves a higher tuning range than IMSL and CPW but remains challenging to organise the structural integrity problem. The packaging requirement also increases the device footprint, which limits its integration into chips with close feature registration.

An even bigger challenge is how to best design and fabricate low-loss tunable devices in the millimetre-wave regime to enable innovative phased-array applications and open the door of low-cost manufacturing for commercialisation. While electromagnetic fields interactions with LCs have been well researched for optical and comparatively low-frequency bands, there have been few studies reporting measurements and development for the millimetre-wavelength range. Developing LC-based GHz/THz phased-array antennas remains in an embryonic proof-of-concept stage. Design and optimisation space remain largely unexplored. Challenges in LC at millimetre-wave are studied in Chapter 2.2.

The choice of the LC material type and the structure design of a variable delay line depend on different beam steering applications. For missile-tracking radars, where fast response time is an important consideration, the LC layer must be thinner to enhance the switching speed. Instead, for weather radars, airport surveillance or microwave relay satellite, there is little need for ultra-fast response (e.g. for relay links between a faster moving low-earth-orbiting satellite and a geostationary relay satellite, the requirement for angular tracking velocities of low earth orbiting satellites is typically 180˚ in 45 minutes, i.e. 4˚/min), so the LC layer could be made thicker to reduce the insertion loss. To improve phase shift performance without degrading the switching speed significantly, we could replace the current LC materials with higher birefringent ones to reduce the thickness of the LC layer (but insertion loss will be increased), or optimise the device structure as discussed next.

Chapter 2. Different Approaches of Phase Shifter Configurations with LC above 60GHz

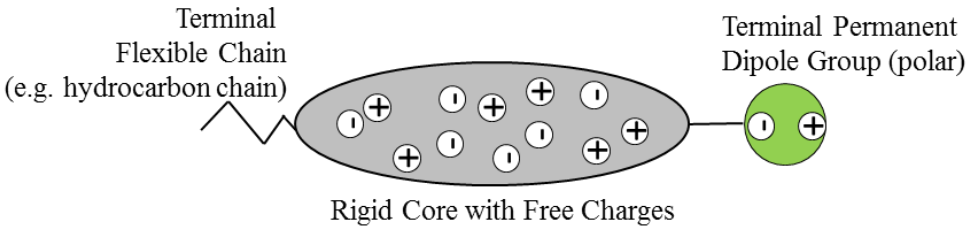
This chapter conducts a critical review of the situation in existing knowledge about LC-based phase-shifting device configurations, which provides motivation and justification for the research question. Based on the working principles and unique structural requirements of LC-based phase components (Chapter 2.1), a variety of challenges are envisioned for the 60GHz phase shifters combining with LC (Chapter 2.2).

2.1 Principle of Liquid Crystal based Phase Tuning Components

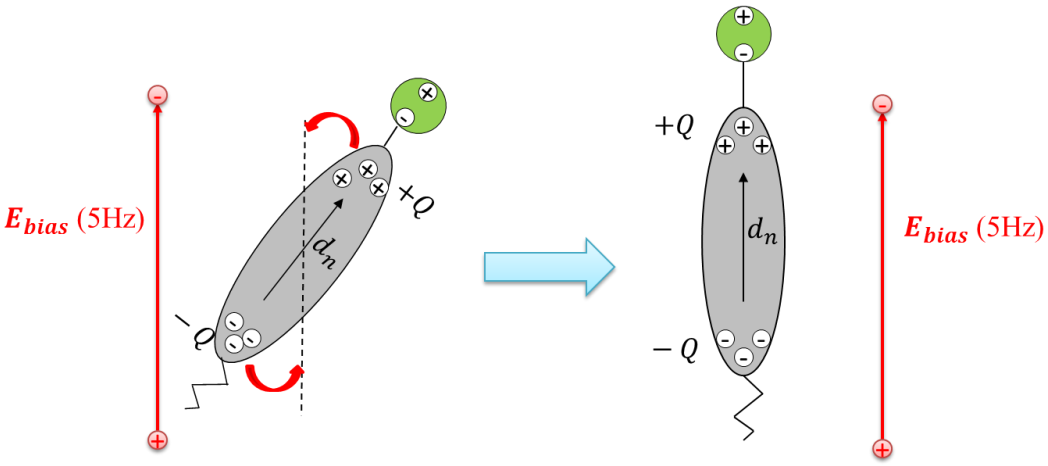
The potential of liquid crystals (LCs) as reconfigurable materials arises from their appreciable tunability, low polarisation loss (especially above 30GHz), ease of control (continuous tuning with low power consumptions), transparency, and possible integration with printed and flexible circuit technologies. Working as electrically tunable dielectrics based on molecular shape anisotropy (section 2.1.1), nematic LCs have relatively high tunability and low loss to outperform ferroelectric materials (e.g. barium strontium titanate BST thin films) in the millimetre-wavelength range (>30GHz). The underlying physics and chemistry of nematic liquid crystals reviewed in literature [64] and [30] are applied to our research into the LC-based millimetre-wave phase shifter device.

2.1.1 LC Dielectric Anisotropy due to Molecular Shape Anisotropy

First, we depict a rod-shaped model of the liquid crystal (LC) in nematic phase in Fig.9 (a) below, with mobile charges inside a rigid core polarised by an external low-frequency bias field (5Hz for example) as shown in Fig.9 (b), resulting in reoriented dipole moments.



(a) An Exemplary Molecule Representation of the Nematic Liquid Crystal



Reorientation of LC's dipole moment ($Q\overrightarrow{d_n}$) by electrostatic field

(b) Bias Field-Induced Reorientation of the Liquid Crystal in Nematic Phase

Fig.9 An Exemplary Nematic LC Molecule Model and the Reorientation Mechanism

The chief effect of a low-frequency field $\vec{E}_{bias}$ applied to the molecule is producing dipole moments that align themselves in the direction of $\vec{E}_{bias}$ (a phenomenon called polarised). From the free-energy minimisation point of view, lowest energy of the anisotropic LC occurs when the largest component of the dielectric constant tensor is in line with the applied bias field, hence the induced reorientation as shown above.

The fundamental of LC's tunability in the dielectric constant is attributed to its molecular shape anisotropy, where the size across two orthogonal molecule axes differs (i.e. $d_\perp \neq d_\parallel$), resulting in dipole moment difference and hence the difference in polarisation $\vec{P}$=$NQ\vec{d}$ (C/m^2). We depict this in Fig. 10 below, with a positive dielectric anisotropy assumed (i.e. $d_\parallel > d_\perp$ and hence $\overrightarrow{P_\parallel} > \overrightarrow{P_\perp}$). The polarisation $\vec{P}$ characterises the polarisation density (induced dipole moment per unit volume) of the LC dielectric medium under the 60GHz field $\vec{E}_{60GHz}$ to be transmitted. Here N denotes the number of dipoles per unit volume, and $Q\vec{d}$ is the dipole moment. Note that the LC reorientation effect is not induced by the 60GHz electric field (as it is oscillating too fast for molecules to follow, and also the field is too weak far below the

transition voltage), but attributed to the low-frequency AC biasing, or mechanical anchoring using a surface alignment layer (section 2.1.3).

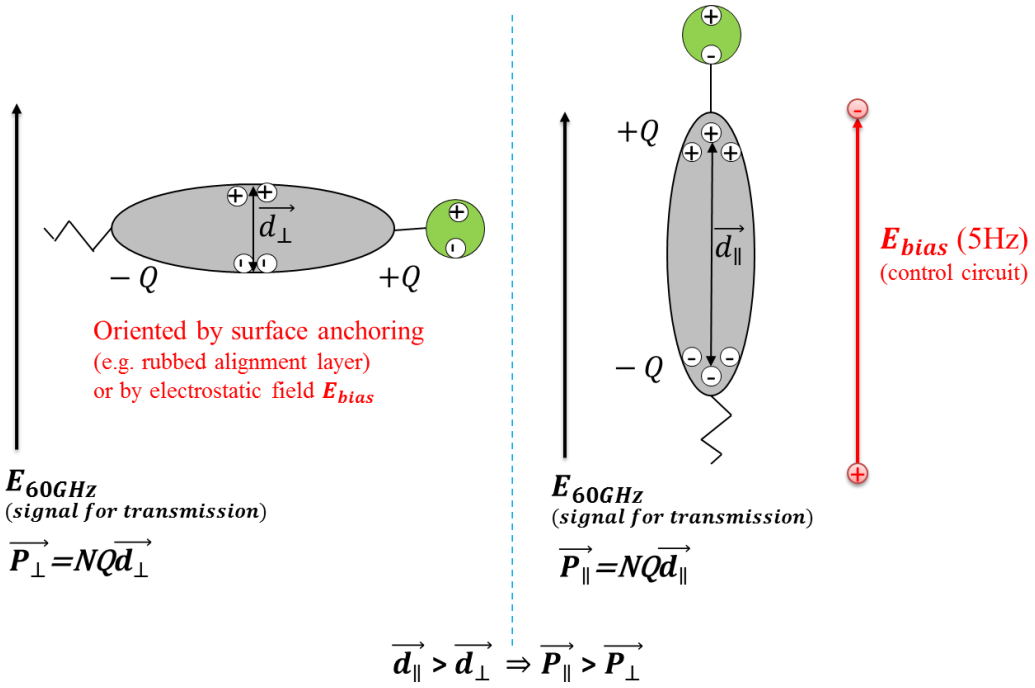


Fig.10 LC Molecule Interacting with 60GHz Signal:

Molecular Shape Anisotropy and the Resulted Polarisation Difference

From $\vec{P}=NQ\vec{d} = (\varepsilon_r - 1)\varepsilon_0\vec{E}$, and the $\vec{P_\parallel} > \vec{P_\perp}$ as explained above, we can derive that $\varepsilon_{r,||} > \varepsilon_{r,\perp}$. With this dielectric anisotropy ($\varepsilon_{r,||} > \varepsilon_{r,\perp}$), the low-frequency bias voltage - dependent molecular director transition from the perpendicular to the parallel state allows a continuous tuning of the dielectric constant and hence a differential phase shift for a phase shifter device, as interpreted in the following section 2.1.2.

2.1.2 Elements of Electrically-Tuned LC Phase-Shifting Architecture

In Fig.11 below, we sketch a classical structure of two-planar-electrodes separated by a distance (cell gap) where LCs and alignment layers are placed. The cell gap is within the range of the anchoring effect enforced by surface treatment (alignment layer). The low-frequency voltage bias (V_{bias}) here is a low-frequency AC (e.g. 5Hz sinusoidal or rectangular) instead of a DC for avoiding ions localisation in the LC.

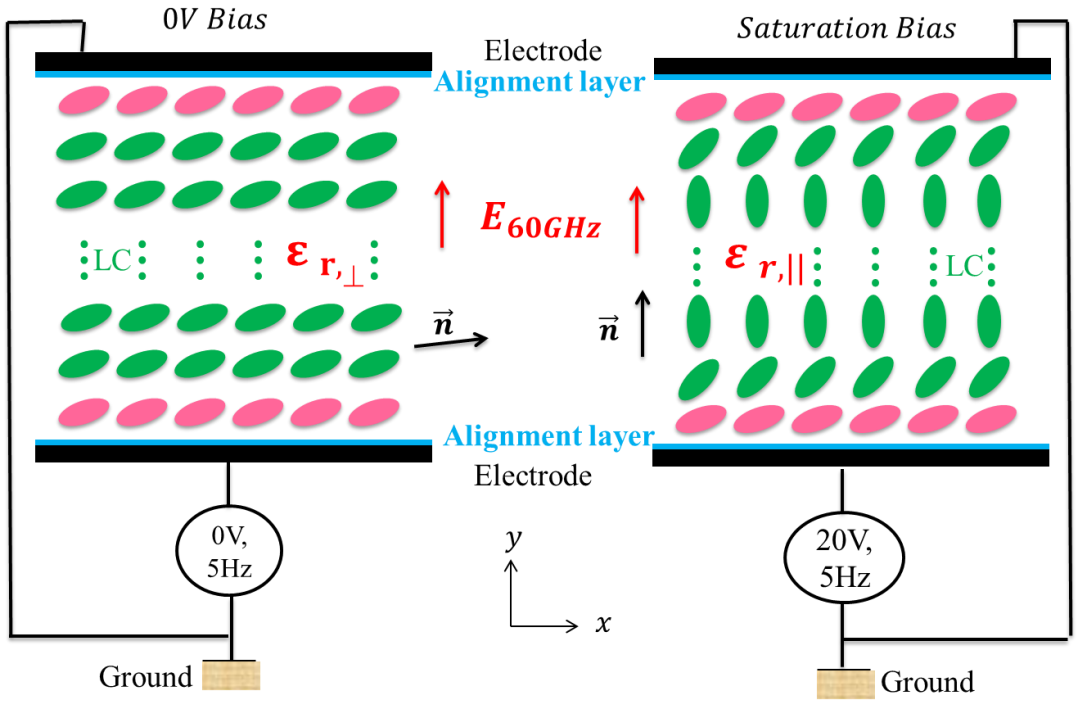


Fig.11 Exemplary Architecture of the LC-based Phase Shifter and the Tuning Mechanism

When the bias voltage is lower than a threshold, i.e. the Fredericks transition voltage [64], molecular switching is not induced, but anchored by the pre-treated surface with a mechanically rubbed polyimide film (called alignment layer). A nearly homogeneous LC dielectric layer with molecular directors orthogonal to the 60GHz electric field can be assumed ($\varepsilon_{r,LC} = \varepsilon_{r,\perp}$). With the applied voltage increasing to the saturation bias, the mechanical anchoring effect by the treated surface is eclipsed by the low-frequency biasing field, resulting in the directors being in parallel with the biasing field. Note that for a standard transmission line structure that supports transverse-electromagnetic (TEM) mode (cutoff frequency is 0Hz, i.e. DC), the 60GHz electric field vectors follow an identical direction of the biasing field at the low frequency. Therefore, the director of the LC layer under the saturation bias is also parallel with the 60GHz signal's polarisation, i.e. $\varepsilon_{r,LC} = \varepsilon_{r,||}$. The dielectric anisotropy and hence the dielectric tunability of the material is defined as:

$$Tunability = \frac{\varepsilon_{r,||} - \varepsilon_{r,\perp}}{\varepsilon_{r,\perp}} \times 100\% \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (5)$$

The dielectric constants ($\varepsilon_{r,\perp}$ and $\varepsilon_{r,||}$) here are bulk (macroscopic) properties. The macroscopic dielectric anisotropy and hence the material tunability depends on the ordering of the molecules and polarisabilities of the molecules. For an incident millimetre-wave signal, the bias voltage-controlled analogue tuning of the LC's dielectric constant can produce a

continuous differential time delay Δt and hence the differential phase shift $\Delta\Phi_{21}$ as derived below.

$$\text{Differential time delay } \Delta t = \frac{L}{c_0}\Delta n_{eff}\,(V_{bias}) \quad \ldots\ldots\ldots\ldots\ldots (6)$$

$$\text{Differential phase shift } \Delta\Phi_{21} = 2\pi f\Delta t = \frac{2\pi fL}{c_0}\Delta n_{eff}\,(V_{bias}) \quad \ldots\ldots\ldots\ldots\ldots...(7)$$

where:

f is the frequency of the millimetre-wave signal.

L is the is the physical length of the phase shifter.

c_0 is the light velocity in vacuum.

The effective birefringence $\Delta n_{eff} = \sqrt{\varepsilon_{r,eff,||}} - \sqrt{\varepsilon_{r,eff,\perp}}$ here is the maximum effective dielectric anisotropy in the wave-occupied volume (*WoV*, a concept we propose and is detailed in Chapters 2.6 and 4.2).

Note that both $\varepsilon_{r,eff,||}$ and $\varepsilon_{r,eff,\perp}$ are effective dielectric constants based on the wave-occupied volume *(WoV)* of a specific device structure, instead of purely the permittivity of LC in two extreme states. In this regard, the device tuning range *(TR)* of a LC-based tunable phase shifter structure is defined as eq.8 below (not to confuse device's tuning range with material's tunability).

$$TR = \frac{\varepsilon_{r,eff,||} - \varepsilon_{r,eff,\perp}}{\varepsilon_{r,eff,\perp}} \times 100\% \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots..(8)$$

With a fixed type of LC material (i.e. tunability is known and fixed), the device's tuning range (*TR*) is not only a function of the LC material's tunability, but also is affected by the guiding structure's geometry as well as the dielectric properties of other substrates interacting with the millimetre-wave fields. We will cover the investigation into the device's tuning range maximisation and optimisation in Chapters 2.6 and 4.2.

2.1.3 Planar Alignment by Surface Anchoring

Planar alignment of LC molecules can be achieved by mechanically rubbing micro-grooves on a polyimide film, which helps anchoring the molecules in a desired reference direction ($\varepsilon_{r,\perp}$), for which the maximum tunability can be realised when a saturation bias voltage is applied ($\varepsilon_{r,||}$). Meanwhile, it helps restoring the original planar structure when the bias is removed.

In addition, LC-filling is arguably also an alignment process. As illustrated in Fig.12 below, it is energetically favourable to make the LC filling direction in line with the pre-alignment (rubbing) direction to minimise distortions in the director field.

(a) Not Desirable (b) Desirable

Fig.12 Implications of the LC-Filling Direction and the Rubbing Direction

2.2 Challenges in LC-based Phase Shifters at Millimtre-wave

2.2.1 Transmission Line Effects and Characteristics of Various Line Structures

At extremely high frequency (microwave and millimetre-wave) as the circuit length is comparable to the guided wavelength ($>\lambda/8$), transmission line effects become prevalent. The behavior of a transmission line in the millimetre-wavelength range is predominately wave-like, exhibiting a distributed parameter network, where voltages and currents vary appreciably in magnitude and phase over its length, making it insufficient to define voltage, current and impedance by the classical circuit theory (e.g. lumped element model). The propagation effects produce substantial time delays in time domain, or phase shifts in harmonic (phasor) amplitudes. The dynamic behavior is governed by the full set of Maxwell's equations. Electric and magnetic field vectors governed by Maxwell's equations are the primary unknown quantities, whereas voltages and currents (as secondary quantities) are derived by integrations along specific paths upon which they depend [19].

A transmission-type phase shifter (i.e. phase delay produced by transmission of a signal through a device) can be implemented in different transmission-line or waveguide topologies (Table.1), depending critically on the targeted wavelength range.

Table 1. Comparison of Various Types of Transmission Lines [45]

(★★★★★ is very good, ★★★★☆ is good, ★★★☆☆ is neutral, ★★☆☆☆ is poor)

Topology	Frequency (GHz)	Characteristic Impedance (Ω)	Q-factor	Power Handling	Physical Size	Ease of Fabrication
Strip Line	<20	10-120	★★☆☆☆	★★★☆☆	Medium	★★★☆☆
Slot Line	<40	20-150	★★★☆☆	★★☆☆☆	Medium	★★★☆☆
Coaxial	<50	10-600	★★★★☆	★★★★☆	Large	★★☆☆☆
Suspended Strip	<50	30-200	★★★★☆	★★★☆☆	Large	★★★★☆
Microstrip	<50	10-120	★★☆☆☆	★★☆☆☆	Small	★★★★☆
Coplanar Line	<100	40-150	★★☆☆☆	★★☆☆☆	Medium	★★★★☆
Waveguide	1-300	100-500	★★★★★	★★★★★	Large	★★☆☆☆

Conductor loss and dielectric loss are of paramount research importance, with the theoretical calculating mechanism of which detailed later in Chapter 3.4, as it is challenging to decompose different losses by experiment. Beyond that, there are a few loss mechanisms that are particularly of research interest for 60GHz-90GHz. With the decrease of wavelength from microwave to millimetre-wave, circuit performance degradation not observable at the microwave bands can, however, be noticeable in the millimetre-wave frequencies. A few millimetre-wave effects that make a difference to the device performance are studied and reported in the following sections.

2.2.2 Line Loss due to Standing-wave Resonance and Parasitic Mode Radiation

A standing-wave resonates when nodes and antinodes correlate with the ends of a transmission line with a quarter-wavelength and harmonic frequency of the quarter wavelength. To complicate the picture, the variation of characteristic impedance with diverse phase shifting states (under diverse bias voltages) can cause different levels of reflection loss and hence insertion loss variations at the same frequency.

Theoretically, the length of a ground return path should be minimised and with no impedance anomalies. As will be covered in section 2.6.2, the physical gap and contact resistance between two ground planes (intended to connect with each other) can result in unequal potentials and hence parasitic modes radiation at the discontinuity. Given the gap dimension comparable to a quarter guided wavelength, the aforementioned standing-wave resonance can be induced, disrupting the signal integrity and even leading to malfunction of the phase shifter.

2.2.3 Line Loss due to Metal Surface Roughness and Skin Effect

Metal profile (surface texture) has a marked effect on the device's insertion loss at 60GHz, as the penetration depth (calculated in Fig.13 below) becomes comparable to the physical scale of the statistical metal surface roughness (root-mean-square value measured in section 4.3.3).

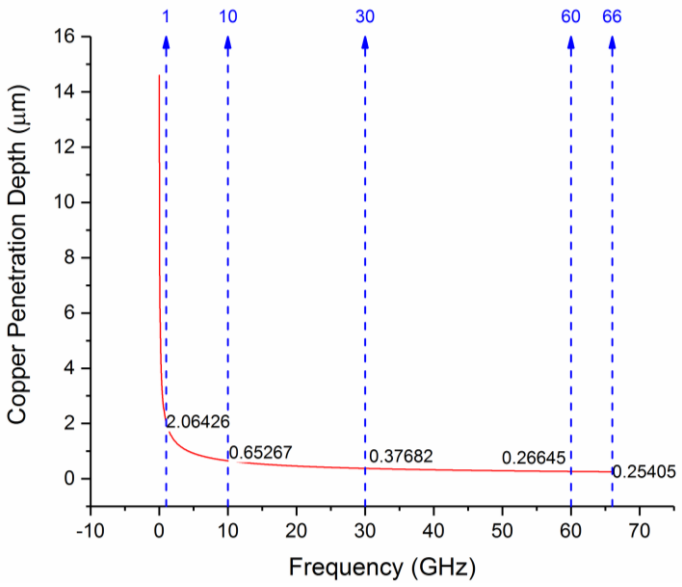
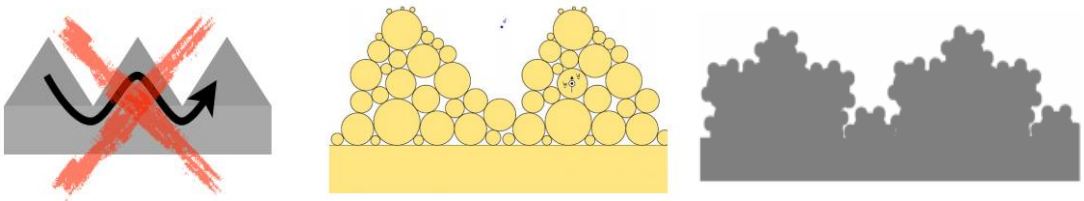


Fig.13 Frequency-Dependent Penetration Depth for Cu

In an actual performance-measurement of a fabricated LC-based device, higher-than-expected metal loss can occur because of metal surface roughness not considered at the design or simulation stage. Compared with an ideally smooth surface, a rough surface in real practice can alter the propagation constant (including phase constant which affects phase shifting accuracy, and attenuation constant which affects insertion loss), characteristic impedance, and effective dielectric constant.

However, the impact of surface roughness on insertion loss has long been a hugely contentious issue. As illustrated in Fig. 14 below, the existing surface roughness models developed by a variety of research groups are still highly debatable. Latest literature from [24] points out the deficiencies of the widely-accepted model by [20], which assumes that the microwave current path follows the rough surface contour, as shown in Fig.14 (a). The prediction power of a snowball model based on stacked spheres [57] and the follow-up multi-level hemispherical model [87] are also inherently limited.



(a) [20] (b) [57] (c) [87]

Fig.14 Evolution of Surface Roughness Models Proposed by Different Research Groups

2.2.4 Line Loss due to Substrate's Thermal Properties

Polytetrafluoroethylene (PTFE)-based materials are relatively soft. When the PCB substrate is manufactured, Cu foil is pressed into the PTFE surface under heat. When cooling the substrate down to the room temperature, internal stress has been developed in the PTFE and the higher modulus Cu foil due to differences in the coefficient of thermal expansion (CTE, as detailed in section 4.3.1).

When we partially remove Cu in our etching process, the remaining Cu is no longer able to fully stretch the PTFE. Unbalanced internal stresses distributed in the materials come out and often a bow can be seen (PTFE is shrinking, which is restrained by the bonded Cu). As covered in section 4.3.2, such dimensional instability can disrupt the 60GHz signal integrity and cause impedance mismatch, resulting in standing waves resonance and higher-order modes radiation, which elevates the insertion loss.

Low thermal coefficient of dielectric constant (measured in Appendix A) is also required for the PCB substrate, as it contributes to a stable electrical performance concerning phase and impedance stability.

2.2.5 Manufacturing Tolerance

Stringent dimensional tolerances account for another challenge in the 60GHz components fabrication. For 0.5oz Cu (17μm-thick) foil on printed circuit board (PCB), the achievable feature size by chemical etching is 100μm for traces and the gap between traces. Although a much finer feature is manufacturable, the conductor's vertical profile is susceptible to trapezoidal effect and undercut, with the adverse impact on the insertion loss simulated in section 7.5.3. The following Tables 2 and 3 summarise the size tolerances of the manufacturing methods we employ in this work.

Table.2 Feature Size and Manufacturing Tolerances in Low-cost Cu-based PCB Patterning

	Properties		Fabrication Method
Minimum Trace Width	100μm		Photolithography and Chemical Etching
Minimum Gap Spacing	100μm		
	Cu Weight		
	0.5oz (17μm-thick)	1oz (34μm-thick)	
Trace Width Tolerance (and Gap Spacing Tolerance)	±15 μm	±25 μm	

Table.3 Manufacturing Tolerances in Metal Processing

	Positional Error	Diameter Error	Minimum Hole Diameter
Tooling Holes Drilling	±100 μm	±50 μm	20 μm
	Positional Error	Cavity Depth Error	Fabricating Method
Cu Cavity Milling	±100 μm	±10 μm	Electrical Discharge Machining (EDM) and Milling

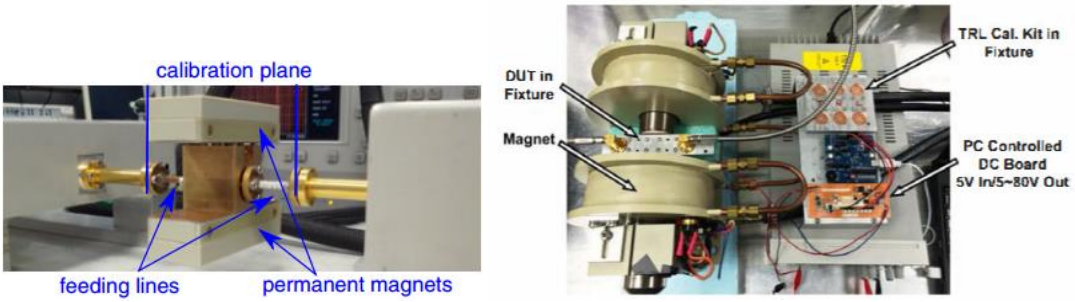
Variations of the phase shifter's electrical performance due to the manufacturing tolerances are simulated and reported in Chapter 5.6, while detailed fabricating procedures are explained in Chapter 6.

LC-based continuously tunable phase shifters could be realised in a few transmission line or waveguide topologies (e.g. coaxial, strip line, inverted microstrip lines, coplanar waveguide, waveguide etc.), depending on the operating wavelength range. The configuration is also limited by the liquid-like nature of the LC materials, e.g. the LC-filled device periphery should be sealed properly. To minimise insertion loss and maximise power transfer, guiding structures for the electromagnetic signal should be designed properly according to the operating frequency whilst satisfying the impedance matching. Chapters 2.3 and 2.4 review LC-based phase shifters based on waveguides and traditional transmission line technologies, respectively. Chapters 2.5 and 2.6 propose our solutions to address the challenges in 60GHz phase shifting components.

2.3 Waveguide and Substrate Integrated Waveguide Methods

For V band (40GHz-75GHz) and W band (75GHz-110GHz), a LC-based rectangular waveguide phase shifter has been demonstrated with low metal loss, low insertion loss, and high figure-of-merit (ratio of phase shift to insertion loss) for 65GHz-110GHz [68], 80GHz-110GHz [48] and even envisioned for 250GHz by design [15]. A detailed summary of their phase shift and insertion loss is presented in section 7.3.1. More recently, LC-based substrate integrated waveguide (SIW) has also attracted considerable research interest.

Compared with planar transmission line structures in a two-conductor system where electrical tuning is feasible, the chief drawback of the waveguide (single-conductor) approach is the bulky and power-consuming circuit required by magnetic control (> 1 Tesla). As shown in Fig.15 (a) (b), bulky permanent magnets are necessary for the LC pre-alignment and tuning.



(a) LC-based Waveguide [48] (b) LC-based SIW [39]

Fig.15 LC-based Magnetically Tuned Phase Shifter based on (a) Waveguide, and (b) Substrate Integrated Waveguide (SIW) Structures for 60GHz Proof of Concept

As limited by the non-planar structure, it is technically demanding to mechanically rub a polyimide film (as alignment agent) for the surface anchoring of LC. With the absence of alignment layer, the LC reorientation is extremely slow given post-removal of the bias field, as verified by [15], the switching time of their LC-based rectangular waveguide phase shifter is in the range between 45 seconds (switching-on) and 210 seconds (switching-off). Albeit it is claimed to meet the project specification of the Light-weight Inter-satellite Antenna Electronic Steering ($LISA_{ES}$), the low tuning speed struggles to meet agility requirement by most commercial applications.

2.4 Traditional Transmission Line Method

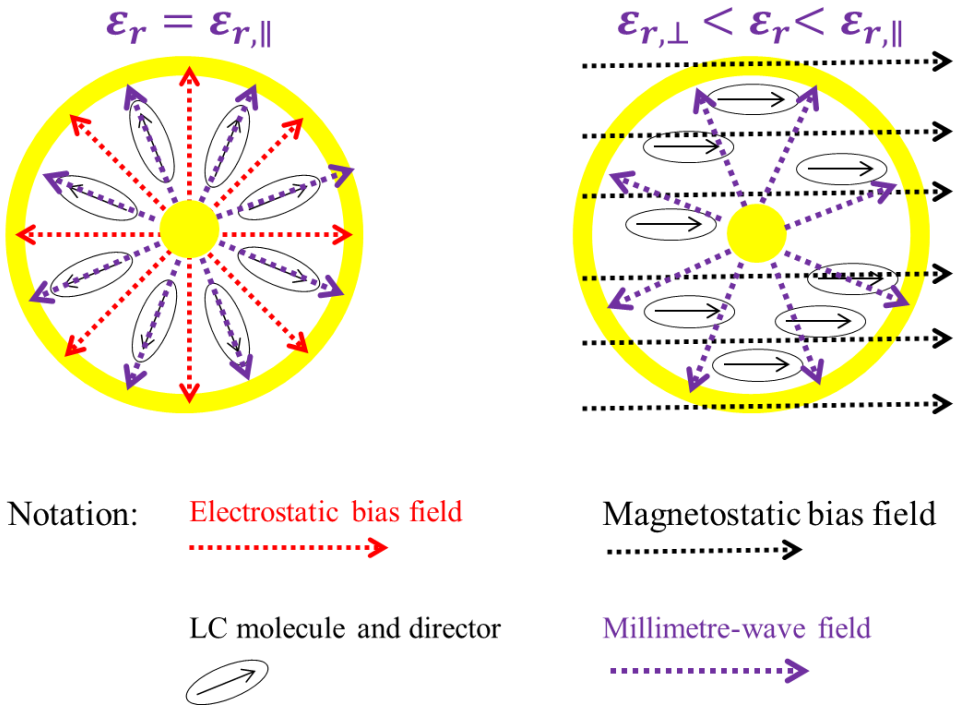
The earliest transmission method by twin lines no longer works for microwave frequencies because of the open-nature and high radiation losses. This accounts for the employment of classical coaxial cables designed in a closed structure, which has subsequently evolved into planar transmission-line structures such as a strip line (sandwiched between two conductor plates), and a microstrip line (printed on top of a dielectric substrate). To higher frequency ranges (>50GHz), however, they all exhibit severe lossy problems due to the skin and proximity effects, material dispersions and associated impedance mismatching, etc. They are therefore replaced by coplanar waveguide (CPW) and waveguides. This has been detailed before in Table 1 of section 2.2.1. In this chapter, we focus on assessing the compatibility of these structures with LC, particularly for phase shifting device considerations.

2.4.1 LC-filled Phase Shifters based on Coaxial and Stripline Structures

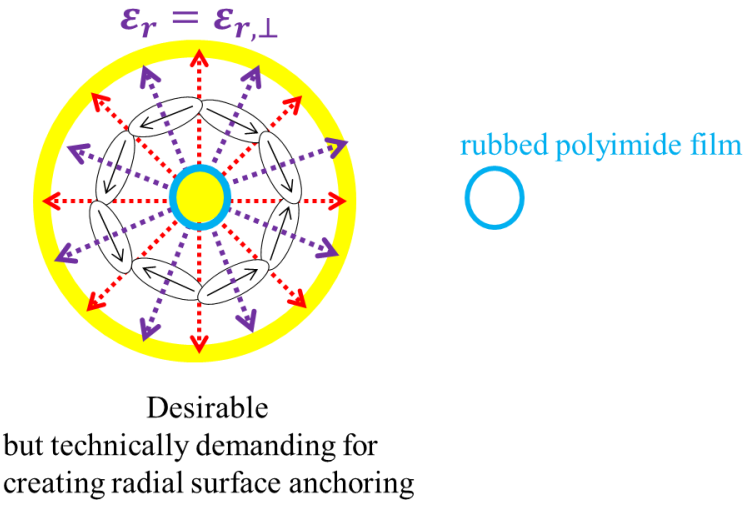
For a LC-filled coaxial transmission line, a core conductor is embedded in the lossy LC tunable dielectrics, exhibiting a non-planar TEM mode with radially polarised electric field. This structure features high isolation and radiation-free properties up to the cutoff frequency beyond which the higher-order TE_{11} mode comes into play. From the wave-occupied volume ratio (*WoVR*) point of view for the coaxial structure with LC surrounding a core line, 100% of the millimetre-wave signal is confined in the tunable dielectrics without leakages, thus the device tuning range (*TR*) can theoretically reach the LC's material tunability. In this regard, it seems that the theoretically highest tuning range can be realized in this structure.

However, it is not the case due to the impossibility of achieving the extreme value of $\varepsilon_{r,\perp}$ for the bulk dielectric volume. By ways of illustration in Fig.16 below, we depict the cross section of a LC-based coaxial phase shifter and the relevant biasing fields employed for LC reorientation. Due to its radial and non-planar nature, it is technically infeasible to create a radial surface-anchoring effect by mechanically rubbing an alignment film (Fig.16b) onto the tiny core (diameter in the order of 1 millimetre at 60GHz), because maintaining the core's structural integrity is challenged. Instead, a magnetic field (Fig.16a) can be used for LC

alignment, but this results in high power consumption and a large footprint due to the request for permanent magnets.



(a) LC-based Coaxial Phase Shifter biased by Electrical and Magnetic Fields



(b) Imaginary Depiction of LC Anchored by Radial Surface Alignment

Fig.16 Investigating LC-based Coaxial Phase Shifter and Biasing Schemes for LC Tuning

As analysed in Fig. 16 above, the impossibility of switching from $\varepsilon_{r,\perp}$ leads to a degradation of the tunability and hence the tuning range of the structure, which cancels out the advantage of the 100% wave-occupied-volume ratio (*WoVR*). Furthermore, from the insertion loss point of view, the metal ohmic loss is obtained by integrating the square of the millimetre-wave field intensity over the effective surface areas of the entire core and the entire metallic shield

(ground). The substantial effective surface areas of this structure to be integrated account for a large metal loss compared with that using planar transmission-line solutions.

Due to a combination of the lossy problems, no ease of alignment, lack of mechanical stability, and technically-demanding for integration, such a coaxial structure is currently only suitable for LC material characterisation purpose at the lower frequency range of millimetre-wave, e.g. a characterisation work up to 23GHz by [67] for a novel mixture of LC (MDA-03-2838).

Stripline, a semi-planar structure suffers from identical disadvantages as with coaxial when combining with LC for device considerations. In conclusion, a LC-based phase shifter realised in a coaxial or stripline structure struggles to fulfill the quest for low-loss, low-power consumptions and compactness required by the 60GHz wideband phased arrays.

2.4.2 LC-based Inverted Microstrip Line (IMSL) vs. Coplanar Waveguide

For the wavelength range below 30GHz, it is popular to implement LC phase shifters in an inverted microstrip (IMSL) topology with planar advantages (easy fabrication) and relatively mature technology. The inverted microstrip is a core line with a ground plane inverted on top, exhibiting a quasi-TEM fundamental mode with dispersive behavior.

2.4.2.1 Limitations of LC-based Inverted Microstrip Meander Line Phase Shifter

Past action by our group has been based on putting nematic LC next to the microstrip's core line. By modulating the LC's dielectric constant with electrical field and surface anchoring, the wave speed going through the LC section of the microstrip changes, leading to a variation of the output phase and thus a variable phase delay. In collaboration with the Cambridge Astrophysics Group, the author has been actively involved in the project entitled *Variable Dielectric Delay Lines in Liquid Crystals for Phased Array Feeds*, in which the author has assisted the development of compact microstrip phase shifters for 1GHz-10GHz, mainly working independently on device fabrication, characterisations and a large amount of optimisation. As shown in Fig.17 below, an optimised LC-based 9-folded microstrip phase shifter is developed and measured for up to 20GHz, realising a 0-360º continuous tuning by a 0-18V bias. The structure features with bias-T integrated on substrate.

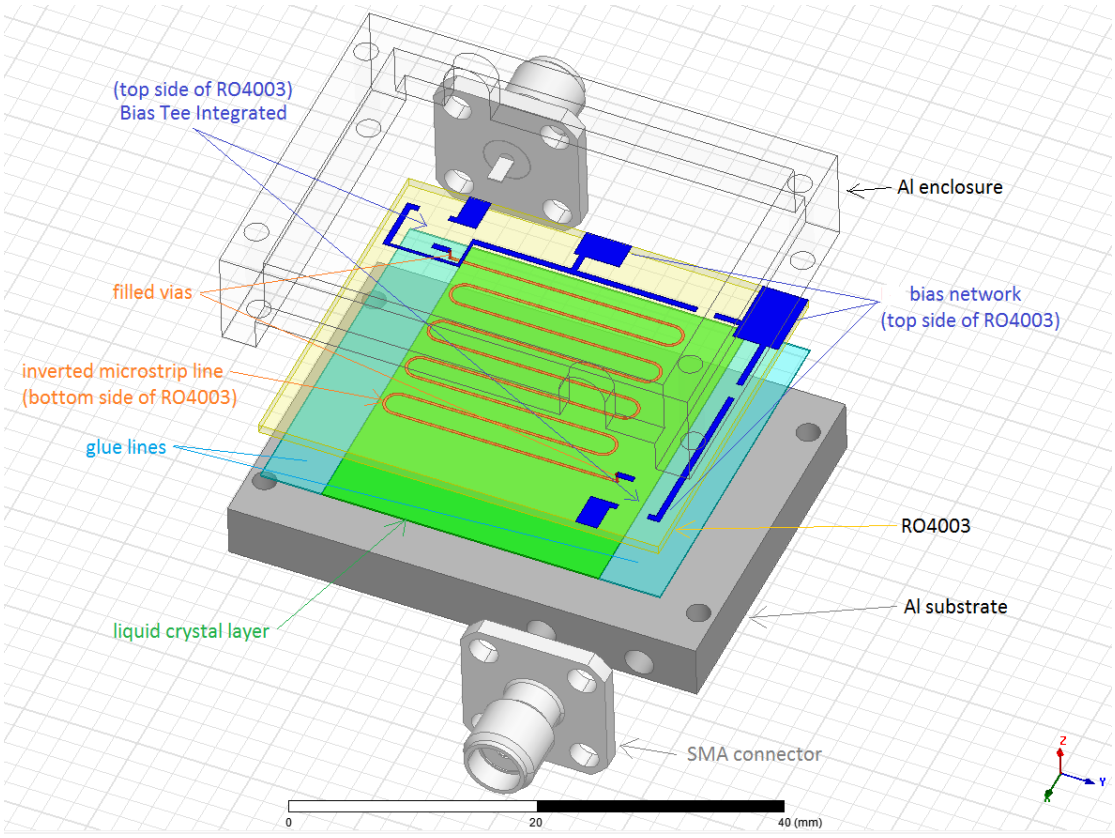


Fig.17 Exploded View of a Bias-T Integrated IMSL Phase Shifter Device based on LC

Flange-mounted SMA connectors and the electronic biasing network are top-launched (i.e. positioned on top of a RO4003 substrate) with easy access. With filled-vias, the microwave signal is routed from connectors to the meander microstrip line printed underneath the RO4003 substrate, and vice versa. The measured maximum insertion loss at 20GHz is -12dB at 0V bias, a figure-of-merit of 30º/dB which exhibits a 50% degradation as compared with a similar IMSL structure (60º/dB) we measured for a lower frequency range of 1GHz-10GHz and published at the Japanese Journal of Applied Physics [41].

The elevated insertion loss above 10GHz and limited bandwidth reported by most literature is owing to the inherently dispersive nature of the microstrip structure, as well as the inherent deficiency of the non-planar circuit access (as core and ground are not on the same plane) which increases radiation loss at a higher frequency. According to the state-of-the-art phase shifters reported above 60GHz and realised in LC-based inverted microstrip with gold-plated conductors [88], the minimum insertion loss at 66GHz is -10dB for 0-180º continuously shifting, a maximum figure-of-merit of 18˚/dB only.

From the materials' absorption loss point of view, to enable the microstrip structure working towards millimetre-wave with a decent figure-of-merit, the geometry design merits a trade-off between several factors that are in tension with each other. Increasing the thickness of the LC layer can reduce the conductor loss (according to the Ampere's law for the integration loop over a reduced microwave field intensity around the metal surface), but at the cost of reducing the surface anchoring efficiency of the alignment and hence slowing down the LC reorientation response.

In conclusion, the sharply elevated insertion loss above 30GHz due to the inherent structure inefficiency with LC and the limited room for optimisation impede the IMSL's deployment for millimetre-wave applications. This motivates our research to explore new planar device structures and contribute towards 60GHz-90GHz applications.

2.4.2.2 LC-based Coplanar Waveguide (CPW)

A promising solution is developing a LC-based coplanar waveguide (CPW), with a core line at the centre with two adjacent ground planes (and an enclosed ground on top). The same concept of putting LC next to the core line mentioned in IMSL can be applied. Now the structure to be investigated is not only confined to one LC layer above the core, but also the two slots between the core strip and the two coplanar grounds. The centre core builds up a coplanar-microstrip hybrid propagation mode that is modulated by the surrounding LC dielectrics and affected by the non-tunable PCB substrate. Based on this philosophy, we expect to employ it for a 0-π differential phase shifting, driven by a low-frequency (5Hz) and low-amplitude (<10V) electric field.

According to literature, implementing LC-based delay lines in CPW topology provides the following advantages over other planar transmission lines.

Firstly, the fundamental even mode of CPW is less dispersive than the fundamental mode of IMSL, as evidenced by Fig.18 the simulated characteristic impedance of our proposed LC-based floating-electrode-free CPW (FE-free CPW) phase shifters (detailed in Chapter 2.5). The minor dispersion and the resulted true-time-delay properties are favorable for a broadband phased array antenna system (Rotman, 2016) to eliminate the frequency-dependent beam shape (distortion) for an improved resolution in imaging and tracking applications.

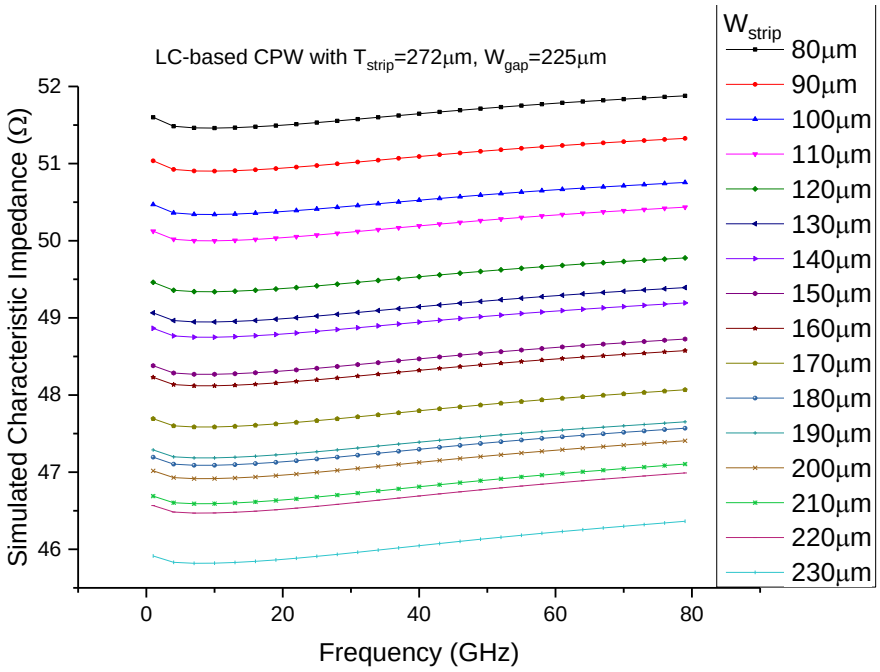


Fig.18 Simulated Dispersion in Characteristic Impedance of a LC-based FE-free CPW

Secondly, the modification of the phase-shifter accesses from IMSL to CPW structure as reported by (Martin, 2002), increases the figure-of-merit from 0.4°/GHz/cm to 0.87°/GHz/cm at 18GHz. Specifically, LC saturation is reached with a lower AC field intensity (from 20V to 10V), indicating an improved agility.

The third benefit attributes to the coplanar nature wherein the signal line and grounds are in the same plane. The crosstalk between adjacent lines is significantly reduced when multiple phase shifters realised in CPW (instead of IMSL) are integrated on a substrate for a phase-steered antenna array. This means that the spacing of the array feeding networks can be further reduced by comparison with IMSL.

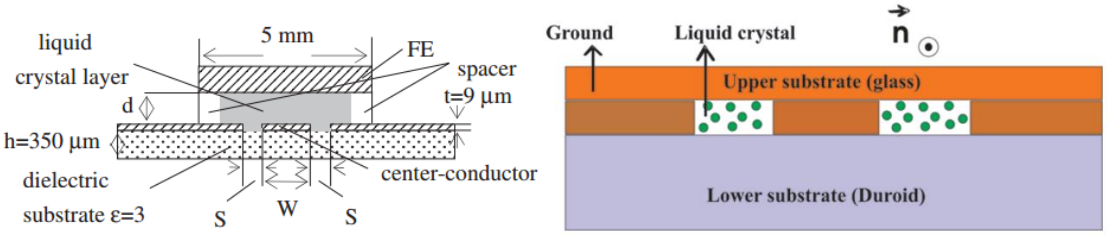
Fourthly, the available range of characteristic impedances is larger for CPW (30Ω–140Ω) than that of the IMSL (25Ω–95Ω). Unlike IMSL and strip line, in which the core line width is heavily limited by the LC layer's thickness for a controlled impedance (50Ω) structure, the impedance of CPW depends on one more geometrical aspect ratio, i.e. the strip-to-slot width ratio, with the performance less sensitive to the dielectric thickness. In other words, CPW possess more degrees of freedom than IMSL for geometry optimisation, in particular the metal thickness T_{strip}, and the signal-to-ground spacings (W_{gap} and LC thickness T_{layer}). This provides the

possibility to miniaturise the circuit with low-loss performance up to much higher frequencies towards 60GHz-90GHz.

2.4.3 LC-based Traditional CPW with Top-floated Electrode (FE CPW)

2.4.3.1 Two Existing Groups of Structures for LC-based CPW Phase Shifters

According to the literature survey, existing LC-based CPW phase shifter structures are divided into two approaches, i.e. with and without top-floating electrode as shown in Fig.19 (a) and (b) below, respectively (cross-sectional view). They differ in the electrode configuration as well as the LC tuning mechanism.



(a) With LC Layer on Top (Kamei, 2010) (b) Without LC Layer on Top (Sahbani, 2011)

Fig.19 Recent Advance in the LC-based CPW Phase Shifter Structures

Fig.19 (a) reports a CPW cell with ITO glass as floating electrode (FE) and LC sandwiched in between in response to current IMSL's slow switching problem (Kamei, 2010). With a transparent electrode on top, light-wave measurement is conducted observing the transitional movements of NLC molecules under different biasing scenarios. However, the insertion loss and achievable differential phase shift of the structure have yet to be reported.

Instead, the one presented in Fig.19 (b) only puts LC into the two coplanar slots as effective tunable region. With 5CB NLC, the designed 14mm-long CPW with 35µm-thick Cu exhibits an insertion loss of -4.3dB at 40GHz. However, the maximum differential phase shift only reaches 17˚ with a saturation bias of 10V.

2.4.3.2 Analysis of the Floating Effect on 60GHz

If the top conductor is not electrically connected to the coplanar grounds, the CPW exhibits a top-floated electrode structure (CPW-FE) as designed by several Japanese research groups including [46] [47] [71] [78] and [79] in their LC characterisation experiments. The biasing

arrangement of the electrodes at low frequency and the resulting conductor-backed CPW (CBCPW) stray mode at microwave frequencies is illustrated in Fig.20.

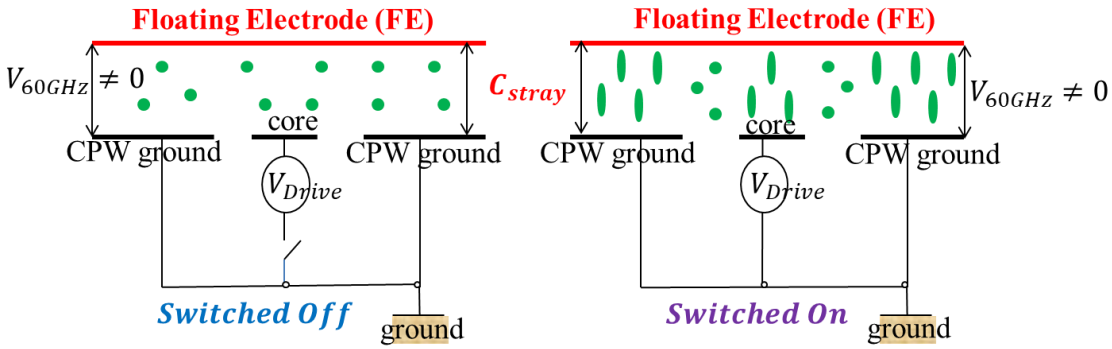
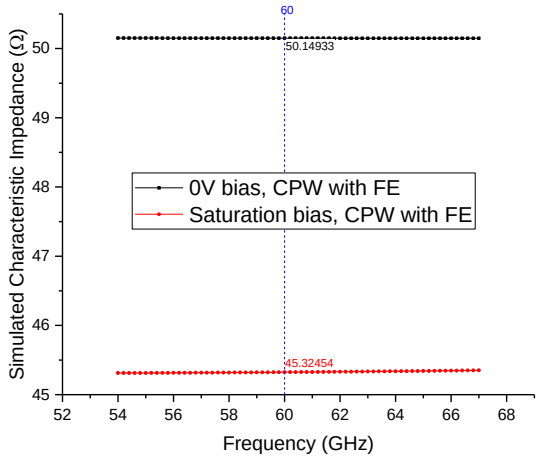


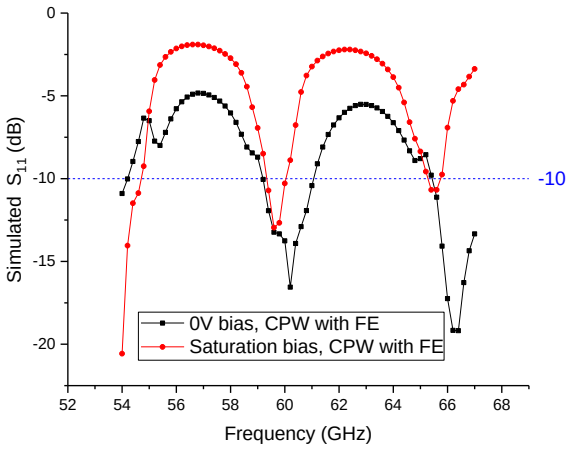
Fig.20 Parasitic CBCPW Mode due to the Floating Electrode (FE) on Top

Physically, the floating effect introduces fundamental problems that impede the circuit functions properly. Firstly, at low frequency, the floating electrode does not reorient the LC in a controlled and efficient manner, as the electric potential difference between the core and the floating one is unknown. Secondly, at millimetre-wave frequencies, the potential difference between coplanar grounds and the top electrode produces stray modes that degrade the fundamental TEM mode's signal transmission. The standing waves produced can even resonate at circuit features comparable with a quarter of the guided wavelength.

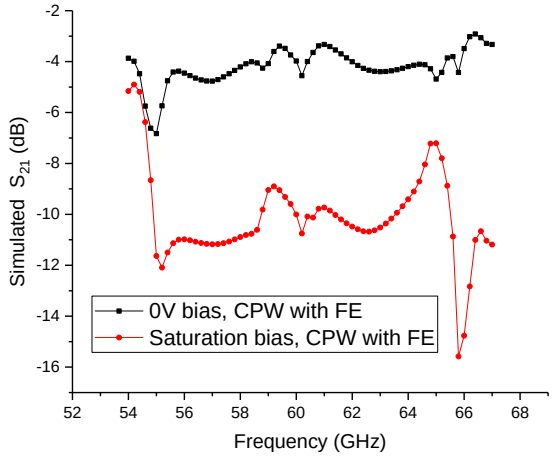
As illustrated in Fig.21 below, we simulate a CPW with top floated electrode (FE) with the geometry matched at 60GHz under 0V bias (where $\varepsilon_{r,\perp}$=2.5 is assumed for the LC layer) and targeted for a maximum phase shift of π (under saturation bias where $\varepsilon_{r,||}$=3.3 is assumed for the LC layer).



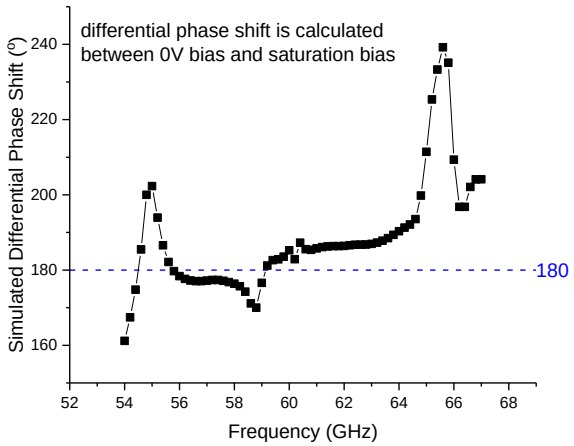
(a) Characteristic Impedance



(b) Return Loss



(c) Insertion Loss



(d) Differential Phase Shift

Fig.21 Simulated LC-based CPW with FE (54GHz-67GHz), Matched at 60GHz and 0V Bias

From the simulation results, we can conclude that the floating structure impedes a wideband operation of the CPW. As evidenced by the high return loss across 54GHz-66GHz except the 60GHz and 66GHz for low-reflection operating, such a narrow band capability contradicts with the 50.1Ω simulated impedance-matching across 54GHz-67GHz under 0V bias. The high return loss is due to the excited higher-order modes owing to the unequal potentials between the core and the floating electrode.

The dispersion of the simulated impedance is low, but a 5Ω difference between 0V bias and the saturated bias is observed. In most literature reported, the maximum insertion loss normally occurs at the 0V bias since the LC dissipation factor (loss tangent) at the $\perp$ state is at maximum. However, for this CPW-FE structure, the saturation bias state becomes most problematic due to the shortest guided wavelength at this state ($\varepsilon_{r,||}$ is assumed) and hence more vulnerability to resonance of parallel plate mode that strongly radiates into surface waves on the substrate. As a consequence, the insertion loss at the saturation bias (where LC absorption is minimum) even outweighs that of 0V. A 5-9dB difference in S_{21} between 0V and the saturation bias (corresponding to 0 and π shift of the phase) is observed, which is undesired for a phased array system (requiring amplitude compensation networks for each delay line, which are lossy and bulky). In recognition of these detrimental impacts of the floating ground at 60GHz, we summarise the importance of a unified ground in section 2.4.3.3 below.

2.4.3.3 Importance of a Unified Ground at 60GHz

In the multi-conductor system of a CPW (one core, two ground planes) and a top conductor, the non-unified ground return paths not observable at low frequency (long wavelength) makes a difference at 60GHz due to the vulnerability of exciting higher-order modes and cavity resonance especially at structural discontinuities with sizes comparable to a fraction of the guided wavelength.

As depicted in Fig.22, the ill-judged unequal potential problem in multi-conductor transmission lines (i.e. CPW, CBCPW) becomes more pronounced at millimetre-wave frequencies, which limits their operation bandwidths due to the propagation of undesired slot line mode (in CPW), parallel plate mode and waveguide mode (in CBCPW). The slot line mode (zero-frequency cut-off) is an odd mode with higher field intensity at one slot than the other. The parallel plate and waveguide modes are discussed further in section 2.6.3.

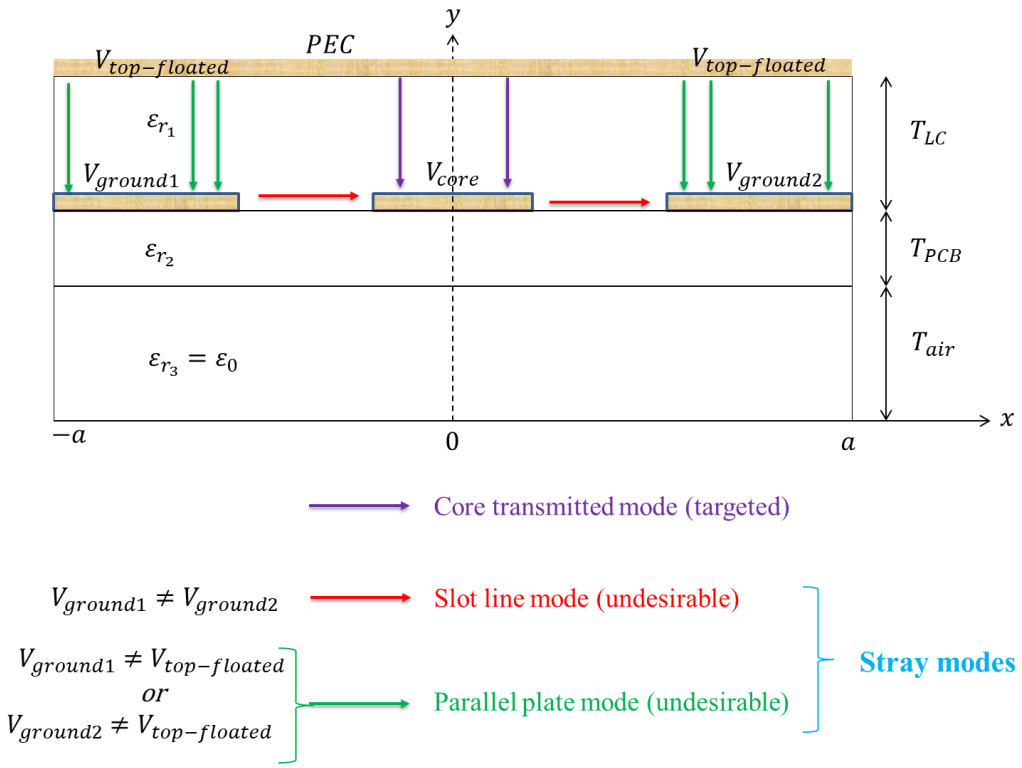


Fig.22 Stray Modes in a CPW and CBCPW with Floating Electrodes (FE)

A LC superstrate [11] reports a top-grounded CPW using a metal housing in contact with the coplanar grounds to enable on-waver probe measurement. This superstrate overcomes the problems due to floating electrodes. However, the top grounded CPW designs reported so far are for LC characterisation purpose only, i.e. by extracting the effective dielectric constant from the *S*-parameters measurement using a three-finger contact probe station. The loss properties

are neither reported nor analysed. These ill-designed structures have yet to constitute a low-loss phase-shifting device level for modern communications or radar systems.

2.4.4 LC-based Traditional CPW with MEMS Switches

A state-of-the-art CPW millimetre-wave phase shifter combining LC varactors with MEMS switches [13] is shown in Fig.23 below.

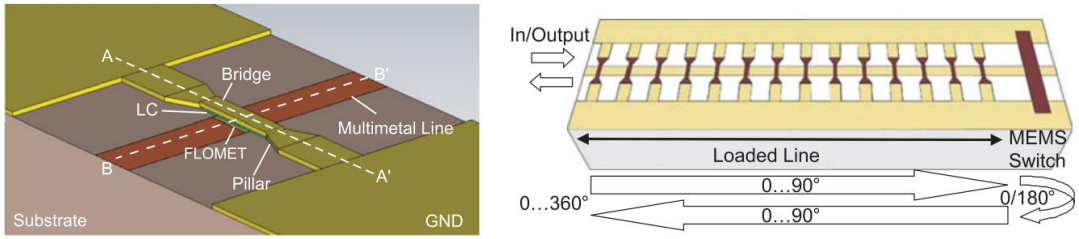


Fig.23 A Tunable 2π Reflection Type Loaded Line Phase Shifter [13]

The CPW loaded by LC varactors underneath MEMS bridges produces a differential phase shift of 92˚, and an insertion loss of -2.2dB at 76GHz. This hybrid prototype takes advantage of the MEMS-distributed transmission line and LC's continuous tunability for 2π modulation. Relatively fast switching speed (2ms for rising and 21ms for decay) is reported due to the ultra-thin LC layer (only 1.6μm) required for the varactors. However, the resolution is still digital in nature and highly limited for precise beam steering. The mechanical-based device also suffers from reliability issues.

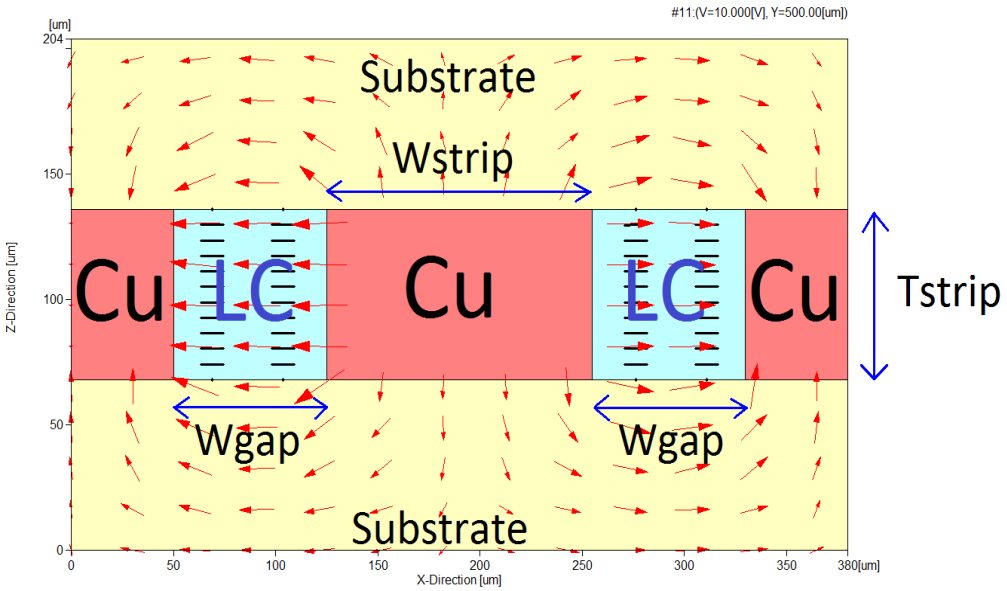
In a summary, currently reported LC-based CPW continuously-variable delay lines exhibit an advantage of low dispersion, but the very low tuning range and hence small differential phase shift makes it incapable to compete with state-of-the-art IMSL or coaxial cable (in the same length) below 50GHz, and struggles to outperform waveguides beyond 60GHz. For a fixed LC material, improved device tuning range means reduced physical length requirement for a specified phase shift, thus the transmission line can be made more compact with fewer bends and thereby minimising extra loss associated with discontinuities and couplings.

2.5 Proposed CPW with no Floating Electrodes (FE-free CPW)

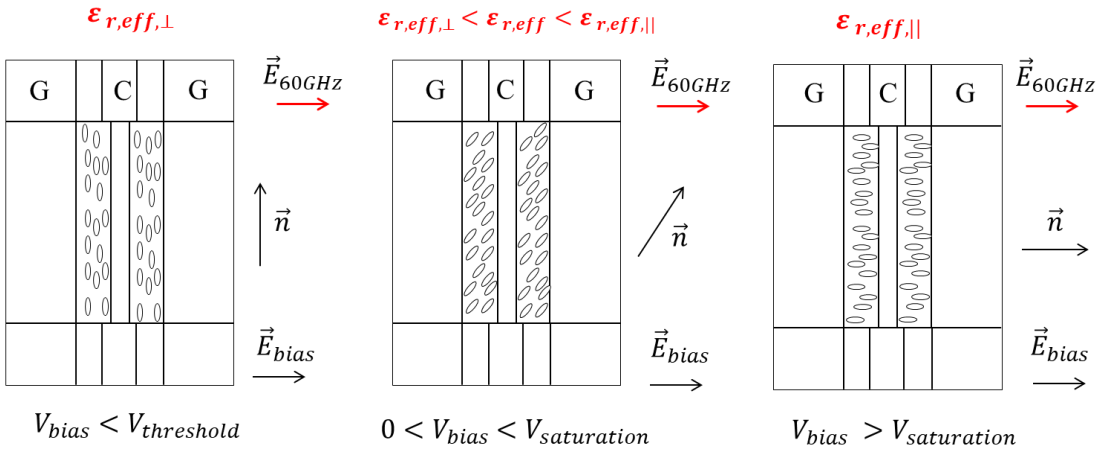
To our knowledge, few research reports so far have been concerned with how to increase the tuning range of CPW phase shifters. Specifically, no work has been carried out on optimising CPW geometry by making more efficient use of LC's anisotropic dielectric properties. The geometrical effect on modes and different loss mechanisms has yet to be studied. This provides us opportunities to take countermeasures and push the LC-based millimetre-wave technology forward.

2.5.1 Floating Electrode Free CPW Structure (FE-free CPW)

In response to the aforementioned limitations, we firstly proposed a floating electrode free (FE-free) CPW design for LC-based phase shifters. By contrast with conventional CPW-FE structures with undesired floating effect (section 2.4.3), the proposed FE-free CPW device can be modulated by nematic liquid crystals confined in two symmetric feeding channels as shown in Fig.24 (a) (b) below. The nearly true-TEM nature of this CPW design enables wideband and low-loss operations, particularly in high frequencies up to 90GHz. The results of this chapter have partially been published in the Proceedings of 46th European Microwave Conference [32].



(a) Cross Section Sketch of the Proposed LC-based FE-free-CPW with TEM Mode



C: core line G: ground
$\vec{n}$: LC director

(b) Bias Voltage Dependent Tuning of the Proposed LC-filled FE-free-CPW (Top View)

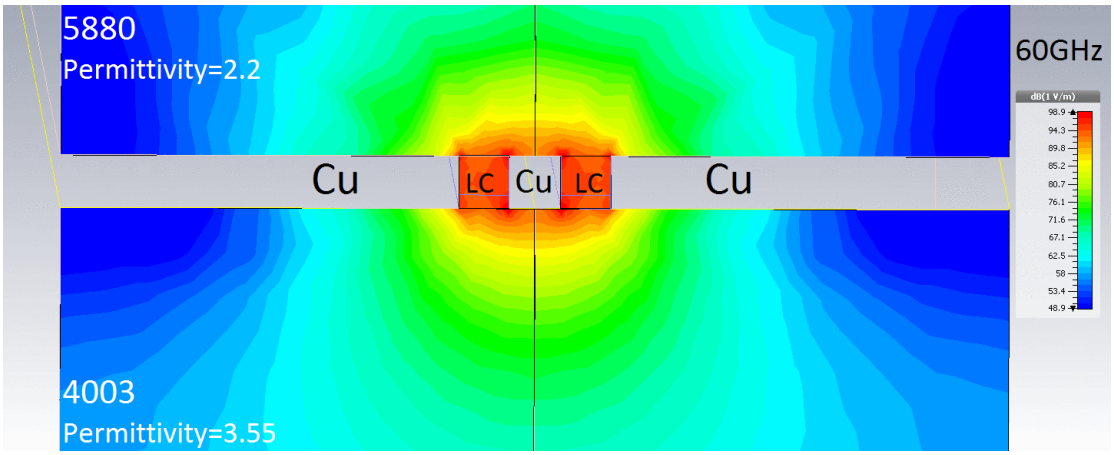
Fig.24 Proposed LC-based Floating Electrode Free CPW (FE-free-CPW) and the Tuning Mechanism

As shown in Fig.24 (a) above, the proposed FE-free CPW with copper strip thickness (T_{strip}) of 70μm, and channel width (W_{gap}) of 75μm filled with the LC is modelled using LCD Master (Shintech). LC alignment is set as 90º pre-twist in line with the millimetre-wave propagating direction. Macroscopic data of the nematic LC (GT3-24002) used in this work are: $\varepsilon_{r,\perp}$=2.5, $tan\delta_{\perp}$=0.0123, $\varepsilon_{r,||}$=3.3, $tan\delta_{||}$=0.0032 [32]. In this work, we investigate a new method for a marked improvement in the device's tuning range by maximising the effective wave-occupied volume in the tunable part, and propose a novel driving-voltage dependent impedance matching scheme (Chapter 4.1). By quantifying the impact of the substrate's dielectric constant (section 2.5.2) and geometrical aspect ratios (section 2.5.3) on tuning range, insertion loss and impedance, multi-objective optimisation using HFSS (High-Frequency Structure Simulator) and LCD Master is performed obtaining the optimum FE-free CPW structure by simulation.

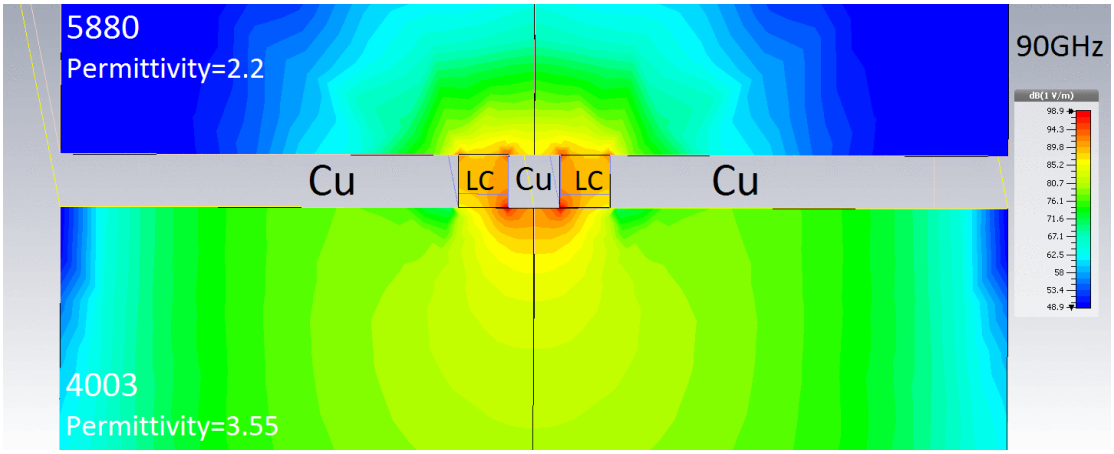
2.5.2 Tuning Range Study and Impact of Substrate Materials

Millimetre-wave travels both in LC-filled channels and sheltering substrates, thus the tuning range (*TR*) as defined in section 2.1.2 is influenced by the millimetre-wave-occupied volume (*WoV*) in the tunable dielectric part relative to the outside non-tunable part. For a fixed LC material, *TR* is closely connected to device geometry (aspect ratio effect) as well as material

properties of sheltering substrates interacting with millimetre-wave fields outside the tunable part. By ways of illustration in Fig.25 below, we put a RT/duroid 5880 (ε_r=2.2) on top, whilst a RO4003 (ε_r=3.55) at bottom of a LC-filled CPW to investigate the difference of millimetre-wave propagating behavior in different substrate materials. Simulated electric field intensity is compared between Fig.25 (a) and (b) based on the same color-bar system.



(a) Simulated 60GHz Electric Field Intensity Distribution (Input Power = 1W)



(b) Simulated 90GHz Electric Field Intensity Distribution (Input Power = 1W)

Fig.25 Simulated Effect of Dielectric Constant and Frequency on Electric Field Distribution

When the frequency increases towards 90 GHz, there is clearly a large proportion of millimetre-wave-occupied volume in the non-tunable 4003 substrate, whereas this phenomenon is less pronounced for the 5880 with smaller dielectric constant. Note that LC permittivity decreases gradually with frequency. This exacerbates the millimetre-wave dispersed into substrates with high permittivity, and hence degrading *TR* as evidenced by Fig.26 below, where *TR* of three designs with different substrates (but each design with identical substrate materials for top and bottom) is simulated.

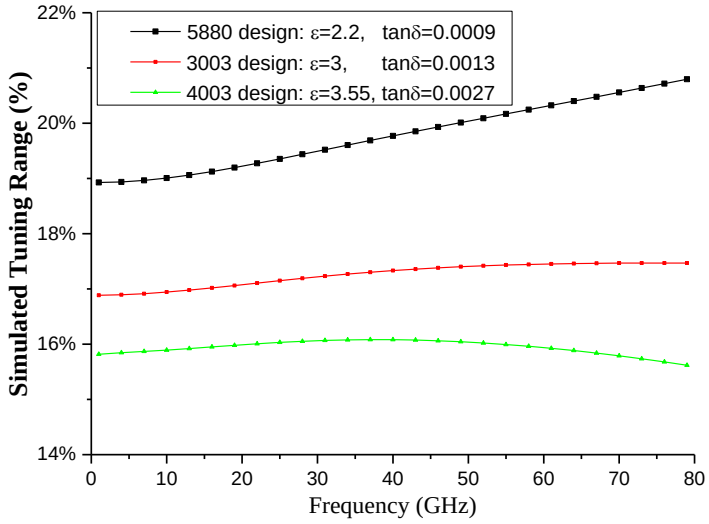
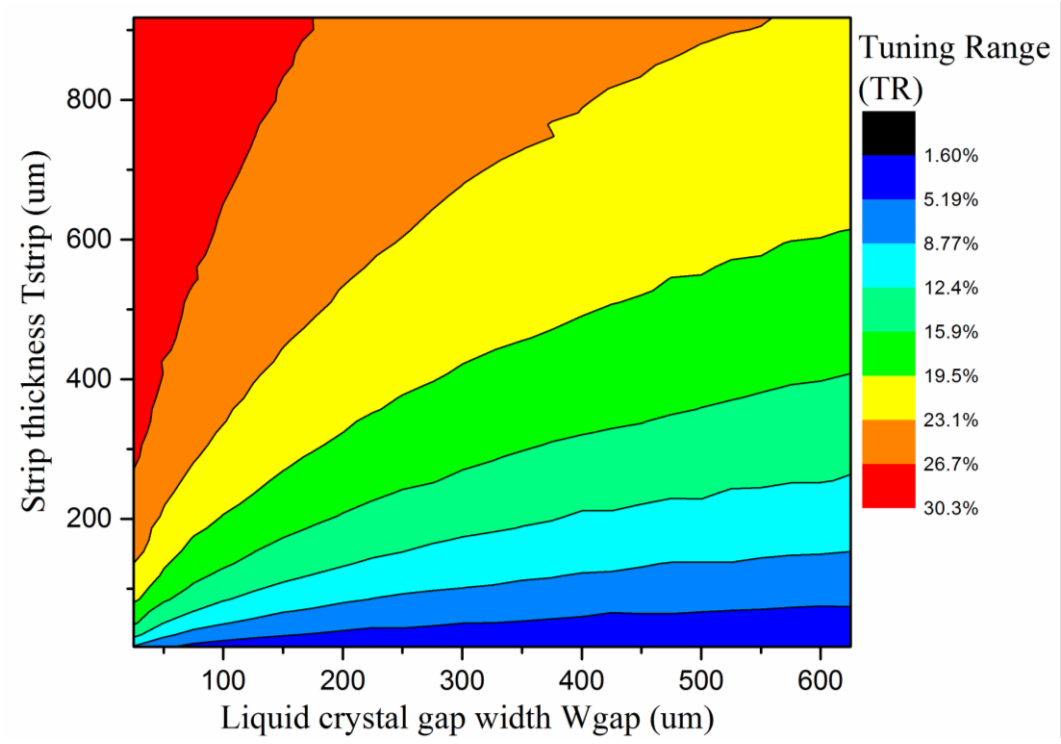


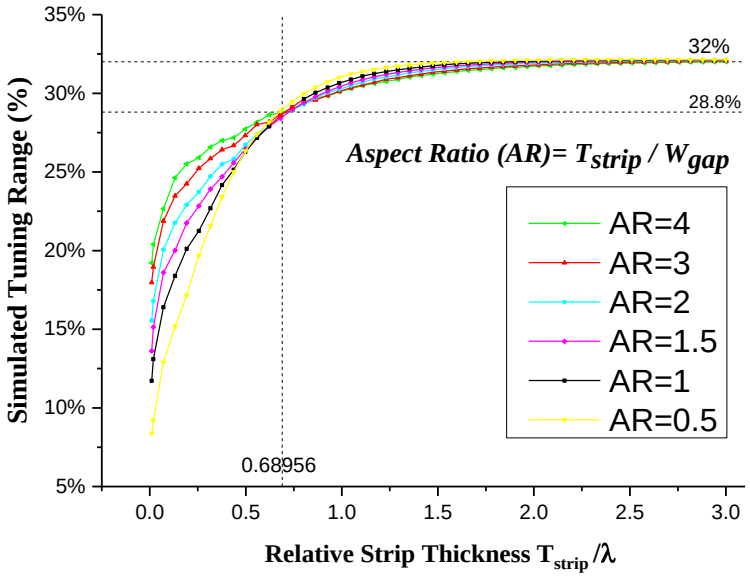
Fig.26 Simulated Dispersion of *TR* for FE-free-CPW Designs using Different Substrates

2.5.3 Aspect Ratio Effect on Modes and Tuning Range

Geometry-dependent CPW mode affects the millimetre-wave-occupied volume (WoV_{eff}) within the tunable channels and hence the *TR*. As depicted in Fig. 27 (a), we perform simulations and obtain a library of *TR* parametrized with respect to T_{strip} and W_{gap}. Aspect ratio (*AR*), defined as the ratio of T_{strip} to W_{gap} in Fig.27 (b), is used to further investigate the geometrical size (compared with wavelength) effect on the modes evolution and *TR*.



(a) Effect of Geometry Size on *TR* (79 GHz, Saturation Bias)



(b) *TR* vs. T_{strip} at Different *AR* (79 GHz, Saturation Bias)

Fig.27 Simulated Geometrical Aspect Ratio Effect on Tuning Range (79GHz)

As shown in Fig.27 above, the rise of T_{strip} increases WoV_{eff} and hence improves *TR* due to mitigation of radiation outside the tunable channels. When $T_{strip} << \lambda/2$, higher *AR* (i.e. narrower W_{gap}) leads to a larger *TR* before *TR* begins to saturate when $T_{strip} \approx \lambda/2$, as the generation of TE_{10} mode and 2D propagation partially reduces $WoV_{eff.}$ Specifically, we observe that W_{gap} loses its impact at $T_{strip} \approx 2\lambda/3$, where each *AR* design exhibits the same *TR* (28.8%). When $T_{strip} > 2\lambda/3$, the trend even reverses (i.e. a lower *AR*, a larger *TR*), but finally all level off at 32%, with minor difference observed. To quantify the modes transition effect, we present *TR* vs. *AR* (by varying W_{gap} for each T_{strip}) in Fig. 28 below. With $T_{strip} << \lambda/2$, the proposed CPW exhibits a nearly true-TEM mode, *TR* rises almost linearly with *AR*, as the tuning capacitance per unit length is governed by eq.9.

$$C = \varepsilon_{r.eff} \times \frac{T_{strip}}{W_{gap}} = \varepsilon_{r.eff} \times AR \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (9)$$

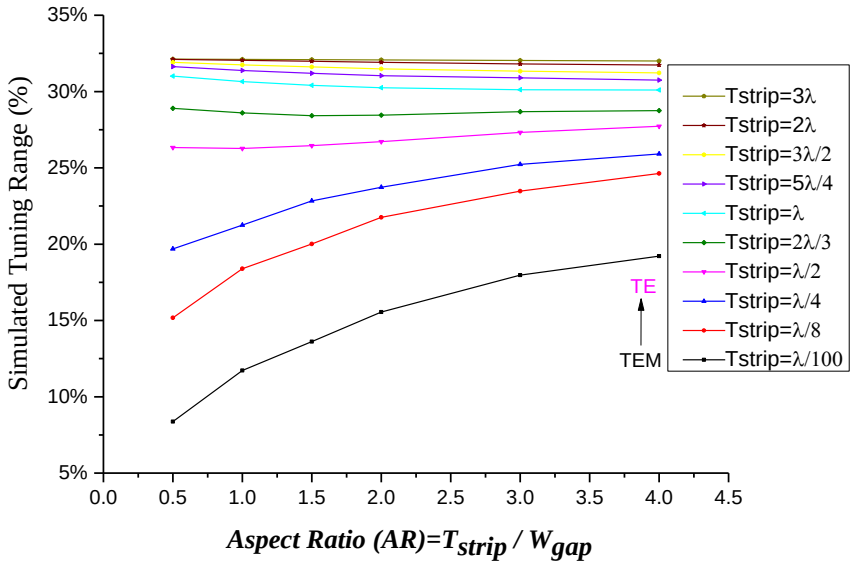
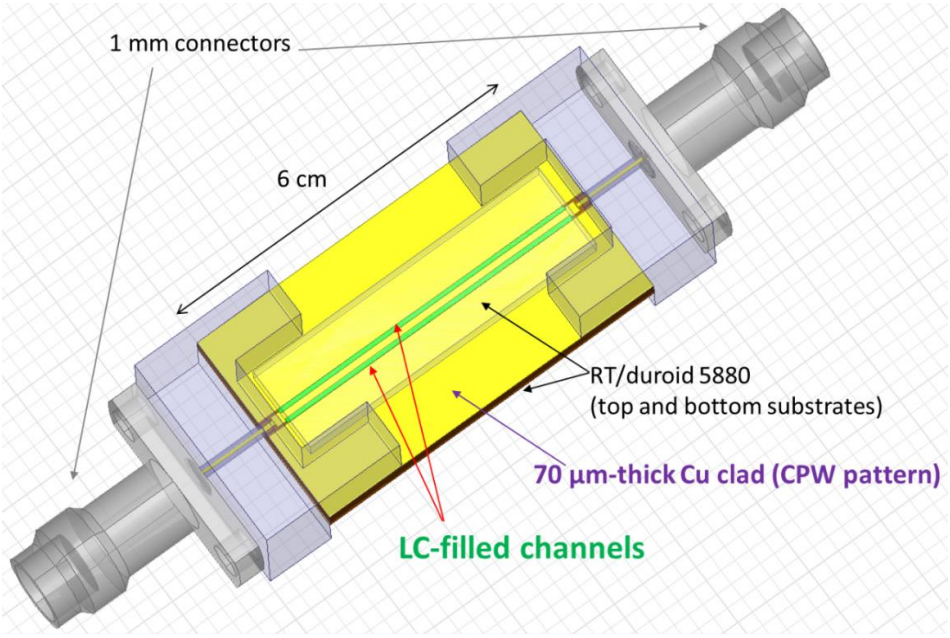


Fig.28 Simulated *TR* vs. *AR* (79 GHz, Saturation Bias)

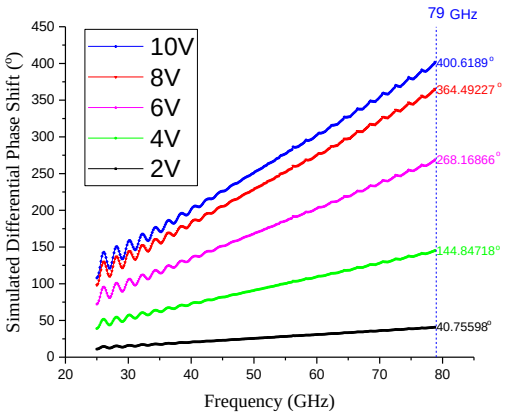
With T_{strip} rising towards $\lambda/2$, the millimetre-wave electric field pattern variations become pronounced along the strip height, as TE_{10} mode begins to dominate each channel (slot). The rate of change in *TR* with *AR* drops gradually to 0, and turns negative with $T_{strip}>2\lambda/3$.

2.5.4 Performance Analysis by Simulation

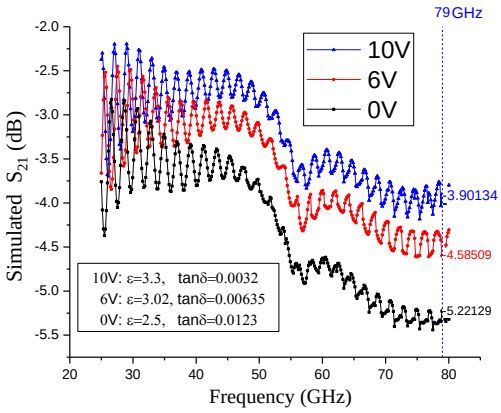
To optimise between tuning range and insertion loss, the aspect ratio of the CPW structure is optimised to maximise the defined Figure-of-Merit (*FoM*), i.e. the ratio of the largest phase shift to the largest insertion loss. By considering different loss mechanisms (Chapter 3.4) in the designed structure and the effect of LC orientations, the driving-voltage dependent impedance matching (Chapter 4.1) is examined to minimise the return and insertion losses. As an example, we present a phase shifter design aimed at 79 GHz in Fig.29 below, showing a wide phase shift range of 0-400˚ and a low insertion loss from -5.2dB to -3.9dB, i.e. a corresponding *FoM* of 76.9˚/dB.



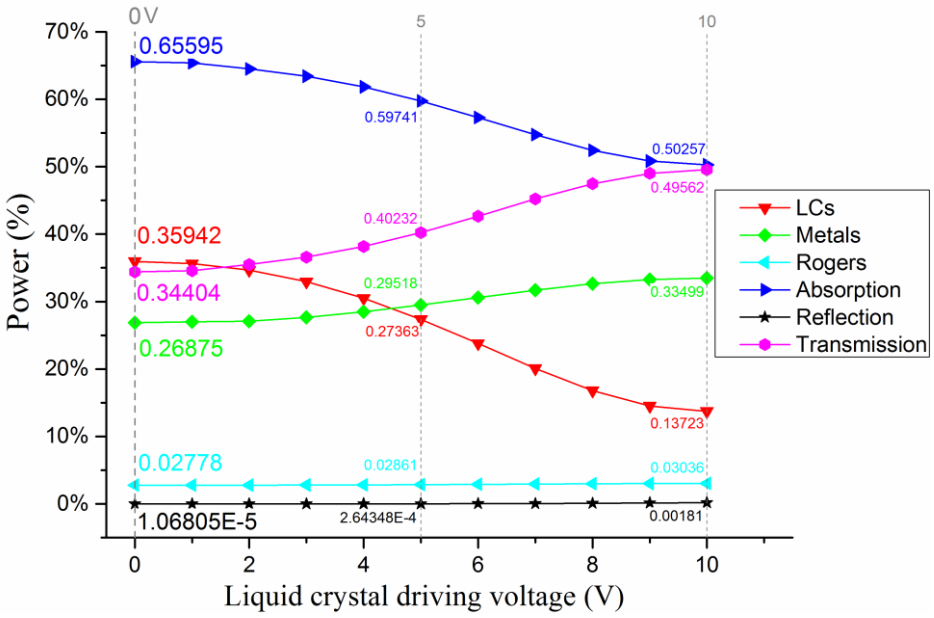
(a) Simulation Model Established for LC-based FE-free-CPW Phase Shifter for 79GHz



(b) Simulated Differential Phase Shift



(c) Simulated Insertion Loss (with Connectors)



(d) Loss Decomposition Analysis for the 0V-bias-Matched Design

Fig.29 Simulation Results for the Proposed LC-based FE-free-CPW Phase Shifter

Note that from Fig.29 (d), the total absorption loss predominately follows the trend of the LC loss, and largest insertion loss (lowest transmission) always occurs at 0V bias. Therefore, we strategically match our design at 0 V, so that the largest insertion loss is minimised compared with that by matching at other bias voltages.

2.5.5 Challenges in Heavy-Cu Patterning and Alignment inside

The performance has yet to be experimentally verified due to the limited precision and high costs in the high-profile electrodes patterning on extreme (heavy) copper (2oz, i.e. 70μm). The gerber files of the PCB design for photolithography are shown in Appendix B. By experiment, however, the classical UV-lithography fails to produce precise sidewall properties due to pronounced undercuts.

Laser ablation as an alternative method is attempted. We pattern the 70μm channels for CPW by a 1065nm fiber laser with pulse diameter of 30μm, but it suffers severely from post-ablation debris and the recast layer formation (as shown in Fig.30 below), distorting the conductor's profile significantly. Moreover, the unremovable recast at the core line edges (wherein is the maximum electric field confinement) with degraded conductivity exhibits appreciably elevated conductor loss. The recast removal and the incidence angle of the laser pulse merit optimisation to minimise the sputtering's secondary deposition, and improve the shot-to-shot reproducibility.

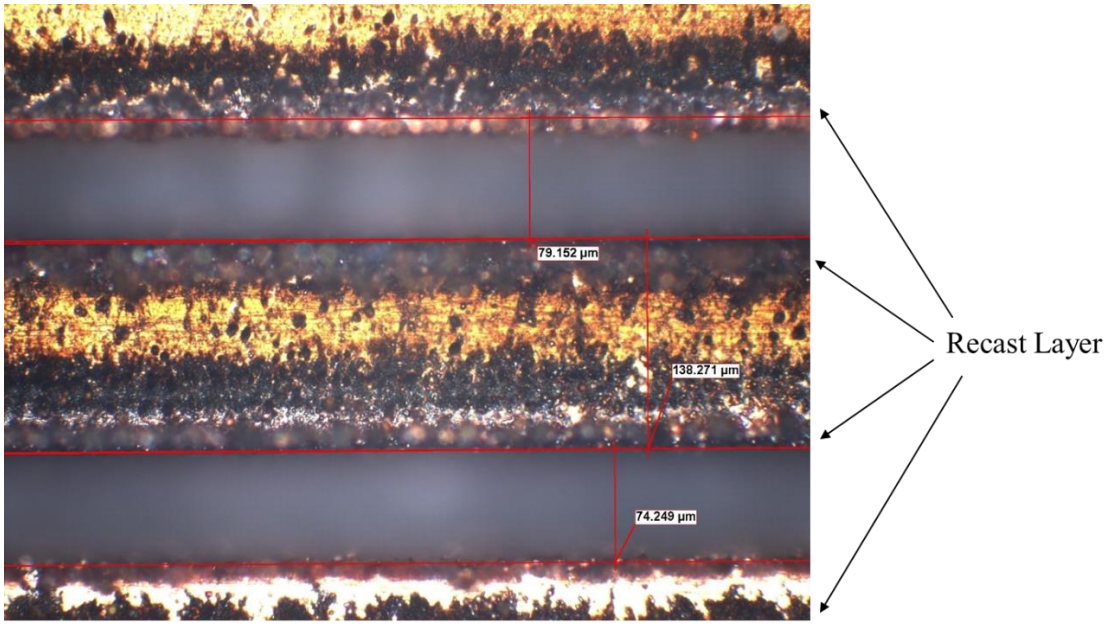


Fig.30 Fabricated FE-free-CPW with 70μm-thick Cu by 1065nm Laser Ablation (Top View)

A promising candidate to manufacture such high-aspect-ratio structures with large conductor height (70μm) while a vertical sidewall profile is required, is LIGA (German acronym for a three-stage micromachining technology, including X-ray lithography, electroplating and molding). However, the X-ray lithography based on synchrotron radiation is by no means a cost-effective solution.

Assuming the thick-Cu patterning problem can be addressed, rubbing inside the high-profile channels poses another biggest challenge. Pile contacting inside such channels with a large depth (70μm) and a narrow width (75μm) is technically demanding for standard mechanical rubbing wherein a low aspect ratio of height to width is desirable. Optical alignment is envisioned in place of the mechanical rubbing. We experimentally test a mixture of LC and CPND7 azo dyes for photochemically-induced order-disorder change in LC alignment using a 473nm laser. However, the effective range (depth) is only up to 10μm. Moreover, the azo dye is highly lossy at the millimetre-wave length range and hence not suitable for our device.

2.5.6 Limitations of the Proposed LC-based FE-free CPW

In conclusion, the pilot research we have done above shows that the floating electrode free CPW (FE-free) we initially propose is not the optimal structure for 60GHz phase shifting devices. We summarise the limitations of the FE-free CPW structure as below.

From the device physics point of view, phase tuning of the proposed FE-free CPW is entirely based on the two coplanar vertical channels (slots), instead of a planar cavity in a standard structure such as the inverted microstrip line (IMSL). The low wave-occupied-volume ratio of tunable LC versus non-tunable substrate in the currently manufacturable FE-free CPW with 0.5oz (17μm-thick) or 1oz (35μm-thick) Cu clad results in a low tuning range (far less than the phase shift requirement of π for a compact line length) as compared with IMSL. We strategically increase the Cu thickness (T_{strip}) of the proposed FE-free-CPW to 2oz (70μm) and above for a drastic improvement in the wave-occupied-volume ratio of LC, and hence an appreciable increase in the tuning range (*TR*) and phase shift.

However, the increase of T_{strip} and hence the *TR* improvement is limited by the onset of TE-like waveguide modes when T_{strip} is comparable to $\frac{\lambda_{guided}}{2}$ (1.3mm for 66GHz). With substantial LC volume and metal surface area upon which the square of electric field is integrated, such a high-profile structure exhibits insertion loss behavior comparable to a standard strip line and IMSL, whilst the required thick-Cu patterning and surface anchoring inside a deep channel challenge the status of precision manufacturing and LC alignment technology. Furthermore, the structure shows a certain degree of similarity to a waveguide, which loses the planar advantages as held by a transmission line, e.g. cost-effectiveness in patterning and ease of alignment. Admittedly, such a thick-Cu design is arguably not the optimal approach of device structure for 60GHz, albeit the undesirable floating electrode effects are largely eliminated (but not completely, because the two coplanar ground planes are not electrically connected, there remains uncertainty in potential difference and slot line mode generation).

In recognition of the limitations of classical transmission lines and waveguides, the following structure properties are desirable for a 60GHz phase shifter device.

(1) Higher-order stray modes free

(2) Interference and radiation free

(3) Substantial wave-occupied-volume ratio of tunable LC

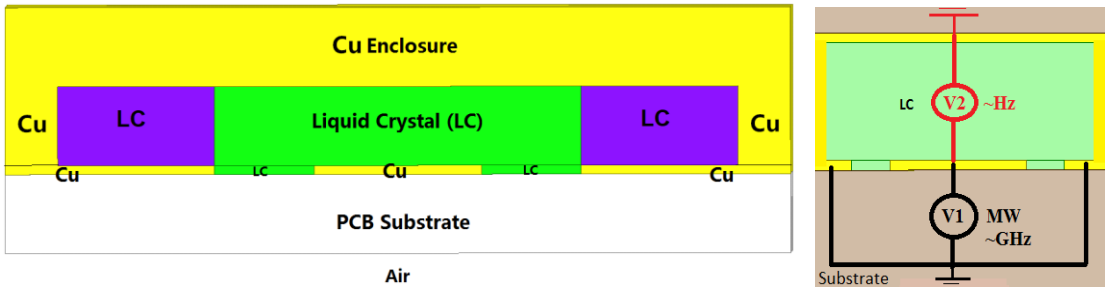
(4) Ease of fabrication and low-cost manufacturing

In response to these, a new device structure is proposed in Chapter 2.6 below, which combines all the advantages mentioned above.

2.6 Proposed Enclosed Coplanar Waveguide (ECPW) Method

2.6.1 LC-based Enclosed Coplanar Waveguide (ECPW)

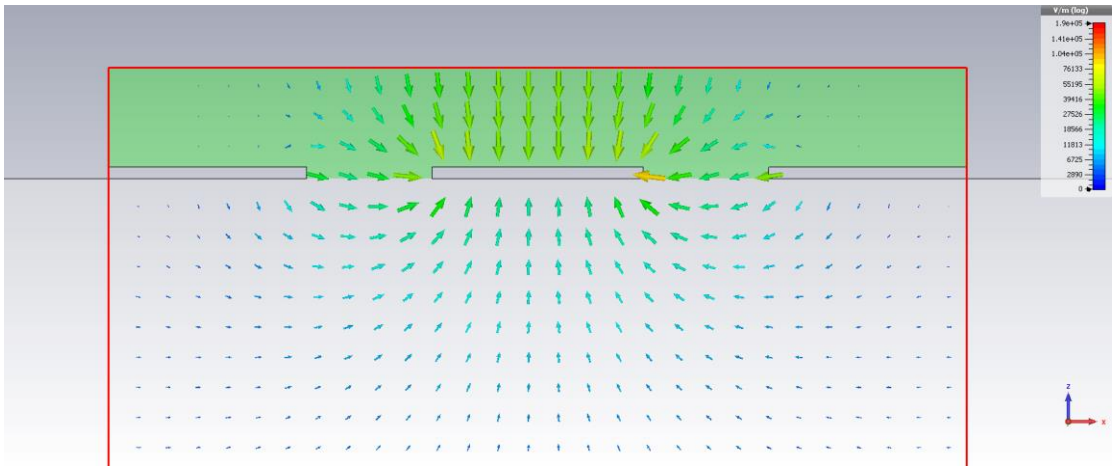
We propose a novel enclosed coplanar waveguide (ECPW) structure as shown in Fig. 31 (a) below, with the electrical biasing control scheme sketched in Fig.31 (b). The core line and a unified ground (combining two coplanar ground planes and the enclosure with continuous sidewalls) jointly guide an ECPW mode at 60GHz. They also function as electrodes for low-frequency biasing of LC molecules. The structure is developed based on our understanding in the importance of wave-occupied-volume of tunable LC on phase shift's tuning range, as well as the role of electrical connectivity between the top electrode and the coplanar grounds (section 2.6.2) on a unified ground path with floating-free properties. Compared with conventional LC-based CPW with a floating electrode on top for phase modulation, the top conductor in our proposed ECPW structure is electrically shorted with the two coplanar grounds by continuous lateral sidewalls densely spaced within half a wavelength, with the inner cavity's depth defining the LC layer's thickness.



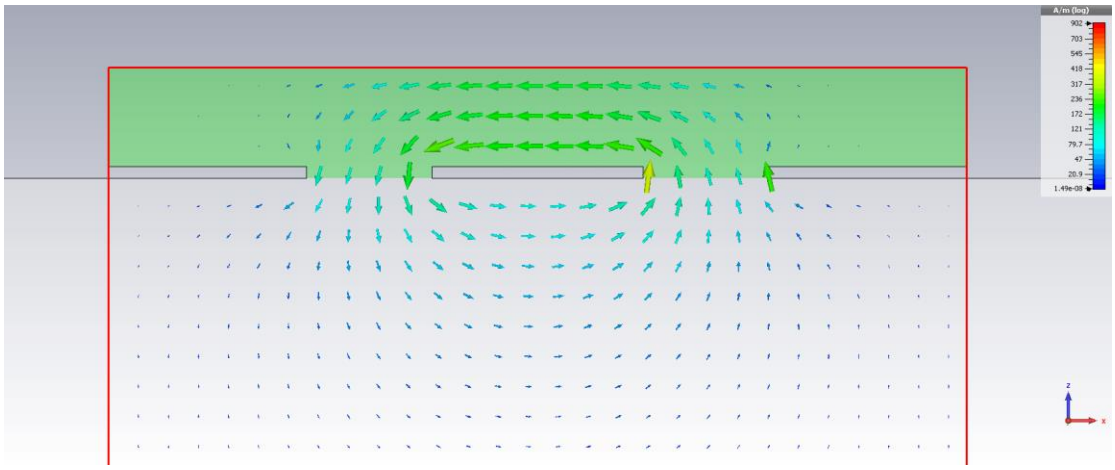
(a) Cross Section Sketch (b) Biasing

Fig.31 Proposed LC-based Enclosed CPW (ECPW) Structure and the Biasing Scheme

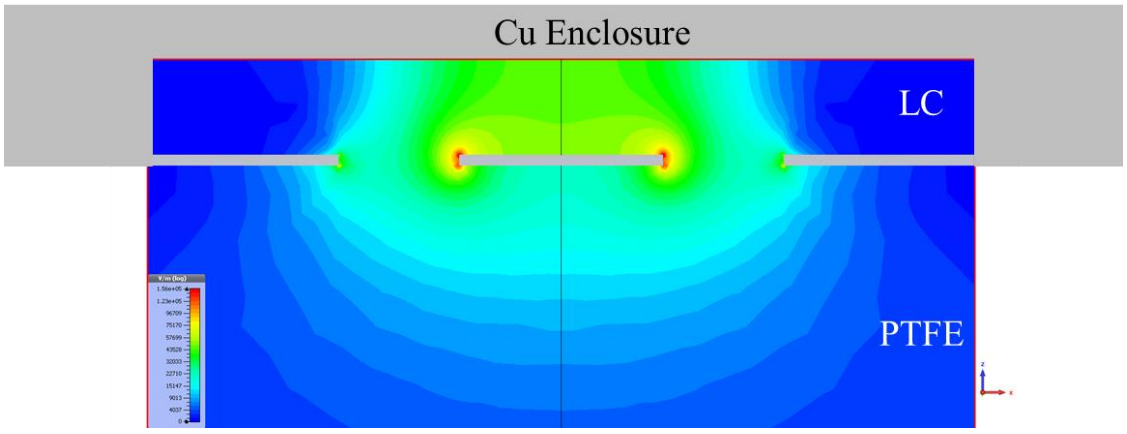
Fig.32 below illustrates the 60GHz mode (electric and magnetic vector fields and intensity distributions) exhibited by the proposed ECPW. The wave port analysed covers the critical elements of the structure, i.e. the core, coplanar ground planes, enclosure, LC-filled cavity and the PTFE substrate. This enclosure-attached structure equalizes the grounding electrodes' electric potential, hence allowing a true-TEM ECPW mode propagation while suppressing parasitic modes (e.g. zero-frequency cut-off parallel plate mode, uneven slot line mode, and the associated modes-coupling problems).



(a) 60GHz Electric Vector Field



(b) 60GHz Magnetic Vector Field



(c) 60GHz Electric Field Intensity

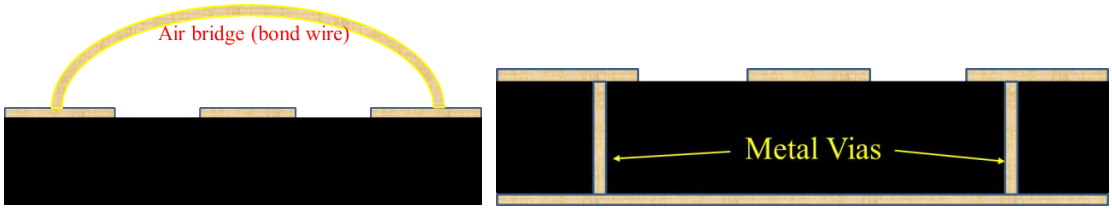
Fig.32 Simulated ECPW Mode at 60GHz for the Proposed ECPW Structure

With all the ground planes physically bonded, the top metal plate also provides mechanical strength and serves as a heat sink for high-power applications. In a summary, this via-free and bond wire-free ECPW topology including an enclosed ground plate provides a low-loss and

low-cost device-on-substrate solution. Note that the proposed enclosed CPW (ECPW) is patterned in two parts (PCB, and enclosure) and joined together by inverting the enclosure onto the PCB. The electrical contacts between them affect the conductor loss, and more fundamentally, defines the boundary conditions for the electromagnetic fields as studied below.

2.6.2 Connectivity between the Top Conductor and the Coplanar Ground Planes

As shown in Fig.33 the CPW-related structures, there are two traditional methods to mitigate higher-order modes generation due to unequal potentials between the coplanar grounds.



(a) Wire-Bonded CPW (b) GCPW with Vias

Fig.33 Typical Ways for Potential Equalization in CPW and CBCPW (GCPW)

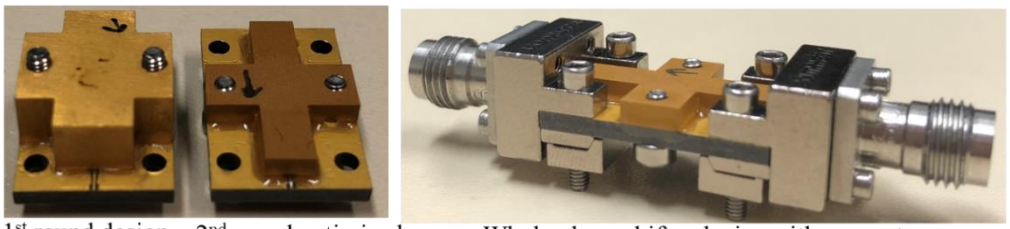
As shown in Fig.33 (a), conventional CPW uses air bridges (bond wires) to tie the two coplanar grounds together (to equalize the potential), forming a two-conductor transmission line. An air bridge is electrically modelled as a wire-bonded network consisting of series inductors with resistors and shunt capacitors. The resistor $R=\frac{L_{bridge}}{\sigma\delta P_{bridge}}$ is inversely proportional to the skin depth as well as the perimeter of the wire (P_{bridge}). Regarding Fig.33 (b), conventional conductor-backed CPW (CBCPW) employs periodically-placed vias (by plating-through-hole) to connect the coplanar grounds with the back conductor to equalize the potential, hence the name grounded CPW (GCPW). A via is modelled as a network consisting of at least a resistor in series with an inductor.

For the above structures, contact resistances of the interconnecting parts (i.e. air bridges, bond wires, or vias) are unacceptably large (due to limited contact circumference) for millimetre-wave low-loss applications. The high contact resistance can introduce appreciably large conductor loss in case of high-power applications with a high-frequency and large-amplitude current flow. Moreover, given the length of the bridge (wire) and vias are comparable to certain fractions of a wavelength, they can exhibit radiating properties like an antenna, hence degrading

signal transmission performance required by a phase shifter. To build electrical connections between the top ground conductor and the two coplanar ground planes underneath, traditional metal-bonding approaches by soldering (tin conductivity：0.867×10^7S/m) or placing Au wires (gold conductivity：4.1×10^7S/m) in between [88] produce substantial resistive losses due to the imperfect bounding layer with poor contacts, which directly leads to a degradation of the whole LC-based phase shifter's transmission by 10 dB/cm at 60GHz.

In this work, we propose and develop a low-loss (large-area and flat-surface contacts) and low-cost (electrical discharge machining) fast-prototyped enclosure solution which optimises the grounds connectivity. As depicted in Fig.34 below, we engrave an enclosure by electrical discharge machining (EDM) a narrow cavity at the bottom centre of a thick Cu plate to accommodate LC (i.e. the cavity depth defines the LC thickness), whilst producing continuous sidewalls with substantial contact areas with the CPW's ground planes. The sidewalls of the cavity replace spacers traditionally used in most LC-based structures, which provides improved uniformity of the LC layer (for electrical performance stability) and enables fast prototyping.

Proposed LC-based Enclosed CPW (ECPW) Structure



1st round design　2nd round optimised　Whole phase shifter device with connectors

Fabricated prototypes of the proposed LC-filled ECPW

Fig.34　Proposed LC-filled ECPW Structure from Design to Prototype

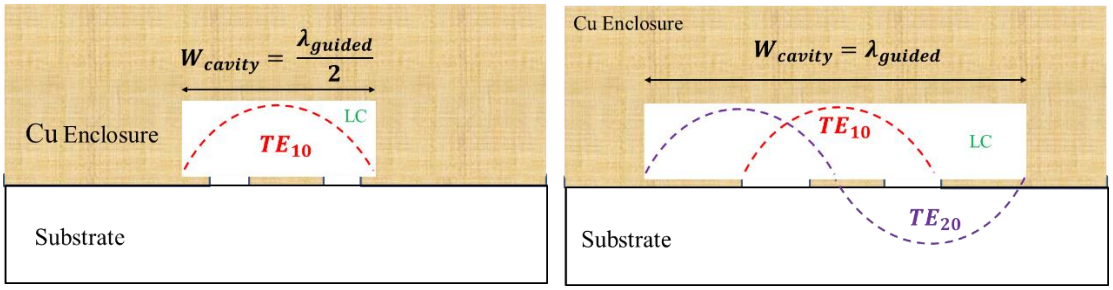
All the patterned conductors (enclosure and PCB) are gold-plated, with silver conductive paste (silver conductivity：6.3×10^7S/m) applied between the enclosure and the CPW's ground planes

for enhanced connectivity. Detailed prototyping and optimisation steps are interpreted in Chapters 6 and 7.

2.6.3 Upper Frequency Limit of a Single ECPW Mode Operation

With the wide and flat conducting sidewalls of the enclosure attached with the coplanar grounds, the parasitic parallel plate mode and uneven slot line mode are largely suppressed by our proposed ECPW structure.

However, the upper frequency for a single ECPW mode operation is limited by waveguide modes excitation depending on the dimension of the cavity as compared with the wavelength (i.e. the number of half wavelengths that the cavity can accommodate). It is worth noting that the enclosed CPW (ECPW) resembles a rectangular waveguide with two aperture slots to guide the electromagnetic energy. Providing that the largest cross-sectional dimension (i.e. spacing of sidewalls) is comparable or above a half of the minimum wavelength, higher-order rectangular waveguide modes cutting off are illustrated in Fig.35 (a) (b). This phenomenon can be explained by both classical electromagnetics and quantum electromagnetics.



(a) 1st Higher-order Stray Mode (b) 1st and 2nd Higher-order Stray Modes

Fig.35 Impact of the Cavity Dimension on Higher-order Waveguide Modes Excitation

When a higher-order mode coexists with the quasi-TEM mode above a certain frequency, it may disrupt the phase and loss performance since it will take away some of the energy of the quasi-TEM mode. The share of power that sustains the higher-order mode is inevitable due to energy conservation and the fact that the total energy propagating in a transmission line is finite. The presence of these modes can cause the fundamental ECPW mode's field distribution to spread across the entire cavity width instead of being confined to the slots and the regions above, hence degrading the tuning range. Moreover, it can lead to cavity resonance when terminating

at the coaxial connectors. According to the coupled-mode theory, power can be exchanged between modes as they propagate, depending on the transmission line length. The non-TEM modes' energy distributed outside the slots and the above region will not be detected by the 1.85mm coaxial connector with TEM nature. Instead, it will resonate in the cavity structure with a finite length. The larger this non-TEM energy is, the stronger the resonance.

To avoid excitation of the pseudo rectangular waveguide mode and ensure a resonance-free unimodal quasi-TEM wave propagation up to 67GHz, we limit the maximum cavity width (W_{cavity}) within half a minimum guided wavelength ($min.\frac{\lambda_{guided}}{2}$). The minimum guided wavelength is frequency dependent as well as bias-voltage dependent due to the tunable dielectric constants of LC, as calculated in Table 4 below.

Table.4 Limitation of Cavity Dimension Compared with Guided Wavelength for Signal Mode

	60GHz		67GHz	
	0V bias	Saturation Bias	0V bias	Saturation Bias
ε_{eff}	2.40	2.95	2.40	2.95
$\frac{\lambda_{guided}}{2}$	1.61 mm	1.46 mm	1.45 mm	1.30 mm
$Min.\ \frac{\lambda_{guided}}{2}$	1.46 mm		1.30 mm	
$Max.\ W_{cavity}$	1.46 mm		1.30 mm	

The minimum guided wavelength across 1GHz-67GHz is 2.6mm (under the saturation bias and considering the upper 67GHz signal), thus the width of the cavity (sidewalls spacing) is designed as 1.3mm. Measurement results and optimisation of the cavity dimension are detailed in Chapter 7.1 and 7.2.

Chapter 3. Computational Electromagnetics for LC-based Enclosed CPW (ECPW) at 60GHz

3.1 Transmission Line Computation Approaches and Assumptions

There are two approaches in analysing a transmission line, i.e. static and dynamic. The static (or quasi-static) approach produces transmission-line parameters (frequency-independent lumped capacitance and inductance) for TEM or quasi-TEM mode based on circuit theory, which is rigorously valid at DC only. This difference notwithstanding, this method can still provide design guidelines for devices up to the first higher-order mode frequency (e.g. millimetre-wave frequencies assuming unimodal condition). The upper frequency limit is determined by comparing the computed quasi-static transmission line parameters (e.g. by conformal mapping method) with the spectral domain values and observing the frequency at which the two sets of results deviate more than a few percent.

The dynamic (or full-wave) solution calculates frequency-dependent distributed transmission-line parameters (e.g. equivalent capacitance and inductance) based on wave theory. The dynamic approach can not only produce the frequency-dependent transmission-line parameters for the TEM or quasi-TEM mode, but also produce those for the higher-order modes, whose parameters are functions of frequency. For instance, the LC dielectric loss density $p = 2\pi f \varepsilon_0 \varepsilon_r' tan\delta |E|^2$ per unit volume, when integrating the density p over the volume to get volumetric loss, the static approach assumes a uniform $E(x, y) = \Delta V / T_{LC} = E$ (i.e. a constant) and hence the problem is simplified by taking E out of the volume integral. Such static assumption works only rigorously for a uniform field and no fringing field effect is considered (i.e. the distance between the two plates are sufficiently close, and two plates are infinitely large compared with the distance). However, the skin and proximity effects (non-uniform E) are not accounted for.

Nevertheless, the quasi-static approach may still be a quick design guideline for the enclosed CPW (ECPW) if we limit the dimension to much smaller than half a minimum wavelength (1.3mm) at the frequency range of interest (54GHz-67GHz), hence only a single quasi-TEM mode is supported. Performance at higher frequency may deviate from quasi-static estimation

due to the electromagnetic field's dispersion behavior as well as the skin and proximity effects, resulting in the wave-occupied volume ratio (*WoVR*) change, and higher-order (e.g. TE, TM or hybrid) modes excited particularly near discontinuities, etc. To obtain a closed form solution for effective dielectric constant and characteristic impedance, the analytical equations can be theoretically attempted by the conformal mapping method [14], spectral domain method [73], finite difference method [65], etc. The solutions are then compared with computational results from full-wave analysis and gone through experimental validation. We use a quasi-static approach to qualitatively estimate dielectric and conductor losses as a design guideline, and employ the full-wave dynamic approach to optimise the device structure.

3.2 Numerical Approaches and Adaptive Meshing

There is a spectrum of numerical approaches. The earliest computer-aided designs rely on distributed circuit-theory-based approach (i.e. by building Y-matrix of numerous nodes) without regard for the radiation loss and the mutual coupling mechanism. The solution time (matrix inversion) for the analytical transmission line models depends on the physical size of the network, instead of its size compared with the wavelength (i.e. electrical length).

3.2.1 Full-wave Approach based on Field Theory

Field-theory-based solvers are introduced to the distributed geometry for a more microscopic view [19], allowing all the electromagnetic effects (parasitic coupling between adjacent lines, interaction between discontinuities, potential interaction with the package or housing, surface waves, radiation, etc.) to be included into the analysis, although leading to a larger size of the numerical problem and hence a longer solution time.

The field-solvers subdivide the geometry by meshing 10 to 30 elements per guided wavelength. Surface meshing solvers (2.5D) based on Method of Moment (MoM) can handle standard strip or slot-based planar circuits. For arbitrary 3D geometries, waveguide discontinuities, transitions between different guiding systems (e.g. transition from CPW to microstrip), 3D volume meshing codes based on Finite Element Method (FEM) and Finite Difference Time Domain (FDTD) method are powerful.

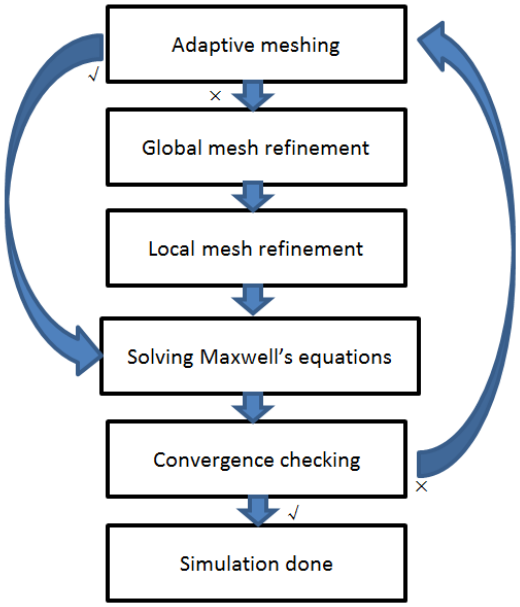
Both MoM and FEM require filling and inverting a matrix, while FEM's matrix is larger and sparse. The solution time is proportional to a factor between n^2 and n^3 where n is the number of nodes (Swanson, 2003). Thus, the required memory and solution time scale increase dramatically with the size of the problem. FDTD is a time-stepping code with the solution time linearly proportional to the size of the problem. However, the need to perform Fourier transform for huge numbers of sampling time steps makes it not a computationally efficient method for electrically-small filters or antennas structures.

For the benchmark purpose, we use two different solvers, based on different theoretical methods (integral and differential), to computationally characterise the LC-based phase shifter device. If both results are in good agreement within statistics, it is reasonable to argue that the models established are convincible by simulation.

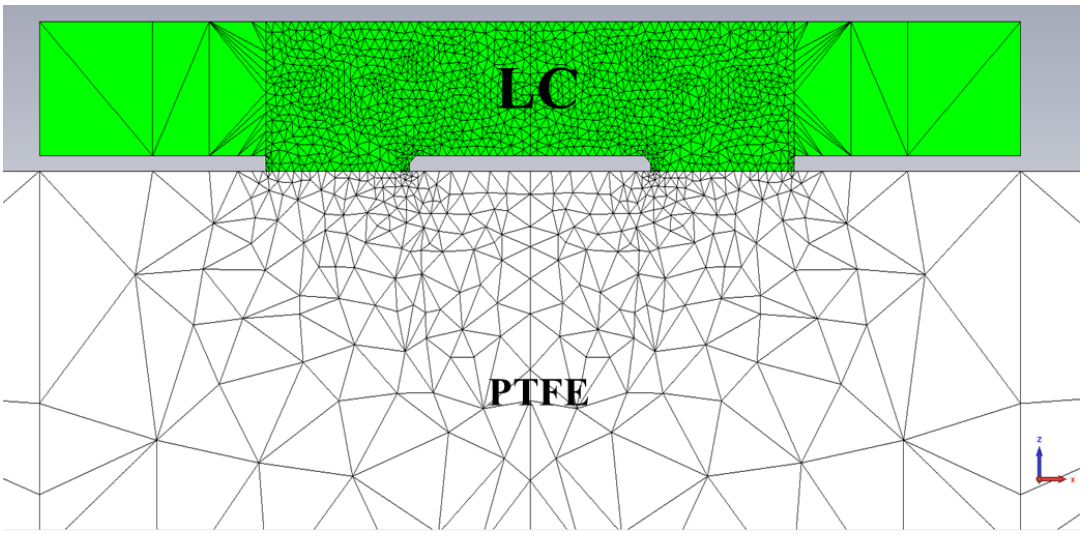
3.2.2 Adaptive Meshing inside Dielectrics

The prediction accuracy of the numerical approach can depend significantly on meshing. We investigate the convergence of meshing inside dielectrics in this section, and report the results for meshing metals in the next section 3.2.3.

We take frequency-domain adaptive meshing based on tetrahedral mesh as an example. The sensitivity of the full-wave simulation results to the tetrahedral meshing process is investigated to ensure reasonably accurate field approximations while alleviating the computation burden, i.e. a balance between accuracy and efficiency. This is based on the principle that when solving equations numerically, the numerical solution converges to an exact analytic solution in the limit of extremely fine meshes. In the frequency domain (e.g. FEM-based methods), the adaptive mesh refinement is done at one frequency only (typically the highest frequency of interest). Once the solution is converged at that frequency, the mesh is assumed to be valid (accurate) for all other frequencies. Fig.36 (a) below outlines the philosophy underlying the simulations we conduct in this study. Fig.36 (b) illustrates a case study we have performed for adaptive meshing a proposed LC-filled ECPW phase shifter with the core's top edge chopped by 45°.



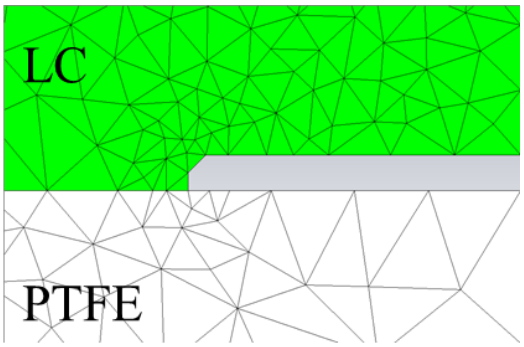
(a) Computational Electromagnetic Analysis Procedure (High-level) in this Work



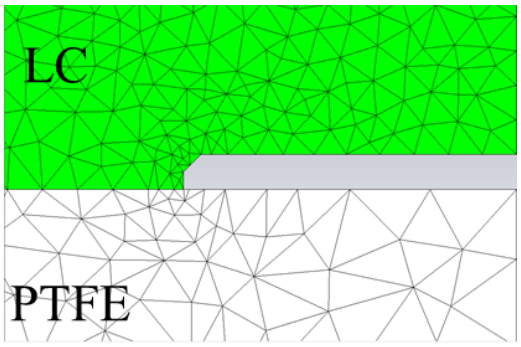
(b) Adaptive Meshing for a LC-based ECPW with Core Chopping Angle α_c=45°

Fig.36 Numerical Simulation Procedures and Adaptive Meshing for the LC-based ECPW

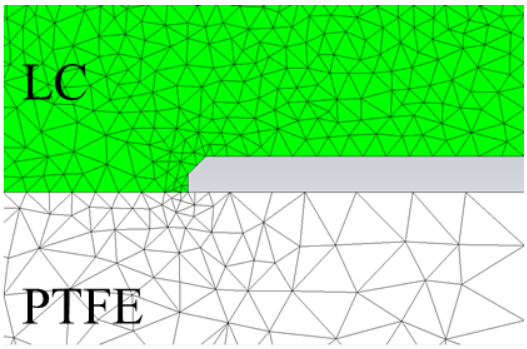
The number of mesh cells discretisation in the critical region affects the capturing accuracy of the field gradients. We therefore refine meshes around the electrode edges where the field gradients are high and of the greatest errors. The convergence criteria of $\left|S_{21_{i+1}} - S_{21_i}\right|$ is restricted within 0.005dB, below which the mesh refinement will terminate. Looking into the meshed structure we depict in Fig.36 (b) above, the same geometry is solved at 60GHz in Fig.37 (a)(b)(c)(d) below, with different levels of adaptive-meshing refinement for the LC layer surrounding the ECPW's core line.



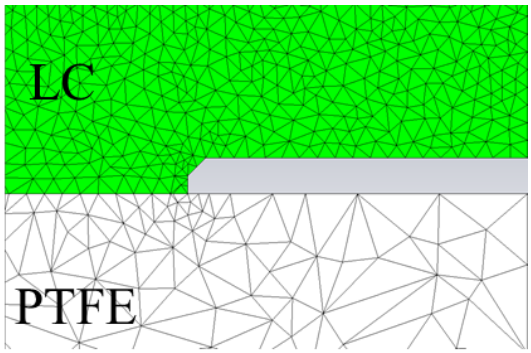
(a) Local Mesh Size < $\frac{\lambda_{guided}}{20}$



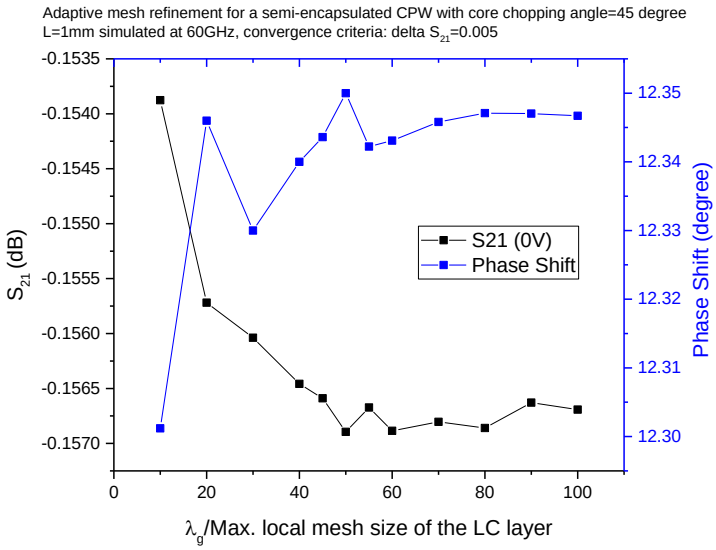
(b) Local Mesh Size < $\frac{\lambda_{guided}}{40}$



(c) Local Mesh Size < $\frac{\lambda_{guided}}{60}$



(d) Local Mesh Size < $\frac{\lambda_{\mathrm{guided}}}{80}$



(e) Sensitivity of the Insertion Loss and Phase Shift to the Local Mesh Refinement Ratio

Fig.37 Local Mesh-refinement Study into the Dielectrics Enclosing the ECPW's Core Line

Simulated results in the above Fig.37(e) indicate that both *S*-parameters and the derived differential phase shift (ϕ) are converged with the increase of mesh refinement ratio to 1/60 of a guided wavelength, where the maximum deviation ΔS_{21} is controlled within the targeted 0.0002 dB/mm, and the maximum $\Delta\phi$ falls below 7×10^{-5} °/mm.

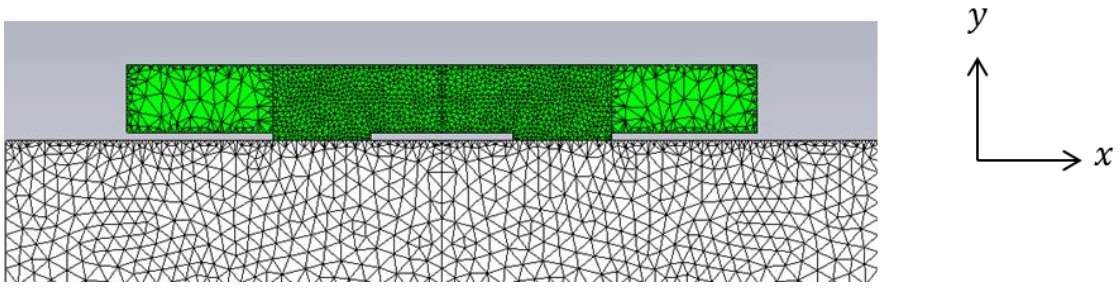
3.2.3 Adaptive Meshing inside Metals

By default, computational electromagnetic software (HFSS and CST) take the representation of conductors as surface impedance Z_s (eq.10).

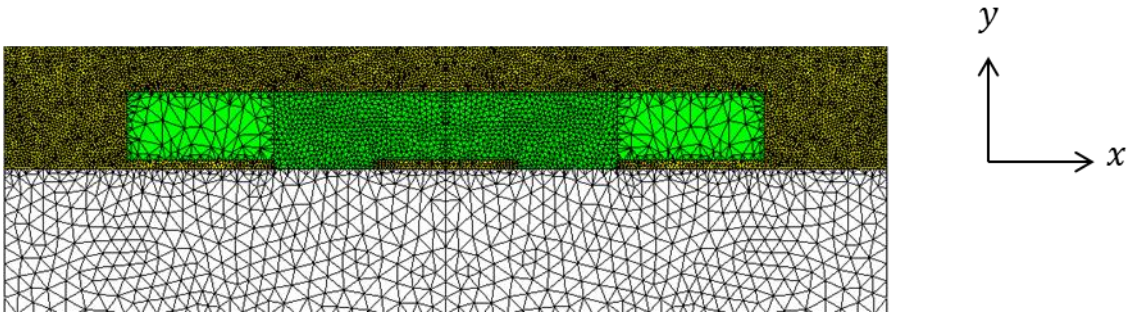
$$Z_s = \frac{e^{kt} + \frac{\sigma z_c - k}{\sigma z_c + k} e^{-kt}}{e^{kt} - \frac{\sigma z_c - k}{\sigma z_c + k} e^{-kt}} \times \frac{k}{\sigma} \quad \text{.....(10)}$$

where $k = \frac{1+j}{\delta}$, and $z_c = \sqrt{\frac{\mu_0}{\varepsilon_0}}$ represents the characteristic impedance of the free space (377Ω in vacuum). This applies when conductor thickness t >> penetration depth δ. Meshing and computing the fields are only performed at the conductor surface and in the space outside the conductors. The space inside conductors is not meshed. The effects of the internal fields are considered by the surface impedance model, given that the internal fields fall exponentially with the distance from the surface.

We firstly perform 60GHz simulations for our ECPW structure with a half-ounce Cu clad (T_{Cu}=17μm >> δ_{Cu}) laminated on the PCB substrate, with gold plating not considered first. A comparative study is conducted for the following two methods. Method 1 is not meshing inside metals, but based on HFSS's default surface impedance model, as shown below in Fig.38 (a). Method 2 is meshing inside metals, i.e. solving the internal field of the metals, as shown below in Fig.38 (b).



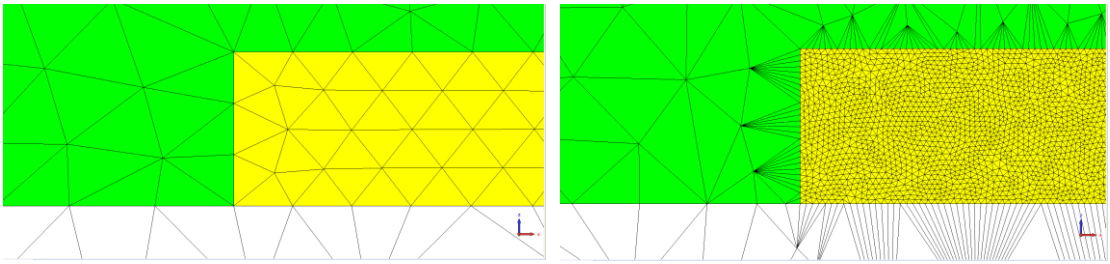
(a) Meshing based on HFSS's Default Surface Impedance Model (not Meshing inside Metals)



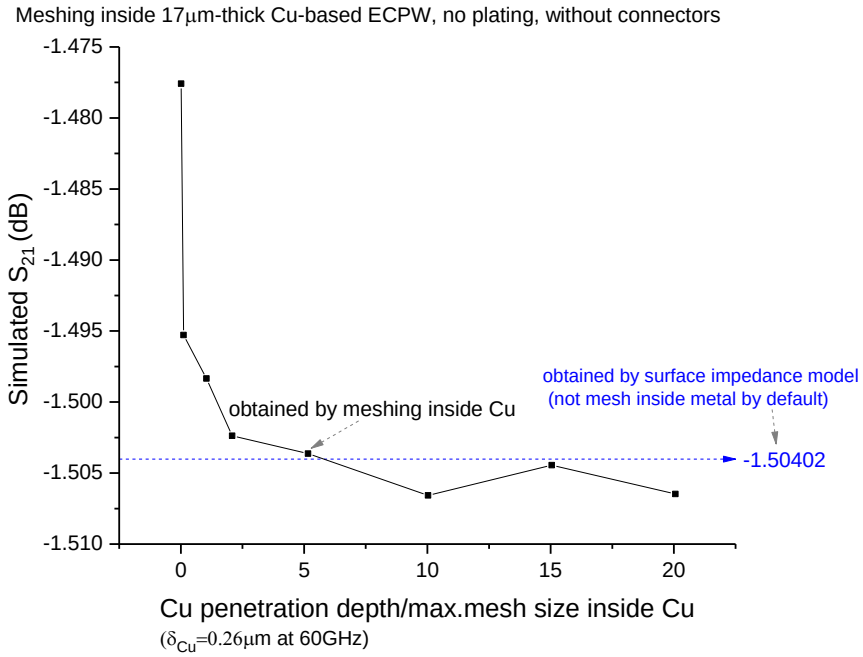
(b) Meshing inside Metals

Fig.38 Cross-section Mesh View of (a) Surface Impedance Model vs. (b) Meshing inside Metals

Note that for the simulation of meshing inside metals, we use a *y*-*z* plane symmetry to alleviate the computation burden. We refine the volume and surface meshes where the field gradient is high, until the convergence criteria $\left|S_{21_{i+1}} - S_{21_i}\right|$<0.005dB is met. The local mesh in the LC volume and the metal surface is based on the maximum mesh size < 1/60th of a guided wavelength as derived above in section 3.2.2. For our Cu-based ECPW design without gold-plating at 60GHz, guided λ=2.4mm, δ_{Cu} =0.26μm, T_{Cu} / δ_{Cu} =63. Convergence of the adaptive-meshing refinement inside the core line's metal is shown in Fig.39 (b) below (starting to converge when the refinement ratio >5).



(a) Different Refinement Ratios (δ_{Cu}/Max. Mesh Size inside the Cu Core)



(b) Convergence of Insertion Loss vs. the Mesh Refinement Ratio

Fig.39 Adaptive Meshing inside Cu with Thickness >> Penetration Depth δ_{Cu} at 60GHz

Benchmarking the two methods as shown above in Fig.39 (b), it is numerically verified that S_{21} given by HFSS's surface impedance model (not meshing inside metals) agrees with that by meshing inside conductors given the conductor's thickness is well above the penetration depth.

However, it is not the case when we do gold-plating on the circuit patterns. For the same LC-based ECPW geometry as above, we simulate gold-plated Cu with gold thickness changing from 0 to 4μm (i.e. from 0 to 16 times of δ_{Au} at 60GHz) and compare the S_{21} given by the default surface impedance meshing method versus that by meshing inside conductors. Finally, we derive a threshold of the gold-plating thickness that the surface impedance model is valid. The gold-plating simulation results are presented later in section 4.4.2.

3.3 LC's Material Tunability with the Enclosed CPW Structure

We explore the use of liquid crystals as tunable media for tunable millimetre-wave components. Specifically, we propose the enclosed coplanar waveguide (ECPW) for 60GHz signal and aim to investigate how to optimally combine the structure with liquid crystals as tunable dielectrics for a phase-shifting device.

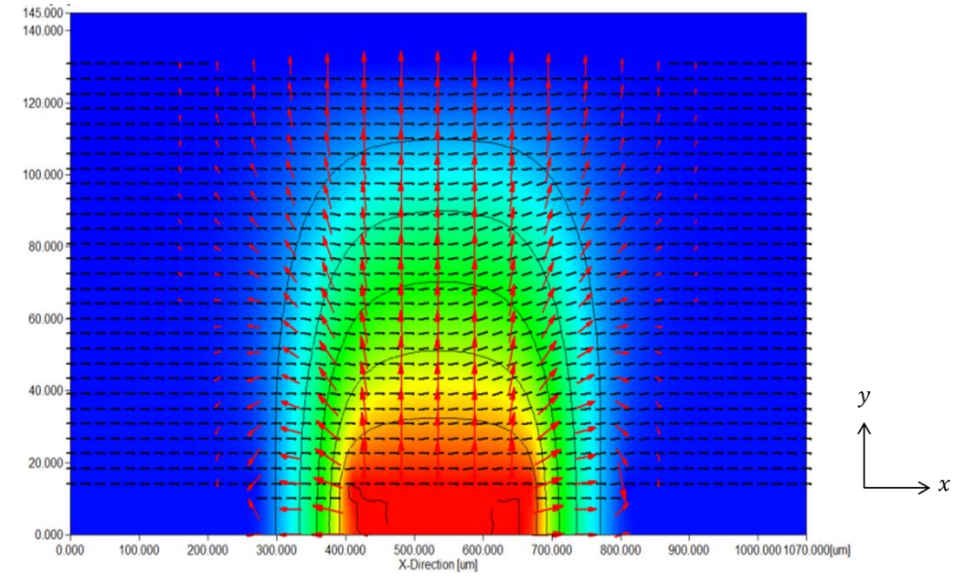
Based on the nature of TEM mode (zero cutoff frequency), the millimetre-wave electric vector field is identical in the polarisation with that at low frequencies. From the theory of dielectrics at low frequencies and the millimetre-wave frequencies, we notice that the highly inhomogeneous millimetre-wave electric field intensity distribution affects the electric flux and hence the wave-occupied-volume ratio of the dielectric in a specific region k ($WoVR_k$).

3.3.1 Surface-anchoring Alignment Direction for the Maximum Tunabiltiy

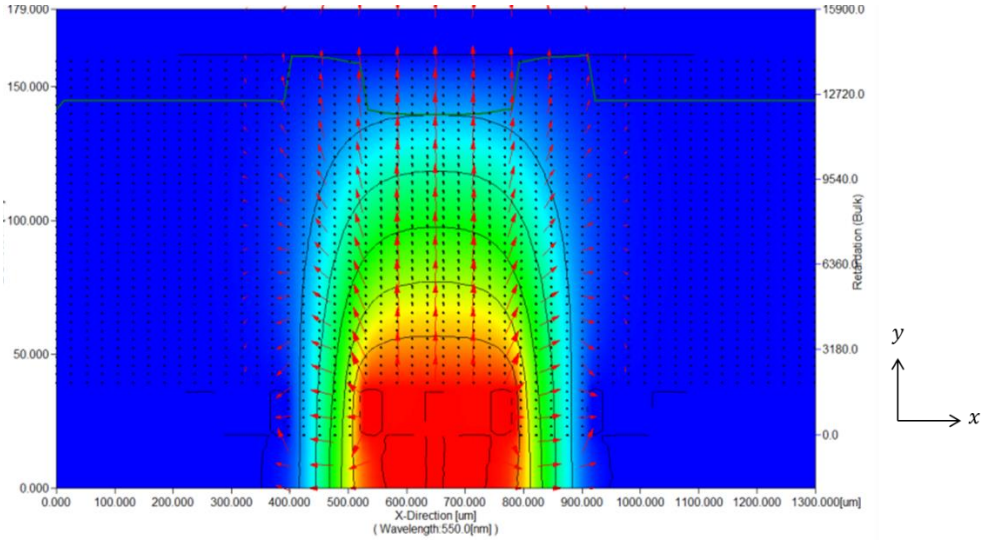
Recalling from Chapter 2.1 that the maximum differential phase shift ($\Delta\Phi_{21}$) is given by eq.11 below for a tunable transmission line with a length of *L*.

$$\Delta\Phi_{21}=\frac{2\pi fL}{c_0}\times(\sqrt{\varepsilon_{eff\ (max.bias)}}-\sqrt{\varepsilon_{eff\ (ref.bias)}}) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(11)$$

where $\varepsilon_{eff\ (max.bias)}$ and $\varepsilon_{eff\ (ref.bias)}$ denote ε_{eff} in the saturation and reference voltage-biasing states, respectively. For a maximum achievable $\Delta\Phi_{21}$, the reference bias is chosen as the voltage below Fredericks transition (e.g. <4V) and with a longitudinal LC alignment by surface-anchoring the LC directors parallel with the wave-propagation direction (*z*-axis as shown in Fig.40 (b) below). The reason behind that is explained in the next section 3.3.2 for details. Fig.40 below illustrates the LC directors' orientation (produced using LCD Master) and the implications on $\varepsilon_{eff\ (ref.bias)}$ under two rubbing (surface-anchoring) directions for the alignment layer. The red arrows indicate the electric field direction, whilst the background colours represent the electric field intensity distribution.



(a) Transversal Surface-Anchoring (Alignment along *x*-axis): $\varepsilon_{eff\ (ref.bias)} > \varepsilon_{eff,\perp}$



(b) Longitudinal Surface-Anchoring (Alignment along *z*-axis): $\varepsilon_{eff\ (ref.bias)} = \varepsilon_{eff,\perp}$

Fig.40 Effect of Surface-Anchoring Direction on $\varepsilon_{eff\ (ref.bias)}$ below Fredericks transition

3.3.2 A Partitioning Model for Local Polarisation and Tunability Analysis

For a clear illustration of the difference in the LC material's maximum tunability with this ECPW structure by different surface anchoring directions, we develop a 4-region partitioning model as shown in Fig.41 below. The following Table 5 summarises the local dielectric anisotropic and inhomogeneous properties under the two alignment directions shown above (Fig.40).

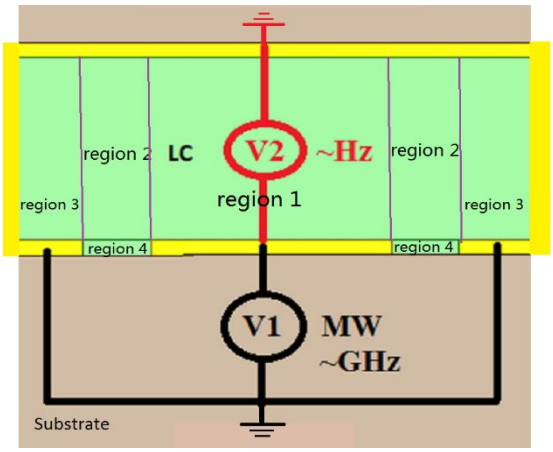


Fig.41 A 4-Region Model to Simplify Tunability Analysis

Table.5 ECPW's Local Dielectric Constant and Polarisation Analysis

Region Number (Refer to Fig.41 above)	Transversal Alignment		Longitudinal Alignment (Preferable)	
	Ref. bias	Sat. bias	Ref. bias	Sat. bias
1 (above core line, strong *E*)	$\varepsilon_{LC,\perp}$	$\varepsilon_{LC,\parallel}$	$\varepsilon_{LC,\perp}$	$\varepsilon_{LC,\parallel}$
2 (above two slots, weak *E*)	$\varepsilon_{LC,\perp}<\varepsilon_{eff}<\varepsilon_{LC,\parallel}$	$\approx \varepsilon_{LC,\parallel}$	$\varepsilon_{LC,\perp}$	$\approx \varepsilon_{LC,\parallel}$
3 (low E, and un-switched)	$\varepsilon_{LC,\perp}$	$\varepsilon_{LC,\perp}$	$\varepsilon_{LC,\perp}$	$\varepsilon_{LC,\perp}$
4 (two slots, strong *E*)	$\varepsilon_{LC,\parallel}$	$\varepsilon_{LC,\parallel}$ (un-switched)	$\varepsilon_{LC,\perp}$	$\varepsilon_{LC,\parallel}$ (in-plane switched)
Macroscopic ε_{eff}	$\approx \varepsilon_{eff,\ LC\ ave}$	$\approx \varepsilon_{eff,\ LC\parallel}$	$\varepsilon_{eff,\ LC\perp}$	$\approx \varepsilon_{eff,\ LC\parallel}$
Max. Tuning range ratio *(TRR)* defined in section 4.2.1	$\frac{\sqrt{\varepsilon_{eff,\ LC\parallel}}-\sqrt{\varepsilon_{eff,\ LC\ ave}}}{\sqrt{\varepsilon_{LC\ (sat.bias)}}-\sqrt{\varepsilon_{LC\ (ref.bias)}}}$		$\frac{\sqrt{\varepsilon_{eff,\ LC\parallel}}-\sqrt{\varepsilon_{eff,\ LC\perp}}}{\sqrt{\varepsilon_{LC\ (sat.bias)}}-\sqrt{\varepsilon_{LC\ (ref.bias)}}}$	
Conclusion	*TRR* (Transversal Alignment) < *TRR* (Longitudinal Alignment)			

Note: $\varepsilon_{eff,\ LC\ ave}$ denotes the structure's effective dielectric constant with LC at the averaged ordering state. Ref. bias is the bias voltage below the Fredericks transition. Sat. bias denotes the saturation bias.

Given the transversal surface alignment, region 4 is non-tunable and region 2 exhibits low tunability as well. The overall tuning range could be significantly smaller than that of longitudinal surface alignment. Furthermore, this alignment is prone to defects and uncertainty when rubbing the discontinuous conductors' edges and gaps.

Given a longitudinal surface alignment and under the reference bias state (below Fredericks threshold), the millimetre-wave electric field's polarisations are perpendicular to the LC's

orientations at all regions. Therefore, taking $\varepsilon_{eff} = \varepsilon_{LC,\perp}$ is rigorous. This surface-anchoring direction can also avoid alignment-related defects such as disclination lines. More importantly, the achievable maximum tuning range is the largest as compared with any other surface-anchoring directions. Therefore, we only focus our design on the longitudinal surface anchoring.

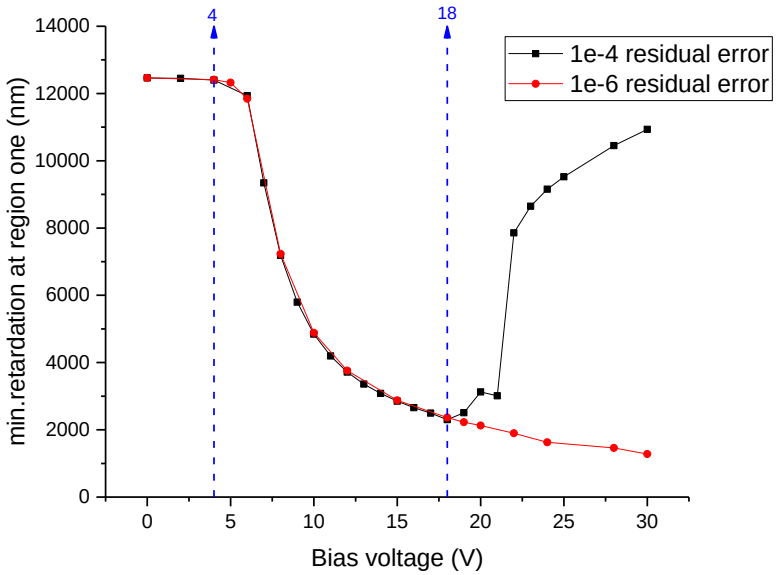
It is worth noting from the above table that, the region 2 is regarded as a fringing-field region (both low frequencies and millimetre wave), in which the field intensity (both low frequencies and millimetre wave) is much weaker than that of regions 1 and 4. Under a saturation-biased state, although LC molecules in region 2 do not switch by 90° (from the reference bias state), however, the local LC orientations (almost parallel with low frequency field) at this region are also nearly parallel with millimetre-wave electric field polarisations, as there is minor difference between electric polarisations at different frequencies for a TEM wave (although the magnitude distribution will be significantly different due to the skin and proximity effects at millimetre wave frequencies). Thereby, we could envision that taking local effective dielectric constant $\approx \varepsilon_{LC,\parallel}$ for region 2 will not overestimate the tuning range significantly.

However, for intermediate biasing voltage states (beyond the Fredericks threshold but before saturation), the 4-region dielectrics model struggles to provide a macroscopic ε_{eff} accurately. Looking into the ECPW's cross-sectional (*x*-*y* plane) electrodes' configuration, $\varepsilon_{LC}(x, y)$ and $tan\delta_{LC}(x, y)$ are inhomogeneous. To gain an accurate knowledge of the low-frequency biasing voltage dependence of the $tan\delta_{LC}$ (60GHz) and ε_{LC} (60GHz) distributions, we numerically simulate the LC molecular orientations (biasing voltage dependent) using LCD Master (section 3.3.3 below), the results of which are subsequently fed into HFSS (Chapter 4) for millimetre-wave electromagnetic simulations.

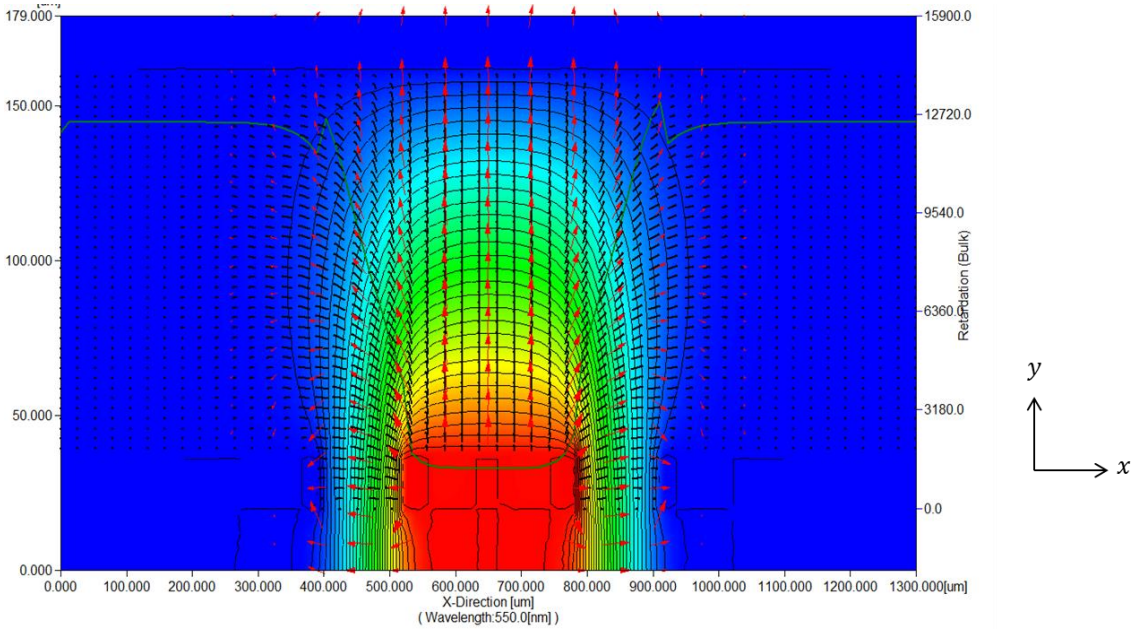
3.3.3 LC Director Calculations based on Finite Element Simulations

LCD Master (Shintech) is used to perform low-frequency calculations (numerically solving Poission's Equations) to gain the bias voltage-dependent LC molecular orientations and consequently the spatial (local) LC dielectric constant, which is subsequently fed into electromagnetic simulators for 60GHz full-wave analysis. Longitudinal rubbing (along the *z*-axis) with a pretilt angle of 3° and anti-parallel assembling is assumed. As shown in Fig.42 (a),

the convergence of the director simulation is reached when refining the residual error criteria to be 10^{-6} for the saturation biasing states (above 18V).



(a) Convergence of the LC Directors Simulation by Finite Element Method



(b) LC Directors Distribution at 20V (Saturation Bias) and the 60GHz Field Polarisations

Fig.42 LCD Master 3D Simulations of the LC-based ECPW Structure

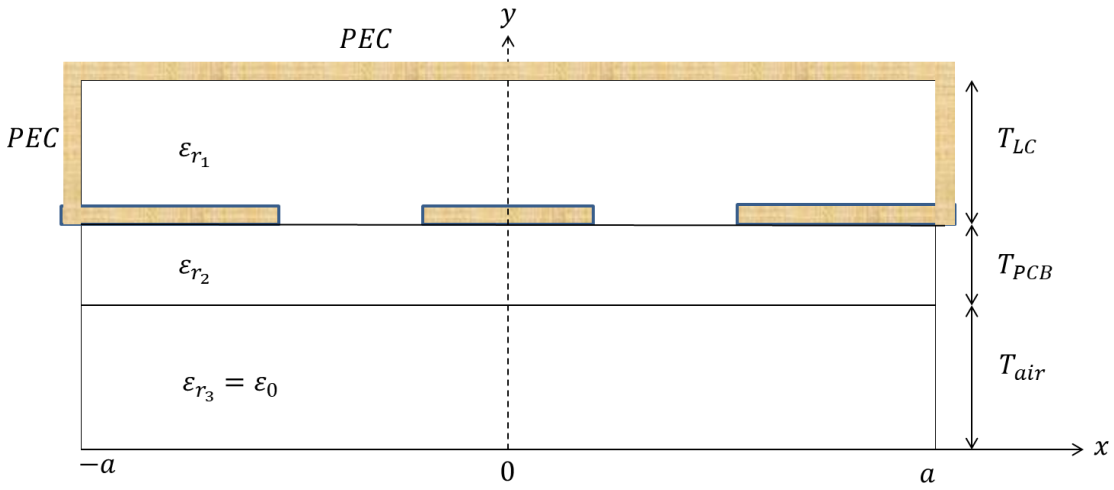
Benchmarking the simulation results from the LCD master shown in Fig.42 (b) and from the proposed analytical model stated in section 3.3.2, we confirm that the 4-region dielectrics model is quasi-rigorous for the reference bias and the saturation bias states assuming a longitudinal surface-anchoring. The model can be used as a fast-design guideline that provides local dielectric constants of the medium to be fed into the millimetre-wave simulator. For conservative reasons and depending on initial experiment results, we introduce a +10% of line length allowance to meet the targeted phase shift of π.

3.4 Theoretical Modelling and Full-wave Simulation of Enclosed CPW (ECPW) at 60GHz

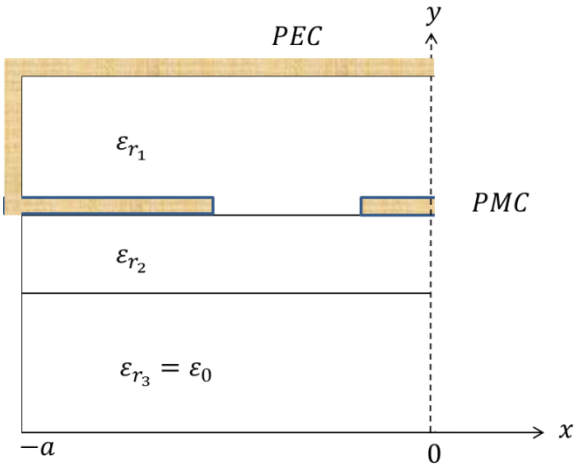
To lay a firm foundation for subsequent structure design and optimisation (Chapters 4 and 5), we conduct a theoretical analysis of the proposed enclosed coplanar waveguide (ECPW).

3.4.1 Analytical Model of the ECPW Structure

A simplified analytical model is built below in Fig.43 (a), assuming 60GHz time-harmonic electromagnetic fields in a linear, homogeneous and isotropic medium, with ε_{r_1}, ε_{r_2} and ε_{r_3} denoting the relative dielectric constant of the cavity, substrate and air, respectively. Note that the ε_{r_1} here as a macroscopic representation is for brevity reasons. More accurately, ε_{r_1} equals ε_0 prior to LC-filling (i.e. air-filled), while it exhibits nonlinear, nonhomogeneous and anisotropic behaviour after filling LC as a tunable dielectric medium. Conductors of the structure are assumed as Perfect Electrical Conductor (PEC), indicating no electric field inside the conductors, and only a normal component of the electric field is present at the surface boundary (no tangential component). Specifically, for our ECPW structure, Perfect Magnetic Conductor (PMC) assumption can be imposed to simplify the analytic model into solving half of the problem space based on the half-plane symmetry as Fig.43 (b) below.



(a) Enclosed CPW (ECPW) Model (Linear, Homogeneous and Isotropic Medium)



(b) Simplified Enclosed CPW (ECPW) model based on Half-plane Symmetry

Fig.43 A Simplified Theoretical Model of the Proposed ECPW Structure

The derived Helmholtz Equations based on the phasor form of Maxwell equations, wave equations and the constitutive relations are detailed in Appendix C. Full-wave electromagnetic simulators are introduced to assist numerically solving the equation sets as derived.

In response to the upper frequency limit of the single-mode operation as we mentioned in section 2.6.3, the cut-off frequency of the problematic higher-order modes that satisfy Maxwell's equations are estimated based on the theoretical model. The normalized phase constant $\frac{\beta_g}{\beta_0}$ is obtained in Fig.44 below, where the phase constant $\beta_g = \frac{2\pi}{\lambda_g} = \frac{2\pi f}{c}\sqrt{\varepsilon_{eff}}$.

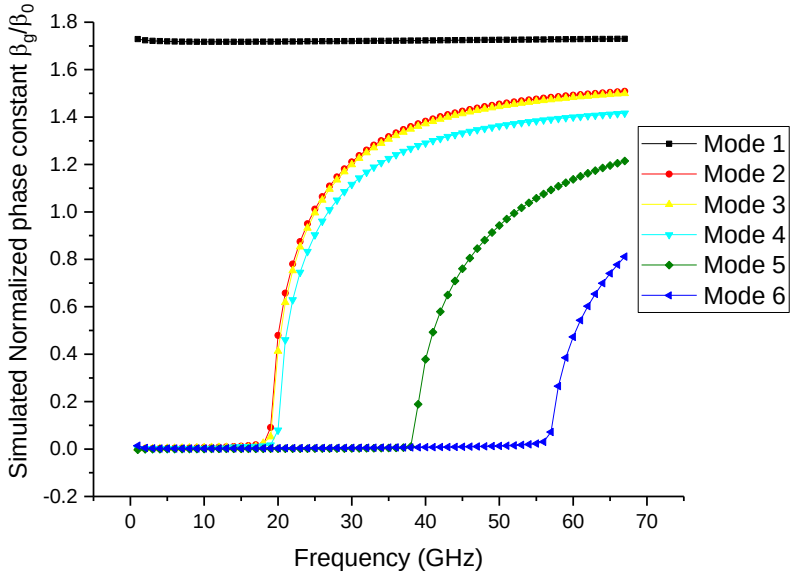


Fig.44 Dispersion of a LC-based ECPW with Cavity Width=5.2mm≫ $\frac{\lambda_{guided}}{2}$ (6 Modes Exicited)

The insertion loss of a phase shifter is due to a combination of conductor loss, dielectric loss, impedance-mismatching loss (return loss), and radiation loss. Peak phasor forms of different material absorption loss components are derived as follows (section 3.4.2 and 3.4.3).

3.4.2 Calculation of Conductor Loss

For a wave (time-harmonic) propagating in a lossy medium, according to the phasor form of Maxwell 4th equation, we have eqs.12, 13 and 14.

$\nabla \times \overrightarrow{H_s} = \overrightarrow{J_{c_s}} + \overrightarrow{J_{d_s}}$=total $\overrightarrow{J_{vol_s}} = (\sigma + jw\varepsilon)\overrightarrow{E_s}$=$[\sigma + jw(\varepsilon' - j\varepsilon'')]\overrightarrow{E_s} = (\sigma + w\varepsilon'' + jw\varepsilon')\overrightarrow{E_s}$

$= jw[\varepsilon' - j\frac{(\sigma + w\varepsilon'')}{w}]$, …….. (12)

and loss tangent is defined as $tan\delta = \frac{(\sigma + w\varepsilon'')}{w\varepsilon'}$, ……(13)

the time-averaged conductor loss is given by $P_{metal_{ave}} = \frac{1}{T}\int_0^T P_{metal_{ins}} dt$ …...(14)

For our analysis without loss of generality for any frequency, all the *E*, *D*, *H*, *B*, *J* and ρ below are in the peak phasor form, e.g. $\overrightarrow{E_s(x,y,z)} = \overrightarrow{E_s(x,y)_0} e^{-\gamma z}$ where $E_s(x,y)_0 = \left|\overrightarrow{E_s(x,y)_0}\right|$ is the peak phasor quantity, i.e. at *t=0* or *z=0*.

The peak phasor form of the conductor loss at core line top surface (per unit length) is given by

$P_{metal_{s_0}} = I_{s_0}{}^2 R = [\int_{x=0}^{w_{strip}} \int_{y=-\delta}^{0} \sigma E_s(x,y)_0 dS]^2 \times \frac{1}{\sigma\delta w_{strip}} =$

$[\int_{x=0}^{w_{strip}} \int_{y=-\delta}^{0} \sigma E_s(x,y)_0 dS]^2 \times \frac{\sqrt{\pi f\sigma\mu}}{\sigma w_{strip}}$ ……(15)

Using surface current density, peak phasor form of the total core line metal loss (thickness T_{strip} considered) per unit length is given by eq.16 or eq.17.

$P_{core_{s_0}}$=$[\int_{x=0}^{w_{strip}} \sigma E_s(x, y=0)_0 dl + \int_{x=0}^{w_{strip}} \sigma E_s(x, y=-T_{strip})_0 dl]^2 \times \frac{\sqrt{\pi f\sigma\mu}}{\sigma w_{strip}}$

$+2[\int_{y=-T_{strip}}^{0} \sigma E_s(x=0,\ y)_0 dl]^2 \times \frac{\sqrt{\pi f\sigma\mu}}{\sigma T_{strip}}$ ……(16)

or $P_{core_{s_0}} = [\int_{x=0}^{w_{strip}} H_s(x, y=0)_0 dl + \int_{x=0}^{w_{strip}} H_s(x, y=-T_{strip})_0 dl]^2 \times \frac{\sqrt{\pi f \sigma \mu}}{\sigma w_{strip}} +$

$2[\int_{y=-T_{strip}}^{0} H_s(x=0,\ y)_0 dl]^2 \times \frac{\sqrt{\pi f \sigma \mu}}{\sigma T_{strip}}$. ……..(17)

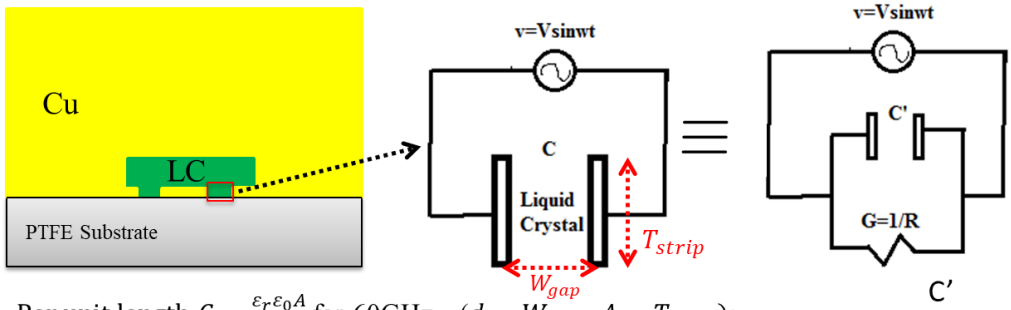
The peak phasor form of conductor loss of grounds can be given in the similar way. Due to the proximity effect, $E_s(x = 0\ and\ w_{strip})_0 > E_s(0 < x < w_{strip})_0$ and $E_s(x, y=0)_0 > E_s(x, y=-t)_0$ for most of the *x* values.

3.4.3 Calculation of Dielectric Loss

As shown in Fig.45 below, we theoretically derive the loss dissipated in the volume of LC dielectrics based on a parallel capacitor model filled with lossy dielectrics. Here the dimension of the LC cell is limited to far less than half a guided wavelength, so that a TEM-nature is assumed (i.e. without higher-order waveguide modes) and the quasi-static approach based on circuit theory can be used.

Deriving LC volume loss at one ECPW slot as an example:

Assumptions: Slot's cross section dimensions $\ll \frac{1}{2}\lambda$ →LC layer modelled as parallel plate capacitor with lossy dielectric:



Per unit length $C = \frac{\varepsilon_r \varepsilon_0 A}{d}$ for 60GHz, $(d = W_{gap},\ A = T_{strip})$:

$Z = \frac{1}{jwC} = \frac{d}{jw\varepsilon_r\varepsilon_0 A}$, $\xrightarrow{Y=1/Z}$ admittance $Y = \frac{jw\varepsilon_r\varepsilon_0 A}{d} = \frac{jw\varepsilon_0(\varepsilon_r' - j\varepsilon_r'')A}{d} = \frac{jw\,\varepsilon_0\varepsilon_r' A}{d} + \frac{w\varepsilon_0\varepsilon_r'' A}{d}$

Admittance is equivalent to a parallel combination of an ideal lossless capacitor C′ with ε_r', and a resistance of *1/G* or conductance $G = wC'tan\delta$.

$P_{input} = YV^2 = jwC'V^2 + GV^2$. (Note: P_{input} and *V* are for 60GHz signal)

Dielectric Volume Loss in liquid crystal

60GHz field intensity

$= GV^2 = \frac{w\varepsilon_0\varepsilon_r'' AV^2}{d} = \frac{2\pi f\,\varepsilon_0\varepsilon_r'' V^2 T_{strip} L}{W_{gap}} = 2\pi f\,\varepsilon_0\varepsilon_r''\, V^2 L * AR = 2\pi f\,\varepsilon_0\varepsilon_r'' \left(\frac{V}{W_{gap}}\right)^2 T_{strip} W_{gap} L$

Liquid Crystal Volume

where ε_r'' is driving voltage dependent (not 60GHz field dependent),

Aspect Ratio $AR = \frac{T_{strip}}{W_{gap}}$

Fig.45 LC Dielectric Loss Model Derived by Quasi-static Approach (Circuit Theory)

Alternatively, the dielectric loss can also be derived from current density model, i.e.

$$\overrightarrow{J_{vol}} = (\sigma + jw\varepsilon_0\varepsilon_r'')\vec{E} \quad \text{.....(18)}$$

$$P_{LC} = \frac{1}{G} = \frac{d}{w\varepsilon_0\varepsilon_r'' A_1} \quad I = \int \overrightarrow{J_{vol}} \cdot d\vec{S} \quad \text{.....(19)}$$

Combining eqs.18 and 19, we have eq.20 that is identical to the lossy capacitor model we have derived above.

$$P_{LC} = (J_{vol} \cdot A)^2 \cdot \frac{d}{w\varepsilon_0\varepsilon_r'' A} = \frac{w^2\varepsilon_0{}^2\varepsilon_r''^2 E^2 A^2 d}{w\varepsilon_0\varepsilon_r'' A} = w\varepsilon_0\varepsilon_r'' A d E^2 = 2\pi f\varepsilon_0\varepsilon_r'' \cdot E^2 \cdot volume \quad \text{.....(20)}$$

$$tan\delta = \frac{\varepsilon_r''}{\varepsilon_r'} = \frac{\sigma}{2\pi f\varepsilon_0\varepsilon_r'} \quad \text{.....(21)}$$

where σ is total effective conductivity caused by ionic conduction and displacement current.

The instantaneous LC volumetric loss $P_{LC_{ins}}$ is given as eq.22 below.

$$P_{LC_{ins}} = 2\pi f\varepsilon_0 \int_{x=0}^{w'} \int_{y=0}^{h} \int_0^L \varepsilon_r'(bias, x, y, z) tan\delta(bias, x, y, z) \left|\overrightarrow{E(x, y, z)}\right|^2 dV \quad \text{..... (22)}$$

where tensor $\varepsilon_r' tan\delta$ depends on bias voltage, and vector $\overrightarrow{E(x, y, z)}$ also depends on $\varepsilon_r'(bias)$. For the longitudinal surface alignment, $\varepsilon_r' tan\delta$ is homogeneous (i.e. a constant) at reference biasing state below the Fredericks threshold, thus this term can be taken out of the integral, and the instantaneous LC volumetric loss is given by

$$P_{LC_{ins}} = 2\pi f\varepsilon_0\varepsilon_r' tan\delta \int_{x=0}^{w'} \int_{y=0}^{h} \int_{z=0}^{L} \left|\overrightarrow{E(x, y, z)}\right|^2 dV \quad \text{..... (23)}$$

The time-averaged power loss in LC is hence given by $P_{LC_{ave}} = \frac{1}{T} \int_0^T P_{LC_{ins}} dt$ ..... (24)

Power absorbed per unit volume at any instant time is expressed in eq.25, based on the assumption that power is uniformly distributed throughout the volume and thermal equilibrium has been achieved.

$$P = \sigma|E|^2 = 2\pi f\varepsilon_0\varepsilon_r' tan\delta|E|^2 \quad \text{.....(25)}$$

For our analysis, the peak phasor form of LC volumetric loss per unit length at reference biasing state (below the Fredericks threshold) is given by:

$P_{LC_{s_0}} = 2\pi f\varepsilon_0\varepsilon_r' tan\delta \int_{x=0}^{w'} \int_{y=0}^{T_{LC}} \left|\overrightarrow{E_s(x, y)_0}\right|^2 dxdy$, where $\overrightarrow{E_s(x, y, z)} = \overrightarrow{E_s(x, y)_0} e^{-\gamma z}$ ... (26)

As charges are not uniformly distributed, *E* is not a constant everywhere (i.e. non-uniform) due to skin effect and proximity effect, which is significantly different from that at electrostatics. 3D full-wave simulations are thereby performed to numerically quantify these.

3.4.4 Optimisation in Stages

The aim of optimisation is to produce circuit element values that result in the desired target performance. The optimisation target in this study is S_{21} maximisation whilst satisfying 0-π phase-shifting functionality. The optimisation opportunity is based on the nonlinear relationship between dielectric loss, phase shift and electric field intensity.

Optimisation begins with the simplest circuit and smallest number of variables, i.e. the tunable ECPW transmission line part without connectors. We optimise in stages, i.e. firstly, the guiding conductor configuration and cavity dimension which defines the optimisation's boundary condition, then the geometrical aspect ratio and LC thickness T_{LC} for highest figure-of-merit, followed by electrodes shaping for further decrease of insertion loss. Finally, a complete device optimisation including connectors and matching networks is conducted over a certain bandwidth.

As a wide bandwidth response is desirable, we choose a few frequency points to begin investigations, such as the lower (54GHz), the centre (60GHz) and the upper (67GHz) frequency points, to reduce the computation burden needed for initial optimisation. Frequency points are added gradually as the response approaches the criteria set by the performance specification. It is not possible to achieve reflection-free for all frequencies. The bandwidth in our application is specified as the maximum frequency range that can be tolerated for which the insertion loss stays below -4.5dB and return loss below -15dB.

Chapter 4. Tunable Part Design: Tailoring Spatial Volume and Distribution of Millimetre-wave Signal Occupying Tunable versus Non-tunable Dielectrics

4.1 Impedance-Matching Scheme Targeted for a Phased Array

The molecular orientation of LC is controllable by varying the low-frequency biasing voltage, the resulting polarisability's variability leads to dielectric constant's tunability, allowing a continuously-tunable phase-delaying function for antenna array-feeding. In different phase-delaying states between 0 and π, the characteristic impedance and reflection loss can change remarkably with the voltage applied. At the voltage-biasing state where the LC director field is perpendicular to millimetre-wave polarisation, the material absorption loss in LC is at a maximum ($tan\delta_{\perp}=0.0123 \gg tan\delta_{\parallel}=0.0032$ for GT3-24002 used in this work).

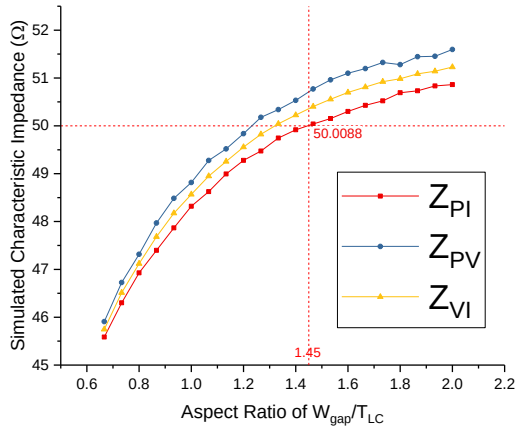
4.1.1 Novel Biasing-voltage Dependent Wideband Impedance-Matching

A particular novelty of this work is the development of a biasing-voltage dependent impedance-matching scenario to systematically reduce insertion loss. We strategically design the geometry to be of lowest reflection loss at the biasing state with maximal materials' absorption losses. Thereby, adding up absorption and reflection losses, the total insertion loss is minimised. Furthermore, this method minimises insertion loss variation with bias voltages during 0-π continuous phase tuning, thereby minimising the steering-beam distortion without the need for tunable amplifiers or attenuators. This hugely reduces the complexity of the system and mitigates noise level introduced by the amplitude-compensating networks.

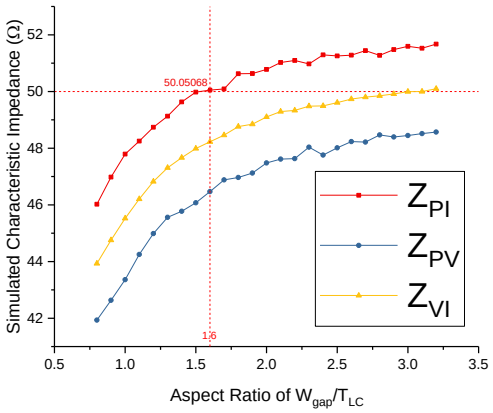
4.1.2 ECPW's Geometrical Aspect Ratios for 50Ω Controlled Impedance

For different PCB substrates (5880 and 3003) of different dielectric constants at 66GHz ($\varepsilon_{5880}=2.195, \varepsilon_{3003}$=2.993 as detailed in appendix), the aspect ratios of W_{strip}/T_{LC} and W_{gap}/T_{LC} for 50Ω are searched in Fig.46, where W_{strip} denotes the core line's width, W_{gap} is the width of the slots between the core and the coplanar grounds, T_{LC} is the distance between

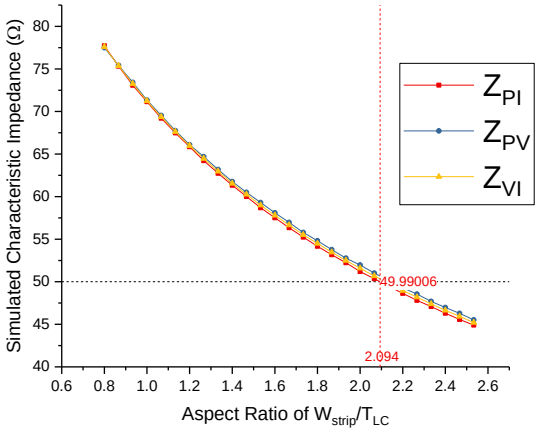
the core and the top enclosed ground. Note that the computation results of the characteristic impedance Z_0 is not unique at 66GHz, but is depending on the calculation methods. The Z_0^{PI} approach is used as voltages are not uniquely defined for our structure.



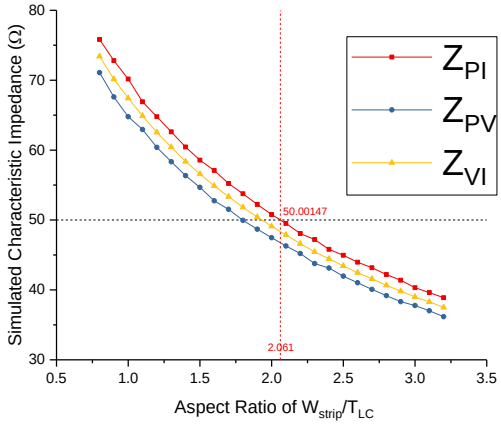
(a) RT/duroid 5880: $\frac{W_{gap}}{T_{LC}}$ = 1.45



(b) RO3003: $\frac{W_{gap}}{T_{LC}}$ = 1.6



(c) RT/duroid 5880: $\frac{W_{strip}}{T_{LC}}$ = 2.094



(d) RO3003: $\frac{W_{strip}}{T_{LC}}$ = 2.061

Fig.46 Simulated Aspect Ratios for a 50Ω LC-based ECPW Structure

Based on the aspect ratios derived for the 50Ω-matching, the optimal thickness of the liquid crystal is searched for by looking into the minimum insertion loss whilst satisfying the quest for a maximum phase shift of π.

4.2 Nonlinearities in Tuning Range and Insertion Loss

4.2.1 Definition of wave-occupied-volume ratio and tuning range ratio (*TRR*)

The impact of dielectric constant on the millimetre-wave propagating mode indicates that the electric flux tends to distribute in a region with a higher dielectric constant. Phase shift and insertion loss both closely connects with the dielectric constant ratio of tunable to non-tunable media, i.e. $\varepsilon_{LC}/\varepsilon_{PCB}$ in this study, as it determines spatial volume distribution of millimetre-wave electric flux in lossy but functional dielectrics (i.e. LC). A concept of wave-occupied-volume ratio (*WoVR*) is proposed in eq.27 below for analysing the effective dielectric constant (ε_{eff}) of the transmission line.

$\varepsilon_{eff} = \sum_{k=1}^{n} \varepsilon_k WoVR_k = \varepsilon_1 \times$ *flux ratio in region 1* $+ \varepsilon_2 \times$ *flux ratio in region 2* $+ \ldots + \varepsilon_k \times$ *flux ratio in region k,* ……...(27)

where $WoVR_k$ indicates the electric flux ratio in the region *k*, which depends on dielectric constant of the region (ε_k) and the conductors' geometry.

Combining eqs.11 and 27 in this study, increasing $\varepsilon_{LC}/\varepsilon_{PCB}$ results in an elevated $WoVR_{LC}$ and thus an improved $\Delta\Phi_{21}$. Without loss of generality for a variety of LC with different birefringence, we denote the maximum tuning range ratio (*TRR*) normalized to a specific type of LC in eq.28 below.

$$max.\ TRR = \frac{\sqrt{\varepsilon_{eff\ (max.bias)}} - \sqrt{\varepsilon_{eff\ (ref.bias)}}}{\sqrt{\varepsilon_{LC\ (max.bias)}} - \sqrt{\varepsilon_{LC\ (ref.bias)}}} \times 100\% \quad \ldots\ldots\ldots\ldots\ldots\ldots(28)$$

Note that the liquid crystal's dielectric constant range is limited around 2.4 to 3.3 at microwave and millimetre-wave frequencies, thus a change in the liquid crystal materials makes a limited difference to the wave-occupied-volume ratio, while the non-tunable PCB substrate can tip the balance as the ε_{PCB} ranges from 2.1 to 10.2 depending on material compositions (e.g. PTFE, ceramic, woven glass fiber). We firstly model an enclosed CPW (ECPW) with a fixed LC (ε_{LC}) and a fixed LC-layer thickness (T_{LC}), computing the maximum *TRR* parametrised with $\varepsilon_{LC}/\varepsilon_{PCB}$ for the following two cases, i.e. a fixed geometry (with varied impedance), and a fixed impedance (by a varied geometry), with the simulation results shown in section 4.2.2 below.

4.2.2 Fixed LC-layer Thickness: Compute *TRR* Parametrised with $\varepsilon_{LC}/\varepsilon_{PCB}$ for Fixed Geometry (Varied Impedance) vs. Fixed Impedance (Varied Geometry)

By 66GHz simulations, we obtain in Fig.47 that *TRR* drops with the decrease of $\varepsilon_{LC}/\varepsilon_{PCB}$ owing to the reduced $WoVR_{LC}$. However, there is a slump in *TRR* in the case of the 50Ω controlled-impedance requirement as compared with that in case of a fixed geometry, as illustrated in the area coloured blue where the fixed geometry exhibits an impedance lower than 50Ω.

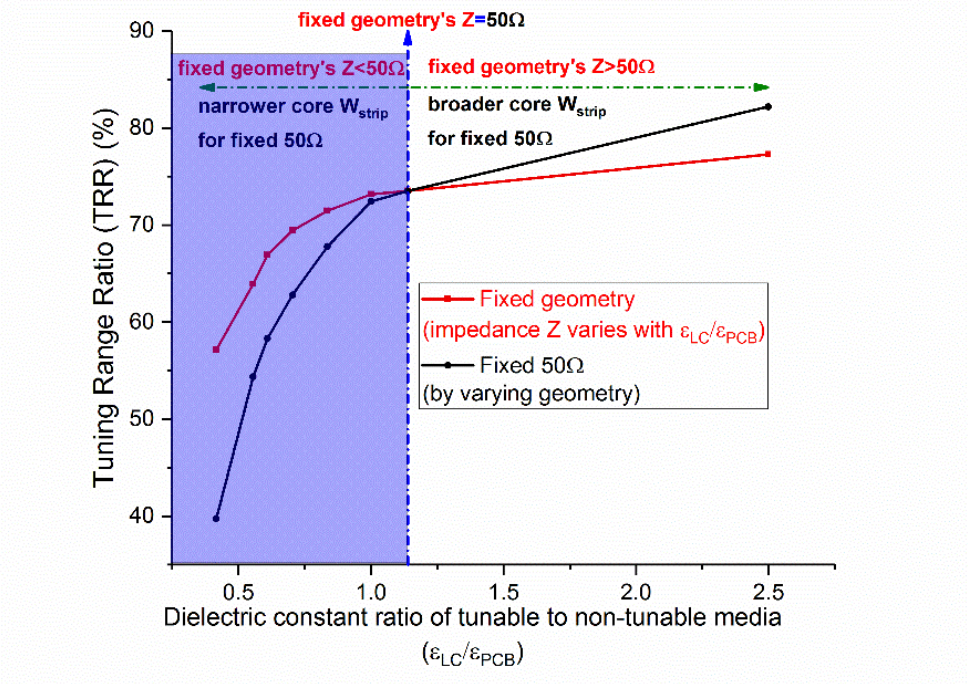
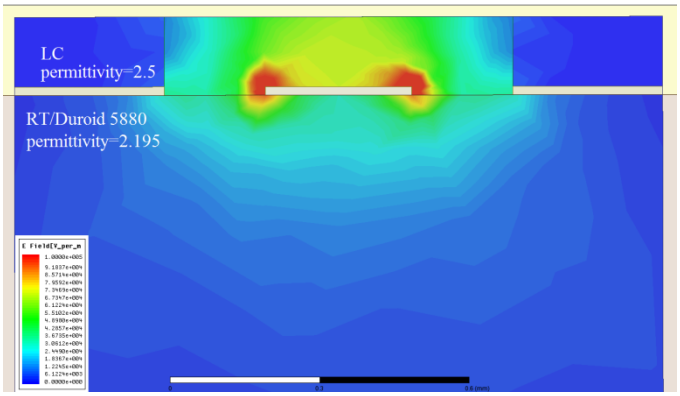
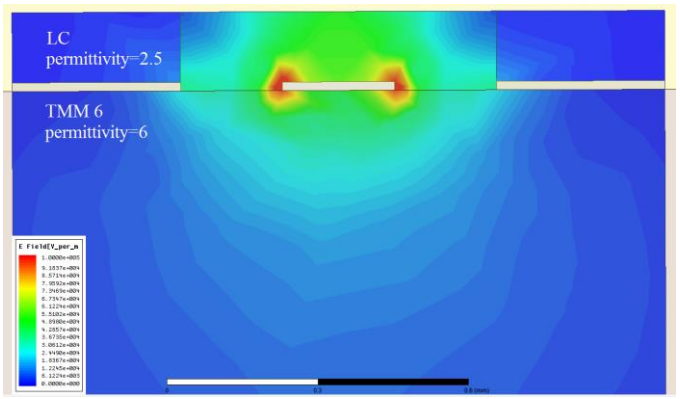


Fig.47 Simulated max. *TRR* of the LC-based ECPW: Fixed Geometry vs. Fixed 50Ω (66GHz)

The enhanced nonlinearity observed in the fixed-impedance case is attributed to the core-line's geometrical variations, i.e. to maintain 50Ω, the core-line's width W_{strip} narrows with the decrease of $\varepsilon_{LC}/\varepsilon_{PCB}$. By ways of illustration in Fig. 48 (a) and (b) below (with the same scale bar of the field intensity), the narrowing of the core reduces the $WoVR_{LC}$ further, which aggravates the nonlinearity as shown above in Fig.47, i.e. the *TRR* nonlinearity is a combined effect of the dielectric constant ratio ($\varepsilon_{LC}/\varepsilon_{PCB}$) and the geometry. Arguably, the maximum *TRR* characterises the geometrical coefficient of the tunable dielectrics, which positively correlates to the $WoVR_{LC}$.



(a) $\varepsilon_{LC}/\varepsilon_{PCB}$ =1.14, 50Ω (0V Bias), Power Input=1W at 66GHz



(b) $\varepsilon_{LC}/\varepsilon_{PCB}$ =0.42, 50Ω (0V Bias), Power Input=1W at 66GHz

Fig.48 Simulated 66GHz Electric Field Intensity in LC-based ECPW (0V Bias, Fixed 50Ω)

4.2.3 Optimising LC-layer Thickness by Balancing *TRR* and the Minimum Sum of Conductor and Dielectric Losses

Based on the aspect ratios derived for 50Ω impedance-matching, the optimal thickness of the liquid crystal is searched for by looking into the minimum insertion loss while satisfying the phase shift requirement of π. For a fixed geometry, the phase-tuning range and insertion loss both increase with the dielectric constant ratio of LC to PCB substrate ($\varepsilon_{LC}/\varepsilon_{PCB}$) as observed in the last section 4.2.2. However, such increase is nonlinear in case of a controlled impedance because of the geometrical variation's impact on the wave-occupied-volume ratio ($WoVR_{LC}$). The phase shift-to-loss optimisation is performed in recognition of this nonlinearity. According to our derivation in section 3.4.3, the peak phasor form of the LC volumetric loss per unit length at the 0V biasing state is given by eq.29.

$$P_{LC_{s_0}} = 2\pi f \varepsilon_0 \varepsilon_r' tan\delta_{LC} \int_{x=0}^{w'} \int_{y=0}^{T_{LC}} \left|\overrightarrow{E_s(x,y)_0}\right|^2 dxdy \quad \ldots\ldots\ldots\ldots\ldots\ldots(29)$$

Based on the surface current density, the peak phasor form of the total metal core loss (thickness T_{strip} considered) per unit length is given by eq.30.

$$P_{core_{s_0}} = {I_{s_0}}^2 R = \frac{\sqrt{\pi f \sigma \mu}}{\sigma w_{strip}} \left[\int_{x=0}^{w_{strip}} \sigma E_s(x, y=0)_0 dl + \int_{x=0}^{w_{strip}} \sigma E_s\left(x, y=-T_{strip}\right)_0 dl\right]^2$$

$$+2\frac{\sqrt{\pi f \sigma \mu}}{\sigma T_{strip}} \left[\int_{y=-T_{strip}}^{0} \sigma E_s(x=0, y)_0 dl\right]^2 \quad \text{.....(30)}$$

We quantify the insertion loss (dielectric loss plus metal loss) for the above parametric models. For the case of a fixed geometry and length *L*, it is assumed that the loss calculation is not normalised to any controlled impedance, and thus the S_{21} obtained in Fig.49 below is free of return loss, and only the materials' absorption losses (by dielectrics and metals) constitute the insertion loss. Note that at 66GHz the PCB substrate is less lossy than LC as $tan\delta_{PCB} \ll tan\delta_{LC}$, thus the decrease of $\varepsilon_{LC}/\varepsilon_{PCB}$ (i.e. a reduced $WoVR_{LC}$) results in a lower insertion loss (i.e. improved S_{21} as shown in Fig.49 below). However, for the case of a fixed-50Ω (reflection-free) and a fixed phase shift, the slump in *TRR* (as shown in the last section 4.2.2) requires an increased length *L* to compensate for a fixed phase-shifting requirement (e.g. π), and hence a dramatic drop in S_{21} is observed with the decrease of $\varepsilon_{LC}/\varepsilon_{PCB}$. The insertion loss nonlinearity presented here is a comprehensive effect of not only the dielectric constant ratio ($\varepsilon_{LC}/\varepsilon_{PCB}$) and the cross-sectional geometry, but also of the transmission-line length (*L*).

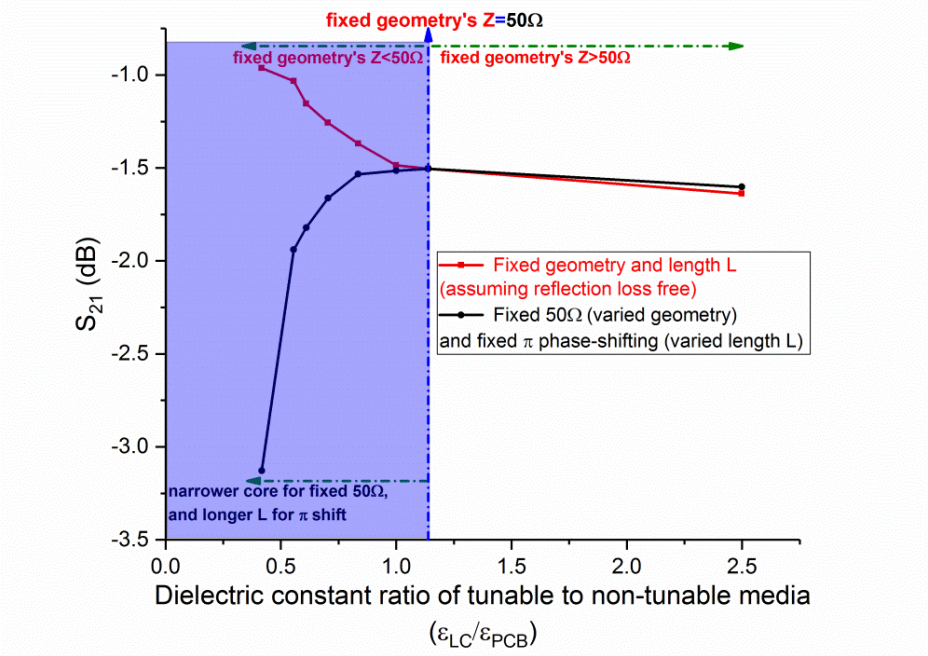
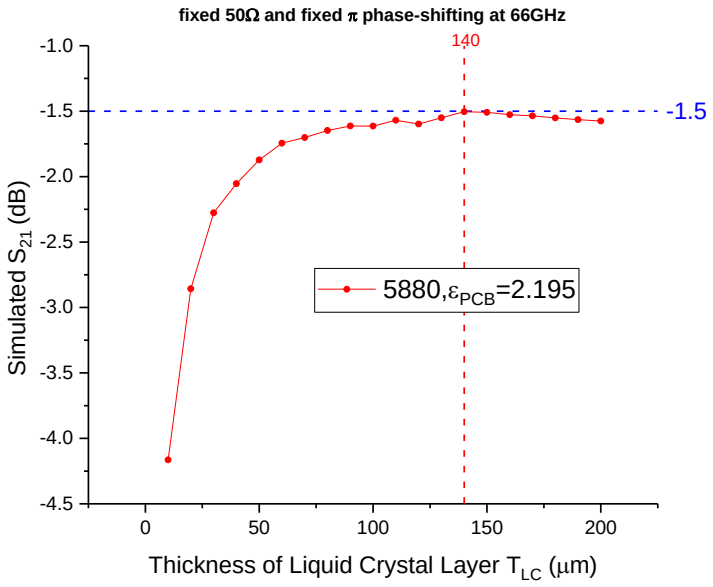
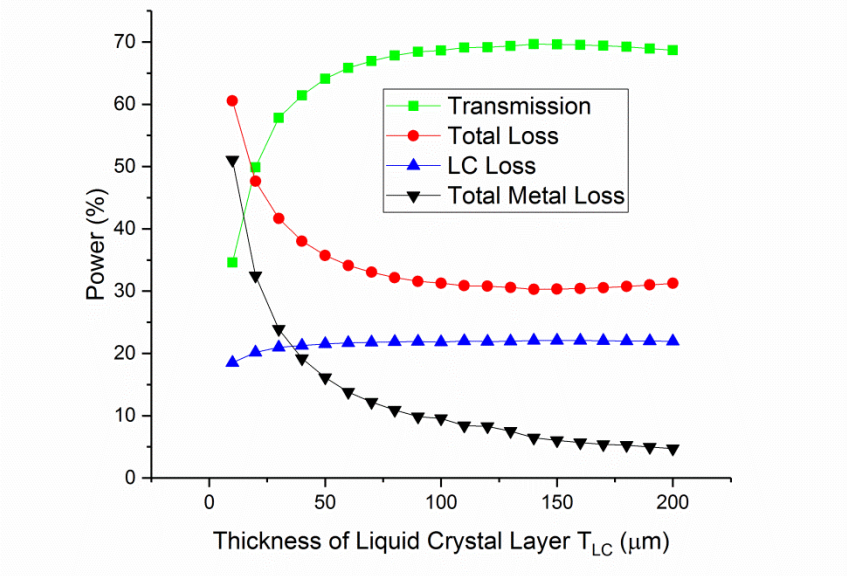


Fig.49 Simulated S_{21} at 66GHz (0V Bias) for Two Cases: Fixed Geometry vs. Fixed 50Ω

In awareness of the nonlinearities above for a fixed LC-layer thickness T_{LC}, we subsequently vary T_{LC} targeted for fixed-50Ω and π-shifting. Likewise, W_{strip} narrows with the drop of the T_{LC} to keep 50Ω. However, the closer proximity of core and top conductor results in an elevated electric field intensity especially around the core's surface, hence the domination of metal loss (see Fig.50 (b) below), which contributes to a slump in S_{21} as shown in Fig.50 (a). The ratio of the total conductor losses (assuming a perfectly-smooth surface) to the total losses is quantified as parametrised with the LC thickness at 66GHz. The simulation is performed in a 50Ω controlled impedance (by varying W_{strip} and W_{gap} for each T_{LC}) and for a fixed phase shifting of π (by varying the line length L).



(a) Simulated S_{21} vs. T_{LC} (66GHz, 0V Bias, Fixed 50Ω, π-shifting)



(b) Loss Decomposition Analysis vs. T_{LC} (66GHz, 0V Bias, Fixed 50Ω, π-shifting)

Fig.50 Simulated Effects of T_{LC} on S_{21} and Loss Decomposition Analysis

It is worth noting from the mathematical expressions (eqs. 29 and 30) we have derived for the material losses that the squaring then integrating (for dielectric loss) is different from the integrating then squaring (for metal loss). This accounts for the different phenomena that metal loss and dielectric loss level off with T_{LC}, respectively, as illustrated in the almost constant LC loss versus the change of T_{LC}, while the metal loss drops dramatically.

There are few freedoms to optimise the LC's dielectric dissipation by changing the geometry, due to the limit of keeping the aspect ratio (W_{strip} to T_{LC}) for impedance-matching. However, increasing the LC thickness plays a dominant role in reducing the conductor loss and hence reducing the total material absorption loss at 66GHz, even without considering the metal surface roughness (which may elevate the proportion of conductor loss further). Increasing the LC thickness from 10μm to 100μm, the conductor loss is reduced from 51.1% to 9.6%. The total loss is correspondingly reduced by 30%.

In a summary of the above simulated results, commercially-available RT/duroid 5880 or Taconic's TLY-5 are theoretically the most suitable PCB substrate candidates, because their dielectric constant (ε_{PCB}=2.195) at 54GHz-67GHz is closest for the optimal dielectric constant ratio (ε_{LC} /ε_{PCB}) based on the nematic LC we are using, i.e. GT3-24002 with ε_{LC} =2.5 at 0V bias. The corresponding 50Ω-optimised ECPW transmission line (with fabrication tolerances considered) is with a cross-sectional geometry of W_{strip} =293μm, W_{gap} =203μm, T_{LC} =140μm and a length L of 14.32mm for a maximum differential phase shift of π at 66GHz.

4.3 Low-loss PCB Substrates and Cu Foil Investigation at 60GHz

From the technical point of view for our device's assembling system (connectors edged-mounted on PCB substrate with an enclosure to provide a cavity accommodating LC layer), dimensional instability of PCB substrate and the bonded Cu foil on top (section 4.3.1) can degrade the fabricated device's electrical performance significantly at 60GHz (interpreted in section 4.3.2).

4.3.1 Mismatch in Coefficient of Thermal Expansion (CTE) and Post-etch Stress Relief

To bond the Cu foil to PTFE-based dielectric substrates (e.g. RT/duroid 5880 and RO3003), the lay-up of Cu foil and dielectric substrate is clamped and heated above the crystalline melting point of PTFE (i.e. >327˚C). It is worth noting that the post-laminated PTFE exhibits a bi-phase nature, i.e. half crystalline and half amorphous in the dielectric. Specifically, the amorphous phase is viscoelastic, characterised by a rubbery state (elastic) and a glassy state (viscous). On one hand, the elastic property immediately responds to stress applied, hence resulting in deformation instantly. On the other hand, the viscous property exhibits a time-dependent stress response, i.e. a long-term (in days) continued effect on deformation.

The Coefficient of Thermal Expansion (CTE) is measured for two dielectric substrate candidates (5880 vs. 3003) and the Cu foil laminated on top. As shown in Table 6, Cu's CTE is isotropic (17 ppm/ºC for all axes), while 5880 and 3003 dielectric substrates exhibit anisotropic CTE which are mismatched with those of Cu's. In particular, as glass microfiber reinforced PTFE with no ceramic-filled, 5880 exhibits largest CTE mismatching with Cu in the y-axis (thickness direction). As 3003 is ceramic-filled and glass fabric free, it exhibits better in-plane CTE match to Cu foil.

Table.6 Measured Coefficient of Thermal Expansion for Cu vs. 5880 vs. 3003

Coefficient of thermal expansion (CTE)	Cu	5880 (measured condition: 0-100˚C)	3003 (measured condition: -55 to 288˚C)
x-axis	17ppm/˚C	31 ppm/˚C	17 ppm/˚C
z-axis	17ppm/˚C	48 ppm/˚C	16 ppm/˚C
y-axis	17ppm/˚C	237 ppm/˚C (4.74% at 200˚C)	25 ppm/˚C (0.5% at 200˚C)

The CTE mismatch between Cu foil and the dielectric substrate causes an internal stress to develop in the laminate as it cools. Based on this, dimensional change can occur in the following fabrication processes of our devices.

[1] Post-etch stress relief.

When a pair of Cu channels are etched off to form a CPW pattern, residual stress developed in the PTFE-Cu system is relieved, resulting in conductor profile distortion and substrate bow (marked effect on thin PCB). The level of distortion and shrinkage depends on the amount of Cu removed, the relative thickness of each, main orientation of remaining Cu traces, the orientation of reinforcing fiber, and the time elapsed since Cu foil is bonded to PTFE (as is a continued effect). Additionally, CTE is anisotropic, i.e. deformation along machine direction (*x*-axis) defers from that along cross machine direction (*z*-axis). The exact amount of pattern distortion and etch shrinkage is technically demanding to predict.

[2] Post-bake cooling (after the soft and hard baking of alignment agents).

Due to mismatch in CTE, the PTFE-based PCB substrate and the bonded Cu foil are liable to deform in different levels at fluctuating temperatures. Note that rubbery state exhibits an appreciably faster stress relief rate than that of glassy state. Thereby, baking above glass transition temperature (130˚C) arguably accelerates the rate of stress relief.

Technically, the thermal coefficient is a problem for the 5880 material and difficult to maintain good flatness when cooling after the baking process with a single sided design using it. The reason is that the glass reinforcement is randomly-chopped glass as opposed to sheet glass. The 3003 is slightly better, but the filler in this is ceramic which also does not give much mechanical support. However, if the heating process can be performed flat and under pressure, then it should be able to maintain the flatness of the substrate.

4.3.2 CTE Mismatch Induced Standing Waves Resonance and Higher-order Modes Radiation

As the major cause of dimensional instability, in-plane coefficient of thermal expansion (CTE) mismatch between PCB and Cu foil has been investigated in section 4.3.1. The dimensional instability produces two adverse impacts on the device's electrical performance.

Firstly, the PCB substrate's non-uniformity can result in defected electrical contacts. Undesired gaps created between ground paths (or between connector pins and PCB core conductors) can cause higher-order modes and standing waves resonance, given the gap sizes are comparable to a quarter guided-wavelength in dielectrics ($\frac{\lambda_g}{4} \approx 0.7$mm). All of these disrupt the signal integrity and adds insertion loss significantly.

Secondly, the non-uniformity of PCB substrate also results in non-uniform thickness of the LC layer. This can alter phase constant and characteristic impedance for 60GHz wave propagation, causing phase shift distortion and problems related to impedance mismatch.

4.3.3 Effect of Copper Surface Roughness on Insertion Loss

For the sake of improved adhesion, metal surface roughness of the side laminated to the PCB substrate (dielectric side) is greater than that of the top side, as illustrated in Fig.51 the bonding interface (shown in red) is rougher than other sides.

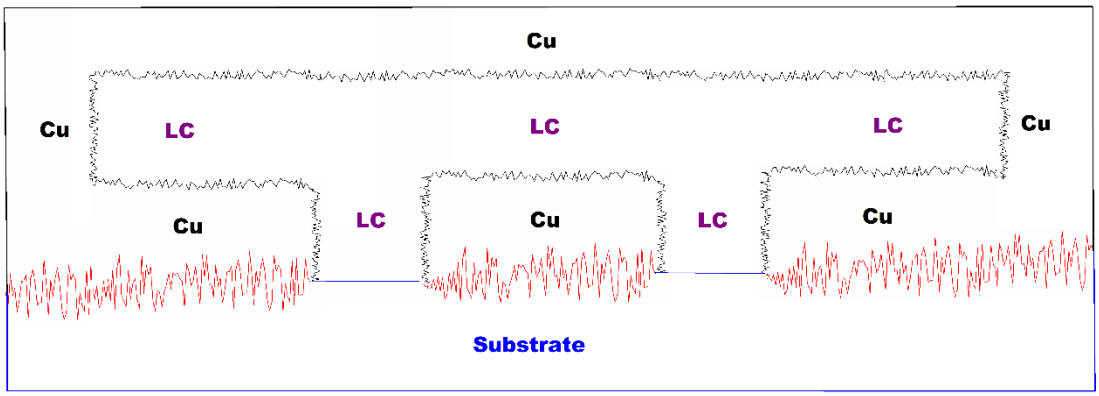
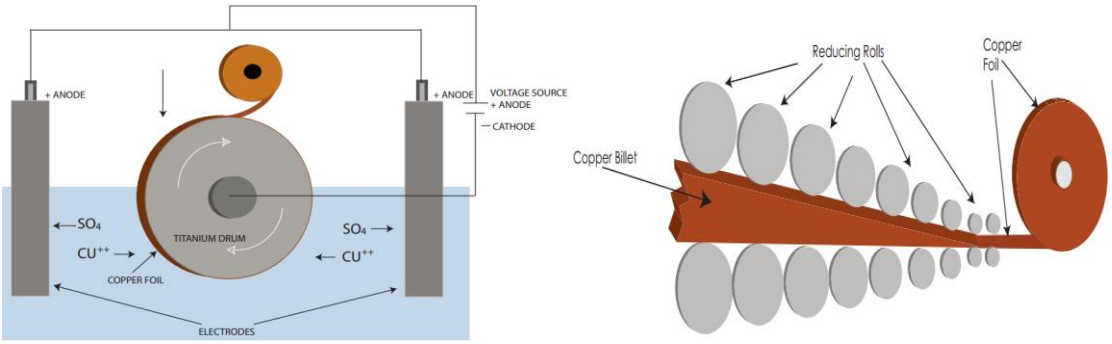


Fig.51 Actual Cross Section of Enclosed CPW (ECPW) with Cu Surface Roughness

By the nature of 60GHz-90GHz electromagnetic waves, electric field and current intensity are higher at the top side (especially the edge and corner) of the metal as compared with that of the bottom side. Electrodeposited (ED) copper and rolled annealed (RA) copper are the two main types of copper laminated to the PCB dielectric substrate, with the Cu surface roughness at the PCB dielectric side differing because of the fabrication process depicted in Fig. 52 below.



(a) Electrodeposited Cu (b) Rolled Annealed Cu

Fig.52 Fabrication Process of (a) ED Cu, and (b) RA Cu (Rogers)

Measured root-mean-square (RMS) roughness of the copper surface profile at the top side and dielectric side (i.e. Cu-PCB substrate interface) for different treatments is detailed in Fig.53. The measuring details carried out by surface profiler are reported later in section 6.1.3.

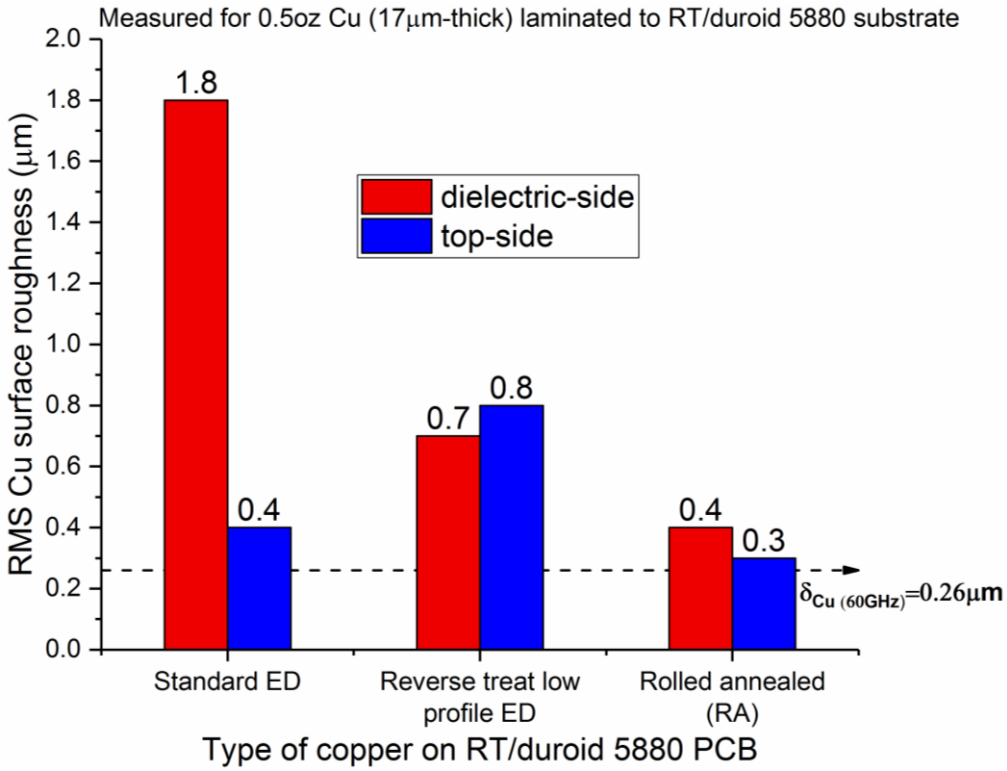


Fig.53 Surface Roughness Measured for 0.5oz Cu laminated to RT/duroid 5880 Substrate

The impact of metal surface profile on insertion loss is frequency dependent and highly related to the ratio of penetration depth to the metal surface roughness. As shown in Fig.53 above, penetration depth in copper is equivalent to (less than) the copper surface roughness for even the smoothest copper at 60GHz. In this case, the surface effects of the conductor will be significant, i.e. rougher surface will cause more stray inductance and a change in the surface impedance, and ultimately, result in an increase in insertion loss. From the mechanical point of view, surface roughness of metal has positive impact on the bond strength and hence enhancing adhesion capability to the resin systems. However, the adhesion of different copper foil to the 5880 substrate is not sensitive for our application.

Regarding commercially available substrates with Cu foils laminated, Taconic's TLY-5 PTFE-glass substrates with ULPH (ultra-low-profile half oz) Cu are comparable to Rogers's RT/duroid 5880 substrates with rolled Cu in terms of dielectric, thermal, CTE, mechanical properties and surface roughness. We purchased 5880 panels of rolled and electrodeposited copper, respectively, and experimentally verified the impact of the surface roughness on insertion loss of our device (Chapter 7.1).

4.4 Electrode Materials and Gold-plating

4.4.1 Electrical Conductivity of Enclosure Materials and Oxidation

As characterised in Fig.54 below, a number of base metal candidates are considered for the enclosure, with a special focus on the post-oxidised degradation in the electrical conductivity (increase in resistivity).

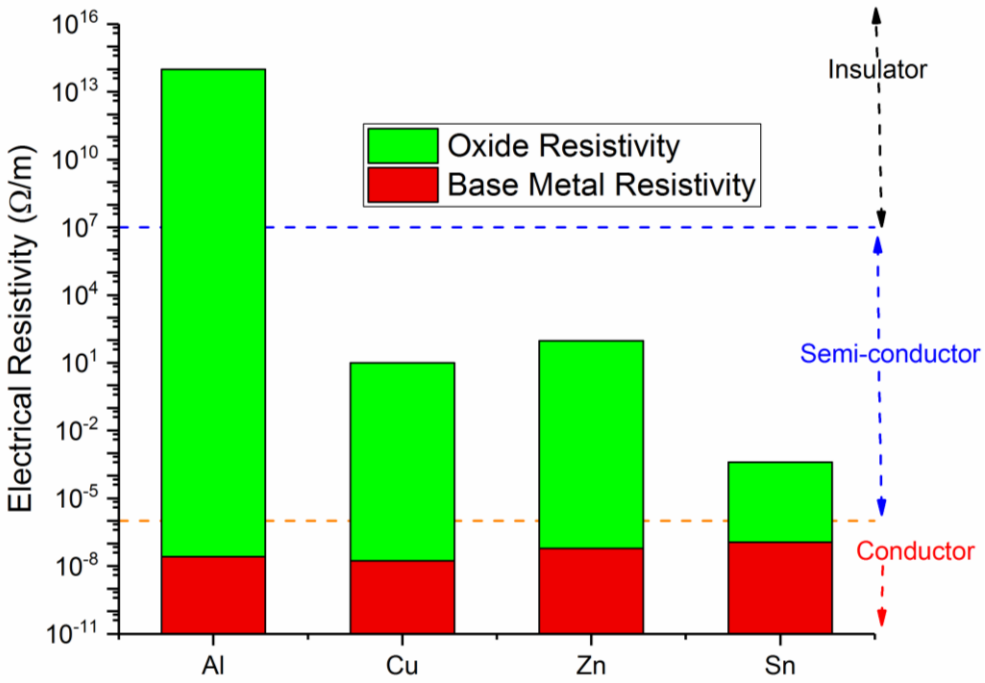


Fig.54 Electric Resistivity of Various Candidate Materials for the Enclosure

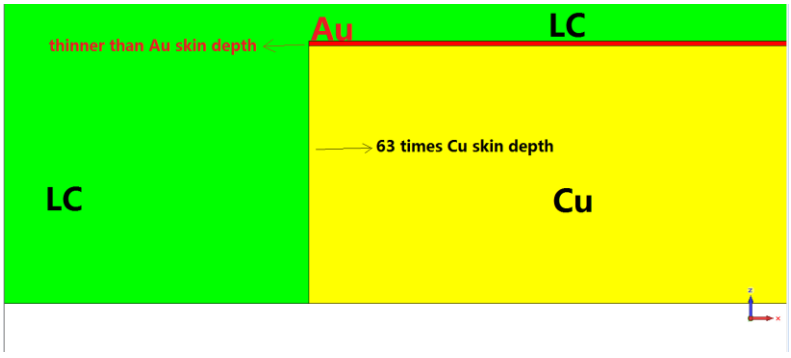
Pure aluminium (Al) and aluminium alloy 1350 (>99.5% aluminium) is the metal used previously as our 1-10GHz microstrip device's ground plane. They form insulating oxide layer rapidly, disrupting the electrical continuity of the ground path (high resistivity at the metal-to-metal interface contacts), and hence not suitable for our 60GHz applications. Stainless steel (alloy with a small amount of chromium) features high durability, and corrosion-resistance reported as a few 1.85mm coaxial connectors' body. However, it exhibits an electrical conductivity 40 times lower than that of Cu, which struggles to meet the low resistivity requirement. For the same reason, C360 Brass (a copper-zinc alloy 27% as conductive as Cu) being deployed as some 1.85mm connectors' housing material is also not considered for our enclosure design.

Silver is more conductive than gold, but it oxidises over time (Moore, 1998) unlike gold. Moreover, silver-plating is susceptible to a corrosion called red plague (Morgan, 1967) especially for porous silver layer under moisture, which raises a problem for phase shifters operating in high humidity environment. For lowest conductor loss and to deter oxidation, we employ C101 pure Cu as the enclosure body, and directly conduct gold-on-Cu plating without a barrier layer (e.g. nickel). The implications of gold-plating thickness on insertion loss is simulated as follows (section 4.4.2), with technical issues considered in section 4.4.3.

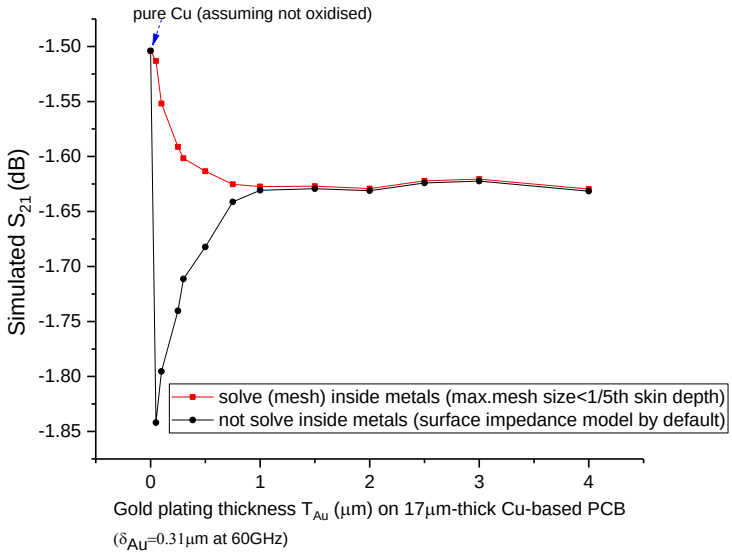
4.4.2 Simulated Impact of Gold-plating Thickness on Insertion Loss

Many of the metals used as a finish for PCBs are less conductive than copper, and the addition of these finishes results in an increase in conductor loss. Depending on the gold-plating thickness (T_{Au}), the addition of gold can disrupt the electric field around the conductor edges, and modify the tunable dielectrics volume, which affects the phase-shift tuning and loss performance. As observed in Fig.55 (b) below, the addition of gold finish on both the Cu-based PCB and enclosure degrades S_{21} due to increased resistance as compared with non-plated pure Cu (assuming oxidisation not happened).

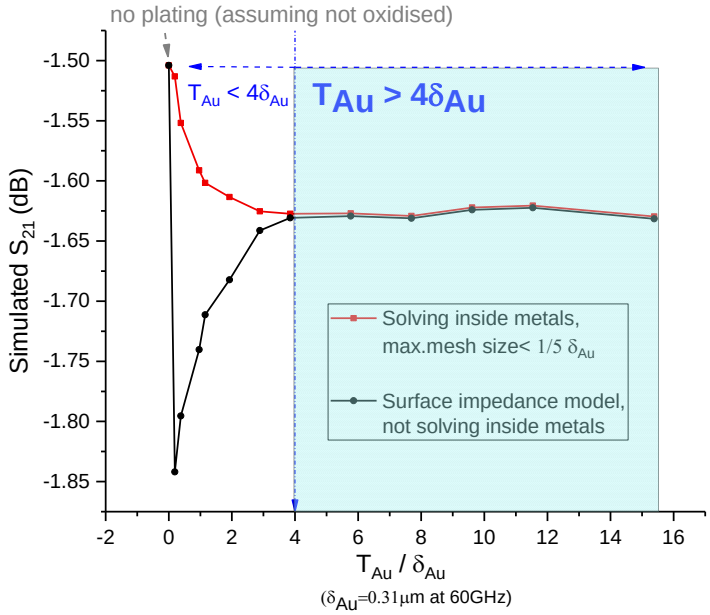
As mentioned in section 3.2.3, the validity of the adaptive meshing based on surface impedance model (without meshing inside metals) is examined here for the thin gold-plating layer on Cu, as shown in Fig.55 (a) below. The penetration depth at 60GHz is 0.31μm for gold (δ_{Au}) and 0.26μm for copper (δ_{Cu}). We analyse the simulated results from Fig.55 (b) and replot our findings in Fig.55 (c) by looking into the S_{21} versus the ratio of the gold-plating thickness to the gold's skin depth (T_{Au}/δ_{Au}) at 60GHz.



(a) A Sketch of the Size Comparison between Plated Gold, Base Cu, and Their Skin Depths



(b) Simulated Insertion Loss vs. Gold-plating Thickness based on Two Calculation Methods: Meshing inside Metals vs. Surface Impedance Model withou Meshing inside Metals



(c) Results Analysis based on (b): Surface Impedance Model Fails for $T_{Au}<4\delta_{Au}$

Fig.55 Simulated Impact of Gold-plating Thickness on Insertion Loss at 60GHz

As already numerically proved in Chapter 3.2.3, for the conductor thickness T >> the penetration depth δ, the surface impedance model by default (not solving inside metals) works fine. There is no need for meshing inside conductors which increases the computation burden significantly. For structures in which the penetration depth of the field into the conductors is of the same order as the conductor thickness, such as when $T_{Au}<4\delta_{Au}$ in the gold-plated Cu model as shown in Fig.55 (c), substantial errors can occur in the loss estimation. As illustrated in the gold-plated Cu model with $T_{Au}<4\delta_{Au}$, the surface impedance model over-estimates the

conductor loss by up to 0.3dB/cm. In this case (conductor thickness comparable to the skin depth), it is highly important to mesh (solve) inside metals (gold) to accurately represent the field's decaying behaviour without overestimating the conductor loss. It is observed that S_{21} levels off when T_{plated} increases to 4 times of δ_{Au}, beyond which both calculation models agree in statistics.

4.4.3 Practical Consideration of Gold-plating Thickness: Cu Migration into Gold and Oxidation

At elevated temperature, an inadequate thickness of pure gold deposited on the PCB can result in a diffusion of Cu atoms into gold (tarnishing), exposing the copper and ultimately formation of oxide layer which degrades the electrical conductivity, as demonstrated by the experiment results shown in section 6.1.3 and section 7.2.3.

Out of the concern for the problematic Cu migration into gold (accelerated by evaluated temperature when baking the alignment solvent), the plated gold should be thick enough compared with the Cu foil underneath. However, the etching and plating errors both increase dramatically with the plating thickness, resulting in a substantial deviation from the original right-angle design of the conductor profile. The optimisation of T_{plated} is hence based upon the compromise upon both theoretical and technical factors. It is experimentally shown in our device measurements (section 7.2.3) that 2μm suffices to reliably deter Cu oxidation, while degrading S_{21} by only 0.1dB as compared with bare Cu in the simulation (assuming no oxidation occurred) mentioned above (section 4.4.2).

Chapter 5. Design of Connector-to-PCB Transitions

The transmission line model considered thus far in the preceding chapters can be treated as a cross section of conductors embedded in tunable and non-tunable dielectrics, by which phase tuning is realised along the line length. Phase shifters reported in up-to-date documentation so far have been mainly characterised by microwave probe station with no connectors included. However, making a device with suitable coaxial connectors mounted is not only for characterisation purpose with a vector network analyser (VNA), but is also essential for delivering products of industry standard that readily interconnect with other components or cables. To enable the complete device's functionality with low reflection when incorporating connectors, matching network (connector-to-PCB transition) design is described in this work.

5.1 Geometry Discontinuity, Polarisation Transition, and Coupling

Interfaces between the optimised 50Ω tunable ECPW and 50Ω coaxial connectors are not 50Ω owing to the change of electric field polarisations (modes), hence the need for a transition design. From the wave-propagating point of view (longitudinal direction), configuration of the phase shifter device is divided into multiple cross sections (Fig. 56 below) with different modes at the interface of each geometrical discontinuity.

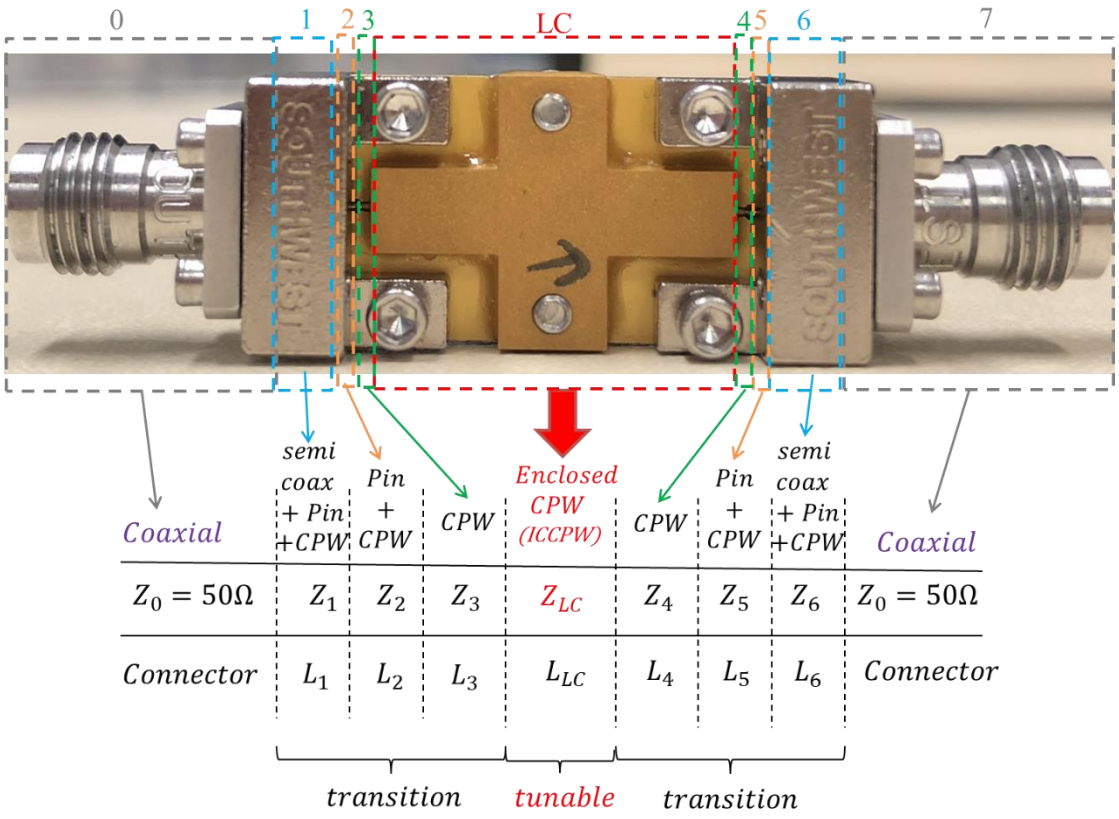


Fig.56 Segmentation Analysis of the Complete Phase Shifter with Connectors Installed (Device Photo Taken for Our Optimised Design after Experiment as Detailed in Chapter 7)

As depicted in Fig.56 above, the phase shifter device can be divided into 9 portions according to modes diversity caused by geometrical discontinuities. From left to right and a tunable part in the middle, the circuit is characterised by 9 modes with 8 transitions, i.e. from coaxial to semi-coaxial to elevated-CPW to CPW to tunable enclosed CPW (ECPW) to CPW to elevated-CPW to semi-coaxial, and finally back to coaxial. Detailed cross-sectional analysis on each portion is as follows.

Cross section 0 is a 50Ω 1.85mm coaxial connector (insertion loss of -0.4dB measured at 60GHz) and its transition block (insertion loss of -0.09dB). The mode of this part is coaxial. Cross section 1 represents the connector's launch pin attached to the top surface of CPW's core trace on PCB. The gold-plated pin is shielded by connector's full-arch-shaped ground, with nickel plate at the bottom for screw positioning and stress equalization. The mode of this part is semi-coaxial. Cross section 2 denotes the launch pin extending outside the connector's full-arch-shaped ground, while still attached to CPW's core on PCB, and with nickel plate at bottom. The mode of this part is elevated-CPW since the pin landing on the CPW core elevates the core

conductor exposed in air. Cross section 3 is CPW on PCB, with glue deposited on top for sealing the opening of the LC-filled cavity. Cross section LC denotes the 50Ω enclosed CPW (ECPW) tunable transmission line (S_{21}= -1.5dB simulated for π shift) already optimised in Chapter 4. Cross sections 4-7 are symmetric with cross sections 0-3.

Given the coaxial connector and the PCB CPW transmission line are of the same characteristic impedance (50Ω) as above. When joining them together, structural discontinuity at the interface disrupts the electric field distribution, resulting in mismatching and non-transmitted higher-order modes. By the circuit theory, geometrical discontinuity at the interface is equivalent to adding a shunt capacitor (with a susceptance of *b* measured in *siemens*) between the two parts, as interpreted in Fig.57 below.

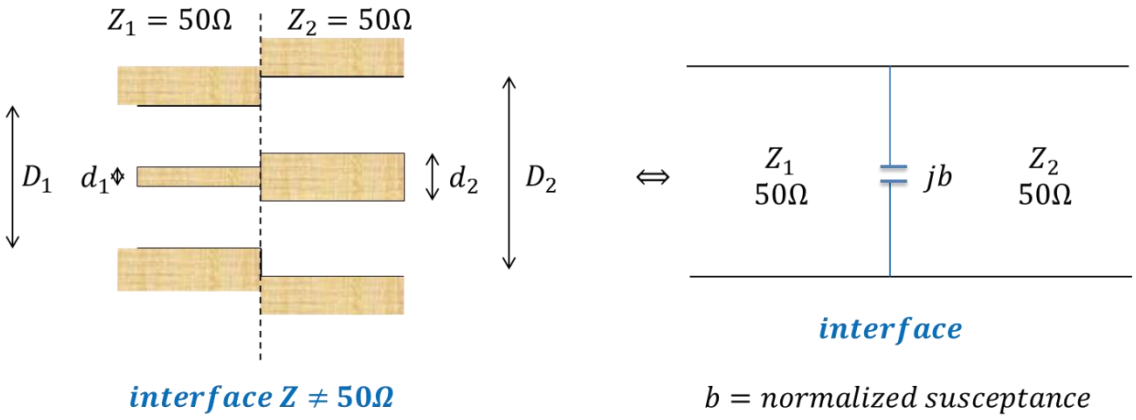


Fig.57 50Ω Coaxial to 50Ω CPW Geometrical Transition Schematic and Equivalent Circuit

Reflection coefficient at the interface is $\Gamma = \frac{1-(1+jb)}{1+(1+jb)} \approx \frac{b}{2}$ (for small *b*). The value of *b* depends on geometrical discontinuity (polarisation difference) and frequency. The higher the frequency and the larger the discontinuity, the more pronounced the mismatching. Furthermore, the discontinuity part is vulnerable to dielectric breakdown, which limits its high-power applications.

One approach we employ to tackle this specific mismatching problem is based on offsetting the core pin by a small distance of *l*, which is far smaller than a wavelength. This creates two discontinuous interfaces, denoted with shunt conductance of C_1 and C_2, and a series inductance of *L* in the equivalent circuit analysis shown in Fig.58 below. The offset distance *l* is chosen strategically to equalise the characteristic impedance between the offsetting part and

the adjacent parts. The offsetting concept has been implemented in the design of our connector's transition block, i.e. extending the connector's core pin by a small distance when landing on the edge of the PCB core trace.

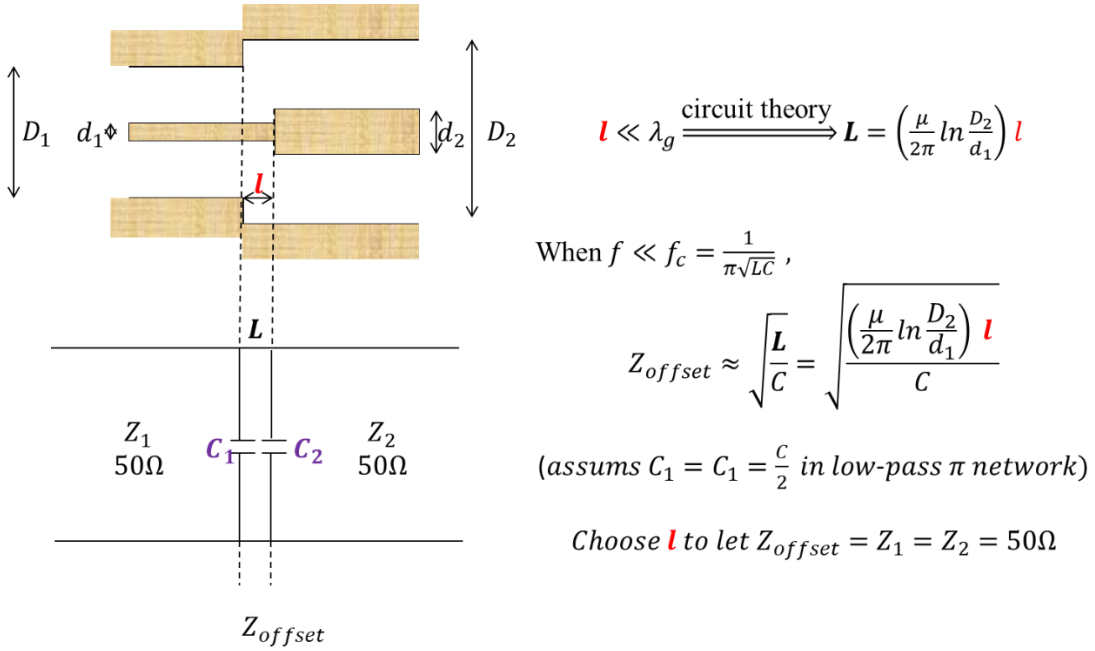


Fig.58 50Ω Coaxial to 50Ω CPW Matching by Conductor Offsetting

However, the above schematic constitutes only an extremely simplified circuit analysis. To complicate the picture, pin-to-core attachment exhibits a height discontinuity that is not ignorable.

Moreover, the method for accurately characterising the impedance of each transition parts is worth investigation for the whole device optimisation. The fundamental difference between the tunable part simulation (aforementioned) and the whole device simulation (to be attempted in this chapter) is that the tunable portion simulation assumes an infinitely-long transmission line, taking a small line section's cross section (TEM polarised field) for analysis. However, the whole device with connectors and transition parts is no longer an infinite transmission line. Instead, wave polarisation changes sequentially from cylindrical (2D radial, *x*-*y* plane) to planar CPW (almost 1D, *x*-axis), then to enclosed CPW (2D, *x*-*y* plane), followed by planar CPW (almost 1D, *x*-axis), and the other way round back to the cylindrical (2D radial, *x*-*y* plane).

To recapitulate, given that the tunable portion is optimised (insertion loss of -1.5dB) and the coaxial connectors and transition blocks are fixed (insertion loss of -0.98dB for a pair), current

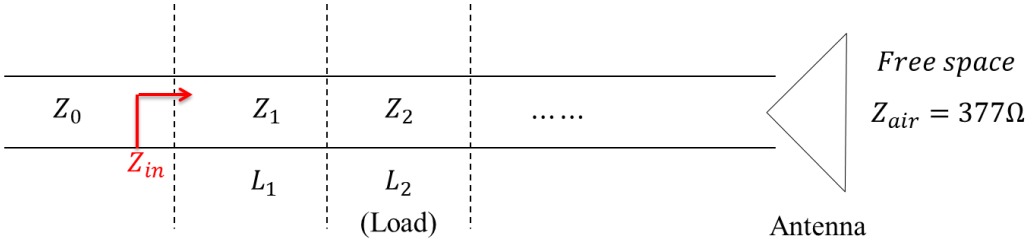
work is to design the transition part between them in recognition of the polarisation difference, i.e. to couple the polarisations in different planes smoothly and minimise the generation of higher-order modes that satisfy Maxwell's equations with the boundary conditions at the coaxial-to-coplanar transitions.

5.2 Wideband Impedance-Matching Scenarios for ECPW Device

Theoretically, impedance transform between parts with diverse impedances can be realised by wave interferences, e.g. impedance stepped transform by a-quarter-wavelength cancellation, or impedance continuous transform by tapering the guiding conductors. However, these techniques work only for a limited bandwidth. In another words, the most-matched frequency is dependent on the transmission line (taper) length.

5.2.1 Cascade of Sections with a Uniform Impedance for Symmetric Network

Impedance matching scenarios are application-oriented. By ways of illustration in Fig.59 below, consider a lossless uniform transmission line with multiple sections in the wave propagating direction, a-quarter-wavelength method or tapering can transform an impedance from low (e.g. 50Ω transmitter) to high (e.g. an antenna), or vice versa. A broadband solution might be obtained by a cascade of *λ/4* sections of gradually varying characteristic impedance. Note that the loads in this work are not purely resistive, hence complex impedances are assumed, where voltages and currents are not in phase.



$$Z_{in} = Z_1\left[\frac{Z_2+Z_1\tanh(\gamma L_1)}{Z_1+Z_2 tanh(\gamma L_1)}\right] = Z_1\frac{Z_2+jZ_1\tan(\beta_1 L_1)}{Z_1+jZ_2 tan(\beta_1 L_1)} \text{ (lossless assumed)}$$

$$Let\ L_1 = \frac{\lambda_1}{4} \Rightarrow\ tan\beta_1 L_1 = tan\frac{\pi}{2} \to \infty \Longrightarrow Z_{in} = \frac{Z_1^2}{Z_2} = Z_0 \Leftrightarrow Z_1 = \sqrt{Z_0 Z_2}$$

……

$$Let\ L_n = \frac{\lambda_n}{4} \Longrightarrow \boldsymbol{Z_{n-1} = \frac{Z_n^2}{Z_{n+1}}}$$

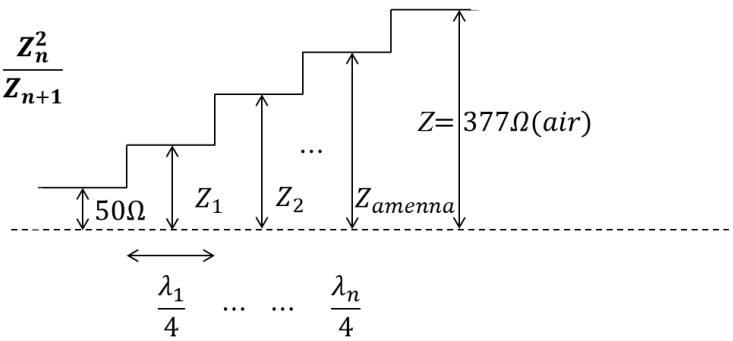


Fig.59 Impedance Transforming by a-quarter-wavelength Approach

Unlike the antenna system above with impedance's gradual variation from 50Ω feeding line stepped to 377Ω free space, the phase shifter in this study is a two-port device with input and output both connected to 50Ω coaxial cables, forming a symmetric network. For this boundary condition, the only solution to the equation sets of $\frac{Z_0}{Z_1} = \frac{Z_1}{Z_2} = \frac{Z_2}{Z_3} = \frac{Z_3}{Z_{\mathrm{LC}}} = \frac{Z_{\mathrm{LC}}}{Z_4} = \frac{Z_4}{Z_5} = \frac{Z_5}{Z_6} = \frac{Z_6}{Z_0}$ is $Z_0 = Z_1 = Z_2 = Z_3 = Z_{LC} = Z_4 = Z_5 = Z_6 = 50\Omega$, i.e. a uniform impedance of 50Ω for each cascaded cross section.

5.2.2 Coupling and Higher-order Modes

In particular, geometrical shape difference here gives rise to abrupt polarisation (mode) variations, from cylindrical (2D radial, *x*-*y* plane) to semi-coaxial-shielded CPW, planar CPW (almost 1D along x-axis), enclosed CPW (2D, x-y plane), then reverses back. The E_z component satisfying Maxwell's equations with boundary conditions at the coaxial-to-coplanar transition generates higher-order modes in the form of surface waves that contribute to radiation loss.

For instance, the edges of the connector's core pin (signal line) and the LC-filled metal enclosure (ground) are prone to undesired coupling (non-TEM E_z component as illustrated in Fig.60 below) and a quarter-wave resonance as well.

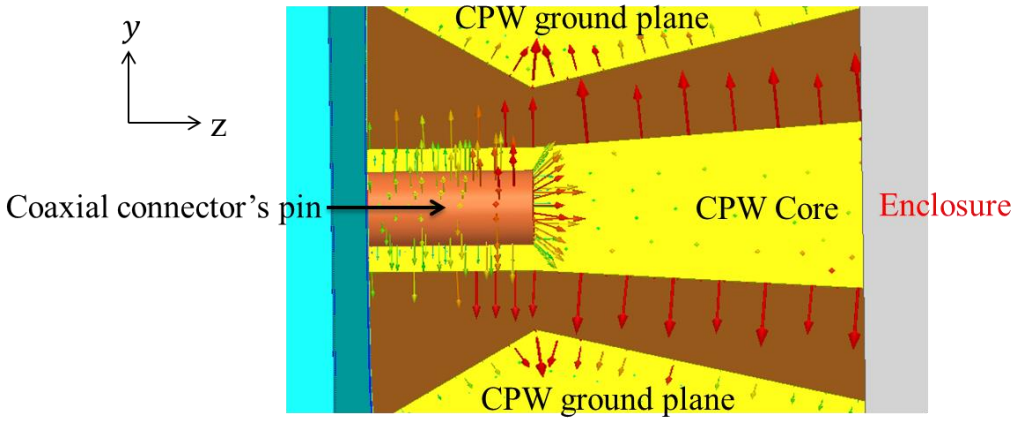


Fig.60 Simulated Coupling between the Connector's Core Pin and the Enclosure

The elevated CPW mode (due to the pin's height) and the coupling between the pin and the enclosure are addressed by tapering the ground conductors (W_{taper} is optimised later in section

5.4.2.1), whilst investigating the optimum distance between the pin and the edge of the enclosure (L_{taper} is studied later in section 5.4.2.3).

5.2.3 Getting Knowledge of the Interface Impedance by TLM vs. TDR

In summary, the matching solution of this symmetric ECPW phase shifter configuration is approximating the device with 50Ω at every cross section. To minimise coupling losses (reflection and radiation) arising from the connector-to-PCB interface, frequency-dependent adjustments of the PCB edge's geometry are made through the combinations of core width (W_{taper}) and core-ground slot spacing to modify the inductance and capacitance of the signal launch.

Fundamentally, the geometry design requires a precise knowledge of the transient impedance of each line section. If a line section is physically short enough compared with wavelength (e.g. $<\frac{\lambda}{10}$), a signal may not be sensitive to some of the important properties we usually associate with a transmission line (i.e. no longer a transmission line, but a lumped capacitor or inductor). Here the length of the connector pin exposed in air=0.254mm$<\frac{\lambda}{10}$, which is electrically small and should not be treated as a transmission line.

While a conventional frequency domain solution based on the infinitely-long transmission line model fails to gain the knowledge of every section's impedance when joining all sections together, transient network analysis can be used to complement the infinitely-long transmission line model. Chapters 5.3 and 5.4 report the results of both solutions particularly for 0V where LC absorption loss is at maximum over all bias states (based on the proposed voltage-dependent impedance matching covered in Chapter 4.1).

5.3 50Ω Interface Matching based on Infinitely-long Transmission Line Model (TLM)

If the whole device with all sections targeted for 50Ω is designed based on the Infinitely-long Transmission Line Model (TLM) calculations, cascading these section does not result in a uniform impedance as illustrated later in Chapter 5.4, as the knowledge of impedance for each section is based on an infinitely-long transmission line with the assumption that the next section is fed by a preceding section with an identical polarisation. However, polarisation variations occur between different sections (from 2D to almost 1D).

By quantifying the time-domain transient impedance (methodology outlined later in Chapter 5.4) of every cross section of the whole device in Fig.61 below, it is verified that the classical infinitely-long transmission line model (TLM) fails to realise impedance matching for the interface (deviations by up to 30Ω are observed at the two peaks). The interpretation of the timed-dependent transient impedance is detailed later in section 5.4.2.5.

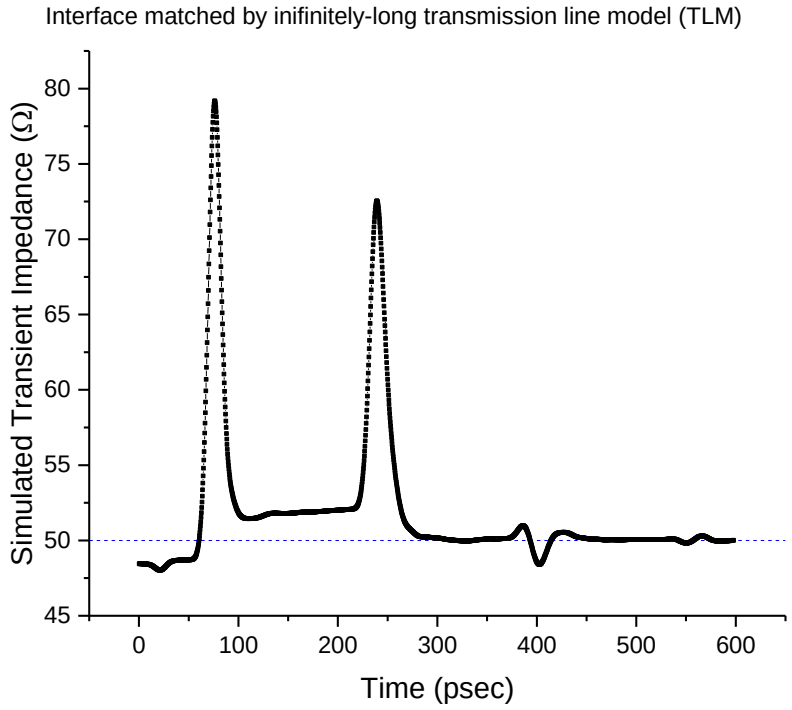


Fig.61 Transient Impedance Simulated for the Whole Phase Shifter (Connectors Included): Interface Design based on Infinitely-long Transmission line model (TLM)

In the wave-propagating direction, the phase shifter device involves multiple sections, i.e. the tunable transmission line and coaxial connectors, which are electrically-long at 60GHz, and the PCB transition between them, which includes certain electrically-short sections (by rule of thumb, shorter than $\lambda/10$ - $\lambda/16$).

However, such short sections in the connector-to-PCB joint cannot be considered as a transmission line in the design and analysis, hence the whole structure targeted for a controlled impedance obtained by conventional frequency domain infinitely-long transmission line model (TLM) is invalid, as illustrated in Fig.61 above. Here we propose using a time-domain reflectometry (TDR) method to quantify the transient impedance to optimise the electrically-short PCB transition.

5.4 50Ω Interface Matching by Time Domain Reflectometry (TDR)

5.4.1 TDR Concept and Calculation Setup

The Time-domain Reflectometry (TDR) method is used to locate and identify discontinuities. The concept behind TDR is injecting a pulse (time derivative of a step function with a finite rise time) into the device under test and observing reflections over time due to impedance anomalies (variations) at geometrical discontinuities. Based on the reflected signal, the transient characteristic impedance (*TDR Z*) along the device can be obtained based on the impedance ratio:

$$\frac{TDR\ Z}{Z_0} = \frac{input+reflected}{input-reflected} \qquad \text{.....(31)}$$

where Z_0 denotes the characteristic impedance at the input terminal.

The TDR model of the whole device is established by setting the TDR rise time = 13psec (10-90% rise time of the step function, shown in purple), corresponding to a frequency up to 67GHz. The actual excitation will be the derivative of the step function. See Fig.62 below, the excitation is the pulse shown in red when the input step (purple) reaches the maximum rate of change at t_{rise}=20psec. This is to be able to detect steady state and end the simulation, when observing that the fields everywhere in the model have fallen below a certain level.

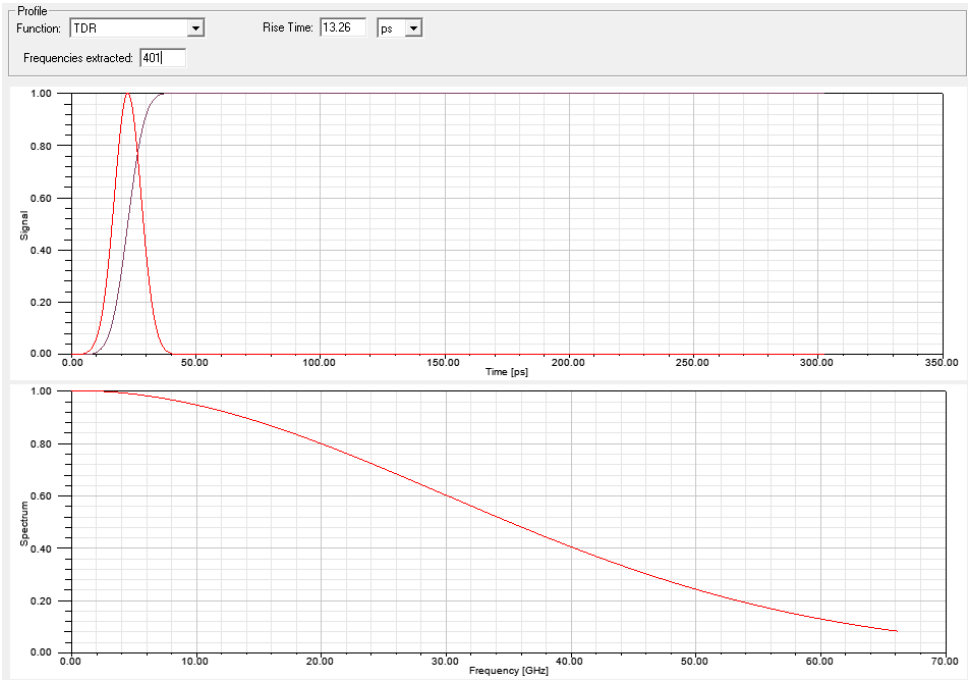


Fig.62 Rise Time and Simulation Frequency Setting in Time Domain Reflectometry (TDR)

Based on the electrical length expressed in time, i.e. $t = \frac{l}{c} \times \sqrt{\varepsilon_{eff}}$ …….. (32)

we can make the following estimations of the time taken for the signal bouncing back.

Connector transition block (dielectric is Teflon with ε_{eff}=2): $t_{teflon} = \frac{4.24\times10^{-3}m}{3\times10^{8}m/s} \times \sqrt{2}$ *=20 psec*

PCB transition block (dielectrics are air and PTFE with $\varepsilon_{eff} = 1.459$):

$t_{joint} = \frac{1.962\times10^{-3}m}{3\times10^{8}m/s} \times \sqrt{1.459}$ *=8 psec*

Tunable transmission line (dielectrics are LC and PTFE with ε_{eff}=2.408):

$t_{tunable} = \frac{14.32\times10^{-3}m}{3\times10^{8}m/s} \times \sqrt{2.408}$ *=74 psec*

Therefore, it takes at least $t_{rise} + 2 \times [(t_{teflon} + t_{joint}) \times 2 + t_{tunable}]$= *280 psec* to observe the reflection from the output terminal.

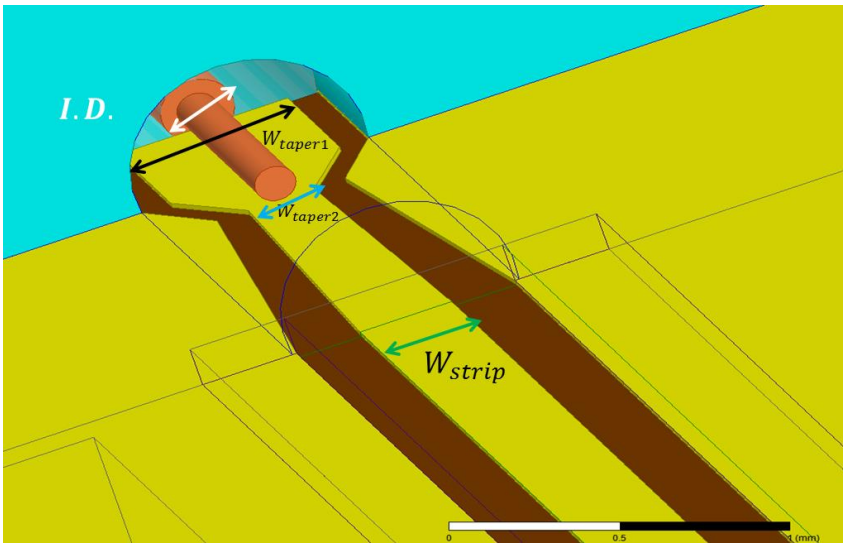
5.4.2 Taper Design by TDR vs. TLM and 60GHz Electric Field 3D Visualisation

As mentioned above, the interface geometry design of the PCB consists of two main transitions, first, the taper from the coaxial inner conductor to the PCB core, and second, the taper between the CPW and the tunable enclosed CPW (ECPW). The widths of the tapers are denoted as W_{taper1} and W_{taper2}, respectively.

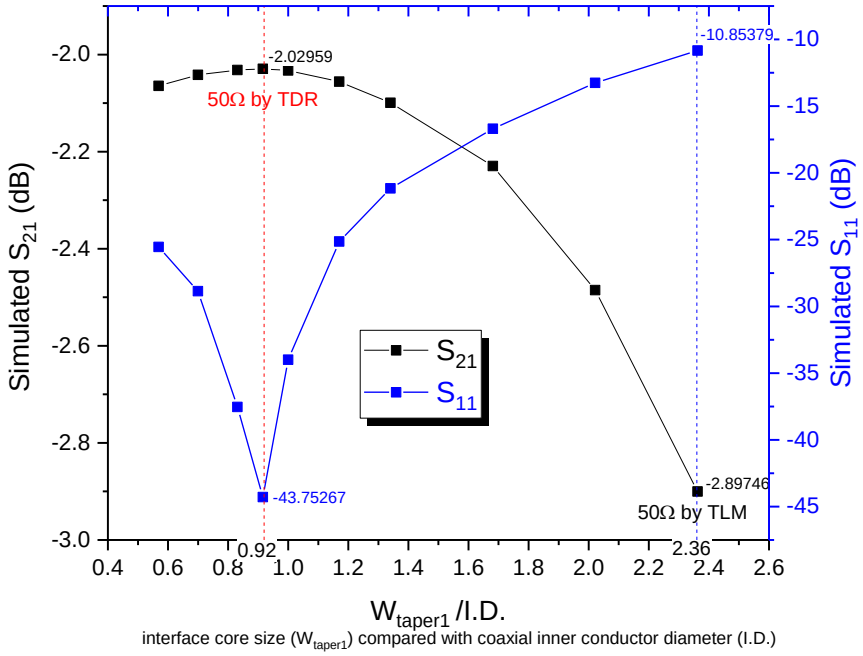
5.4.2.1 Cross-sectional Design of the Taper (W_{taper1} and W_{taper2})

As depicted in Fig.63 (a) below, the optimal W_{taper1} is investigated with respect to the connector's inner diameter (*I.D.*) as already known, while the optimal W_{taper2} is searched with respect to the tunable part's W_{strip} as already optimised. Time domain simulation is performed in Fig.63 below in search for the optimal aspect ratios at 60GHz. Fig.63 (b)(c) parametrise the *S*-parameters and loss percentage with the ratio of $\frac{W_{taper1}}{I.D.}$. Fig.63 (d)(e) present similar calculations but parametrised with $\frac{W_{taper2}}{W_{strip}}$. Designs based on TDR-matched and TLM-matched are compared based on the same tunable ECPW part (all other parameters the same),

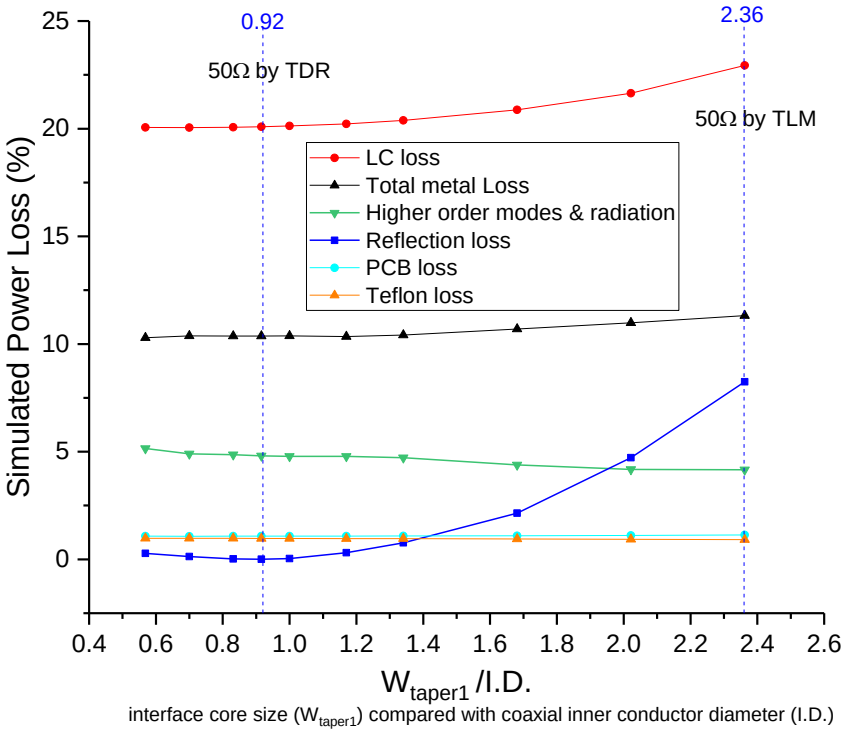
differing only in the geometry of the taper (targeted for 50Ω) due to the different impedance-calculating mechanisms.



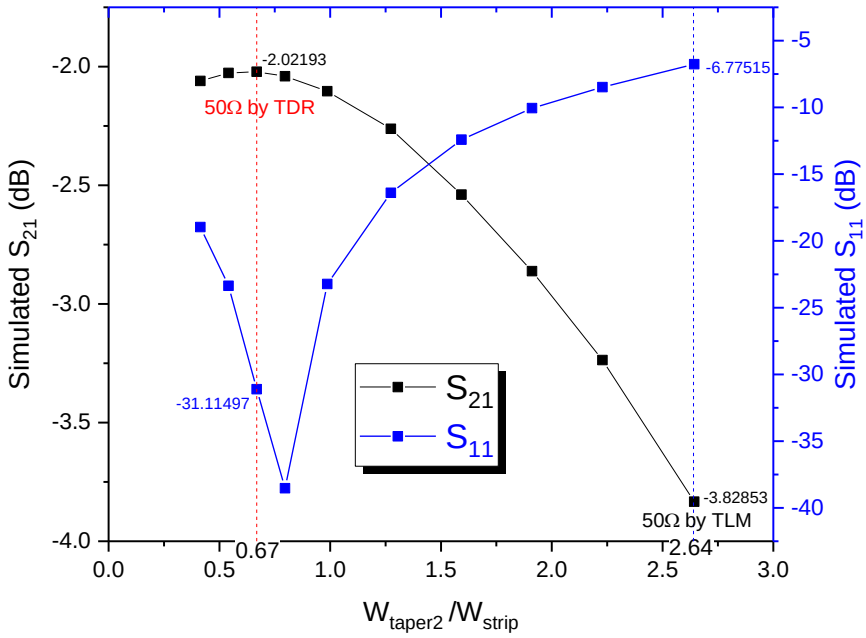
(a) Sketch of the Connector's Inner Diameter (*I.D.*) and Tapers to be Designed



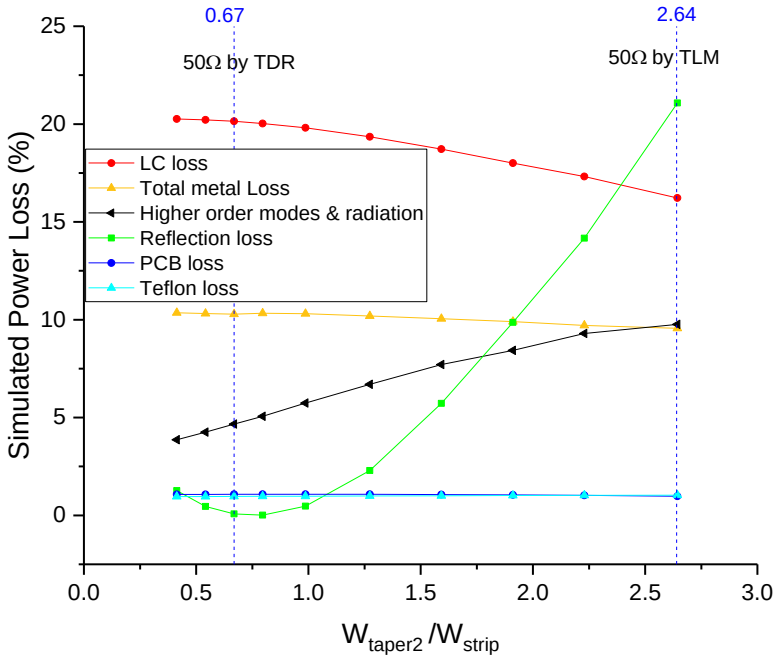
(b) Simulated *S*-parameters Parameterised with $\frac{W_{taper1}}{I.D.}$



(c) Loss Decomposition Analysis Parameterised with $\frac{W_{taper1}}{I.D.}$



(d) Simulated *S*-parameters Parameterised with $\frac{W_{taper2}}{W_{strip}}$



(e) Loss Decomposition Analysis Parameterised with $\frac{W_{taper2}}{W_{strip}}$

Fig.63 Design of Taper's Cross Dimensions (W_{taper1}, W_{taper2}) based on Loss Analysis

As observed from the power analysis in Fig.63 (c) (e) above, the variation of the taper's cross-sectional dimensions (W_{taper1} and W_{taper2}) has minor impact on the intrinsic material absorption loss (including metals and dielectrics), as the LC-based tunable ECPW part is fixed. However, the reflection loss is strongly influenced by the aspect ratio of the taper's cross dimension (W_{taper1} and W_{taper2}). As illustrated in Fig.63 (e), the taper geometry matched by TLM method exhibits 20% more of the return loss than that by the TDR approach. The aspect ratios of the taper's cross-sectional dimension for 50Ω are summarised in Table 7 below.

Table.7 Lateral Dimension of the Taper Targeted for 50Ω for Minimum Reflection Loss

Aspect Ratio Targeted for 50Ω	Matched by TLM	Matched by TDR
$\frac{W_{taper1}}{I.D.}$	2.36	0.92
$\frac{W_{taper2}}{W_{strip}}$	2.64	0.67

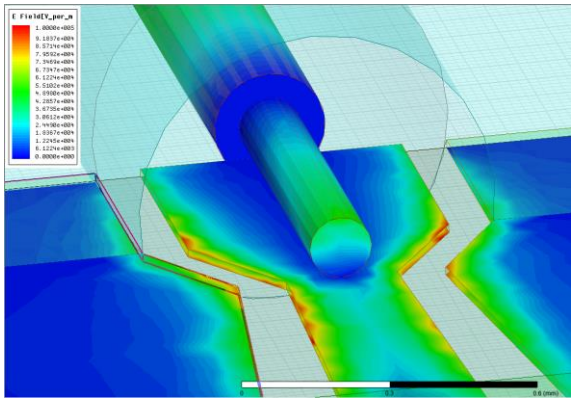
It is also worth noting the rising power dissipation due to higher-order modes and radiation arising at the semi-open CPW section when there is a large dimensional difference between the semi-open core width (W_{taper2}) and the core width (W_{strip}) of the tunable ECPW section. The

increased reflection and radiation jointly result in a huge deterioration of S_{21}, as confirmed in Fig.63 (b) (d) above.

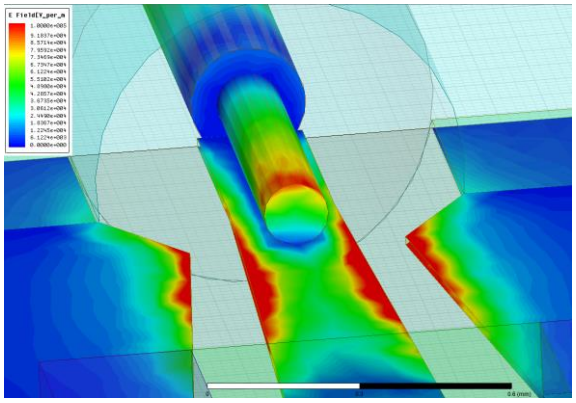
In conclusion, the interface's taper structure matched by the TLM method gives a large dimensional difference (discontinuity) as compared with the connector's inner diameter as well as the ECPW's core width, resulting in high reflection and radiation losses. Instead, the TDR approach solves the impedance-matching problem correctly and achieves optimal signal transmission.

5.4.2.2 3D Visualisation of the 60GHz Electric Field Distribution

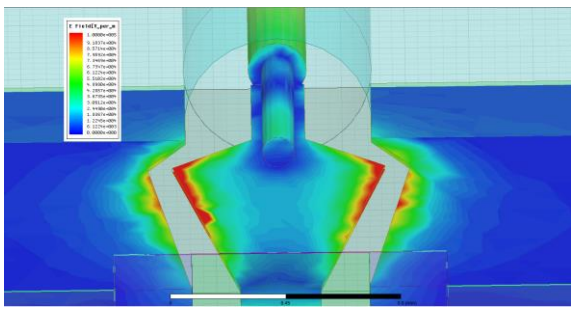
From the 60GHz wave-propagation point of view, we calculate the distribution of 60GHz electric field intensity in the interface regions from the connector to the designed PCB edge (tapers). Fig.64 below visualises the 60GHz field distribution difference between the structures matched by TDR versus TLM. All the figures share the same scale bar for the field intensity.



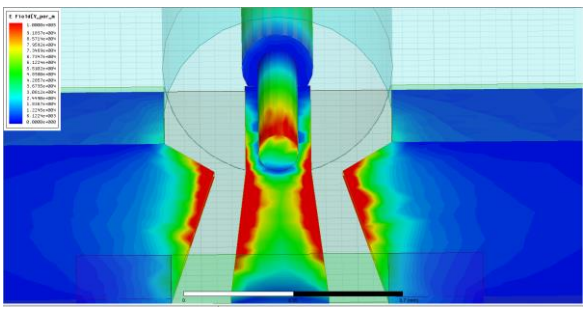
(a) $\frac{W_{taper1}}{I.D.}$ =2.36 (50Ω by TLM)



(b) $\frac{W_{taper1}}{I.D.}$ =0.92 (50Ω by TDR)



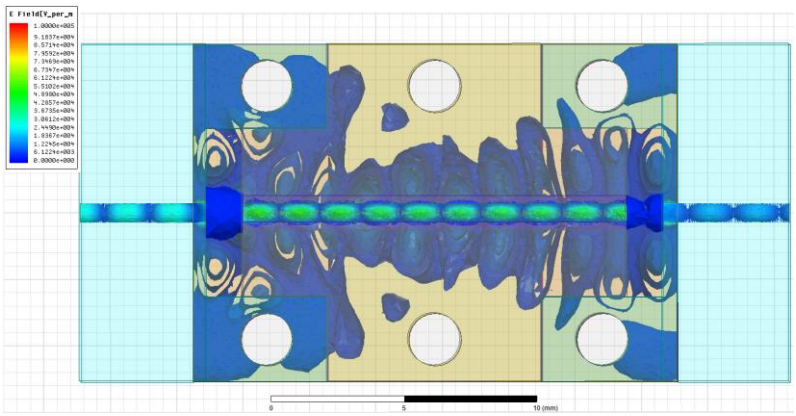
(c) $\frac{W_{taper2}}{W_{strip}} = 2.64$ (50Ω by TLM)



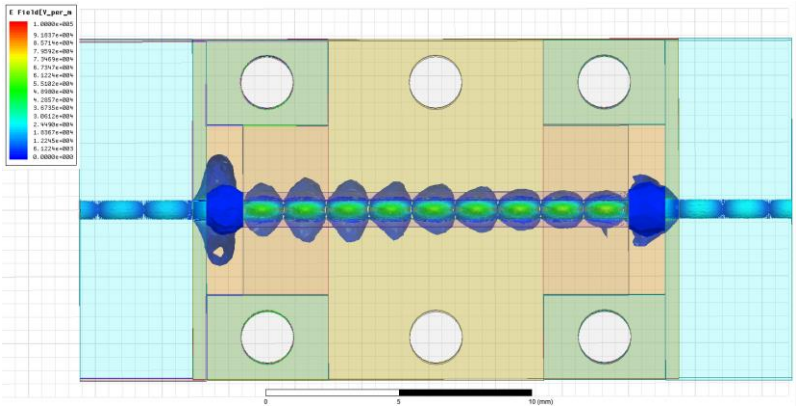
(d) $\frac{W_{taper2}}{W_{strip}} = 0.67$ (50Ω by TDR)

Fig.64 60GHz Electric Field Intensity Simulated for Interface Matched by 2 Methods

3D propagation of the 60GHz electric field is presented below for the whole phase shifter device, with Fig.65 below showing distribution in dielectrics only (LC and PTFE), while Fig.66 looking into critical metals only (core line, connector pin, and the CPW grounds). The field visualisations well agree with the above *S*-parameters and loss analysis. As evidenced in Fig. 64 (a)(c) above, the structure matched by TLM suffers heavily from higher-order modes and surface-wave radiation losses, as the electric field is poorly confined within the targeted CPW mode. Instead, the structure matched by TDR allows the electric field at 60GHz well-confined at the CPW's core (especially at the edges due to proximity effect) with minor radiation.

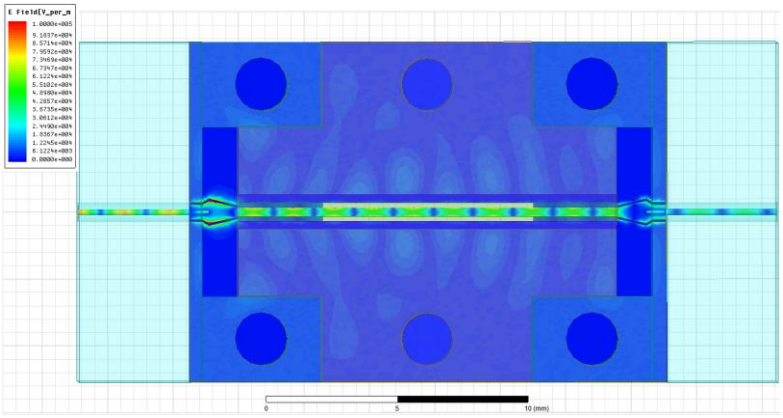


(a) $\frac{W_{taper2}}{W_{strip}} = 2.64$ (50Ω by TLM)

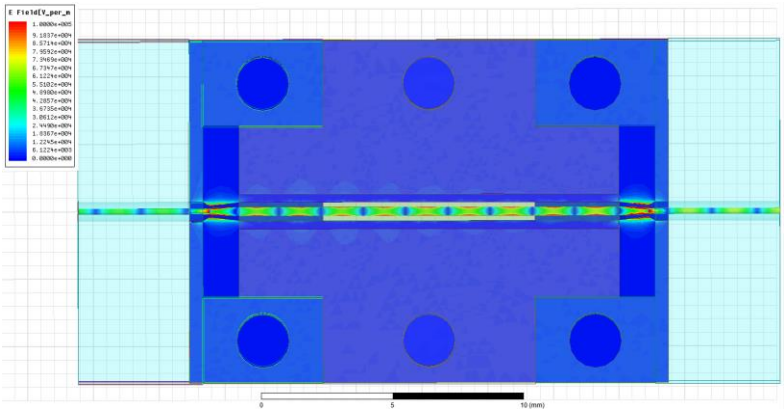


(b) $\frac{W_{taper2}}{W_{strip}} = 0.67$ (50Ω by TDR)

Fig.65 60GHz Field Distribution in Dielectrics of the LC-based ECPW Phase Shifter (Top View)



(c) $\frac{W_{taper2}}{W_{strip}} = 2.64$ (50Ω by TLM)



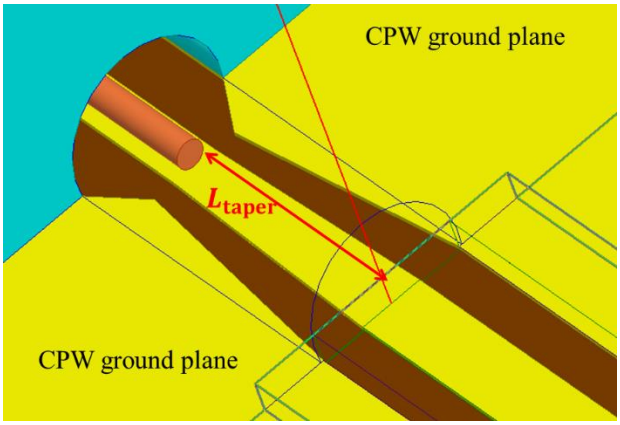
(d) $\frac{W_{taper2}}{W_{strip}} = 0.67$ (50Ω by TDR)

Fig.66 60GHz Field Distribution in Metals of the LC-based ECPW Phase Shifter (Top View)

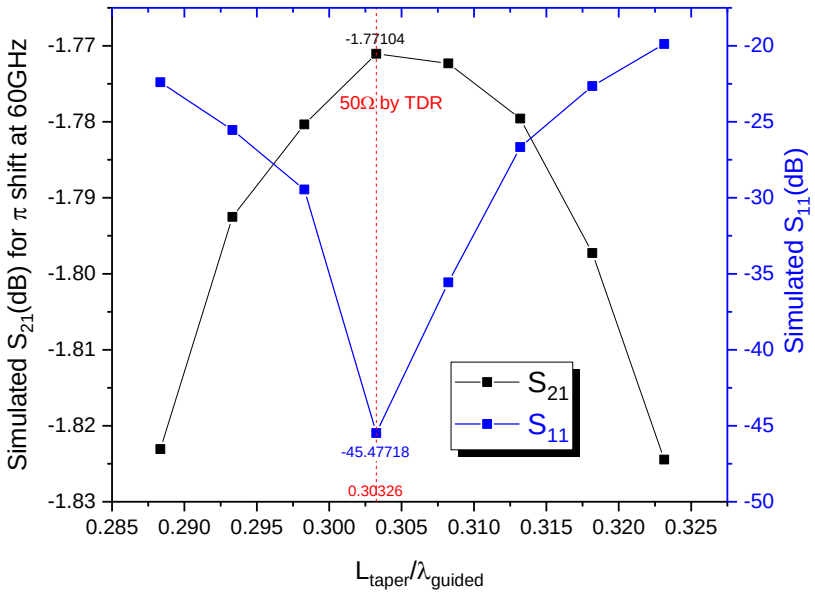
We conclude that the edge of the PCB's core line should start in a relatively narrow profile (based on a smooth geometrical transition between different polarisations) rather than a wide profile (based on the inaccurate infinitely-long transmission line assumption) to minimise the discontinuity reactance. The optimal width of the core (W_{taper1}) at the PCB edge is calculated as 0.92 times the internal diameter (*I.D*) of the coaxial connector's inner conductor (the connector core section prior to the launch pin), i.e. W_{taper1} =0.92 *I.D.* =0.21mm, and W_{taper2}= 0.67W_{strip}=0.196mm.

5.4.2.3 Design of the Taper Length

We have derived the optimised taper's cross-sectional geometry by TDR method. Based on this, the taper length L_{taper} denoted in Fig.67 (a) below affects the transient impedance as well as the additional loss due to undesired coupling between the connector pin and the enclosure as illustrated previously in Chapter 5.2. The coupling is also a higher-order mode that merits mitigation.



(a) Sketch of the Taper's Length to be Optimised



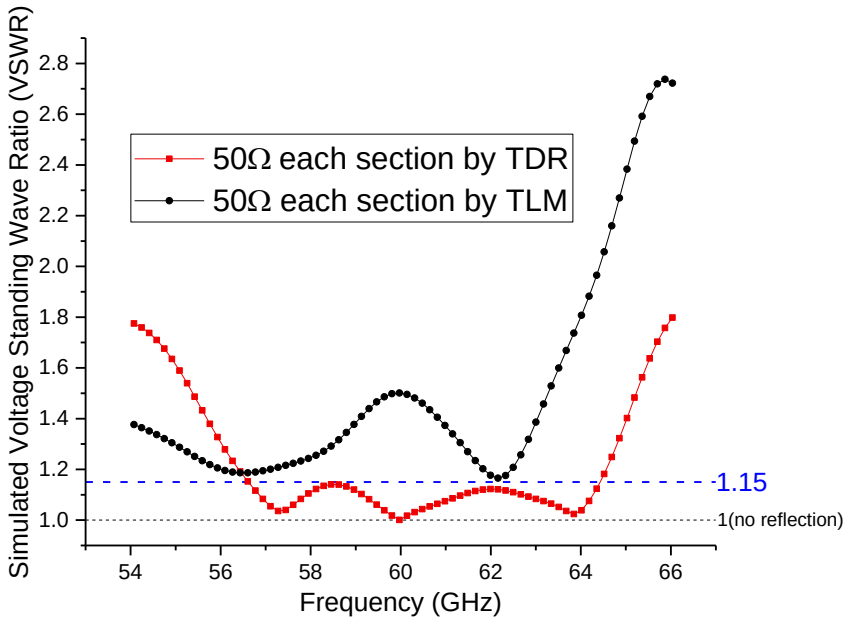
(b) Simulated Return and Insertion Losses vs. Relative Taper Length at 60GHz

Fig.67 Optimising the Length of the Taper based on Time Domain Simulation

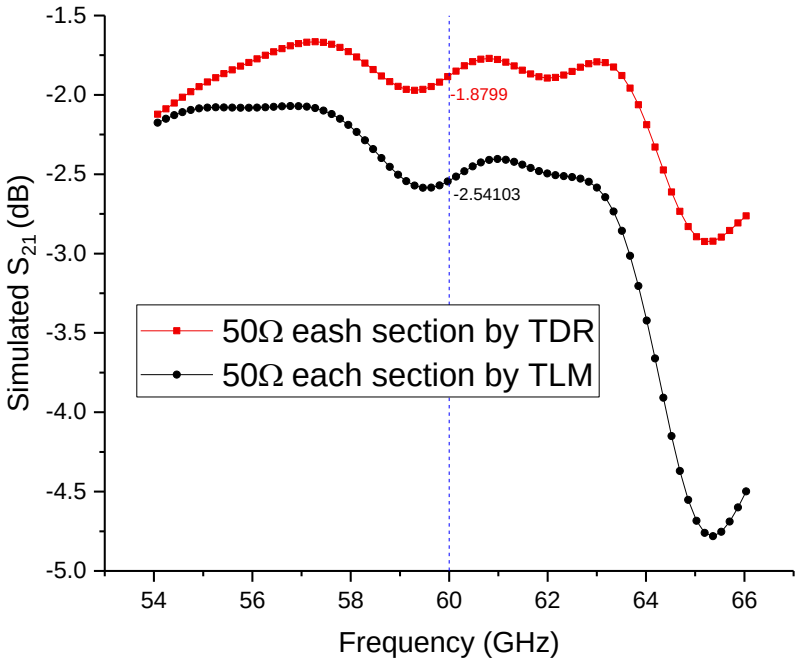
By parametrising the *S*-parameters versus L_{taper} in Fig. 67 (b) above whilst keeping other parameters constant, we derive that the optimal length of the taper is $\frac{3}{10}$ of a guided wavelength, where the reflection loss and insertion loss are both minimised. Summarisingly for 60GHz, the optimal core line shape at the PCB edge is with W_{taper1}*=0.21mm*, W_{taper2}*=0.196mm* and L_{taper}*=1.22mm*, with CPW slots spacing tapered accordingly for a smooth transition into the optimised tunable part derived in Chapter 4.

5.4.2.4 Simulated Wideband Performance of Phase Shifters Matched by TDR vs. TLM

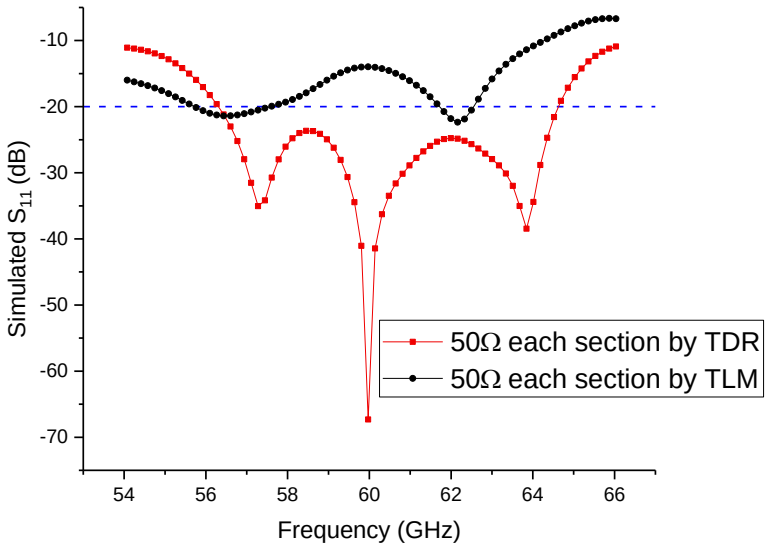
Based on the 60GHz optimised design derived above, the dispersion of the interface structure is examined. The obtained 50Ω-optimised structure based on TDR is compared with that by TLM across 54GHz-67GHz as reported in Fig.68 below, concerning the voltage standing wave ratio (*VSWR*) and insertion loss.



(a) Simulated Voltage Standing Wave Ratio (VSWR)



(b) Simulated Insertion Loss



(c) Simulated Return Loss

Fig.68 Time-domain Simulation of LC-based ECPW Phase Shifter (Connectors Included): Designs based on Connector-PCB Interface Matched by TDR vs. TLM

The structure matched by TLM exhibits a *VSWR* above 1.15 across the whole spectrum (54GHz-67GHz), while the TDR one achieves a VSWR within 1.15 across 57GHz-65GHz. By TDR optimisation, impedance of every section is well matched at 60GHz (S_{11}= -67dB). Compared with that obtained by TLM method, S_{21} improves considerably, from -2.54dB to -1.88dB. Insertion loss due to the interface structure is significant if there is a substantial variation in impedance. We quantify the transient impedance versus time in Fig.69 below and interpret the results in the next section (5.4.2.5).

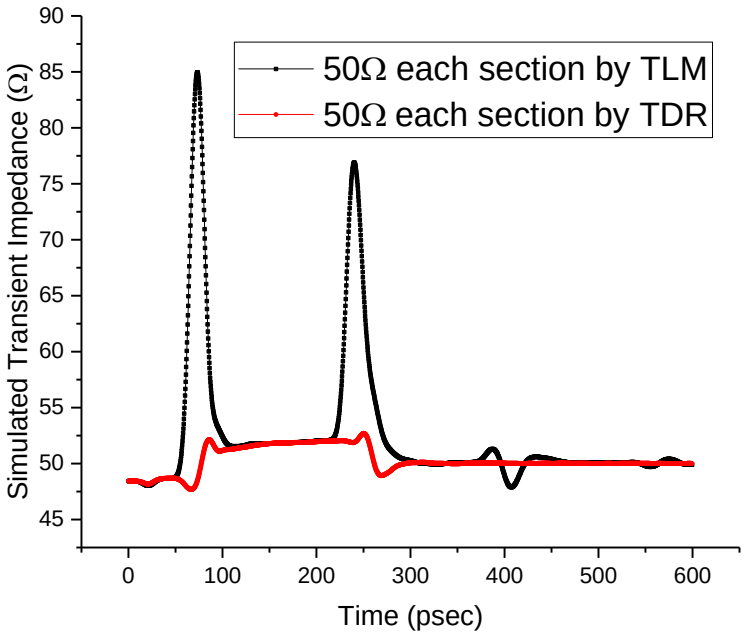


Fig.69 Simulated Transient Characteristic Impedance versus Time for the LC-based ECPW

5.4.2.5 Interpretation of the Transient Impedance vs. Time

To interpret the correlation between the transient impedance and time as shown in Fig.69 above, the electrical length estimated in section 5.4.1 is used. The times in the *x*-axis link to the distances from the input observation terminal (i.e. the round-trip of the signal from the input terminal to a discontinuity and bouncing back), as well as considering the rise time (t_0=20psec) of the input signal.

Table.8 Correlation of Time, Geometry Discontinuity, and Transient Impedance

Interpreting Transient Impedance	**TLM Design**	**TDR Design**
Rise time t_0	t_0=20 psec, $Z_{coax\ connector}$=48.4 Ω	
Connector transition dielectric Δt_{teflon}	Δt_{teflon}=15 psec	
1st inductive spike at t_{peak1}	t_{peak1}=73 psec, Z_{peak}=85 Ω	t_{peak1}=87 psec, Z_{peak}=52 Ω
Tunable dielectric Δt_{LC}	Δt_{LC} = 60 psec	
2nd inductive spike at t_{peak1}	t_{peak2}=240 psec, Z_{peak}=69 Ω	t_{peak2}=250 psec, Z_{peak}=52.7 Ω

As summarised in Table 8 above, the transient impedances of both designs both start with 48.4Ω for the coaxial connector's cross section. A small capacitive dip at *t*=20psec indicates the signal has gone through the rise time and starts to travel from the transition block. The first inductive

spike both begin at *t*=50psec, indicating the signal spends 15psec to arrive at the first discontinuity, i.e. the coaxial-to-PCB interface.

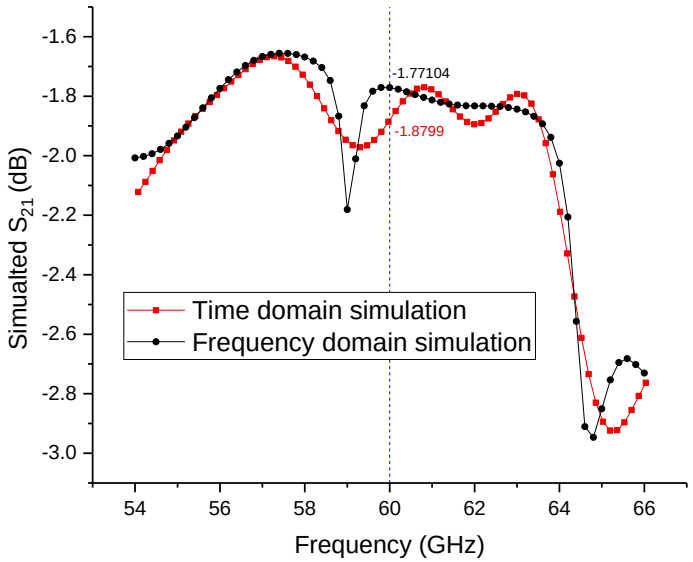
Note the difference in the time where the peak spike happens due to the difference in the wave speed, the TDR one exhibits a slow-wave effect. The peak of the inductive spike occurs at *t*=87psec for the TDR one (while *t*=73psec for the TLM one), indicating another 18.5psec for the signal to travel through the PCB transition part (tapered core), reaching the second discontinuity, i.e. interface between the joint and the tunable part. Then it takes 60psec for the signal to go through the tunable ECPW transmission line with LC as estimated, and reaches the interface between tunable part and non-tunable parts at the output side. Note the slope of the curve, the transient impedance increases slightly with time owing to the loss of the transmission line.

For the TLM one, there is a third spike and dip happening after t=370psec corresponding to the bouncing back and forth of the reflected power from the output terminal. These oscillations are due to residual fields undergoing multiple reflections between discontinuities before reaching the input terminal. For the TDR one, the residual reflected power is too weak to be observed.

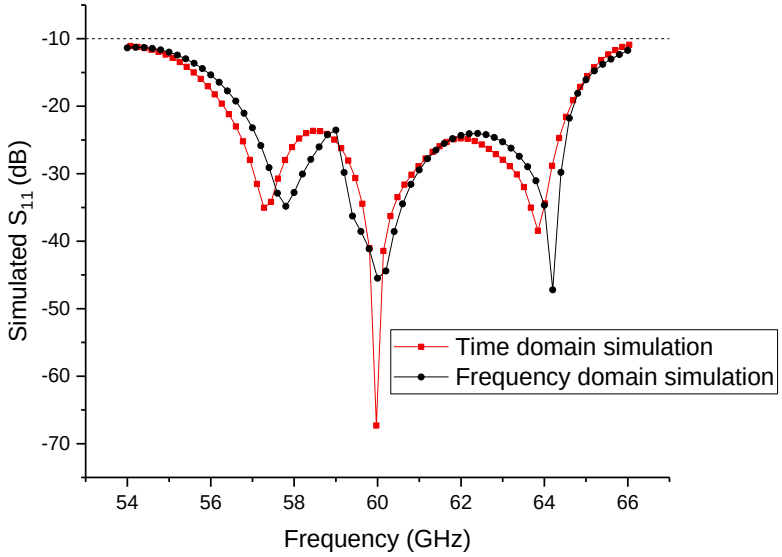
In conclusion, we have theoretically confirmed by time domain simulation the optimised taper geometry matched by the TDR method, i.e. geometrically continued with the inner diameter (*I.D.*) of the connector, and smoothly transitioning to the tunable part's core line (W_{strip}).

5.5 Benchmarking the 50Ω-transition Structure Optimised by the Proposed TDR Method in Frequency Domain

Optimised by the proposed TDR method, the 50Ω transition structure is benchmarked in frequency domain based on an identical adaptive meshing precision. As demonstrated in Fig.70 below, the simulation results by frequency domain and time domain show reasonably good agreement in statistics across 54GHz -67GHz, with the difference in S_{21} largely within 0.1dB.



(a) Simulated Insertion Loss by Time Domain vs. Frequency Domain



(b) Simulated Return Loss by Time Domain vs. Frequency Domain

Fig.70 Benchmarking the Optimised LC-based ECPW Phase Shifter Design in 2 Domains

The high insertion loss spike predicted by simulators at 59GHz is owing to the meshing inaccuracy for irregular configurations. The degradation in transmission (drop in S_{21}) at about 63GHz indicates the onset of a higher-order stray mode, which is potentially damaging for applications that are supposed to transmit narrowband signals around this moding regime. Benchmarking HFSS (Finite Element Method) against CST (Finite-Difference Time-Domain Method), the reasonably good agreement largely within statistics confirms the validity of the proposed LC-based ECPW phase shifter model.

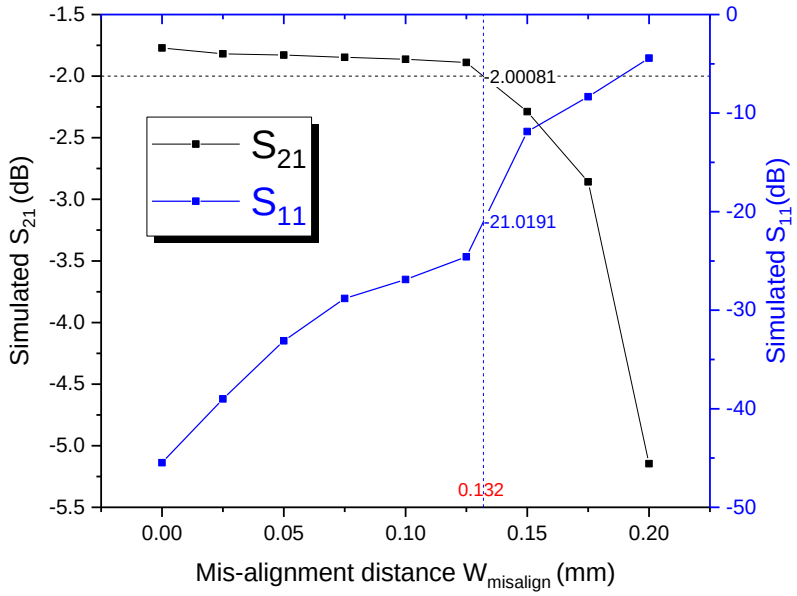
In a summary, this work includes 1.85mm connectors in the simulation for the whole-device impedance matching. This is an important part for lower loss and the work itself is challenging because of the irregular nature of the connection region. By full-wave numerical simulations and benchmarking designs based on time-domain reflectometry (TDR) against the conventional infinitely-long transmission line model (TLM), we observe inconsistency in the estimation of the joint's transient characteristic impedance. To experimentally verify the TDR method instead of conventional TLM one, two designs based on these methods respectively are fabricated and measured, as compared later in section 7.1.1.

5.6 Device Simulation Incorporating Fabricating Tolerances

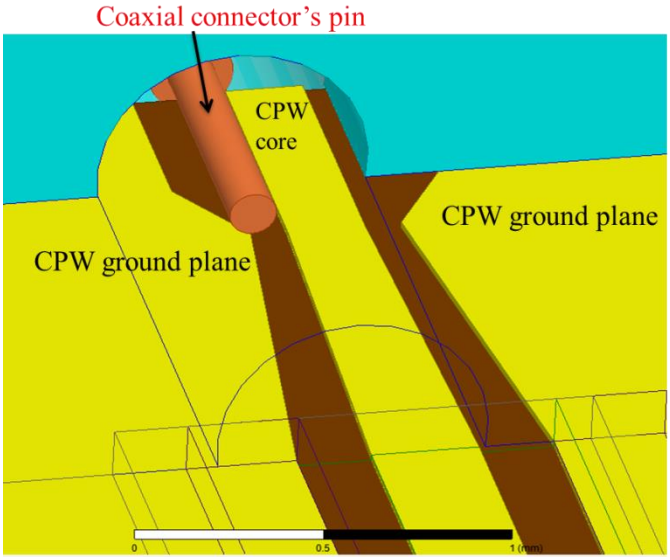
To ensure that the fabricated device can function as designed, insertion loss's sensitivity to the following manufacturing tolerance should be considered.

5.6.1 Impact of Connector Misalignment on Insertion Loss

Impact of connector misalignment on insertion loss is simulated and reported in Fig.71 below. The misalignment here is defined as the distance (position error) of the connector launch pin's centre deviating from the CPW's core centre.



(a) Simulated Sensitivity of *S*-parameters to Misalignment of the Connector Pin



(b) $W_{misalign}$>0.225mm (Short Circuit Malfunction)

Fig.71 Impact of Connector Pin Misalignment on *S*-parameters (0V bias, 60GHz)

From the signal integrity point of view, Fig.71 (a) above shows that misaligning the connector by up to 132μm is acceptable for the S_{21} degradation (by 0.5dB), although the return loss keeps rising with the misaligned distance, it is still well below -20dB and hence not a big deal for insertion loss increase. With the increase of the misaligning distance exceeding this tolerable distance, the return loss begins to make a difference, as evidenced by the sharp drop of the S_{21} by 3.5dB, when the connector's core pin is almost in touch with one of the CPW's ground planes as shown in Fig.71 (b), resulting in malfunctioning of the whole circuit.

According to the mechanical tooling tolerances as specified in section 2.2.5, the maximum tolerance of the screwing position (0.15mm due to the drilled holes' diameter error and position error combined) should be smaller than the slot spacing (W_{gap}) to avoid connector's core shorting with one of the CPW's grounds. In other words, the PCB edge's core-to-grounds spacing W_{gap} is designed sufficiently large to allow for this. For the same reason, the enclosure's cavity width is designed to reserve for the M2 screwing mounting position tolerance to avoid a short circuit between CPW's core line and the enclosure's sidewalls. In conclusion, the PCB edge (connector-to-PCB interface) design is a compromise between impedance matching (by minimising abrupt diametrical changes) and the ease of assembly (considering fabrication tolerances).

5.6.2 Impact of Alignment Layer on Insertion Loss

The polyimide film rubbed on the gold-plated PCB (for surface anchoring of LC) can block the grounding path by increasing the contact resistance. Depending on the thickness of the alignment film, the contact resistance due to this can disrupt the desired ECPW mode due to the imperfect grounding as mentioned in section 2.6.2. The blocking effect for the whole device is simulated at 60GHz under 0V bias, with the results shown in Fig. 72 below.

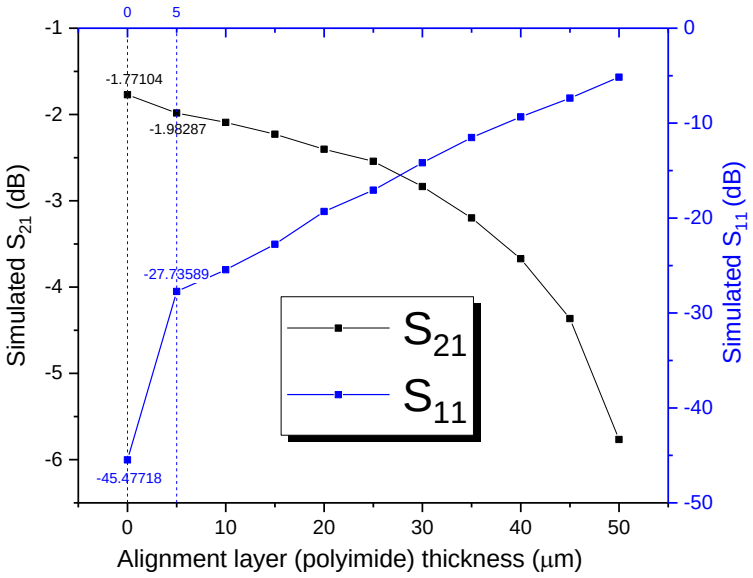


Fig.72 Simulated Impact of Polyimide Alignment on Insertion Loss at 60GHz

By experiment in Chapter 6.2, we obtain the spin-coated alignment film to be only 60nm. By simulation in Fig.72 above, the polyimide layer only adds less than 0.1dB to the insertion loss. Therefore, it is predicted that deployment of alignment layer exhibits only minor impact on the return loss and insertion loss, and hence will not cause a concern for device degradation if the fabrication is carefully performed (detailed in Chapter 6). Other fabrication tolerances (e.g. etching rate, gold-plating thickness) obtained via experiments (Chapter 6) are considered for design optimisation (Chapter 7.2) accordingly.

Chapter 6. Device Fabrication and Experimental Setup

Having progressed from design and simulation in previous chapters, this chapter reports on device making, with critical steps outlined below in Fig.73.

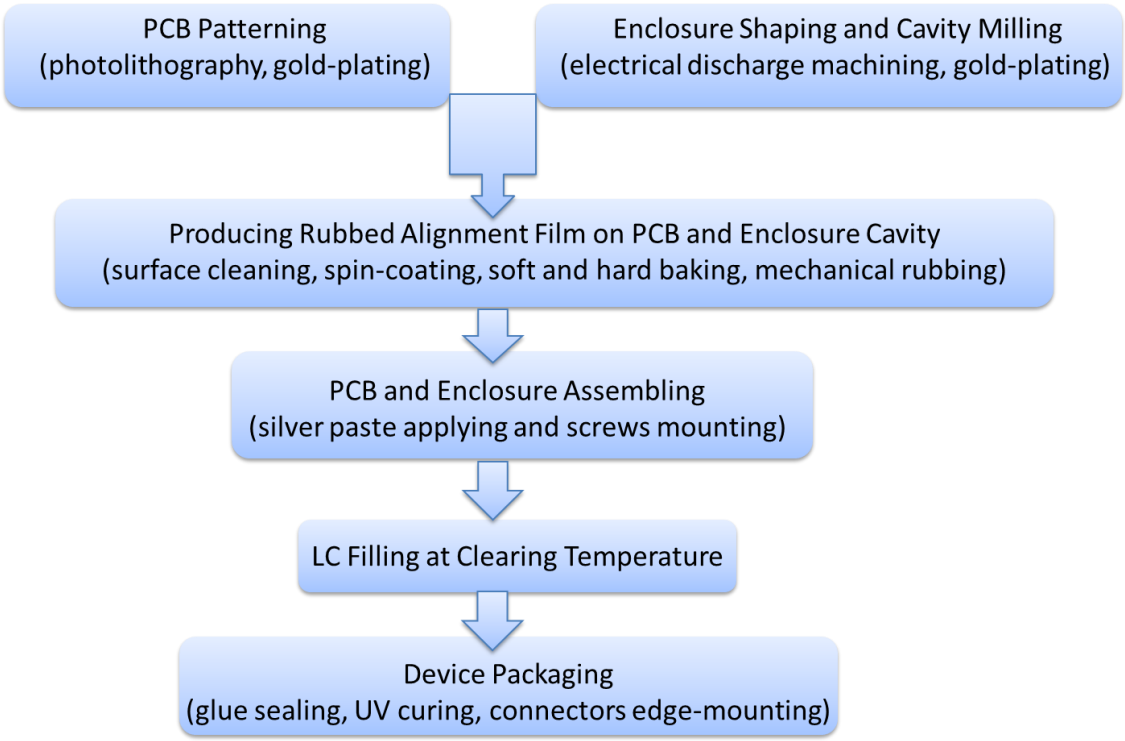


Fig.73 Flowchart of the Device Making Process

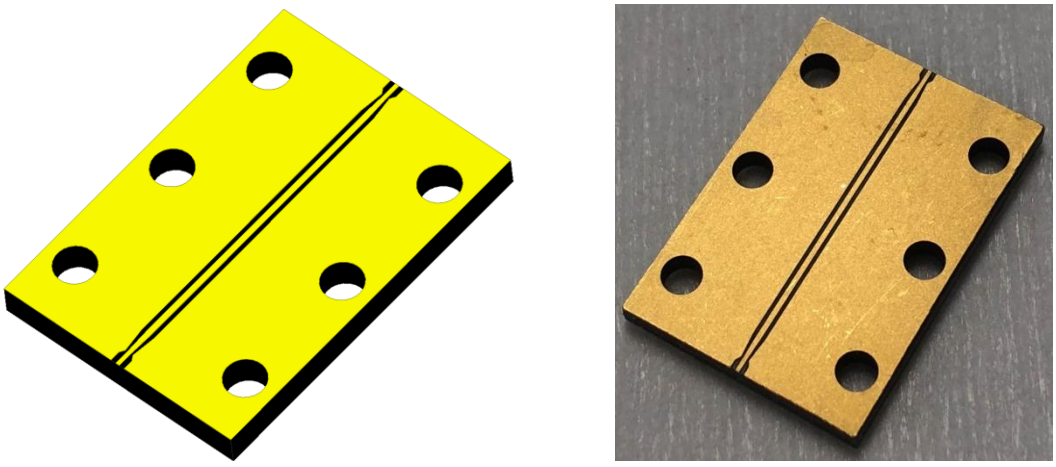
To ensure that the fabricated device can function as designed, a lot of attention is paid to electrodes patterning (Chapter 6.1) as well as cleanroom techniques for substrates processing (Chapter 6.2) and device assembly (Chapter 6.3).

6.1 Electrodes Patterning and Substrates Shaping

Prior to fabrication, commercially available PCB materials (Cu foil laminated on a PTFE substrate panel) are purchased from Rogers Corporation. Pure Cu plates of grade C101 stocked in the workshop are prepared. Device fabrication work begins from substrates shaping, which includes Cu-patterning on PCB substrates to produce a CPW circuit (section 6.1.1), machining of C101 Cu to form a cross-shaped enclosure with a cavity to accommodate LC (section 6.1.2), and surface finishing of these substrates by gold-plating (section 6.1.3).

6.1.1 PCB Engraving by Photolithography

Electrodes of the CPW are photolithographically engraved on 0.5oz Cu clad (thickness=17μm) laminated on 1.575mm-thick RT/duroid 5880 substrate cut into various dimensions. The width of the PCB is chosen as 12.7 mm to be compatible with all brands of 1.85mm connectors. M2 screw holes with a quantity of six are drilled mechanically (for device assembly later). Fig.74 (a) (b) show the designed PCB and the fabricated one (with gold finish), respectively.



(a) (b)

Fig.74 (a) Designed PCB for Photolithography, and (b) the Fabricated One (gold-plated)

The optical lithography is based on an image reversal photoresist AZ-5214E processed in a positive tone, i.e. enabling the resist at unmasked traces exposed to UV light and being easily dissolved in a developer (AZ-351B), thus unwanted Cu at those areas can be wet-etched away by diluted Ferric Chloride ($FeCl_3$). The process is akin to that of the Fresnel lens array I fabricated for photon sieve devices [55]. They differ in detailed recipes catering for different conductors and substrates. Detailed manufacturing steps are summarized as follows.

First, a clear-field (positive) photomask is designed to present multiple opaque line traces (targeted for core line and ground electrodes on the CPW substrate), and transparent line traces (aimed for gaps to be etched between the core line and grounds). The traces are designed in various sizes to verify various design concepts, with manufacturing tolerances specified in Chapter 2.2 considered (e.g. cavity depth tolerance and hence LC thickness control). Size information of multiple designs are detailed in Appendix. CAD drawing of one PCB design of

the size 18.284mm × 12.7mm × 1.575mm is illustrated in Fig.75. The designed chromium-coated photomask is fabricated by e-beam lithography.

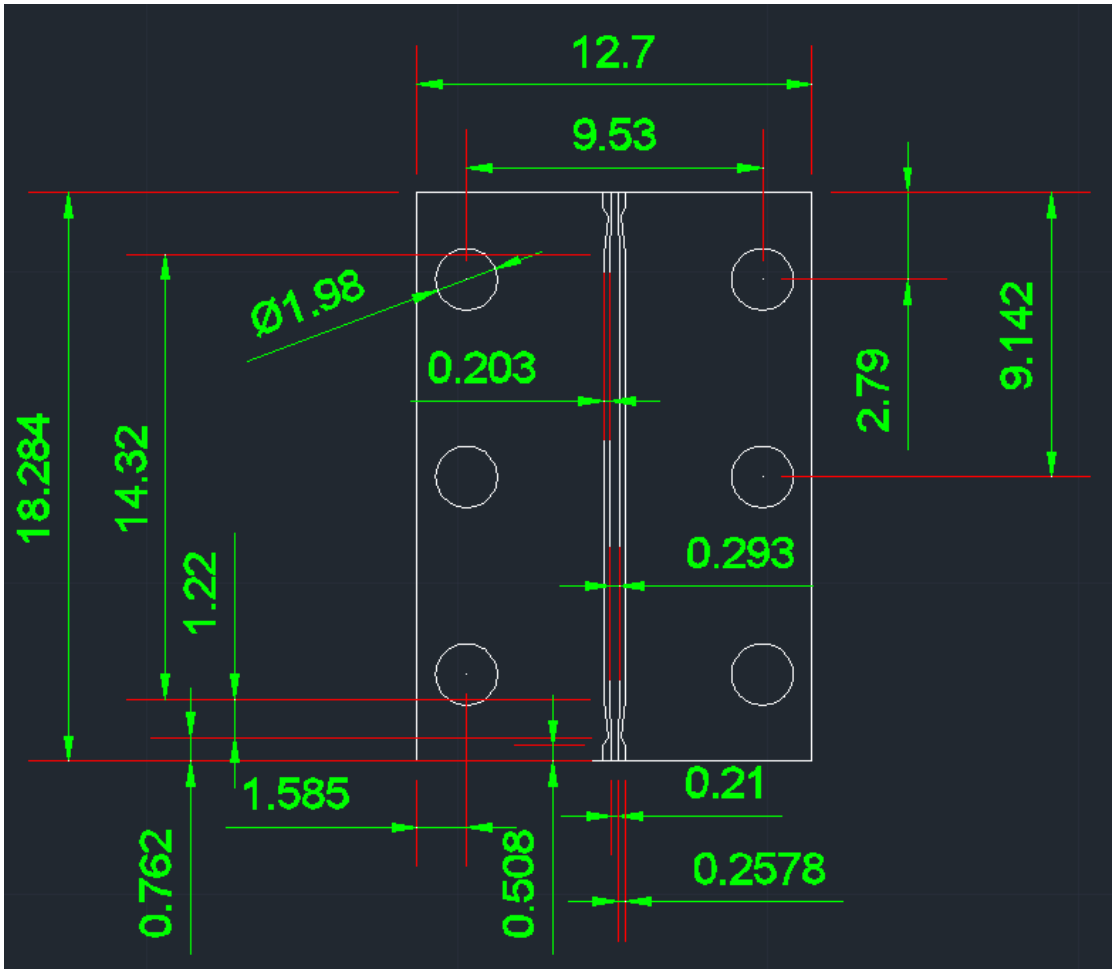


Fig.75 Photomask Design with Size Annotation (Units are in mm)

Configuration of the core and the adjacent grounds traces can be described as five sections (Table 9), with the core width tapering from 0.21mm to 0.293mm. The minimum feature size is 100μm, which is the spacing between core and grounds between section 1 and 2 (or between section 4 and 5 as the design is symmetric).

Table.9 Geometry Details of a PCB Design (for π Phase-Shifting)

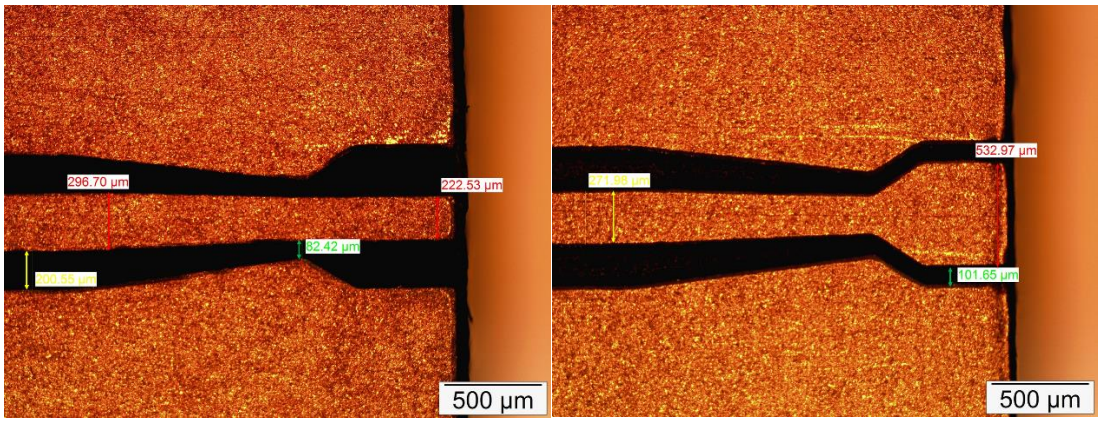
Section	Center Trace Width (mm)	Length (mm)	Gaps Spacing (mm)
1	0.21	0.762	0.2578 tapered to 0.1
2	0.21 tapered to 0.293	1.22	0.1 tapered to 0.203
3	0.293	14.32	0.203
4	0.293 tapered to 0.21	1.22	0.203 tapered to 0.1
5	0.21	0.762	0.1 tapered to 0.2578

UV lithography is performed to transfer the patterned mask structure to the PCB. The patterning procedures and conditions are given as follows. Prior to photoresist coating, the 5880 substrate is first ultrasonically cleaned with acetone and Isopropyl Alcohol (IPA) sequentially (each for 5 minutes), rinsed in deionized (DI) water, and then dehydrated on a hotplate at 90˚C for 3 minutes. A 1.4μm-thick layer of AZ-5214E photoresist is spun on the substrate with 4000rpm for 30 seconds. To evaporate the coating solvent, the substrate is then pre-heated (soft-baked) on the hotplate at 90˚C for 1 minute and placed at room temperature for 5 minutes.

Subsequently, the substrate is exposed on a UV light source for 5 seconds, and then developed in AZ351B (1:4 diluted in DI water) for up to 3 minutes until the pattern becomes visible. The exposure time, development time and the soft-bake temperature mentioned above have been optimised for a sufficient radiation dose and a controllable dissolution rate, whilst inspecting feature sizes of the patterned photoresist under microscope against the design value.

The substrate is then hard-baked on the hotplate at 120˚C in 2 minutes for polymerisation of the resist. The post-baked substrate is put into a Ferric Chloride ($FeCl_3$) solution (50g $FeCl_3$ etch pearls and 100mL water) on a hotplate at 50˚C for etching in 6 minutes. The $FeCl_3$ concentration, etching temperature and time have been optimised by adjusting etching rate for minimum dimensional shrinkage of the PTFE substrate as well as minimum surface roughness of the Cu film (top side). The unexposed photoresist layer is finally stripped by acetone, followed by postprocess cleaning. As mentioned in Chapter 4.3, the thermal expansion coefficient mismatch between Cu clad and 5880 substrate creates cyclic internal stress on the clad when the sample is subjected to fluctuating temperatures. The post-etch stress relief is investigated for our CPW pattern by measuring the substrate's flatness.

The fabricated patterns are well shaped and sized as observed in Fig.76 below for designs matched by time domain reflectometry (TDR) and infinitely-long transmission line model (TLM). The measured core line's width exhibits an error of 3μm (1% difference) as compared with the designed value. Measured cross section of the post-gold-plated conductor profile is reported in section 6.1.3. Undercut is minimised by tight control of the etch time.



(a) Interface Matched by TDR (b) Interface Matched by TLM

Fig.76 Fabricated PCBs with Diverse Interface Patterns based on 2 Matching Mechanisms

6.1.2 Enclosure Machining by Wire Erosion

5mm-thick C101 Cu plate is firstly machined with four edges cut in the local workshop. On the polish side of the cross-shaped sample, a cavity of 140µm in depth and 1.3mm in width is subsequently engraved centrally between mounting holes, as shown in Fig.77 below. The manufacturing method here is electrical discharge machining (EDM), also known as wire erosion, i.e. a copper electrode mold is installed in the EDM machine and shapes the workpiece by creating sparks that melt tiny portions of the C101 sample progressively until the desired 140µm depth is reached.

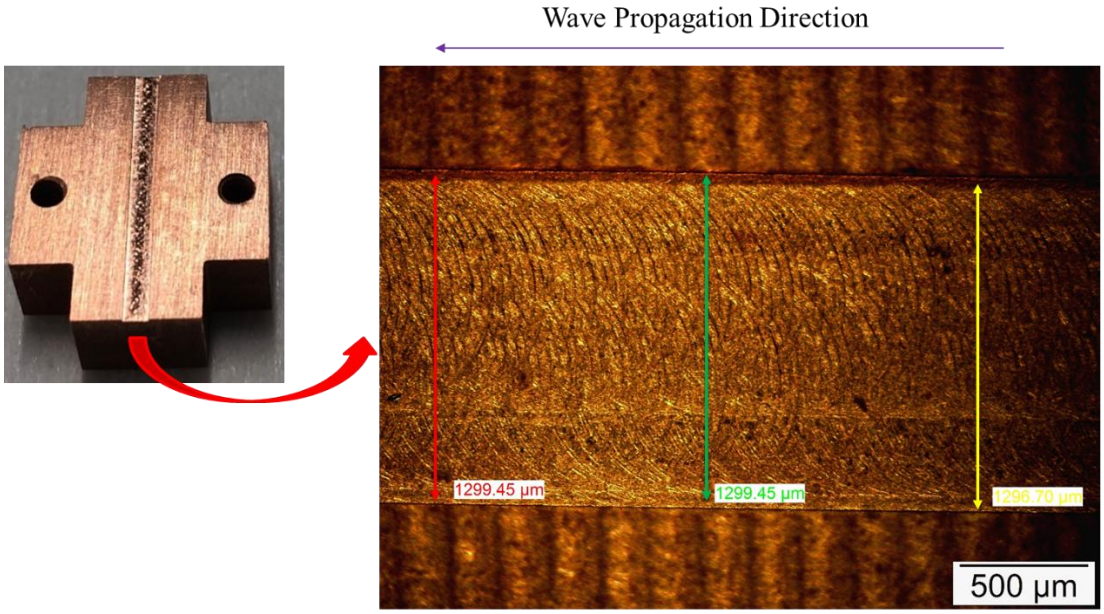


Fig.77 Post-Machining Measurement of the C101 Cu Enclosure

As measured under a microscope, the machining error of the engraved cavity width is -1.6μm, whilst the error of the cavity depth due to overburnt has been tightened within the range of ±5μm. The depth tolerance has been considered at the design stage (refer to section 5.6 for LC-thickness tolerance simulation).

Two problems arise with C101 bare Cu. First, Cu oxidizes quickly, which is accelerated by the process of alignment agent baking. Second, if nylon and formic acid is used for alignment agents, formic acid is highly corrosive to Cu. To address these, we do PCB finish with gold-plating (see the following section) and replace nylon and formic acid with polyimide (covered later in section 6.2.1).

6.1.3 Gold-plating and Conductor's Profile Measurement

The post-patterned Cu-based substrates (PCB and enclosure) are surface-finished with gold by a standard electrolytic process. The plating is nickel-free to minimise conduction loss at 60GHz. The screwing holes of the PCBs are masked during the plating process to tighten the position tolerance of screws and avoid undesired metal vias generation.

The thickness of gold-plating is experimentally investigated for reliable protection without degrading the conductor performance after the 200˚C baking process (for evaporating the solvent of the coated alignment agent on the substrate, which is discussed in more depth in section 6.2.1). Different thicknesses of gold-plating (from 0 to 3μm) are performed for a group of CPW substrates with 0.5oz Cu foil (thickness=17μm). The gold-plated PCB surface at room temperature is shown in Fig.78 below.

(a) non-plated Cu (b) 50nm gold-plated (c) 2μm gold-plated

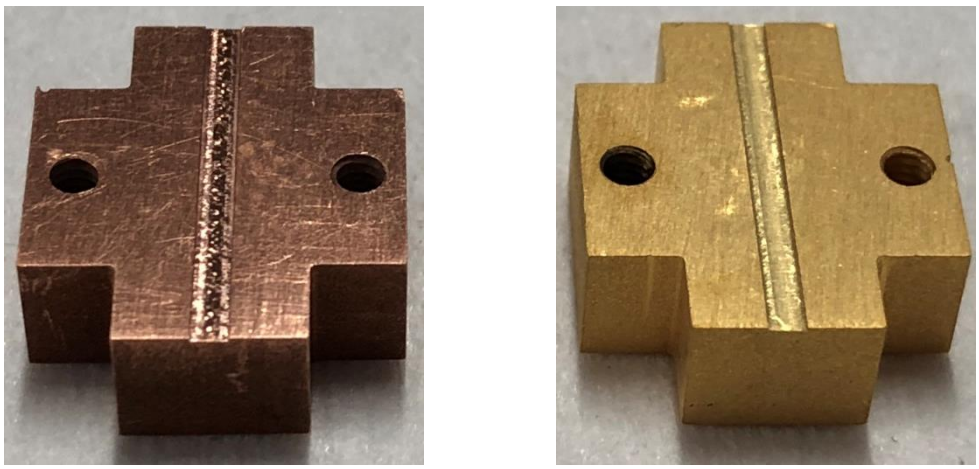
Fig.78 PCBs of Different Gold-plating Thicknesses at Room Temperature

After 200˚C baking for 20 minutes, the same groups of substrates are inspected again, with their profiles shown in Fig.79 below.

(a) non-plated Cu (b) 50nm gold-plated (c) 2μm gold-plated

Fig.79 PCBs of Different Gold-plating Thicknesses after 200˚C Baking for 20 mins

The coating of polyimide as alignment agent cannot deter the bare Cu from oxidation (see both Figs.79 and 80). For 50 nm gold-plating on Cu, tarnishing occurs as Cu atoms migration into gold during the 200˚C heating. This is an irreversible process, which still raises a problem with Cu oxide layer formation.



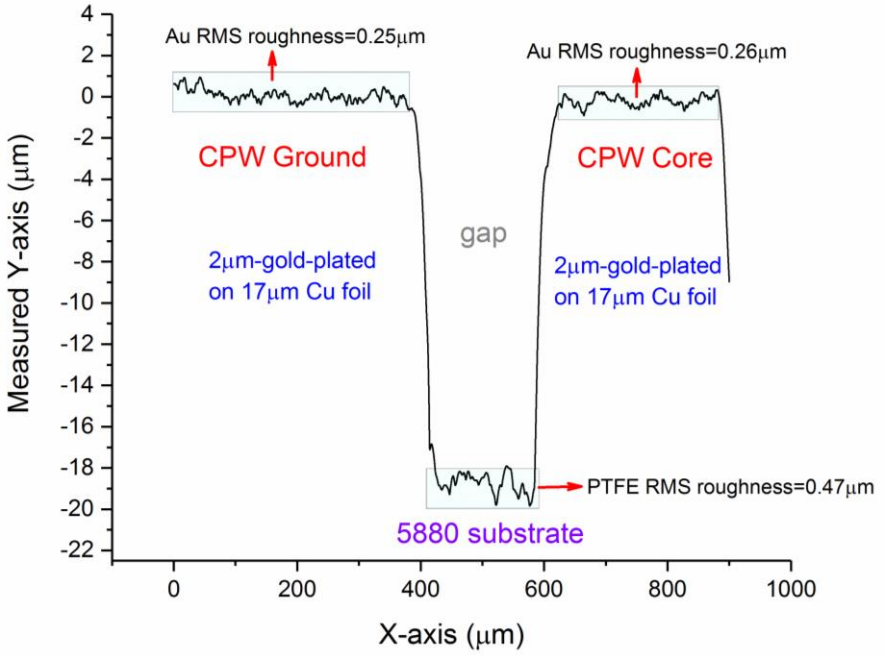
(a) non-plated Cu (Oxidised) (b) 2μm gold-plated

Fig.80 Enclosures after 200˚C Baking: Pure Cu (Oxidised) vs. with Gold-plating

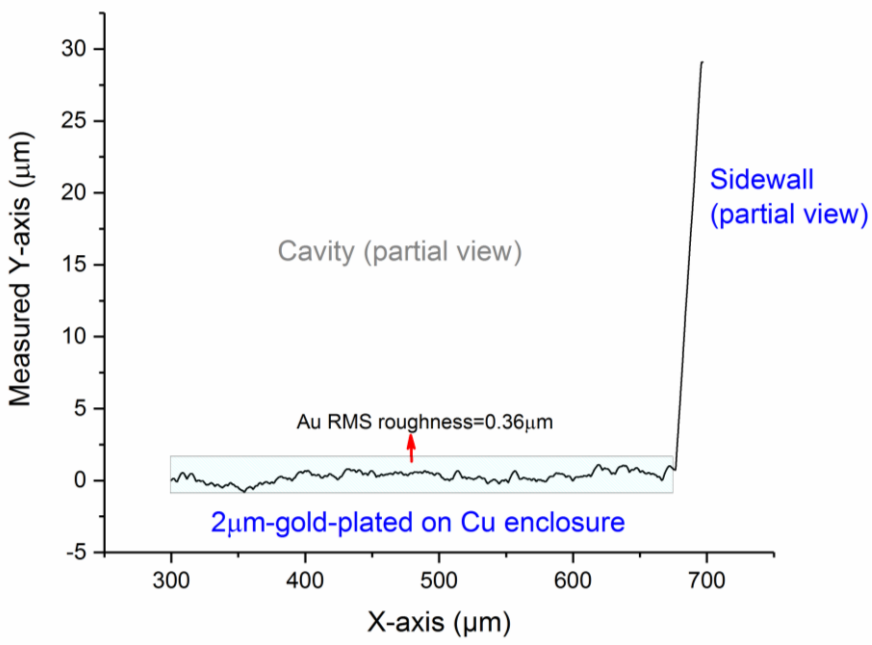
At DC and low frequency, skin depth is so huge that Cu underneath the oxide layer still conducts current. At 60GHz, skin depth is comparable to the oxide layer, Cu oxidation and migration into gold (tarnishing) dramatically increases resistance, which raises the need for gold-plating with adequate thickness. By experiment, the optimal plating thickness for best

environmental protection without degrading insertion loss is 2-3μm. Beyond this thickness, the cross-sectional profile of the added gold exhibits substantial error due to the resolution of electroplating.

To delve into the conductor's cross section profile after gold-plating, Veeco Dektak 150 profilometer (with stylus radius of 12.5μm) is used to scan the hills and valleys of the CPW as well as the enclosure cavity, with measured statistics enclosed in Fig.81 (a) and (b), respectively.



(a) Measured Cross Section of the Gold-plated CPW Substrate



(b) Measured Cross Section of the Gold-plated Enclosure

Fig.81 Dektak Surface Profiler Measuring Gold-plated CPW Substrate and Enclosure

Standard deviation analysis shows that root-mean-square (RMS) roughness of the gold-plating (2μm-thick) surface is 0.26μm for the CPW core and 0.25μm for the CPW ground plane. Such plated gold smoothness outperforms most documentation with 0.4-0.5μm of RMS roughness reported. To recapitulate from section 4.3.3 that Cu penetration depth at 60GHz is 0.26μm. The reduction of core conductor's roughness from 0.4μm to 0.25μm is expected to significantly mitigate metal loss due to skin effect, as verified by S-parameters measurement covered in Chapter 7. The gold-plated enclosure's central cavity exhibits a rougher surface (0.36μm RMS roughness) than that of the PCB, due mainly to uncertainty of plating inside a 140μm-depth cavity. This smoothness is reasonably good and exhibits minor concern for device performance as the ground metal loss accounts for a much lower portion in the total metal loss as compared with that of the core line due to non-uniform distribution of electric field intensity.

Note that the RMS roughness of the post-etched bottom surface of the gap is 0.47μm. This characterises the roughness of the lay-up of Cu foil and 5880 PTFE substrate, which is two times higher than that of the conductor's top side. Such an increase in roughness is intended to enhance the bonding strength, as mentioned in section 4.3.3. To measure the impact of the laminating interface's roughness on insertion loss, S-parameters of devices based on two types of Cu foils (i.e. Electrodeposited (ED Cu) vs. rolled annealed (RA Cu)) are measured respectively and reported in Chapter 7. Post-etch substrate shrinkage and gold-plated Cu pattern distortions are quantified by comparing the measured trace width and gap spacing to the design values as shown in Table 10 below.

Table.10 Dimension Measurement of the Patterned Features

Fabricated Components	Designed (μm)	Measured (μm)	Difference
CPW core line width	293	274	-6.4%
CPW gap spacing	203	171	-15%
Enclosure cavity depth	140	135	-3.4%

The post-etched and gold-plated core line is 6.4% narrower than the designed width. The implications on device performance are return loss variation (due to increased characteristic impedance), and a decrease of differential phase shift (due to reduced wave-occupied-volume in tunable dielectrics). Moreover, the 15% narrowing of the CPW gap spacing confirms the PTFE substrate shrinkage due to mismatch in coefficient of thermal expansion coefficient

aforementioned in section 4.3.1. Based on this fabrication tolerance due to etching and gold-plating, CPW designs are optimised accordingly by increasing core line width slightly and increasing the gap spacing sufficiently to reserve for the post-etch gap shrinkage and pattern distortions.

The above measurements for conductors' top surface and cavity's bottom surface are in reasonably good accuracy. However, surface roughness measurement is almost bypassed for conductors' sidewalls, resulting in a smooth representation, as shown above in Fig.81 (a) and (b). A limitation of the above stylus-based surface measurement lies in incapability of measuring the high aspect ratio sidewalls (the steep transition part from hill to valley, or from valley to hill). This is because of the geometry of the stylus, which terminates in a radius of 12.5μm. As illustrated in Fig.82 below, the roughness of conductor's height (19μm for CPW's gap after plated, and 142μm for enclosure's cavity) is filtered out.

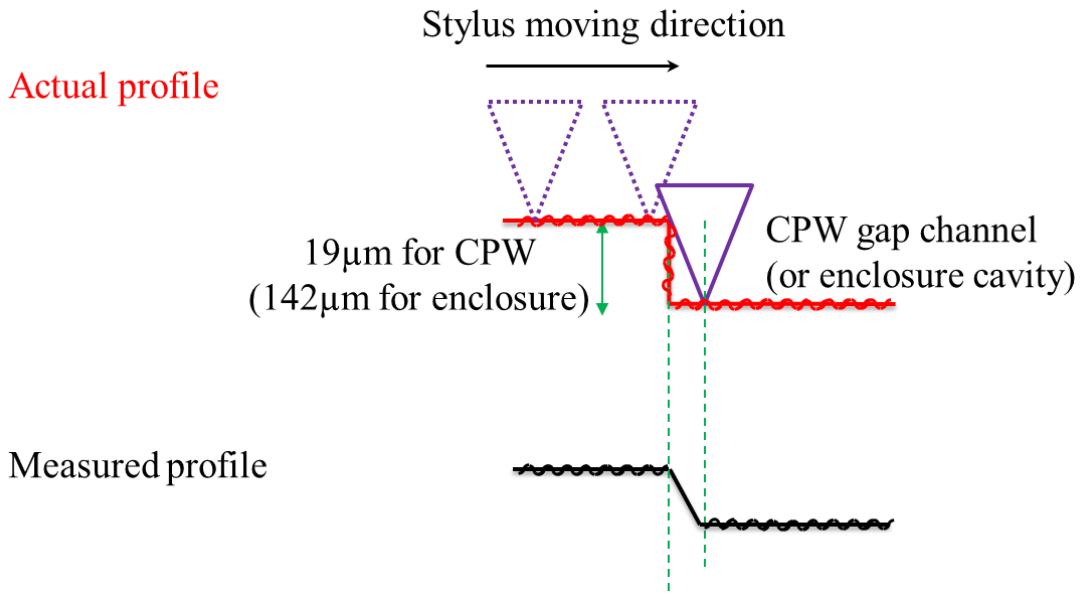


Fig.82 Interpretation of the Limitations of Dektak in Measuring the Surface Roughness

In a summary, the low-cost chemical etching and standard electroplating achieve reasonably good accuracy for the electrically-critical circuit traces of our proposed ECPW structure.

6.2 Creating Rubbed Alignment Layers for Surface Anchoring

The patterned substrates are then coated with an alignment layer and mechanically rubbed to anchor LC for a targeted orientation. Substrates alignment and device assembling are performed using the local facilities in the Class 100 cleanroom located at the Centre for Advanced Photonics and Electronics.

Prior to deposition of alignment agents, ultrasonic cleaning is applied to both substrates (gold-plated PCB and enclosure). Acetone and Isopropyl Alcohol (IPA) are used sequentially as the cleaning solvents in an ultrasonic bath. To avoid marks of residual solvents tarnishing the LC and hence affecting the electrical performance of the device, the post-dipped substrates are immediately vapour-degreased and dried using an IPA dryer (evaporator) for 10 minutes, and then placed on a tray and dried under a flow cabinet.

6.2.1 Spin-coating Planar Alignment Agents

We now improve the process for millimetre-wave devices by taking the following measures, as distinct from the facilities used for microwave devices we made before.

[1] New planar alignment agent (AL1254):

Instead of the previous recipe based on the mixture of 0.1ml Nylon and 50ml formic acid, we use a new planar alignment agent, namely JSR Optmer AL1254 polyimide (JSR Micro). Detailed recipes are compared in Table 11. The AL1254 is a premixed solution (ink) that is ready to use. More specifically, the polyimide is pre-imidized organic-solvent-soluble, i.e. the ink contains polymer molecules dissolved in a solvent (GBL/BC*). It is free of formic acid and hence eliminating the corrosion problem. Moreover, the processing time is significantly reduced from 3 hours to less than 30 minutes, exhibiting two benefits. First, the much shorter baking time alleviates aforementioned dimensional instability of substrates due to mismatch in coefficient of thermal expansion (section 4.3.1), hence mitigating a series of losses at millimetre-wave caused by this (section 4.3.2). Second, the decreased time needed for substrates processing allows fast device-prototyping. This benefit is noticeable, as the efficiency of the LC-based device assembling process is highly limited by the long baking time.

Table.11 Comparison of Two Alignment Agents

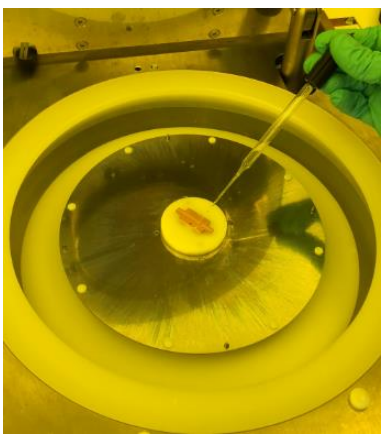
	Nylon	AL1254
Solution	Nylon: formic acid=2:998	GBL/BC* (formic acid-free)
Deposition (spin cast)	30 seconds at 3000 rpm	40 seconds at 2000 rpm
Baking	200˚C for 3 hours	80˚C for 2 minutes, then 200˚C for 25 minutes
Rubbing (roller rotating)	300rpm, 2 passes (forwards and backwards), 200μm pile contact	

* GBL denotes Gamma-butyrolactone, BC denotes Butyl Cellosolve.

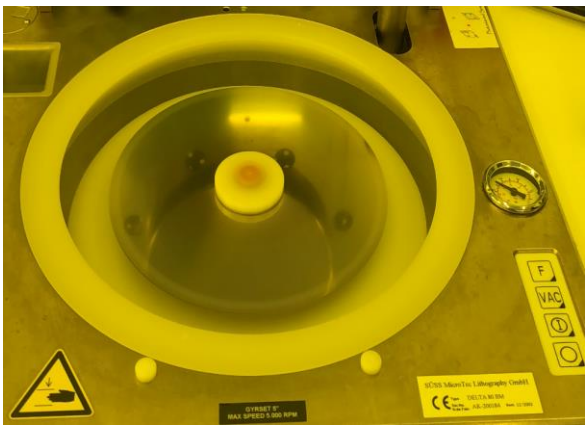
[2] New spin coater (DELTA 80):

The spinning chamber used previously is replaced with DELTA 80 (SUSS), which features particularly strong vacuum at the chuck to hold down large samples. This fixes the flying-away problem we frequently encountered before when spinning long and heavy ground plates. Digital control of rotation speed and time with programmable acceleration is available. Our large enclosure is positioned stably during spinning without sacrificing the rotating speed, which also mitigates the edge building up.

Static dispensation of the alignment agent is performed for the cleaned substrate placed on the new spin coater with vacuum on. First, a small puddle of AL1254 is deposited on the gold-plated conductor side of the PCB substrate, as well as the cavity of the gold-plated Cu enclosure, as shown in Fig.83 (a). The dispense volume fully covers the substrate surface and the cavity. The substrate (either the PCB or enclosure) is then rotated at a speed accelerating from 0 to 2000 rpm for 40 seconds as shown in Fig.83 (b), with a majority of the ink flung off the side, leaving a 60nm-thick uniformly-coated film.



(a) AL1254 Deposition



(b) Rotating at 2000 rpm

Fig.83 Deposition of Alignment Agent and Spin-coating

Residual solvent in the coated film is then dried by preheating (soft-baking) at 80˚C for 2 minutes using a hotplate as shown in Fig.84 (a), leaving a plasticised film on the substrate. The soft baking is intended to avoid killing the polyimide caused by over-baking (which loses the LC reorientation capability). After the pre-heating, 200˚C baking for 25 minutes with a reversed beaker covering the samples is performed to fully dry the film, leaving only the polymer molecules on the surface.

(a) 80˚C Preheating (b) 200˚C Baking

Fig.84 Eliminating Excess Solvents from the Coated Film

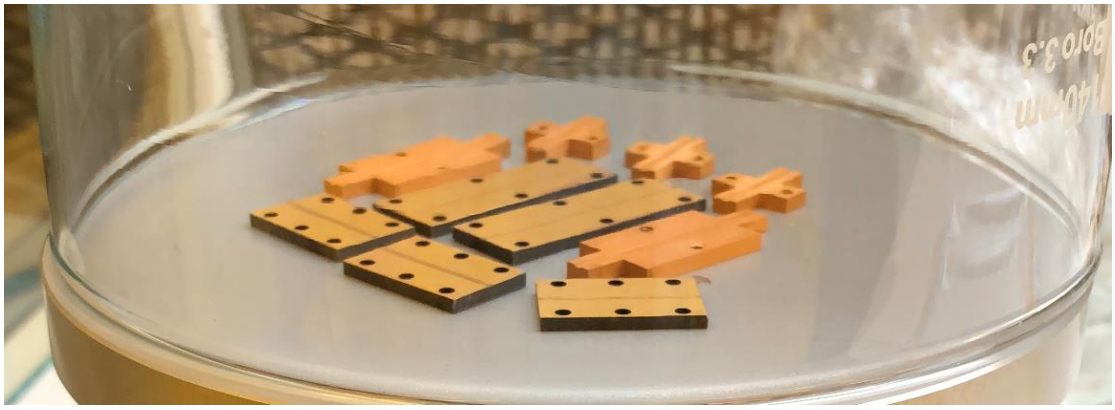


Fig.85 Post-baked Substrates

6.2.2 Rubbing Polyimide Alignment Film

AZ LCD's MF7 bench top model is used for alignment of the polyimide film, as shown in Fig.86 below. Before rubbing, the alignment direction is marked on the back of the substrates with an arrow for post-rubbed anti-parallel assembling.

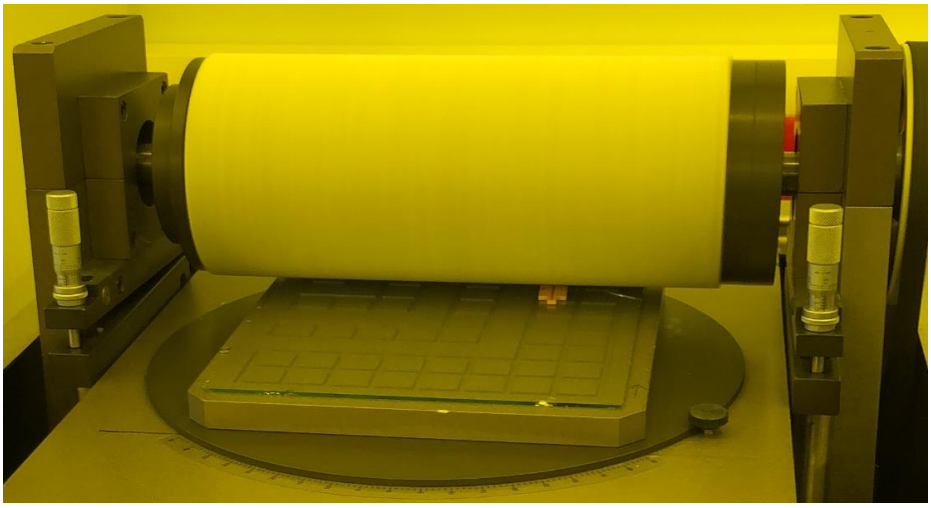


Fig.86 Rubbing a PCB by a LCD Rubbing Machine (model: MF-7)

Several substrates of diverse thicknesses are sacrificed to determine the suitable roller vertical position such that 200μm pile contact length is achieved. The pile contact length is selected out of concern for electrostatics and scratching samples (provided gap-free between the cloth and the substrate). The Table 12 below records the results of micrometre gauges adjusting for our PCB and enclosure, respectively. Controlling the contact with cloth is realised by monitoring the wheel current variation as well as listening to the change of sound (before contact vs. in contact). Both PCB and enclosure are rubbed hard to ensure that the alignment films at the bottom surfaces of the CPW channels (width=203μm, depth=17μm) and the enclosure cavity (width=1300μm, depth=140μm) can be rubbed inside and are in good contact with the velvet piles (200μm contact length is assumed).

Table.12 Micrometre Gauges Settings of the Roller for Different Substrates

Roller Position for PCB (1.575mm-thick)		Roller Position for Enclosure (2mm-thick)	
Left*	Right	Left	Right
2.00mm	2.50mm	1.65mm	2 .15mm
Wheel Current Change for PCB		Wheel Current Change for Enclosure	
1.86 to 1.96		1.5 to 1.7	

*Two micrometre gauges (left and right) set the roller's vertical position.

However, prior to device assembling and filling with LC (Chapter 6.3), there is currently no way to confirm if it was rubbed properly (e.g. whether the pile is rubbing the inside of the cavity, or bending and staying on the edge). In the measurement of devices reported in Chapter 7, we measure and compare the phase delay produced by the following two cases, i.e. (1) 0V bias, and (2) applying 10V first, then removal of voltage (i.e. back to 0V). Measurement result shows that the phase delay is almost unchanged (<1˚ difference), indicating that the rubbed alignment layer is well-behaved for LC reorientation.

Post-rubbing treatment is performed for the roller to avoid accumulation of dirt and tarnishing of samples. This is carried out by IPA static dispense and blowing with a nitrogen gun for the velvet cloth.

6.3 Substrates Assembling, LC-filling, and Connectors Mounting

Fig.87 below illustrates the components to be assembled by hand for a whole device.

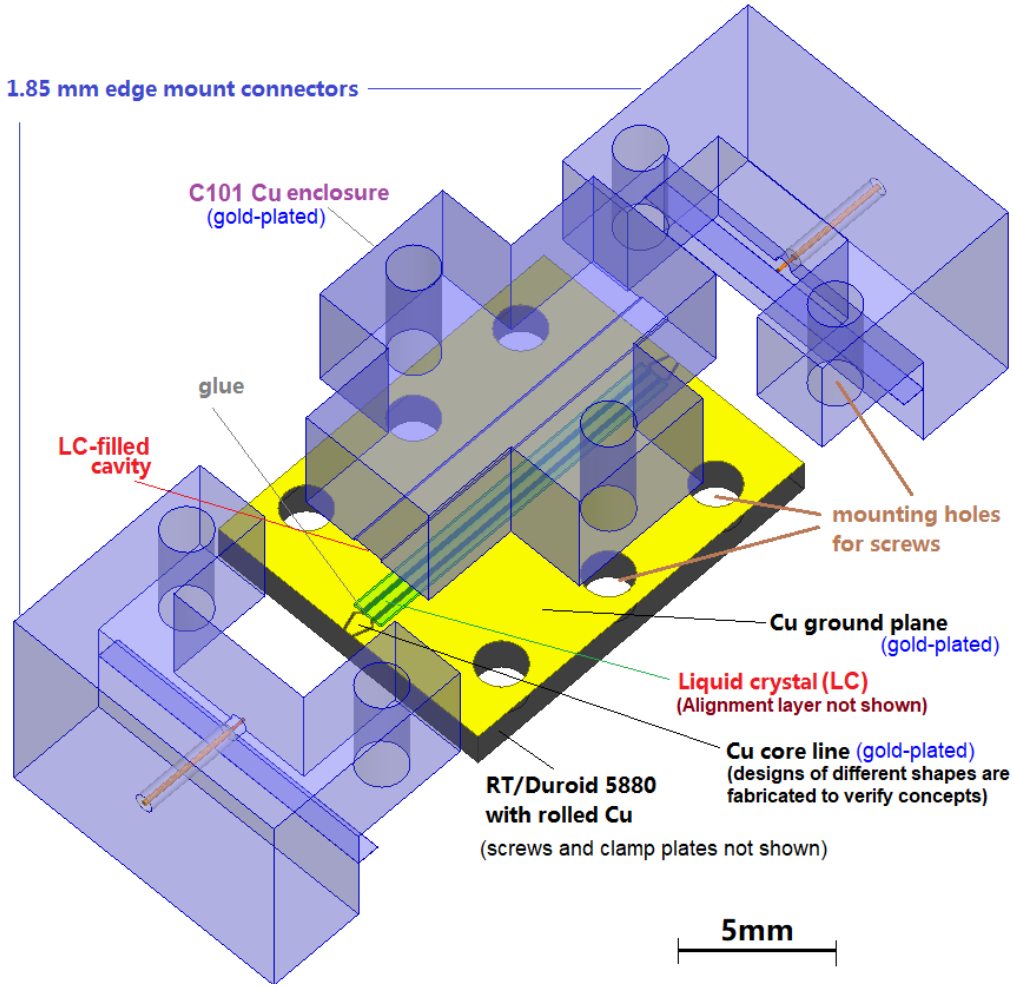


Fig.87 Exploded View of the Proposed LC-filled ECPW Phase Shifter

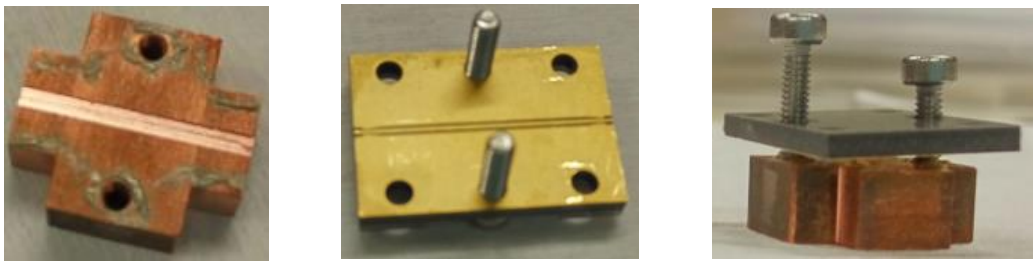
The assembling process consists of three steps as detailed in this section, i.e. PCB and enclosure pressed by screws, LC-filling followed by openings-sealing, and finally connectors edge-mounting.

6.3.1 Assembling with Screws and Silver Conductive Paste

First, the post-rubbed PCB and enclosure are assembled in anti-parallel alignment direction, and closely clamped by Stainless Steel Allen Bolt Socket Cap Screws with Hex Head (M2×2). Such a mechanical mounting raises a concern for problematic electrical connection at millimetre-wave due to inevitable gaps (discontinuity) existing between the ground enclosure surface and the CPW's ground surface on the PCB. Since the circuit is made by joining the two separate parts, electrical contact resistance between the enclosure and the CPW grounds affects the potential difference and hence the stray modes radiation loss.

To investigate electrical connectivity improvement for a unified grounding path, silver conductive paste (SCP) is applied in between the enclosure and PCB ground surfaces. First, we place one drop of LC onto the SCP deposited on the enclosure surface. No contamination of the LC is observed, confirming that LC and SCP make no reaction. SCP is then applied following the procedures described below.

1. Stir SCP using metal with a ball-like shape.
2. Draw lines of SCP on enclosure peripheral areas, as shown in Fig.88 (a).
3. Invert the PCB (with screws) onto the enclosure, fasten the screws, as illustrated in Fig.88 (b) and (c).
4. Squeeze hard the assembled substrates and wait overnight. No curing is needed.



(a) (b) (c)

Fig.88 Applying SCP before Substrates Assembling

The assembled substrates are subsequently put on a hotplate heating from room temperature to 175˚C (LC clearing temperature). Extra screws are temporarily put on the connector mounting holes for the purpose of a stabilised process for the later LC-filling, where uniformity is desired.

Fig.89 Heating the Assembled Substrates in Preparation for LC-filling

Devices assembled with SCP and without SCP (i.e. mounted by screws only) are made respectively, measured and compared later after LC-filling.

6.3.2 One-Drop LC Filling based on Capillary Action

For the Enclosed CPW (ECPW) configuration, the following scenarios are envisaged for LC-filling into the cavity and CPW channels.

Assuming that LC-filling is performed after connectors are installed, we can firstly use glue to seal the device all the way round, then drill holes from metal walls or from connector dielectrics, and fill LC inside by either capillary or syringe injection. However, electrical properties of the guiding structure can be disrupted significantly due to discontinuity caused by drilled holes. Syringe filling carries the risk of air bubbles injection. In addition, connectors mounted and

glued on the filled-device cannot be dismounted once assembled, which elevates the development costs.

Assuming that LC-filling is run prior to mounting of connectors, a one-drop capillary method is deployed at one end of the cavity opening, over-filling the cavity and CPW channels until LC comes out at the other end. After that, residual LC outside the cavity is cleaned before sealing the cavity and channel openings. Connectors are mounted after the gluing. Minor disruption of electrical properties is caused (only adding a thin-layer of glue to the openings). Furthermore, this process exhibits advantages of modularity and flexibility for dismounting and reuse of connectors. However, the capillary filling capability from one end of the cavity to the other is unknown, as the ratio of the cavity width to the channel length is $\frac{1.3}{14.75} < \frac{1}{10}$.

We experimentally investigate the second scenario (i.e. filling prior to mounting of connectors), with the detailed procedure shown in Fig.90 below. First, pre-filled assembled substrates are placed on the hotplate and heated to the LC clearing temperature (175˚C). Using a pipette, a drop of LC is placed at one end of the Enclosed CPW (ECPW) cavity. Relying on capillary effect, the LC sucks in the cavity (channels) and flows very fast along with the alignment direction until wetting the other end of the cavity (channels). Note that the filling is also a LC-alignment process. We observe that one drop at one end suffices to overfill the design targeted π-shifting.

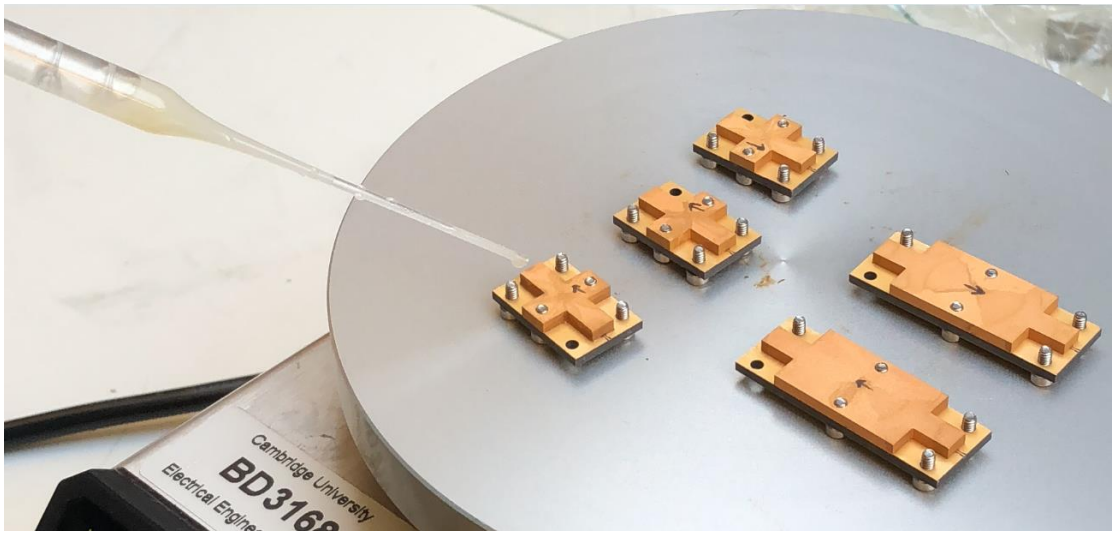
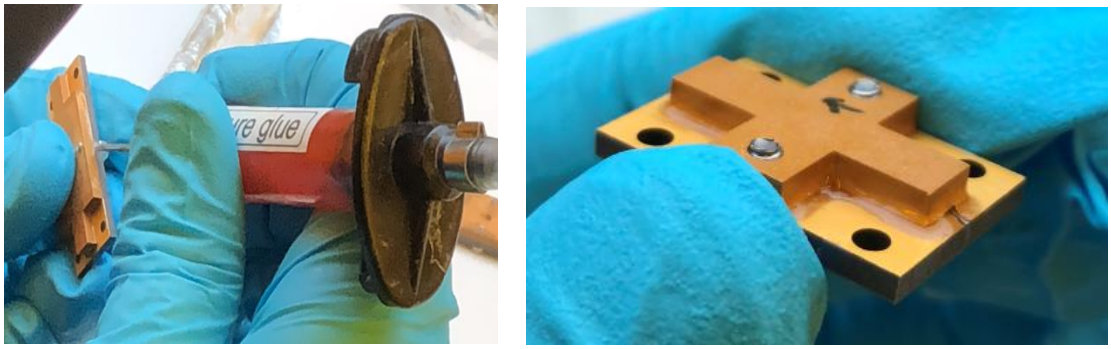


Fig.90 LC-filling based on One-drop Capillary Effect

6.3.3 Samples Sealing and Connectors Installing

Prior to sealing the openings at the two ends of the cavity, residual LC at the periphery area outside the openings is wiped away by sponge tips. When the temperature of the above LC-filled samples drops down below 60˚C (avoiding polymerization of glue to be applied), a needle with inner diameter of 108μm is then used to apply glue to tightly seal the tunable samples, as shown in Fig.91(a). The amount of glue applied is controlled carefully by air pressure and speed of writing. Note that the two openings are glued first, put into UV lamp for 3 minutes curing, and taken out for inspection of the glued profile. The peripheral sides of the sample are subsequently glued and processed in the same way. The step-by-step sealing avoids glue spreading everywhere else. Finally, the all-sealed samples are UV-cured for another 10 minutes. A sealed tunable sample is presented in Fig.91 (b). The glue profile at the cavity ends seems a concern for degrading electrical conduction between the CPW core line and the connector pins to be attached. According to the simulated tolerance of the gluing effect on insertion loss, this only adds up to 0.1dB. Solvents are carefully applied to remove some outer glue layer at the core line region without removing the inner glue layer.



(a) Glue Writing (b) after UV Curing

Fig.91 Tunable LC-filled ECPW Samples Sealing before Installing Connectors

1.85mm end-launch connectors are edge-mounted on the sealed LC-filled ECPW shown below.

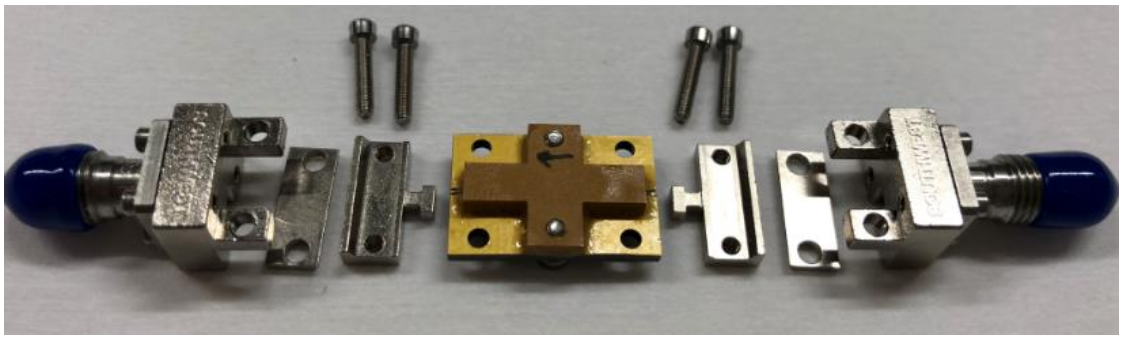


Fig.92 Exploded View of the Final Device Assembling by Edge-Mounting the Connectors

Looking into the unique clamping mechanism of the end-launch connectors, the bottom level of the grounding block is not exactly in the same altitude as the pin. This is one of the intended design features of the end launch connector. The pin is intended to be slightly below the bottom surface of the transition block to create an interference fit between the pin and the CPW core trace, to insure sufficient pressure contact without solder. One of the key features of the end launch is the no-solder requirement resulting in a removable and reusable connector. However, if the end launch is intended to be mounted permanently for a shippable item, then the pin can be soldered. But no solder is preferable for electrical performance reasons and reusability. Note that gold dissolves readily in standard tin-lead solders. The intermetallic compounds produced increases surfaces roughness and poses gold embrittlement problems in solder joints. No soldering is performed during our assembling process, thus not raising a concern for the reliability of gold-coated patterns.

Fig.93 below presents the post-assembled phase shifter in different views.

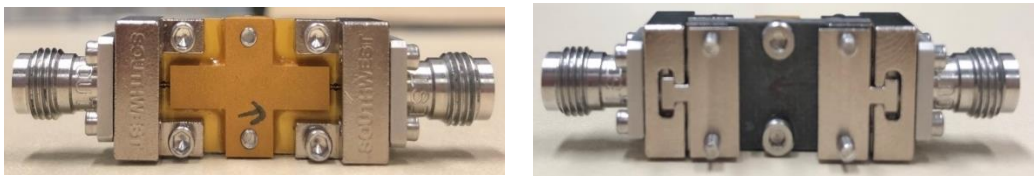


Fig.93 Top and Bottom Views of the Final Assembled Device

The connector mounting approach can be further optimised by strategically supplying a unified metal block at the bottom to homogenise the mechanical stress and hence an improved uniformity of the substrate as well as the functional LC layer.

6.4 Device Measurement Setup

6.4.1 Instruments and Calibration

Scattering parameters were measured using a two-port one-source Vector Network Analyser (VNA) R&S®ZVA67 with the frequency range from 1MHz to 67GHz. Tailored for our unidirectional transmission measurements, VNA calibration is performed with One-Path Two-Port standard, covering four procedures, i.e. Open, Short, Match and Through.

As shown in Fig.94 below, Agilent 33120A synthesized function generator is used to supply a low-frequency (5Hz) square-wave voltage for liquid crystals-based device driving. External bias-T circuits are not required for the setup, as an internal bias network has been embedded in the VNA instrument. Thereby, the function generator's output is directly connected to the VNA bias port, whose input voltage range is limited below 30V.

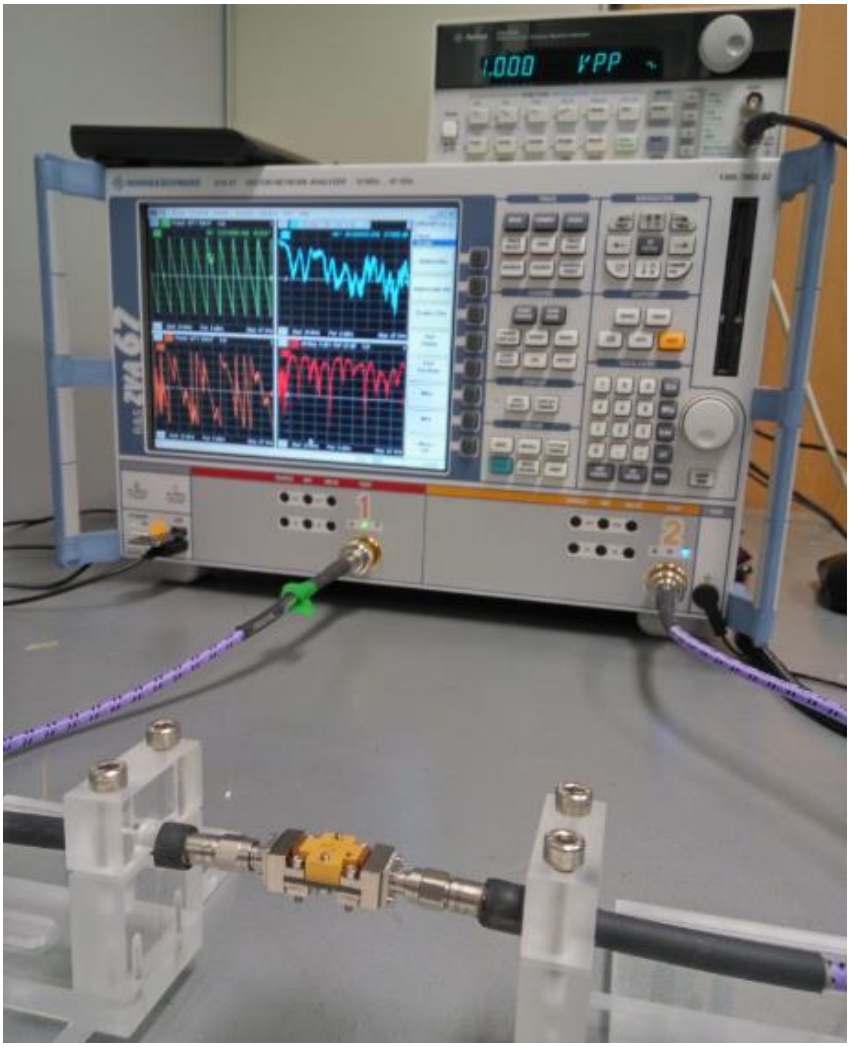


Fig.94 Front-panel View of Measuring Instruments Setup (Voltage Amplifier not Shown)

6.4.2 Data Collection and Processing

Based on network analysis, signal transmitted (S_{21}) and reflected (S_{11}) are measured with phase ($^{\circ}$) and amplitude (dB) information. Measured data of all channels and traces is saved in .csv format and exported to laptops for data-processing using Matlab and originLab.

The voltage-dependent differential phase shift is processed by taking the phase delay at 0V as a reference and computing the difference with other voltages. Delay length is derived based on

$$\frac{\Delta\Phi}{360^{\circ}} = \frac{Delay\ Length}{\lambda} \implies \text{Delay Length } = \frac{\Delta\Phi}{360^{\circ}}\,\lambda \qquad \text{.....(33)}$$

For loss decomposition analysis, the collected power ratio based upon dB definition is converted back to percentage based on eqs.34 and 35.

$$S_{21} = 10log\frac{P_{transmitted}}{P_{in}} = 10log\frac{P_{in}-P_{loss}}{P_{in}} = 10\,log(1-\frac{P_{loss}}{P_{in}}) \qquad \text{.....(34)}$$

$$S_{11} = 10log\frac{P_{reflected}}{P_{in}} \qquad \text{..... (35)}$$

We define power loss (dB) due to radiation, interference, and higher-order spurious modes as

$$P_{radiated} = 10log\frac{P_{out}(with\ enclosed\ sidewalls)-P_{out}(without\ sidewalls)}{P_{in}}$$

$$= 10log\,(10^{\frac{S21\,(with\ enclosed\ sidewalls)}{10}} - 10^{\frac{S21\,(without\ sidewalls)}{10}}) \qquad \text{..... (36)}$$

Combining eqs. 34 and 36, the output signal-to-noise ratio *(SNR)* is thus calculated by

$$SNR = \frac{P_{transmitted}}{P_{radiated}} \qquad \text{.....(37)}$$

Chapter 7. Measured Device Performance, Optimisation, and Future Research Possibilities

To verify the performance of the proposed phase shifter designs (Chapter 7.1), groups of phase shifter prototypes were fabricated, assembled, measured, experimental results analysed, compared with designed properties, optimised (Chapter 7.2), and evaluated against states-of-the-arts (Chapter 7.3).

7.1 S-parameters-based Measurement and Validation

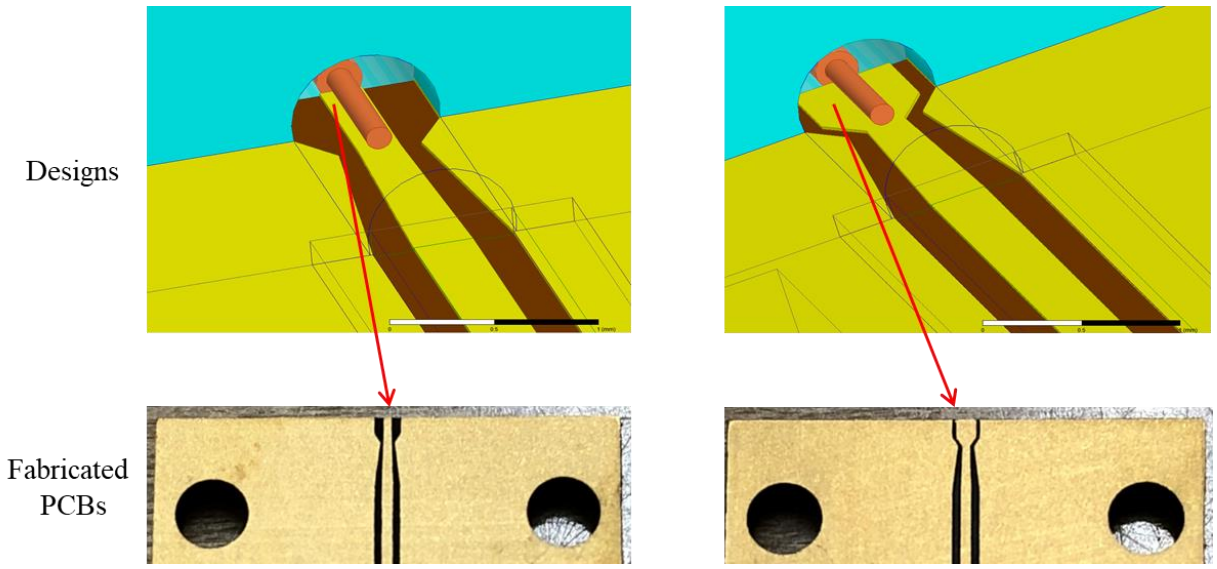
For experimental verifications of different concepts and methods, device measurements have been conducted for the following comparative designs.

[1] Impedance matching methods for the PCB-connector interface, i.e. time domain reflectometry (TDR) vs. infinitely-long transmission line model (TLM).
[2] Effect of silver conductive paste (SCP) on insertion loss, i.e. with SCP vs. no SCP.
[3] Effect of Cu-PTFE interface's surface roughness on insertion loss, i.e. RA Cu vs. ED Cu.
[4] Optimal gold-plating thicknesses on Cu, i.e. non-plated vs. thin gold-plated vs. thick gold-plated.

Note that the above first two cases are measured first for verification of the fabricated device's functionality, while the latter two are for optimisation purposes and reported in Chapter 7.2. For each case, all the other parameters are kept constant except for the variable being investigated. The measured frequency range focuses on 60GHz with ±10% bandwidth, i.e. 54GHz-67GHz, which covers the useful 57GHz-66GHz unlicensed band designated in Europe for 5G communications. For each design, *S*-parameters are measured and averaged across three devices (LC-filled and fully assembled) to minimise the effects of random errors.

7.1.1 Measured Performance of Devices with Interface Matched by TDR vs. Infinitely-long Transmission Line Model (TLM)

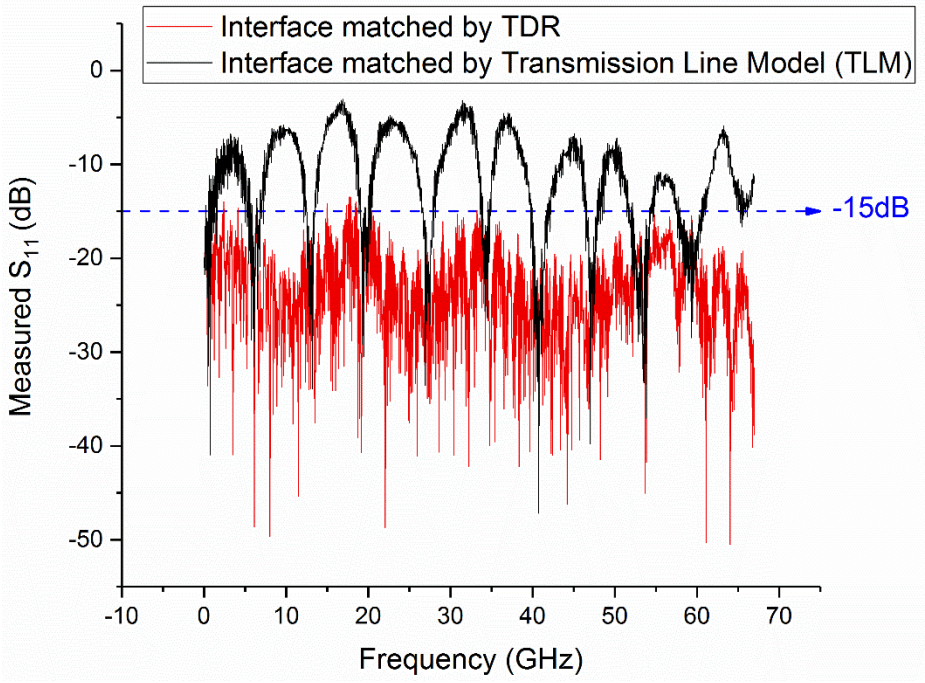
Two groups of devices were assembled with diverse PCB designs at the connector-to-PCB interface, as shown in Fig.95 (a) the smoothly-tapered one designed by time domain reflectometry (TDR), and Fig.95 (b) the one whose derivation is based on the infinitely-long transmission line model (TLM). They share the same LC tunable design part but differ at the interface portion of the PCB's traces.



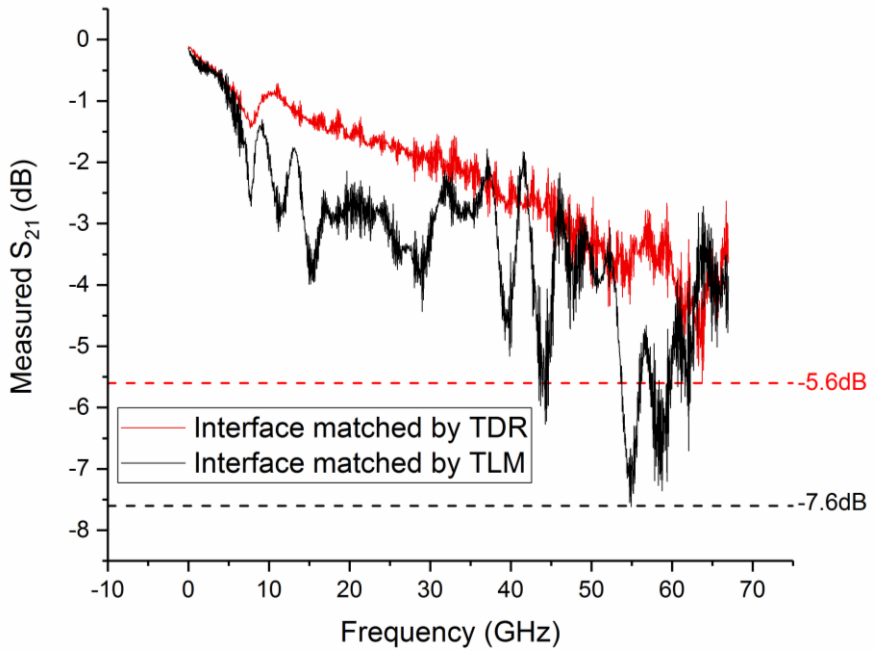
(a) Designed by TDR (b) Designed by TLM

Fig.95 Devices with Different Interface Designs based on Diverse Matching Mechanisms

The measured low return loss for a broadened bandwidth (< -15dB from 20MHz-67GHz) reported in Fig.96 (a) validates the use of the TDR method for clean signal transitions at connector-PCB interfaces, which significantly mitigates the return loss by up to 10dB and ultimately, reduces insertion loss. Measured maximum insertion loss (0V bias) is less than -5.6dB across 20MHz to 67GHz for the device matched by TDR, as demonstrated in Fig.96 (b).



(a) Return Loss Measured at 0V: Devices Matched by TDR vs. TLM



(b) Insertion Loss Measured at 0V: Devices Matched by TDR vs. TLM

Fig.96 Measured Losses of Devices with Interface Matched by Diverse Matching Methods

Arguably, obtaining knowledge of characteristic impedance from the infinitely-long transmission line model (TLM) is infeasible and fails to characterise the transient impedance of the connector-to-PCB joint (multiple sections). Beyond that, constructive and destructive interferences of reflected waves can cause more appreciable side-effects than initially considered, as exemplified in the differential phase shift measured in Fig.97 below. Strong oscillations are observed for the device matched by the TLM method, resulting in undesired

beam squinting (i.e. the beam steering angle varies with frequency) when integrating the phase shifters into a phased array antenna beam steering system. Instead, the TDR method exhibits a more linear response and henceforth its validity is confirmed for the connector-to-PCB interface design at millimetre-wave frequencies.

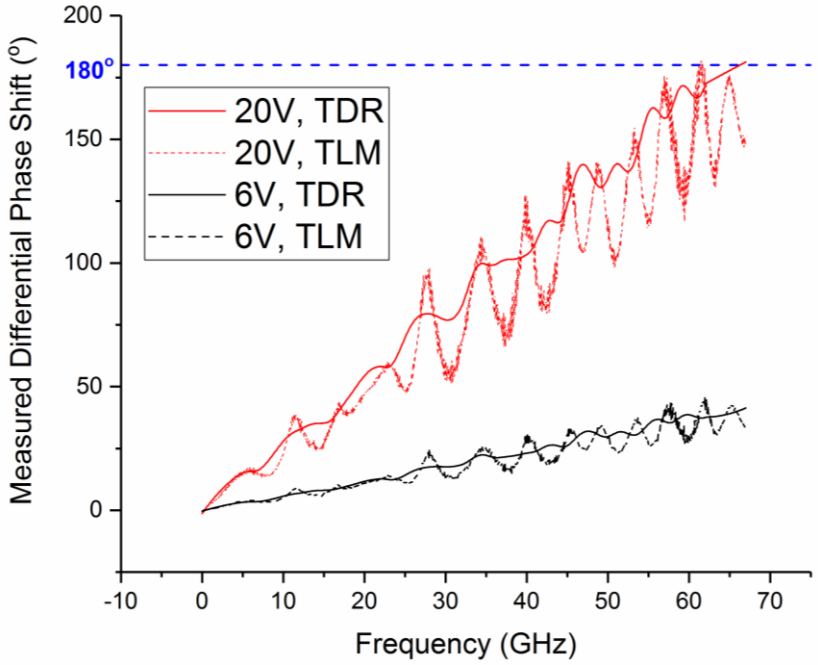


Fig.97 Measured Differential Phase Shift of Devices Matched by TDR vs. TLM

Looking into the voltage response of the shifted phase (Fig.98 below) measured for the device matched by TDR, 0˚-180˚ continuous phase shift is achieved by a bias voltage from 0V to 20V.

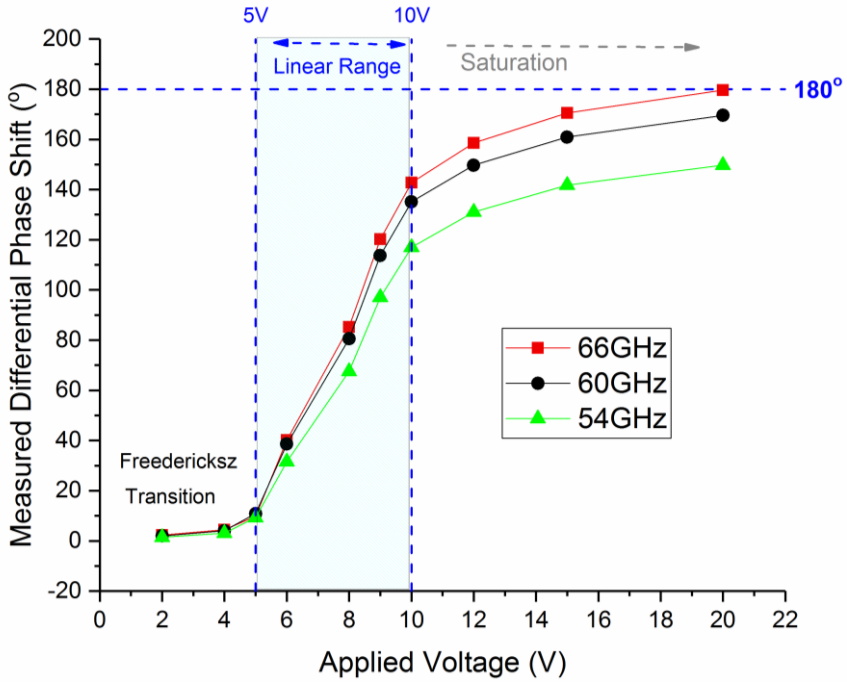


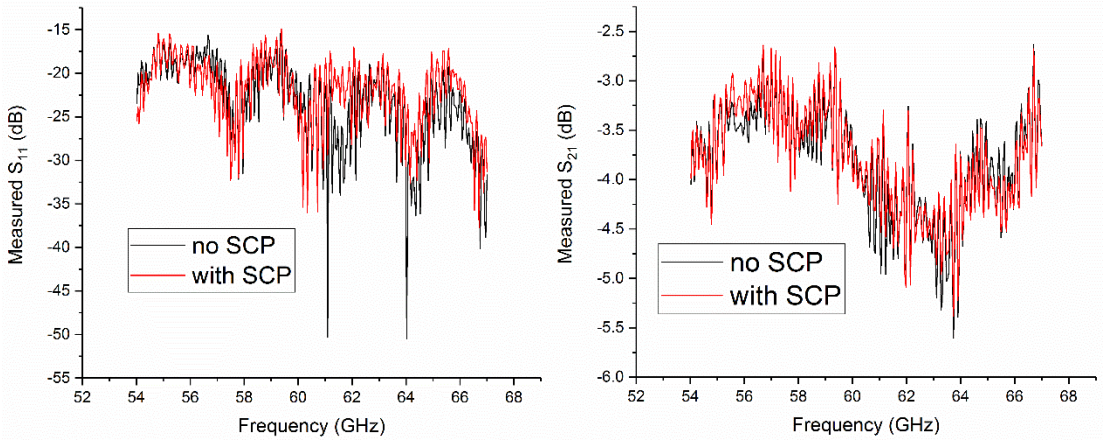
Fig.98 Measured Voltage Response of Phase Shift: Device Matched by TDR

(1st Round Design)

To be more specific, there is a quasi-linear phase shift vs. voltage response range from 5V (the threshold of Fredericks transition) to 10V (the beginning of saturating), wherein the applied low-frequency electric field in the proposed ECPW cavity controls LC's molecular polarizability to vary continuously and contribute to agility efficiently. The minor nonlinearity in this range is due mainly to the trapped charges in the alignment agent, which distorts the low-frequency field.

7.1.2 Measured Performance of Devices with SCP vs. no SCP

The impact of silver conductive paste (SCP) adding to the grounding path's electrical connectivity is measured and evaluated with S-parameters reported in Fig.99 below for two groups of devices assembled without and with SCP (applied between CPW's ground planes and the enclosure).



(a) Measured Return Loss (b) Measured Insertion Loss

Fig.99 Measured Impact of SCP on Return and Insertion Losses (0V bias)

Although pressing the enclosure on the PCB substrate carefully, the non-uniformity due to the uncertainty of the applied SCP layer results in elevated return loss and adds to the insertion loss, which cancels out the benefit of improved conducting paths connecting the grounds. Therefore, SCP is not applied in the final-round of device fabrication to minimise the impact of manufacturing tolerances.

7.1.3 In-depth Analysis and Limitations of the 1st Round Fabricated Devices

The device matched by TDR exhibits a low return loss of < -15dB across a wideband from 20MHz to 67GHz, as observed from the measured spectrum of S_{21} above (section 7.1.1 and 7.1.2). The low return loss ensures signal integrity and hence is amenable to loss-decomposition analysis for device optimisation (Chapter 7.2). Given the signal transmission with low reflection, a couple of deficiencies spotted for the 1st round device design can be analysed. Fig.100 below summarizes the issues, with the details explained in the following sections.

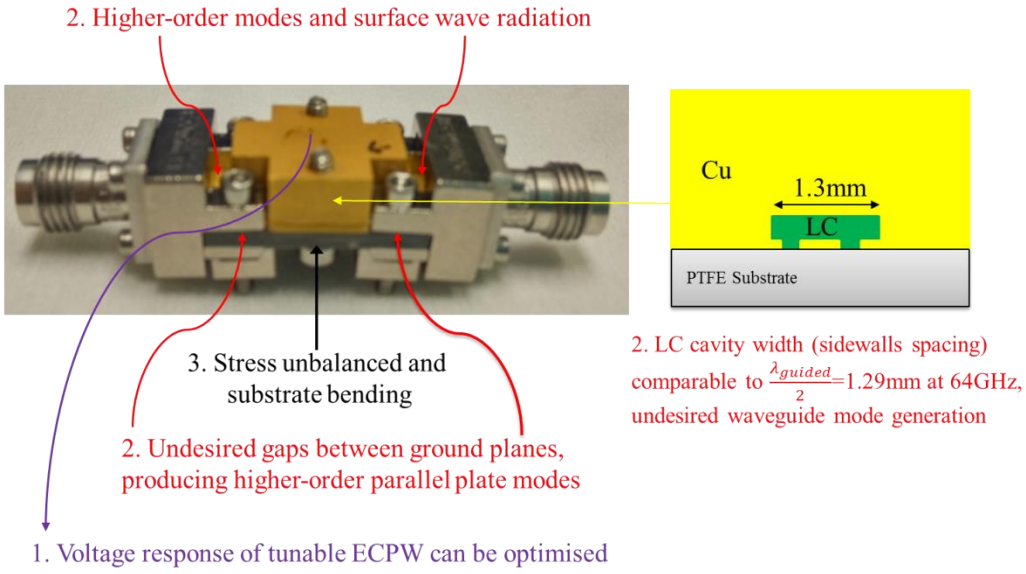


Fig. 100 Problems Spotted for the Fabricated 1st Round Device Design

7.1.3.1 Phase Shift – Voltage Response

The first property that merits optimisation is the bias voltage response for the phase shift of π. At 66GHz, the π shift is realised with a bias voltage of 20V, which can be optimised to be lowered to 10V for more ease of control, lower power consumption, and more importantly, allowing the π shift falling within the desired linear response range (5V-10V).

Two methods are considered to achieve the desired shifting of π at 10V: (1) reducing the LC layer's thickness, and (2) extending the length of the tunable ECPW transmission line.

The intension of the first method is to increase the tuning range by increasing the 66GHz E-field intensity and hence the wave-occupied-volume ratio of the tunable LC to the non-tunable PTFE. However, reduced LC thickness lowers the saturation voltage (i.e. a steepened curve)

and loses the linear advantage exhibited by the 1st round design (i.e. linear shift-voltage response from 5V to 10V). Moreover, reducing the LC thickness makes only minor improvement to the phase shift increase as the reduced LC volume cancels out the field intensity increase effect and hence makes only a minor contribution to an improved tuning range.

Since the differential phase shift is proportional to the length of the tunable part, we thereby employ the second method for optimisation, i.e. extend the tunable line length of the proposed ECPW, whilst maintaining other design features (cross section geometry and LC thickness). This method aims to scope the 0-π shifting at the linear voltage response range from 5V to 10V, with the results demonstrated in Chapter 7.2.

7.1.3.2 Higher-order Modes

The second characteristic that attracts our attention is a sharp dip in the insertion loss at around 64GHz, which limits the targeted low-loss performance at 60GHz across a bandwidth of ±10%. Mismatching is not the cause of the problem, as shown by the measured return loss (-30dB at 64GHz). We suspect the elevated attenuation is due to the excitation of higher-order modes.

The strong resonance observed around 64GHz is due to a combination of two effects. First, a parasitic resonant structure is coupled to the device through unattended air gaps comparable to a quarter guided wavelength ($\frac{\lambda_{guided}}{4}$=0.64mm for 64GHz) between the connector's ground, the CPW's ground planes, and the enclosure. A significant part of the signal is radiated into free space where it may potentially interfere with adjacent phase shifters in a phased array system. Second, pseudo rectangular-waveguide modes are excited in the LC-filled metal cavity with sidewalls spacing (1.3mm) comparable to half a wavelength of 64GHz ($\frac{\lambda_{guided}}{2}$=1.29mm), hence disrupting the signal integrity and breaching the quasi-TEM nature. The coexistence of the problems increases the insertion loss by 2dB. Optimisations by minimisation of the noticeable gaps and narrowing the sidewalls spacing are discussed in Chapter 7.2.

7.1.3.3 Stress Relief and Dimensional Instability

A noticeable bending is observed for the 5880 PTFE substrate. We believe that such a dimensional instability accounts for the generation of undesired gaps and hence the higher-order modes mentioned above. The bending is a joint effect of the following:

Firstly, the post-etch shrinking and post-bake bending of the PCB substrate due to CTE mismatch. As interpreted in section 4.3.1, the post-laminated 5880 PTFE substrate exhibits both crystalline and amorphous phases, with immediate elastic property and slow viscous property in response to stress relief. The shrinking of the 5880 immediately after assembling is a joint effect of the elastic responses from crystalline and amorphous phases. The viscous response from amorphous phase contributes to residual shrinkage which takes some days to finish until a stress balance is reached.

Secondly, the inhomogeneous mechanical loadings and hence stress unbalance across the substrate adds to the substrate's dimensional instability. Note that both the connectors and the 5mm-thick enclosure (three individual components in total) are anchored onto the post-etched soft PTFE substrate by mounting screws. By inspection, the substrate suffers from different degrees of bending depending on the order of installation and conditions of the three components.

7.2 Device Optimisation

7.2.1 Components Miniaturisation and Return Loss Reduction

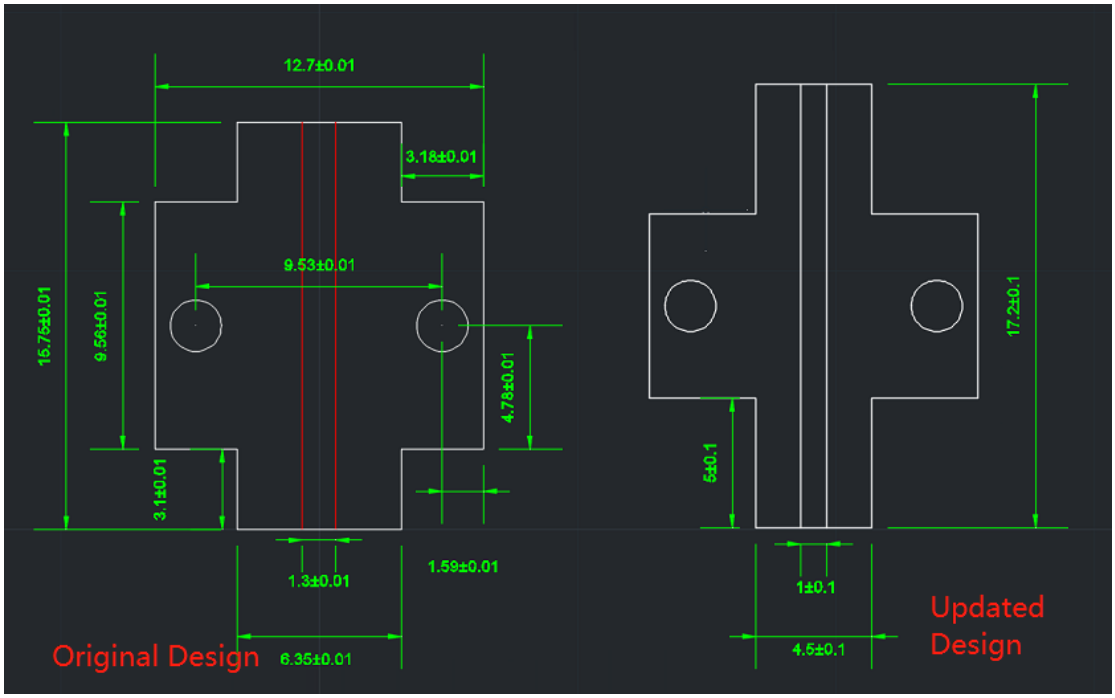
In recognition of the issues stated above in section 7.1.3, the following optimisation measures are experimented accordingly.

[1] According to section 7.1.3.1, we extended the tunable line length from 16.7mm to 17.2mm, whilst keeping the LC thickness (140µm). The aims were to achieve a phase shift of π at 66GHz with 10V only and with linear voltage response for 5V-10V.

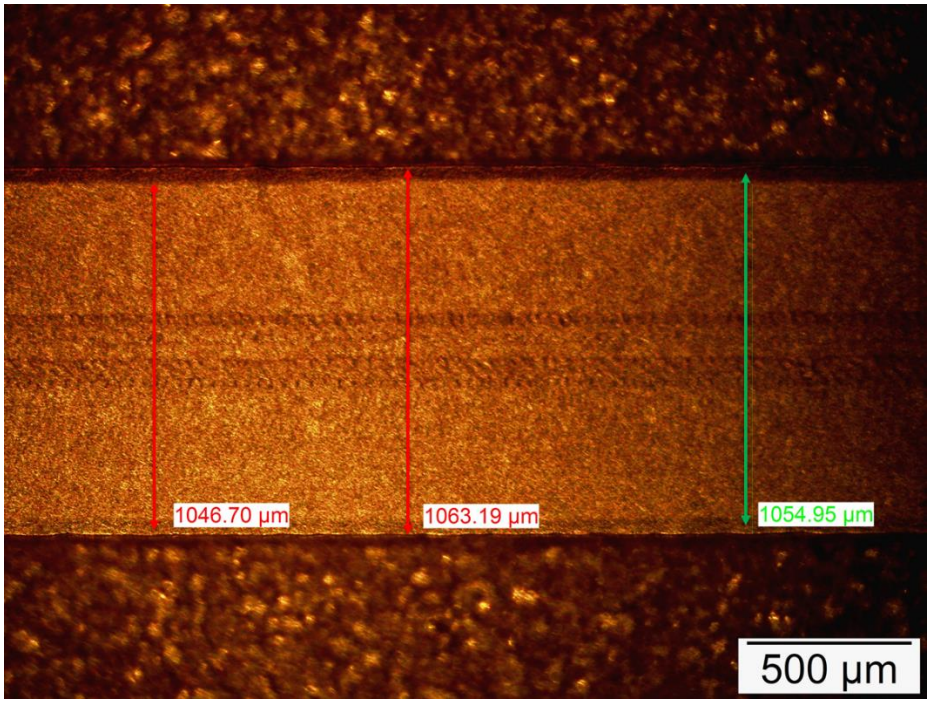
[2] According to section 7.1.3.2, we reduce the cavity's width (sidewalls spacing) of the enclosure from 1.3mm to 1mm in order to avoid pseudo rectangular-waveguide modes excitation. This aimed to broaden the operating bandwidth by pushing the highest frequency up to 67GHz without causing resonance and insertion loss dip. Meanwhile, we extended the two ends of the cavity and minimised the air gap between connectors and the enclosure.

[3] According to section 7.1.3.3, we reduced the thickness of the Cu enclosure (the whole top plate) from 5mm to 2mm. We also reduced the footprint of the enclosure to reserve ample space for connectors' grounds landing on the PCB.

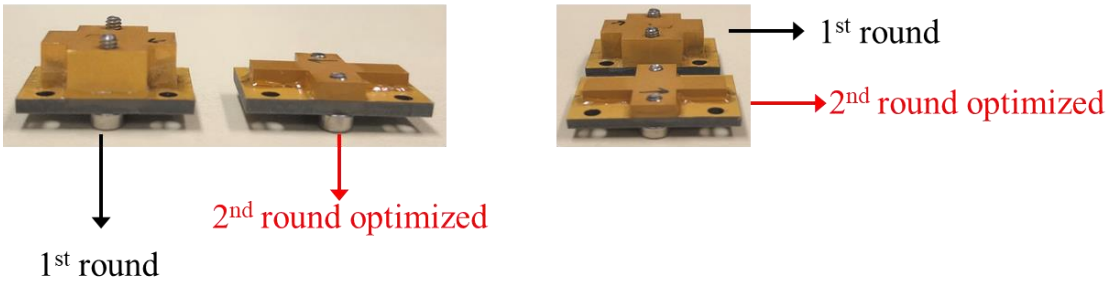
An updated design and the fabricated prototype of the proposed LC-based ECPW incorporating the optimisation methods mentioned above are presented in Fig.101 below.



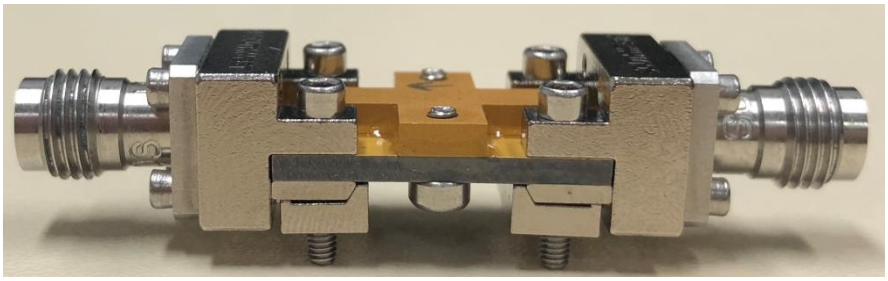
(a) Enclosure Designs (Top View): 1st Round (Left), and 2nd Round Optimised (Right)



(b) Measured Cavity Width of the Fabricated 2nd Round Design under a Microscope



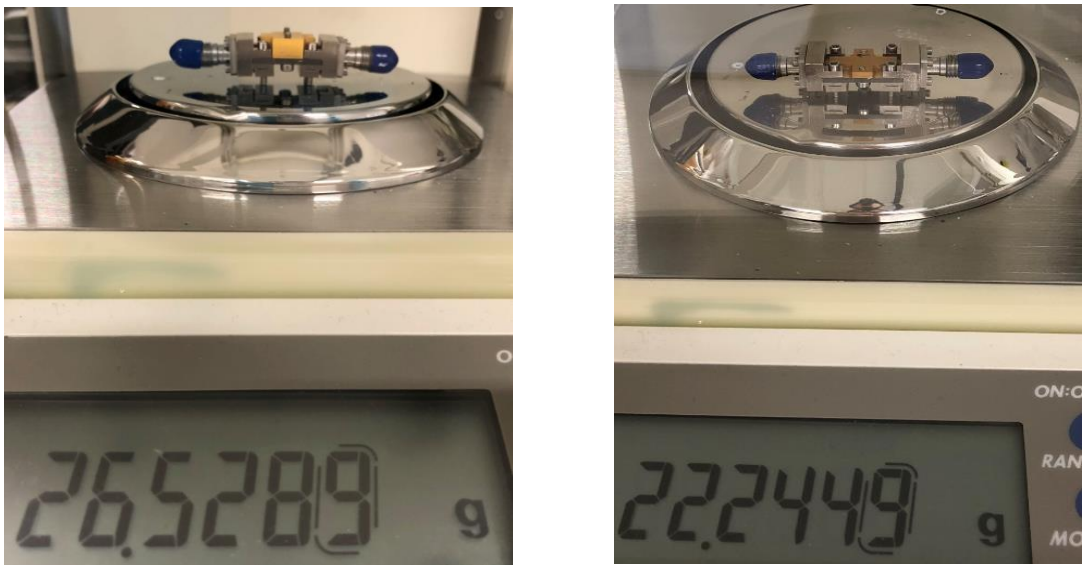
(c) Fabricated ECPW: 1st Round vs. and 2nd Round Optimised (Different Views)



(d) Assembled Whole Device with Connectors (2nd Round Optimised)

Fig.101 Optimisation of the Proposed LC-based ECPW (Design and Fabrication)

As demonstrated in Fig.101 (d) above, the bending issue of the substrate is largely mitigated, exhibiting a reasonably good uniformity of substrate for LC switching. Weight measurement (Fig.102) performed for the 1st and 2nd round devices shows that the miniaturisation of the enclosure contributes to 16.2% of the decrease in the weight of the device.



(a) 1st Round Device (b) Post-Optimised 2nd Round Device

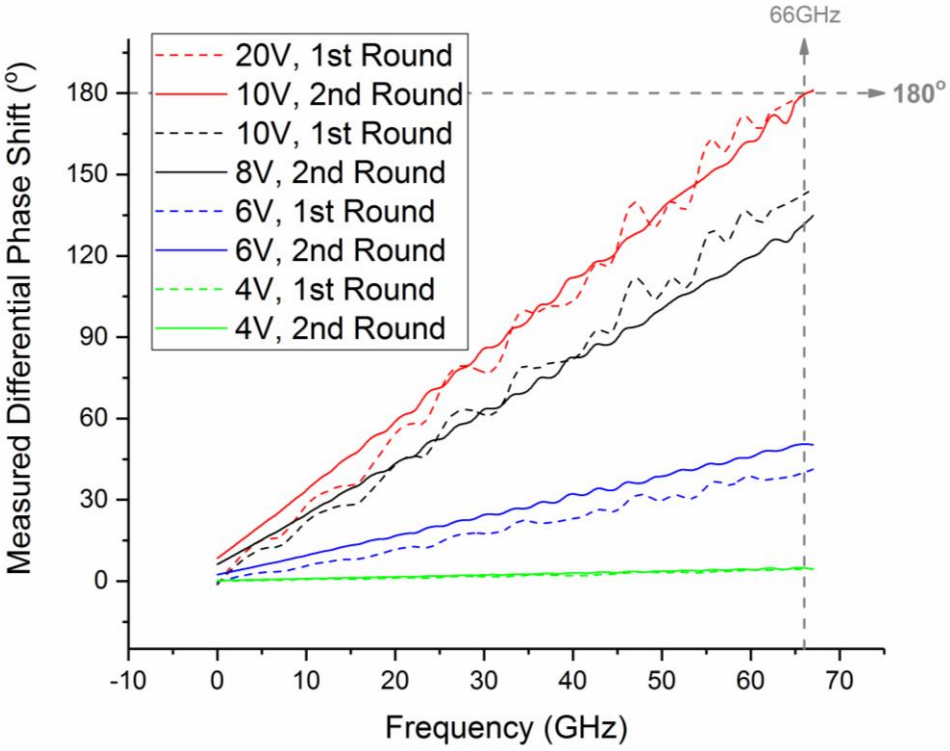
Fig.102 Weight Measurement of Devices before and after Optimisation

S-parameters are measured in the following section 7.2.2 to validate the optimisation of phase shifting functionality and insertion loss.

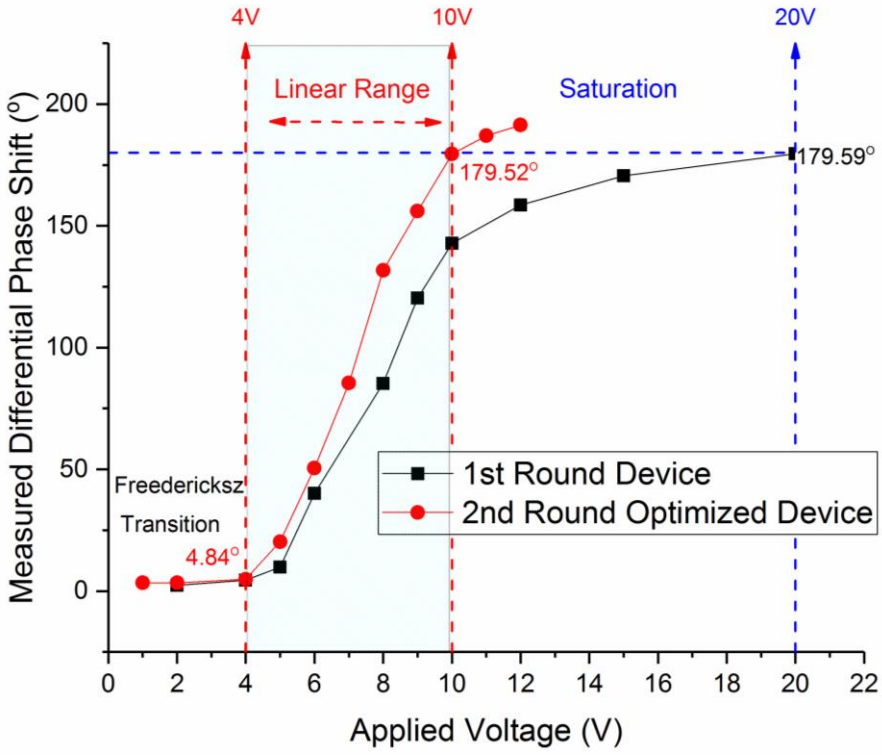
7.2.2 Measured Performance of 2nd Round Optimised Devices vs. 1st Round

7.2.2.1 Verification of Phase Shift and Voltage Response Optimisation

Differential phase shifts as a function of frequency and bias voltages were measured for devices of the 1st round (before optimisation) and the 2nd round (optimised) designs. As demonstrated in Fig.103 (a) and (b) below, a phase shift of π at 66GHz is achieved with ease by a much lower biasing field of only up to 10V for the 2nd round optimised device, as compared with the 20V required by the 1st round. In Fig.103 (a), phase shift ripples in the spectrum are further mitigated, which verifies the optimisation methods in addressing CTE mismatch and surface waves radiation as mentioned in section 7.1.3.



(a) Measured Phase Shift of 1st and 2nd Rounds Devices (20MHz-67GHz)



(b) Measured Phase Shift - Voltage Response of 1st and 2nd Rounds Devices (66GHz)

Fig.103 Measured Phase Shifting Performance of Our Devices before and after Optimisation

As evidenced by Fig.103 (b), the 2nd round (optimised) device keeps a desirable feature of the 1st round design, i.e. the linear response of differential phase shift vs. bias voltage from 5V to

10V for low-voltage control (≈0.1V/μm). By extending the length of the tunable ECPW part but without altering LC's thickness (i.e. not changing the agility of field-dependent orientation variation), the bias voltage required for π shift is confirmed to decrease from 20V to 10V for ease of control and reduced power consumption. The linear phase shift agility now covers the phase shift range from 4.8˚ to 179.5˚, corresponding to a low-frequency voltage bias from 4V to 10V. The non-linearities occurring below the Fredericks transition voltage (4V) and above the saturation voltage (10V) are of minor importance to the performance, as the linear range has covered most of the full phase tuning range (0-π).

Based on the differential phase shift measured, delay length (in millimetre) is quantified in Fig.104 below. The delay produced by the optimised device (2nd round) exhibits frequency-independence. This demonstrates a highly desirable true-time-delay advantage for ultra-wideband phased array antenna beam steering with no beam squinting.

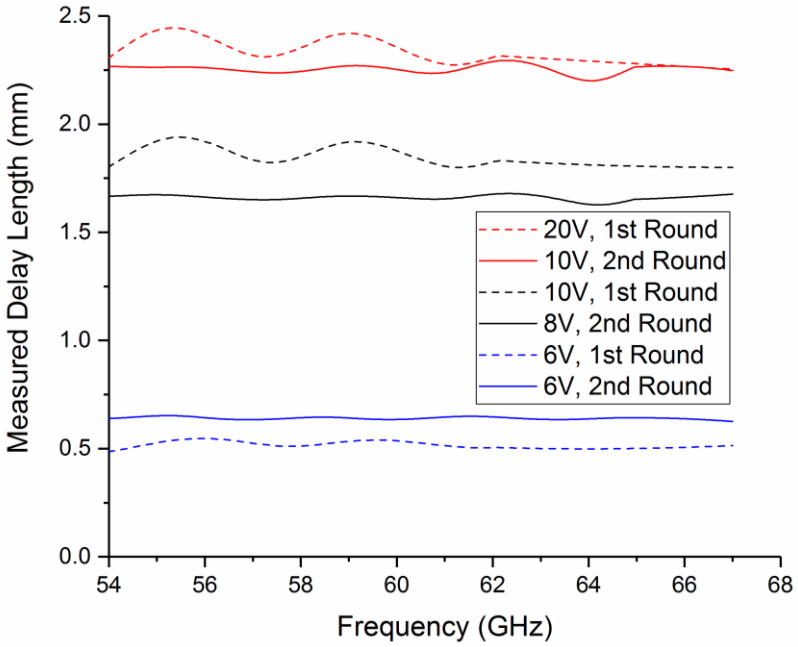


Fig.104 Measured Delay Length vs. Frequency of Our Devices before and after Optimisation

7.2.2.2 Demonstration of Insertion Loss and Wideband Figure-of-merit Optimisation

In addition to the phase shift optimisation verified above, measured insertion loss in Fig.105 below confirms that the narrowing of the cavity width (from 1.3mm to 1mm) compared with wavelength accounts for the insertion loss dip-free spectrum broadening, with the single-mode upper operation frequency (limited by the onset of waveguide modes and the associated surface-wave coupling) pushed from 64GHz to a certain frequency above 67GHz.

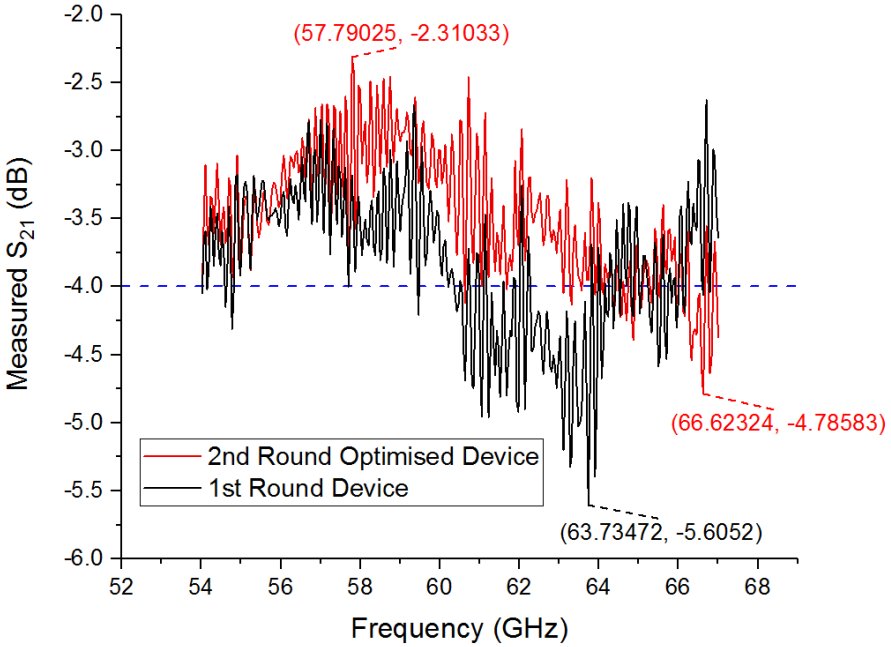


Fig.105 Measured Insertion Loss of 1st Round vs. 2nd Round Devices, 0V Bias

Since the 2nd round devices are 10% longer in the tunable part as compared with those of the 1st round (for phase shift optimisation already confirmed), this partially cancelled out the insertion loss mitigation due to the optimisation measures outlined in section 7.2.1. Since both phase shift and insertion loss are length-dependent, we quantify in Fig.106 below a widely-used comparison criterion called the figure-of-merit (*FoM*), which is based on the ratio of the maximum differential phase shift (between the saturation bias and 0V bias) to the maximum insertion loss (normally 0V bias). A maximum FoM of 68°/dB is reported for the 1st and 2nd round optimised devices across 54GHz to 67GHz.

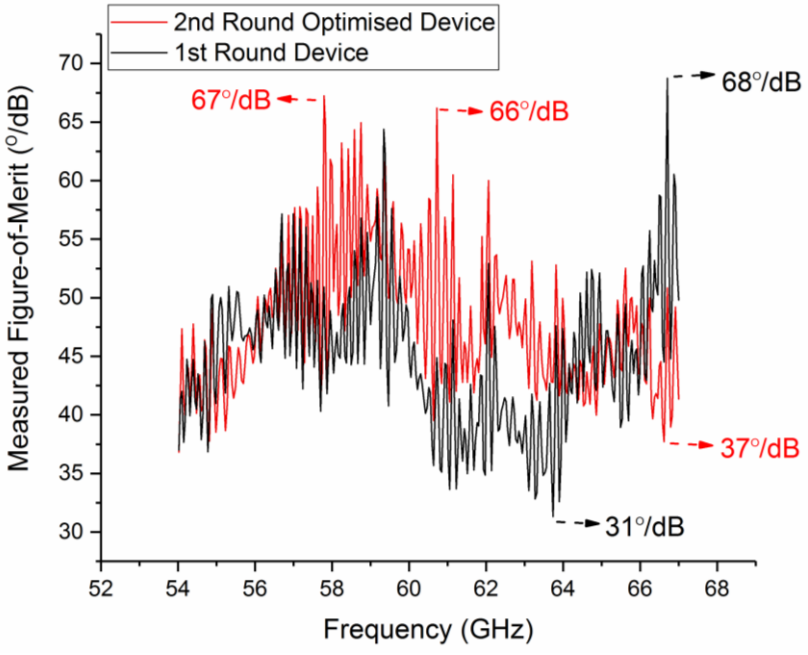


Fig.106 Measured Figure-of-merits of 1st Round vs. 2nd Round Devices

Arguably, the *FoM* analysis only partially reflects the device's tuning performance, as it overlooks a variety of other important properties, e.g. the device's size, the linearity of voltage response, and the driving circuit's power consumption. Resulting from this study, the control voltage for a π shift at 66GHz has been scaled down to 10V by our 2nd round optimised devices compared with 20V for the 1st round devices.

7.2.3 Optimisation of Conductor Surface Treatments

7.2.3.1 Optimum Gold-plating Thickness on Cu with no Nickel

The effect of nickel-free gold plating on the final device's insertion loss is measured in Fig.107, based on the optimised device structure and geometry used in the 2nd round design,

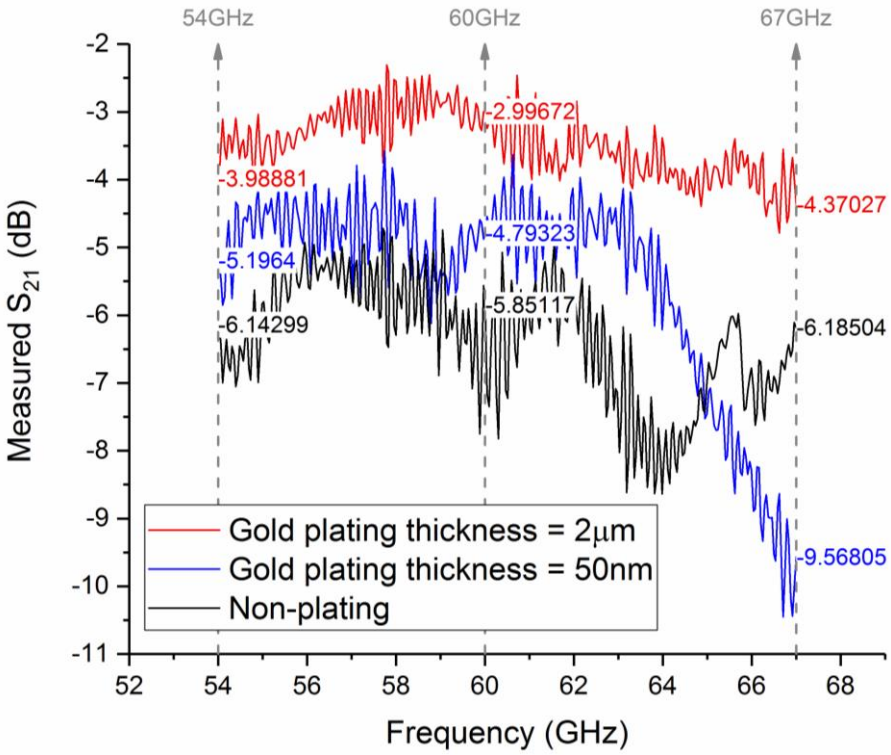


Fig.107 Measured Insertion Loss (0V Bias) of Devices with Diverse Gold-plating Thicknesses (All based on 2nd Round Design Geometry)

For the devices with non-plated Cu conductors (oxidised), the measured deterioration of insertion loss (it degrades up to 4.5dB at 64GHz when compared with the devices plated with an optimal thickness) demonstrates that relying purely on the polyimide coating (as alignment agent) has limited scope in preventing oxidation of the bare Cu.

The insertion loss degradation is even worse for the devices with 50nm gold-plated especially above 65GHz. Tarnishing due to Cu migration into gold during the polyimide baking process (200˚C for 30 minutes) raises a problem of oxide layer formation. The coexistence of the tarnishing and oxidizing effects exacerbates the increase in metal loss by 3.4dB at 67GHz as compared with no gold plated (oxidised).

Instead, the increase of plating thickness to 2μm reliably fixes the elevated metal loss problem caused by oxidation and tarnishing, as verified by the marked improvement in S_{21} across 54GHz-67GHz. Measurement results reported in the last section (7.2.2) are based on this optimal gold-plating thickness. Regarding metal surface roughness after plating, a number of cleaning processes are performed during the photolithography process on Cu, which change the surface topography and hence never achieve a mirror finish.

7.2.3.2 Measured Surface Roughness Impact on Insertion Loss: RA Cu vs. ED Cu

Devices are fabricated based on rolled annealed copper (RA Cu), and standard electrodeposited copper (ED Cu), respectively, then gold-plated with the optimal thickness derived above. They differ only in the Cu surface roughness at the dielectric side (Cu-PTFE interface), with all the other variables kept the same (e.g. circuit dimensions, LC thickness, gold-plating thickness, etc.). The sensitivity of insertion loss to copper surface roughness (dielectric side) is measured.

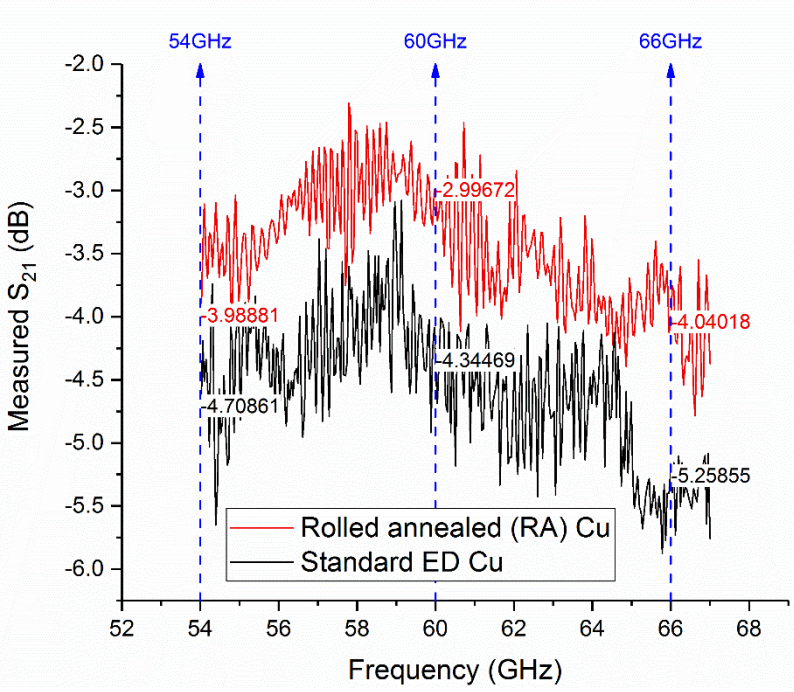


Fig.108 Measured Insertion Loss (0V Bias) of Devices based on Two Different Types of Cu Foils with Diverse Roughness (Both based on 2nd Round Design Geometry)

Electric field and current intensity are higher at the top edge of the metal as compared with that of the bottom, by the nature of electromagnetic waves at millimetre-wave frequency. However, the use of smoother RA Cu instead of ED Cu (which reduces the roughness at the bottom side) can mitigate insertion loss by at least 1dB. In conclusion, we experimentally obtained the optimum surface treatment at 60GHz for our LC-based ECPW structure, which is the employment of 2μm-thick gold-plating (nickel-free) and rolled annealed Cu with lowest surface roughness up to date.

7.3 Measured Performance Compared with State-of-the-arts

Measured performance of the optimised device at 66GHz is compared with up-to-date documentations covering state-of-the-art millimetre-wave phase shifters realised in a variety of technologies and structures.

7.3.1 Summary of Performance Comparison with Different Technologies

Figure-of-merit, defined as the ratio of maximum achievable phase shift to the maximum insertion loss among all control states, constitutes a partial view of the performance evaluation. We have pointed out in section 7.2.3 the limitation of this widely-used comparison approach, i.e. in only providing a big picture of the phase shift per insertion loss but suffering from a lack of evaluation on other device properties. Therefore, we also focus on individual performance indicators for a case-by-case device comparison.

7.3.1.1 Different Technologies Compared at a Same Frequency

As shown in Table 13 below, our wideband (54-66GHz) phase-shifting solution outperforms solid-state technology in terms of lower insertion loss (-4dB>-5.9dB).

Our modest-loss solution is even as competitive as those state-of-the-art MEMS and magnetic-biased waveguide. Note that the phase shifter measurements in other people's work are predominately performed by on-wafer probe-based setups with no connectors, under which case the insertion loss can be underestimated significantly as compared with our device with connectors included.

Table.13 Measured Performance of 66GHz Phase Shifters Realised by Different Technologies

Reference	Technology	f	Max. Shift	Min. S_{21}	FoM
[27]	SiGe BiCMOS	66GHz	180˚	-5.9dB	31˚/dB
[25]	Distributed MEMS (4-bit)		182˚	-2.7dB	67˚/dB
[13]	LC and MEMS		74˚	-2.0dB	37˚/dB
[39]	LC-based Substrate Integrated Waveguide (Magnets Bias)		300˚	-8.5dB	35˚/dB
[68]	LC-based Ridged Waveguide (Magnets Bias)		325˚	-4.6dB	70˚/dB
[88]	LC-based Microstrip (Gold Plated and Analogue Voltage Bias)		180˚	-10dB	18˚/dB
This work	LC-based Enclosed CPW (ECPW) (0-10V Analogue Voltage Bias)		**180˚**	**-4.0dB**	**45˚/dB**

Compared with our LC-based device, the MEMS-based phase shifter reported at 66GHz exhibits a lower insertion loss (-2.7dB > -4dB) for a phase shift of π. However, the MEMS solution is inherently digital and hence resolution-limited when integrating in a beam steering system. Furthermore, the reliability and robustness merits further investigation for a clearer picture of its competitiveness over LC.

Regarding LC-based waveguide technology, the ridged waveguide phase shifter [68] presented in the 36th European Microwave Conference provides the best performance in terms of highest phase shift and lowest insertion loss realised at the same time. The LC material they deploy is MDA-03-2844 (a highly anisotropic mixture synthesised by Merck), with a 100μm cell gap and 17mm in the tunable length. However, as already pointed out in section 2.3.1, the major disadvantage of the waveguide approach lies in the bulky and power-consuming networks required by magnetic control, as well as slow response time. Although in [68]'s work that the || state can be achieved by 10V driving, the ⊥ state can only be realised by a magnetic field, which significantly limits its potential for applications requiring light-weight and low-power

consumptions. Arguably, LC-based phase shifter realised in waveguide structure is bulky, power-consuming and extremely slow, hence only suits for limited applications such as the inter-satellite link.

7.3.1.2 Comparison of LC-based CPW-related Structures

Keeping an eye on the CPW-related structures with LC (Table 14 below), we observe that our ECPW solution is the best in terms of both high tuning range and low insertion loss.

Table.14 Measured Performance of Phase Shifters Realised by CPW-related Structures

Reference	Structure	f	Max. Shift	Min. S_{21}	*FoM*
[23]	LC-based CPW (Tuning in 2 Slots)	40GHz	17˚	-4.3dB	3.9 ˚/dB
[1]	CPW Piezoelectric		45˚	-1.8dB	25 ˚/dB
[23]	LC-based Microstrip with CPW Access		90˚	-8.5dB	11 ˚/dB
This work	LC-based Enclosed CPW		112˚	-2.4dB	**46.7˚/dB**
[77]	LC-based CPW with ITO as FE	60GHz	60˚	-15dB	4˚/dB
This work	LC-based Enclosed CPW		162˚	-3dB	**54˚/dB**

Arguably, each of these millimetre-wave technologies exhibits a distinct trade-off between phase shifting range, insertion loss, cost, operating bandwidth, linearity, signal-to-noise figure, power handling, power consumption, response time, reliability, lifetime, packaging, robustness, size, large-scale integration, and weight. The comparative study made in the tables above is very high level and scope-limited, as different technologies and different devices done by other people were based on different treatments. Detailed comparison in properties of interest is reported in the following sections in the format of a case-by-case review of our device versus selected state-of-the-arts to justify the advantages and limitations.

7.3.2 Discussion on Phase Tuning Range and Linearity: ECPW vs. CPW

As measured in the last chapter (section 7.2.2), our device features a 0-180° continuous tuning capability (66GHz), and ease of low-voltage electronic control with linear phase shifting agility from 4V to 10V. We compare the measured voltage response of the GT3 LC-based ECPW phase shift in this work with that by a K15 LC-filled standard CPW phase shifter [23] at 40GHz, as depicted in Fig.109 below.

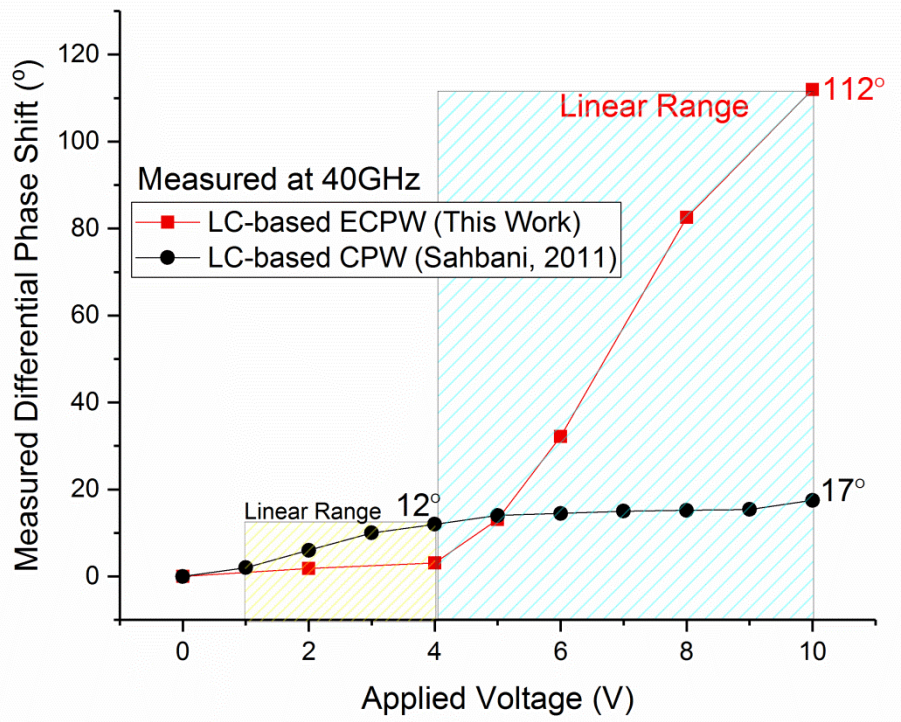


Fig.109 Measured Voltage Response of Differential Phase Shifts for the Proposed LC-based ECPW vs. CPW

With different LC materials used (dielectric properties shown in Table 15 (a) below), different structures (ECPW vs. CPW) and geometries (detailed in Table 15 (b) below), our device structure (ECPW) features a higher threshold voltage of LC switching (from 4V) as compared with that of the CPW structure (from 1V). The threshold voltage difference is due mainly to the diversity in LC materials' elastic constants (splay and twist), as well as diverse low-frequency field intensity in different cell gaps (ECPW with 140μm vs. CPW with 40μm).

The saturation voltage of the K15-based CPW in the literature is 4V, corresponding to a differential phase shift of only 12°. As shown in the interface between the two linear regions marked in Fig.109 above, the saturation voltage of the K15-based CPW is approximately the threshold voltage of our GT3-24002-based ECPW. The classical K15 LC for the display

industry is arguably not suitable for millimetre-wave applications, as explained by the material's figure-of-merit at 60GHz, which is 10 times lower than that of the GT3-24002 we use.

Table.15 (a) LC Materials used in this Comparative Study

LC Materials	Orientation	ε'_r	$tan\delta$	$\varepsilon'_r tan\delta$	Tunability	$\frac{Tunability}{\varepsilon'_r tan\delta\ (\perp \text{state})}$
K15 [23]	||	2.98	0.04	0.1192	13%	0.6
	⊥	2.64	0.08	0.2112		
GT3-24002	||	3.3	0.0032	0.01056	32%	10.41
(This Work)	⊥	2.5	0.0123	0.03075		

Table.15 (b) CPW-related Structures and Geometries used in this Comparative Study

Structures	Top LC Layer	Tuning Areas	Core	Slots (Gaps)	Length
CPW [23]	No	2 Slots (Gaps)	100μm-wide 35μm-thick	40μm-wide	14mm
ECPW **(This Work)**	Yes (140μm-thick)	Top Layer and 2 Slots (Gaps)	293μm-wide 17μm-thick	203μm-wide	18.3mm

Though exhibiting a higher threshold voltage by using our ECPW structure, the high tuning range and hence large differential phase shift per unit length allows a much superior device functionality than the CPW. The high tuning range is not only owing to the higher anisotropy of LC material we use, but is more importantly, attributed to the planar structure advantages offered by the proposed ECPW as well as the optimisation we performed in Chapter 4. We have already pointed out in section 2.5.6 the structure limitations of the LC-based FE-free CPW with tuning only based on the two vertical slots. But even with such a structure (the one we are comparing with in the above table) and a fixed LC material, we can still improve the tuning range noticeably based on the proposed concept of competing wave-occupied-volume ratio in tunable vs. non-tunable media, as evidenced by the FE-free CPW structure we studied in Chapter 2.5 (published in the 46th European Microwave Conference).

7.3.3 Comparison on Signal-to-noise Ratio: ECPW vs. CPW with FE

The LC-based enclosed CPW (ECPW) phase shifter we developed is compared with the conventional CPW with floating electrode (FE) on top, in relation to the signal-to-noise ratio (*SNR*). The comparative measurement results in Fig.110 below demonstrates our improvement in the signal-to-noise ratio (*SNR*) drastically across a wide band from 57GHz to 66GHz.

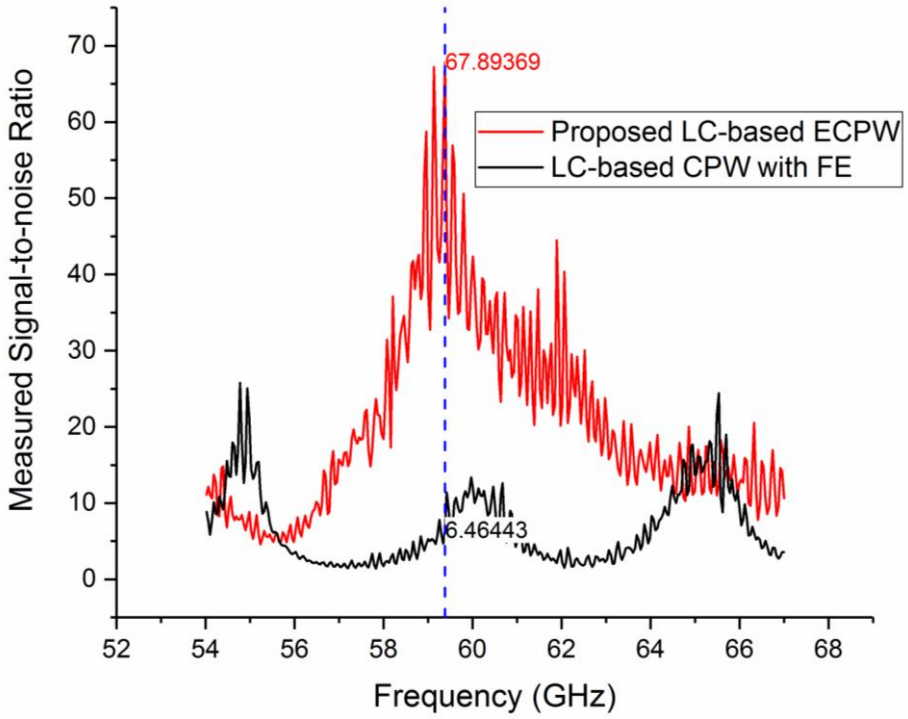


Fig.110 Measured Signal-to-noise Ratio of the Proposed LC-based ECPW vs. CPW with FE

The proposed ECPW structure including an enclosed ground in the design appreciably reduces the instability due to the floating effect of the transmission line. Further analysis is performed by a loss-decomposition simulation at 60GHz, concerning the power percentage in signal transmission, signal reflection (due to mismatching and higher-order modes), material absorptions by dielectrics and metals (including energy from the fundamental mode, as well as the stray modes), higher-order modes and surface wave radiation into the free space. The results are summarised in Fig.111 below.

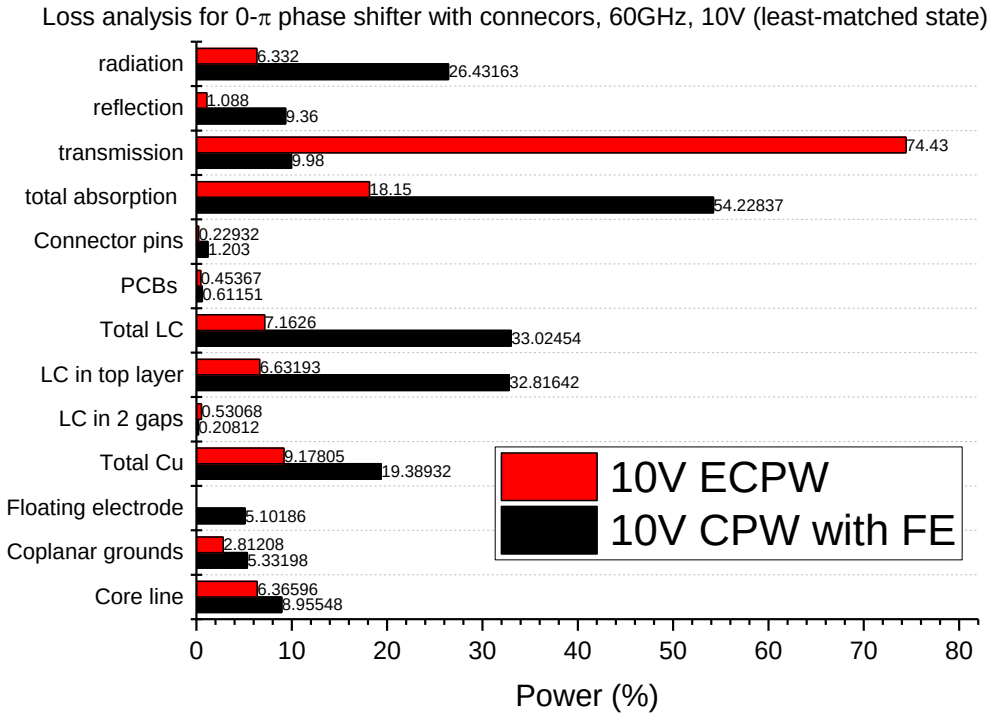


Fig.111 Loss Analysis of LC-based Phase Shifter by FE-CPW vs. the Proposed ECPW

As shown in the loss-decomposition comparative analysis between ECPW and CPW with FE, the proposed ECPW achieves suppression of higher-order spurious modes radiation into the free space by 20% and reduces LC absorption loss by 26% due to the elimination of extra dissipations introduced by the higher-order modes. For the similar reason, the total metal loss also decreases by 10%. And the return loss is reduced by 8%. In total, the total transmission is improved by 65% (in another words, insertion loss reduces by 65%).

7.3.4 Material Absorption Loss Analysis

Our low-reflection device structure is amenable to loss-decomposition analysis both experimentally and theoretically when compared with documentation [35] who performed a simulation concerning various sources of insertion loss in a LC-based microwave variable delay line. By simulation and confirmed with experiments, the material loss in our ECPW structure at 66GHz is substantially due to the LC dielectric absorption, followed by the metal loss due mainly to the core line. Therefore, device optimisation can centre upon the LC dielectric loss minimisation (whilst keeping a fixed phase tuning range). As will be covered later in section 7.6.1, this problem can be transferred into a search of LC materials with an improved material's figure-of-merit (defined as the ratio of tunability to $\varepsilon_r' tan\delta$ at the $\perp$ state).

7.4 Discussion on Device Scalability

7.4.1 Scalability for 70GHz-90GHz

We have currently only verified our low-loss device performance up to 67GHz, due to the limit in the measurable frequency range (1MHz-67GHz) of our vector network analyser. However, it has already been experimentally confirmed in Chapter 7.2 that the bandwidth limitation of our ECPW structure lies chiefly in the enclosure's cavity width (spacing of the continuous sidewalls), which limits the highest frequency before the onset of higher-order waveguide modes coming into play. Based on existing experiment results, we can envision that the proposed LC-based ECPW phase shifter structure is very likely to be scalable for a higher frequency (e.g. 70GHz-90GHz) for extended applications.

According to the wavelength shrinking and components' size scaling, the same design and optimisation procedures as mentioned in this work can be followed for pushing the ECPW structure to operate towards 90GHz or higher (up to 110GHz), except for the concern of increased sensitivity of the insertion loss to today's manufacturing tolerances. For instance, our current 60GHz design of the cavity width includes reservation for screwing tolerances (including holes' position and diameter tolerances) to avoid the connector pin short-circuiting with the CPW grounds. The 2nd round optimised device is well-mounted and demonstrated with minor concern for this tolerance.

However, the same mechanical tolerances tend to make a difference for 90GHz where a subtle misalignment of a single component (e.g. 1mm connector for 90GHz measurement instead of the current 1.85mm connector) can lead to signal disruption and device malfunction not noticeable at 60GHz. The philosophy behind that is identical to the one we have successfully tackled in this work when bringing LC-based phase shifters from microwave to millimetre-wave applications.

Besides size scaling down, the strategy we propose for operating frequency upgrade (to 90GHz) includes tailoring the whole device structure especially the components mounting scheme. Furthermore, filling LC using a vacuum chamber might be an alternative approach as compared with the standard capillary effect, which struggles to wet the >1cm-long cavity with reduced

width (90μm for 90GHz). We propose in section 7.6.3 a method to relieve the tight tolerance of the cavity width by introducing artificial magnetic conductor (AMC) for the ECPW's ground plane. We will confirm these possibilities in the future as soon as a frequency extender is installed on the network analyser.

7.4.2 Scalability for 2π Phase Shifting

Based on our optimised design for a differential phase shift of π, a 2π-shifting device is scaled by only extending the line length, whilst keeping other design parameters unchanged. By experiment, we observe that the post-baked 5880 substrate (3.5cm-long) exhibits unacceptable bending, resulting in unignorable gaps between the enclosure and the substrate when assembled. The substrate's non-uniformity can cause a series of long-term reliability problems (recalling the long-term effect of stress relief explained in Chapter 4.3), such as LC leakage from cavity, and the standing-wave resonance and higher-order modes radiation as mentioned earlier. A method to minimise the etch shrinkage can be attempted by double etching, which is a two-step lithography process.

Arguably, the non-uniformity induced problems become more pronounced when dealing with a longer-scale substrate like this one. In addition, increased fabricating errors due to spin-coating of alignment agent on a longer substrate and increased uncertainty in the LC-filling a longer channel can degrade the electrical performance further. A way to address these is by bending the CPW pattern. Modes distortion due to a curved bend is simulated in Fig.112 below.

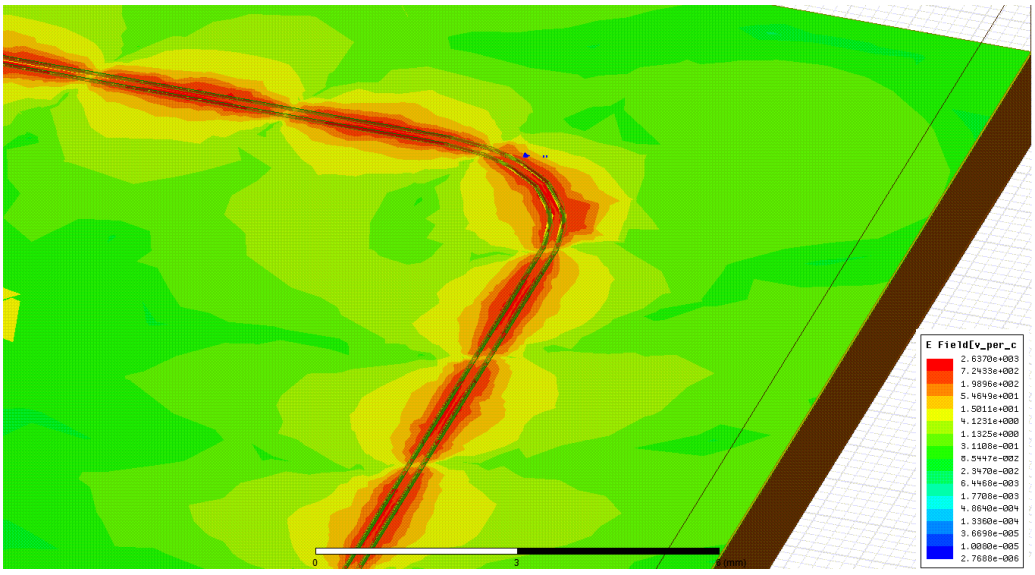


Fig.112 60GHz Electric Field Intensity of the Proposed Enclosed CPW with a Curved Bend

Further optimisation measures and other research possibilities are outlined in Chapters 7.5 and 7.6, respectively.

7.5 Controlling 60GHz Field Distribution by Tailoring the Electrodes' Profile

7.5.1 60GHz Field Homogenisation

It is worth noting from the measured conductor's cross-sectional profile that trapezoidal edges are observed as distinct from the designed right angle ones. The implication of this on insertion loss is studied by simulation. We have derived the peak phasor form of metal' absorption power in Chapter 3.4.2, i.e. the core line's conductor loss (thickness T_{strip} considered) per unit length is given by:

$$P_{core_{s_0}}=[\int_{x=0}^{w_{strip}} \sigma E_s(x,y=0)_0 dl + \int_{x=0}^{w_{strip}} \sigma E_s\left(x,y=-T_{strip}\right)_0 dl]^2 \times \frac{\sqrt{\pi f \sigma \mu}}{\sigma w_{strip}}$$

$$+2[\int_{y=-T_{strip}}^{0} \sigma E_s(x=0,\ y)_0 dl]^2 \times \frac{\sqrt{\pi f \sigma \mu}}{\sigma T_{strip}} \quad \text{……..…(38)}$$

Due to the proximity effect, $E_s\left(x=0\ or\ w_{strip}\right)_0 > E_s\left(0<x<w_{strip}\right)_0$ and $E_s(x,y=0)_0 > E_s(x,y=-t)_0$ at most x values.

As derived in section 3.4.3, LC volumetric loss per unit length at 0V biasing is given by:

$$P_{LC_{s_0}}=2\pi f \varepsilon_0 \varepsilon_r' tan\delta \int_{x=0}^{w'} \int_{y=0}^{T_{LC}} \left|\overrightarrow{E_s(x,y)_0}\right|^2 dxdy \quad \text{……(39)}$$

From eqs.38 and 39, the integration of $\left|\overrightarrow{E_s(x,y)_0}\right|^2$ at the electrode surface concerns metal loss, while the product of $\varepsilon_r' tan\delta$ and the integration term of $\left|\overrightarrow{E_s(x,y)_0}\right|^2$ within the dielectric volume concerns dielectric loss. We therefore propose to reduce the total material absorption loss by levelling off $\left|\overrightarrow{E_s(x,y)_0}\right|$ (i.e. shaping the field more homogeneously distributed) at the biasing state when $\varepsilon_r' tan\delta$ is maximum (i.e. at 0V). This can be done in certain ways as below.

(1) Shaping electrodes' profile (contour)

(2) Introducing a back conductor (or defected conductor) to fully (or semi) enclosed the core line

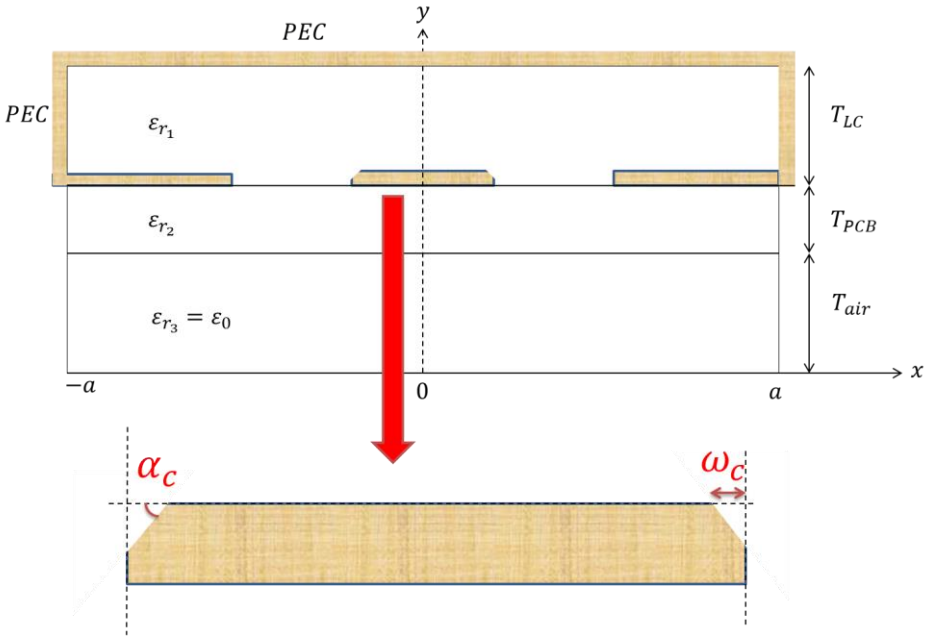
(3) A combination of the above methods

Due to the change of $\left|\overrightarrow{E_s(x,y)_0}\right|$ distribution, the corresponding change in tuning range is compensated by adjusting the line length to maintain a phase shift of π. Integrating the power per unit length over the required length for π shift, we expect to see a decrease in materials'

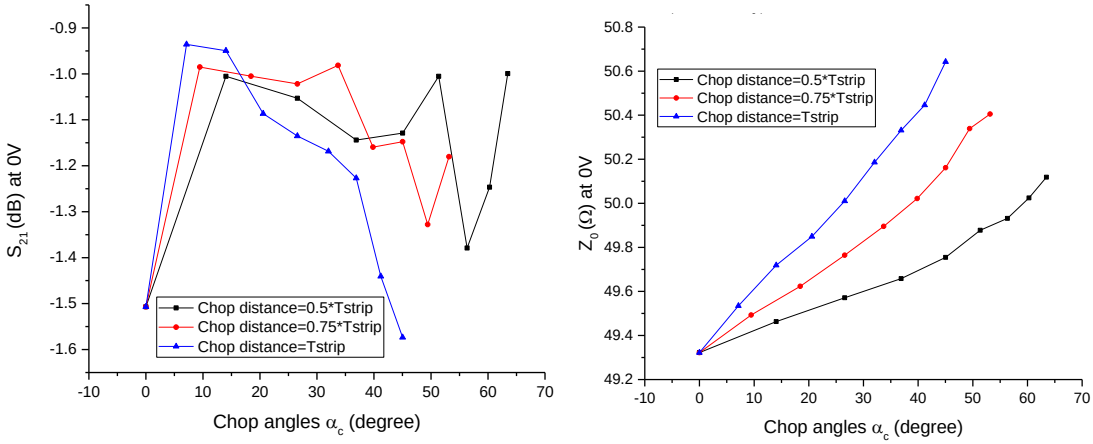
absorption loss by utilizing the non-linear relation between loss and the field intensity. First, chopping positions and chopping angles of the guiding conductors are studied.

7.5.2 Hexagonal Core, Right-Angled Ground

With a chop angle α_c and chop distance w_c shown in Fig.113 (a) below, the guiding conductor(s) can be shaped in different forms. For a hexagonal core and right-angled grounds, simulated performance is parametrised with chop angle and chop distance in Fig.113 (b).



(a) Enclosed CPW (ECPW) with Hexagonal Core and the Zoomed-in View

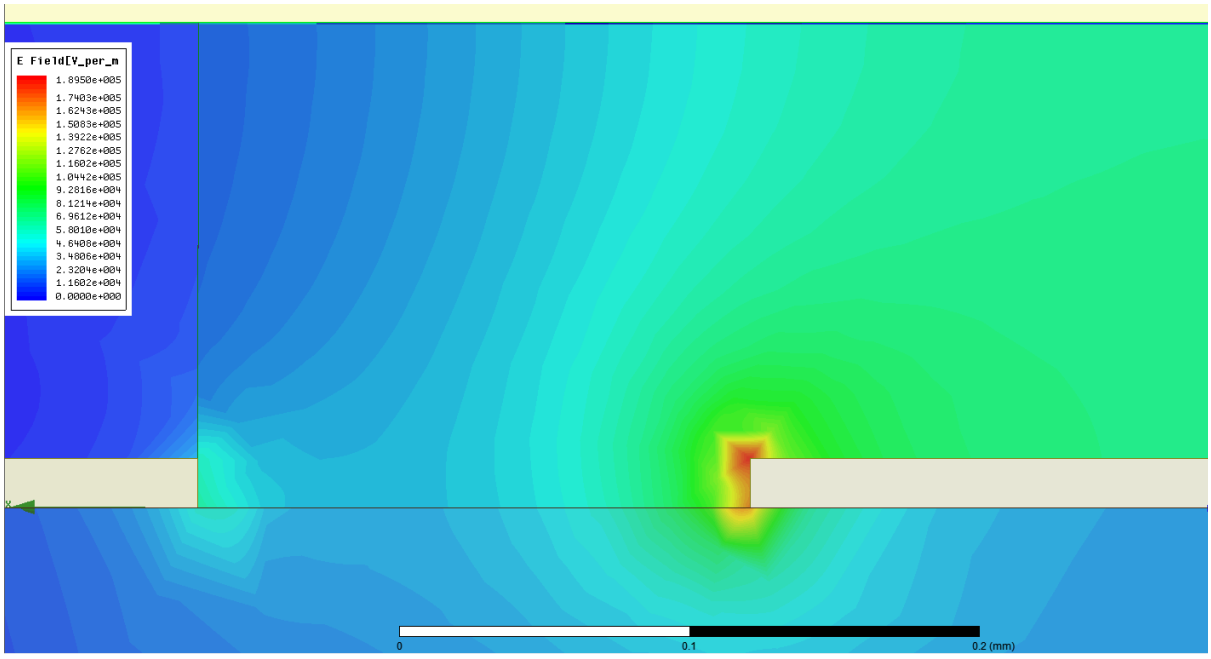


(b) Simulated S_{21} and Z_0 vs. the Chopping Angles and Chopping Distances

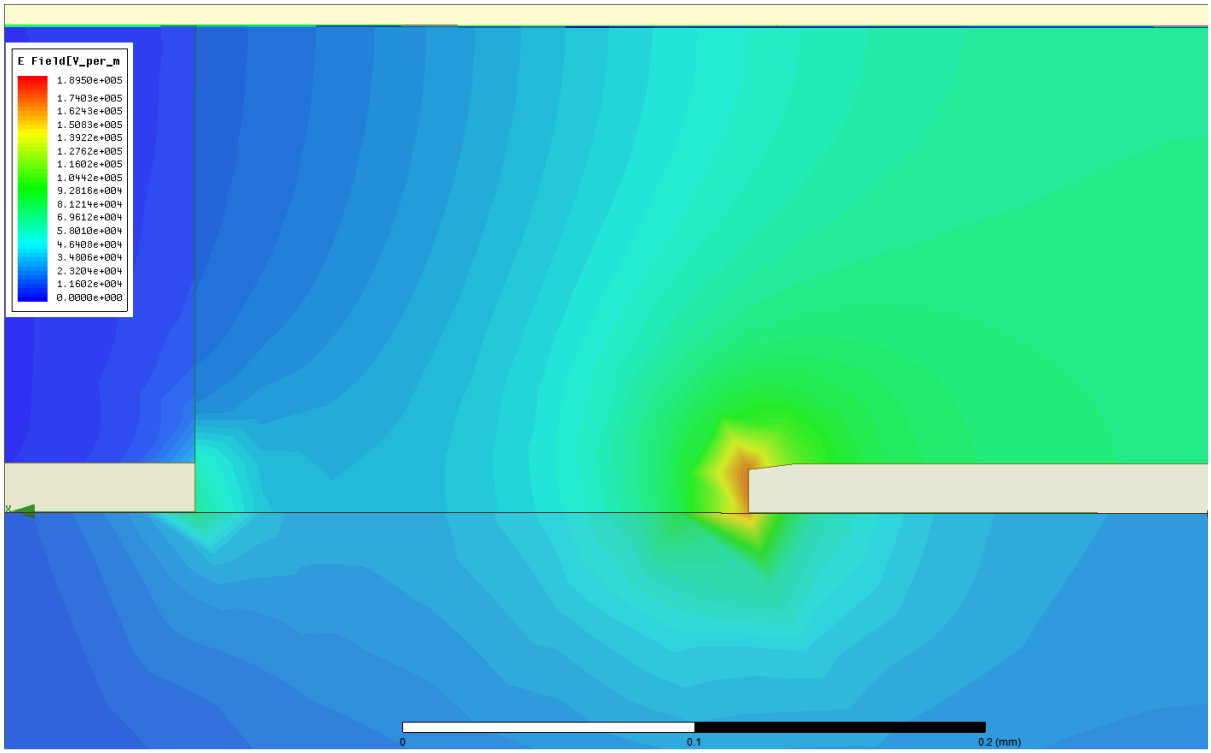
Fig.113 Impact of Chopping Positions on Performance of ECPW with a Hexagonal Core

The peak phasor quantity $\left|\overrightarrow{E_s(x,y)_0}\right| = E_0$ representing a time-harmonic E field is computed and portrayed below in Fig.114. For the comparison reason, the range of colour bar of each figure is unified (using the one with optimal performance as a reference). Ideal rectangular

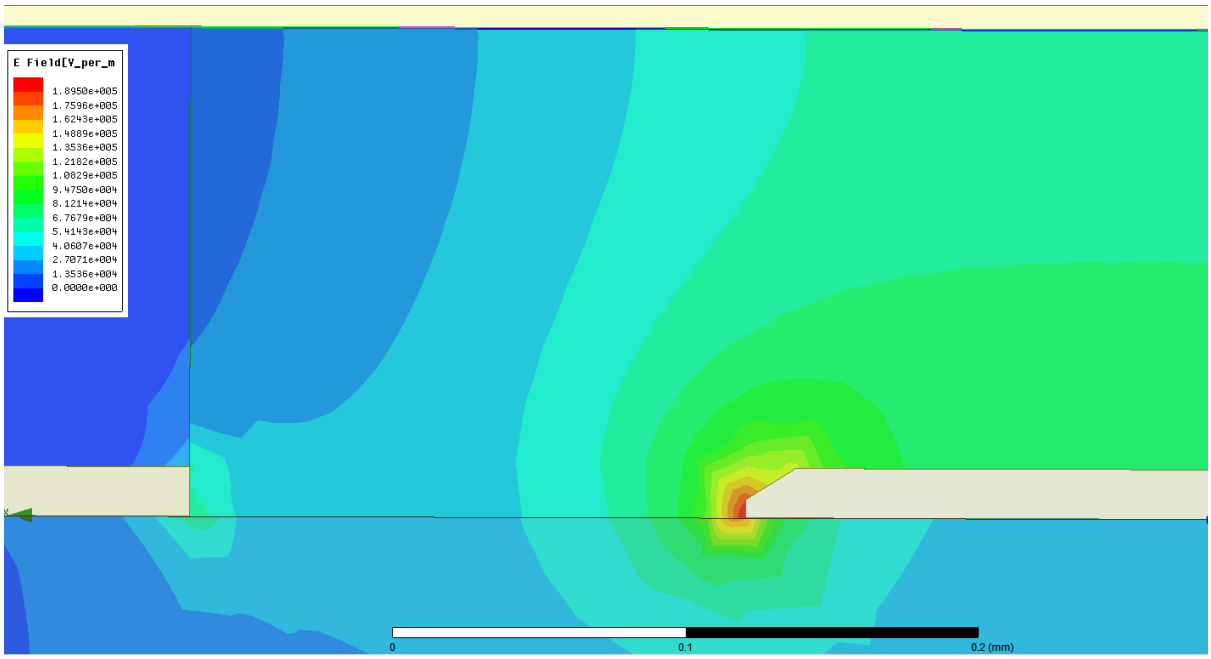
electrode structure exhibits the dominant current density at top edges of the core where max. $\left|\overrightarrow{E_{sx_0}} + \overrightarrow{E_{sy_0}}\right|$ occurs. We find the optimal chopping position is with α_c =7.12°, w_c=17μm as shown in Fig.114 (b), while the further increase of the chopping angle degrades S_{21}, as illustrated in Fig. 114 (c).



(a) Core α_c = 90°, w_c=0, Peak E_0=2333V/cm, S_{21}= -1.50704dB (right-angled one)



(b) Core α_c = 7.12°, w_c=17μm, Peak E_0=1895V/cm, S_{21}= -0.93575dB (Optimised)



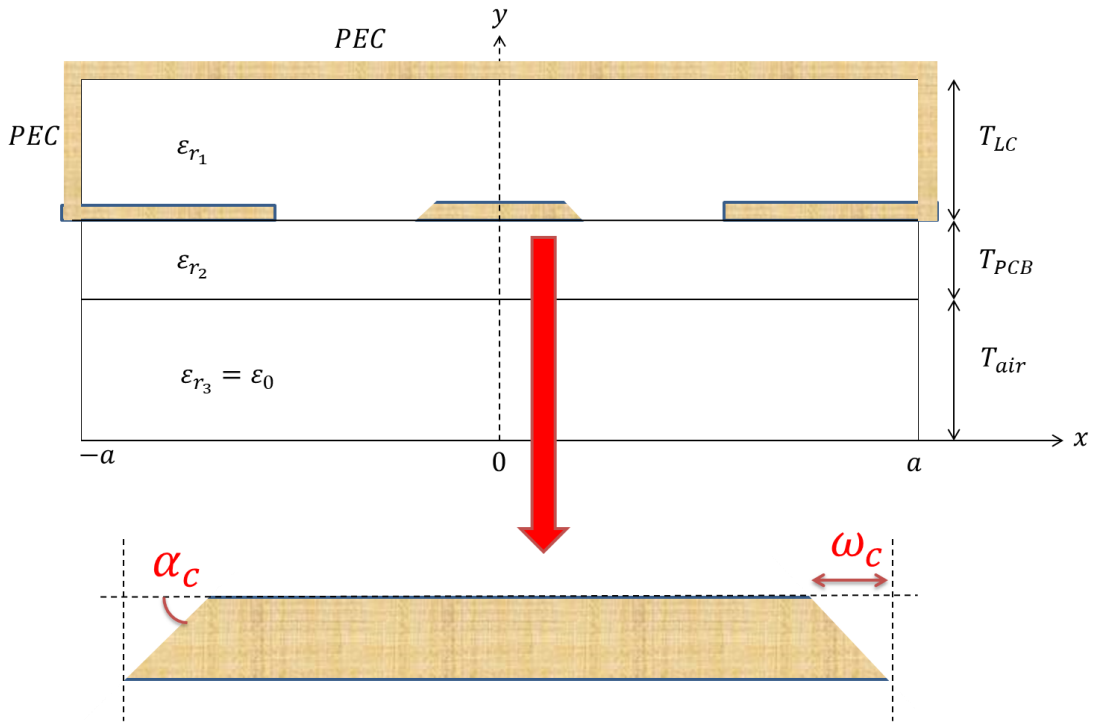
(c) Core α_c =32.02°, w_c=17μm, Peak E_0=2085V/cm, S_{21}= -1.16847dB

Fig.114 Optimising the Hexagonal Core's Chopping Positions (Angles and Distances) based on 60GHz Electric Field Homogenisation

By chopping the top edge by an optimal angle and distance (α_c=7.12°, w_c=17μm), the peak of E_0 (i.e. max. $\left|\overrightarrow{E_{sx_0}} + \overrightarrow{E_{sy_0}}\right|$) drops to the value where the local $E_0(x, y)$ exhibits a reasonably homogeneous distribution for material loss mitigation.

7.5.3 Impact of Trapezoidal Effect on the Increase of Insertion Loss

For a fixed chopping distance, when the chopping angle increases to the value where the hypotenuse intersects with the PCB substrate, the core (or ground) becomes a trapezoid as shown in Fig.115 (a). The simulated performance is parametrised against chopping angle α_c.



(a) Enclosed CPW (ECPW) with Trapezoidal Core and the Zoomed-in View

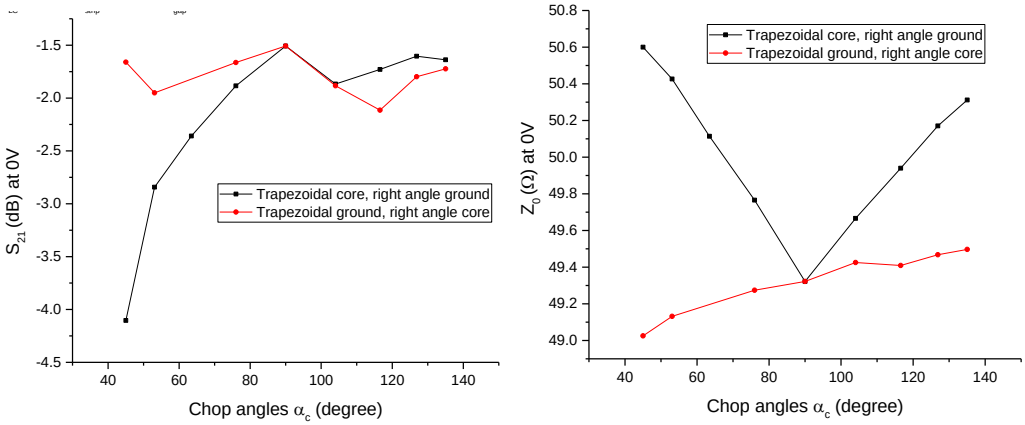
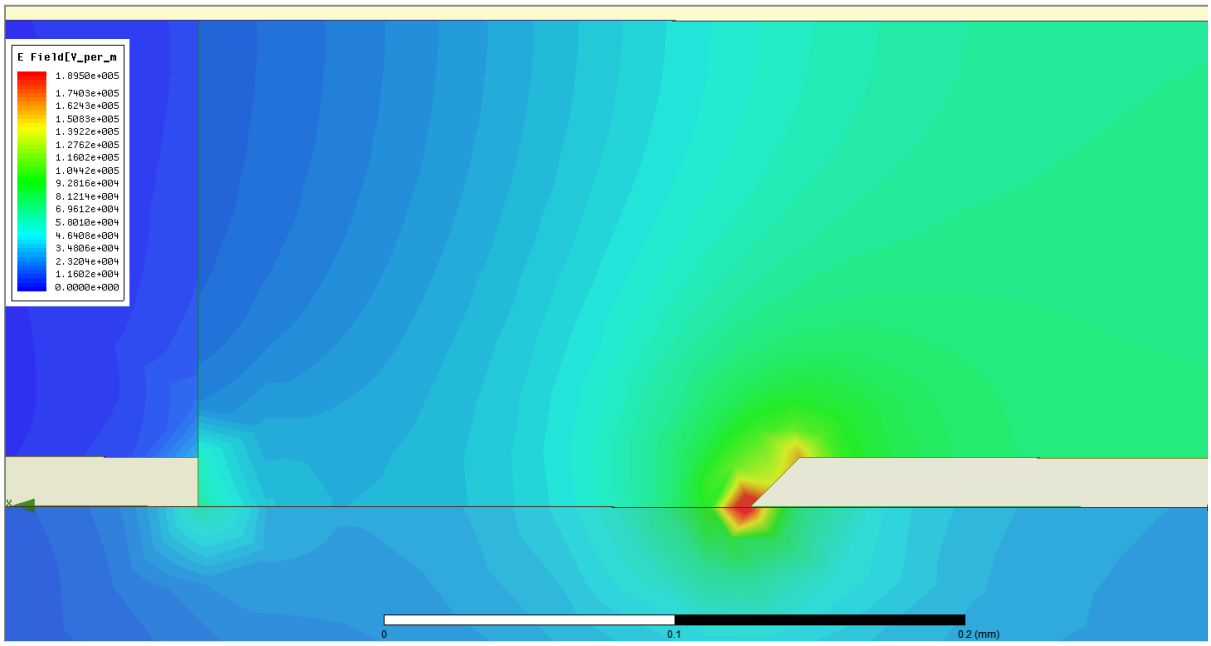


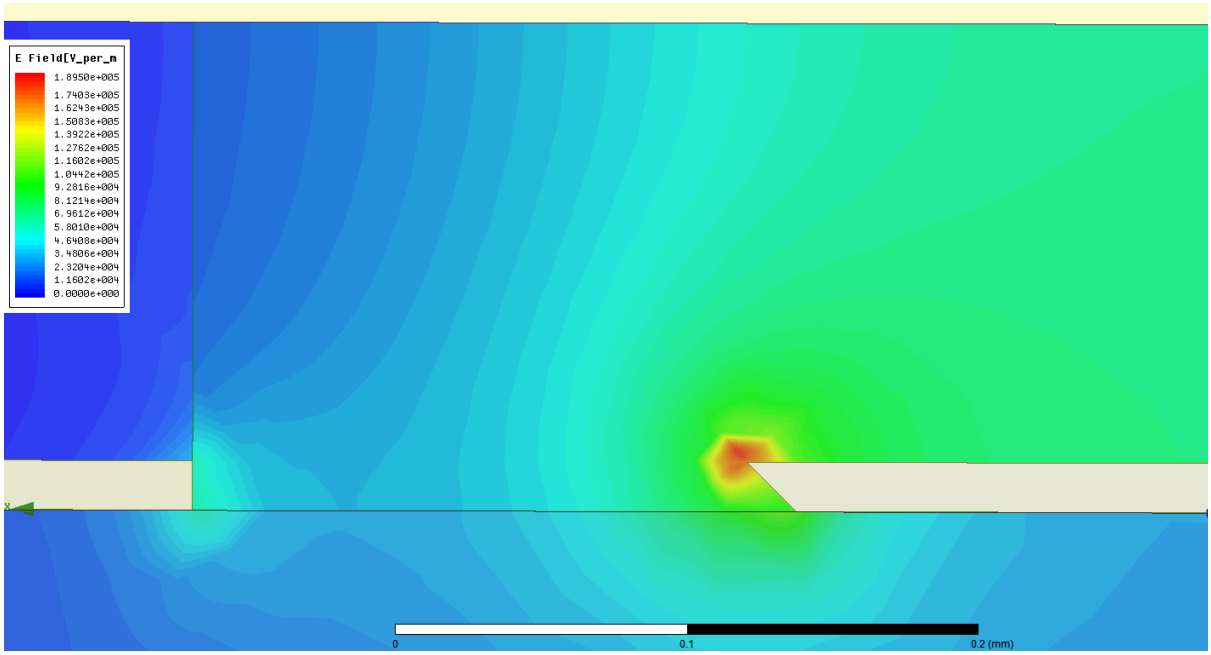
Fig.115 Impact of Chopping Angles on Performance of ECPW with Trapezoidal Conductor

Compared with right-angled conductors (i.e. core and ground both with chop angles=90°), trapezoidal effect (either acute or obtuse chop angles) increases the peak of E_0 and degrades S_{21}. The S_{21} degradation is more pronounced for the case of trapezoidal core with acute chopping angles. It is evident from Fig.116 (a) (d) below that a right-angled electrode design

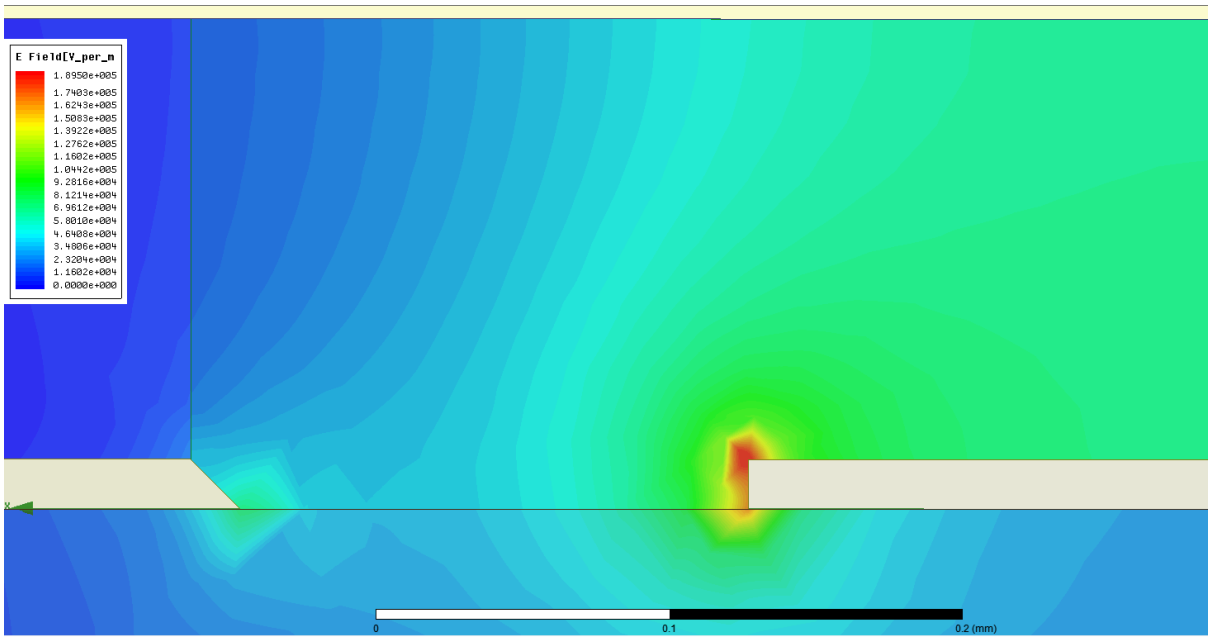
can be very sensitive to fabrication tolerance, as the trapezoidal one could degrade S_{21} by up to 2.6dB (assuming copper surface roughness=0). Moreover, when there is elevated current density at the base owing to this trapezoidal effect, the copper surface roughness will have more influence on losses and the propagation constant. In addition, Comparing Fig.116 (b) with (a), the undercut one (obtuse chopping angle) exhibits lower loss than the trapezoid with acute chopping angles.



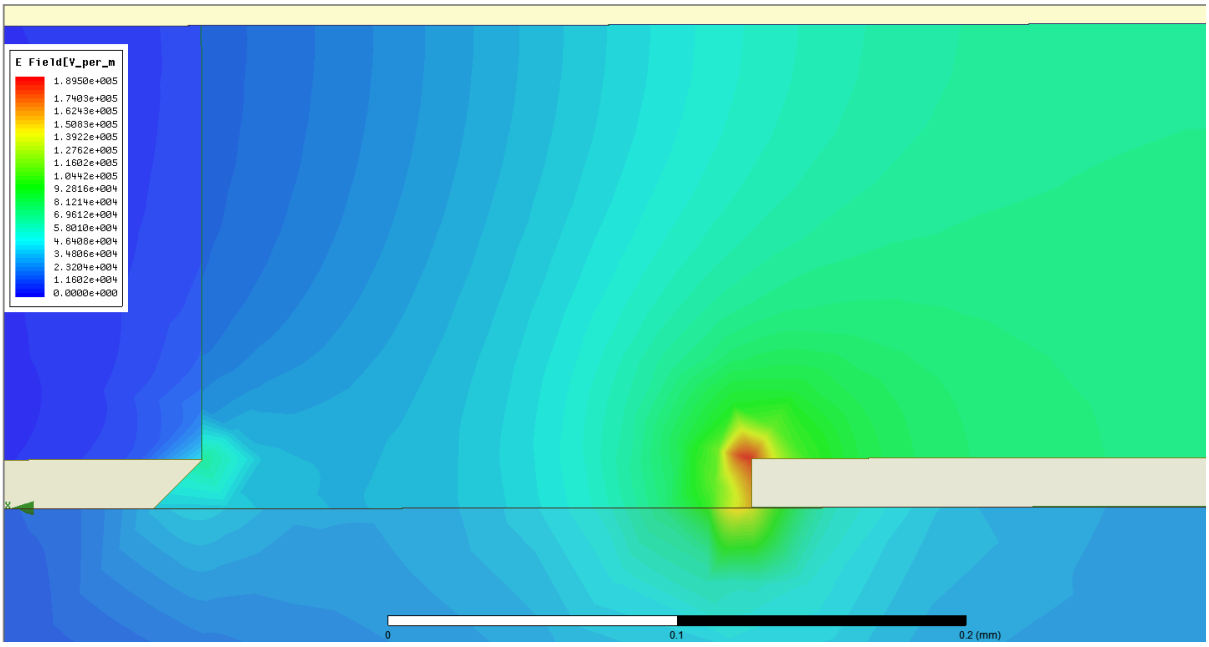
(a) Core α_c = 45°, w_c=17μm, Peak E_0= 3352.4V/cm, S_{21}= -4.1039dB (worst)



(b) Core α_c = 135°, w_c=17μm, Peak E_0= 2426.4V/cm, S_{21}= -1.6378dB



(c) Ground α_c = 45°, w_c=17μm, Peak E_0= 2422.6V/cm, S_{21}= -1.6598dB

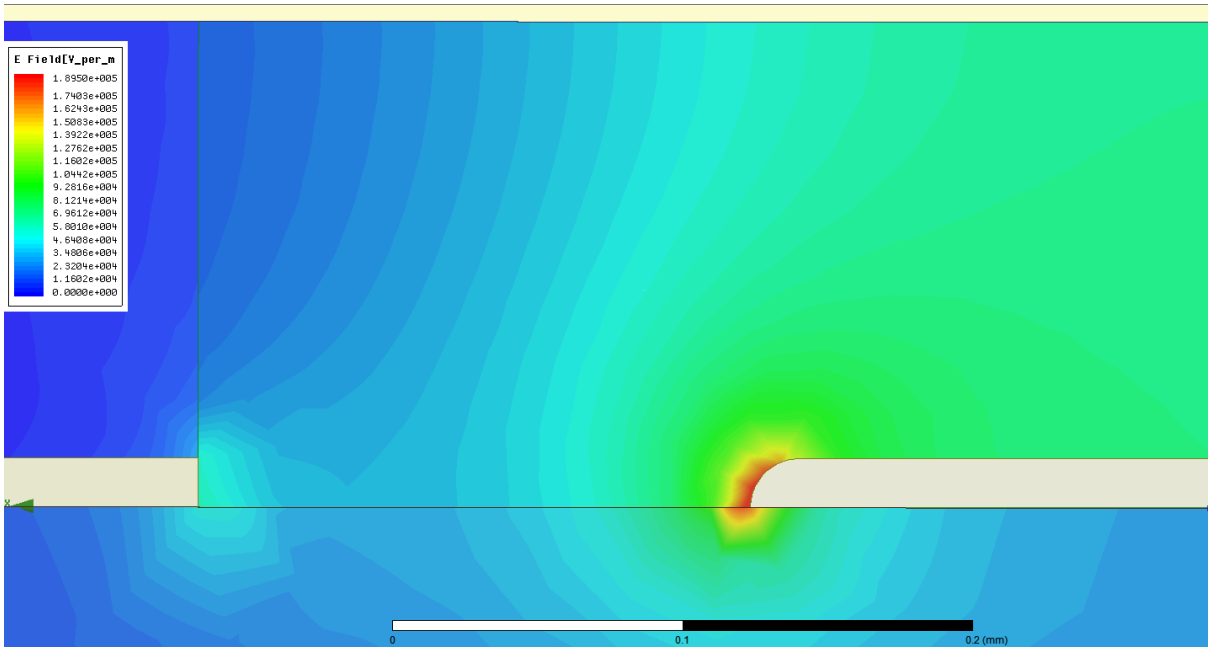


(d) Ground α_c = 135°, w_c=17μm, Peak E_0= 2469.6V/cm, S_{21}= -1.7236dB

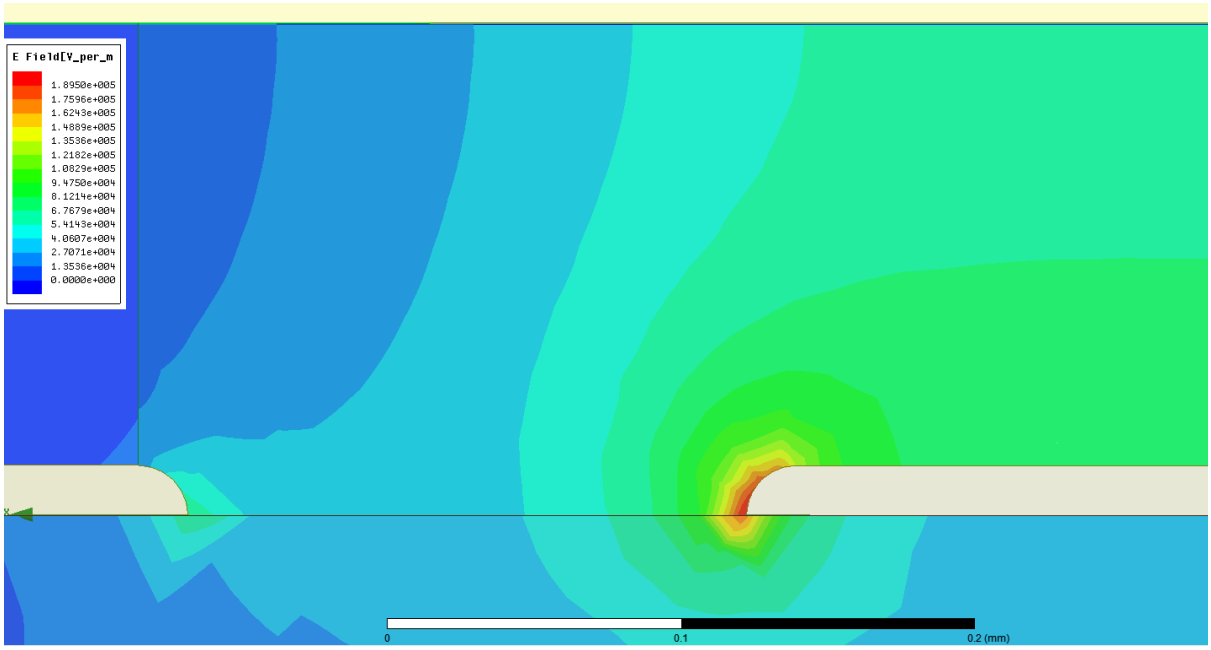
Fig.116 Impact of Trapezoidal Conductor Shapes on 60GHz's Field Peaking (Undesirable)

7.5.4 Round Conductor(s)

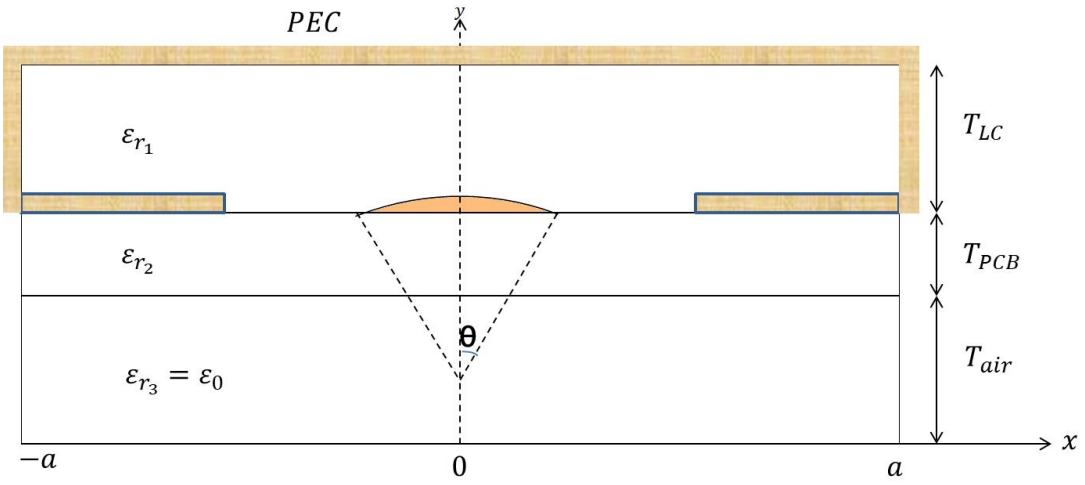
When the number of hypotenuses increases to infinity, the conductor edge becomes round. Comparing Fig.117 (a) with (b), insertion loss of the right-angled ground one is lower. This complies with the adverse trapezoidal effect we have investigated in the last section (7.5.3), thus a right-angled ground is preferred. However, the rounded core with right-angled ground performs no better than the one with the optimal hexagon core obtained in section 7.5.2. Furthermore, current fabrication techniques struggle to contour a round electrode profile.



(a) Core round edge radius r=17μm, Peak E_0 = 2487.1V/cm, S_{21}= -1.7739dB



(b) Core and ground round edges radius r=17μm, Peak E_0= 2656.9V/cm, S_{21}= -2.0891dB



(c) Other Shaping Possibility of the Rounded Core

Fig.117 Simulation of the LC-based ECPW with Rounded Conductor (s)

In conclusion, the optimal chopping position of the guiding conductors is with a hexagonal core, whereas the transmission performance is degraded with trapezoidal core or grounds, due to the inhomogeneous field distribution produced. The analysis made in this chapter quantifies the importance of minimising the trapezoidal conductor profile during the photolithographically patterning process.

7.5.5 Full Conductor-backing Enclosed CPW (CB-ECPW)

Owing to the proximity effect, signal current on the core line is drawn towards the ground planes-facing side (i.e. the edges), and confines the returning current on the top ground plane, mostly staying above the core line. In recognition of the integration term $\int_{x=0}^{w}\int_{y=0}^{h}\left|\overrightarrow{E(x,y)}\right|^2 d\,S$, reducing $\left|\overrightarrow{E(x,y)}\right|$ in the LC region (partially surrounding the core line) may reduce the total loss, although at the cost of increasing LC volume (line length) to reach the same differential phase shift level.

Therefore, we modify the enclosed CPW (ECPW) structure by introducing a conductor backing with vias shorting it, such that the proximity effect is mitigated, and the millimetre-wave electric field becomes more evenly distributed (i.e. reducing the peak of $\left|\overrightarrow{E(x,y)}\right|$ in the region of $y>-t$). The increased $\left|\overrightarrow{E(x,y)}\right|$ in the region of $y<-t$ doesn't contribute much to the PCB dielectric loss because the dissipation factor of 5880 is 0.0012 at 60GHz, which gives

$\frac{\varepsilon_r' tan\delta\ (PCB\ substrate)}{\varepsilon_r' tan\delta\ (LC)} = \frac{2.155\times 0.0012}{2.5\times 0.0123} = 0.084 = \frac{1}{11}$, i.e. LC dielectric loss density is 11 times larger than that of the PCB substrate. The simulated infinitesimally small dielectric loss density in the PCB substrate region has confirmed this.

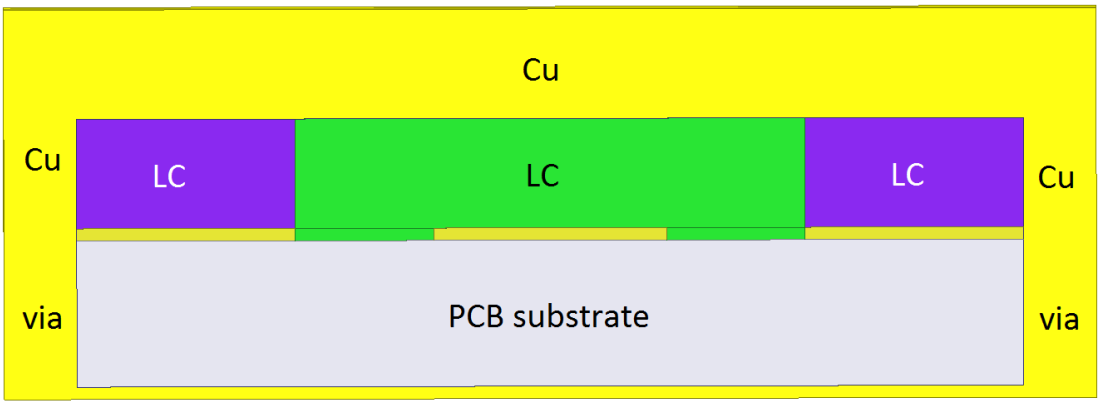


Fig.118 A Proposed Conductor-Backed ECPW (CB-ECPW) for Future Study

The chief limitation of the improvement lies in the reduced wave-occupied volume ratio (*WoVR)* in LC, due to which the line length should be increased to compensate for a same phase shift. Note that the LC volume increases linearly with the line length, hence the integration of reduced $\left|\overrightarrow{E(x,y,z)}\right|^2$ over the increased volume provides a limited level of loss mitigation.

7.6 Other Research Possibilities for Optimisation

7.6.1 LC with Lower Product of Dielectric Constant and Dissipation Factor

With the amplitude change of the low-frequency biasing voltage, the maximum difference in the dielectric loss occurs between the two extreme states (⊥ at 0V bias, and || at saturation bias) as derived in section 3.4.3. Assuming an unchanged 60GHz field distribution, the loss ratio of the two states will be $\frac{\varepsilon_r' tan\delta\ (\perp states)}{\varepsilon_r' tan\delta\ (||\ states)} = \frac{2.5\times\ 0.0123}{3.3\times\ 0.0032} = 2.9119$. This confirms that loss management should be focused on the 0V-biased state when LC's intrinsic absorption is at maximum.

One direct way of decreasing LC dielectric loss is changing the dielectric materials to those of lower product of $\varepsilon_r' tan\delta$ (at ⊥ state), such as the TUD series shown in Table 16 below.

Table.16 Dielectric and Tuning Properties of LC Material Candidates for Millimetre-wave

LC Candidates	Orientation	ε_r'	$tan\delta$	$\varepsilon_r' tan\delta$	Tunability	$\frac{Tunability}{\varepsilon_r' tan\delta\ (\perp \text{state})}$
GT3-24002 (This Work)	||	3.3	0.0032	0.01056	32%	10.41
	⊥	2.5	0.0123	0.03075		
TUD-670	||	3.06	0.0037	0.01132	26.4%	10.49
	⊥	2.42	0.0104	0.02516		
TUD-566	||	3.11	0.0021	0.00653	34%	22.21
	⊥	2.32	0.0066	0.01531		
TUD-899	||	3.41	0.0025	0.00852	39%	22.98
	⊥	2.46	0.0069	0.01697		

From the material's figure-of-merit (here defined as the ratio of tunability to $\varepsilon_r' tan\delta$ at the ⊥ state), we can derive that the deployment of TUD-566 or TUD-899 in place of the current GT3-24002 is very likely to reduce dielectric loss appreciably and ultimately allows our ECPW's insertion loss comparable with the state-of-the-art LC-based waveguide phase shifters such as [48] and [68].

7.6.2 Enclosed CPW (ECPW) with Artificial Magnetic Conductor (AMC)

To enable controlled excitation and propagation of unimodal electromagnetic waves up to 67GHz, the proposed enclosed CPW (ECPW) is based on full metallic ground planes and restricted sidewalls spacing (cavity width) less than half a guided wavelength to suppress stray modes. However, we have discussed in section 7.4.1 the scalability of the structure for a higher frequency will be highly limited by the cavity width's manufacturability, LC's filling capability, and the insertion loss's sensitivity to the fabrication tolerance.

To relieve the tight tolerance of the cavity width for a higher frequency operation, an uncharted direction for future research is introducing the concept of artificial magnetic conductor (AMC) to the ECPW's ground structure. As illustrated in Fig.119 below, AMC in the form of longitudinally corrugated hard surface exhibits high-impedance to orthogonal higher-order modes' propagation (e.g. the undesired parallel plate mode). By this method, only the ECPW mode is guided locally in the LC-filled cavity.

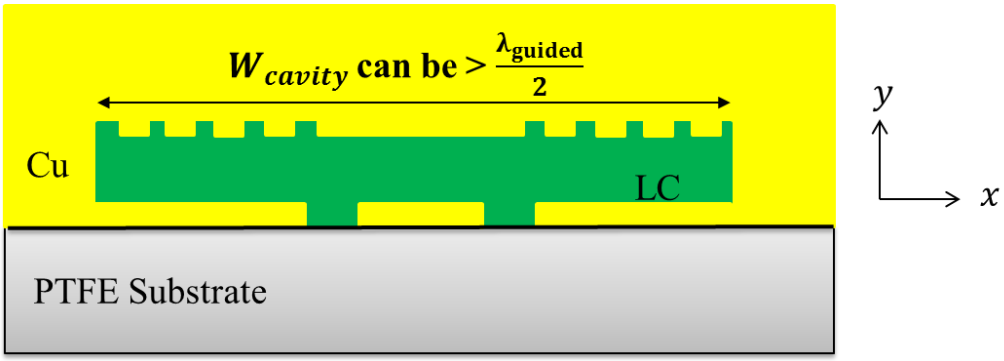


Fig.119 ECPW with Longitudinal Corrugations on Enclosure to Suppress Higher-order Modes whilst Reliving Tight Tolerance on Cavity Dimension

7.6.3 LC-based ECPW Phased Shifters Integration for 60GHz Beam Steering

The developed LC-based ECPW phase shifters can be scoped to integrate on a phased array antenna as a non-mechanical millimetre-wave beam steerer featuring lightweight and a smaller footprint.

To do this accurately and efficiently, 60GHz beams can be steered electronically by sequentially shifting the phase of each radiating components (realised by tuning the proposed LC-based ECPW phase shifters) to produce constructive or destructive interference for shaping the desired radiation pattern. For instance, tilting the main lobe of a 1D array antenna consisting of equally-spaced elements can be realised by controlling the bias voltages to each pixel, with each pixel excited by a LC-based ECPW phase shifter developed by us, as sketched in Fig.120 below.

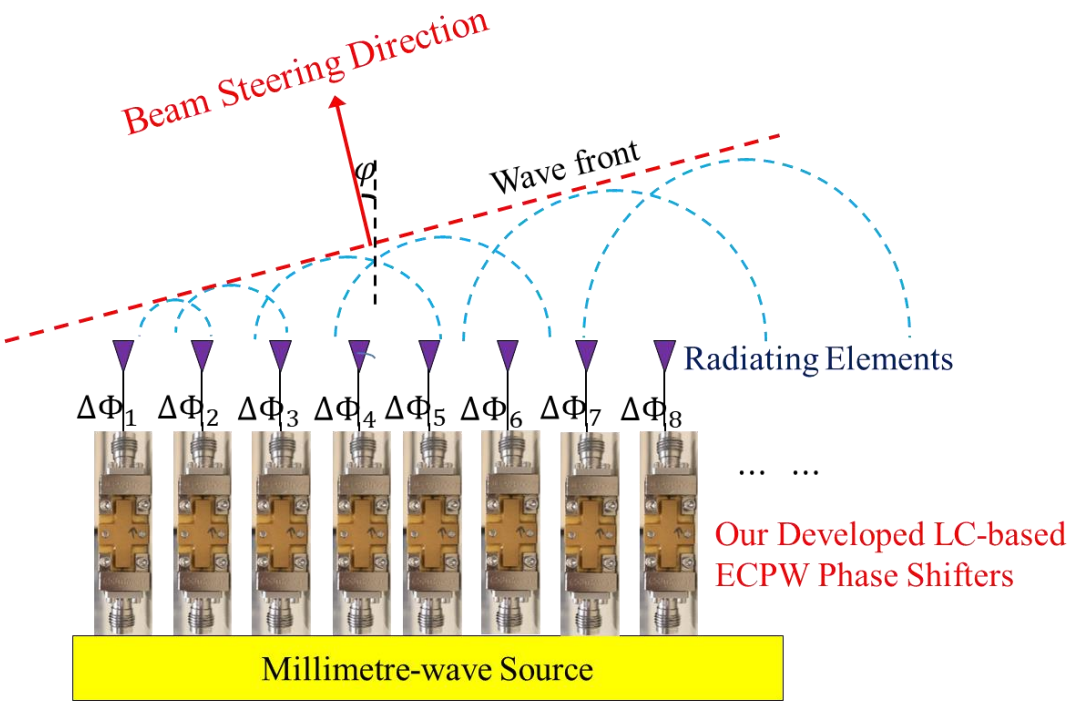


Fig.120 Smart Beam Steering Networks Incorporating our LC-based ECPW Phase Shifters

The beam steering system incorporating our phase shifters exhibits three chief advantages, i.e. the 0-2π continuous phase shift (due to LC tuning mechanism) for unlimited beam steering resolution, the true-time-delay nature (group delay independence on frequency) for beam squinting-free, and the linear phase shift-voltage response without the need for bulky compensation networks. With emitters fed by the proposed high-performance phase shifters, a linearly increasing phase progression profile could be produced, allowing individual wave fronts to propagate diverse distances at a given time. The cumulative wave front is thereby tilted by a pivot angle, and thus all the elements radiate coherently along a desired direction. The radiation pattern will be the product of two factors, i.e. the element factor as a function of radiator's physical realisation, and the array factor as a function of the array geometry and the element excitations.

In addition to the phase shifting hardware solution we have developed in this work, a modern phased array beam-steering system also calls for a combination of advanced beam-forming algorithms and control techniques. The requirement for massively high data rates for back end real-time digital signal processing challenges the design of real time beam-formers and correlators. Future work could therefore center around the development and optimisation of adaptive beam-forming and the control network. It remains to be seen how computational electromagnetic simulation suites could be combined with millimetre-wave network system models to optimise the whole array system, including radiating elements, our developed LC-based ECPW phase shifters, receiver electronics, as well as signal processing.

Chapter 8. Conclusion and Outlook

This thesis reports on the development and characterisation of liquid crystal based low-loss phase shifters for millimetre-wave applications. Theory, simulations and measurements are supported by careful comparisons and benchmarking. Functionalities and manufacturability are demonstrated. The proposed structure and optimisation of LC-based FE-free-CPW and ECPW adds significantly to existing research on millimetre-wave phase shifting components operating above 60GHz.

8.1 Concluding Remarks of the Device

8.1.1 Performance Advantages

We have developed a new LC-based Enclosed CPW (ECPW) phase shifter structure with demonstrated advantages outlined below as compared with competing technologies.

[1] The proposed ECPW structure drastically improves signal-to-noise ratio whilst removing the need for bond wires or vias for the grounding paths' potential equalization, which reduces insertion loss significantly and enables a wideband single-mode low-loss operation across 54GHz-67GHz.

[2] Precise 0-π continuous phase delay with unlimited beam-steering resolution.

[3] True-time-delay property (group delay expressed in delay length is independent of frequency), which is free of the beam squinting (steering angle dependent on frequency) and free of distortions in spatial and temporal resolutions.

[4] Linear phase shifting vs. voltage response, which removes the need for compensation networks widely used in a conventional phased array system, and hence reduces the total component losses.

[5] Ease of control with 0-10V low power consumptions (≈0.1V/μm).

[6] Low insertion loss variation for the full range of phase shift over the required frequency band, which minimises beam distortion while steering.

[7] Balance between phase-tuning range and insertion loss, i.e. high figure-of-merit.

[8] Planar solution, miniature (19.7mm×12.7mm×3.6mm), and robust (moving-parts free).

[9] Fabricated inexpensively and fast prototyping at scale.

[10] Scalability to higher frequency (70GHz – 90GHz) for more interesting applications.

8.1.2 Limitations of the Device Research

8.1.2.1 Conflicts between Response Time, Linearity, and Insertion Loss

Transient performance of the LC-based ECPW phase shifter is assessed by measuring the response time under various voltages bias, with the results ranging from 4 seconds (rise time with 10V bias applied) to 12 seconds (fall time once removal of 10V bias), with minor dependence on the millimetre-wave spectrum (identical switching speed for 54GHz and 67GHz signal), as the LC orientation is attributed to the low-frequency electric field only.

Note that the rise time (response time for switching on) depends on the biasing field applied, whereas this is not the case for the fall time (response time for switching-off). The worst agility occurs at post-removal of the bias, with the response time limited chiefly by the quadratic dependence on the LC thickness due to the effective anchoring range of the rubbed alignment layer, relying on which the LC elastically reorients to the initial 0V bias state (10 to 12 seconds to reorient and stabilise for our 140μm-thick LC layer in ECPW structure).

In view of the quadratic dependence the response time on the LC thickness, we do not intend to reduce the LC thickness at this stage for a faster response but at a cost of degrading the desirable linearity of 0-π shift vs. 4-10V bias, as well as increasing the material absorption and hence insertion loss due to elevated electric field intensity. Albeit struggling to meet the fast response requirement by the future autonomous driving radar, our LC-based millimetre-wave phase shifters can still be deployed advantageously as a static beam steering solution for weather radars, radio telescope, and satellite relay links, where fast response is not a priority.

8.1.2.2 Dielectric Anisotropy and CTE Anisotropy of the Non-tunable Dielectric Substrate

The simulation-based design has yet to account for dielectric anisotropy of the PCB substrate, which can affect the prediction accuracy of the wave-occupied volume ratio (*WoVR*) of the tunable LC to the non-tunable substrate, the effective dielectric constant, the phase constant, and ultimately, the differential phase shift, and insertion losses.

Anisotropic CTE of PTFE-based dielectric substrate (5880) and the mismatch with Cu is taken care of in device-making. However, there is still room to optimise by updating the mechanical

assembly design of diverse parts. Further minimisation of the dimensional instability (substrate bending and non-uniform LC layer as a result) can be implemented by using a thicker dielectric substrate or adding a common metal plate at the bottom linking all the screws, hence equalising the stress imposed by connectors pressing on to the substrate. Another way that can be attempted is using PCB with double sided Cu clads and strategically etching pattern on the unused side (to create another stress relief in an opposite direction that compensates the bending of the side under consideration).

8.1.2.3 Inaccurate Measurements during Fabrication

As pointed out in section 6.1.3, the roughness of steep sidewall is filtered out in the surface profile measurement using Dektak, due to the geometry of the stylus. Replacing the current stylus with specialized super sharp ones terminating in a finer radius tip can improve the resolution for characterizing high aspect ratio features. As specified in section 6.2.2 the polyimide rubbing process, it remains to be seen how to set up the best pile contact position of the roller for optimised LC pre-alignment.

8.2 Knowledge Contributions

Firstly, this work contributes a new transmission line structure enclosing tunable dielectrics, i.e. enclosed coplanar waveguide (ECPW) including an enclosed ground conductor (enclosure) in the design, which significantly reduces the instability due to the floating effect of the transmission line. The structure not only retains the true-TEM advantage of the FE-free CPW we initially designed (Chapter 2.5), but also achieves high tuning range based on modulating a planar LC layer on top of the CPW's core line in addition to the two CPW slots (channels). More fundamentally, the continuous sidewalls of the enclosure's cavity serve as a unified grounding path, which fully addresses the stray modes and energy leakage problems posed by conventional CPW with floating electrodes (FE-CPW as analysed in section 2.4.3).

On this basis (i.e. stray-mode free ECPW boundary condition), this work optimises the tunable transmission line portion by competing spatial volume distribution of the millimetre-wave signal occupying lossy tunable dielectrics (i.e. LC) versus low-loss but non-tunable dielectrics (i.e. PTFE), and minimising the total of dielectric volumetric loss and metal surface loss for a fixed phase-tuning range under controlled impedance. For a fixed geometry, phase-tuning range and insertion loss both increase with dielectric constant ratio of LC to PCB substrate. However, such an increase is nonlinear in the case of controlled impedance (e.g. 50Ω) due to geometrical variation effects on the wave-occupied-volume ratio. Phase shift to loss optimisation is thereby performed in recognition of this nonlinearity.

Thirdly, 1.85mm connectors are accounted in the simulation for the whole-device impedance-matching. This is an important part for low-reflection signal transmission. The work itself is challenging because of the irregular nature of the connection region. Time domain reflectometry (TDR) method is employed to accurately characterise the transient impedance of the coaxial-CPW-ECPW interfaces. The PCB's edge patterns at these interfaces are sized accordingly to tailor the polarisation transition in different planes smoothly. The minimised diametrical discontinuities and tight transverse couplings are verified to minimise reflection and higher-order modes radiation.

Fourthly, to reduce conductor loss for the frequency of interest, the device manufacturing process employs gold-plating of optimal thickness on ground enclosure as well as PCB with unconventional rolled annealed copper foil of lowest surface roughness. Given the gold-plated thickness is comparable to the penetrating depth of gold at 60GHz, meshing inside metals is performed to accurately represent the field's decaying behaviour without overestimating the conductor loss. We have experimentally verified the impact of metal profile on 60GHz device performance concerning insertion loss, dispersion and phase constant, etc. Proceeding one step further, we numerically model loss optimisation by contouring conductor profile to tailor the electric field distribution. The substrates processing and device assembling process is optimised, which opens the door for rapid device-prototyping.

Due to a convergence of these, the optimal LC-based enclosed CPW (ECPW) phase shifter targeted for the frequency range of 54GHz-67GHz presents a tangible improvement in the phase shift effectiveness and signal-to-noise ratio, as well as lower insertion and return losses, more ease of control and lower-cost fabrication as compared with up-to-date documentation.

8.3 Potential Applications and Social Impacts

The developed low-loss liquid crystal based 54GHz-67GHz phase shifter with 0-10V continuous tuning and true-time-delay properties will be deployed advantageously in millimetre-wave beam-steering phased array sub-systems for use in a broad range of applications, including but not limited to the followings.

[1] Responding to the ever-evolving needs of the next generation of wireless communications, providing bandwidth so severely needed for improved data throughput and video performance in 5G wireless communication systems, e.g. 60GHz communication backhaul (a global unlicensed band between 57GHz and 64GHz).

[2] Aerospace applications such as communications as an Inter-Satellite Link, with the proposed LC-based ECPW phase shifters feeding phased array antennas aboard geostationary (GEO) or low-earth-orbiting (LEO) satellites. Table 17 below outlines the steering angles and slew rates typically required for a phased array beam steerer.

Table.17 Angular Tracking Requirement by Inter-satellite Communications [4]

	Angular Tracking Velocity	
LEO Tracking GEO	180°/45minutes	4°/minute
GEO Tracking LEO	22°/45minutes	0.5°/minute

Benchmarking these specifications (modest angles and slew rates requirement especially for GEO tracking LEO) with our device's response time (12 seconds for the worst case of LC reorientation post-removal of voltage bias), the proposed LC-based ECPW phase shifters are sufficiently fast and low-loss to meet the tracking requirement by the communication partners.

[3] Gesture recognition and potentially shaping the future of radar-based autonomous driving. The proposed LC-based ECPW phase shifters feeding phased array radar will possess continuously tuning capability, moving-parts-free, compact size and cost-competitive hardware solution for use as gesture sensing radar or vehicular radar operating in 54GHz-67GHz.

Selected Publications during PhD

A selection of methodologies, techniques and results reported on the thesis are linked with the following research articles published (and in preparation for published) during my PhD.

[1] **J. Li**, H. Xu and D. Chu, "Design of liquid crystal based coplanar waveguide tunable phase shifter with no floating electrodes for 60–90 GHz applications," Proceedings of 2016 46th European Microwave Conference (EuMC), London, United Kingdom, 2016, pp. 1047-1050. DOI: 10.1109/EuMC.2016.7824526

Available at: https://ieeexplore.ieee.org/document/7824526/

[2] L. Cai, H. Xu, **J. Li** and D. Chu, "High Fig-of-merit compact phase shifters based on liquid crystal material for 1–10 GHz applications," Japanese Journal of Applied Physics, vol. 56, no. 1, Jan. 2017. DOI: 10.7567/JJAP.56.011701

Available at: http://iopscience.iop.org/article/10.7567/JJAP.56.011701/meta

[3] L. Cai, H. Xu, **J. Li** and D. Chu, "High FoM liquid crystal based microstrip phase shifter for phased array antennas," Proceedings of 2016 International Symposium on Antennas and Propagation (ISAP), Okinawa, 2016, pp. 402-403

Available at: http://ieeexplore.ieee.org/document/7821401/

[4] Ö. Yöntem, **J. Li**, and D. Chu, "Imaging through a projection screen using bi-stable switchable diffusive photon sieves," Optics Express, Vol. 26, Issue 8, pp. 10162-10170 (2018). DOI: 10.1364/OE.26.010162

Available at: https://www.osapublishing.org/oe/abstract.cfm?uri=oe-26-8-10162

[5] **J. Li** and D. Chu, "A liquid crystal based enclosed coplanar waveguide (ECPW) phase shifter for 54-67GHz applications", submitting to IEEE Transactions on Microwave Theory and Techniques

[6] **J. Li**, and D. Chu, "Tuning range and insertion loss optimisation of a liquid crystal based enclosed coplanar waveguide structure by competing millimetre-wave-occupied volume ratio in

tunable vs. non-tunable dielectrics," In preparation for publication in Molecular Crystals and Liquid Crystals

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Appendices

Appendix A: Measured Material Properties and Loss Analysis

Loss Decomposition Analysis for Optimal PCBs with Diverse Dielectric Constants

Table.18 Product of Dielectric Constant and Dissipation Factor: 5880 vs. 3003

54-66GHz	ε_r'	$tan\delta$	$\varepsilon_r' tan\delta$ *(RO3003)/* $\varepsilon_r' tan\delta$ *(RT5880)*
RT5880	2.195	0.0012	
RO3003	2.993	0.001	1.136

Table.19 Measured Temperature Coefficient of Dielectric Constant (TCDk) for 5880 vs. 3003

	5880 (measured condition: -50 to 150°C)	3003 (measured condition: -50 to 150°C)
Temperature coefficient of Dielectric Constant (TCDk)	-125 ppm/°C (-2.5% at 200°C)	-3 ppm/°C (-0.06% at 200°C)

Table.20 Tunable Part Loss Analysis for 50Ω ECPW (Optimised for Each PCB Dielectric Constant)

(a)

60GHz, 0V bias	ε_r	$\frac{W_{strip}}{T_{LC}}$	$\frac{W_{gap}}{T_{LC}}$	T_{LC} (μm), W_{gap} (μm) and W_{strip}(μm) for max. S_{21} with π shift			Length L for π Shift (mm)	LC volume (mm^3)	Core surface area (mm^2)	$\left\|\overrightarrow{E_s(x,z)_0}\right\|_{max}$ (V/mm)
Air	1.0006	2.467	1.27	T_{LC} =160	W_{gap}=203	W_{strip}=395	12.7	2.729	10.46	140.5
RT5880	2.195	2.094	1.45	T_{LC} =140	W_{gap}=203	W_{strip}=293	14.32	2.705	8.88	174.5
RO3003	2.993	2.061	1.6	T_{LC} =100	W_{gap}=160	W_{strip}=206	15.2	2.058	6.78	298.3

(b)

60GHz, 0V bias	ε_{eff} (0V bias)	ε_{eff} (max. bias)	Min. λ_g (mm)	S_{21} (dB)	S_{11} (dB)	Transmitted (%)	Reflection loss (%)	LC loss (%)	Conductor loss (%)	PCB substrate loss (%)	Higher-order modes loss (%)
Air	2.067	2.673	3.056	-1.398	-44.59	72.47	0.0035	21.82	4.62	0	1.08
RT5880	2.408	2.972	2.898	-1.504	-39.79	70.73	0.0105	21.31	5.99	0.61	1.34
RO3003	2.658	3.215	2.787	-1.587	-41.25	69.39	0.0075	20.89	8.67	0.72	0.31

Appendix B: CAD for PCB Fabrication

CAD File of 70μm-thick Cu Design for FE-free-CPW Proposed in Chapter 2.5

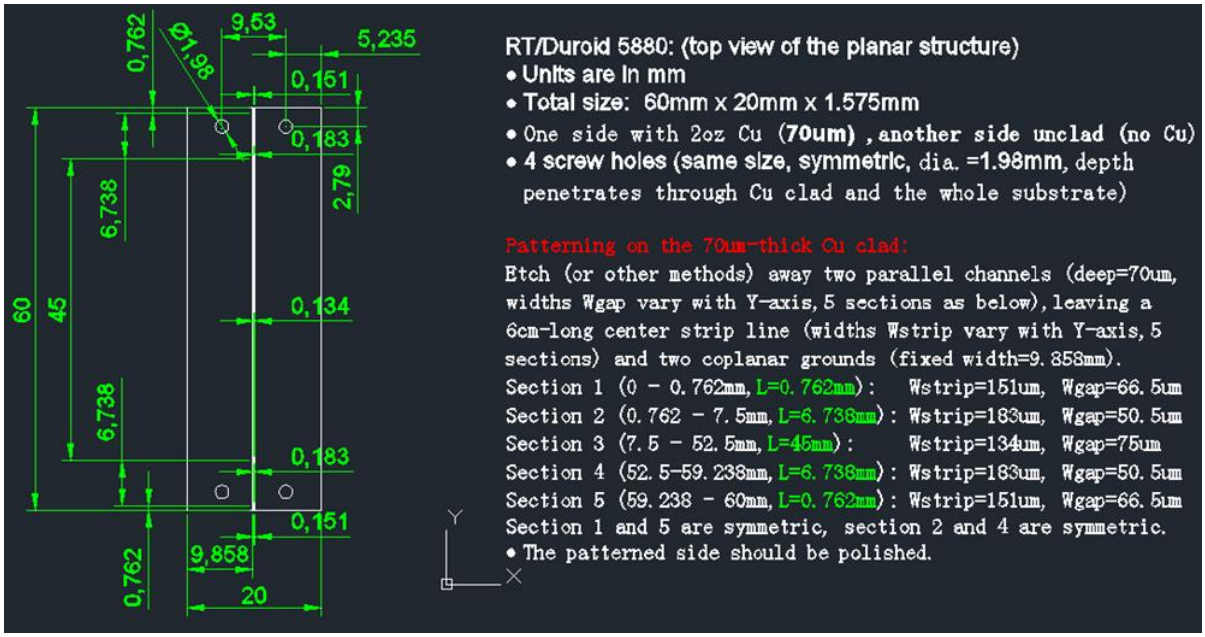

Fig.122 Top Plan View of the 2oz-Cu PCB Design with Size Annotation

PCB Panel Design Details for the Proposed ECPW Structure

Substrate material: 1.575mm-thick RT/duroid 5880 panel, with 0.5oz rolled Cu on one side (to be patterned and gold-plated), another side no Cu clad (removed by etching).

RT/duroid 5880 panel size: 230mm×173mm×1.575mm, reserving 6.35mm between each individual design. Within one panel, engrave 9 designs as specified below. The size of each design piece is identical in width (12.7mm), but differs in lengths and also the patterns. For each piece, there are 6×M2 screwing holes.

Table.21 Summary of Multiple Designs Engraved within a RT/duroid 5880 Panel

	PCB Size (mm)	Simulated (60GHz)		Verification Purpose	LC Thickness T_{LC} (μm)
		Shift	S_{21} (0V to max. bias)		
Design 1	18.284×12.7	181.1°	-1.76dB to -1.03dB	π shift optimal loss (TDR)	140 (targeted)
Design 2	19.716×12.7	197.3°	-1.97dB to -1.14dB	+10% shift reserved	
Design 3	32.604×12.7	360.4°	-3.16dB to -1.80dB	2π shift optimal loss (TDR)	
Design 4	35.468×12.7	397.2°	-3.43dB to -1.93dB	+10% shift reserved	
Design 5	18.284×12.7	180.2°	-2.36dB to -1.43dB	π optimal (Frequency domain)	
Design 6	18.284×12.7	181.1°	-1.77dB to -1.06dB	Tolerate for LC cavity +10μm	150
Design 7	18.284×12.7	181.3°	-1.78dB to -1.05dB	Tolerate for LC cavity +20μm	160
Design 8	18.284×12.7	181.1°	-1.77dB to -1.05dB	Tolerate for LC cavity -10μm	130
Design 9	18.284×12.7	180.6°	-1.79dB to -1.08dB	Tolerate for LC cavity -20μm	120

Appendix C: Theoretical Modelling

Theoretical Model Derivation for the Proposed LC-based ECPW in Section 3.4.1

According to the phasor form of Maxwell equations, wave equations and the constitutive relations, we have

$$\nabla \times \overrightarrow{E_s} = -jw\mu\overrightarrow{H_s}, \qquad \nabla \times \nabla \times \overrightarrow{E_s} = -jw\mu\left(\nabla \times \overrightarrow{H_s}\right), \qquad \nabla \times \overrightarrow{H_s} = (\sigma + jw\varepsilon)\overrightarrow{E_s}$$

$$\because \nabla \times \left(\nabla \times \vec{A}\right) = \nabla\left(\nabla \cdot \vec{A}\right) - \nabla^2\vec{A},$$

$$\therefore \nabla \times \nabla \times \overrightarrow{E_s} = \nabla\left(\nabla \cdot \overrightarrow{E_s}\right) - \nabla^2\overrightarrow{E_s} = -jw\mu(\sigma + jw\varepsilon)\overrightarrow{E_s}$$

$$\Rightarrow \begin{cases} \nabla^2\overrightarrow{E_s} - \gamma^2\overrightarrow{E_s} = 0 \\ \nabla^2\overrightarrow{H_s} - \gamma^2\overrightarrow{H_s} = 0 \end{cases}$$

$$\begin{cases} \vec{E} = -jw\mu\nabla \times \overrightarrow{\Psi_h} \\ \vec{H} = k^2\overrightarrow{\Psi_h} + \nabla(\nabla \cdot \overrightarrow{\Psi_h}) \end{cases} \qquad \begin{cases} \vec{E} = k^2\overrightarrow{\Psi_e} + \nabla(\nabla \cdot \overrightarrow{\Psi_e}) \\ \vec{H} = jw\varepsilon\nabla \times \overrightarrow{\Psi_e} \end{cases}$$

$$\overrightarrow{\Psi_h} = \overrightarrow{\Psi_{h_t}} + \overrightarrow{\Psi_{h_z}} = \overrightarrow{\Psi_{h_t}}(x,y)e^{\pm\gamma_n z} + \overrightarrow{a_z}\Psi_h(x,y)e^{\pm\gamma_n z}$$

$$\overrightarrow{\Psi_e} = \overrightarrow{\Psi_{e_t}} + \overrightarrow{\Psi_{e_z}} = \overrightarrow{\Psi_{e_t}}(x,y)e^{\pm\gamma_e z} + \overrightarrow{a_z}\Psi_e(x,y)e^{\pm\gamma_e z}$$

$$\begin{cases} {\nabla_t}^2\overrightarrow{\Psi_h}(x,y) + (k^2 + {\gamma_h}^2)\Psi_h(x,y) = 0 \\ {\nabla_t}^2\overrightarrow{\Psi_e}(x,y) + (k^2 + {\gamma_e}^2)\Psi_e(x,y) = 0 \end{cases}$$

$$\text{For medium i} \Longrightarrow {\nabla_t}^2\psi_i^p(x,y) - (\beta^2 - {k_i}^2)\psi_i^p(x,y) = 0,$$

$$where\ P = e, h$$

$${\nabla_t}^2 = \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2}$$

Boundary conditions: $E_t\ is\ continuous,$

for PCB − air interface: $-a \le x \le a,\ y = T_{air}$

$$\begin{cases} E_{x_3}(x, y = T_{air}) = E_{x_2}(x, y = T_{air}) \\ E_{z_3}(x, y = T_{air}) = E_{z_2}(x, y = T_{air}) \\ H_{x_3}(x, y = T_{air}) = H_{x_2}(x, y = T_{air}) \\ H_{z_3}(x, y = T_{air}) = H_{z_2}(x, y = T_{air}) \end{cases}$$

for PCB − LC interface: −a ≤ x ≤ a, $y = T_{air} + T_{PCB}$

$$\begin{cases} H_{x_2}(x, T_{air} + T_{PCB}) - H_{x_1}(x, T_{air} + T_{PCB}) = J_z(x) \\ H_{z_2}(x, T_{air} + T_{PCB}) - H_{z_1}(x, T_{air} + T_{PCB}) = -J_z(x) \\ E_{x_2}(x, T_{air} + T_{PCB}) = E_{x_1}(x, T_{air} + T_{PCB}) = E_x(x) \\ E_{z_2}(x, T_{air} + T_{PCB}) = E_{z_1}(x, T_{air} + T_{PCB}) = E_z(x) \end{cases}$$

$$E_x(x), E_z(x) \begin{cases} \neq 0 & in\ two\ LC\ slots, \\ = 0 & elsewhere \end{cases}$$

LC − top plate interface: $y = T_{air} + T_{PCB} + T_{LC}$

$$E_{x_1}(x, y = \cdots) = E_{z_1}(x, y) = 0$$

sidewalls: $x = \pm a, E_{z_1}(x, y) = 0$