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High LO-RF isolation of zero-IF mixer in 0.18 μm CMOS technology*

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Abstract In this study, we introduce a zero-IF sub-harmonic mixer with high isolation in the 5 GHz band using 0.18 μm CMOS technology. Placing an LC-Tank between the class AB stage and the mixer core improves the isolation between the LO to RF at low supply voltage. The measured isolation is 48 dB between the LO and RF ports, and the 9.5 dB conversion gain is achieved with a supply voltage of 7 mA at 2.5 V. In order to alleviate the degradation of linearity due to the high conversion gain, we adopt the class AB stage as RF input stage. The measured IIP_3 is −7.5 dBm.

Keywords Double-balance · LO-RF isolation · Low voltage · Sub-harmonic mixer · Zero-IF receiver

1. Introduction

Growing markets in the wireless communication enable variable aspect of researches, especially for application in the 5–6 GHz ISM band [1, 2]. The highly integrated Direct Conversion Receiver (DCR) is replacing the conventional Super Heterodyne Receiver (SHR). Although the DCR looks promising for low power system-on-a-chip applications, problems such as dc offset, 1/*f* noise, and isolation seriously impede the implementation of DCR into circuit architecture. Of particular concern is the degradation of 'signal to noise ratio' (SNR) performance from LO leakage, resulting from the self-mixing of the local oscillator (LO) with the RF port [3].

The sub-harmonic mixer alleviates the self-mixing problem by separating the fundamental LO and RF frequencies as described in recent research [3–5]. These reported architectures, however, adopt a cascoded configuration and the corresponding circuits must be operated at a high supply voltage. Indeed, the topic of self-mixing is paramount in DCR design when using CMOS technology. In DCR architecture, the RF frequency is identical to the LO frequency and the LO power is generally greater than 0 dBm. Inevitably, some of the LO power leaks into the lossy silicon substrate. The leakage from the RF port mixes with the LO signal, generating a dc offset at the IF band. Thus, it is important to maintain good LO-RF isolation to suppress the LO leakage into the RF port.

In order to achieve both high LO-RF isolation and low voltage operation, the proposed sub-harmonic mixer uses a folded current-commutating architecture with an LC-Tank between the RF signal and the mixer core. In contrast to previous designs [3–5], this proposed architecture, using an LC-Tank, does not use cascoded switching-pairs at the RF stage. Hence, the design is capable of supporting low voltage operation. In additional to this advantage, the design also increases LO-RF isolation.

2. Circuit architecture

The circuit block of the double-balance sub-harmonic mixer includes the following components: a class AB input stage (for RF and LO), phase splitter, LC-Tank, Gilbert cell core, and differential amplifiers (Fig. 1). The single-ended class AB stage is initiated at both the LO and RF input ports for

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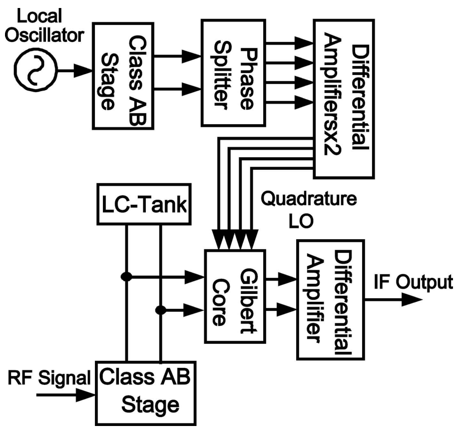


Fig. 1 Circuit block diagram of the proposed sub-harmonic mixer

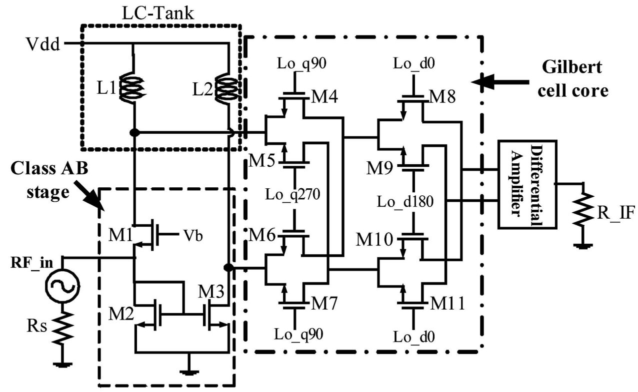


Fig. 2 Proposed sub-harmonic mixer schematic with folded current-commutating architecture and LC-Tank

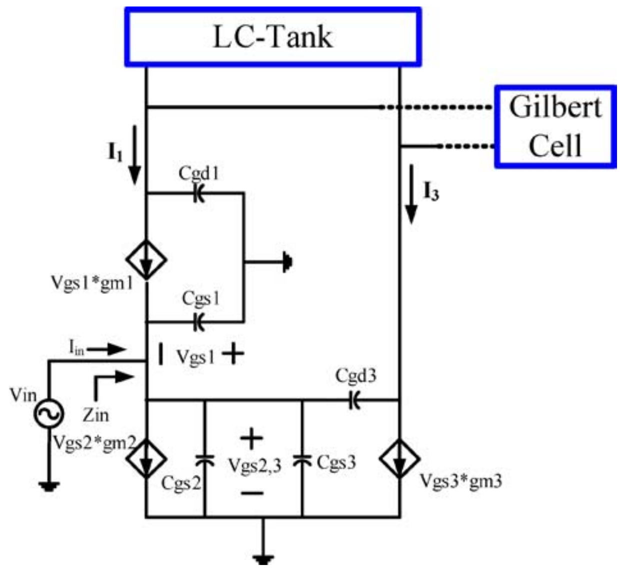


Fig. 3 Small-signal circuit of class AB stage

on-wafer measurement. The translated differential mode current passes into the Gilbert cell core. The LC-Tank is designed to pass the signal into the Gilbert cell only at the RF frequency (i.e., 2*LO). Hence, this tank suppresses the other harmonics generated by the class AB stage of the RF port and by the LO leakage.

Furthermore, the single-ended signal of the local oscillator changes to a differential signal through the class AB stage. In order to drive the switching-pair of the sub-harmonic mixer, a LO signal with a quadrature phase is necessary. A phase splitter is used to generate this quadrature signal. Finally, a low-pass filter (not shown) is placed between the output of the Gilbert mixer core and the differential amplifier. Consequently, the filtered output signal of the sub-harmonic mixer is translated to a single-ended signal by the differential amplifier.

Some of these critical sub-circuits are described in detail below.

2.1. Single-to-differential (Class AB stage)

The characteristics of the class AB stage [6] facilitate a high-speed response and eliminate the requirement for common-mode rejection. The common-gate of the M1 transistor, as shown in Fig. 2, possesses an excellent frequency response, while the speed of the common-source M3 transistor is improved by adding a low impedance diode-connected M2 transistor at the input stage.

The input impedance is derived by using the small-signal analysis in the circuit. Figure 3 depicts the equivalent circuit of small-signal behavior in class AB stage, the input voltage and current express as $\mathrm{V}_{in} = -\mathrm{V}_{gs1} = \mathrm{V}_{gs2,3}$ and $I_{in} = -V^*_{gs1} g_{m1} + V^*_{gs2} g_{m2}$, respectively. Afterward the input impedance is given by

$$\mathrm{Z}_{in} = \frac{\mathrm{V}_{in}}{\mathrm{I}_{in}} = \frac{\mathrm{V}_{in}}{\mathrm{V}_{in}\,(\mathrm{g}_{m1} + \mathrm{g}_{m2})} = \frac{1}{\mathrm{g}_{m1} + \mathrm{g}_{m2}} \tag{1}$$

Hence, the input impedance in the RF port can easily be matched to 50 Ω over a wide bandwidth.

2.2. Generation of quadrature phase (Phase splitter)

The quadrature LO signals are generated using the RC poly-phase filter technique [7]. A schematic diagram of the one-stage RC poly-phase filter is shown in Fig. 4. This pole of the filter is designed according to the formula of: $\omega_p = 1/(RC) = \omega_{LO}\ (f_{LO} = 2.525\,\mathrm{GHz})$. The accuracy of the quadrature phase is shown to be frequency independent, as is illustrated by sweeping the LO frequencies from 1 GHz to 3.5 GH (Fig. 5).

2.3. Mixer core (folded current-commutating architecture with LC-tank)

The fundamental concept of the sub-harmonic mixer rests upon the frequency conversion of N^*f_{LO}, where the N

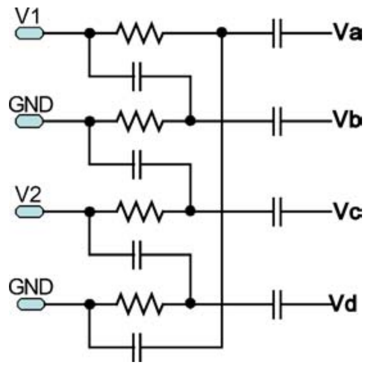


Fig. 4 Diagram of the RC phase splitter

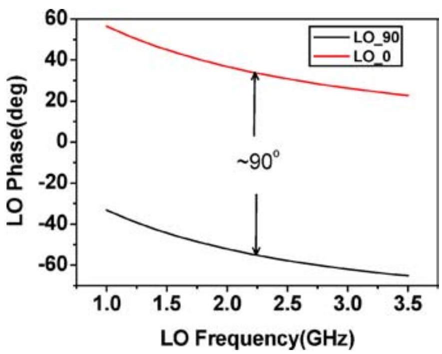


Fig. 5 Generated quadrature phase from the RC poly-phase filter

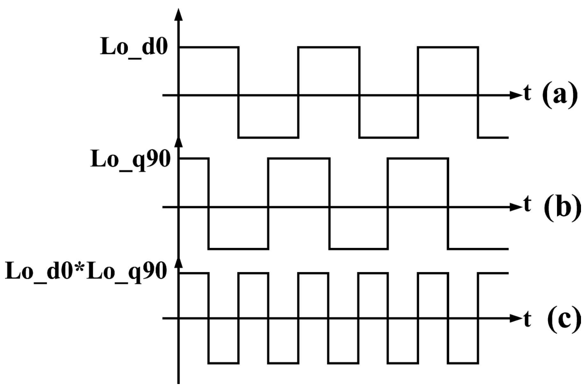


Fig. 6 LO waveforms for multiphase

different phase-shifted LO signals are required. The signals must be phase-shifted by 180°/N. Figure 6 shows the LO signal (Figs. 6(a) and (b)) and the effective LO signal (Fig. 6(c)). In this case, the RF input signal is multiplied by 2*LO (as in Fig. 6(c)).

In order to explain the frequency translation in the sub-harmonic mixer, we assume that local oscillator 1 and 2 operate in the free running frequencies as ω_{LO1} and ω_{LO2}, respectively. Hence, the mix of these two frequencies is given by

$$\cos(\omega_{LO1}t)\cdot\cos(\omega_{LO2}t+\theta) = \frac{1}{2}[\cos((\omega_{LO1}+\omega_{LO2})t+\theta) + \cos((\omega_{LO1}-\omega_{LO2})t-\theta)]. \quad (2)$$

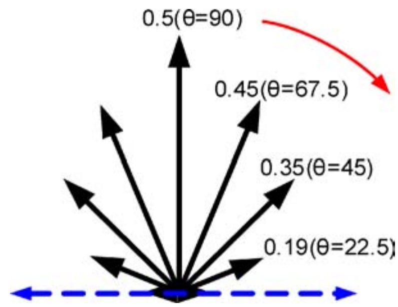


Fig. 7 Amplitudes variation with different phase angles

Setting identical values of ω_{LO1} and ω_{LO2} in sub-harmonic application, the resulted frequency response is expressed as $1/2\,[\cos(2\omega_{L01}+\theta)+\cos(\theta)]$. The magnitude variation with different phase angle θ is depicted in Fig. 7. Obviously, when the phase angle equals to 90° the resulted amplitude has the maximum value. Hence, the phase of LO waveform is orthogonal as descript in Fig. 6.

The sub-harmonic mixers reported in previous studies [3–5] consume more headroom than the conventional double-balance Gilbert mixer. In order to solve this issue, the mixer design proposed here (Fig. 2) is a folded current-commutating architecture with an LC-Tank (L1, L2, and parasitic capacitors). One advantage of this architecture is that the mixer consumes only two transistor voltage drops to maintain low voltage operation. Furthermore, the two parallel inductors in the LC-Tank connect with the common source terminals of transistors M4, M5, M6 and M7, which cancel the parasitic capacitors to prevent RF signal loss through the parasitic capacitor (i.e., C_{gs} and C_{sb}) in the M4-M7 transistors.

The design of LC-Tank is based on Fig. 8, the simulation of different inductances results in the variation of bandwidth. Sweeping the inductance from 2.5 nH to 1.7 nH, the corresponding bandwidth is decreased as shown in this graph. The widest bandwidth is obtained at the value of 2.5 nH inductance. Although the narrow band behavior is the inherent characteristic of LC-Tank, the reactive elements do not affect resulted bandwidth by the careful selection of inductance. The 3 dB bandwidth is 1.4 GHz in this design and capable of IEEE 802.11a application. The design parameters and corresponding performances of LC-Tank is listed in Table 1.

If the center frequency of the LC-Tank is designed to be the same as the RF frequency, the LO leakage will be attenuated. Consequently, LO-RF isolation is improved by the LC-Tank network. In addition, the dc offset voltage generated by the DCR architecture is also improved.

3. Experimental results and discussion

The sub-harmonic mixer proposed in this paper is fabricated by the TSMC 0.18 μm CMOS technology. Figure 9

Table 1 LC-Tank parameters and performances

$C_{gd1} + C_{db1} + C_{gd3} + C_{db3}$	Inductance	Parasitic resistance	Q-factor	f_o	$BW_{3\ dB}$
0.53 pF	2.5 nH	200 Ω	3.56	5.25 GHz	1.4 GHz

illustrates a die photo of the mixer with double-balance architecture. The implementation of single-ended RF, LO, and IF ports is used to feed on-wafer GSG measurement.

The maximum conversion gain, shown in Fig. 10, is approximately 9.5 dB during a LO power sweep from 0 to 10 dBm at the frequencies of 2.525 GHz and 5.1 GHz with LO and RF signals, respectively.

As mentioned above, the sensitivity of a DCR signal is degraded by dc offset. The dc offset cancellation due to self-mixing is expressed as:

$$\text{dc offset cancellation} = \frac{G_{RF}}{G_{LO} * V_{LO,leak}}, \tag{2}$$

where $V_{LO,leak}$ is the RF port leakage voltage generated by the LO signal, G_{RF} is the conversion gain of the mixer at the RF input frequency (5.1 GHz), and G_{LO} is the conversion gain of the mixer at the LO input frequency (2.525 GHz). Equation (2) suggests that the key to improving dc offset cancellation is a low $V_{LO,leak}$ value and high G_{RF}/G_{LO} ratio. Because the desired frequency conversion occurs at twice the

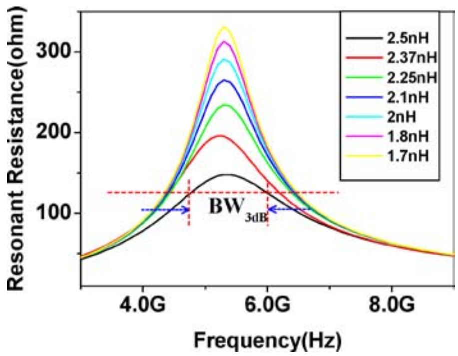


Fig. 8 Bandwidth variations with different inductances

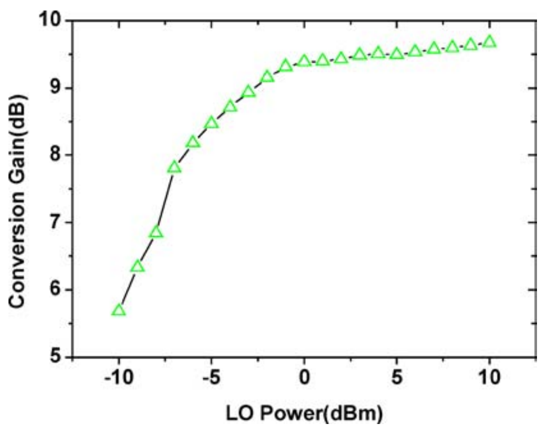


Fig. 10 Measured conversion gain

Fig. 9 Die photo of the proposed sub-harmonic mixer

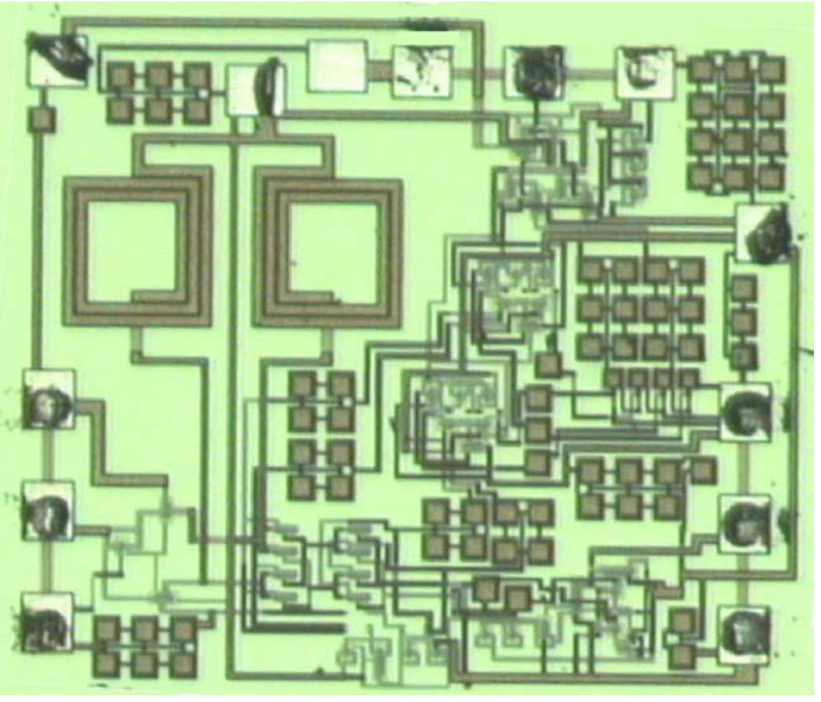
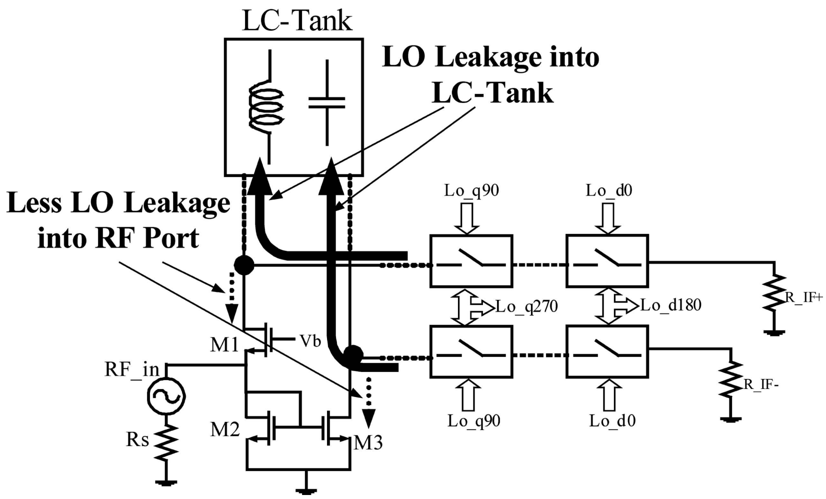


Fig. 11 Attenuation of LO leakage by LC-Tank



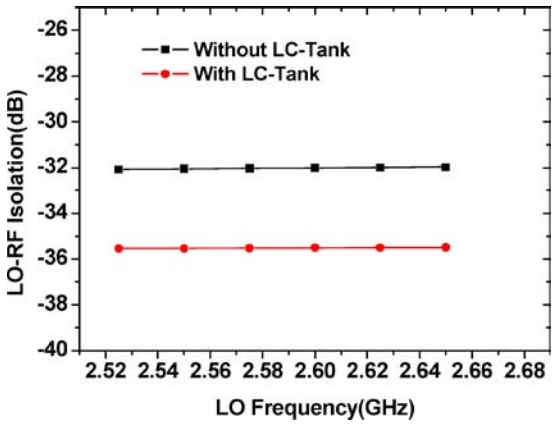


Fig. 12 Simulated LO-RF isolation with and without LC-Tank

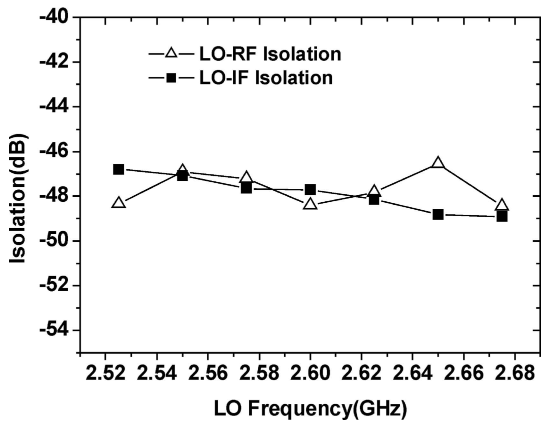


Fig. 13 Measured LO-RF and LO-IF isolation

LO frequency, a frequency of 2*LO has a higher conversion gain than the fundamental LO frequency.

Obviously, a high G_{RF}/G_{LO} ratio is a desirable characteristic for sub-harmonic mixers. In addition to having this characteristic, the proposed architecture uses an LC-Tank to prevent LO leakage ($V_{LO,leak}$) into the RF port. Because

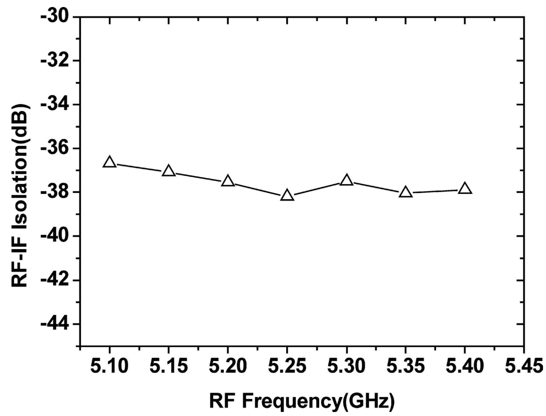


Fig. 14 Measured RF-IF isolation

the center frequency is in the RF range, the LO leakage is attenuated by the LC-Tank. This attenuation mechanism is depicted in Fig. 11. The bold arrows in this diagram represent LO leakage due to circuit mismatching and the lossy silicon substrate. The proposed LC-Tank can alleviate this LO leakage, indicated in the diagram by the dashed arrows.

Figure 12 shows the improvement in LO-RF isolation with the added LC-Tank. The simulated LO-RF isolation results in an improvement of 4 dB across the LO frequency spectrum. In Fig. 13, we see that the measured LO-RF isolation, with the LC-Tank, is 48 dB at 0 dBm LO power for LO and RF frequencies of 2.525 and 5.1 GHz, respectively. Because the down-converted output is 50 MHz, these high RF and LO frequencies, and their harmonics, are suppressed by the low pass filter. The improved LO-IF and RF-IF isolation values are shown in Figs. 13 and 14.

The mixer must also provide appropriate conversion gain across the whole RF front-end, to compensate for noise and IIP_3 in the DCR architecture. However, a larger conversion gain is generally a trade-off with linearity. The

Table 2 Performance comparison with reported literatures

	This work	[3]	[4]	[5]	[8]	[9]
Supply (V)	2.5	3	3.3	5	NA	3
Conversion gain (dB)	9.5	11.61	19	7.7	19	5.4
LO-RF isolation (dB)	48	NA	35	35	38	NA
IIP_3 (dBm)	− 7.5	− 13.5	− 3	− 6.1	− 12.5	− 2.3
RF Frequecy (GHz)	5.1	2	2	5.25	2.4	2.4
Process	CMOS 0.18 μm	CMOS 0.25 μm	Si/SiGe HBT	Si/SiGe HBT	CMOS 0.18 μm	CMOS 0.35 μm

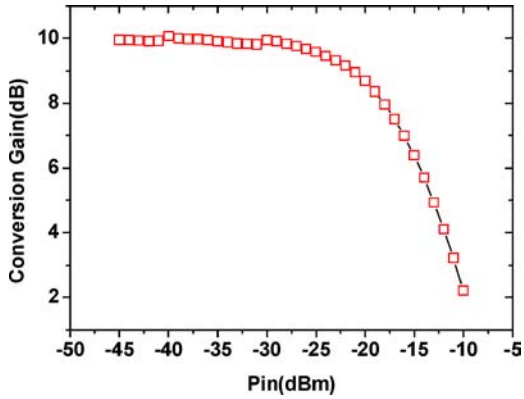


Fig. 15 One tone power measurement

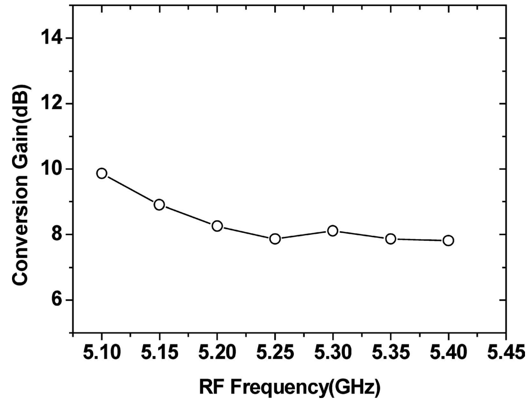


Fig. 17 Measured conversion gain as a function of RF frequency

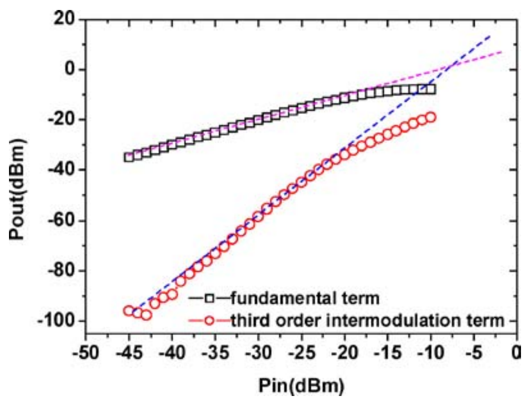


Fig. 16 Two tone inter-modulation power measurement

transconductor makes the principal contribution to nonlinearity in the mixer. Thanks to the advantages of the proposed Gilbert micromixer [6], the class AB amplifier of the RF input can alleviate the degradation of linearity. Figure 15 illustrates a one-tone power measurement. The results show an almost 10 dB conversion gain with $IP_{1dB} = -20$ dBm, at LO and RF frequencies of 2.525 and 5.1 GHz, respectively. A two-tone inter-modulation power measurement is shown in Fig. 16. The spacing of the two tones is 1 MHz, with $IIP_3 = -7.5$ dBm.

Figure 17 illustrates the measured conversion gain as a function of RF frequency at a constant IF frequency of 50 MHz. This result demonstrates the flat conversion gain over the operational bandwidth of the IEEE 802.11a standard. Finally, Table 2 compares the results presented here to results reported in the literature. The LO-RF isolation achieved here is superior to results achieved in other studies, with lower V_{dd} values related to the adoption of 0.18 μm CMOS technology.

4. Conclusion

A new proposed sub-harmonic mixer using folded current-commutating architecture with LC-Tank is shown to operate at low supply voltage, suppressing LO leakage, improving LO-RF isolation and improving the dc offset generated by LO leakage. The measured LO-RF isolation is 48 dB across LO and RF frequencies at 2.525 and 5.1 GHz, respectively. In addition, performance characteristics of the proposed mixer include a 9.5 dB conversion gain, -20 dBm of input, 1 dB compression point (IP_{1dB}) and -7.5 dBm of input intercept point at the 3rd order (IIP_3). The proposed architecture provides a valuable reference point for the design of a low dc offset DCR using low supply voltage.

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References

1. H. Samavati et al., "A 5 GHz CMOS wireless LAN receiver front end." *IEEE JSSC*, vol. 35, no. 5, pp. 765–772, 2000.
2. T.P. Liu et al., "5-GHz CMOS radio transceiver front-end chipset." *IEEE JSSC*, vol. 35, no. 12, pp. 1927–1933, 2000.
3. S.J. Fang et al., "A 2 GHz CMOS even harmonic mixer for direct conversion receivers." *IEEE ISCAS*, pp. 807–810, 2002.
4. L. Sheng et al., "A wide-bandwidth Si/SiGe HBT direct conversion sub-harmonic mixer/downconverter." *IEEE JSSC*, vol. 35, no. 9, pp. 1329–1337, 2000.
5. D.A. Johnson et al., "A packaged SiGe x2 sub-harmonic mixer for U-NII band applications." *IEEE BCTM*, pp. 159–162, 2001.
6. B. Gilbert, "The micromixer: A highly linear variant of the Gilbert mixer using a bisymmetric Class-AB input stage." *IEEE JSSC*, vol. 32, pp. 1412–1423, 1997.
7. J. Crols et al., "A single-chip 900 MHz CMOS receiver front-end with a high performance low-IF topology." *IEEE JSSC*, vol. 30, no. 12, pp. 1483–1492, 1995.
8. C.C. Meng et al., "A high isolation downconversion micromixer using 0.18-um deep N-well CMOS technology." *IEEE RFIC Sym.*, pp. 619–622, 8–10 June 2003.
9. J-Y. Choi and S-G Lee, "A low-noise, high-gain single-ended input double-balanced mixer." *Journal of Analog Integrated Circuits and Signal Processing*, vol. 36, no. 3, pp. 263–266, 2003, Springer Science.