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CMOS HYPERBOLIC SINE ELIN FILTERS FOR LOW/AUDIO FREQUNECY BIOMEDICAL APPLICATIONS

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Abstract

Hyperbolic-Sine (Sinh) filters form a subclass of Externally-Linear-Internally-Non-Linear (ELIN) systems. They can handle large-signals in a low power environment under half the capacitor area required by the more popular ELIN Log-domain filters. Their inherent class-AB nature stems from the odd property of the sinh function at the heart of their companding operation. Despite this early realisation, the Sinh filtering paradigm has not attracted the interest it deserves to date probably due to its mathematical and circuit-level complexity.

This Thesis presents an overview of the CMOS weak inversion Sinh filtering paradigm and explains how biomedical systems of low- to audio-frequency range could benefit from it. Its dual scope is to: consolidate the theory behind the synthesis and design of high order Sinh continuous–time filters and more importantly to confirm their micro-power consumption and 100+ dB of DR through measured results presented for the first time.

Novel high order Sinh topologies are designed by means of a systematic mathematical framework introduced. They employ a recently proposed CMOS Sinh integrator comprising only p-type devices in its translinear loops. The performance of the high order topologies is evaluated both solely and in comparison with their Log domain counterparts. A 5^{th} order Sinh Chebyshev low pass filter is compared head-to-head with a corresponding and also novel Log domain class-AB topology, confirming that Sinh filters constitute a solution of equally high DR (100+ dB) with half the capacitor area at the expense of higher complexity and power consumption. The theoretical findings are validated by means of measured results from an 8^{th} order notch filter for 50/60Hz noise fabricated in a 0.35μm CMOS technology. Measured results confirm a DR of 102dB, a moderate SNR of ~60dB and 74μW power consumption from 2V power supply.

Declaration

The systematic synthesis method for the design of high order Sinh filters presented in Chapter 4 was carried out in collaboration with Mr. Konstantinos Glaros (Department of Bioengineering, Imperial College London).

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To my parents, *Michalis* and *Fotini*

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Abbreviations

ADC: Analog-to-Digital Converter

AP: All pass

ASIC: Application Specific Integrated Circuit

BAN: Body Area Network

BP: Band pass

BSN: Body Sensor Network

CAS: Circuit and Systems

CMRR: Common Mode Rejection Ratio

CMUT: Capacitively Micro-machined Ultrasonic

CMOS: Complementary Metal Oxide Semiconductor

CW: Clockwise

CCW: Counter-clockwise

DR: Dynamic Range

DTL: Dynamic Translinear

ELIN: Externally-Linear-Internally-Non-Linear

ECG: Electrocardiogram

EMG: Electro-myogram

EEG: Electro-encephalogram

EOG: Electro-oculogram

EU: European Union

ESS: Exponential State Space

GML: Geometric Mean Law

HRV: Heart-Rate-Variability

HML: Harmonic Mean Law

IC: Integrated Circuit

IF: Intermediate frequency

LHS: Left Hand Side

LO: Local oscillator

MI: Modulation index

NHS: National Health System

ODE: Ordinary Differential Equation

PAN: Personal Area Network

PPG: Phono-cardiography

PSD: Power-spectral Density

PTAT: Proportional to Absolute Temperature

RHS: Right Hand Side

SNR: Signal-to-Noise Ratio

SoC: System on Chip

SNDR: Signal-to-Noise-plus-Distortion-Ratio

SC: Switched Capacitor

SFG: Signal Flow Graph

STL: Static Translinear

THD: Total Harmonic Distortion

TL: Translinear

UWB: Ultra-wideband

UDR: Useable Dynamic Range

WBAN: Wireless Body Area Network

WI: Weak Inversion

1 Motivation

The increased life expectancy in developed countries combined with the need for cost-effective and practical healthcare solutions dictate the pace of progress of biomedical systems. Fully integrated solutions occupying small chip area and consuming low power have been a sought after target. Such a trend imposes unavoidable challenges to the analogue signal processing part of systems [1-4] whereby continuous-time filtering plays a vital role for a wide range of both mature (i.e. implantable pacemakers, cochlear implants, hearing aids etc.) and emerging (e.g. Wireless Body Area Networks) applications.

Ultra low power wireless connectivity among devices placed in, on and around the human body, is considered a key technology, enabling unprecedented portability for the monitoring of physiological parameters in the hospital, at home and on the move as well as for replacing or enhancing an impaired or lost functionality of an organ or simply for providing feedback about people's well being [5-6], all of which could provide a solution to the current problems faced by the healthcare sector globally.

The wide acceptance of such biomedical systems, which are directly challenged with respect to their performance and functionality, in a low power supply regime, will depend on existing and in progress developments in areas ranging from battery technology through to circuit design and material science.

The scope of this thesis is to explore the potential of a relatively new continuous-time filtering paradigm termed Hyperbolic-Sine (Sinh) filtering. This type of filters are the outcome of the perpetual effort of the Circuits and Systems (CAS) community towards the realisation of low power, high dynamic range (DR) filters which can be fully integrated on a small chip area.

The attractive properties of CMOS Sinh filters when compared to passive and active linearized (G_m-C, MOSFET-C) -often implemented by off-the-shelf components- continuous-time filters can be summarized in a) electronic tuning of the frequency response and full integration on-chip without the need for off-chip capacitors b) low power consumption by means of active devices operating in their weak inversion mode and c) a wide input dynamic range without the need for power to be spent on linearization schemes. Moreover, Sinh filters can achieve a wide dynamic range at half the capacitor area required by other filters with which they share the same design principles (in the family Externally-Linear-Internally-non-Linear filters where they belong) due to their inherent class-AB property. For the above reasons the theoretical and practical performance of CMOS high order Sinh filters is investigated under the perspective of their integration in the analogue front-end part of Wireless Body Area Networks (WBANs) due to their importance as a biomedical system in the healthcare revolution (see Figure 1.1) which is driven by social [7-8], demographic [9-13] and financial reasons [5,14-18].

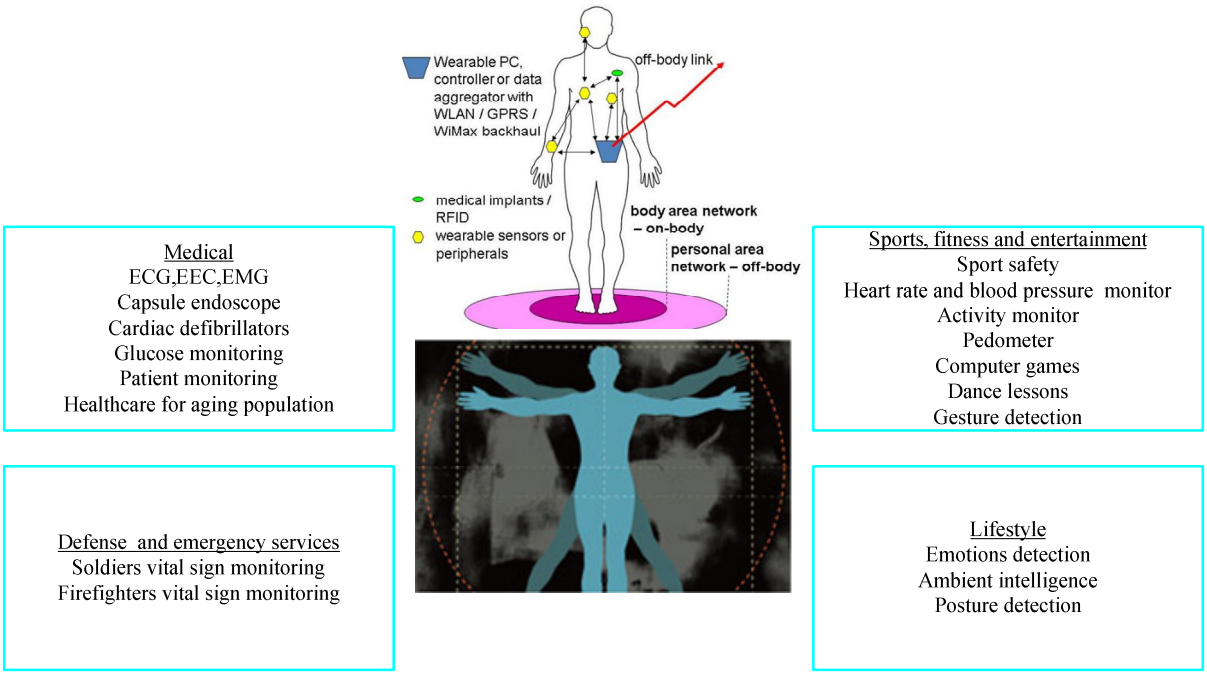


Figure 1.1: Examples from possible applications of WBANs [5].

1.1 Unobtrusive health monitoring

In the past, healthcare has focused on short-term treatment of life-threatening problems and has mostly been reactive rather than proactive [19]. Moreover, access to healthcare has been has been limited in the developing or third world countries or even among the lower level income people of the wealthy and technologically advanced places.

Recording and displaying bioelectric events required the development and adaptation of a variety of primitive instruments, not all of which were electronic [20]. Since 1905 when Einthoven transmitted ECGs from a hospital to his laboratory by directly connecting immersion electrodes to a remote radio, till today, the field of continuous and unobtrusive monitoring has gradually matured and benefited from technological advances. The most popular example of portable/ambulatory monitor is the Holter monitor [21] which is still used to continuously monitor the electrical activity of the heart.

Research towards wearable monitoring is evident since 1996, when Zimmerman explained the concept of using the human body as a channel of communication and presented the concept of Personal Area Networks (PANs) to demonstrate how electronic devices on and near the human body can exchange information by capacitively coupling tiny (a few pA) currents through the body [22]. It took almost seven years for his ideas to materialize [23] in the form of a prototype of a (3cmx3cm) wearable transceiver for intra-body communication.

Visions describing wearable technologies that will silently monitor heart rhythm, detect irregularities and alert emergency personnel in the event of a heart attack, also appear as early as 1999 [24]. In 2000 the concepts of Body Area Networks (BANs) and ubiquitous computing begin to appear in publications of IEEE. In [25], a survey of the so called context-aware computing research until 2000 is provided. By then the concept of wearable [26] BANs was well conceived and its appearance as a title of scientific papers either with that term or else referred to as PANs [27], mobile or ubiquitous computing [28] or tele-medicine/

tele-monitoring [29] started to increase rapidly [30-32]. Extensive literature review of telemedicine systems and their employment in disciplines ranging from cardiology to locating geographical position and physical activity are summarised in [33-34] for a timeline of 35 years (1966-2001).

Since the establishment of the Holter monitors, technology has brought about improved and much more practical versions of heart monitors as well as numerous almost seamless fitness heart rate monitors in the form of watches, rings, wallets, armbands and many other comfortable objects [19,35-36]. Moreover the notion of a computer has changed as we are moving towards ever decreasing dimensions of personal computers (PCs) which take the form of personal digital assistance devices (PDAs). Nowadays we are well past the transition from one computer for many people to a many-to-one correspondence which is often termed as ubiquitous, pervasive or mobile computing.

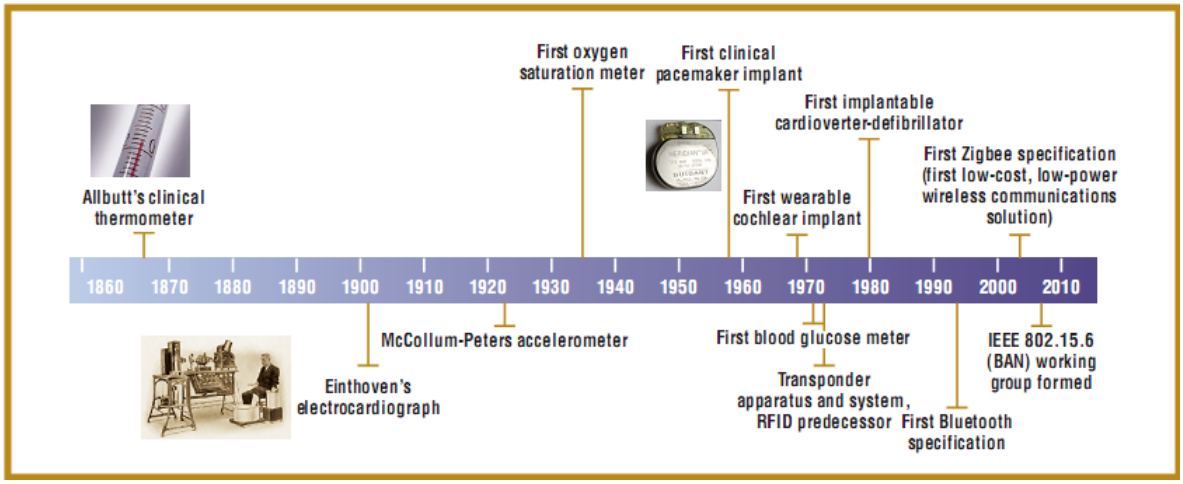


Figure 1.2: Milestones in sensor and wireless technology [37].

The bridging of technological gaps (Figure 1.2) has also allowed the incorporation in daily life of small enough to be discrete, wirelessly networked sensor-systems [38-39]. In the last five years the research efforts in various fields have paid off by the emergence of a plethora of working prototypes [40-47] of this new generation of devices with increased wireless capabilities, ease of use and functionality [35,48]. These systems can be wearable [19,46,49-62], disposable (patch like [63-66]), implantable [67-69] or swallowable [70-71] and are capable of real-time processing, giving feedback [41,72] or even responding to an abnormal event by warning or action [73-75] and the interest towards their development [60,64,76-86] is widespread globally [14,87-88].

A number of collaborative research projects have been funded by the 5th and 6th research framework programme of the European Commission which has also committed billions on projects for the development of independent-living technologies [38,89]. During the 6th framework for example, emphasis was placed on personalization of health care systems and BANs [44,89-91] with the focus on developing technology, components and communications infrastructure for home care while encouraging maintenance of fitness, social activity and cognitive engagement.

The realisation that even within the hospitals, there are a lot of unmonitored cases especially in general wards where failure to respond to patients' deterioration increases costs in the sense of both money and lives, [92] has made clear the need to introduce cost-effective, early detection systems in general wards. Portsmouth NHS trust is an example of cost reduction of 1 million pounds in a year by introducing vital signs monitoring system Vital PAC™ into 3 wards [93-94]. Taking this example of improvement of the workflow of a hospital a step further, it can be realized how useful it will be to be able to harvest data from a global network of continuously monitored patients (and non-) from smart phone based data

systems. This could enable health professionals to understand the minute by minute changes in body chemistry that occur for instance in response to medication, stress or infection [95].

Gaming industry is also pushing this technology forward by incorporating more sophisticated interfaces based on human movement. BANs are well positioned for this purpose since they could be used to deliver biofeedback and interactivity for the next generation of fitness and entertainment applications.

Making use of BANs in feedback systems can also be deployed for the control of prosthetics or remote assistive devices [24]. Electro-myogram (EMG) signals from the eyelid or jaw might be used for example to control a device that assists or replaces a limb or to activate a robotic device that opens doors or controls simple household appliances. Although new materials [96] and advances in electronics have made prostheses more functional, there is still a lot of room left to improve the currently unnatural control mechanisms [97-98].

BANs could be also very useful as part of drug delivery and blood glucose regulation systems facilitated by implantable biochemical sensors [24]. Multi-parameter blood analysis will enable continuous multi-analyte measurements with wearable devices during normal activity at home or at work through multi-sensor arrays, the fabrication of which will rely on the use of micro-technologies to make these devices as unobtrusive as possible [89].

Feedback control through BANs which would continuously monitor physiological and bio-chemical parameters could also open exciting opportunities for realizing wearable /portable artificial organs such as portable dialysis devices small enough to be attached to a patient's belt [89]. Such devices require multidisciplinary work from the fields of ICT, biology, material sciences and electronics in order to mimic the physiological operation of natural organs successfully and be functional and seamless enough to be socially acceptable.

Finally, other emerging technologies such as ultra wideband (UWB [99]) radar communications and capacitive micro-machined ultrasound transducer (CMUT [100]) arrays

offer the opportunity of integrating imaging capability to the measurement of vital body signals. We could thus expect to see the evolution of ultrasound devices from large sophisticated scanners in imaging wards and portable bedside units to wireless handheld devices for remote diagnosis [89]. Beds with scanning blankets [101] which wrap around the patient, monitoring their internal organs is also not taken from a sci-fi movie anymore as we are getting closer in enabling that technology.

This Thesis is more concerned with the WBANs as an application area where Sinh filters could further increase their capabilities, having recognised the social and commercial potential of unobtrusive physiological monitoring technologies [102]. The next section will therefore be focusing on WBANs.

1.1.1 Wireless body area networks (WBANs)

WBANs, personal area networks (PANs), Body Sensor Networks (BSNs) or wearable intelligent sensors as often termed otherwise, are special purpose wireless sensor networks which incorporate multiple sensor nodes and/or devices placed in/at different parts of the body in order to sense biological (and non- e.g. location) information which is then transmitted over a short distance to a control device (wirelessly or not), worn or implanted in the body or placed at an accessible location. The collected data from the control device are then transferred to remote destinations by incorporating a wireless network for long range transmission [56,103].

Wireless sensor nodes are also termed Body Sensor Units (BSU) or motes i.e. tiny microcomputers capable of sensing, limited processing, and using wireless media able to communicate with other wireless sensor nodes in the network [39]. The motes combine processing, sensing, wireless networking and a power unit, in a tiny packaging placed on the human body as a patch or implant/hidden in the user's clothes allowing ubiquitous physiological measurements in the natural environment over an extended period of time. The

conceptual diagram of a general purpose WBAN is illustrated in Figure 1.3. Figure 1.4 illustrates the different blocks which implement the general concept of Figure 1.3. The sensor nodes create an interface to humans, typically encapsulating an energy source, multiple sensors, a mixed signal processor and a transceiver for communication. Some nodes also support data storage for feedback control to body-based actuators such as an insulin pump or a robotic prosthetic.

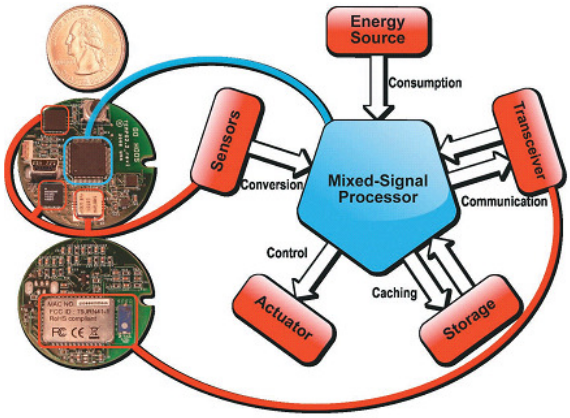


Figure 1.3: Conceptual diagram of a WBAN architecture [24].

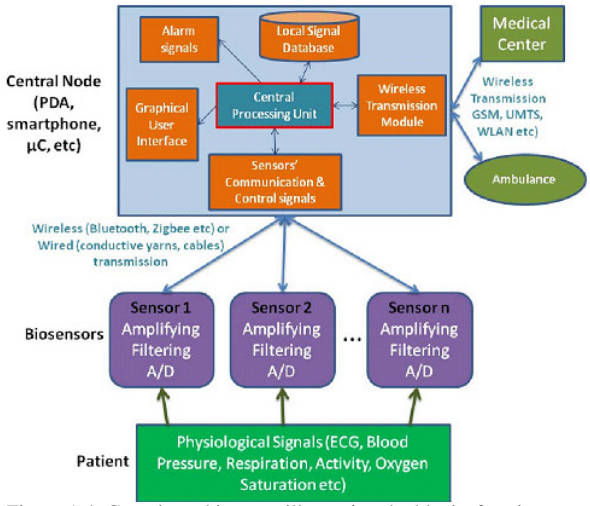


Figure 1.4: Generic architecture illustrating the blocks forming a WBAN [38].

A WBAN typically includes many physiological sensors, depending on the end user and application. Sensors fall into three main categories with respect to the measured parameter: a) physiological sensors which measure parameters such as ambulatory blood pressure, continuous glucose levels, core body temperature, blood oxygen, signals related to respiration, ECG, EEG, EMG, b) bio-kinetic sensors which measure parameters such acceleration and angular rate of rotation and c) ambient sensors which measure environmental phenomena such as humidity, light, sound pressure, and temperature. Finally information from several sensors can be combined to generate new information.

BAN sensors are heterogeneous due to placement constraints. Wearability requirements can vary drastically across applications. Some call for multiple wired networks

in a single garment, some others for multiple wirelessly networked devices securely attached at various body locations and others call for ultra-miniature, biocompatible implanted devices with less frequent communication with the outside world.

The sensors typically generate analogue signals that are either interfaced to standard wireless network platforms which provide computational capabilities or they feature on-sensor processing capability. Multiple sensors can share a single wireless network node. Signal processing can be sub-divided in pre-processing (signal acquisition which implies signal conditioning) and in further processing for feature extraction performed typically by a microcontroller or remotely at a PC. The network node continuously collects and processes raw information, stores them locally and sends them to the personal server. The type and nature of the application, will determine the frequency of relevant events therefore significantly determining the power consumption.

There are three types of communication links in the system. Communication links a) between the biosensors b) between the biosensor and the control device and c) the link between control device and the base station. Communication of the nodes with the external world can be wireless or not as far as the connectivity of the sensor nodes with each other is concerned although wires do not fit the concept of BANs unless they are seamless enough e.g. woven in appropriate textile. Typical radio-frequency (RF) communication includes UWB [103], Bluetooth, Zigbee while other forms of communication include pathways of the human body called bio-channels [104].

1.1.2 System-level hardware implementation considerations

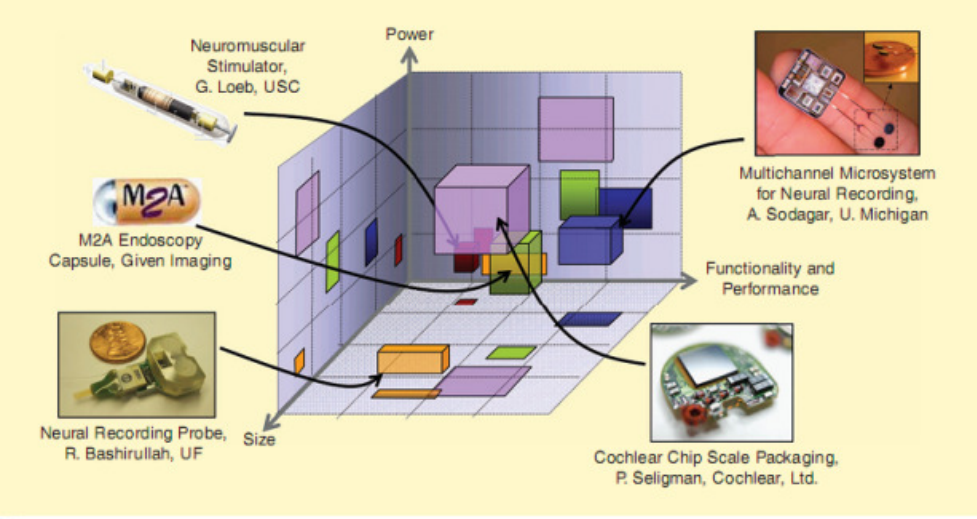


Figure 1.5: Hardware implementations of implantable biomedical systems parametrized in terms of size, power and functionality [71].

Although the requirements imposed on WBAN systems are application specific, the framework for their hardware implementation shares a common set of constraints with respect to size, power consumption and functionality across all systems. The interplay between these constraints determines important specifications such as the available processing bandwidth for the front-end electronics, the operating time and the communication range and bandwidth of the wireless link. Battery-operated devices with stringent size requirements (<16mm^2) are functionally limited by the size of the battery and their overall lifetime is limited by power consumption. In addition, the size requirements also directly affect the geometry and performance of the communication link. Parameters such as increased resolution per sensor channel, number of channels, computational bandwidth and transmission data rates generally determine the power budget and its distribution as well as the required integration area.

Table 1 : Power requirements of implantable sensors [105].

Type of sensor	Power requirement
Cardiac Pacemaker	1.34V and 650mAh
Sensors for ischemia	1.5V 120μW
Sensors for neural activities	200μW-480μW
Monitoring intra-cranial pressure	10mW
Temperature	2.25mW
Oxygen content	400μW
Blood dynamics	340μW
Glucose measurement	375μW
Urea sensors	600mW

Commercial sensors exhibit a wide range of power requirements (Table 1), calibration parameters, output interfaces and data rates. Therefore, earlier prototypes of BANs tend to use multi-chip solutions manufactured from off-the-shelf components. Engineering BAN nodes to accommodate this breadth of sensing requirements could either necessitate an application specific approach that minimizes the design space, improves efficiency and optimizes cost over a single application or alternatively, a high degree of configurability could improve cost over a much larger range of applications [24].

Processing data at a given rate (Figure 1.6) consumes less power on average than transmitting the data wirelessly therefore on-node signal processing can be even more beneficial in applications with a large number of channels and requirements for parallel processing. Most of the power budget is typically spent on the communication part of the system and can be further reduced by allowing sensors to communicate directly with each other over a short range sending a collaborative message with the important information [106]. Technologies such as smart textiles, magnetic induction, and body coupled communication have shown promise in relaxing the constraints even further. In the systems based on smart textiles, the wires which are woven into the clothes reduce the complexity and

power consumption but they have limited functionality when it comes to integrating more sensors in the system. Near field communication like that achieved by magnetic coupling, also suffers less path loss compared to radiative communication. More exotic means of communication such as using the human body itself as a communication channel can satisfy low energy requirements (Figure 1.7).

The need to replace or recharge batteries often makes the capabilities and desire for widespread use of BANs limited. Energy harvesting is also often incorporated in WBAN systems. Although increasing battery life through harvesting would revolutionize BANs, more research [105] is needed to create highly efficient hybrid solutions that incorporate energy generation and storage. One major drawback of harvesting systems is that the sources vary widely in the energy available per area therefore making their efficiency both placement and packaging dependent.

From the above discussion, it is clear that the hardware design of BANs is driven by trade-offs in size, power consumption and system functionality (Figure 1.5) wherein highly functional, ultra-low-power and miniature implantable devices are generally most challenging [71]. Low power operation and miniaturisation are the two critical requirements of the sensor nodes as they determine the lifetime of the devices and their suitability for being worn/carried by or implanted in a patient [103].

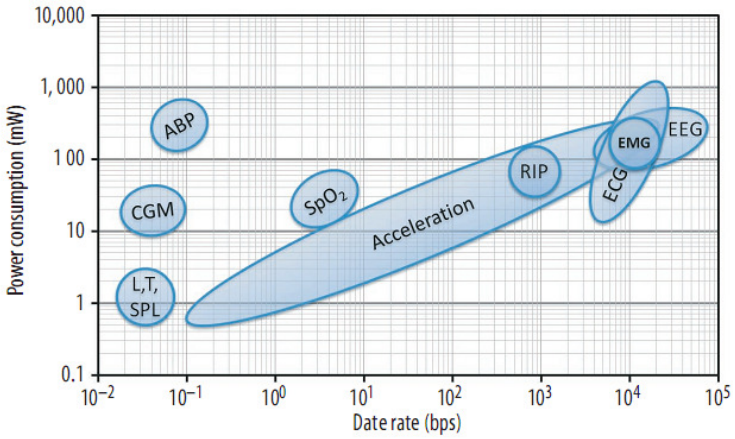


Figure 1.6: Average power consumption of continuous ambulatory monitoring applications. The differences suggest the need to support multiple applications in narrow range of data rates such as combining ECG, EMG, EEG on a single node or to support a single application across a wide range of data rates such as acceleration. ABP: ambulatory blood pressure, CGM: continuous glucose monitoring, L, T, SPL: light, temperature, sound pressure level, SpO2: pulse oximetry, RIP: respiratory inductive plethysmography [24].

Technology	Spectrum	Modulation	Channels	Data rate	Operating space	Peak power	nJ/b	Topology	Join time
Bluetooth classic	2.4 GHz	GFSK	79	1–3 Mb/s	1–10 m on-body only	~45mA @3.3V	50	Scatternet	~3 s
Bluetooth Low Energy	2.4 GHz	GFSK	3	1 Mb/s	1–10 m on-body only	~28mA @3.3V	92	Piconet Star	<100 ms
ZigBee	2.4 GHz	O-QPSK	16	250 kb/s	10–100 m on-body only	~16.5m A@1.8V	119	Star, Mesh	30 ms
ANT	2.4 GHz	GFSK	125	1 Mb/s	10–30 m on-body only	~22mA @3.3V	73	Star, tree, or Mesh	
Sensium	868 MHz 915 MHz	BFSK	16	50 kb/s	1–5 m on-body only	~3mA @1.2V	72	Star	< 3 s
Zarlink ZL70101	402–405 MHz 433–434 MHz	2FSK/4FSK	10 MedRadio, 2 ISM	200–800 kb/s	2 m in-body only	~5mA @3.3V	21	P2P	< 2 s

Figure 1.7: Characteristics of candidate wireless communication technologies for BANs [5].

1.1.3 Analogue front-end for bio-signal acquisition

Circuit design and in particular filter design is a critical part of the enabling technology of the systems described in the previous sections. It is directly linked to the extent of flexibility of the systems through size, power consumption and accuracy of the measurement or function they perform.

In physiological measurements the measured is usually a signal or quantity generated by an organ or system, derived from a tissue sample or elaborated from some associated physical property [107]. Measurements of temperature, blood pressure, respiration rate and

heart rate are often termed vital signs and are of most importance for the applications discussed in the previous section. Moreover, signals like electro-myogram (EMG), electro-oculogram (EOG), electro-encephalogram (EEG), are biological signals of great importance as control signals in implants, brain machine interfaces or simply for monitoring and treating or enhancing a dysfunctional organ -implants/prosthetics- as well as for animal and human studies.

Table 2: Amplitude range and bandwidth of common continuously monitored bio-signals [105].

Signal	Amplitude	Bandwidth (Hz)
ECG	0.1-5mV	0.05-250
EEG	1-300μV	0.5-60
EMG	10μV-15mV	10-500
EOG	0.01-0.1mV	DC-10
Respiratory rate	2-50breaths/min	0.1-10
Temperature	32-40C	0-0.1
Galvanic skin reflex	30μV-3mV	0.03-20
Blood pressure	10-400mmHg	0-50

The range of amplitudes of those signals and their frequency content are major factors which influence the design specifications of an instrument for their recording and processing. The amplitude range expected to be the input of the processor is what determines the required dynamic range (DR) of the signal processor, and is in turn dependent on a) the type of signal and the person itself where the signals are obtained from and b) the type of sensor (electrode) and its position relative to the location where the desired measured quantity originates from. Most physiological variables change very slowly, have amplitudes in the range of μV- mV (Table 2) and are typically affected by ambient and generated noise, dependence on other variables such as temperature, humidity and pH, electromagnetic interference or by perturbations caused by emotional or physical arousal. Moreover there is spectral overlap

between different physiological signals and between information and noise. For example ECG contains frequencies of clinical interest from approximately 10 Hz to a maximum of 250Hz depending on the application. EMG and nerve potentials have bandwidths extending from 3Hz-10kHz [108].

Monitoring systems for continuous multi-parameter monitoring [109] will typically necessitate the co-existence of an analogue front-end for pre-processing and a digital part to carry out more sophisticated algorithmic processing for feature extraction, classification and interpretation or decision making.

The analogue pre-processing blocks are required to compensate for the unwanted sensor characteristics and to increase the system signal-to-noise ratio (SNR). Especially in the case where a single chip is to be used for the pre-conditioning of multiple parameters, configurability of the electronics is an important feature in order to accommodate the breadth of input signals required to be processed.

The pre-conditioning is normally achieved by amplifiers and filters. Signal conditioning should preserve the information contained in the original signal and should not introduce any form of distortion that could destroy the contained information. Typical applications of analogue filters as part of the bio-potential signal acquisition include high pass, low pass, band reject (notch) and band pass filters. High pass filters are often used for dc offset elimination. For example, high pass filtering at 0.5Hz helps to reject slow baseline wander from electrode potentials associated with skin hydration drifts [110-111]. Low pass filters are typically used for artefacts elimination. For example ECG artefacts must be removed from EMG recordings in real-time myoelectric prosthesis control [112-113]. Also any movement that causes muscle utilisation generates noise that interferes with the ECG signal [88] and is often removed by a low pass filter. Other use of low pass filters is for anti-

aliasing after the analogue-to-digital converter (ADC) while notch filters are often used for elimination of power line interference of 50-60Hz[1].

Typically Bessel (high order) filters are preferred over other filter approximations due to their property of linear phase frequency response which ensures that the signal shape will remain undistorted. The general specifications that must be satisfied by the chosen implementation can be summarised in: low noise, high DR, low distortion, small die area, low power consumption and electronic tuning.

For example the measurement of action potentials and local field potentials simultaneously, imposes stringent requirements for the noise and bandwidth of the filters. Moreover, the necessity to implant the sensors which obtain those signals requires further care in setting power dissipation to be compatible with minimal tissue damage over long term use [67]. The spike activity which is detected with extra cellular electrodes is typically of the order of 90-120μV. On the other hand, local field potentials are much stronger signals in amplitude and require that the processing modules of the front-end are able to accommodate amplitudes of at least 4mV. The peak-to-peak swing of the ECG signal can also vary from 100μV up to 4mV from patient to patient. The realized signal processor therefore is required to have low input-referred noise (μV) and large linearity for a signal range of at least 60dB. The latter demand for linearity and large DR is at odds with low power consumption since power has to be spent on linearising the inherent non-linear active devices of linear filters (e.g. G_m-C) in order to accommodate a large DR.

[1] Low pass filters have also been used for that purpose set at 30Hz and below to reduce line interference (from ECG) with danger of the monitored bio-potential waveform shape to change [77] X. Qian, Y. Xu, and X. Li, "A CMOS continuous-time low-pass notch filter for EEG systems," *Analog Integrated Circuits and Signal Processing,* vol. 44, pp. 231-238, 2005, [107] J.Webster, *Medical instrumentation: application and design*: Wiley-India, 2009, [109] J. G. Webster, *Medical instrumentation: application and design*: 1978, 1978, [114] L. Hejjel and L. Kellenyi, "The corner frequencies of the ECG amplifier for heart rate variability analysis." vol. 26, 2005, pp. 39-47, [115] C. Ma, P. Mak, M. Vai, P. Mak, S. Pun, W. Feng, and R. Martins, "A 90nm CMOS Bio-Potential Signal Readout Front-End with Improved Powerline Interference Rejection," *Proc. IEEE ISCAS 2009,* pp. 665-668, 2009.. Band pass filters are required in implants like cochlea, retina and they are typically arranged in parallel filter banks.

1.1.4 **ECG: An important bio-signal**

Heart disease has always been in the spotlight of research [116-119] since it is identified as the major cause of death in most countries around the world [120]. Heart rate (HR) and heart rate variability (HRV) [114,121] obtained through ECG [122-124] are of great importance in determining human physiological status [125] although there are a number of other ways to obtain heart information with diagnostic value by considering the heart as moving muscle, blood volume pump (impedance cardiography [126]) or noisy pump (phono-cardiography [127-129]).

The principle behind ECG is to consider the heart as an electrical generator [130] and measure the electric potentials resulting from complex bio-chemical processes [109] by means of surface electrodes. The position and the number of electrodes required for an ECG measurement is determined by the kind of measurement (e.g. complete Q, R, S, T waves or R-R interval only, Figure 1.8). Irrespective of the application, typical ECG processing consists of the operations depicted in Figure 1.10. The complexity of each algorithm varies depending on the application. For example, noise filtering performed in ambulatory monitoring is much more sophisticated than that required for the analysis of resting ECG.

Filtering of the ECG is contextual and should be performed only when the desired information remains undistorted [122]. Mains noise, baseline wander due to respiration, high frequency noises from electronic devices, motion artefacts from changes in skin-to-lead impedance caused by subject movement, and EMG signal of muscle tissue movements, overlap with the frequency content of ECG [88] (Figure 1.9). For instance, mains noise filtering is suitable in a system dedicated to the analysis of heart rate variability, whereas it is inappropriate in a system for the analysis of micro-potentials due to their spectral overlap with the frequency content of power line interference [107].

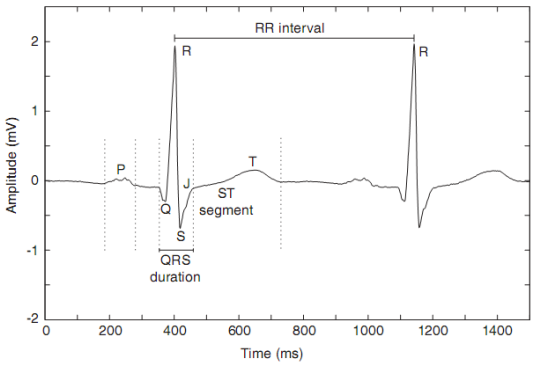


Figure 1.8: Definitions of the waves of a cardiac cycle. The onset and end of the P wave complex and the T wave respectively are illustrated with dotted lines [107].

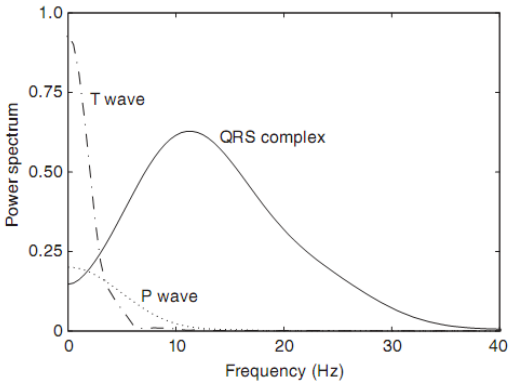


Figure 1.9: A rough guide of the individual spectral components of the P wave, QRS complex and T wave of an ECG signal. Note that large variations exist between beats of different lead, origin and subjects [107].

Removal of baseline wander is required in order to minimize changes in beat morphology that do not have cardiac origin [88]. This is especially important when subtle changes in the low frequency ST segment are analyzed for the diagnosis of ischemia [132]. The frequency content of the baseline wander is usually in the range below 0.5Hz. However, increased movement of the body during the latter stages of a stress test further increases the frequency content of the baseline wander. Even in cases where a stress test is performed under a sitting set-up, baseline wander is related to the motion of the arms and can severely distort the ECG signal [107]. The design of a linear time-invariant high pass filter for removal of baseline wander involves several considerations of which the most crucial is the choice of filter cut-off frequency and the phase response characteristic.

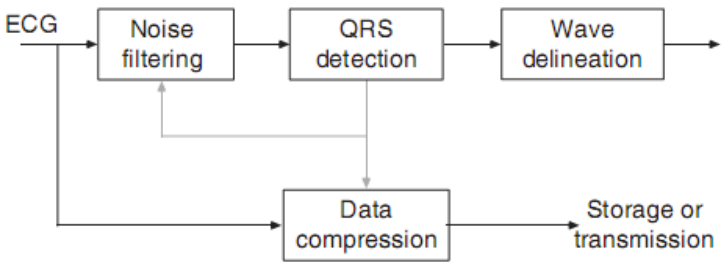


Figure 1.10 : Block diagram of the basic ECG signal processing [107].

Electromagnetic fields caused by a power line represent a common noise source in the ECG that is characterized by 50 or 60Hz sinusoidal interference, possibly accompanied by a number of harmonics. Such narrowband noise renders the analysis and interpretation of ECG difficult. Although various precautions can be taken to remove the effect of power line interference, for example, by appropriately shielding and grounding the electrodes, it almost always requires signal processing to remove it. Several techniques have been presented ranging from straightforward linear band stop filtering or amplification with a high figure of common mode rejection ratio (CMRR) (most commonly) to more advanced techniques that handle variations in the power line frequency.

The presence of the heart beat and its occurrence time is the basic information required in all types of ECG signal processing. As the QRS complex is the waveform which is most easily defined from the ECG, beat detection is synonymous to the detection of QRS complexes. The design of a QRS detector is of crucial importance because poor detection performance may propagate to subsequent processing steps and consequently limit the overall performance of the system. Moreover the detector must be able to detect a large number of different QRS morphologies in order to be clinically useful and able to follow sudden or gradual changes of the QRS morphology [107]. Although there are various approaches [133-135] some of which include wavelet transforms [76], neural networks and genetic algorithms, the general detector structure (Figure 1.10) consists of a pre-processor which is usually implemented as a linear filter followed by a nonlinear transformation. The linear filter is designed to have a band pass characteristic such that the essential spectral content of the QRS complex is preserved while unwanted ECG components such as P and T waves are suppressed. The centre frequency of the filter varies from 10 to 25Hz (Figure 1.9) and the bandwidth from 5-10Hz.

1.2 Success stories from WBANs between 2000-2011

A thorough review of the on-going projects on WBAN systems which have resulted in prototypes or commercial systems is offered in a number of sources [8,14,19,37-38,46,51, 56,64,85,87,89-90,103,106,119,136-138]. A number of examples from the numerous success stories of physiological parameter monitoring has progressed from primitive to highly sophisticated systems are provided in order to a) highlight the ongoing efforts towards shrinking dimensions and decreasing power consumption (see Figure 1.13) and b) in order to identify the gaps that need to be filled prior to successful and widespread introduction of such systems in our daily activity. Although important achievements in the overall hardware implementation of the featured examples are emphasized, the details of the analogue front-end of the systems, is of more concern. Figure 1.11 illustrates some of the key work in the development of WBANs while a number of examples from different filter implementations dedicated to ECG signal processing are listed in Table 3.

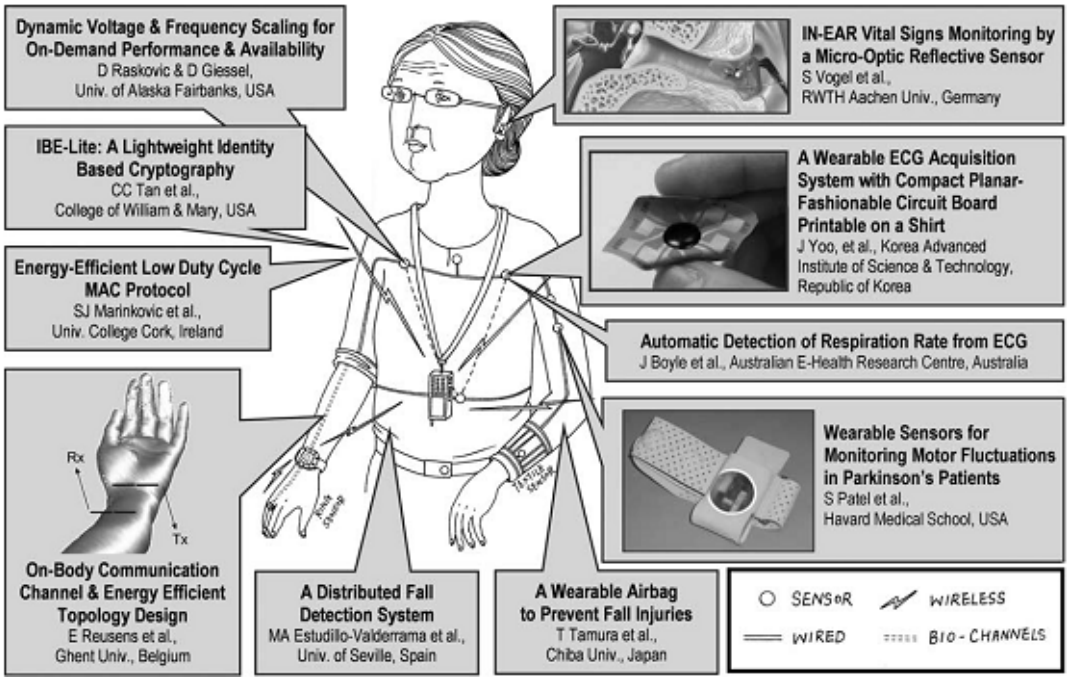


Figure 1.11: Some of the latest technological advances in the field of WBANs [84].

1.2.1 The Human ++ project (2001-2011)

The developments of the Human++ project from IMEC is an excellent example of the advancements which have allowed the passing form bulky wired devices to very discrete devices for continuous monitoring over the last 10 years [139]. An overview of the results achieved until 2005 is provided in [65]. The target has been towards the realization of miniaturized, intelligent and autonomous wireless sensor nodes for body area networks.

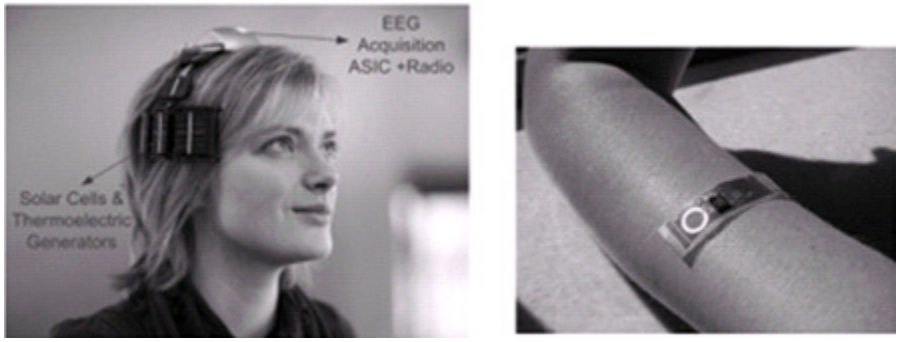
The project started in 2001 with a prototype for a wireless continuous EEG monitoring device comprising off-the-shelf components. It had 24 electrode inputs and a PAD receiver within the short range of the patient. The average power consumption was 145mW running on 4AA batteries for up to three days and occupied 500cm^3. The prototype of this primitive device can be seen in Figure: 1.12.

Figure: 1.12 The initial prototype of the Human ++ project [65].

Figure 1.13: The roadmap towards miniaturization [65].

By 2005, the bio-potential signal amplification and filtering which were based on discrete components in the original prototype, was substituted by a low power 25-channel bio-potential application specific integrated circuit (ASIC) [78] with 25 channels for the processing of EEG signals and one channel dedicated to ECG measurements. Adjusting the bandwidth (0.5-80Hz) of the front-end instrumentation amplifier [78] however required the incorporation of a huge external capacitor (1μF). The power supply was 2.7-3.3 V and the

power consumption a tenth of its predecessor prototype. New further improved generations of the ASIC [79,82] have resulted in two improved systems for continuous EEG measurements [82,140]. The EEG system presented in [140] is a 2-channel system based on energy harvesting. It operates without battery (consuming 800µW from 2V) (Figure 1.14). The ASIC in [79] is a low power and low noise (57nV/√Hz) readout front-end with configurable characteristics for EEG, ECG and EMG signals. The key to its performance is an AC-coupled chopping instrumentation amplifier which is capable of rejecting differential electrode offset up to +/- 50mV from conventional Ag/AgCl electrodes. The amplifier achieves 120dB CMRR. It also includes chopping spike filter implemented in the 0.5µm CMOS process and consuming 20µA from 3V. The filters are linear G_m-C topologies. The most power hungry part of the system is the radio communication part whereas only 25% of the power budget is allocated to the sensing analogue front-end part of the system.



a) b)

Figure 1.14: a) Prototype of the new generation 2-channel EEG which employs energy harvesting and runs without battery consuming only 0.8mW [140], b) the prototype of a flexible bandage to perform continuous ECG monitoring [65].

Another area where the outcomes of research from the Human ++ project clearly indicate the transition towards a new generation of devices, is the flexible bandage illustrated in Figure 1.14b) to perform continuous ECG monitoring. The device is 10 times smaller than a credit card (about as thin as 1-2 mm). It includes antenna, energy scavenger, advanced electronics for low power consumption and the target is towards a device of thickness

100µm. The core of the wireless ECG patch consists of a miniaturized wireless sensor node integrated on a flexible polyimide substrate. The power consumption is maintained below 2mW for continuous data streaming which allows more than 5 days of autonomy with a battery size of 20x20x5mm^3. The biggest challenge in developing such extreme miniaturization is maintaining functionality while dealing with naked chips, chip scaling, assembly process and integration of the entire technology in a biocompatible package [141].

1.2.2 AMON: A wrist-worn device for multi-parameter monitoring

AMON, a wrist worn device which is capable of measuring blood pressure, SpO2 and one lead ECG or -through an interface to external sensors- full 12-lead ECG measurements is presented in [41] and illustrated in Figure 1.15. In 2004, when the prototype was developed, AMON was the only handheld device which could combine multi-parameter measurements. In the first two years of this EU-funded project, the device had already been implemented and tested. The system prototype combines all sensors, communication and processing devices in a single ergonomic enclosure (Figure 1.15). The integration however has the disadvantage of making the signal acquisition -and in particular of the ECG- harder to obtain compared to distributed systems that place the sensors on several specific body locations. The power budget for this device is presented in Figure 1.16, indicating the demands of each sub-system. Note that the analogue part consumes 200mV from 5V supply.

Figure 1.15: Device prototype of the AMON wrist-worn multi-parameter system [41].

function	current	voltage	duty cycle	current eff.
GSM	3.5mA to 2.3A	battery	2.0 %	12.5mA
Inflating	220mA	battery	0.3%	0.7mA
Deflating	90mA	battery	1.0%	0.9mA
Analog Unit	40mA	5V	4.5 %	1.8mA
Digital Unit	9mA	1.8 to 3V	50%	4.5mA
SPO	10mA	3V	50%	5.0mA
Total				25.4mA

Figure 1.16: Break down of the power budget distribution of the AMON device [41]. The power budget duty cycle is based on a typical day of operation from a 1.25 Li ion battery.

1.2.3 Smart shirts for multi-parameter monitoring

In [46] (2008), sensors, transmission and data acquisition of the various physiological parameters (ECG, PPG, body temp, blood pressure, galvanic skin response, heart rate) as well as the position of the wearer, have been integrated into fabric (Figure 1.17). Three filters are included in the front-end (Figure 1.18), a 2nd order high pass and low pass filter, both of Butterworth approximation and a tuneable 50Hz notch filter. The details of their implementation are however not reported.

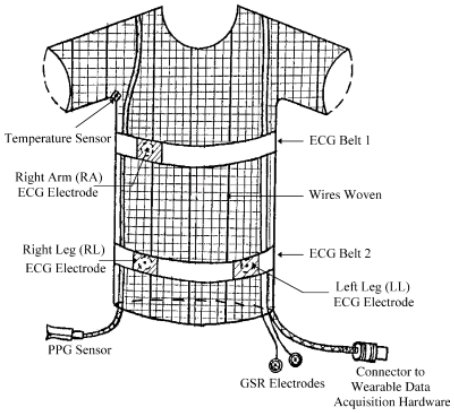


Figure 1.17: Wearable vest with integrated sensors for physiological monitoring [46].

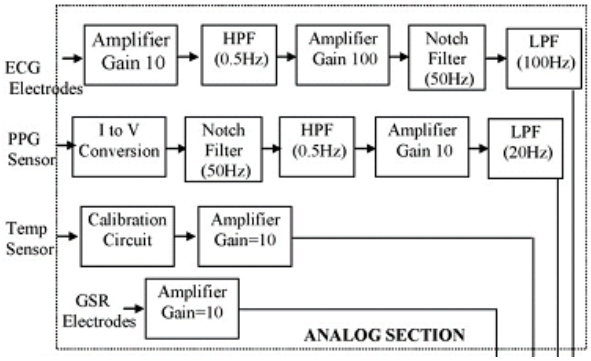


Figure 1.18: Block diagram of the hardware implementation of the wearable vest sensor [46].

Another smart shirt with wireless sensor network compatibility is designed in 2009 and fabricated for continuous monitoring of ECG and physical activity in [142]. The shirt consists of a wireless sensor node, an ECG and accelerometer sensor board and conductive fabric electrodes. This system uses a multi–chip solution (Figure 1.19). The top board

contains the communication blocks and at the bottom lies the sensor interface board. Two electrodes are extended from the ECG sensor board and knitted into the shirt. Two filters are included in the sensor board: a high pass at 0.5Hz and a low pass at 125Hz. The details of the implementation are not available.

Figure 1.19: Integrated wearable sensor node combined with a sensor board in a two-story structure [142].

1.2.4 A wearable real-time ECG device

In 2010, a wearable device (55mmx15mmx3mm) that provides real-time ECG (single lead) and acceleration acquisition has been proposed in [19]. The device is interfaced with a mobile phone and can operate up to 800hs using a small 500mAh lithium battery when processed data is transmitted in a periodic fashion. It is built around a Texas Instruments system-on-chip (SoC) which includes microcontroller, ADC and front-end electronics (including a low pass and a high pass filter consuming 90μA).

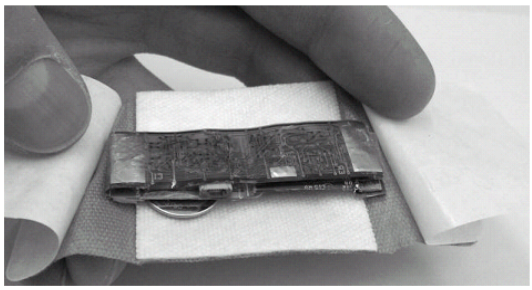


Figure 1.20: Prototype of the wireless health system in [19].

1.2.5 The LOBIN consortium project

The results of the LOBIN consortium project (2010) are presented in [137]. During the first and a half year since the start of the project, the platform was designed and each of its subsystems was separately tested in a real hospital environment. It is based on e-textiles and WSNs to monitor physiological parameters from several patients while also locate them within hospital facilities. Motion artefacts have been the major problem. The system uses a multi-chip solution for the data acquisition, processing board, and the wireless transmitter board while integration in a single board, is the target of future prototypes. The lifetime of the prototype is estimated to be 8-9h from a 600mAh battery. All sensors and the three boards are integrated in a washable smart shirt from Textronics Inc. The system includes filters for pre-processing but the details of implementation are not available.

1.2.6 Systems on chip for wearable or implantable BANs

A fully customized mixed signal silicon chip for wearable or implantable BAN is presented in [143]. It includes low-power analogue sensor interface for temperature and pH, a data multiplexing and conversion module, a digital platform based on 8-bit microcontroller, data encoding and RF with a few off-chip components. The chip has been evaluated and tested by connection to external sensors. The sensor interface consumes 5.7mW from 3 V. A 2^{nd} order low pass filter (200Hz) is included which together with a sigma-delta converter are responsible for 20% of the sensor interface power consumption. A standard OTA two-stage topology is used as filter.

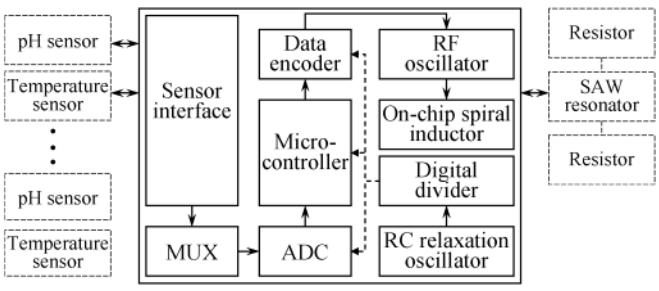


Figure 1.21: Block diagram of the SoC in [143].

A low power low voltage SoC was designed and implemented [144] in 0.18µm CMOS process in 2010, to provide a fully integrated solution for wearable health monitoring. It contains sensor interface, ADC, DSP and a radio-frequency transmitter. The system consumes 700µW at 0.7V when it acquires ECG and can afford continuous monitoring for 200hs without need to recharge the battery. However, it still requires off-chip components (antenna, supply decoupling capacitors). Analogue passive RC anti-aliasing filter has been used while the overall signal filtering is performed by digital filters (Figure 1.22, Figure 1.23, Figure 1.24).

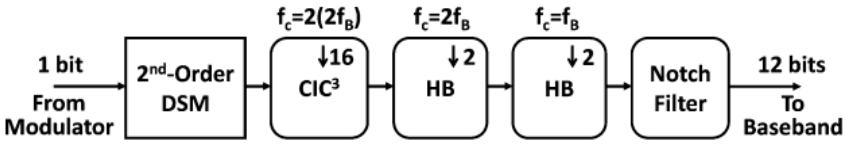


Figure 1.22: Block diagram of the digital filters of the system in [144].

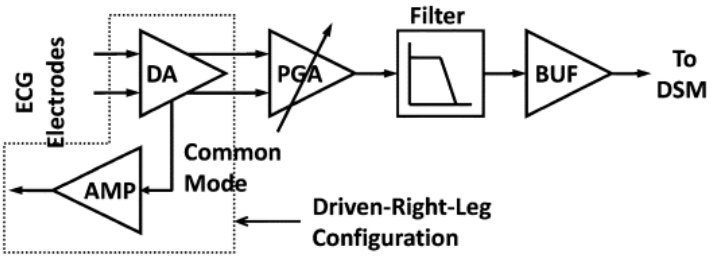


Figure 1.23: Block diagram of the sensor interface of the system in [144].

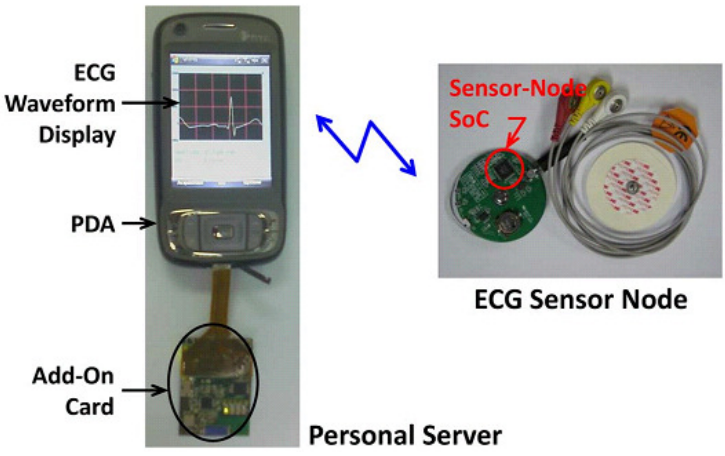


Figure 1.24: Prototype and set up for testing of the system in [144].

A self–configured body sensor network controller and a high efficiency wirelessly powered sensor for wearable continuous time health monitoring are presented in [64]. Its analogue front-end, consumes 12µW of which 5µW are consumed on the chopper amplifier. The sensor is configured in an adhesive bandage patch which also incorporates an inductor. The network controller detects the sensor position, configures the sensor type and wirelessly provides power to the configured sensor thus allowing communication with the selected sensor while consuming 5mW from 1.8V. The chip is fabricated in 0.18µm CMOS process and occupies 4.8mm^2 for the sensor IC and 15mm^2 for the controller. It can continuously operate and collect data for up to 8 days. It has been demonstrated for ECG. Analogue filters are not included.

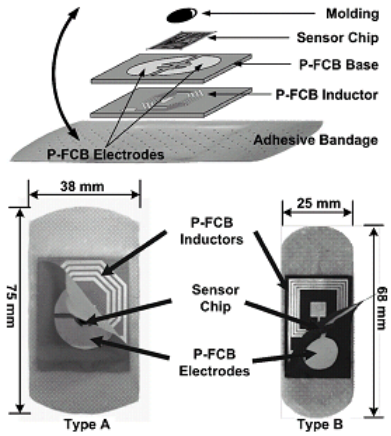


Figure 1.25: An adhesive bandage sensor [64].

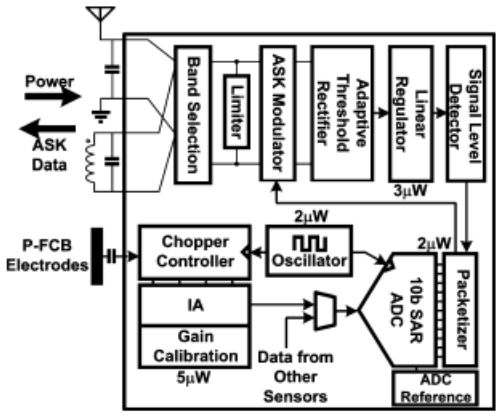


Figure 1.26: An adhesive bandage sensor: IC architecture [64].

1.2.7 Sensium™

A SoC has been developed between 2008 and 2010, specifically for wireless BSNs to monitor vital signs. The SoC (Figure 1.27) integrates a transceiver, hardware media access control protocol, microprocessor, input-output peripherals, memories, A-D converter with antenna and battery in a single chip wearable patch [63]. It is implemented in a 0.13µm CMOS technology and occupies 16mm^2. It can operate from as low a voltage supply as 0.8V. Mixed signal circuitry provides gain, filtering, biasing and buffering of the sensor inputs. The

encapsulated wireless sensor node is in the form of a thin flexible patch that can be attached to a patient for up to 7 days to measure ECG, heart rate, physical activity and optionally skin temperature. The Sensium^{TM} wireless link consumes 2.5mA from 1V supply. Active switched capacitor filters are included in the analogue front–end.

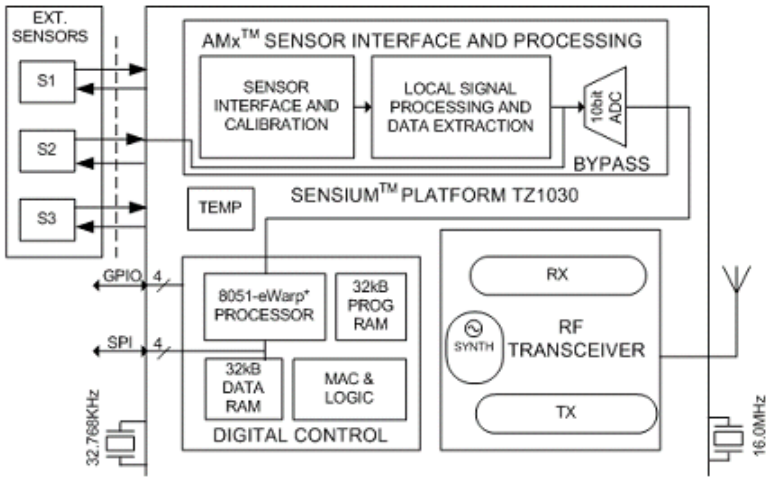


Figure 1.27: Block diagram of Sensium^{TM} [63].

1.3 Conclusions

A review of the state-of-the-art in the field of Wireless Body Area Networks with examples from both the academic and commercial world has been provided upon the recognition of the importance of developing and introducing such systems in our daily lives. Emphasis was placed on the analogue front-end part of the discussed systems and in particular on the implementation of continuous-time filters and the specifications they need to fulfil as critical parts of it. It is clear that there is margin for improvement by exploring alternative more suitable approaches for the hardware implementation of filter topologies for the discussed application.

Table 3: State-of-the art in filters for bio-potential acquisition

Year	**1999 [145]**	**2005[146]**	**2005[16]**	**2006[147]**	**2007[148]**	**2009[149]**		
Application	ECG(commercial)	Heart rate detector	heart rate measurement IC	integrated on-chip ECG system(commercial)	monolithic implementation of ECG signal acquisition system on chip	wireless wearable (wrist type) ECG prototype		
Filter (order)	8^{th} order(250Hz - 1kHz tunable)	8^{th} order band pass (8-30Hz)	0.2Hz Low pass	first order high-pass filter (0.05Hz) and a 2nd order low pass (150Hz)	Passive high pass filter and low pass filter at 10Hz	N/A		
Implementation	Switched capacitor (36.1dB SNDR)	Antializing filter is required	Current steering (poor linearity)	External capacitor, Gm –C	Switched capacitor but antializing filter is required and implemented with passive components	Discrete components and digital filtering for 60Hz noise		
Power consumption	270mW	3µA (13% consumed for the front-end)	N/A	N/A	N/A	N/A		
Power supply	10V	1V	N/A	+/-1.67V	N/A	3.3V		
Area	$65mm^2$	N/A	N/A	$7.5mm_2$	N/A	N/A		
Technology	2µm CMOS	N/A	0.35µm	N/A	0.35µm	N/A		
Year	2010 [150]	2010[151]	2010 [125]	2010[152]	2010[153]	2010[106]	2010[103]	2010[136]
Application	ASIC for ECG QRS detection	Detecting changes in the heart rate which relate to epileptic seizure (commercial)	wireless wearable heart rate monitor for continuous long-term variability studies	wireless, continuous time tele-cardiology system for detecting atrial fibrillation (commercial)	BAN based on RFID telemetry for ranges below 1m	wearable ECG consisting	multi-hoping network for a WBAN system	a portable monitoring device which measures and stores ECG, bio-impedance and acceleration data continuously
Filter (order)	N/A	N/A	N/A	Band pass filter (1-150Hz), 50Hz noise rejected by software	5^{th} order low pass filter at 250Hz	2^{nd} order high pass filter , low pass at 30Hz	Low pass filter and 50Hz rejection(software)	
Implementation	Wavelet decomposition on the digitized signal	N/A	N/A	N/A	Gm-C (50dB DR)	Active, digital	PCB, Tuning by changing capacitors	Passive
Power /current consumption	29µW	8mV when in operation (12% consumed by front-end interface)	0.5mW (for one channel)	30mA	452nW(filter)	N/A	N/A	
Power supply	1V	30h of autonomy for a 100mAh battery	3.6V(built in) weighs up to 7 days	N/A	1V	N/A	N/A	
Technology	N/A	N/A	N/A	N/A	0.18µm CMOS	N/A	N/A	

1.4 Thesis overview

The material of this Thesis is organised as follows: The second Chapter provides an overview of the field of Externally-Linear-Internally-Non-Linear (ELIN) filters, a broad class of filters to which both Log-domain and Hyperbolic-Sine (Sinh) filters belong. The technology and concepts behind the operation of Sinh filters and the advantage that they would bring to the systems which employ them when compared to other standard or ELIN IC filters is elaborated on. In particular, the findings of a recent study comparing a pseudo-differential class-AB Log-domain integrator with a practical CMOS Sinh integrator [154] is presented and therefore clearly demonstrates the potential of the Sinh filtering paradigm which is explored in this work for WBAN applications through high order CMOS Sinh filters based on the aforementioned practical Sinh integrator [154].

Chapter 3 focuses on the synthesis, analysis and implementation of all the (CMOS) Sinh integrators which have been published to date while discussing alternative options for their implementation. The practical integrator in [154] which is the basis of the novel topologies designed and fabricated in this Thesis, features the highest DR and benefits from design simplicity and synthesis elegance when compared to other CMOS and bipolar Sinh implementations. The Chapter concludes with a thorough discussion of the critical points in the design of the integrator at transistor-level while its comparison with the CMOS Sinh integrator proposed in [209] is also provided.

Chapter 4 introduces a novel synthesis method for high order Sinh filters and presents a review of existing synthesis methods through an example of a biquadratic filter. The detailed synthesis and extensive simulations from high order CMOS Sinh filters for biomedical applications and in particular for the ECG signal pre-conditioning in BAN systems is presented. Their performance and suitability for fabrication is assessed. Moreover, Chapter 4 provides a detailed simulation study of a 5^{th} order low pass CMOS Sinh filter of

Chebyshev approximation. A head-to-head comparison of the 5th order Sinh topology with its pseudo-differential Log-domain counterpart is provided.

Chapter 5 presents the first measured results from a high order CMOS Sinh filter. An 8th order CMOS Sinh notch filter for 50/60Hz noise and dedicated to a commercial product (Sensium™ [63]) has been fabricated and tested.

Finally, conclusions as well as future directions are presented in Chapter 6. In particular, the implementation of Sinh filters in bipolar processes for the purpose of high frequency biomedical applications (e.g. micro-beamformers for 3D ultrasound probes), is discussed and some preliminary results are presented.

2 Externally Linear Internally Non-Linear (ELIN) frequency shaping networks

This Chapter provides an overview of the field of ELIN filters and their underlying concepts. The capability of such filters to exhibit high DR under low power operation when compared to linearized conventional filters is explained and the limitations in the performance of CMOS weak inversion ELIN filters are discussed. The concept of class-AB operation, which has facilitated an increase by 23dB of the DR of Log-domain filters when they operate in a pseudo-differential class-AB mode is visited next while the inherent class-AB nature of the so-called Sinh filters -a sub-class of ELIN filters which relies on hyperbolic sine companding- is explained. The Chapter is concluded with the findings of a recent head-to-head comparison of an all-PMOS practical CMOS Sinh integrator proposed in [154] with its pseudo-differential Log-domain counterpart [157]. The potential of the Sinh filtering paradigm is explored in the following Chapters by means of the design and fabrication of high order CMOS Sinh filters based on the aforementioned Sinh integrator.

2.1 The need for companding in signal processing

Analogue active filters typically consist of an interconnection of active elements, capacitors, resistors and biasing currents. The output noise and power dissipation of the filter are determined by the currents used to bias the active devices. In a conventional filter design, the bias currents are constant with respect to variations in the strength of the input and are often set to be large enough to accommodate the voltage swings due to the largest input signal. The output noise is constant due to the constant biasing currents. The vertical separation between the power of the signal and the power of the noise in dB is termed the signal-to-noise-ratio (SNR). The maximum value of the signal that can be applied as input is determined by a measure of the acceptable distortion[2] for a given application. Any signal larger than the maximum signal that the processor can handle will cause the output signal to deviate from its expected linear relation with the input. Likewise, power consumption is also independent from the variations in the amplitude of the input signal. Typically the bias currents are set such that the largest expected signal can be processed without distortion at the output resulting in unnecessarily high power consumption and noise when the processor is called to perform less demanding tasks which require handling smaller input signals.

Consider for example a system with unity gain as illustrated in Figure 2.1. For a given in band signal V_s and noise signal V_n, the SNR is defined as the power ratio V_s^2 / V_n^2. It is often required that this value is no less than a specified minimum, SNR_{min}. The range of signal values over which minimum SNR is satisfied, defines the useable dynamic range (UDR) or simply referred to as DR[3] [158].

[2] Total harmonic distortion (THD) is a common measure for assessing linearity performance of a system. Throughout this dissertation, the definition of the THD has been considered to be: $[\sqrt{\Sigma}(\text{Harmonics})^2] / (\text{Fundamental})^2$ and quoted in (THD%).

[3] The DR is typically the same as the maximum signal-to-noise ratio (SNR) in conventional filters and implies that the minimum SNR is at 0dB. However the maximum SNR and the DR are two different things in companding filters due to the noise being dependent on the input signal. DR is defined here as the maximum signal the processor can handle for an acceptable THD (<4%) over the minimum signal (equal to the input referred noise floor integrated over the BW of the filter). The SNR on the other hand is calculated by considering the P-noise analysis where the dependence of the noise on the input signal is taken into consideration.

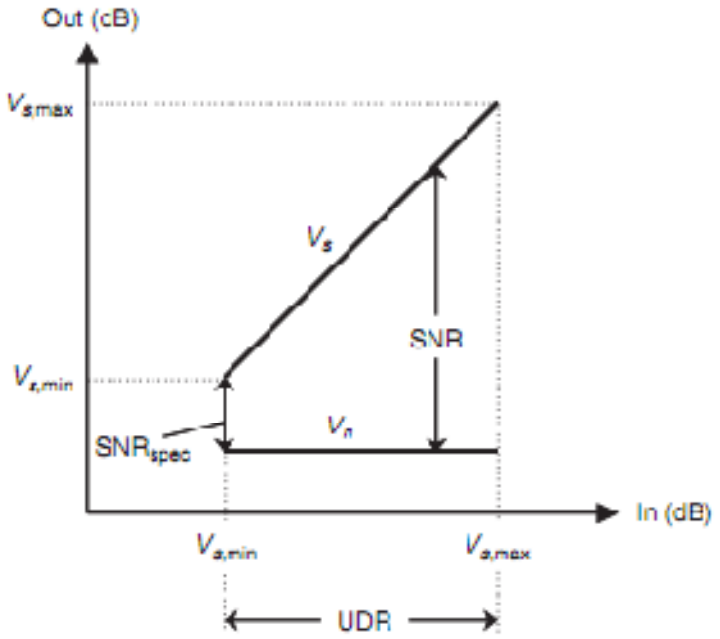


Figure 2.1: Output RMS signal and noise versus input RMS signal for a unity gain signal processor [158]. SNR_{min} in the text refers to SNR_{spec} while $V_{s,\,max}$ is the maximum signal that can be processed and $V_{s,min}$ is the minimum signal that can be processed respectively.

Despite the need to process large signals, $V_{s,max}$ should always remain well below the power supply in order to avoid distortion. Assuming a voltage supply restriction, the only option in order for the processor to have a large DR is to reduce its noise. The required value of the $V_{s,max}$ and the DR determine the minimum signal that can be processed. Taking the example of a first order RC low pass filter, with bandwidth $1/(2\pi RC)$, in which the resistor noise power spectral density, equal to $4kTR$ (where k Boltzman's constant) is processed by the equivalent noise bandwidth, $1/4RC$, a mean square noise of kT/C appears at the output. It is clear that low noise would require large capacitance. Moreover, for a given bandwidth ($1/2\pi RC$), increasing C would necessitate a decreased R and consequently larger currents would be required to drive the increased admittance leading to increased power consumption [158]. Similar results apply to a biquadratic filter. Taking the example of a band pass filter with quality factor Q implemented by means of the G_m-C approach, the centre frequency is given by $g_m/(2\pi C)$. The noise power for this circuit has been calculated as $V_n^2 \sim Q\gamma kT/C$ [158],

where γ is the excess noise factor of the transconductors. The value of the capacitor will be chosen accordingly such that it satisfies the specifications of Figure 2.1 according to:

$$C \approx \frac{q\gamma kT}{V_{s,\max}^{\ 2}} \times SNR_{\min} \times UDR \tag{2.1}$$

From the above, it is clear that large DR and small signal swings (necessary to achieve low distortion) require large capacitance. Moreover, the transconductor bias currents, assuming class-A operation and low distortion, must be larger than the maximum current these elements are expected to drive. The total bias current is proportional to the centre frequency, to the capacitor and the maximum signal. Multiplying the expression for the total bias current with the power supply V_{dd}, the power consumption can be derived as below [158-161]

$$P \approx kTQf \frac{V_{dd}}{V_{s,\max}} \times SNR_{\min} \times UDR \tag{2.2}$$

From this expression, it is clear that the power consumption is not only proportional to the centre frequency f but also to the DR. Therefore in order to improve the desired DR, the power consumption needs to increase. Although the digital part of the typically mixed signal IC biomedical systems directly benefits from lowering the power supply [162-163], this is not the case for the analogue part. Observing (2.2), the term $V_{dd}/V_{s,max,}$ implies that the maximum signal swings need to be well below the power supply for low distortion and therefore a low power regime implies that in order to maintain a high DR, power needs to be dissipated to linearize the active devices. Apart from necessitating large power to be consumed on the linearizing circuitry, this often leads to more complex topologies which strive to accommodate the extra circuitry required for linearisation in a low power regime. The matter is further complicated when high order filters or large filter banks are required

and especially when the cut-off frequencies are low since, large time constants (τ=*RC*) would require either very small g_m or very large capacitors in a typical G_m-C filter, often necessitating the off-chip implementation of the capacitors. From the above examples, it is obvious that it is very easy to run out of chip area and power budget when implementing filters which need to process signals with a wide DR by means of conventional methods.

A class of filters which do not rely on linearization techniques, and which exploit the large signal non-linear characteristics of the active devices, is the outcome of continuous research endeavours towards novel filter topologies that are not affected by the discussed trade-offs. Various terms have been used to coin this class of filters and all of them reveal some of the characteristics of the filters. The so-called Exponential-State-Space (ESS), Companding (*Com*pressing + Exp*anding*), Translinear or Externally-Linear-Internally-Non-Linear (ELIN) filters, are truly current mode topologies whose operation is not based on the small signal approximation. Instead, these filters make use of the large signal exponential *I-V* relation of either weakly inverted MOS or bipolar devices and therefore they exhibit non-linearly (e.g. logarithmically or hyperbolically) compressed voltage swings while the overall transfer function between their input and output currents is linear. The input currents are not restricted to the small linear region of the active devices unlike traditional filter techniques therefore achieving improved DR by 15-20dB [164] under a low voltage supply without the need for increased power consumption.

Companding, i.e. the underlying principle behind ELIN filters, can be used to ensure that the internal signals after they enter the processor remain a) above noise levels and b) below overload levels[4] imposed by the available power supply and the non-linearities of the active devices. This is achieved by compressing the input signal before it enters the

[4] Overload level is defined as the maximum input signal than can be processed for an acceptable distortion defined by the application.

processing module (i.e. filter) and expanding it again at the output to recover its full dynamic range as illustrated in the conceptual diagram of Figure 2.2.

Therefore, an extension of the available DR without unnecessary increase of the signal to noise plus distortion ratio S/(N+D) (see Figure 2.4) is possible as illustrated in Figure 2.3. In addition, when the input and output signals are currents, the overload levels are not directly related to supply-imposed voltage limitations. Hence, truly current mode circuits can be designed where the voltage swings are limited thus facilitating low power operation. For example, considering a "narrowing" of the DR of the processor internally by 40dB corresponds to power consumption savings by almost 10.000 times [158]. Although this is not true in practice due to the power consumption required for the biasing of the companding circuit, the power savings can however still be drastic compared to traditional filter implementations.

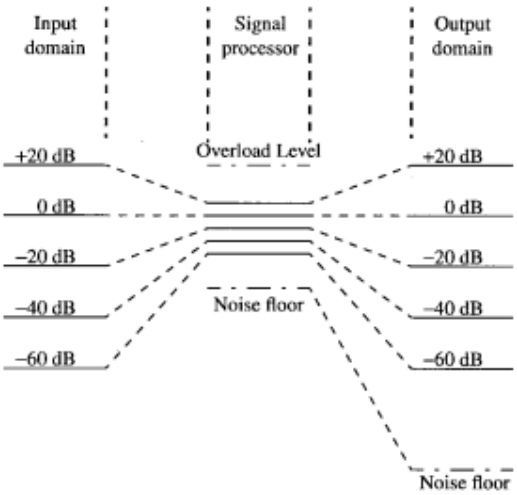


Figure 2.2: General concept of companding [156].

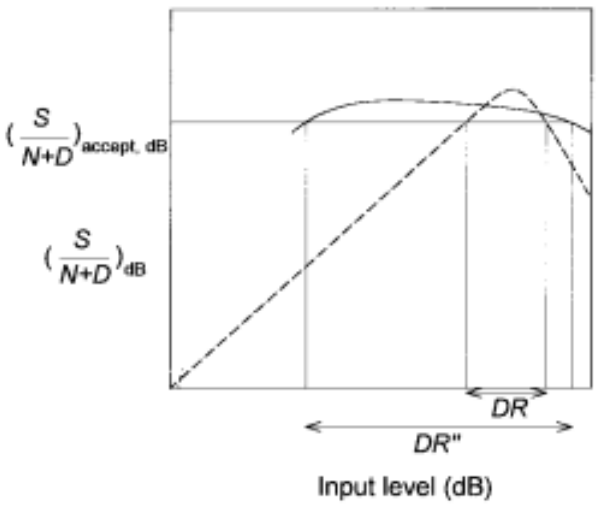


Figure 2.3: Broken line: S/(N+D) without companding. Solid line: S/(N+D) with companding. Note that although the S/(N+D) is not increased, the DR is greatly enlarged for the system emplying companding. Compare with Figure 2.4 which illustrates that an extended DR in a traditional filter is accompanied by a necessary increase of the SNR [156].

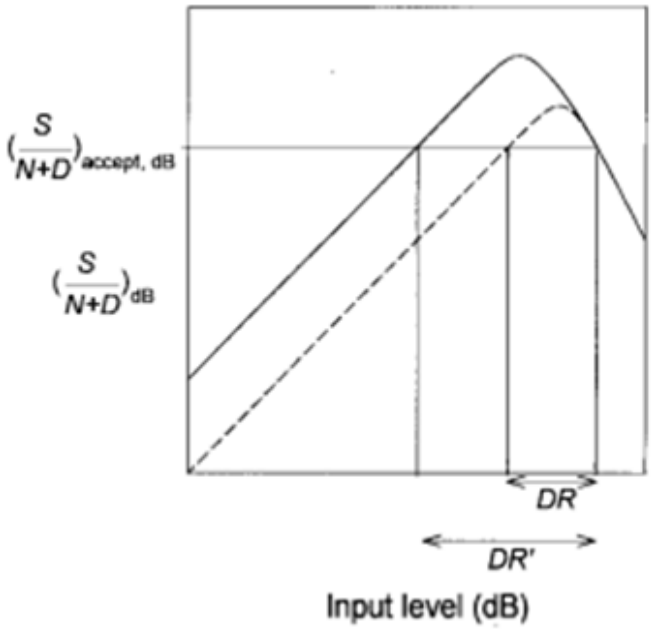


Figure 2.4: The solid line shows the improved S/(N+D) performance from lowering the noise floor of a traditional filter (without companding) thus leading to an extended DR [156].

2.2 Historical overview of companding

Companding is a technique that has been used for many years in communication systems [156]. The concept of companding in filters was introduced firstly by Adams [165]. Companding filters can be divided into two main categories; instantaneous and syllabic companding filters and they constitute a sub-class of ELIN systems [156] which are characterized by an internally non-linear but yet externally linear behaviour. In syllabic companding systems the compression function is updated by some measure of the average signal strength of the signal being processed while the compression in an instantaneous companding system is a function of the instantaneous value of the input signal.

The most familiar and widely researched sub-class of ELIN filters is the category of Log-domain filters which as the word implies, have logarithmically compressed voltages at internal nodes of the circuit. The Log-domain paradigm was introduced by Adams [165] in 1979. Almost 10 years later Seevinck observed the translinear character of Adams's filter

and independently proposed the first Log-domain filter operating in a class-AB mode [166]. Class-AB operation was till then only typical of output stages of amplifiers but had never been used in filter design. Frey was the first to both formalize and generalize the concept behind Adams's Log-domain integrator by introducing a synthesis method which enabled the design of a more general class of high order companding filters which he termed Exponential-Sate-Space filters (ESS) [167] due to his proposed design technique relying on non-linear mappings (typically of exponential or hyperbolic form) of the original linear state space of the filter (see Figure 2.5). Tsividis realized early on [156,168] that Log-domain filters fall within the even broader category of ELIN circuits which rely on the migration and exploitation of the concept of companding principle from communication systems to dynamical signal processing systems (Figure 2.6).

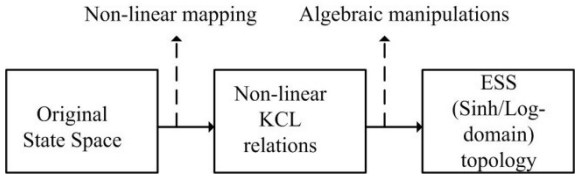


Figure 2.5: Frey's method for synthesis of ESS filters through non-linear mappings of the original state space description [169].

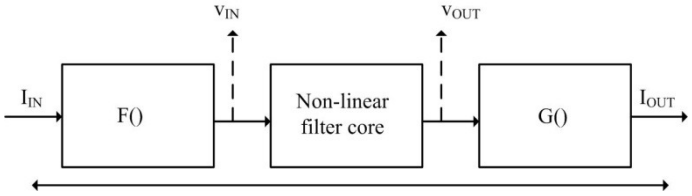


Figure 2.6: General ELIN companding filter [156].

Log-domain filters gained popularity for their performance and simplicity (a transconductor can be as simple as a single bipolar or weakly inverted MOS device) and attracted a lot of research interest early on. Toumazou *et al*. reported an implementation in weak inversion (WI) CMOS showing the potential of their low power operation [170]. The first experimental results were published by Perry and Roberts [171] while the first

experimental results in sub-threshold MOS were published by Ngarmnil *et al*. [172]. Frey demonstrated a systematic way of obtaining class-AB Log-domain filters which could further increase the DR by 23dB [173] and he formalized this approach in [174]. Puzenberger *et al*. demonstrated the suitability of ELIN filters for low-voltage applications and the favourable DR resulting from class-AB operation [203]. Different synthesis methods for Log-domain filters were adopted by various researchers [176-180]. Drakakis *et el.* adopted a "bottom up" approach for the synthesis of Log-domain filters termed Bernoulli-cell [181,183]. A general analysis method was published by Mulder *et al*. [182], who also coined the term translinear filter. Application of the underlying principle behind companding filters has been also used to implement non-linear dynamic functions [184]. Moreover, the noise performance and the secondary effects affecting the performance of ELIN circuits and their non-linear dynamics [185] have been investigated by various researchers [160,186-187,192].

2.2.1 Adams integrator: The first Log-domain filter

In 1979, Adams presented an input-output linear integrator comprising non-linear components (diodes), opamps, current sources and a capacitor [165]. The circuit is illustrated in Figure 2.7. Comparing this to the general companding diagram (Figure 2.2), it is clear that this circuit is a companding signal processor with compressing function being the natural logarithm and the expanding function being the exponential. Comparing Figure 2.7 with a typical RC filter, in Adams's integrator the linear resistor of the RC circuit has been substituted by a diode and a current source. The filter is electronically tuneable by means of the current source I_o. Assuming the exponential I-V characteristic ($I_D=I_S\exp(V_D/V_T)$) holds for the diodes, where I_s is the reverse saturation current and V_T the thermal voltage then from Figure 2.7 it can be deduced that:

$$I_{cap} = I_S \exp\left(\frac{V_i - V_{cap}}{V_T}\right) - I_o = C\frac{dV_{cap}}{dt} \tag{2.3}$$

$$I_{OUT} = I_S \exp\left(\frac{V_{cap} + V_T \ln(\frac{I_o}{I_S})}{V_T}\right) = I_o \exp\left(\frac{V_{cap}}{V_T}\right) \tag{2.4}$$

Taking the derivative of the output current, multiplying both sides of the equation by *C* and rearranging leads to:

$$CV_T \frac{dI_{OUT}}{dt} = I_{cap} I_{OUT} \tag{2.5}$$

Observe the similarity of this equation with (2.13). Multiplying (2.3) and (2.4) and substituting in (2.5) yields (2.6) which is a linear differential equation describing a low pass filter with cut-off frequency $\omega_c = I_o/CV_T$

$$CV_T \frac{dI_{OUT}}{dt} + I_o I_{OUT} = I_{IN} I_o \tag{2.6}$$

Adams proved the feasibility of creating frequency shaping networks which exhibit a linear input-output relation while allowing individual devices to operate in a non-linear large-signal (exponential) mode i.e. non-linear internal signal processing. Although the idea was attractive, the incorporation of opamps rendered it impractical.

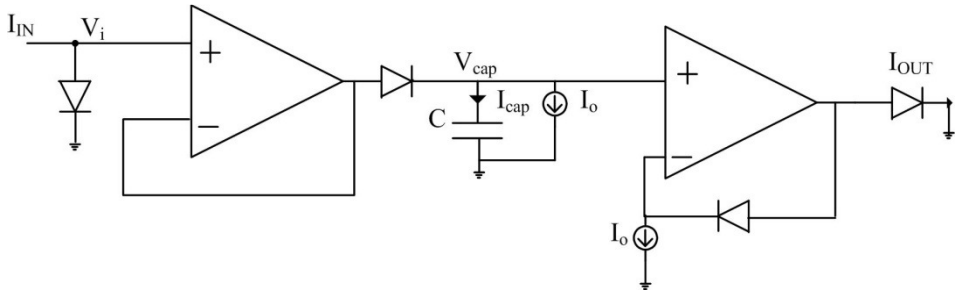


Figure 2.7: Adams' log-domain filter[165].

2.2.2 **Seevinck's class-AB companding Log-domain integrator**

In 1990, Seevinck proposed the BJT-only integrator illustrated in Figure 2.8 and he termed it current mode-companding. The circuit comprises two cross-coupled TL loops each incorporating a capacitor where the non-linear integration takes place.

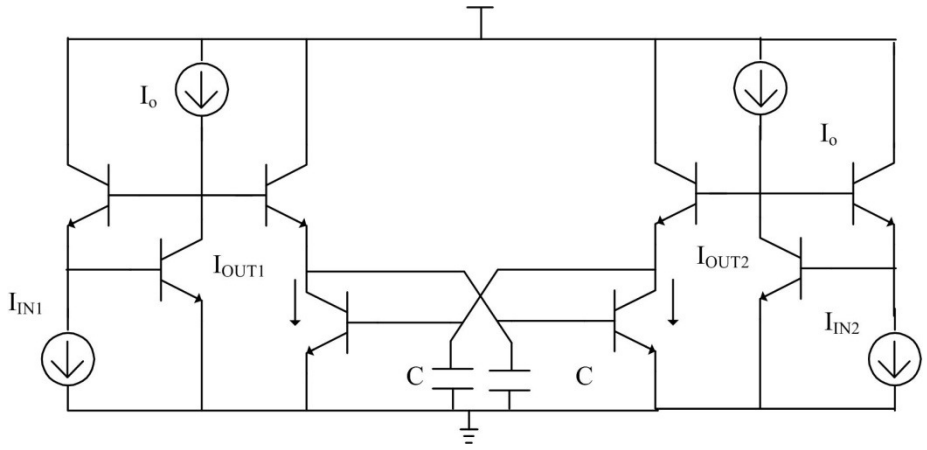


Figure 2.8: Seevinck's class-AB Log-domain integrator [166].

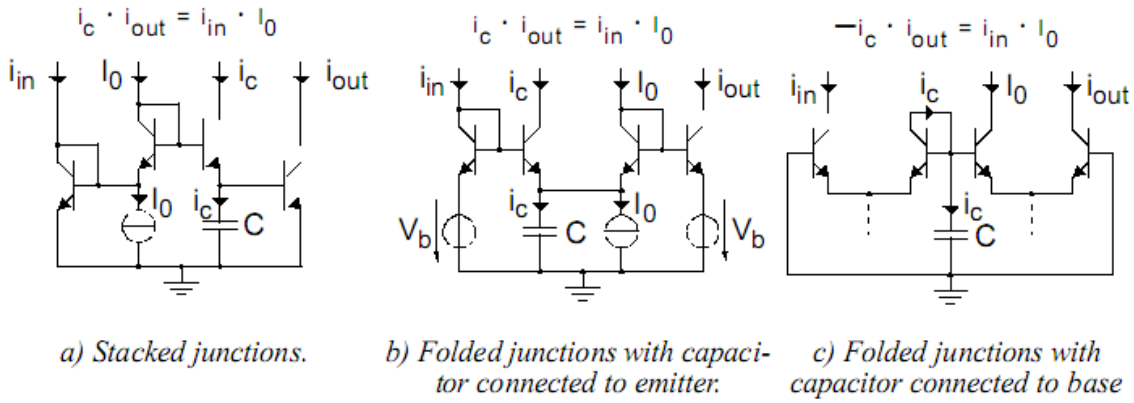
Each of the TL loops with the capacitor, implements a linear differential equation and upon their subtraction, it can be confirmed that the integrator of Figure 2.8 implements a linear class-AB integrator.

$$CV_T \frac{dI_{OUT1}}{dt} + I_{OUT1} I_{OUT2} = I_{IN1} I_o \tag{2.7}$$

$$CV_T \frac{dI_{OUT1}}{dt} + I_{OUT1} I_{OUT2} = I_{IN1} I_o \tag{2.8}$$

Irrespective of the synthesis approach [156,169,179,194] Log-domain integrators are generally based on basic four-transistor TL loops that implement: $i_c i_{out} = \pm i_{in} I_o$. Examples of such implementations are illustrated in Figure 2.9. The critical branch of the circuits typically comprises a diode connected transistor biased by a current source connected to the collector and another connected to the emitter. The minimum supply voltage required can be as low as 1V especially when alternating TL loops are used such as in Figure 2.9 b and c. In addition,

two basic circuit configurations for Log-domain filters can be distinguished: the capacitor can be connected at the emitter terminal such as in Figure 2.9 a and b or at the base of the devices that charge and discharge it like in Figure 2.9 c.



a) Stacked junctions. *b) Folded junctions with capacitor connected to emitter.* *c) Folded junctions with capacitor connected to base*

Figure 2.9: Basic implementations of low-voltage Log-domain integrators [195].

2.2.3 **Translinear principle**

Companding filters are based on Translinear principle (TL) principle for their analysis and hardware implementation. TL principle was firstly formulated by Gilbert [196] for the devices that are based on an exponential relation between current and voltage i.e. naturally the diodes and bipolar devices and later was expanded for MOS devices operating in weak inversion [197] while further brunches of this idea, led to the application of the principle in strong inversion under the assumption of quadratic behaviour [198].

The term is indicative of the fact that the small signal transconductance (g_m) of a translinear element such as a diode, a bipolar device (2.9) or a weakly inverted MOS device (2.10) is proportional to its diode, collector or drain current respectively:

$$g_{m,BJT} = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{B,E=const} = \frac{I_C}{V_T} \tag{2.9}$$

$$g_{m,MOSFET} = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{B,S=const} = \frac{I_D}{nV_T} \tag{2.10}$$

The principle states that "*In a closed loop containing an even number of ideal junctions (with exponential behaviour) arranged such that there is an equal number of clockwise facing and counter-clockwise facing polarities, with no further voltage generators inside this loop, the product of the current densities in the clockwise (CW) direction is equal to the product of current densities in the counter-clockwise (CCW) direction*"

It is mathematically expressed for MOS devices with the same aspect ratio as in (2.11) provided that: a) equal number of n- and p- type devices exist in the loop b) that all devices of the same type have equal threshold voltages (V_{th}) c) all devices have the same sub-threshold leakage current I_{DO} and d) all source-bulk voltages are constant and equal for all devices.

$$\prod_{CW} I_D = \prod_{CCW} I_D \tag{2.11}$$

As indicated by equation (2.11), the TL principle can be used to implement the arithmetic operations of multiplication and division. The operations of addition and subtraction are also straightforward in the current domain by means of current mirrors. Using multiplication/ division and addition/subtraction operations, linear combinations of the input and output currents can be forced through the transistors forming a TL loop. In combination with the multiplication and division operations supplied by the TL loops, a wide variety of polynomials and rational functions can be realised. A major advantage of the circuits implementing those operations is that they are theoretically (subject to good matching practice) temperature (assuming current sources are made proportional to absolute temperature PTAT) and process independent. Note however that in practice this is only true for the bipolar devices since the MOS devices in weak inversion, are process dependent (check the dependence of the g_m of a MOS device upon the sub-threshold slope parameter n,(2.10)).

The simplest example of a TL loop is that of a current mirror. The topology of Figure 2.10 is another very common TL circuit example termed current multiplier. The translinear loop indicated by the red line in Figure 2.10 comprises devices M_1-M_4 (assumed to have equal aspect ratio). The input to the circuit is a current and therefore the input needs to be a low impedance point e.g. the source terminal of M_2 while the output current is obtained from the high output impedance drain terminal of M_4. Devices M_1 and M_3 are biased by the dc current sources I_{o1}, I_{o2}. Note that the input could also be sourced from the drain terminal of M_1 whose impedance is lowered by the gate connection with M_2. This translinear loop is termed stacked due to the arrangement of the gate source voltages.

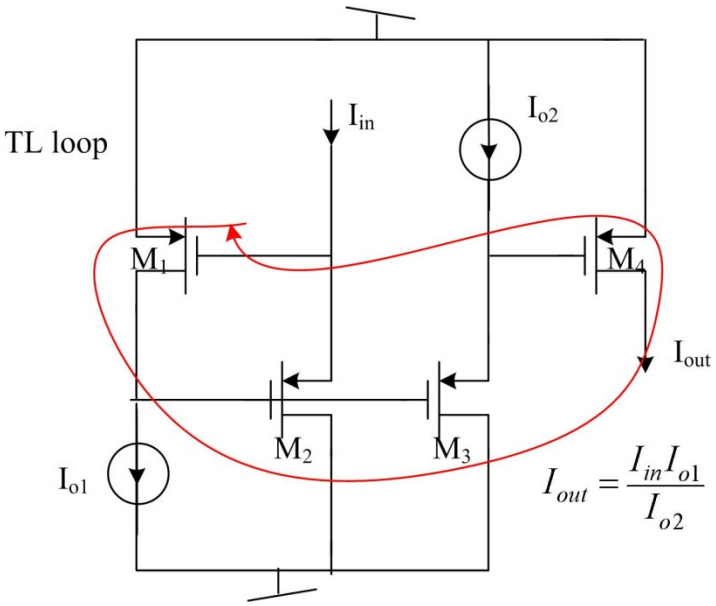


Figure 2.10: A stacked multiplier comprising four transistors (M_1-M_4) which form a TL loop.

An even wider range of functions can be implemented by means of current mode building blocks such as TL loops and current mirrors by introducing capacitors in the TL loops. This allows for the implementation of frequency shaping networks and non-linear equations. The transistor-level implementation of the current mode companding ELIN filters which were conceptually explained in the previous section is based on TL loops and capacitors. Mulder *et al.* coined the term (DTL) Dynamic Translinear Principle [178] in order

to describe the non-linear equations derived from incorporating a capacitor in a TL loop (or Static Translinear Loop). At the heart of the DTL principle lies the fact that the exponential function has a derivative which is equal to the function itself. The principle can be explained with reference to Figure 2.11. The derivative of the equation describing the collector current of a bipolar device is given by (2.12). Multiplying both sides of the equation by *C,* where *C* is capacitance, the term $C\mathrm{d}V_{BE}/\mathrm{dt}$, can be considered as the current flowing in a capacitor where a voltage V_{BE} has been applied, leading to (2.13). In other words, "the time derivative of a current is mapped to the product of two currents". The product of currents on the right hand side of (2.13), can be easily realised by means of a TL loop. Therefore the synergy of the two principles (STL and DTL) can be used to map any equation (linear, non-linear and frequency dependent) to a silicon implementation.

$$\dot{I}_C = I_C \frac{\dot{V}_{BE}}{V_T} \tag{2.12}$$

$$CV_T\dot{I}_C = I_C I_{cap} \tag{2.13}$$

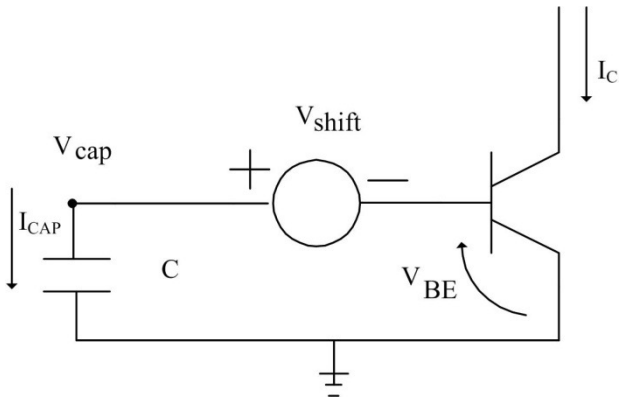


Figure 2.11: The concept of the DTL principle.

2.3 Considerations for CMOS companding filters

Despite the overall linearity of ELIN filters, they differ from linearized filters in two respects: Mismatches can cause distortion and their noise behaviour is complex due to its dependence on the input signal (in particular for class-AB ELIN filters) [156]. Moreover, since companding filters constitute a dynamic extension of translinear loops, the device non-idealities affecting the accuracy of the TL loops will also affect the performance of the filter as a whole.

Looking at the general companding block diagram of Figure 2.6, the two functions *F()* and *G()* must be perfectly co-ordinated. Unavoidable circuit non-idealities which include mismatches and high frequency effects will however make the co-ordination of the two functions less perfect resulting in non-lienarities at the output. Unlike ELIN filters, linearized filters exhibit the effect of mismatches as transfer function errors but not as non-linearities.

The noise dependence on the input signal in ELIN systems is also very important and can be particularly troublesome, in many cases making the use of a linear pre-filter necessary [156]. Interference coupled to intermediate points, can cause inter-modulation products between the interference components and the signal since the system is non-linear from the intermediate points to the output. These concerns are explained in more detail in the following sections.

2.3.1 Transconductance limitations

A bipolar device is considered as an ideal translinear element since its transconductance (g_m) is linear with its collector current (2.9). This is the result of the exponential relation between the collector current and the base-emitter voltage (I_C-V_{BE}) in bipolar devices. Contrary to bipolar transistors, the MOS device exhibits an exponential behaviour only for a limited region of gate-source voltages. Its drain current however, can

range over more than three decades while the exponential *I-V* characteristic still holds (2.14). This indicates that if current signals are used to represent the processed signals, a very wide range of signal values can be accommodated with the transistor remaining in WI.

$$I_D = \frac{W}{L} I_{DO} \exp\left(\frac{kV_{GB} - V_{SB}}{V_T}\right) = \frac{W}{L} I_{DO} \exp\left(\frac{kV_{GS}}{V_T}\right) \exp\left(\frac{V_{BS}(1-k)}{V_T}\right) \tag{2.14}$$

Note that the drain current is exponentially dependent on both the gate-source and the source-substrate voltages. When the source is shorted to the substrate (V_{BS}=0), then the expression for the drain current of a weakly inverted MOS device is codified in (2.15) where k is equal to 1/n, n being the sub-threshold slope parameter typically between 1 and 2.

$$I_D = \frac{W}{L} I_{DO} \exp\left(\frac{kV_{GS}}{V_T}\right) \tag{2.15}$$

The slope of the characteristic (I_D-V_{GS}) of a MOS device is lower than that of a bipolar device by a factor of (1/n) (2.16) and even lower by (1-1/n) factor when looking from the back-gate (bulk) terminal (2.17). Moreover, the g_m/I_D characteristic is not flat in weak inversion but shows a maximum before decreasing as the device enters moderate inversion.

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{VB,VS=const} = \frac{I_D}{nV_T} \tag{2.16}$$

$$g_{mb} = \left.\frac{\partial I_D}{\partial V_{BS}}\right|_{VG,VS=const} = \frac{(n-1) I_D}{nV_T} \tag{2.17}$$

In addition, the slope factor n depends on the biasing conditions due to the dependence of the depletion region capacitance on the source-substrate voltage. The slope varies with V_{BS} according to (2.18) where γ is the body effect coefficient and $\varphi_{F,}$ the Fermi potential of the device. Measured results of the variation of the slope factor are shown in Figure 2.12. It can be observed that for the usual values of $V_{BS,}$ the slope factor varies from around 1 to 1.5. In order to achieve a slope factor almost equal to one and thus more accurate TL behaviour, a large value of V_{BS} can be used. This helps reduce the depletion region capacitance by strengthening the influence of the gate on the surface potential [197].

$$n = 1 + \frac{\gamma}{2\sqrt{\varphi_F + V_{BS}}} \tag{2.18}$$

Another way to bring the behaviour of the MOS device closer to that of an ideal translinear element is by shorting the source to the bulk voltage but this is only feasible in devices that have separate wells which is the case for the PMOS devices in an n-well technology since the substrate of NMOS has to be connected to the most negative power supply. Otherwise, triple-well processes should be employed which apart from not being always available, they also have worse matching properties and are more costly.

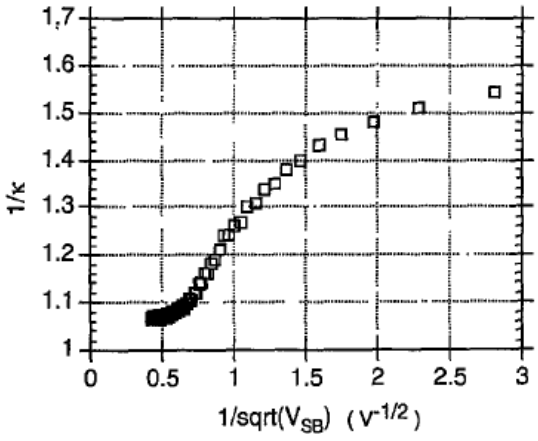


Figure 2.12: Dependence of the sub-threshold slope parameter n on V_{SB} [199].

2.3.2 **Output conductance**

Low output impedance can become significant drawback when TL loops which rely on accurate *I-V* characteristics need to be implemented since the difference in V_{DS} can introduce errors (2.19). Well known techniques for increasing the output impedance such as increasing transistor length, cascading and negative feedback can be employed to reduce the effect.

$$I_D = \frac{W}{L} I_{DO} \exp\left(\frac{\psi_s - V_{SB}}{V_T}\right)\left(1 + \frac{V_{DS}}{V_A}\right) \tag{2.19}$$

2.3.3 **Limited bandwidth**

A measure of the bandwidth of a MOSFET device is given by (2.20). The operating frequency (f_T) of the device is maximised when the maximum current (2.21), is used, for which the transistor is biased in weak inversion resulting in (2.22) [197].

$$f_T = \frac{g_m}{2\pi C} = \frac{I_D}{2\pi n V_T W L C_{ox}} \tag{2.20}$$

$$I_{DMAX} = 2n \frac{W}{L} \mu C_{ox} V_T^{\,2} \tag{2.21}$$

$$f_{TMAX} = \frac{\mu V_T}{\pi L^2} \tag{2.22}$$

In order to maximize the circuit bandwidth, minimum length should be used in the transistors. It should be noted that good design practice necessitates the use of devices with lengths 3-4 times the minimum feature size which implies f_T values much smaller than a few MHz. It is therefore clear that the design with high bandwidth is a challenge in WI. Sub-threshold MOS TL circuits are however very suitable for low to medium frequency

applications such as the biomedical applications discussed in Chapter 1 which extend from very low frequencies (sub-Hz) to audio frequencies (few kHz).

2.3.4 **Mismatch**

There are two sources of mismatch in MOS devices: firstly that of the threshold voltage and secondly that of the transconductance factor β (W/L $C_{ox}\mu_n$). The former is the dominant source of mismatch in WI circuits. Matching in sub-threshold deteriorates drastically when the voltage across the reverse biased source bulk junction is increased (Figure 2.12):

$$V_{th} = V_{FB} + \phi_o + \gamma(V_{BS})\left(\sqrt{\phi_o - V_{BS}} - \sqrt{\varphi_o}\right) \tag{2.23}$$

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}n_{ch}}}{C_{ox}} \tag{2.24}$$

Ignoring the dependence of γ on V_{BS} (2.18), it is clear that if V_{BS}=0, γ is not amplified by the V_{BS} bias. Also thinner oxide technology results in better matching of threshold voltage since γ becomes less significant (2.24).

Reduced voltage signal levels, sub-threshold region of operation and circuits that employ small geometries, make parametric variations due to fabrication process imperfections, increasingly important in determining the ultimate system performance and yield. Perfect transistor matching is impossible because of fabrication process variations and spatial "white noise" in physical parameters [200-201]. The task of matching becomes even more severe when both NMOS and PMOS devices are employed in the design and operate in sub-threshold. Good layout is then required in order to account for this and based on the equations below, using large devices is a way of improving matching at the expense of increased chip

area (2.25) and higher values of parasitic capacitances. AI_{dx} and AV_{TO} are constant parameters defined by the process foundry.

$$\sigma\left(\Delta V_{TO}\right)=\frac{\mathrm{A}V_{TO}}{\sqrt{WL}} \tag{2.25}$$

$$\sigma\left(\frac{\Delta I_D}{I_D}\right)=\frac{\mathrm{A}I_{dx}}{\sqrt{WL}} \tag{2.26}$$

2.3.5 **Noise**

The exact calculation of the noise in instantaneous companding circuits is complicated due to the non-linear behaviour of the circuits and the non-stationary nature of the noise sources [195]. The analysis of a simple first order low pass companding filter has been presented in [195] and will be summarized here in order to provide insight in the noise behaviour of companding filters. For the analysis it has been assumed that the noise sources are stationary current sources i_N(t) having power spectral density (PSD) S_N(f). The time domain differential equation corresponding to the first order system of Figure 2.13 is given by

$$\tau\dot{i}_{out}+i_{out}=i_{in}+i_N m(t) \tag{2.27}$$

Where $m(t)$ is defined as (df/dv)/g_m=G_m(i_{out})/ g_m and represents the signal by which the noise is modulated. The transconductance g_m represents the signal-independent transconductance which is responsible for the tuning of the cut-off frequency while the transconductance G_m is directly dependent on the output signal. For a Log-domain filter g_m= I_o/nV_T, where I_o is the bias current which tunes the cut-off frequency and G_m=i_{out}/nV_T leading to $m(t)$= i_{out}/ I_o. The model of the noisy companding filter is illustrated in Figure 2.13. The PSD of the output noise is given by (2.28) under the assumption that the noise and the input are not correlated. S_m is the PSD of the modulated noise signal.

$$S_{Nout}(f) = \frac{S_m(f)}{1+(2\pi f_T)^2} \tag{2.28}$$

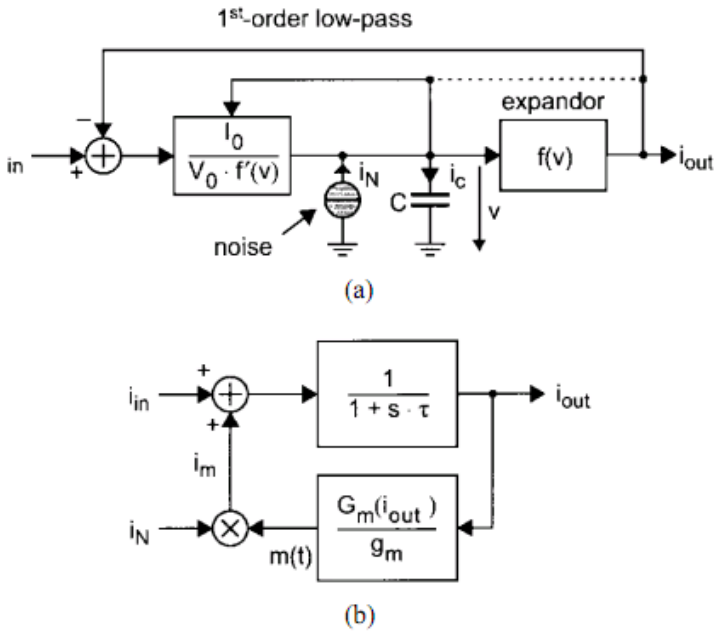


Figure 2.13: Noise in a first-order low-pass instantaneous companding filter [195].

The process of modulation can be explained with reference to Figure 2.14. The original spectrum of the signal is translated to the harmonic frequencies which are weighted by the corresponding normalized power M_n^2 where M_n represents the Fourier coefficient corresponding to the nth harmonic of the output signal. If the noise source is considered white, the modulated noise PSD becomes equal to the original noise multiplied by the power of the modulation signal M^2_{rms}. For a class-A Log-domain filter, the normalized power of the modulation signal M^2_{rms} is defined as $(I_o^2+I^2_{sig\text{-}rms})/I_o$ where $I^2_{sig\text{-}rms}$ is the power of the output signal without accounting for the dc component I_o. For a bipolar or MOS device in weak inversion, the white noise corresponds to shot noise and its PSD is given by $4kT\gamma g_m$ where k is the Boltzman's constant, T is the temperature and γ represents the excess noise factor. It should be noted that there are two contributions to the noise signal: noise due to the constant biasing dc current sources and noise due to the devices which are directly dependent on the

signal. The first type of noise has a constant PSD whereas the second noise source may be non-stationary. Here it is assumed that noise i_N(t) is stationary for simplicity. The output noise power is calculated by integrating the output noise PSD which for the assumption of white noise reduces to (2.29) where $1/4\tau$ is the noise bandwidth of the filter. This result states that in an instantaneous companding filter, the output noise power is proportional to the power of the output signal for large signals. Equation (2.29) for a Log-domain filter is codified by (2.30).

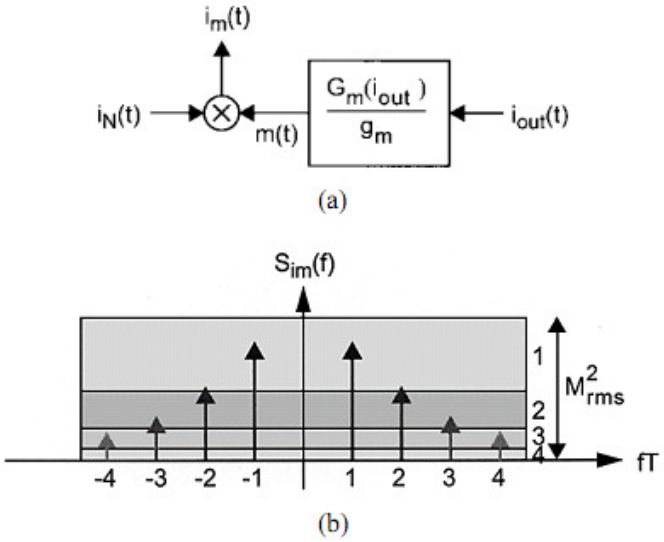


Figure 2.14: Noise modulation process [195].

$$I^2_{Nout} = \int_0^{+\infty} S_{Nout}(f)df = S_o M^2_{rms} \frac{1}{4\tau} \tag{2.29}$$

$$I^2_{Nout} = \frac{\gamma}{n^2}\frac{q}{kTC}(I_o^2 + I_{sig-rms}^2) \tag{2.30}$$

From (2.30) it is clear that in a class-A filter whose signal amplitude is restricted to be smaller than the DC bias current I_o, the noise is almost independent of the signal similar to conventional linearized active filters. On the other hand if the filter is operating in class-AB mode, where the signal is allowed to be much larger than the DC bias current I_o, the noise is

then dependent on the signal amplitude. This is illustrated in Figure 2.15. Observe that although the minimum signal is identical for both class-A and class-AB companding 1st order filters assuming identical capacitors and bias currents, the maximum signal on the other hand, is limited by the biasing current in the class-A case whereas for class-AB circuits it might be limited to higher values subject to the linearity performance of the filter which depends solely on the non-ideal effects such as devices departing from the weak inversion region of operation. Figure 2.15 shows that the DR of class-AB filters can be substantially extended without increasing the max SNR due to the noise almost increasing in proportion to the input signal and therefore without increasing the power consumption. This suggests that in order to exploit the larger DR available, instantaneously companding filters should be operated in class-AB. Measurements and simulations have shown that the DR can be increased by as much as 23dB [202-203].

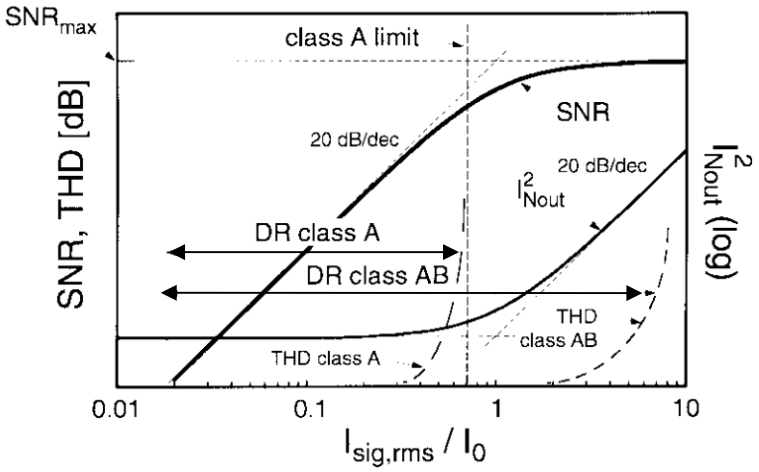


Figure 2.15: Output power of the noise, signal-to-noise and total harmonic distortion (THD) versus the input signal rms current normalized to the bias current [195].

The dependence of noise on the input signal can be particularly troublesome and in many cases. Care should be placed for possible sudden rise of the noise associated with large out-of-band signals which could affect the small in-band signals [156]. If a small desired signal co-exists with an undesired signal, upon increase of the out-of-band (undesired) signal,

the modulation signal will be large and can cause increase of the noise. Even if the unwanted signal is eventually rejected by the system, it will have left its trace in the system since the noise will increase and it will be dependent on the signal that has been filtered out. Depending on the application, this effect can be so troublesome that a pre-filter might be required to reduce the amplitude of large out-of-band signals [156].

Finally, for sub-threshold currents and low operating frequencies, flicker noise becomes a significant noise source in WI. Note that the noise performance improves for large geometries.

$$S_{i,flicker} = \frac{M_{g_m}^2}{C_{ox}WL}\frac{2\pi}{\omega} \tag{2.31}$$

2.4 Hyperbolic sine versus logarithmic companding

As explained previously, it is strongly recommended to operate instantaneous companding filters in class-AB mode for an extended DR without accompanying increase in the power consumption. The concept of class-AB operation is often met in signal amplifiers [204] and was applied to filtering first by Seevinck who proposed a class-AB filter based on cross-coupled TL loops in 1990 [166]. Later on, Frey recognised the potential of class-AB operation in companding filters and proposed a way by which Log-domain filters could operate in class-AB [203].

A class-A filter, is a module that handles the entire input signal by itself. At transistor level this would imply that such a module in order to handle a peak AC swing should have a bias level equal or greater than the maximum anticipated signal swing. This means that higher bias currents are required for maximum input signal swing but low bias currents are needed for lower noise. In class-AB circuits two modules handle half of the signal after it is

split in two positive phases based on a - typically nonlinear- splitting law[5]. The concept of class-AB operation for Log-domain filters is illustrated in Figure 2.16. Based on his approach, a class-AB Log-domain filter can be composed by means of two identical, class-A Log-domain filters which operate in parallel. The input to each filter is ensured to be positive by means of a pre-conditioning block which is termed current splitter and provides two strictly positive phases of the bidirectional input current. Therefore, the input to each of the class-A filters can theoretically attain arbitrarily large values without the need to increase the biasing level of the individual class-A sub-systems, theoretically leading to infinitely large DR restricted only by technology and power supply limitations. The class-AB Log-domain filters resulting from this approach are termed pseudo-differential and a number of Log-domain circuits adopting a pseudo-differential structure have been designed exhibiting over 100dB DR in both simulations and measurements [157,205-206,226,231]. Although class-AB circuit design is an efficient approach to matching the requirements of good linearity and low power consumption, the problem with adopting the pseudo-differential approach for class-AB Log-domain filters is the increase in chip area required to accommodate the two capacitors per pole dictated by the pseudo-differential structure and the increase in complexity and matching effort during layout since the two class-A systems need to be identical.

Unlike the Log-domain circuits, the class-AB operation is inherent for Hyperbolic-Sine filters due to the odd symmetry of the sinh function at the heart of their companding operation. Therefore the output stage of Sinh filters allows for the processing of the integrating voltage at a single capacitor node as opposed to the need for two capacitors per pole in the case of class-AB Log-domain structures thus saving chip area and avoiding matching effort (so that the two sub-systems are identical).

[5] The splitting law can be geometric mean (GM) or harmonic mean (HM).

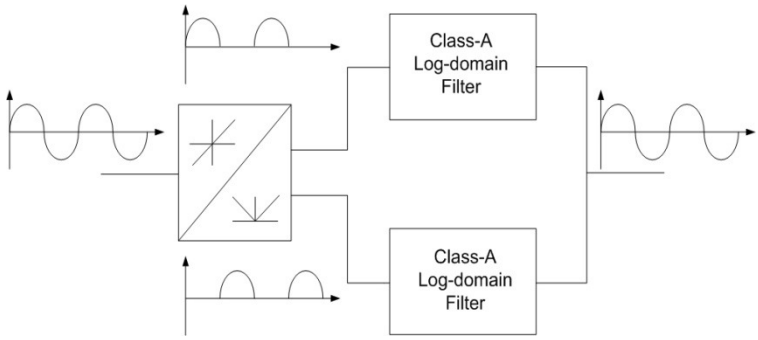


Figure 2.16: The concept of class-AB pseudo-differential Log-domain filters [157].

Although this was recognised early on [156,166,169,203] there has been low interest among the scientific community to exploit the Sinh design paradigm to date [154,157,169,207-211,227,229-230,244] when compared to an increasing rate of publications on Log-domain circuits of both practical and theoretical value [167,171,183,212-220] implemented with CMOS, Bipolar or BiCMOS technologies [203,221-225].

Although Frey realized in 1996 [169] the undoubted and proven through simulations advantageous performance of Sinh topologies with respect to high DR when compared to OTA-C and Log-domain structures as well as their additional advantage of only requiring one capacitor per pole while they operate in class-AB mode inherently, at the same time, he recognised the weakness of the Sinh filtering modality when compared to Log-domain topologies, due to the complexity of his proposed Sinh structures in [169] having followed his systematic methodology of ESS synthesis. He made a call in 1996 for further research on Sinh filters.

It took 9 years for experts in the area to translate Freys' Sinh bipolar designs into CMOS topologies operating in WI while the research on Log-domain filtering had already aken off upon recognition of its potential in achieving high DR in a low power regime (+100dB DR [160,226]). The first CMOS WI Sinh filters were published by Katsiamis and Drakakis in [227]. Biquads and 3rd order CMOS Sinh filters using Frey's synthesis method and building blocks were implemented in CMOS 0.35μm technology but the DR of those

topologies was not significantly better than class-A Log-domain filters (i.e. <75dB) as it was expected in theory [169].

Poort *et al*. [228], presented both simulated and measured results of a prototype Sinh integrator implemented with bipolar devices on a breadboard with reported DR of 73dB. Independently, Tsividis also recognised in [156] that Sinh filters which belong in the class of ELIN filters (as Log-domain filters do), have advantages over their Log-domain counterparts. He proposed a very elegant method by which a Sinh integrator could be synthesized based on the companding principle. Such a topology required different building blocks to the ones needed to implement a Sinh integrator by Frey's synthesis approach. He did not however propose any transistor level design at that time. Others [174,211] have also proposed synthesis methods for high order Sinh filters but their methods have not resulted in any radical improvement in terms of complexity than the designs firstly proposed by Frey neither have they been applied in designing CMOS topologies.

In 2006 two research groups [154,209], almost in parallel, published CMOS Sinh integrators based on Tsividis's general ELIN design approach [156]. Although both integrators have been designed based on companding methods, the integrator in [209] exhibits lower DR (75dB) and has not been further investigated ever since. The work presented in [154], on the other hand, achieved +120dB of DR and has been followed up with studies of both theoretical [157,230,244] and practical value [229]. Moreover the authors in [207] present an ELIN harmonic mean companding Sinh integrator while biquadratic Sinh filters have been proposed in [230]. This Thesis further confirms the practical potential of the Sinh filtering modality by means of silicon characterisation of high order CMOS Sinh filters based on the practical CMOS Sinh integrator proposed in [154]. The following Chapter will elaborate on the proposed in integrator [154] in more detail. Figure 2.17 summarizes its head-to-head comparison with a pseudo-differential Log-domain counterpart (Figure 2.19). It can

be observed that as long as an increase of 100nW/pole can be tolerated by the systems power budget, the Sinh integrator offers significant capacitor area reduction with its DR and SNDR remaining comparable to the Log topology (see Figure 2.18).

Topology	*Sinh*	Log
Power Consumption [μW]	0.2	0.09
Total Capacitance [pF]	20	40
Voltage Supply (V_{DD}) [V]	±1	±0.5
Simulated Pole Frequency (ω_o) [Hz]	2233	2290
Deviation from nominal ω_o, for n = 1.35	1.8%	0.6%
Input-referred Noise Floor [pA]	12.3	10
Maximum modulation index @ $(1/3)\omega_o$	4950	3000
Input DR @ $(1/3)\omega_o$ (THD = 4%) [dB]	132	129
$IMD_{2,3}$ @ m = 1000 [dBc]	–50; –50	–50; –52
SNR @ $(1/5)\omega_o$ [dB]	62 for m > 10	62 for m > 10
SNDR @ $(1/5)\omega_o$ [dB]	46 @ m = 1000	38 @ m = 1000

Figure 2.17: Comparison results of the CMOS Sinh integrator in [157] with a pseudo-differential class-AB Log-domain integrator.

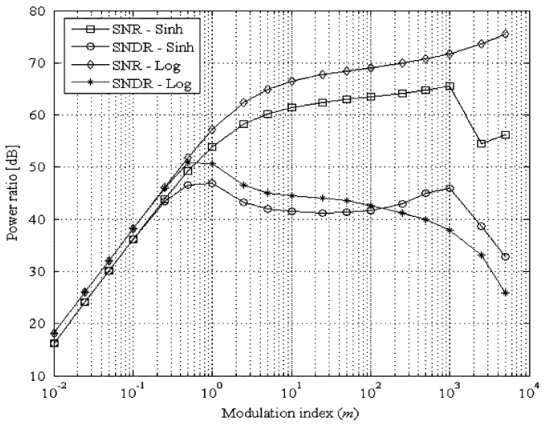


Figure 2.18: SNR and SNDR versus modulation index for both the Sinh and Log integrators in [157].

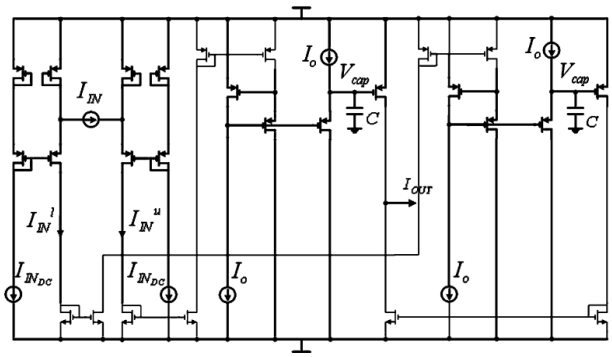


Figure 2.19: The pseudo-differential class-AB Log-domain integrator compared against the proposed Sinh integrator in [157].

2.5 Conclusion

Although, ELIN filters have the potential for unprecedented advantages over traditional filtering methods to the systems that employ them, little interest has been dedicated towards the evaluation of their suitability for specific low-frequency biomedical applications [231-232]]. For example, notch filters for 50/60 Hz elimination are typically still based on off-chip twin-T implementations or on switched capacitor filters which require additional anti-aliasing filters when an IC solution is sought for (see Chapter 1). In [235], the

presented notch filter is suitable for integration on-chip but it lacks ability for electronic tuning. Other groups have put effort in designing universal biquads (with low pass, high pass, band pass and notch outputs) based on current conveyors [236,237], Log-domain structures [223] or current feedback opamps [238] but most of the applications are dedicated towards processing at high frequencies [239] and the focus is the universal character of the filter. Therefore no extensive simulated or measured performance is presented for the notch output. Some of the few on-chip systems for ECG measurement [240-242], rely on G_m-C or SC low pass filters and no explicit mention of power line interference elimination technique is reported although it is necessary [243]. The reason for that is often the limited power budget or the lack of die space.

Sinh filters seem to outperform their conventional linearized counterparts and to at least match the performance of their Log-domain ELIN pseudo-differential class-AB counterparts (Figure 2.18, [157]) while needing only half the capacitor area to operate in class-AB. Therefore, high order CMOS Sinh topologies dedicated towards the low-audio frequency biomedical systems described in Chapter 1 will be assessed in the following Chapters. The novel topologies presented here are based on the practical integrator proposed in [154] which benefits from the additional feature of only comprising p-type of devices in its TL loops thus favouring its implementation in twin-well processes. The details of its implementation are covered in the following Chapter.

3 Synthesis, implementation and analysis of CMOS Sinh integrators

This Chapter details the synthesis and hardware implementation of Sinh lossy and lossless integrators in CMOS technologies. Firstly, the two main and fundamentally equivalent approaches [156,169] that can be employed in the synthesis of Sinh integrators are presented and compared with respect to the topologies resulting when mapping the mathematical equations from each one into circuit components. It progresses with the CMOS hardware implementation and analysis of Sinh lossy integrators. The transistor-level implementation of the presently reported CMOS Sinh integrator topologies is thoroughly explained and alternative implementations are discussed. The practical integrator reported in [154] -which employs only one type of devices in its TL loops- is the building block of the high order Sinh topologies presented in the following Chapters of this Thesis due to its ultra high DR which has not been matched by any other CMOS (and bipolar) Sinh integrator topology proposed to date. The most important findings of the study [154,157,207,229-230,244] of the aforementioned CMOS Sinh integrator are summarized here in order to explain the optimisation of the device sizes and circuit parameters of the high order Sinh topologies presented in the following Chapters. Moreover, a comparison is provided between the integrator in [154] and that in [209], -the only other CMOS Sinh integrator that has been derived by means of the ELIN companding synthesis approach [156]-.

3.1 Synthesis of Sinh integrators

As discussed in Chapter two, there are two main approaches that lead to the systematic synthesis of Sinh integrators a) the Exponential-State-Space (ESS) mapping method theoritized by Frey in [169] and the Externally-Linear-Internally-Non-Linear (ELIN) companding method formulated by Tsividis in [156,245,256].

According to the ESS method, a nonlinear mapping is imposed upon the state-variables (x_i) of a linear state-space description. This mapping is of the form $x_i = I_o \sinh(\alpha V_i)$ with V_i denoting an integrating node voltage, while I_o being a parameter with units of current and a being an implementation and technology dependent constant with units of volts^{-1}. The result of this sinh mapping is a set of nonlinear KCL relations which define the capacitor currents that need to be forced to the integrating nodes of the original linear topology described by a state-space, in order to obtain a Hyperbolic-Sine equivalent topology. The external linearity between the input and output currents, is ensured by a sinh^{-1} compression of the input current to an internal voltage node followed by integration at the capacitor node (as described by the derived non-linear capacitor current) and by a sinh expansion of the capacitor voltage to an output current. On the other hand, according to the ELIN companding synthesis approach, the necessary and sufficient conditions that must be satisfied by the pre-distortion (compressive) and output (sinh expanding) blocks of a companding integrator are revealed, such that a linear input-output relationship is preserved without any requirement placed on the input current.

Both approaches rely on the concept of translinear principle for analysis, synthesis and hardware implementation. Although this Chapter deals mainly with the synthesis of lossy Sinh integrators through the aforementioned methodologies [156,169] that presently have given rise to practical and realisable CMOS Sinh topologies [154,207,209,227-228] other approaches have also been proposed for the synthesis of Sinh filters [174,211,246-247]. A

more thorough review of the systematic approaches for the Sinh filter synthesis is the objective of Chapter 4 under the perspective of the synthesis of high order Sinh filters. The synthesis of a lossy Sinh integrator of the state-space description codified by equations (3.1) and (3.2) will be demonstrated here based on both the ESS and the ELIN approaches.

$$\dot{x}_1 = -\omega_o x_1 + \omega_o I_{IN} \tag{3.1}$$

$$I_{OUT} = x_1 \tag{3.2}$$

3.1.1 **Exponential-State-Space (ESS) synthesis**

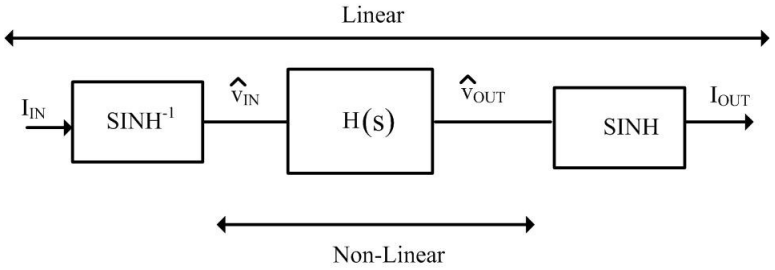


Figure 3.1: Conceptual block diagram of the ESS synthesis method [169] for Sinh filters. The linearity between the input and output of the integrator can be maintained due to the complementary operators SINH and $SINH^{-1}$ applied to the output and input respectively of the original linear filter core.

Step 1: Apply the sinh mapping on the original state-space variables such that the linear state-variables I_{IN}, I_{OUT} map to the nonlinear state variables V_{IN}, V_1 according to equations (3.3) and (3.4) respectively where a has units of V^{-1}.

$$x_1 = I_{OUT} = I_o \sinh(aV_1) \Rightarrow V_1 = \frac{1}{\alpha}\sinh^{-1}(I_{OUT} / I_o) \tag{3.3}$$

$$I_{IN} = I_o \sinh(aV_{IN}) \Leftrightarrow V_{IN} = \frac{1}{a}\sinh^{-1}\left(\frac{I_{IN}}{I_o}\right) \tag{3.4}$$

This step defines the input-compressive/output-expansive laws for realizing a *Sinh* companding system. More specifically, the linear input current variable I_{IN} is $\sinh^{-1}$-

compressed to an intermediate nonlinear input voltage variable V_{IN} and the nonlinear internal variable V_1, is sinh-expanded to the linear output current variable I_{OUT}.

Step 2: Substitute equations (3.3) and (3.4) into equation (3.1) to obtain the transformed nonlinear state-space description of the 1st-order lossy integrator:

$$\dot{V}_1 = -\frac{\omega_o}{a}\tanh(aV_1) + \frac{\omega_o}{a}\frac{\sinh(aV_{IN})}{\cosh(aV_1)} \tag{3.5}$$

Step 3: Multiply both sides of equation (3.5) with a constant parameter C, set $I_o = C\omega_o/a$ and rearrange using hyperbolic identities[6] to obtain the transformed nonlinear state-space:

$$C\dot{V}_1 = I_o\{-1+\cosh[a(V_{IN}-V_1)]\}\tanh(aV_1) + I_o\sinh[a(V_{IN}-V_1)] \tag{3.6}$$

If the parameters C and V_1 have dimensions of farads and volts respectively, then the term $C\mathrm{d}V_1/\mathrm{d}t$ (on the LHS) can be considered as the current flowing through a grounded capacitor. Moreover, if the parameter a, has dimensions of volts^{-1}, then $I_o = C\omega_o/a$ can be viewed as a dc current term that for a given C value, controls the pole frequency of the integrator resulting in an electronically-programmable frequency response. Lastly, the terms of the form $I_o \times f[a(V_i - V_j)]$ in equation (3.6) can be considered as currents generated from specific nonlinear transconductors that exhibit sinh-, cosh- and tanh-dependence upon the differential internal node voltage $V_i - V_j$. Figure 3.2 depicts the complete block diagram of the Sinh lossy integrator described by equations (3.1), (3.2) by means of this method. The reader can verify that in order to obtain a lossless ($\mathrm{d}x_1/\mathrm{d}t = \omega_o I_{IN}$) Sinh integrator, the only

[6] A useful identity is:

$$\frac{\sinh(aV_i)}{\cosh(aV_j)} = \cosh[a(V_i - V_j)]\tanh(aV_j) + \sinh[a(V_i - V_j)]$$

modification to the block diagram of Figure 3.2, is the omission of the dc current I_o from the tail of the T-cell in order to implement equation (3.7) instead of (3.6).

$$C\dot{V}_1 = I_o\{\cosh[a(V_{IN} - V_1)]\}\tanh(aV_1) + I_o \sinh[a(V_{IN} - V_1)] \tag{3.7}$$

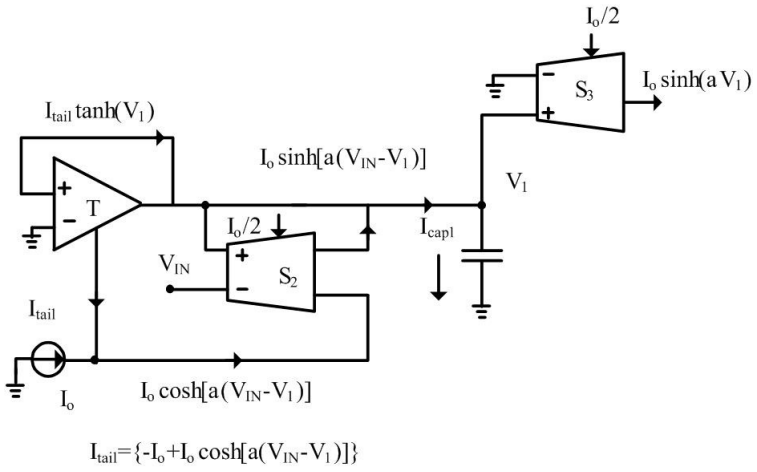


Figure 3.2: Block diagram of the Sinh lossy integrator described by equations (3.1) and (3.2) using Frey's synthesis method [169]. I_{IN} is $\sinh^{-1}$-compressed to the nonlinear input voltage V_{IN} through an additional S_1 transconductor which is not depicted here. The T-cell together with the S_2-cell, generate the currents that define the nonlinear capacitor voltage V_1. The output current is generated by applying V_1 to S_3.

3.1.2 **Externally-Linear-Internally-Non-Linear (ELIN) companding synthesis**

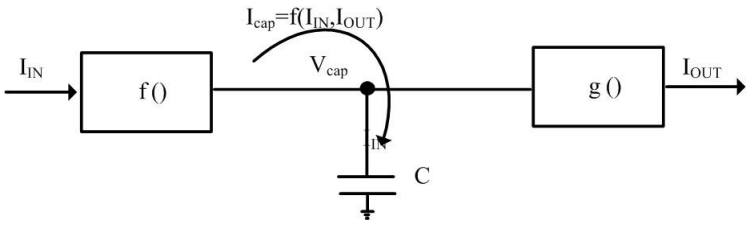


Figure 3.3: Generic block diagram of a companding integrator; the *f*() block plays the role of signal compressor, whereas the *g()* block acts as signal expander upon the integrating voltage V_{cap}. The input and output signals are considered to be currents with the capacitor current $I_{cap} = f(I_{IN,}\ I_{OUT})$ and the output current $I_{OUT} = g(V_{cap})$. Note the difference of the companding block diagram with that of Figure 3.1. Unlike in the block diagram of Figure 3.1, *f()*, the compressive function, does not need to be the inverse of *g()*.

Step 1: Start from the linear time-domain description of a current-mode lossy integrator as described in equation (3.8) with $\omega_{oj(j=1,2)}$ having dimensions of rads/sec. Referring to Figure 3.3 and by applying the chain rule, the time derivative of the output current is given by equation (3.9).

$$\dot{I}_{OUT} = \omega_{o1} I_{IN} - \omega_{o2} I_{OUT} \tag{3.8}$$

$$\dot{I}_{OUT} = \frac{dI_{OUT}}{dV_{cap}} \times \frac{dV_{cap}}{dt} = \frac{dg(V_{cap})}{dV_{cap}} \times \frac{f(I_{IN})}{C} \tag{3.9}$$

Step 2: Set the condition for the expanding block *g()* (see Figure 3.3) according to equation (3.10) with I_{DC} denoting an auxiliary biasing current and with the quantity *a* being a constant with dimensions of volts^{-1}.

$$I_{OUT} = g(V_{cap}) = I_{DC} \sinh(aV_{cap}) \Rightarrow \frac{dg(V_{cap})}{dV_{cap}} = aI_{DC} \cosh(aV_{cap}) \tag{3.10}$$

Step 3: Find the necessary and sufficient condition satisfied by the pre-distortion block *f*() such that input-output linearity of the block diagram of Figure 3.3 is preserved. This condition is found by combining equations (3.8)–(3.10). Equation (3.11) represents the linearization condition which needs to be implemented in real-time so that an ELIN Sinh lossy integrator is realized.

$$f(I_{IN}) = \frac{(\omega_{o1}C/a)I_{IN}}{I_{DC}\cosh(aV_{cap})} - \frac{(\omega_{o2}C/a)I_{OUT}}{I_{DC}\cosh(aV_{cap})} \tag{3.11}$$

Step 4: Obtain the closed-form expression of the capacitor current by making the following reasonable assumption for the input current (3.12): and where $I_{IN}{}^{U,L}>0$[7]. This assumption is necessary in order to ensure the class-AB operation of the topology at the input. Given the inherent class-AB property of the output which is sinh expanded it holds $I_{OUT}{}^{U,L}>0$ while the expression for the output current is codified by equation (3.13). The symbols*:* $I_{IN}{}^{U}$, $I_{IN}{}^{L}$ and $I_{OUT}{}^{U}$, $I_{OUT}{}^{L}$ in equations (3.12) and (3.13), denote the 'upper' and 'lower' split phases of the input and output bi-directional current waveforms.

$$I_{IN} = I_{IN}{}^{U} - I_{IN}{}^{L} \tag{3.12}$$

$$I_{OUT} = \underbrace{\frac{I_{DC}}{2}\exp(aV_{cap})}_{I_{OUT}{}^{U}} - \underbrace{\frac{I_{DC}}{2}\exp(-aV_{cap})}_{I_{OUT}{}^{L}} \tag{3.13}$$

Setting $I_{o1} = C\omega_{o1}/a$ and $I_{o2} = C\omega_{o2}/a$ and substituting equations (3.12) and (3.13) in (3.11), the following non-linear capacitor current expression is obtained:

[7] The condition for the class-AB operation at the input ($I_{IN}{}^{U,L}>0$) is ensured by a rule (e.g. geometric mean law or harmonic mean law) applied to the input current in order to condition it such that it's two phases remain strictly positive at all times ($I_{IN}{}^{U,L}>0$).

$$I_{cap} = \underbrace{\frac{I_{o1}\left({I_{IN}}^{U} + \frac{I_{o2}}{I_{o1}} {I_{OUT}}^{L} \right)}{I_{DC}\cosh(aV_{cap})}}_{I_{cap1}} - \underbrace{\frac{I_{o1}\left({I_{IN}}^{L} + \frac{I_{o2}}{I_{o1}} {I_{OUT}}^{U} \right)}{I_{DC}\cosh(aV_{cap})}}_{I_{cap2}} \tag{3.14}$$

Equation (3.14) codifies the expression of the linearizing capacitor current, for the synthesis of an ELIN lossy Sinh integrator. The damping factor which is associated with the lossy integrator, is realized by the presence of the terms $(I_{o2}/I_{o1})\times {I_{OUT}}^{L}$ and $(I_{o2}/I_{o1})\times {I_{OUT}}^{U}$. The absence of these terms would lead to a lossless integrator. By taking the Laplace transform of (3.8), the overall transfer function of the lossy Sinh integrator is obtained:

$$\frac{I_{OUT}(s)}{I_{IN}(s)} = \frac{\omega_{o1}}{s+\omega_{o2}} = \frac{aI_{o1}/C}{s+aI_{o2}/C} \tag{3.15}$$

From equation (3.15), the currents I_{o1} and I_{o2} control the dc gain of the frequency response, whereas the current I_{o2} alone controls the pole frequency of the integrator. The Sinh lossy integrator derived from this approach, can be implemented by means of three circuit blocks comprising, as illustrated in the block diagram of Figure 3.4: a) an input current splitter to realize (3.12) and ensure ${I_{IN}}^{U,L}>0$, b) a non-linear transconductor that yields currents of sinh/cosh-dependence upon the capacitor voltage V_{cap} as in (3.13) and c) two translinear loops to divide currents as dictated by equation (3.14).

Lastly, it should be noted that the terms $(I_{o2}/I_{o1})\times {I_{OUT}}^{L(,U)}$ that set the dc gain of the integrator can be realised by means of either an additional TL loop or a Sinh/Cosh transconductor whose biasing currents (I_{DC}) are scaled accordingly [157]. For the block diagram of Figure 3.4, the currents which control the dc gain of the integrator, have been set to the same value ($I_{o1}=I_{o2}=I_o$), resulting in unity dc gain.

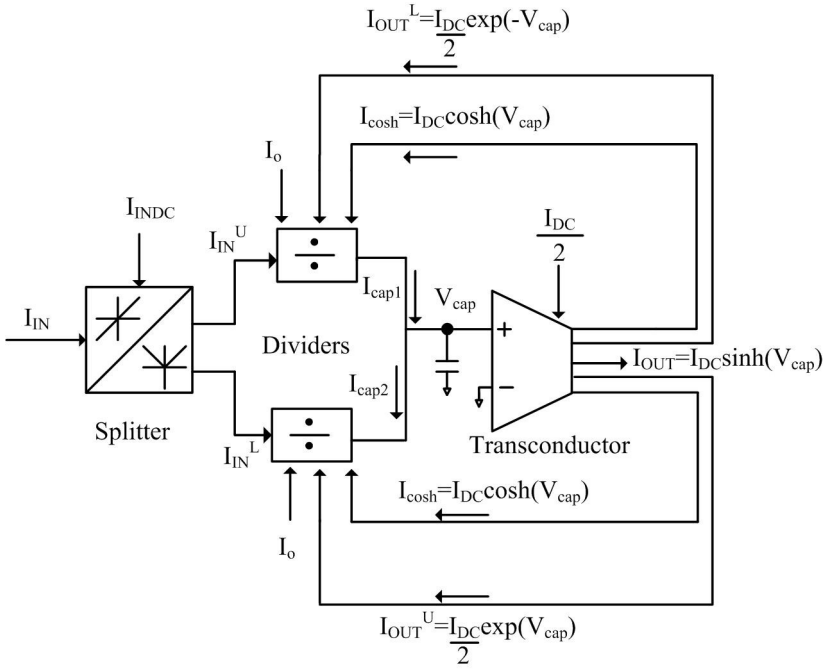


Figure 3.4: Block diagram of a Sinh lossy integrator derived by means of the ELIN companding synthesis method [156]. The sinh/cosh transconductor generates the nonlinear sinh/cosh currents. The dividers compute the upper (I_{cap1}) and lower (I_{cap2}) capacitor currents according to (3.14) which defines the compressed nonlinear capacitor voltage V_{cap}. Here, for unity dc gain $I_{o1}=I_{o2}=I_o$.

Variations of the ESS method have been reported in [211,246] while variations of the ELIN synthesis approach have been reported in [247]. The authors in [246] have proposed an approach similar to the complementary operators method proposed by Perry and Roberts for Log-domain filters synthesis in [171]. Although the complementary operators synthesis method presented in [246] is equivalent to the ESS method [169], the path of a direct implementation of equation (3.5) is explored instead of employing hyperbolic identities to bring it to the familiar from of equation (3.6). The direct implementation is illustrated for a lossless Sinh integrator in Figure 3.5. It can be verified that the block diagram of Figure 3.5 implements equation (3.16) and that it is identical to the block diagram of the Sinh companding integrator of Figure 3.4 derived from the synthesis approach in [156].

$$i_c = 2I_o i_{IN} / 2I_o \cosh(\hat{v}_{OUT} / nV_T) \tag{3.16}$$

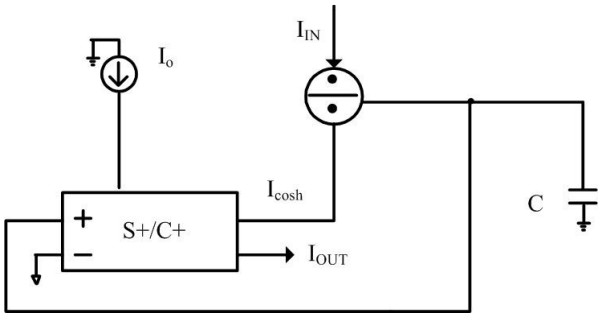


Figure 3.5 : Block diagram of a lossless Sinh integrator synthesized by means of the complementary operators method [246].The block diagram implements equation (3.16) instead of (3.7). Compare with the ELIN companding integrator in Figure 3.4.

3.1.3 **ELIN companding versus ESS synthesis**

Both the ESS [169] and ELIN companding [156] synthesis methods rely on the non-linear mapping of the original linear state-space by means of the hyperbolic sine function which lends its name to the filtering modality itself (Sinh filters) and which is also responsible for the inherent class-AB nature of all Sinh topologies. Despite this fundamental similarity, the two approaches begin to diverge at the point where the condition for the appropriate compression at the input is defined such that the linearity between input and output is maintained. This leads to a number of apparent topological differences between the block diagrams of Figure 3.2 and Figure 3.4 which have been derived by means of the ESS [169] (section 3.1.1) and the ELIN companding [156] (section 3.1.2) methods respectively.

The difference in the way with which the step of compression at the input is realized, leads to two mathematically different capacitor nodal equations (3.6), (3.14) and in turn results in differences in the way with which the lossy term appears. For example, the realisation of the ESS integrator of Figure 3.2 utilises four sinh/cosh transconductors whereas the ELIN integrator of Figure 3.4 only requires one sinh/cosh transconductor at the output. Having said that, the combined role of the three extra transconductors (S_1 -which is not illustrated in Figure 3.2-, S_2 and T-cells) present in the Sinh topology synthesized by means of the ESS approach [169], is matched by the two dividers and the input current splitter

required to implement the compressive condition which is expressed by means of a nonlinear capacitor current of appropriate form (3.14) when following Tsividis's methodology [156] as illustrated in the block diagram of Figure 3.4. This implies that in terms of transistor count both topologies would result in implementations averaging approximately the same number of devices.

Observing and comparing equation (3.6) and (3.14), the damping factor appears in the form of a dc current (I_o) for the integrator of Figure 3.2 as compared to the output current itself in the case of the ELIN integrator (see Figure 3.4). Moreover, the requirement for a T-cell to implement an ESS Sinh integrator, (i.e. a differential pair), imposes transistor-level restrictions to the type of S-cells that can be used. Due to the factor of ½ naturally appearing in the tanh argument of a differential pair implemented in CMOS WI, the S-cells need to be accordingly degenerated (check that the parameter a in (3.6) needs to be the same for all blocks i.e. T-cells and S-cells) resulting in increased power supply levels (~ $8V_T$). This makes also the level of compression weaker hence increasing the power consumption even more since larger biasing currents are needed to realise the same level of compression. In addition to that, the biasing of the T-cell by means of a non-linear tail current, although perfectly viable mathematically, it imposes difficulties to the optimisation of the topology which implements the block diagram of the ESS synthesis method [157] (Figure 3.2).

Moreover, the two topologies (Figure 3.2, Figure 3.4) adopt different class-AB structures due to the differences imposed by the compression step. Looking at Figure 3.6 i.e. the familiar conceptual diagram of a 1st order class-AB explicitly differential topology comprising two identical class-A systems "A" and "B" (e.g. class-A log-domain filters), it becomes obvious how the sinh output stage (or the sinh nonlinear mapping) allows for the merging of the systems A and B at a single output node as indicated in Figure 3.7. A direct consequence of that is the elimination of one capacitor as the design progresses from Figure

3.6 to Figure 3.7. For an equivalent relation between the input (u) and the output (y) for the two topologies, (Figure 3.6 and Figure 3.7) the input should be treated accordingly. A natural choice for that modification is the merging of the two inverse systems f^{-1}_A and f^{-1}_B at the input, into a single node which is essentially the $\sinh^{-1}$ function as depicted in Figure 3.8. Comparing the conceptual diagram of Figure 3.8 with the integrator realized having followed the ESS synthesis approach [169] (Figure 3.2), the equivalence of the two becomes apparent. A less obvious, but yet very elegant manipulation of the input, arises from avoiding its restriction in performing the inverse function of the expansive output. The path that this choice leads to is conceptually illustrated in Figure 3.9. Comparing Figure 3.9 with Figure 3.8, one can notice that the f^{-1} has been substituted by a division with a non-linear current which is essentially the derivative of the output current with respect to the output voltage (See Step 3 in 3.1.2). Notice the similarity of the conceptual block diagram of Figure 3.9 with the integrator realized having followed Tsividis's ELIN companding approach [156] (Figure 3.4). Unlike the case of the Sinh integrator arising from ESS method [169] an input current splitter is central to the realisation of the topology by means of Tsividis's ELIN approach [156]. The main role that the current splitter fulfils is to condition the input signal, in such a way to maintain the class-AB mode of operation of the overall filter. Although the sinh trasnconductor is a class-AB structure, the topology which implements the division of the input current with the appropriate non-linear current is typically a class-A topology (i.e. a stacked or alternating TL loop). It is therefore necessary that the collector currents flowing through the transistors of the divider remain strictly positive. In order to have a class-AB divider, the pseudo-differential structure should be adopted for the input (Figure 3.6). This is implemented by means of a current splitter which conditions the input signal into two strictly positive phases which are in turn fed into a class-A divider each. The class-AB capacitor current (3.14) is formed by subtracting the two outputs from each divider. The use of a

current splitter is not required in the class-AB structure of Figure 3.8 since the $\sinh^{-1}$ function is inherently able due to its odd symmetry to process both positive and negative input currents which merge into a $\sinh^{-1}$ internal voltage node.

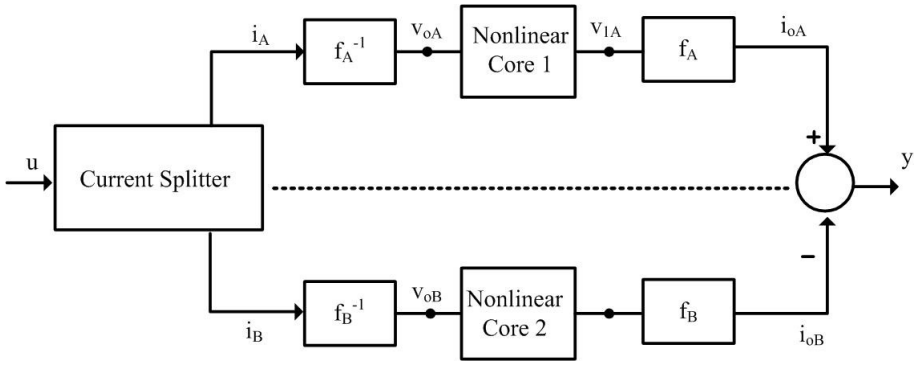


Figure 3.6: Explicitly differential class-AB structure: It can be verified that the illustrated structure represents a class-AB pseudo-differential 1st order log-domain filter if each of the non-linear cores is substituted by a capacitor and the function *f* by the exponential function.

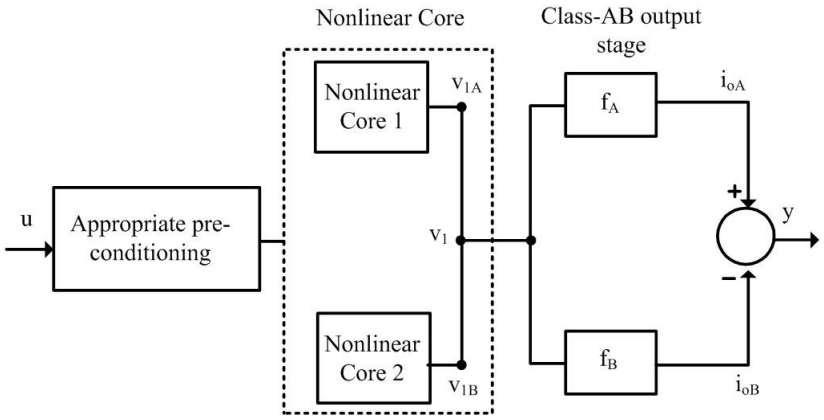


Figure 3.7: Externally equivalent class-AB structure with that of Figure 3.6. Here the output class-AB stage allows for the two non-linear cores to merge into a single node (v_1). Upon the correct choice of the input pre-conditioning the equivalence of the two systems is ensured. The merging of the non linear cores 1, 2 (e.g. into a single capacitor) is permitted for non-linear mappings of odd symmetry such as sinh. The need for the two identical systems A, B of the previous case is not present in this implementation.

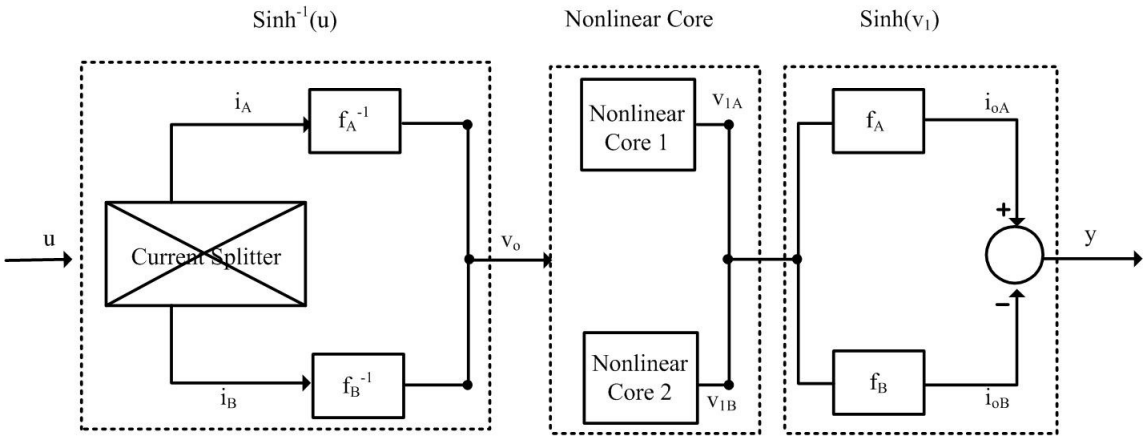


Figure 3.8: Block diagram illustrating the class-AB structure of a Sinh integrator having followed the ESS synthesis method [169]. The sinh^{-1} function allows for the merging of f_A^{-1}, f_B^{-1} into a single block which implements a sinh^{-1} operation and the current splitter at the input is no longer required.

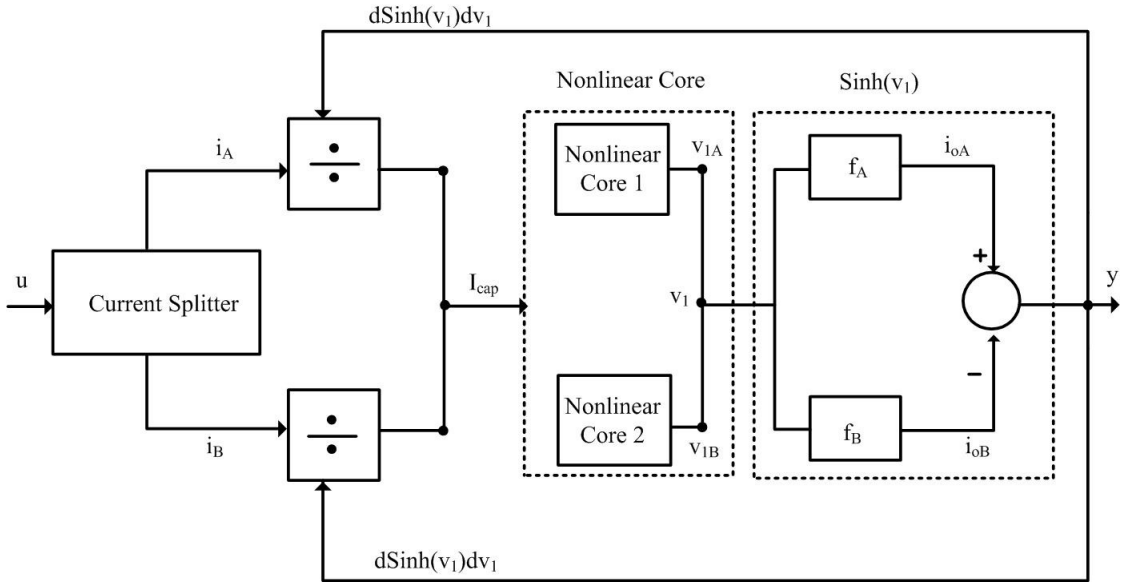


Figure 3.9: Block diagram illustrating the class-AB structure of a Sinh integrator having followed the ELIN companding synthesis method. Note except from the input stage, the structure is exactly the same as that of Figure 3.8 resulting from ESS synthesis method [169]. However, the input arrangement differs from that of Figure 3.8 and necessitates a current splitter to ensure that two positive input currents are fed into the pseudo-differential class-AB structure of the dividers which provide the capacitor current according to (3.14).

Comparing the conceptual diagrams of Figure 3.8 and Figure 3.9, it becomes apparent, that the input is decoupled from the rest of the topology and that the signal phases of the bidirectional input current are freely available to be used in the topology of Figure 3.9 thus leading to further design freedom when compared to a non-linear input voltage being accessible instead in the topology of Figure 3.8. The constraint for the input *I-V* conversion by means of the sinh^{-1} function on the other hand, limits the flexibility over the transistor

level-implementation of the integrator designed by means of the ESS method [169]. The transconductors used to implement the block diagram of Figure 3.2 will need to have zero offsets in order to ensure that the $\sinh^{-1}$ *I-V* conversion is accurate. Otherwise, an offset in the voltage V_{IN} would translate into dc offset terms for the S-cells S_2 and S_3 (see Figure 3.2). For this reason, all of the Sinh topologies reported to date [209,211,227,246], with the exception of the integrators in [154,207] utilize S-cells comprising both type of devices in their TL loops in a symmetric about ground arrangement. Moreover note that although the integrator presented in [209] is synthesized also by means of the ELIN approach, it has been implemented based on complementary devices (see section 3.2.3).

The source of the topological differences between the block diagrams of Sinh integrators by means of the two compared methodologies can be summarized as follows: In the ESS method, the design effort is placed on the mapped voltages all of which must be meaningful and should correspond to a circuit node in the topology: *The input current must be converted to a non-linear voltage which is in turn processed and consequently expanded to obtain linearity by means of the exact inverse function.* On the other hand, the ELIN companding method leads to a true current mode design where all the design emphasis and effort revolves around currents: *The linear input current is compressed by means of a non-linear current of the form* $I_{DC}cosh(aV_{cap})$*, giving rise to an appropriate form of capacitor non-linear current such that the output remains linear with the input.*

3.2 CMOS implementation of Sinh integrators

Frey reported the first transistor level, bipolar implementation of Sinh topologies derived from his ESS method [169]. The first CMOS implementation of Sinh filters is reported by Katsiamis and Drakakis nine years later [227] and arises from direct mapping of Frey's original building blocks in the 0.35μm CMOS technology. One year later and almost in parallel, Haddad and Serdjin in [209] and Katsiamis *et al*. in [154] proposed more practical CMOS Sinh topologies derived from the ELIN companding synthesis method [156]. The latter topology, in addition to its elegance in the synthesis approach, comprises only PMOS devices in its translinear loops and remains to date the only practical CMOS Sinh integrator which has extensively been simulated [154,157], fabricated and tested [229].

On the other hand, the topology in [209] constitutes the CMOS version of the sinh/cosh transconductors that have been originally proposed by Frey in [169]. Following these early implementations of Sinh integrators, Glaros *et al*. in [207] proposed a Harmonic Mean (HM) Sinh integrator which relies on a harmonic mean (HM) splitter and sinh/cosh transconductor instead of a Geometric Mean (GM) one as utilized in [154]. Finally, Kasimis and Psychalinos in [246], have proposed CMOS Sinh integrators based on the ESS synthesis method realized with both p- and n- type devices in the TL loops. Table 4 summarizes the CMOS Sinh integrators that have been proposed to date. The details of their implementation, is discussed in the following sections.

Table 4: CMOS implementations of Sinh integrator-topologies.

Author	[154]	[207]	[209]	[227]	[246]
Year	2007	2008	2006	2005	2011
Technology	0.35µm	0.35µm	0.35µm	0.35µm	0.35µm
Synthesis method	ELIN	ELIN	ELIN	ESS indirect[a]	ESS direct[b] indirect[a]
Current splitter transconductor	GM	HM	GM	GM	GM
Realisation details	All-PMOS	All-PMOS	Comple-mentary devices	Comple-mentary devices	Comple-mentary devices

a Refers to the implementation of (3.6) after using hyperbolic identities.

b Refers to the implementation of (3.7) directly.

3.2.1 An ELIN all-PMOS geometric mean Sinh companding integrator

This section presents the detailed transistor level implementation of the Sinh integrator presented in [154]. Its block diagram and transistor-level design is illustrated in Figure 3.12 detailing the transistor level implementation of a) a current splitter based on Geometric Mean Law, b) two class-A translinear loops functioning as dividers and c) a sinh/cosh transconductor which naturally adheres to the Geometric Mean Law. NMOS and PMOS current mirrors direct the currents to the required locations in the circuit. For the biasing of the individual blocks, three dc current sources are required namely I_{DC}, I_{INDC} and I_{bias} while I_o is the current by which the frequency response of the integrator is electronically tuned for a given capacitor value.

The input current splitter, illustrated in Figure 3.10, separates the input current signal I_{IN} into two strictly positive (unidirectional) currents $I_{IN}{}^{U}$ and $I_{IN}{}^{L}$ according to the GML (3.17) as confirmed by the TL loops of the splitter in Figure 3.10. The nature of the synthesis method [156] allows the decoupling of the input current splitter from the rest of the circuit. Thus any other splitter could be used as long as it ensures that the bi-directional input current is separated into two positive phases (180 degrees apart).

$$I_{IN}{}^{U} \times I_{IN}{}^{L} = (I_{IN_{DC}})^2 \tag{3.17}$$

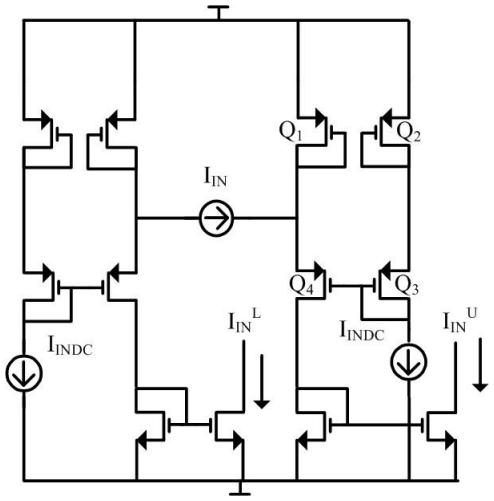


Figure 3.10: Transistor-level implementation of a fully differential GM current splitter [154].

The all-PMOS S-cell (sinh/cosh transconductor) depicted in Figure 3.11, comprises two p-type only E-cells (Q_1-Q_2 and Q_3-Q_4) which sense the input voltage V_{cap}. Their output currents are of the form of (3.18), (3.19) and their combined action results in the cosh (3.20) or sinh (3.21) output currents where $\alpha=1/nV_T$, n denoting the sub-threshold slope parameter and ($V_T=kT/q$) representing the thermal voltage. The exponential expressions for $I_{OUT}{}^{L}$ and $I_{OUT}{}^{U}$ can be confirmed upon applying KVL around the closed loop formed between V_{cap} and ground and containing devices Q_1-Q_2 and Q_3-Q_4 respectively. Moreover, from the alternating TL loop formed by devices Q_1-Q_4, equation (3.22) holds which indicates that the topology naturally adheres to the Geometric Mean Law.

$$I_{OUT}{}^{L} = \frac{I_{DC}}{2}\exp\left(-aV_{cap}\right) \tag{3.18}$$

$$I_{OUT}{}^{U} = \frac{I_{DC}}{2}\exp\left(+aV_{cap}\right) \tag{3.19}$$

$$I_{OUT} = I_{OUT}{}^{U} - I_{OUT}{}^{L} = I_{DC}\sinh(aV_{cap}) \tag{3.20}$$

$$I_{OUT}{}^{U} + I_{OUT}{}^{L} = I_{DC}\cosh(aV_{cap}) \tag{3.21}$$

$$I_{OUT}{}^{U} \times I_{OUT}{}^{L} = \frac{I_{DC}^2}{4} \tag{3.22}$$

The input of the transconductor is the voltage V_{cap} (high input impedance node), applied at the gates of Q_1, Q_3 whereas the gates of the devices Q_2, Q_4 are connected to ground. Q_2, Q_3 are biased by constant dc current sources ($I_{DC}/2$). The outputs of this topology are the currents I_{OUT} (upper and lower) at the drain terminals of Q_1, Q_4. These two currents, upon subtraction, form the bidirectional output current which has a sinh dependence on the input voltage V_{cap} according to equation (3.20) or a cosh dependence (3.21) upon addition. An important feature of this topology is its vertical symmetry. Looking at just the left half of this topology (Figure 3.11), device Q_7 serves as a level shifter which indirectly lowers the impedance at the drain of Q_2 so that Q_2 can be properly biased. The gate-source (V_{gs}) voltage of Q_7 is set by a dc current (I_{bias}) and in turn it sets the V_{gs} of Q_5 which is the "tail" of the E-cell.

The two translinear loops depicted in Figure 3.12 (and Figure 3.13) generate the two phases I_{cap1} and I_{cap2} of the total capacitor current I_{cap} according to equation (3.14). Based on (3.14) it can be verified that the differential equation governing the relation between the input and the output current has as follows:

$$\dot{I}_{OUT} = \frac{dI_{OUT}}{dt} = \frac{dI_{OUT}}{dV_{cap}} \times \frac{dV_{cap}}{dt} = aI_{DC}\cosh(aV_{cap}) \times \frac{I_{cap}}{C} = \left(\frac{aI_0}{C}\right)\left(I_{IN} - I_{OUT}\right) \tag{3.23}$$

Setting $\omega_o = aI_o/C$ rad/sec and applying the Laplace transform yields (3.24) which codifies the transfer function of an input-output linear lossy integrator with a dc-gain of unity and whose pole frequency is tuneable by means of the dc-current I_o.

$$\frac{I_{OUT}(s)}{I_{IN}(s)} = \frac{\omega_0}{s+\omega_0} \tag{3.24}$$

Based on the above it can be deduced that the topology of Figure 3.12 corresponds to an ELIN Sinh integrator which exhibits the desired property of incorporating MOS transistors of one type (p-type) in the signal processing path. This ensures the feasibility of implementing the proposed integrator in standard twin-well CMOS processes without sacrificing the logarithmic conformity since the V_{BS} voltages of at least one type of devices could be set to zero.

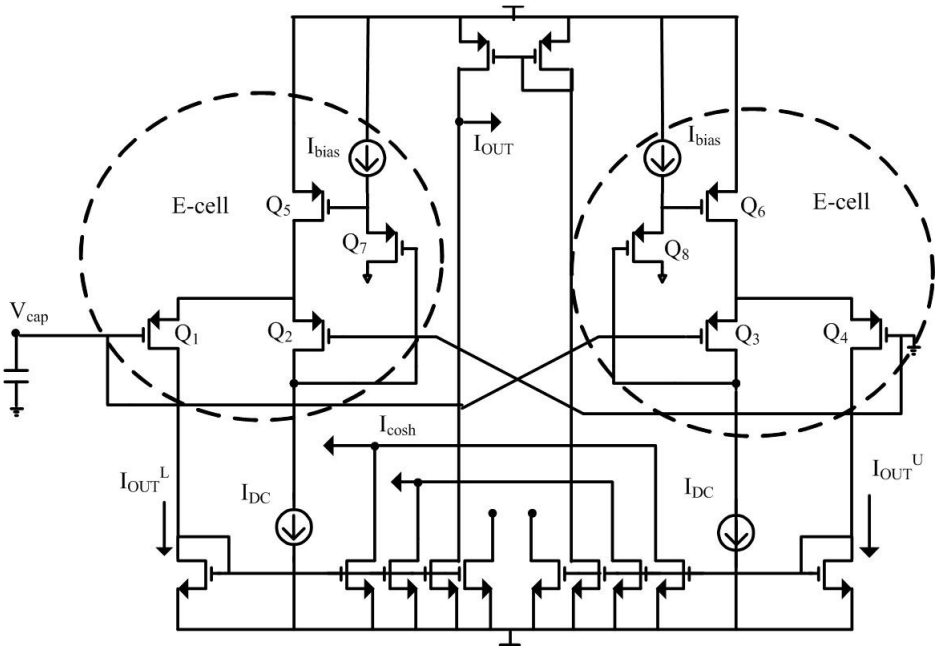


Figure 3.11: Transistor-level implementation of the all-PMOS Sinh transconductor in [154]. The currents I_{cosh} refer to the cosine output current. It can be verified that the TL loop (Q_1-Q_4) of the topology adheres to the GML. The topology implements equations (3.18)-(3.22).

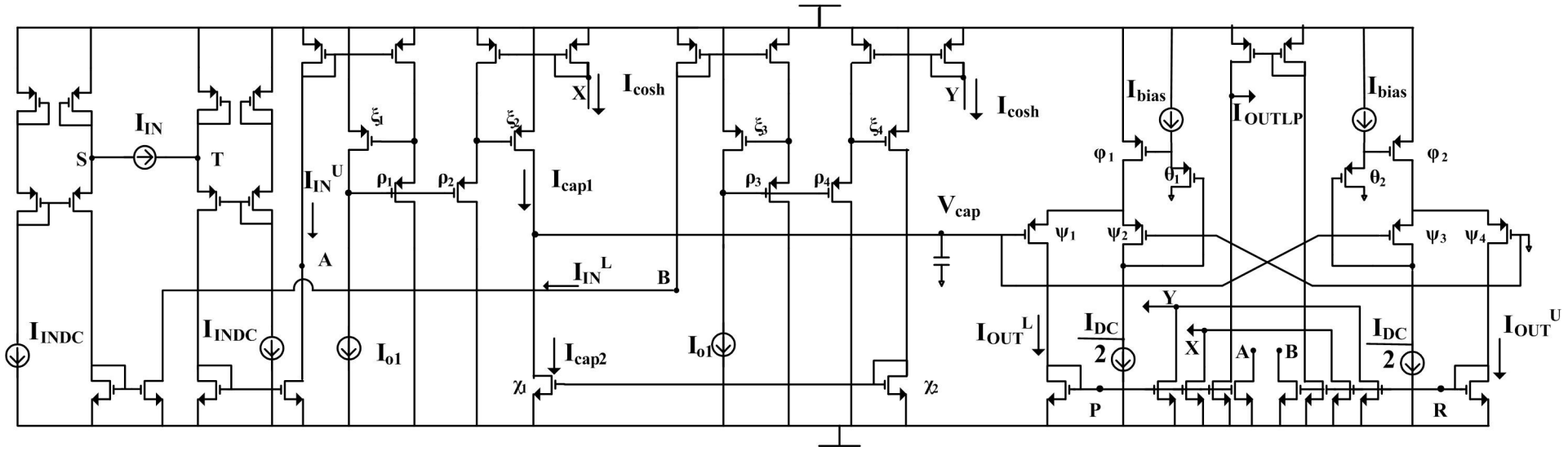


Figure 3.12: The complete transistor-level schematic of the all-PMOS class-AB Sinh ELIN companding lossy integrator based on GML [154]. This topology is the building block used in the design and fabrication of the high order Sinh topologies presented in this Thesis.

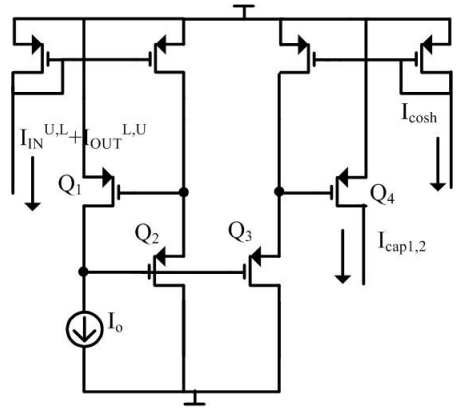


Figure 3.13: Transistor-level implementation of a multiplier/divider. Note that this is a class-A topology and only positive currents can flow at the collector terminals of the devices forming the TL loop. Two dividers are used in a pseudo-differential class-AB arrangement in order to implement equation (3.14). Check the complete transistor-level topology of the Sinh integrator [154] (Figure 3.12).

3.2.2 An ELIN all-PMOS harmonic mean Sinh companding integrator

The authors in [207] have implemented the block diagram of the ELIN CMOS Sinh lossy integrator (Figure 3.4) by means of an input current splitter and sinh/cosh transconductor, which adhere to the HML instead of the GML. HML ensures that the internal currents remain bounded to half the dc bias value for large inputs therefore theoretically leading to less cross-over distortion [207].

The HML based current splitter used in [207] is illustrated in Figure 3.14. It can be verified that the TL loops comprising devices Q_1-Q_4 and their symmetric devices, implement the HML codified by equations (3.25) and (3.26) with Q_1 (and its symmetric device as illustrated in Figure 3.14) having double the aspect ratio of the rest of the respective devices in the loop in order to implement the factor of two appearing at the RHS of (3.26).

$$I_{IN} = I_{IN}{}^{U} - I_{IN}{}^{L} \tag{3.25}$$

$$2I_{IN}{}^{U} I_{IN}{}^{L} = (I_{IN}{}^{U} + I_{IN}{}^{L}) I_{BIAS} \tag{3.26}$$

The topology of the HM transconductor is depicted in Figure 3.15. The TL loop comprising devices Q_1-Q_7, implements (3.27). This topology is highly asymmetric. A symmetric version of the HML transconductor of Figure 3.16 has been proposed in [230] which trades off symmetry for an increase in chip area and power consumption. The complexity of a HM transconductor itself introduces complexity which should be outweighed by an improved performance of the HM Sinh integrator in order to warrant its implementation practical and beneficial when compared to its GM counterpart [154]. The complete topology of the HM Sinh integrator in [207] is illustrated in Figure 3.17.

$$2I_{OUT}{}^{U} I_{OUT}{}^{L} = (I_{OUT}{}^{U} + I_{OUT}{}^{L}) I_{DC} \tag{3.27}$$

$$I_{OUT}{}^{U} = I_{OUT}{}^{L} \exp(V_{cap} / nV_T) \tag{3.28}$$

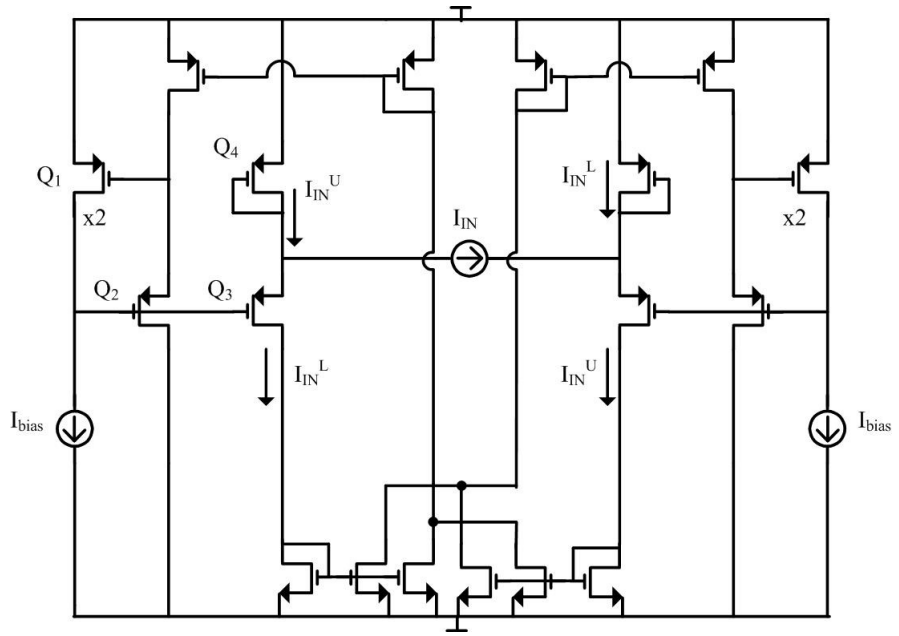


Figure 3.14: The HM current splitter proposed in [207]. The topology implements equations (3.25) and (3.26).

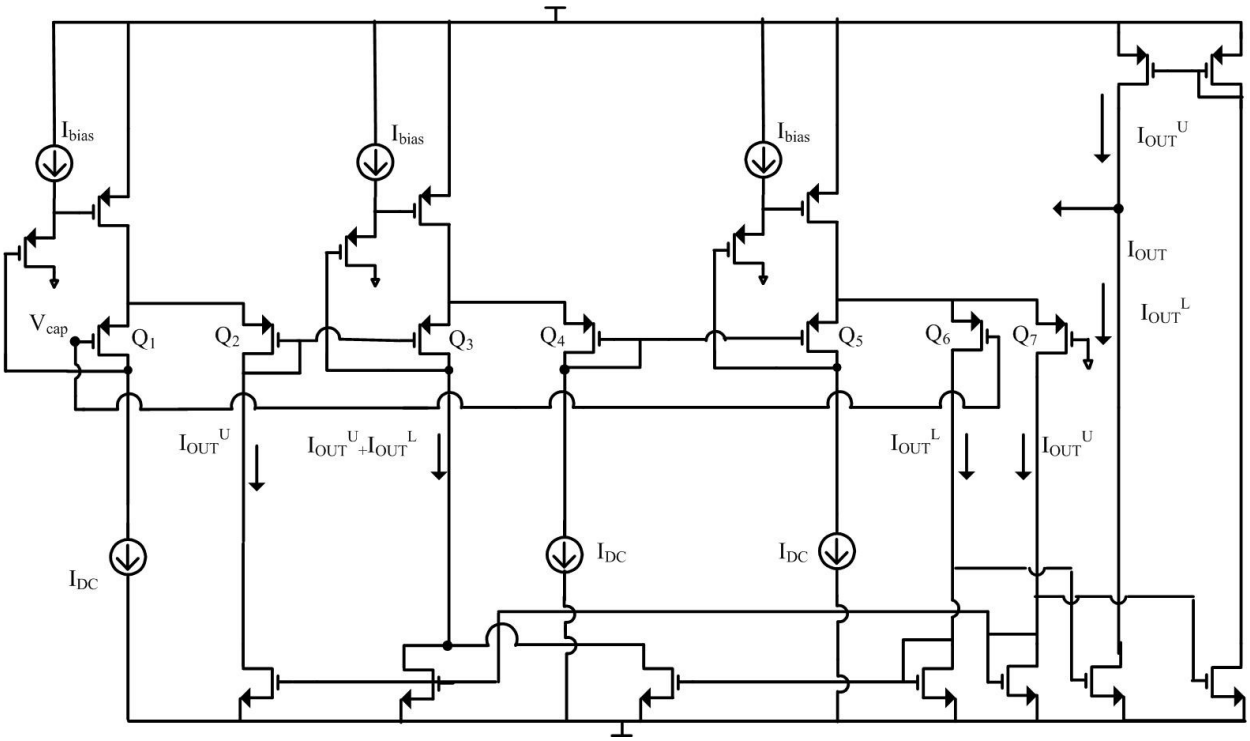


Figure 3.15: The HM transconductor in [207]. The topology implements (3.27), (3.28). Note that the addition of the two output phases, leads to $I_{DC}+I_{DC}\cosh(\alpha V_{cap})$. This implies that (3.14) needs to be modified to account for the additional dc term in the cosine current (see Figure 3.16) for the complete transistor level implementations of the HM Sinh integrator in [207].

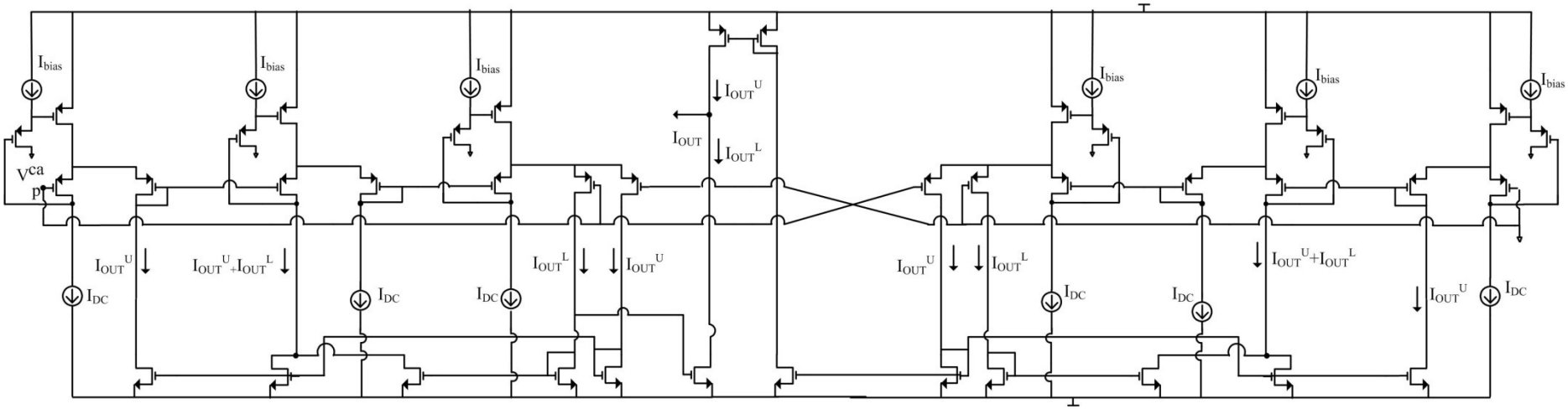


Figure 3.16: A symmetric version of the HM transconductor in Figure 3.15 [207,230].

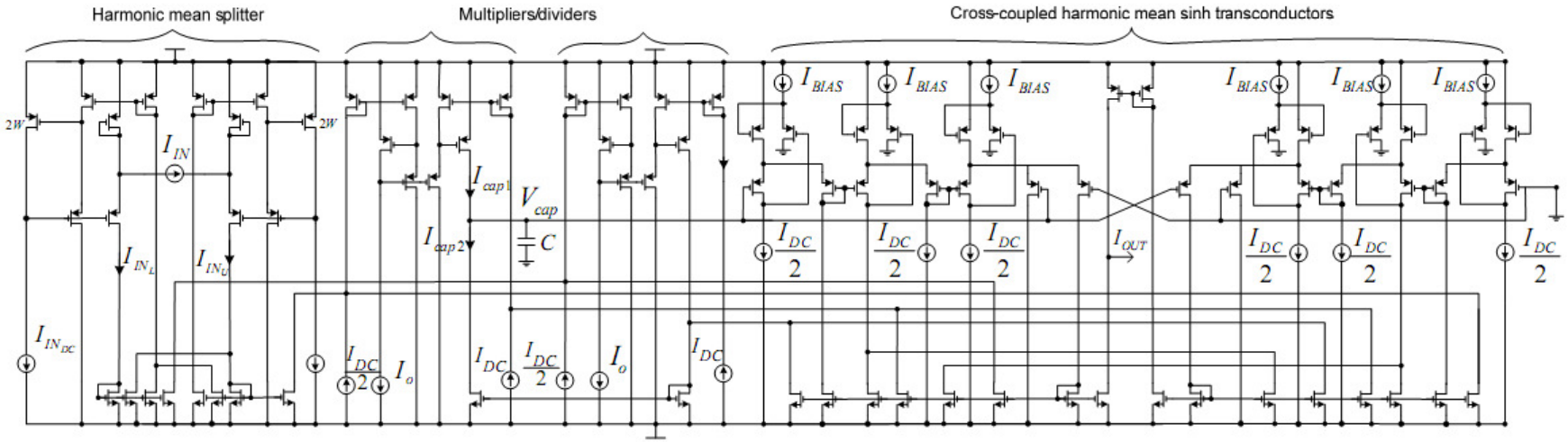


Figure 3.17: Transistor-level schematic of an all-PMOS HM companding Sinh integrator [230].

3.2.3 An ELIN CMOS geometric mean Sinh companding integrator

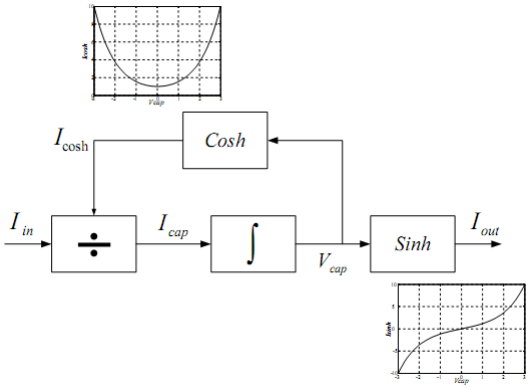


Figure 3.18 : Block diagram of an ELIN companding lossless Sinh integrator [248].

Another topology which implements the Sinh companding block of a lossless integrator (see Figure 3.18), has been reported in [209,249] and is illustrated in Figure 3.19. The input current splitter, conditions the input current in two strictly positive phases I_{IN}^{U}, I_{IN}^{L} according to the GML. Unlike the current splitter of the integrator in [154] (see Figure 3.10, Section 3.2.1) the topology of the input current splitter used in [209] (see Figure 3.19), is based on complementary CMOS devices. Moreover, the latter is a single ended splitter as compared to the differential splitter utilized for the implementation of the integrator in [154]. The trasconductor is also based on complementary devices. One obvious choice for the implementation of the capacitor current is to employ stacked TL loops of p- and n- type, in order to handle the upper and lower phase of the input respectively as illustrated in Figure 3.19. The TL loop formed by the PMOS devices Q_{5A}-Q_{8A}, handles the positive phase of the input current while the TL loop comprising the NMOS devices Q_{5B}-$Q_{8B,}$ the negative phase of the input current. The TL loops implementing the sinh/cosh transconductor (Q_9-Q_{12} Figure 3.19) comply with the GML and are identical with the TL loop implementing the current splitter (Q_1-Q_4). The current flowing through the capacitor of the integrator of Figure 3.19 is given by equation (3.29). In addition, from the DTL loop (Chapter 2), around the capacitor

and the devices of the output currents ($I_{OUT}^{U,L}$) the capacitor current can be related to the output currents according to equation (3.30). Substituting equation (3.30) into (3.29) leads to the linear differential equation of a lossless integrator (3.31). Note that similar to the implementation of the integrator in [154], adding a feedback of the output current phases to each of the input phases (of opposite polarity) would lead to the implementation of a lossy integrator.

$$I_{cap} = I_{8A} - I_{8B} = (I_{IN}^{U} - I_{IN}^{L}) I_o / I_{\cosh} \tag{3.29}$$

$$I_{cap} = nCV_T(\dot{I}_{OUT}) / (I_{OUT}^{U} + I_{OUT}^{L}) \tag{3.30}$$

$$I_{IN} I_o = nCV_T \dot{I}_{OUT} \tag{3.31}$$

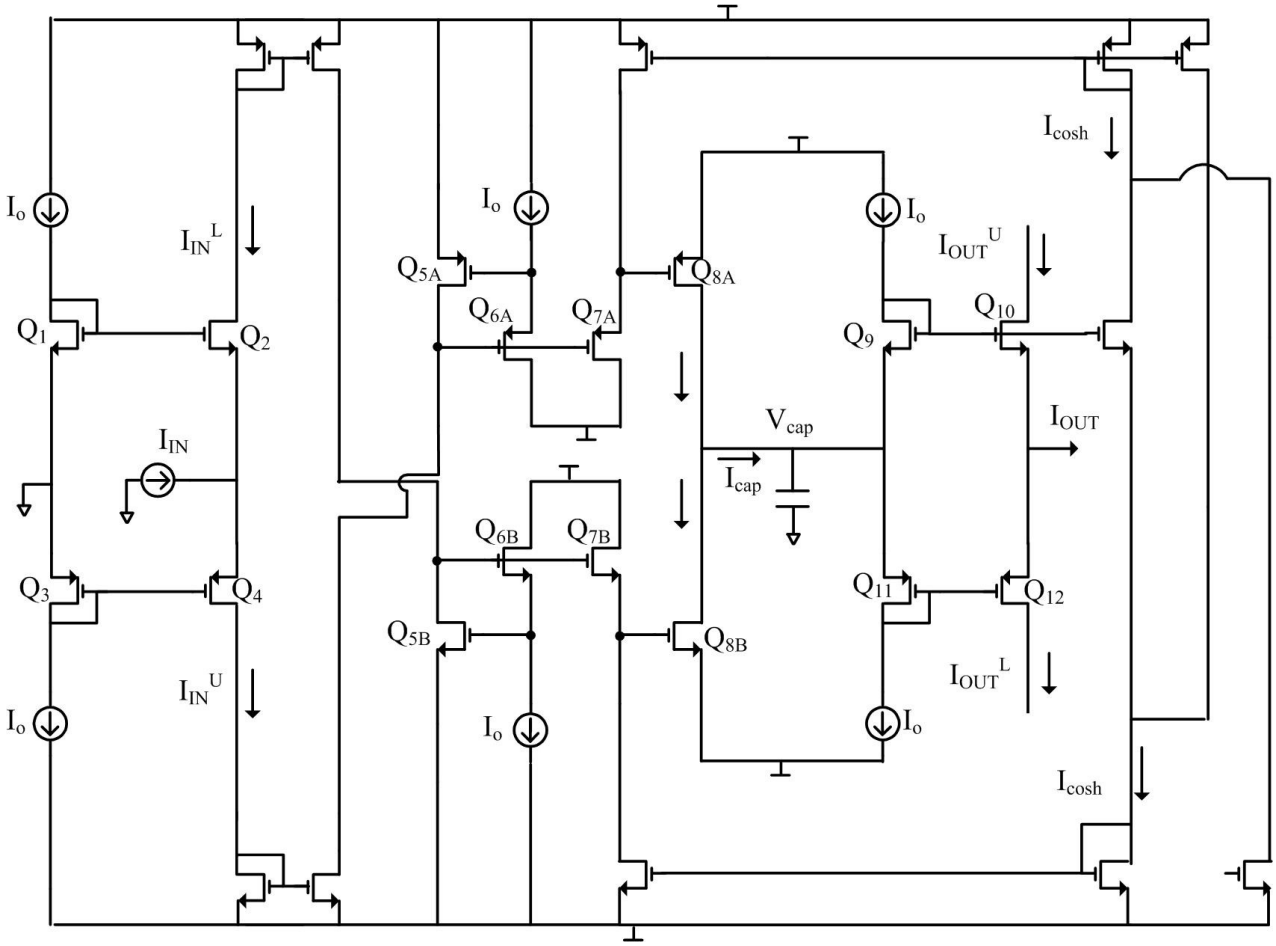


Figure 3.19: An obvious CMOS implementation choice of the Sinh companding block diagram of Figure 3.18 proposed in [249]. Note the similarity of this topology with the CMOS integrator in [154].

The CMOS Sinh integrator presented in [209], is in fact is a modified version of the integrator in Figure 3.19. The main difference lies in the implementation of the dividers in a way such that the divider blocks are also formed by the same TL loop as the input current splitter and the transconductor blocks (see Figure 3.20). The topology of Figure 3.20 comprises three sinh transconductors which are formed by TL loops $Q_{1\text{-}3}$, $Q_{5\text{-}8}$, $Q_{9\text{-}12}$. Note that the input current splitter is not decoupled from the rest of the topology anymore (unlike the integrator of Figure 3.19). In order for this modification to take place while the capacitor equations which ensure linearity still hold, it should be verified that the combined action of the two TL loops of the dividers in the topology of Figure 3.19, is now performed by the sinh/cosh transconductor comprising devices Q_5-Q_8 in Figure 3.20 (3.29). Bearing in mind equations (3.29) and (3.32) and solving for I_{Q5} in the global TL loop formed by devices Q_1,Q_2,Q_5,Q_8,Q_9,Q_{10}, it follows that I_{Q5} should be equal to $I_o I_{dc}/I_{cosh}$. Similarly from the global TL loop formed by devices, Q_3,Q_4,Q_6,Q_7,Q_{11},Q_{12} and considering (3.29) and (3.32), I_{Q6} is found to be equal to $I_o I_{dc}/I_{cosh}$. Substituting the DTL equations from the loops C-Q_9-Q_{10} and C-Q_{11}-Q_{12}, into the capacitor current equation (I_{Q8}-I_{Q7}), a linear lossless integrating function is implemented. In order to obtain a lossy integrator, negative feedback from the output to the input is necessary. The complete transistor implementation of the Sinh integrator proposed in [209] is illustrated in Figure 3.21. The additional transistors $Q_{5A,B}$ and $Q_{8A,B}$ (indicated in red in Figure 3.21), are added in order for the global TL loops to compute the correct capacitor currents at the collector terminals of Q_8, Q_7 as codified by (3.29).

$$I_{IN}{}^{U} I_{IN}{}^{L} = I_{OUT}{}^{U} I_{OUT}{}^{L} = I_{dc}{}^{2} \tag{3.32}$$

$$I_{Q8} = I_o I_{IN}{}^{L} / I_{\cosh} \tag{3.33}$$

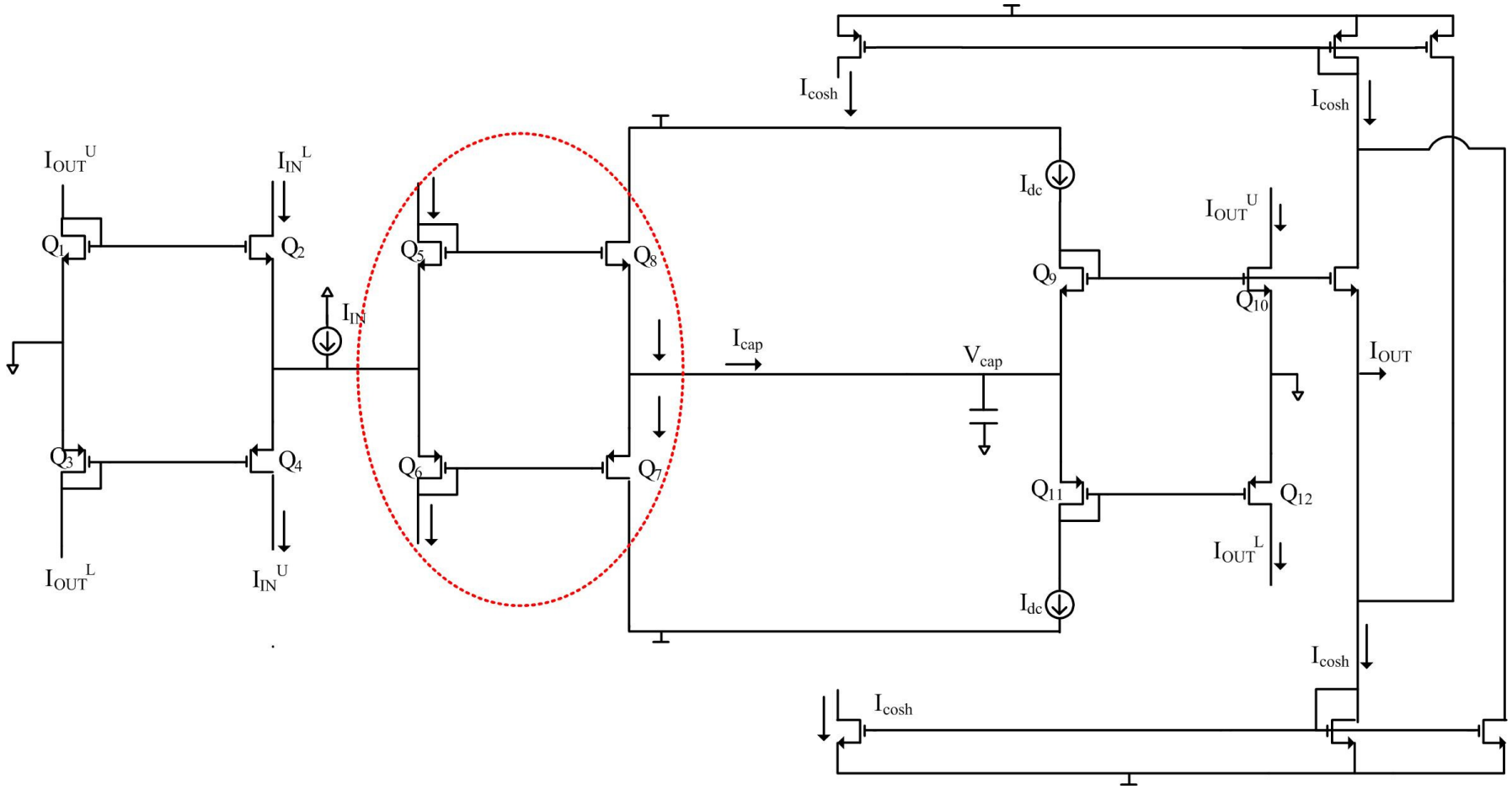


Figure 3.20: Transistor-level topology of the block diagram of Figure 3.18 where the dividers are implemented by the TL loop comprising devices Q_5-Q_8 (circled). Note that unlike the topology of Figure 3.19, the capacitor is charged and discharged at the source of devices Q_8, Q_7. The current splitter is not decoupled any more from the rest of the filter (contrary to the integrator in Figure 3.19 or to the integrator in [154]). In addition, the splitter is not biased directly by dc currents. Instead the upper and lower phases of the output are used to bias the input current splitter.

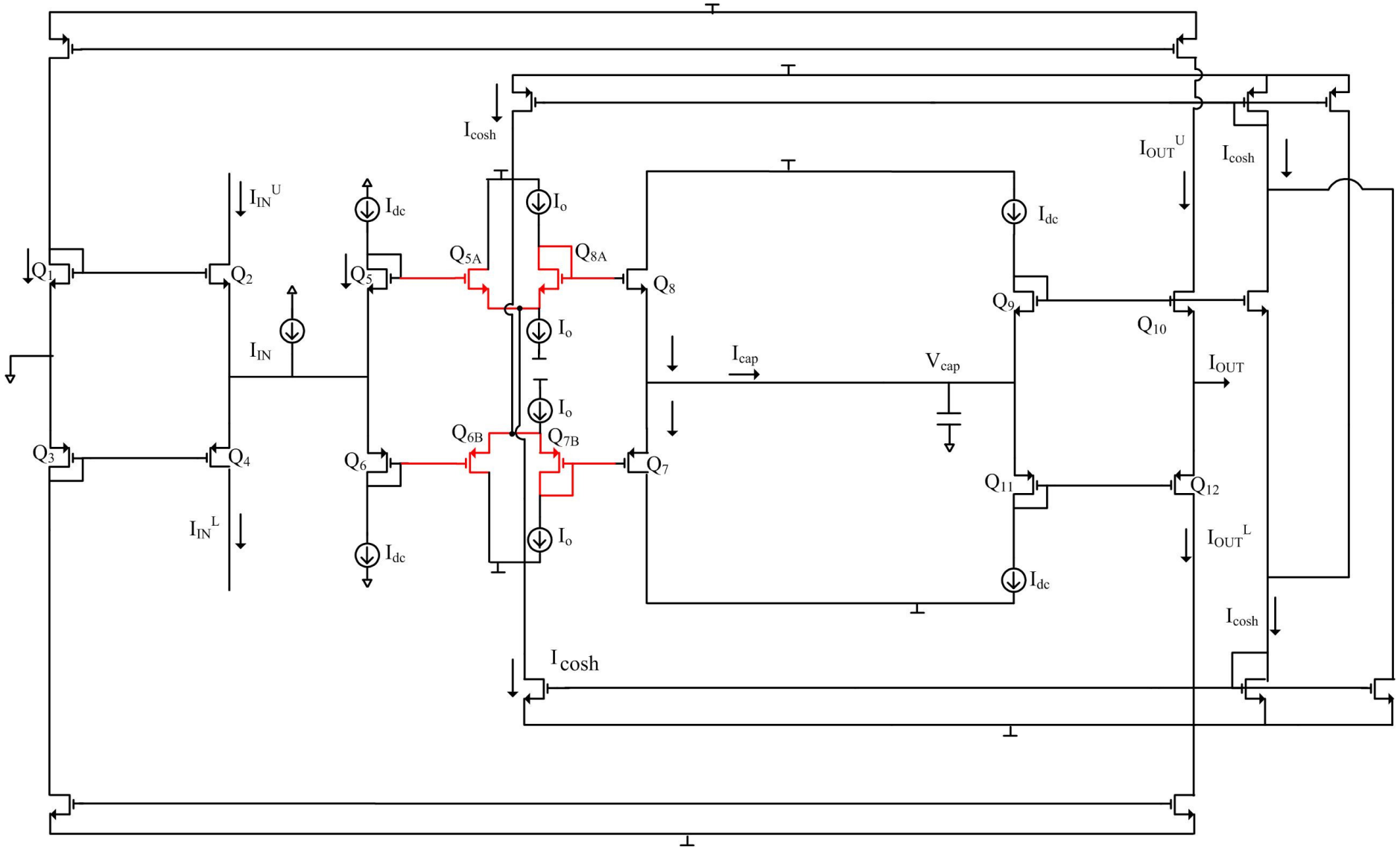


Figure 3.21: Transistor-level topology of the Sinh companding integrator in [209].

3.2.4 **CMOS Sinh integrators based on ESS synthesis**

Frey demonstrated in 1996 the first Sinh topologies in bipolar technology arising from his ESS synthesis approach [169]. His so called S- and T- cells are non-linear transconductor blocks which exhibit the desired hyperbolic sine/cosine and tangentential *I-V* relationships respectively which implement equation (3.6) (see Figure 3.1).

The authors in [227], were the first to suggest CMOS WI Sinh topologies derived from the ESS method and based on the original S- (see its CMOS version in Figure 3.22) and T-cells (Figure 3.23) proposed by Frey in [169]. Figure 3.24 illustrates the CMOS S-cell utilized for the implementation of the Sinh topologies in [227]. It comprises two E-cells i.e. exponential transconductors termed E+ and E- cells and incorporates improved Wilson mirrors in order to increase the output impedance. Note that the *V*- terminal has been replicated so that it can be used as a low impedance terminal where the $\sinh^{-1}$ *I-V* conversion required at the input stage can take place. Addition of the respective outputs from the two E-cells, gives rise to the cosh output current whilst upon their subtraction, the sinh output current is formed.

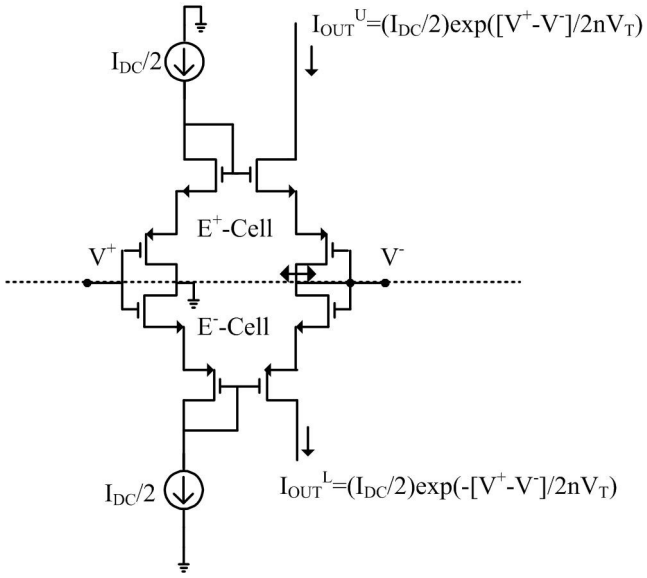


Figure 3.22: Frey's S-cell [169] implemented in CMOS. Note that V. terminal can be used as a low impedance point whereby the input current gets converted to a non-linear voltage node by means of $\sinh^{-1}$. Moreover observe the horizontal symmetry of the topology which ensures theoretically no offsets for zero input current. In the absence of the gate–drain connection of the devices forming V- terminal, both input voltage terminals can be used to sample a differential input voltage.

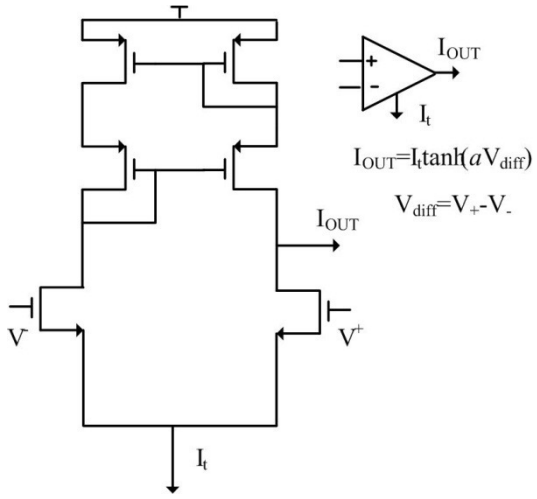


Figure 3.23: The CMOS differential pair (T-cell) used in [227] for the implementation of the CMOS ESS Sinh integrator. Note that $a=1/2nV_T$.

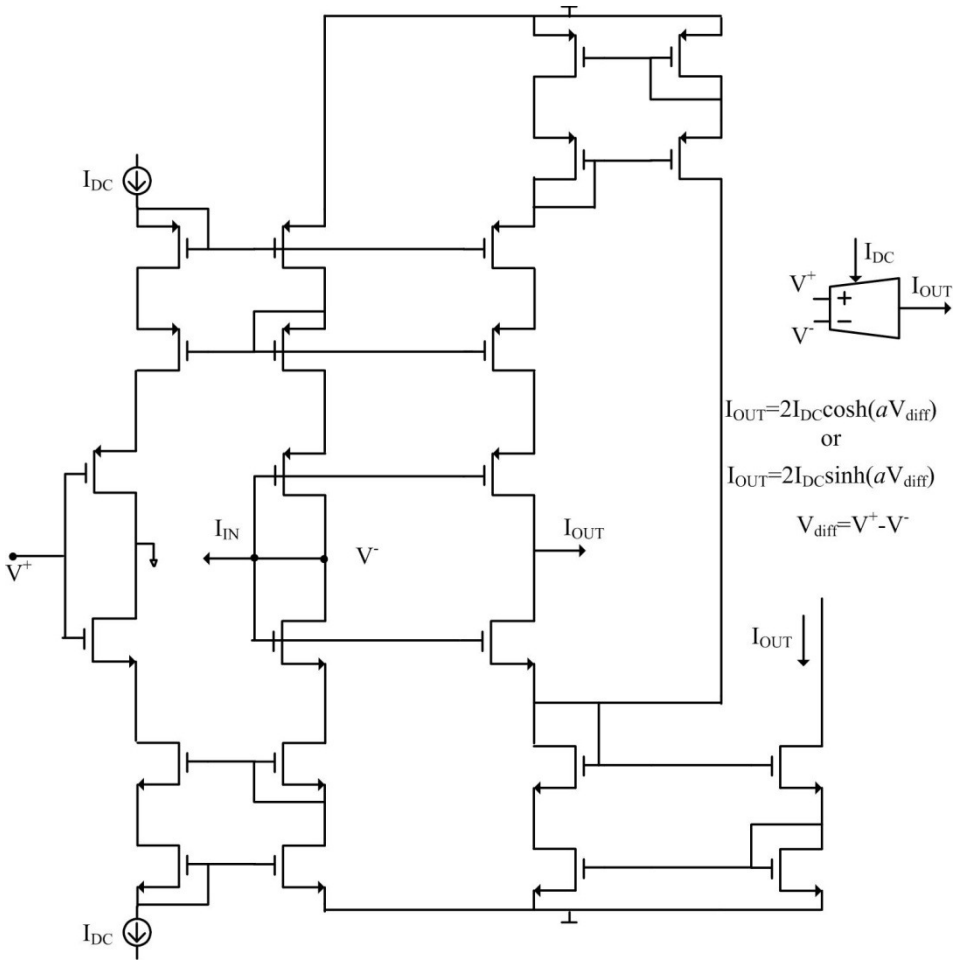


Figure 3.24: The CMOS sinh/cosh transconductor (S-cell)/ $\sinh^{-1}$ *I-V* presented in [227] and originally proposed as a bipolar topology in [169]. Note that the S-cell in [169] has $a=2nV_T$ instead of $a=nV_T$ as in [209]. The degeneration of the devices of the S-cell is imposed by the need to include a T-cell in the capacitor equation (3.6) for the implementation of a Sinh integrator by means of the ESS method [169].

The authors in [146] have also implemented CMOS Sinh topologies based on complementary devices and derived from the ESS synthesis approach [169]. The S-cell used in [246] is formed by the same TL loops used to implement the current splitter and sinh/cosh transconductor in [209]. Unlike Frey's S-cells which are based on compound devises (see Figure 3.22) and therefore have their input voltage terminals secured at high impedance levels (i.e. gate terminals, see Figure 3.22), the S-cell presented in [209,246] (refer to Figure 3.20) has a high impedance positive terminal -assuming matched current sources- where an input voltage can be applied. Its negative terminal on the other hand, cannot be used to apply a voltage (Figure 3.25).

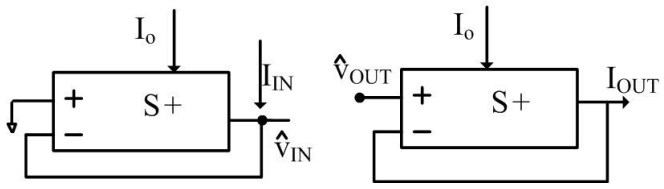


Figure 3.25: The realisation of $SINH^{-1}$ and SINH operators [246]. Compare with Figure 3.1.

A differential S-cell has been proposed in [246] and is illustrated in Figure 3.26. The drawback of this implementation is that it relies entirely on the matching of current mirrors in order to cancel out the current -by adding currents of opposite direction- at the terminal where the voltage v_{IN2} is applied (see Figure 3.26).

The lossless Sinh integrator of Figure 3.5 which directly implements equation (3.16) derived by means of the ESS method, is presented in [246] and employs the S-cell depicted in Figure 3.26 and two quadrant dividers (see Figure 3.27). The S-cell with its positive terminal grounded, is used at the input as a current splitter (see Figure 3.25). Note the similarity of the implemented topology with the lossy integrator presented in Figure 3.19.

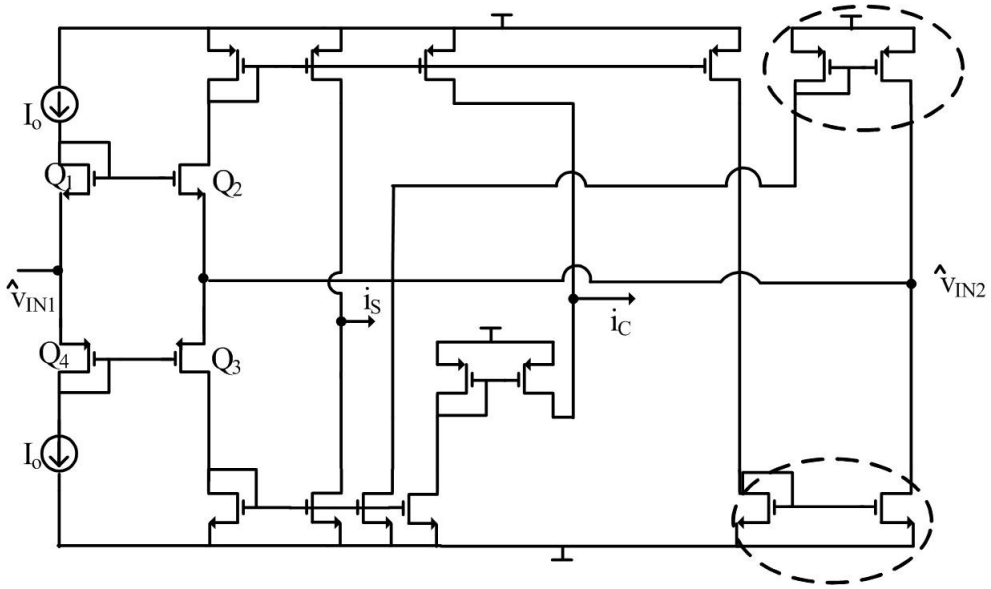


Figure 3.26: Differential input sinh/cosh transconductor. Note that in order to create a high impedance node at v_{IN2}, the circled current mirrors need to be perfectly matched [246].

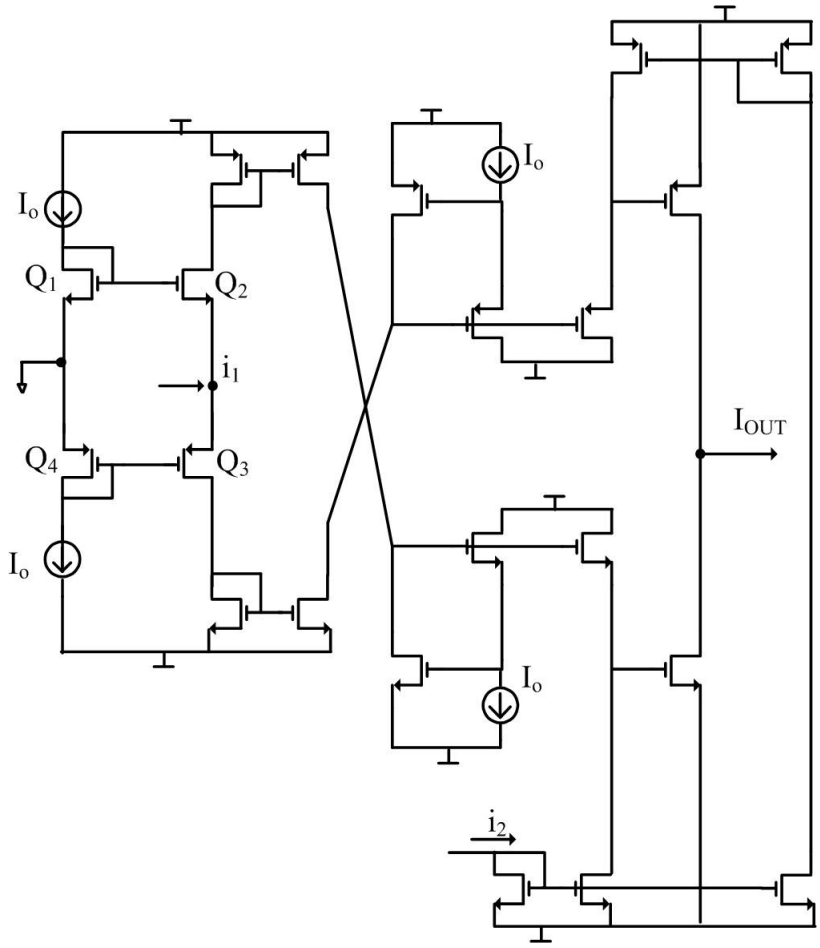


Figure 3.27: Two quadrant multiplier [246].

3.3 Analysis of Sinh integrators

This section deals with the analysis of CMOS Sinh integrators based on Static Translinear (STL) and Dynamic Translinear (DTL) Principles as originally proposed in [249]. Topologies that have been derived by both the ESS and the Companding synthesis methods are analyzed here in order to further examine the details of their transistor-level implementation.

Figure 3.28, illustrates the transistor-level implementation of the ESS Sinh integrator (see Figure 3.2) based on Frey's compound E-cells [169] (Figure 3.22). Five STL loops can be identified: Q_1-Q_4, Q_5-Q_8, Q_{12}-Q_{14}, Q_1,Q_2,Q_5,Q_6,Q_{11},Q_{12} and Q_9,Q_{10},Q_{11},Q_{12},Q_{11},Q_{12} for which it holds respectively that:

$$I_{Q2}I_{Q3} = I_{Q4}I_{Q1} \Rightarrow {I_{IN}}^{U}{I_{IN}}^{L} = {I_{dc}}^{2}/4 \tag{3.34}$$

$$I_{Q6}I_{Q7} = I_{Q5}I_{Q8} \Rightarrow I_{p1}I_{p2} = {I_o}^{2}/4 \tag{3.35}$$

$$I_{Q12}I_{Q13} = I_{Q14}I_{Q11} \Rightarrow {I_{OUT}}^{U}{I_{OUT}}^{L} = {I_{dc}}^{2}/4 \tag{3.36}$$

$$I_{Q2}I_{Q6}I_{Q12} = I_{Q1}I_{Q5}I_{Q11} \Rightarrow 8{I_{IN}}^{U}I_{p1}{I_{OUT}}^{U} = {I_{dc}}^{2}I_o \tag{3.37}$$

$$I_{Q10}I_{Q11}I_{Q11} = I_{Q9}I_{Q12}I_{Q12} \Rightarrow I_{10}{I_{dc}}^{2} = 4I_9({I_{OUT}}^{U})^2 \tag{3.38}$$

Moreover from the DTL principle around the loop formed by C-Q_{11}-Q_{12}, it holds that:

$$I_{cap} = 2nCV_T\frac{\dot{I}_{OUT}{}^{U}}{I_{OUT}{}^{U}} \tag{3.39}$$

From equations (3.40), (3.41), the currents I_9 and I_{10} in the differential pair, can be respectively expressed as follows in (3.42) and (3.43).

[8]The authors in [249] S. A. P. Haddad and W. A. Serdijn, "Ultra Low-Power Biomedical System Designs," in *Ultra Low-Power Biomedical Signal Processing*: Springer, 2009, pp. 131-172.quote equation (3.37) with an extra factor of ¼ at the RHS. It can be verified that the correct Equation is as codified in (3.37).

$$I_{10} - I_9 = I_{cap} + I_{p2} - I_{p1} \tag{3.40}$$

$$I_{10} + I_9 = I_{p1} + I_{p2} - I_o \tag{3.41}$$

$$I_9 = I_{p1} - \frac{1}{2}(I_o + I_{cap}) \tag{3.42}$$

$$I_{10} = I_{p2} - \frac{1}{2}(I_o - I_{cap}) \tag{3.43}$$

The currents I_{p1}, I_{p2} can also be expressed by means of I_{IN}, $I_{OUT.}$ By using expressions (3.34)-(3.37) they can be expressed as codified by (3.44) and (3.45). Applying equations (3.44) and (3.45) to (3.42) and (3.43) and using (3.39), it can be verified that the topology of Figure 3.28, implements a linear lossy integrator as codified by (3.46).

$$I_{p1} = \frac{I_o {I_{dc}}^2}{8 {I_{IN}}^U {I_{OUT}}^U} \tag{3.44}$$

$$I_{p2} = \frac{I_o {I_{dc}}^2}{8 {I_{IN}}^L {I_{OUT}}^L} \tag{3.45}$$

$$I_{IN} = I_{OUT} + \frac{2CV_T}{I_o}\dot{I}_{OUT} \tag{3.46}$$

The authors in [249] prove that the Sinh topology of Figure 3.29 is also an implementation of a Sinh integrator which maps to the linear 1st order ODE (3.46). Unlike the topology in Figure 3.28, the TL loops implementing the individual blocks, are based on single devices instead of compound devises. In order for the topology of Figure 3.29 to codify (3.46), two additional devices (Q_{15}, Q_{16} , circled in Figure 3.29) need to be included in the topology of Figure 3.28 thus forming a STL loop comprising devices $Q_{15,}$ Q_{16}, $Q_{9,}$ $Q_{10,}$ Q_{11}, Q_{12} (Figure 3.29). This is necessary in order to implement (3.38). Following the same analysis steps as for the topology of Figure 3.28, it can be verified that both topologies (Figure 3.28, Figure 3.29) are transistor level implementations of the block diagram of a lossy

Sinh integrator (see Figure 3.1) derived by means of the ESS method. Yet they can be analyzed by means of STL and DTL principles [250].

In 3.2.3, the analysis based on STL and DTL loops has also been applied to verify that the Sinh integrator topology of Figure 3.19 which is derived by means of the companding synthesis approach implements a 1st order ODE. It can be verified that the same analysis can be applied to the integrator in [154] by identifying the STL loops comprising devices : Q_1-Q_4, Q_5-Q_8, Q_9-Q_{12}, Q_{13}-Q_{16},Q_{17}-Q_{20} (see Figure 3.12 in section 3.2.1) and by considering the DTL loops comprising C-Q_{17}-Q_{18} (see Figure 3.12 in section 3.2.1) and C-Q_{19}-Q_{20} (see Figure 3.12 in section 3.2.1) for which (3.47) and (3.48) hold respectively.

$$I_{cap} = nCV_T \frac{\dot{I}_{OUT}{}^{U}}{I_{OUT}{}^{U}} \tag{3.47}$$

$$I_{cap} = -nCV_T \frac{\dot{I}_{OUT}{}^{L}}{I_{OUT}{}^{L}} \tag{3.48}$$

Observe that unlike in the ELIN Sinh topology of Figure 3.20 [154], the Sinh integrator of Figure 3.12, does not have a global STL loop. The ST loops present in the topology of Figure 3.12 are only formed inside each of the individual blocks (i.e. current splitter, divider and sinh/cosh transconductor). This is a consequence of not implementing all the individual blocks by means of the same TL loop. Check that the current splitter and divider in Figure 3.12 are formed by stacked TL loops while the sinh/cosh tansconductor is formed by an alternating TL loop. The same holds for the companding Sinh integrator of Figure 3.19 [209]. Its equivalent implementation (see Figure 3.20 and Figure 3.21) on the other hand, where all individual blocks, (i.e. current splitter, divider and transconductor), are formed from the same TL loop, does possess global STL loops formed by devices Q_1, Q_2, Q_5, Q_8, Q_9, Q_{10} and Q_3, Q_4, Q_6, Q_7, Q_{11}, Q_{12} respectively.

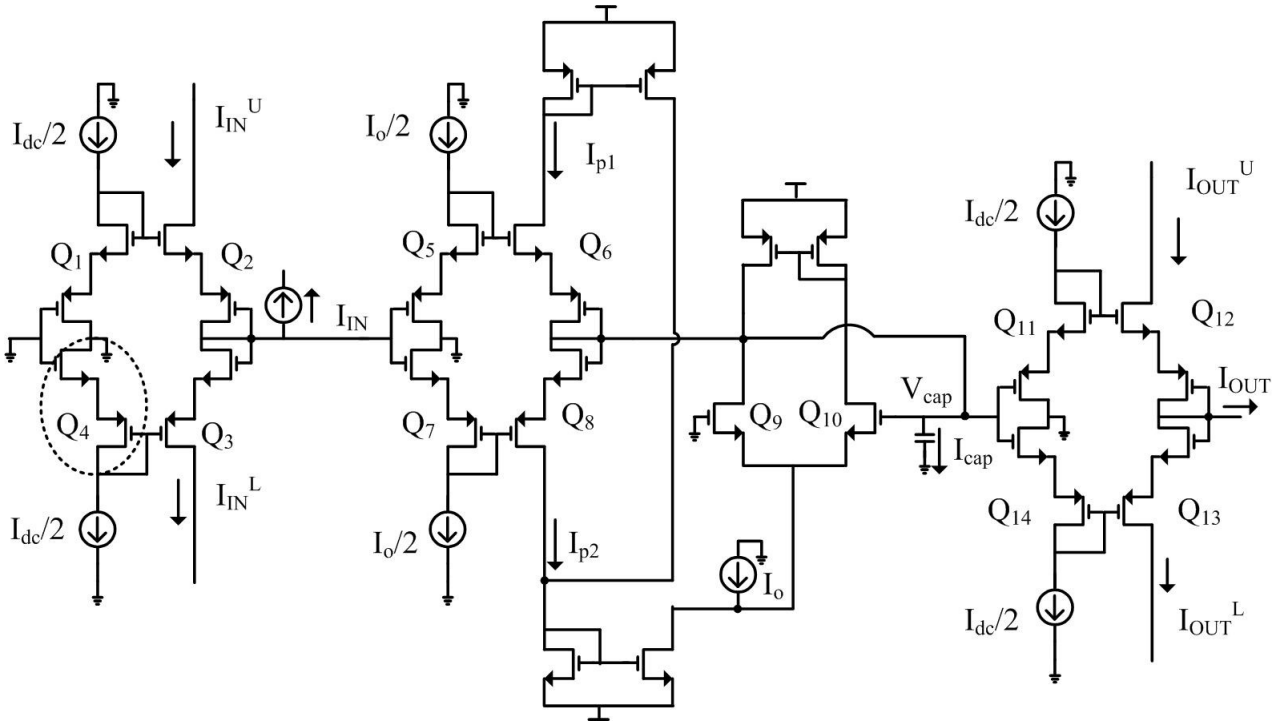


Figure 3.28: CMOS implementation of the Sinh integrator derived by means of the ESS method in [169]. The illustrated topology implements the block diagram of Figure 3.2 [250].

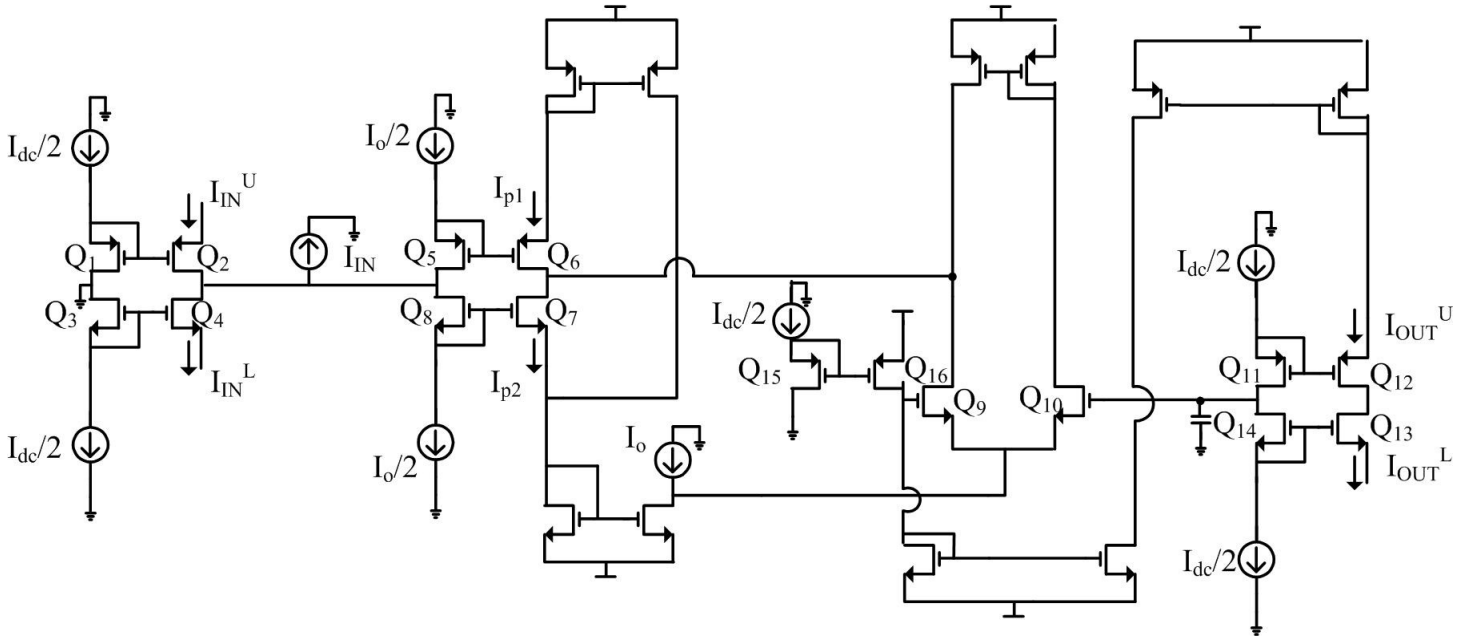


Figure 3.29: Alternative implementation of the block diagram of the ESS Sinh integrator of Figure 3.2. The authors in [250] prove that this topology can be decomposed to the same TL loops as the transistor level topology of Figure 3.28 resulting in the implementation of a Sinh integrator with single type of devices instead of compound devices as in Figure 3.28. The topology of Figure 3.28 had to be modified to include devices Q_{15}, Q_{16}. These devices are part of the TL loop comprising devices Q_{15}, Q_{16}, Q_9, Q_{10}, Q_{11}, Q_{12} which ensure the equivalence of the topology with that of Figure 3.28 by implementing equation (3.38) [250].

3.4 Alternative implementations

Alternative building blocks including $\sinh^{-1}$ *I-V* converters, sinh/cosh transconductors, multipliers/dividers and current splitters, are presented in this section and compared with respect to their suitability for implementing Sinh integrators based on either the ESS or the companding synthesis methods.

3.4.1 $\mathbf{Sinh^{-1}}$ *I-V* blocks

For a Sinh integrator that has been designed by means of the ESS method (see Figure 3.1), a non-linear $\sinh^{-1}$ *I-V* conversion of the input current to an internal voltage node, is necessary as explained previously. Although the transconductors illustrated in Figure 3.22 and Figure 3.24 can be also successfully used as transimpedance blocks, the topology of Figure 3.11 is not suitable for an accurate *I-V* conversion. The horizontal symmetry defined by the p-type and n-type devices of the transconductors in Figure 3.22 and Figure 3.24, which handle the upper and lower phases of the input current respectively, ensures -at least in theory- that for zero input current, the output voltage will be zero (i.e. no offsets). This is not the case with the topology of Figure 3.11 which comprises only p-type devices in its TL loops and hence exhibits a vertical symmetry.

An *I-V* $\sinh^{-1}$ block comprising p-type devices only in its TL loop has been proposed in [157]. The proposed topology is illustrated in Figure 3.30 and consists of the input current splitter and an E-cell used for the implementation of the Sinh integrator in [154] (see Figure 3.10, Figure 3.11). Considering the relation between the $\sinh^{-1}$ function (3.49) and the two input current phases (3.50) and (3.51) of the geometric mean splitter (see Figure 3.30), it is obvious that by adding the input current to the sum of the two split input phases leads to equation (3.52) which corresponds to the argument of the logarithm in the expression of the $\sinh^{-1}(I_{IN})$. Verify that when sourcing the current codified by (3.52) from the output of a p-

type E-cell (Figure 3.30) with its negative voltage terminal grounded, then the voltage appearing at the positive terminal will be equal to the $\sinh^{-1}$ of the input current. Note however that the performance of this topology is restricted by the need for perfect matching of the two input current sources.

$$\sinh^{-1}(x) = \ln(x + \sqrt{x^2 + 1}) \forall -\infty < x < \infty \tag{3.49}$$

$$I_{IN_L} = \frac{-I_{IN} + \sqrt{I_{IN}{}^2 + I_o{}^2}}{2} \tag{3.50}$$

$$I_{IN_U} = \frac{I_{IN} + \sqrt{I_{IN}{}^2 + I_o{}^2}}{2} \tag{3.51}$$

$$I_{IN_U} + I_{IN_L} + I_{IN} = I_{IN} + \sqrt{I_{IN}{}^2 + I_o{}^2} \tag{3.52}$$

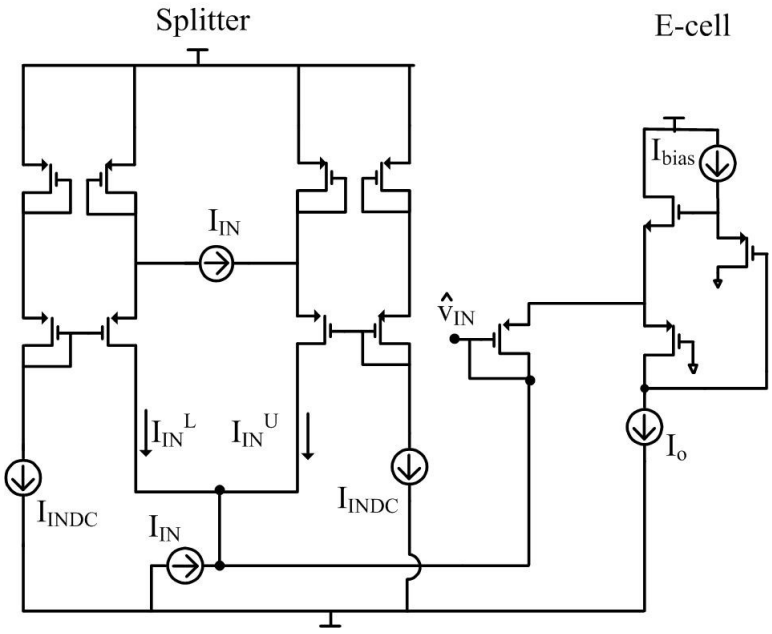


Figure 3.30: An all-PMOS $\sinh^{-1}$*I-V* cell proposed in [157].

3.4.2 Current splitters

For a companding Sinh integrator (see Figure 3.4), the current splitter is an essential building block used to condition the input current so that a class-AB topology is realized. Current splitters which conform to either the GM or the HM law have been presented in section 3.2. A common feature of the aforementioned current splitter topologies is that they are all implemented by means of stacked TL loops. Alternative implementations of input current conditioning circuits which are implemented by means of alternating TL loops have been proposed in [228,251-253]. The alternating TL loops benefit of lower power supply requirements.

For example, Figure 3.31 illustrates the PMOS version of the current splitter topology presented in [251]. The alternating TL loop formed by devices Q_1-Q_4, ensures the GML is satisfied. The authors in [251] have also proposed a HM current splitter based on an alternating TL loop the CMOS version of which is illustrated in Figure 3.32. Other topologies of GM current splitters have been proposed in [228,252-254], the CMOS implementations of which are illustrated in Figure 3.33, Figure 3.36, Figure 3.34 and Figure 3.35. All five topologies are formed by alternating TL loops and only differ in the biasing arrangement. Finally in [191], a noise cancelling technique has been adopted in order to decrease the noise of the GM current splitter of Figure 3.36 and therefore achieving an improvement in its DR by 13dB.

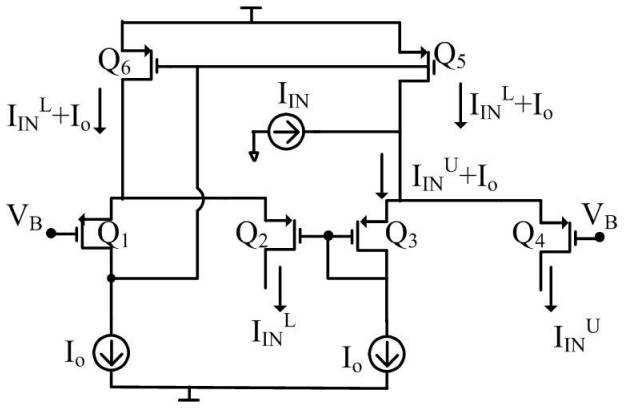


Figure 3.31: PMOS version of the alternating TL loop based geometric mean splitter in [251].

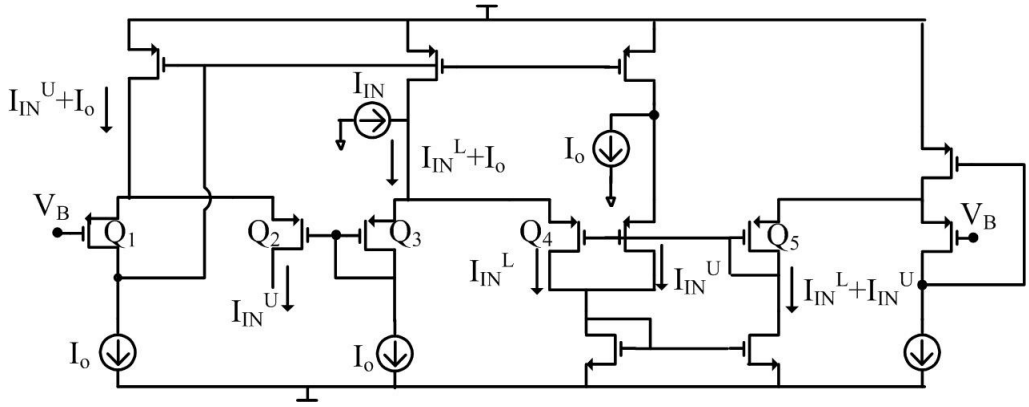


Figure 3.32: PMOS version of the alternating translinear loop based harmonic mean splitter in [251].

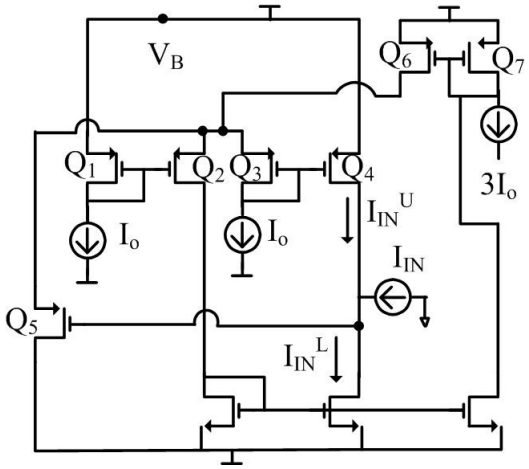


Figure 3.33: PMOS version of the alternating TL loop based GM current splitter in [228].

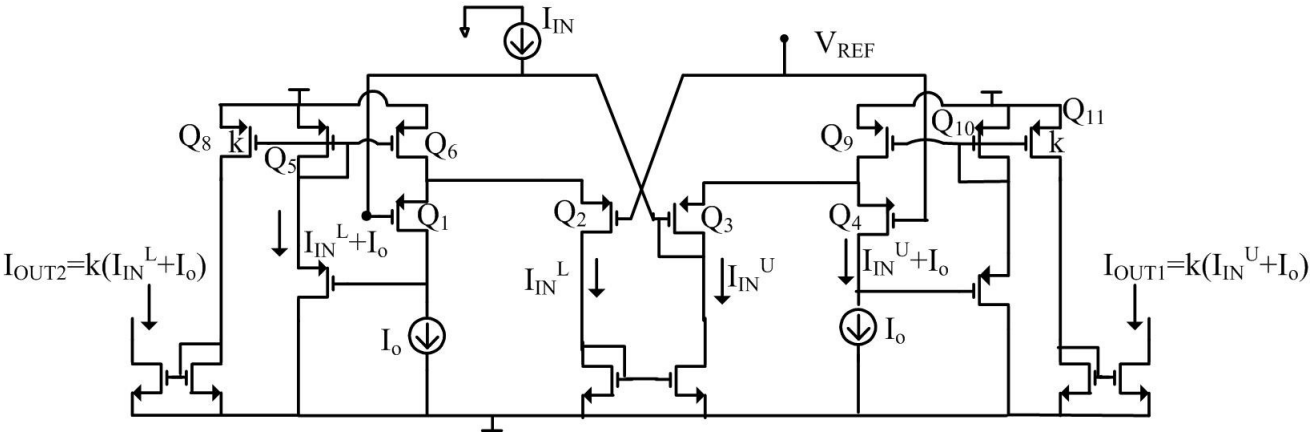


Figure 3.34: Current splitter from [252] based on an alternating TL loop.

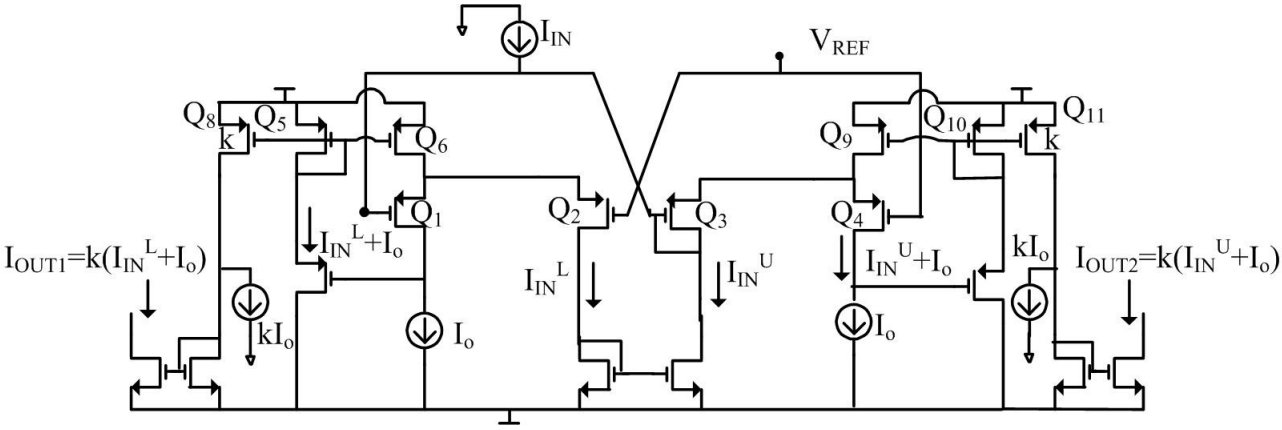


Figure 3.35: Alternative splitter from [253].

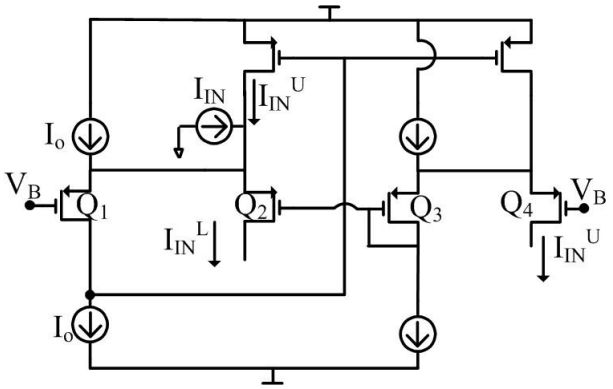


Figure 3.36: Current splitter implementation based on an alternating TL loop from [191].

3.4.3 **Multipliers/Dividers**

A multiplier or divider is a useful block for the implementation of the block diagram of an ELIN Sinh integrator (Figure 3.4) both for carrying out the division of the input current with the derivative of the output current with respect to the integrating voltage as codified by equation (3.14) -i.e. the linearization condition- as well as for providing a tuneable gain (useful both for integrators as well as for the implementation of biquadratic structures). The simplest way to implement class-A multiplier is through a TL loop. For example a stacked TL loop can be used such as the one utilized for the implementation of the integrator in [154] (see Figure 3.13).

Alternatively, an alternating TL loop can be used for the implementation of a class-A multiplier as illustrated in Figure 3.37. This current multiplier is implemented by an

alternating TL loop formed by devices Q_1-Q_4. The input is fed to the low impedance diode connected drain terminal of Q_1 and the output current is obtained from the high input impedance output of device Q_4. Devices Q_2 and Q_3 are biased by the dc current sources $I_{dc1,2}$. Devices Q_7, Q_8 serve as level shifters which lower the impedance at the drain terminals of Q_2 and Q_3 for the correct biasing of the topology. Following the TL loop, the output is obtained as in (3.53). In should be noted that multipliers implemented by alternating TL loops would enable lower power supplies.

$$I_{OUT} = \frac{(W/L)_2 (W/L)_4}{(W/L)_1 (W/L)_3} \frac{I_{IN} I_{dc1,2}}{I_{dc2}} \tag{3.53}$$

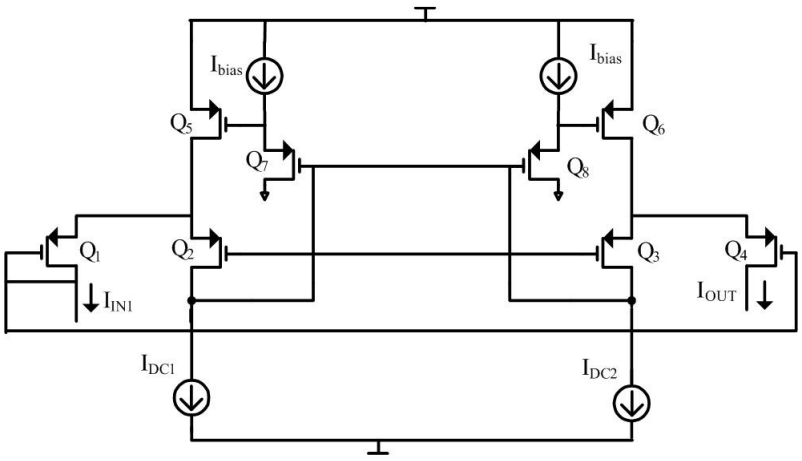


Figure 3.37: An example of an alternating TL loop used as multiplier. The loop comprises devices M_1-M_4.

A class-AB multiplier is easily obtained in a pseudo-differential fashion [154,228,246] whereby a current splitter (see 3.4.2) provides two positive phases of the input current (I_{IN}). Each of the phases is divided by a class-A multiplier (implemented by either a stacked or alternating TL loop) and the output phases are subtracted to obtain the class-AB output. Class-AB multipliers are presented in [252-253]. The concept behind these topologies is illustrated in Figure 3.38. They comprise three sinh transconductors and a current splitter. The output current of the multiplier is codified in (3.54). Assuming that the biasing currents

of the transconductors S_2, S_3 are provided by the current splitter then by substituting $I_{IN2}=I_A-I_B$ in equation (3.54), leads to (3.55). A programmable multiplier can be implemented this way simply by introducing a gain to the current splitter [252-253] such that I_{IN2} is equal to $k(I_A- I_B)$. Then the gain is equal to k/I_o. This topology has been shown to operate from a mere power supply of 0.5V [252-253] hence it suits a low power regime more than the stacked TL loop that has been used in [154] to implement the multipliers of the ELIN Sinh integrator block diagram (Figure 3.4).

$$I_{OUT} = I_{OUT1} + I_{OUT2} = \frac{I_A - I_B}{I_o} I_{IN1} \tag{3.54}$$

$$I_{OUT} = \frac{I_{IN2}}{I_o} I_{IN1} \tag{3.55}$$

Note that the accuracy of these blocks which is very critical for the implementation of ELIN Sinh topologies (see (3.14)) is entirely limited by the accurate exponential conformity of the weakly inverted devices in their respective TL loops.

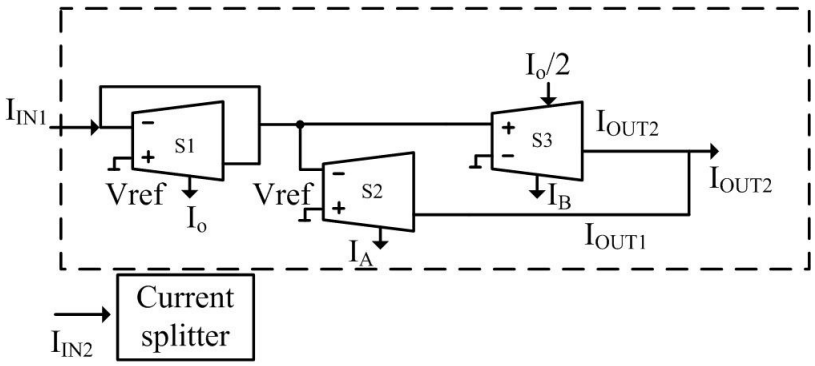


Figure 3.38: Class-AB multiplier block diagram [252].

3.4.4 **Transconductors**

Alternative sinh/cosh transconductor topologies to those presented in section 3.2, have been proposed in [228,252]. The CMOS version of the sinh transconductor in [228] is illustrated in Figure 3.39. By using KVL around the loops comprising V_{shift}, Q_1, Q_2, V_C and V_C, Q_3, Q_4, V_{shift} respectively, and assuming equal aspect ratios for devices $Q_{1\text{-}4}$, the output currents ($I_{OUT}{}^U$, $I_{OUT}{}^L$) are expressed as follows:

$$I_{OUT}{}^U = I_q \exp[(V_C - Vshift)/nV_T] \tag{3.56}$$

$$I_{OUT}{}^L = I_q \exp[(-V_C + Vshift)/nV_T] \tag{3.57}$$

This is also an all-PMOS transconductor which complies with the GML. Note that the capacitor is now applied at the downshifted -by the amount V_{shift}- voltage V_C such that:

$$V_{cap} = V_C - V_{shift} \tag{3.58}$$

$$I_{OUT}{}^U = I_q \exp[(V_{cap}/nV_T] \tag{3.59}$$

$$I_{OUT}{}^L = I_q \exp[(-V_{cap})/nV_T] \tag{3.60}$$

The power supply requirements of this transconductor are lower than the one presented in [154] (see section 3.2.1). Moreover note that the capacitor is applied through a buffer to the source terminal (V_C) of devices M_2, M_3 (Figure 3.39) in order to minimize the effect of capacitor the on the transconductor. This becomes important deep in the pass band where the impedance of the capacitor becomes comparable to the $1/g_m$ of the driving device leading to distortion. An alternative biasing of an alternating TL loop, functioning as a sinh/cosh transconductor, to that proposed in [154], has also been proposed in [252] (see Figure 3.40). This topology also complies with the GML.

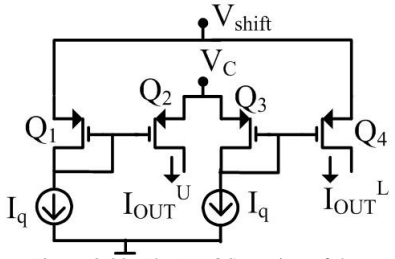


Figure 3.39: The PMOS version of the sinh/cosh transconductor in [228].

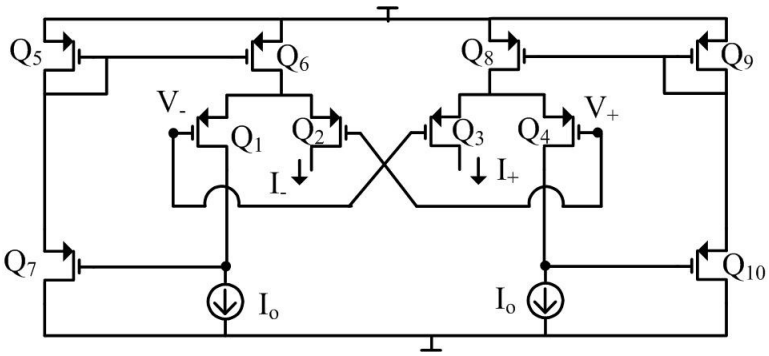


Figure 3.40: Alternating TL loop implementing the transconductor in [252].

3.5 Simulated performance of CMOS Sinh integrators

The simulated performance of the CMOS Sinh integrators reported in [154,207,209] and whose transistor-level topologies were presented in section 3.2, is summarized in Table 5. All the values have been extracted from the relevant publications. For the CMOS integrators reported in [227] and [246], the simulated performance of high order topologies based on them has only been reported and is summarized in Table 6. In order to facilitate comparison, a figure-of-merit (FOM) [195] (3.61) has been introduced. It is clear that the integrator in [154], outperforms all other implementations with respect to DR. In addition, it is the only Sinh integrator that has been implemented by means of p-type devices only in its TL loops (section 3.2.1). As explained in Chapter 2, this ensures more accurate exponential conformity without the need of a triple-well process. The integrator in [209] on the other hand performs best in terms of power consumption. Although not included in the comparison tables (the objective is to compare CMOS integrators), it is worth mentioning that the bipolar Sinh integrator in [228] is the only other fabricated Sinh topology besides [154]. Its transistor level implementation is very similar to the integrator in [154] in that it also comprises pnp only devices in its TL loops with the exception of the dividers while at the same time it has the lowest supply (0.95V) when compared to all CMOS implementations (Table 5, Table 6). Its measured DR however, amounts to 73dB for THD< 2% which is not representative of the full potential of the inherently class-AB Sinh filters. Moreover, one would expect that the DR

would be better in a bipolar implementation where the devices conform inherently to the exponential law over a wider range than the CMOS weakly inverted devices.

$$FOM = \frac{10^{\frac{DR(dB)}{20}}}{\left(\frac{Max.Power}{polexBW}\right) x \left(Tot.Cap.\right)} \tag{3.61}$$

Table 5: Comparison of the performance of the CMOS Sinh integrators in [154,207,209].

Topology	[154]	[207]	[209]
Pole frequency	2kHz	2kHz	636Hz
Power Consumption (μW)	0.2	1.52[a]	0.02
Total capacitance (pF)	20	20	10
Voltage Supply (V)	±1	±1	0.75
Input referred noise floor (pA)	12.3	40	4.2
DR (dB)	132 @1/3ω_o	120 @1/3ω_o	75[b]
SNR (dB)	62 @ 1/5 ω_o	N/A	N/A
SNDR (dB)	46 @ 1/5 ω_o	N/A	N/A
FOM	1.99 x10^{27}	6.28x10^{25}	3.5x10^{23}

a The biasing currents I_{DC} of the sinh/cosh transconductor (see Figure 3.11), have been set to 40nA.

b The DR for the THD level at 1dB compression point.

Table 6: Comparison of the performance of the CMOS Sinh 3rd order low pass filters in [227,246].

Topology	[227] direct implementation	[227] Indirect implementation	[246]
Filter type	3rd order Leapfrog	3rd order Leapfrog	3rd order Butterworth
Pole frequency	10Hz	10Hz	46Hz
Power Consumption (nW)	14	35.5	12.4
Total capacitance (pF)	445	445	N/A
Voltage Supply (V)	±0.75	±0.75	N/A
Input referred noise floor (pA)	0.28	0.59	0.2
DR (dB)	74.6 (THD<1%)	52.5 (THD<1%)	70.6(THD <4%)
SNR (dB)	N/A	N/A	N/A
SNDR (dB)	N/A	N/A	N/A
FOM	2.68X10^{22}	2.1x10^{21}	N/A

3.6 A practical Sinh companding integrator: Design considerations

The integrator proposed in [154] is the building block used for the synthesis of the high order Sinh filters presented in the following Chapters. The aim of this section is to highlight important traits in its performance and insights in its operation in order to explain the choices of device geometries and biasing currents that have been used for the high order topologies presented in the following Chapters.

3.6.1 Current splitter

As an inherent feature of all Sinh integrator implementations based on the ELIN synthesis approach [156] (see section 3.1.2), the input splitter (see Figure 3.10) is decoupled from the rest of the circuit, therefore allowing for more flexibility in terms of transistor-level design and the overall optimisation options. For example I_{INDC} can be set to a low value to reduce the power consumption. The performance of the splitter is critical for the overall performance of the integrator since the linearity of the whole topology cannot exceed that of its input stage.

3.6.2 Multipliers/Dividers

The devices forming the TL loops withstand dc biasing levels with relative differences up to three orders of magnitude for I_o=10nA and need to be sized accordingly in pairs to ensure that each is operating as deep in weak inversion as possible for its respective biasing conditions. Observing the dependence of the g_m/I_D ratio on the V_{gs} variations in the weakly inverted MOS devices (see Figure 3.41), a general good practice is to use devices with large width and small lengths therefore extending the weak inversion operation. From the study of the integrator in [157], it appears that the THD dramatically improves as the width of the lower devices in the TL loop of the dividers (refer to Figure 3.13, Figure 3.12)

increases from 10μm to 300μm for given length size (set to 1 μm) while the upper devices of the divider have been optimized at 5/9. It should be noted here that prior knowledge of the dc levels of the devices of a TL loop, allow for appropriate sizing to be chosen to mitigate variations in the g_m/I_D ratio which is experienced by the TL loop as variations in the value of n. For example, from KVL around the TL loop of the divider in Figure 3.37 it follows that:

$$n_1 \ln\left(\frac{I_1 L_1}{I_{Do} W_1}\right) - n_2 \ln\left(\frac{I_2 L_2}{I_{Do} W_2}\right) + n_3 \ln\left(\frac{I_3 L_3}{I_{Do} W_3}\right) - n_4 \ln\left(\frac{I_4 L_4}{I_{Do} W_4}\right) = 0 \qquad (3.62)$$

Clearly the different values of n will result in gain errors. This can be partially resolved by appropriately sizing the devices and in particular if the current values are known apriori. If for example a gain of 20 needs to be implemented from the divider in Figure 3.37, it is expected that I_{dc2} will be 20 times larger than I_{dc1} and hence the size of the device M_2 carrying 20 times less current could be made smaller than M_3 (check (3.62)) to avoid variations in n. Obviously in M_1 and M_4 should be sized accordingly.

Anticipating the dc current levels however, is not possible for the dividers carrying the capacitor currents unlike in the case of the TL loops implementing a programmable gain. By performing a dc analysis of the TL loop that handles the division (3.14) (see Figure 3.12), the dc current of the devices which carry the upper and lower phase of the capacitor current, is described by equation (3.63). The current I_{INDC}, like the dc biasing current (I_{DC}) of the transconductor (see Figure 3.11) is a free parameter not restricted from the synthesis to attain particular values. Its optimisation has been shown [157] to significantly improve the large signal performance of the integrator. Apart from setting the dc value of the capacitor currents (upper and lower phase, see Figure 3.12) together with the current I_{INDC}, it also controls the level of compression of the input currents. Referring to (3.14), the larger it is, the larger the compression and the smaller the voltage swings at the capacitor node. From the simulations

performed in [157], it appears that in practice, there exists an optimal region in the range of I_{DC} currents which optimises the DR for given device sizes. For the integrator optimized as in [154,157], it appears that upon increasing I_{DC}, the overload[9] level increases but beyond 54μA, the overload level saturates to that value and further increase does not improve the linearity of the integrator. The noise and power consumption also increase linearly with I_{DC}.

$$I_{cap}^{U,L}{}_{(DC)} = \frac{I_o(I_{INDC} + I_{DC}/2)}{I_{DC}} \tag{3.63}$$

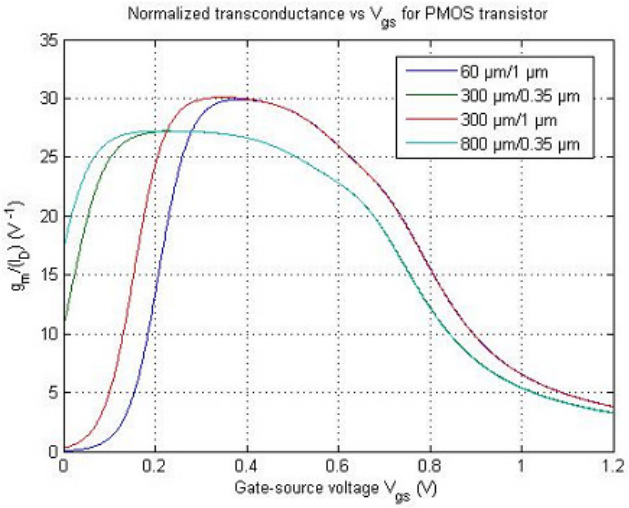


Figure 3.41: Normalized transconductance for PMOS transistors in CMOS 0.35μm technology [230].

Finally, other factors that affect the performance of the dividers, implemented by means of weakly inverted MOS devices, are the variations in the gain due to finite output impedance (i.e. variations in the V_{ds}) as well as the gate-source capacitance at high frequencies. One way to solve the former problem is by cascoding devices which are severely affected by V_{ds} variations although this will have consequences in the minimum power supply that can be achieved. The latter can be tackled by using larger currents $I_{dc1,2}$ which would be affected to a lesser extent from the finite gate currents which become significant at higher

[9] Overload is defined as the maximum input current for THD<4%

frequencies due to the gate experiencing smaller input impedance. Increasing the dc biasing currents however comes at the obvious penalty of increased power consumption.

3.6.3 **Sinh/Cosh transconductor**

Looking at the left half of the transconductor (Figure 3.42), the connection from the gate of Q_5 to the drain of Q_2 through the V_{gs} of Q_7 -which acts as a level shifter-, lowers the impedance at the drain of Q_2 so that it can be biased with the current $I_{DC.}$ As explained in sections 3.2.1, 3.4.3, the level shifter provides more "breathing" space to devices Q_5 (tail transistor) and $Q_{2.}$ Note that following the signal path as the red broken line in Figure 3.42 indicates, the voltage potential from the power supply to the drain of Q_2 is equal to $V_{gs5} + V_{gs7}$ where V_{gs7} is and adjustable voltage shift:

$$V_{gs7} = nV_T \ln\left(\frac{L_7}{W_7}\frac{I_{bias}}{I_{DO}}\right) \tag{3.64}$$

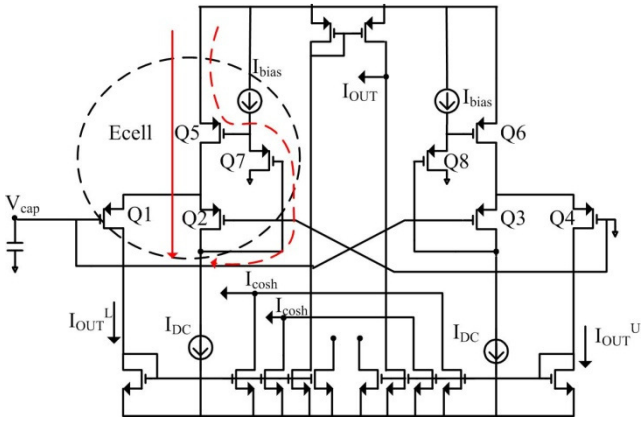


Figure 3.42: The all-PMOS transconductor used in [154].

Following the signal path as the solid red line indicates in Figure 3.42, the voltage potential $V_{gs5} + V_{gs7}$ is equal to the sum of the V_{ds} voltages of the respective devices (Q_2, Q_5). For the sole purpose of lowering the impedance at the drain of Q_2, it would have been adequate to use the gate connection of the tail device (Q_5) however it is trivial to verify that in

the absence of the level shifter, the sum of the drain source voltages of devices Q_5, Q_2 is only equal to V_{gs5}. From (3.64) it is clear that in order to achieve a large voltage shift from a small I_{bias} current, the level shifter needs to be a long, narrow device.

Another important detail in the transconductor topology of Figure 3.42 is the asymmetry it exhibits which is experienced as an asymmetry in the output phases for large currents. Although Q_2 has a constant source voltage (note that its gate is grounded and it is biased at a constant dc current, see Figure 3.42), Q_3 on the other hand, has a time varying V_s since V_{cap} is applied at its gate and is in turn level shifted to its source (by an amount of $nV_T\ln[(L_3I_{DC})/(W_3I_{DO})]$). Assume that a large AC signal is applied to the capacitor node. At the time it obtains its peak, Q_3 has a constant current (I_{DC}) flowing through it and a large voltage potential will appear at its source terminal. This will force Q_4 to draw a large current which in turn needs to be supplied by the tail transistor (Q_6) under limited V_{ds6}. Remember that $V_{ds6} = V_{gs6} + V_{gs8} - V_{ds3}$. V_{ds3} has increased due to the large AC signal at the capacitor node and it might cause the tail device to depart the saturation region. This also explains the need for the level shifter. Observe that a large V_{gs8} will leave more the margin for V_{ds6}.

A number of ways have been suggested in [157,230] to mitigate this effect and they can be summarized in: a) increasing the widths of Q_1-Q_4 so that the voltage shift introduced by Q_3 is smaller, b) increasing the voltage supply which clearly does not suit a low power supply regime, c) lowering the common mode level of the S-cell (see Figure 3.42) by inserting an offset voltage. This will lead to two exponential dc current terms which will correct the dc voltage offset at the capacitor and d) making Q_6 large so that it has better current sourcing capability. Note that attention should be paid in not making the voltage shift provided by Q_3 too small since this would imply that Q_4 will be switched off for large negative voltage swings at the capacitor node. Moreover when the capacitor node exhibits a large negative voltage swing, Q_4 would draw very small current and this might cause the gate

of the tail device (Q_6) to hit the power supply. This effect would be even more prominent at the absence of the level shifter. Note that if the gate of Q_8 was directly connected to the drain of Q_3, then (for a large negative voltage swing at the capacitor node), the drain of Q_3 would increase while at the same time its source would reduce. The limited V_{ds3} would cause the device to depart from the saturation region.

3.6.4 Matching and linearity versus bandwidth

When large devices are used in order to improve matching and linearity (as discussed previously) and small currents in order to a) ensure that devices operate in weak inversion and b) to maintain low power consumption, parasitic poles will be inserted at higher frequencies. The f_T of the devices will be smaller (remember from Chapter 2 that f_T is proportional to I_D/WL). Parasitic poles can in turn be the source of excess phase shift which will become a burden when the integrator is to be used in feedback loops (e.g. biquadratic structures, [230].

3.6.5 Simulated performance

The CMOS Sinh integrator proposed in [209] and presented in section 3.2.3 has the lowest reported power consumption out of all the CMOS Sinh topologies reported to date (see Table 5). Both ELIN integrators [154,209] have been simulated in Cadence Design Framework in order to be compared since they are the only CMOS Sinh topologies derived by means of the ELIN companding synthesis approach [156]. For the integrator in [209], the power supply has been set to ±0.75V and all devices have been sized 100μm/1μm as reported in [209]. The simulated results reported in [209] could not be faithfully reproduced.

Figure 3.43 depicts the tuning of the small-signal frequency response of the topology in [209]. Observe that the transfer function has a gain error of approximately 2. The power consumption and noise of the topology for I_o=10nA and C=20pF appear to be as reported in [209] however the linearity of the filter is quite poor. Referring to Figure 3.44, the THD is

higher than reported in [209]. A possible explanation of the worse linearity of this topology when compared to the integrator in [154] is that the splitter is not biased adequetely for input frequencies close to the stopband of the filter. The choice of indirectly biasing the input current splitter with currents I_{DC} (see section 3.2.3, Figure 3.21; the splitter is biased by means of the output phases of the sinh transconductor) has as a result a) that the splitter is coupled to the rest of the topology and b) when the input signal is placed at/ close to the stop band, the splitter is not adequately biased. This speculation could explain the high THD level illustrated in Figure 3.44. Finally the interested reader could confirm that if the splitter is biased by means of I_{DC} current sources, then devices Q_5, Q_6 should be biased with $I_{OUT}{}^{U}$ and $I_{OUT}{}^{L}$ (Figure 3.21) respectively in order for the correct capacitor currents to flow at the collectors of Q_8, Q_7. It has been confirmed that this modification both corrects the gain error (see Figure 3.45) in the transfer function and improves the linearity.

Figure 3.46 illustrates the frequency response of the Sinh integrator proposed by in [154] tuned by means of current I_o with 20pF capacitor. Its power supply has been set to ±1V while all PMOS devices have been sized 300µm/1µm and all NMOS devices 115 µm/1µm with the exception of the upper devices in the TL loop of the multipliers (see Figure 3.13) which have been optimized 5µm/9µm, the level shifters in the transconductor optimized at 2 µm /115µm and finally the NMOS devices of the mirror which carries $I_{cap}{}^{L}$ to the capacitor node which are optimized to 1µm/20µm. Under this set-up, the simulated power consumption of the integrator is 687nW and its input referred noise floor integrated over its 3dB bandwidth amounts to 27pA. Figure 3.47 illustrates the THD versus modulation index for two input tones at 1/3 of f_o and deep in the passband. Observe the excellent linearity of the topology. The effect of the improvement in linearity of the filter [154,157] when the I_{DC} current (Figure 3.12) of the sinh/cosh transconductor is increased, is illustrated in Figure 3.48 for an input tone at f_o. For an input tone at $f_o/3$, the THD reaches 4% faster and it can be confirmed that an

increase of I_{DC} has no effect on the linearity performance (refer to Figure 3.49). Figure 3.50 depicts the SNR versus modulation index for an input signal deep in the passband confirming the class-AB nature of the integrator (Chapter 2).

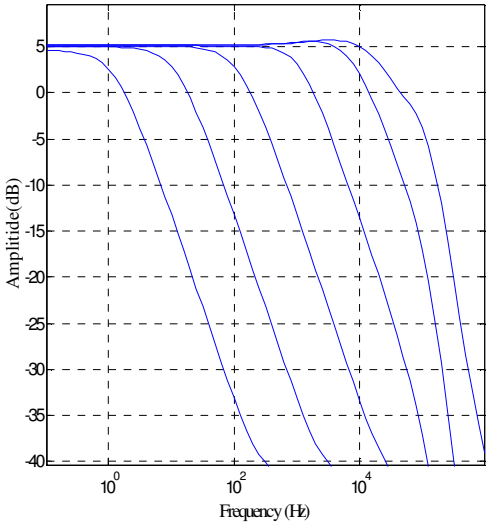


Figure 3.43: Tuning of the frequency response of the integrator in [209] by means of I_o. The capacitor is set at 20pF. Note that there is gain error of ~2 in the transfer function.

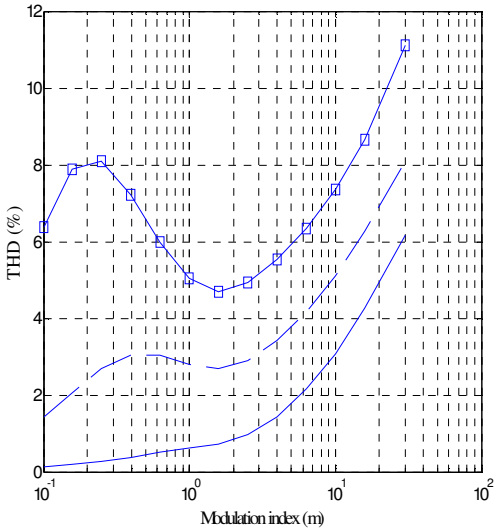


Figure 3.44: THD versus modulation index for the integrator in [209] for three tones placed deep in the pass band, at 1/3 of f_o (--) and at f_o (squares). The THD rises sharply to 4% for tones in the pass band while in the stop band the linearity is even worse.

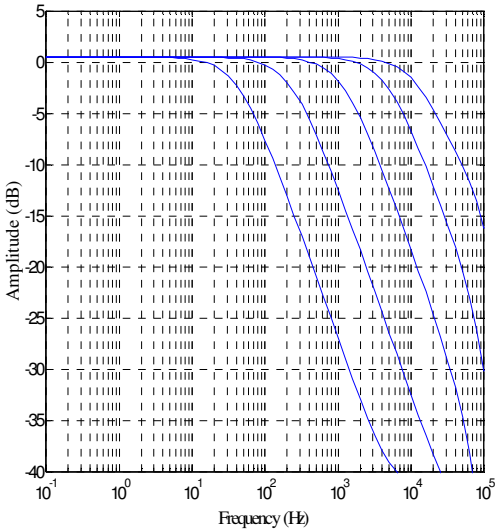


Figure 3.45: Tuning of the frequency response of the integrator in [209] when it is modified so that its input current splitter is biased with dc currents I_{DC}. Note that the gain error (see Figure 3.43) is corrected. The response is tuned by means of I_o with C=20pF.

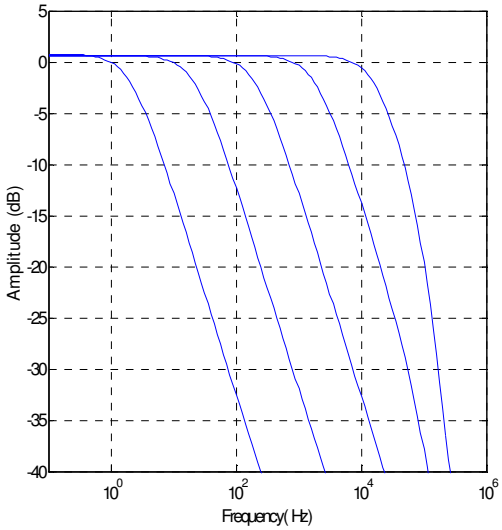


Figure 3.46: Tuning of the frequency response of the integrator in [154] by means of I_o. The capacitor is set at 20pF.

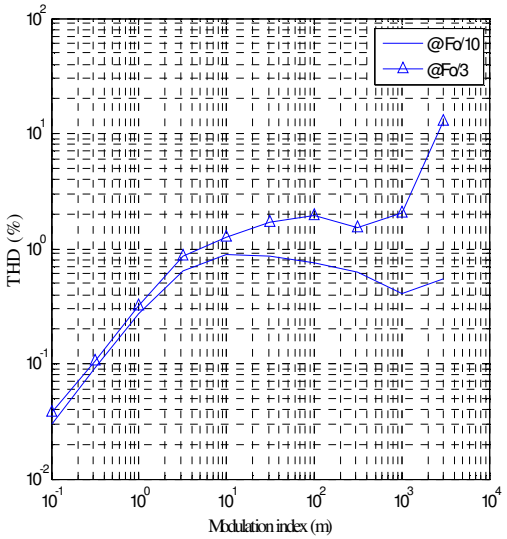


Figure 3.47: THD versus modulation index for the integrator in [154] with input tones at $f_o/3$ and at $f_o/10$. THD remains below 1% for modulation index values up to 1000. This corresponds to a DR>110dB.

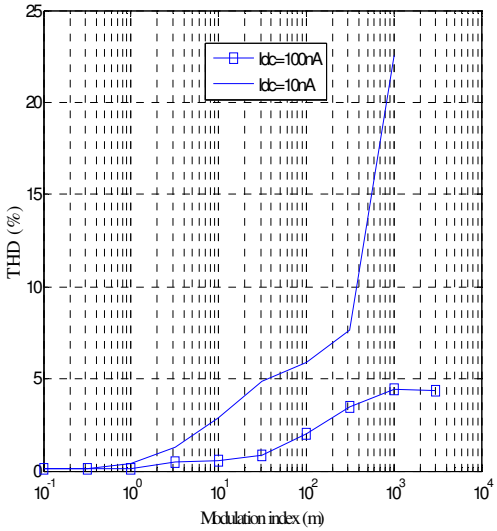


Figure 3.48: THD versus modulation index for the integrator in [154] with the input tone at f_o. The simulated pole frequency (f_o) is 2300Hz. Observe the improvement of (DR>100dB) when the dc current of the transconductor increases from 10nA to 100nA.

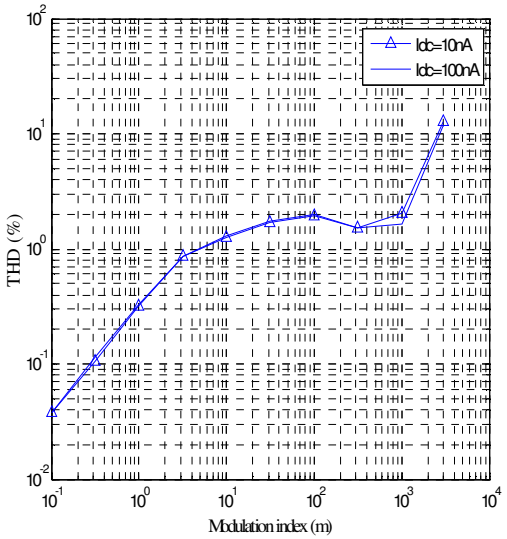


Figure 3.49: THD versus modulation index for the integrator in [154] with an input tone at $f_o/3$.

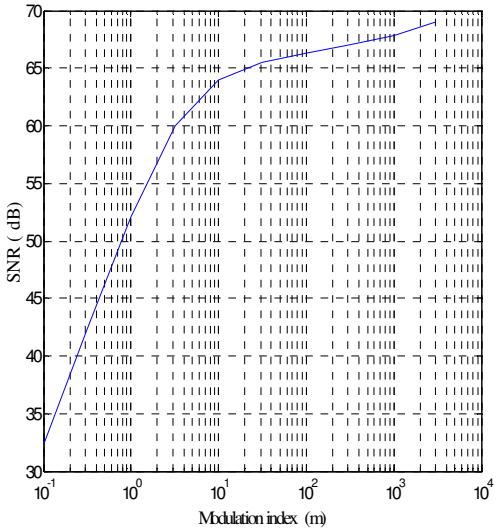


Figure 3.50: The SNR of the Sinh integrator in [154] corresponding to an input tone deep in the pass band (f_o/10) versus modulation index. For m=1000, THD<1% and SNR>65dB while DR>110dB.

3.7 Conclusion

This Chapter has dealt with the synthesis, hardware implementation and analysis of all presently reported CMOS Sinh integrators while extensions for possible alternative implementations have been suggested. The integrator proposed in [154] has been shown to outperform all other CMOS Sinh integrators. It is therefore chosen as the building block of the high order CMOS Sinh topologies presented in the following Chapters.

4 Simulation study of high order CMOS Sinh filters

This Chapter provides a review of the synthesis methods by which high order Sinh filters can be designed and details a transistor level synthesis approach which enables the design of high-order class-AB Sinh filters by means of CMOS weak-inversion Sinh integrators comprising p-type only devices in their translinear loops (TL). The synthesis method is demonstrated via the step by step design of a biquadratic filter. Further examples of 3^{rd} and 6^{th} order CMOS Sinh topologies are designed following the introduced synthesis framework and their performance is assessed by means of simulations featuring frequency and time-domain performance. More specifically, a 3^{rd} order low pass Sinh filter of Bessel approximation for ECG processing and a 6^{th} order Bessel Sinh topology based on the cascade of 3^{rd} order sections are presented. The Chapter progresses with a study of the simulated performance of a 5^{th} order Chebyshev Sinh CMOS filter response with a cut-off frequency of 100Hz and a pass band ripple of 1dB. The topology is also compared head-to-head with the behaviour of its pseudo-differential class-AB CMOS Log-domain counterpart. All five filter topologies namely: the biquadratic filter, the 3^{rd} order and 6^{th} order low pass Bessel filters and the 5^{th} order low pass Chebyshev Sinh and Log-domain filters are novel. The assessment of the performance of the aforementioned topologies is based on Cadence Design Framework simulations, using the commercially available 0.35μm AMS process parameters.

4.1 Synthesis methods for high order Sinh filters

The biquadratic filter described by the linear state space equations (4.1)-(4.4), will be used as an example to demonstrate the step by step synthesis of high order Sinh topologies by means of the reviewed methods presented in Sections 4.1.1-4.1.3 .

$$\dot{x}_1 = -\frac{\omega_o}{Q} x_1 - \omega_o x_2 + \omega_o u \tag{4.1}$$

$$\dot{x}_2 = \omega_o x_1 \tag{4.2}$$

$$y_{LP} = x_2 \tag{4.3}$$

$$y_{BP} = x_1 \tag{4.4}$$

4.1.1 **Exponential-State-Space (ESS) mapping method**

Step1: Apply a non-linear mapping of the form $x_i = I_{DC}\sinh(aV_i)$ to the state variables of the linear state-space (4.1)-(4.4).

Step 2: Rearrange the equations of the mapped state-space in order to bring them to the form of the non-linear KCL design equations (4.5) and (4.6) which represent non-linear capacitor currents. The choice of transforming or not equations (4.5) and (4.6) in a more convenient form for implementation of (4.8), (4.9) by means of the identity in (4.7), will lead to the two different topologies illustrated in Figure 4.1 and Figure 4.2.

$$C\dot{V}_1 = -\frac{\omega_o}{Q}\frac{C}{\alpha}\frac{\sinh(aV_1)}{\cosh(aV_1)} - \omega_o\frac{C}{\alpha}\frac{\sinh(aV_2)}{\cosh(aV_1)} + \omega_o\frac{C}{\alpha}\frac{\sinh(aV_{IN})}{\cosh(aV_1)} \tag{4.5}$$

$$C\dot{V}_2 = \frac{\omega_o}{Q}\frac{C}{\alpha}\frac{\sinh(aV_2)}{\cosh(aV_1)} \tag{4.6}$$

$$\frac{\sinh(aV_j)}{\cosh(aV_i)} = \cosh[a(V_j - V_i)]\tanh(aV_i) + \sinh[a(V_j - V_i)] \tag{4.7}$$

$$I_{cap1} = I_o\tanh(aV_1)\left\{-\frac{1}{Q} - \cosh[a(V_2 - V_1)] + \cosh[a(V_{IN} - V_1)]\right\} + I_o\sinh[a(V_{IN} - V_1)] - I_o\sinh[a(V_2 - V_1)] \tag{4.8}$$

$$I_{cap2} = I_o \cosh[a(V_2 - V_1)] \tanh(aV_2) - I_o \sinh[a(V_2 - V_1)] \tag{4.9}$$

Every voltage variable in the equations (4.5) and (4.6) must be represented by an actual node in the circuit. The bipolar Sinh biquad presented in [169], following this method, is the first mentioned Sinh topology. Its CMOS implementation is presented in [227]. The block diagram which implements equations (4.8) and (4.9), is illustrated in Figure 4.1.

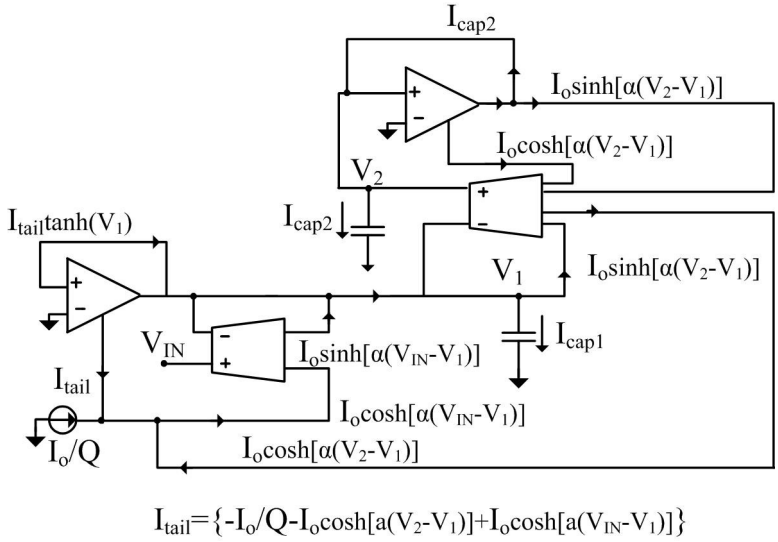


Figure 4.1: Block diagram of the Sinh biquad represented by the state-space description of (4.1)-(4.4) based on the ESS mapping synthesis method. Note that the two additional transconductors required for obtaining the outputs are not included in this figure. The variable α, is technology and implementation dependent. Capacitors are assumed to be equal ($C_1=C_2=C$) and $\omega_o C/\alpha = I_o$.

If one chooses not to employ identity (4.7) and equations (4.5) and (4.6) are implemented instead by means of multipliers/dividers, it can be verified that the resulting topology will be that illustrated in Figure 4.2. Note that the tanh transconductors with non-linear tail currents of the topology in Figure 4.1 have now been replaced by multipliers/dividers. Also note that the *I-V* conversion at the input is still required and that the total number of blocks required -to implement the design equations- is still the same as that of Figure 4.1.

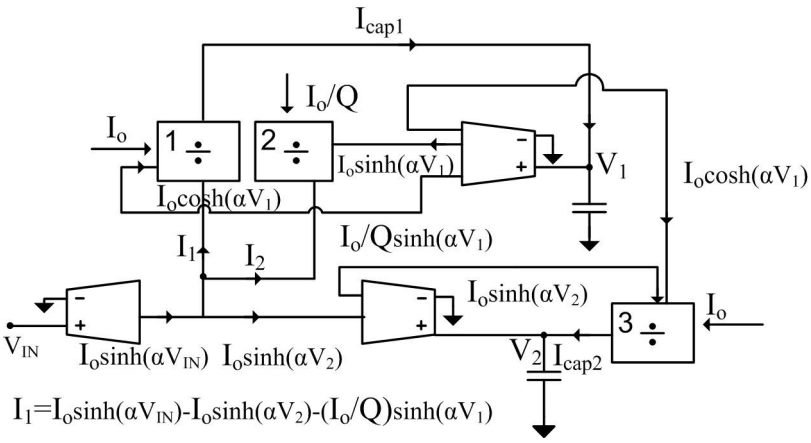


Figure 4.2: Block diagram of an alternative implementation of the biquad described by (4.1)-(4.4) based on direct implementation of (4.5) and (4.6) without the use of identity (4.7). Divider 1 implements: $I_{cap1}=[I_oI_1/I_o\cosh(aV_1)]$, divider 2 implements $I_2=[(I_o/Q)\ I_o\sinh(aV_1)]$ and divider 3 implements $I_{cap2}=I_oI_o\sinh(aV_2)]/I_o\cosh(aV_1)]$.

The authors in [211,255] present a component-substitution method which is based in the transformation of any linear G_m-C filter to an ELIN topology. In their approach, each linear g_m of a G_m-C topology, is substituted by an appropriate non-linear transconductor (G_m) of the form *sinh(αV$_i$)/cosh(αV$_j$)*. Their approach has been demonstrated for the synthesis of a bipolar Sinh biquad based on complementary devices. The resulting topology does not differ from that of Figure 4.1.

Generalizing equations (4.5) and (4.6), high order Sinh filters can be designed by means of the ESS method by implementing equation (4.10) through one of the options discussed above.

$$C_i\dot{V}_i = \sum_{j=1}^{n} \frac{\alpha_{ij} f(V_j)}{\dot{f}(V_i)} + \frac{b_i f(V_{IN})}{\dot{f}(V_i)} \qquad (4.10)$$

4.1.2 **Translinear synthesis method**

Step 1: Transform the dimensionless variables of the state-space equations (4.1)-(4.4) into currents by means of a normalizing current I_o in order to obtain the set of current mode polynomials codified by (4.11) and (4.12) with I_{x1} being the BP output and I_{x2} the LP output.

$$\tau \dot{I}_{x1} = -\frac{1}{Q} I_{x1} - I_{x2} + I_{in} \tag{4.11}$$

$$\tau \dot{I}_{x2} = I_{x1} \tag{4.12}$$

Step 2: Use the dynamic translinear principle (DTP) to express the derivative of currents as products of the state variables $I_{x1,2}$ and the capacitor currents according to (4.13), (4.14) where I_{xi}^{U} represents the upper phase of the state currents and I_{xi}^{L} the lower phase respectively with $I_{x1,2}^{U,L} > 0$ for every input current and state current. Substitute (4.14) into equations (4.11) and (4.12), in order to eliminate the derivatives of the state currents as shown in (4.15), (4.16) where τ/CV_T, is the reciprocal of a current I_T. Comparing (4.1) and (4.2) with (4.15) and (4.16), $\omega_o = I_T/CV_T$. Note that the capacitor current has been mapped into a non linear capacitor current which is a function of the state currents and their derivatives as compared to the capacitor voltage mapping of the ESS method into a non linear voltage of hyperbolic form.

$$I_{capi} = \frac{CV_T \dot{I}_{xi}}{I_{xi}^{U} + I_{xi}^{L}} \tag{4.13}$$

$$I_{xi}^{U} + I_{xi}^{L} = \frac{dI_{xi}}{dV_{capi}} = I_{DC} \cosh(aV_{ci}) \tag{4.14}$$

$$\frac{\tau I_{cap1}}{CV_T} = \frac{(-\frac{1}{Q} I_{x1} - I_{x2} + I_{in})}{I_{DC} \cosh(aV_{c1})} \tag{4.15}$$

$$\frac{\tau I_{cap2}}{CV_T} = \frac{I_{x1}}{I_{DC} \cosh(aV_{c2})} \tag{4.16}$$

Step 3: Apply translinear decomposition to equations (4.15) and (4.16) to obtain a set of translinear design equations based on which the Sinh filter can be implemented by means of translinear loops. Note that instead of (4.13) for the capacitor current, other expressions could be used, but they would necessitate different choices for the translinear decomposition.

4.1.3 Class-AB formulation

The condition for class-AB operation is expressed in [174] as the need for the internal variables ($\overline{w}$) of a system described by (4.17) to remain strictly positive for any input or state variable ($\overline{x}$) (4.18). The system in (4.17) is assumed to experience an overall linear external behaviour and the internal variables $\overline{w}$ are considered to be currents resulting from non-linear mappings of the state variables $\overline{x}$.

In the more appropriate description of a class-AB dynamical system, the state variables and input are expressed in a differential form according to (4.19) resulting in the system description of (4.20).

$$\frac{d\overline{x}}{dt} = \overline{f}(\overline{x},u); y = g(\overline{x},u) = L(u) \tag{4.17}$$

$$\overline{w} = h(\overline{x},u) > 0 \tag{4.18}$$

$$\overline{x} = \overline{x}_\alpha - \overline{x}_b; u = u_\alpha - u_b; A = A_o - A_1; \overline{b} = \overline{b}_o - \overline{b}_1 \tag{4.19}$$

$$\begin{cases} \dfrac{d\overline{x}_\alpha}{dt} = A_o\overline{x}_\alpha + A_1\overline{x}_b + b_o u_\alpha + b_1 u_b + \overline{f}(\overline{\rho}) \\ \dfrac{d\overline{x}_b}{dt} = A_o\overline{x}_b + A_1\overline{x}_\alpha + b_o u_b + b_1 u_\alpha + \overline{f}(\overline{\rho}) \end{cases} \tag{4.20}$$

$$y = \overline{c}^T(\overline{x}_\alpha - \overline{x}_b) + d(u_\alpha - u_b)$$

$$\overline{w} = h(\overbrace{\overline{x}_\alpha, \overline{x}_b, u_\alpha, u_b}^{\rho}) > 0 \tag{4.21}$$

The state variables are required to remain strictly positive for all bounded inputs and the selected internal variables also need to be positive as long as the state variables are positive. The difference of the class-AB constraint of (4.21) with that in the more general formulation expressed in (4.18) is that the internal variables are now constrained to be positive for positive derived state variables and inputs $\overline{x}_\alpha, \overline{x}_b, u_\alpha, u_b$. Note that in (4.20), cross coupling terms can be added by means of $\overline{f}(\overline{x}_\alpha, \overline{x}_b, u_\alpha, u_b)$ as long as they are multiplied by the same factor. Although this method could be used for the synthesis of class-AB Sinh filters, the author recognizes d($\overline{x}_{\alpha,b}$)/dt as two separate systems (filters/capacitors) which together upon subtraction result in the overall system d$\overline{x}$/dt. Strictly speaking this statement immediately hinders the description of Sinh filters from the above class-AB formulation due to the fact that the output stage of Sinh filters permits for the subtraction of the two subsystems in (4.20) to be performed at a single capacitor node. Therefore the formulation in [174], although it perfectly describes the constraints need to be imposed on the internal variables (4.21), it is incomplete in the sense that it does not allow for the description of inherently class-AB systems whose output stages merge the two derived variables (4.19) per state in one capacitor. This formulation can describe the Sinh topologies presented in [169,211], but it is not very intuitive or suggestive of the details of the implementation of topologies which have not resulted from ESS mapping based methods such as [154,207,209,228].

4.2 Discussion and comparison

All of the reviewed methods in section 4.1 have been originally formulated for the synthesis of Log-domain filters and have been extended so that they can cover the synthesis of Sinh filters as well. As a result of this, the methods fail in guiding the designer towards optimal Sinh implementations or they become daunting due to the mathematical complexity associated with high order designs. With the exception of [169,227], there is no evidence of any Sinh topology arising from any of those although in principle they cover the design of high order Sinh filters. Despite the hardware implementation differences identified through the example of the Sinh biquad synthesis in 4.1 by means of ESS mapping based methods, it is common to all that the emphasis is placed on the non-linearly mapped voltage nodes rather than the resulting currents. Hence, the designer is restricted to think in terms of appropriately interconnected *V-I* non-linear transconductor blocks for the realization of a Sinh topology. Also for maintaining linearity, an accurate *I-V* block is required at the input of the Sinh filter so that all the voltage nodes in the circuit are meaningful. Although this method results in elegant and intuitive designs for mappings of logarithmic form, it introduces both mathematical and practical complexity to the synthesis of high order Sinh topologies. In addition to handling complex equations –with progressively increasing difficulty when high order filters are designed-, the *I-V* conversion based on $\sinh^{-1}$ is not as straightforward as the logarithmic compression which is implemented by a single diode-connected device. The complexity of this method could explain why no other high order Sinh filter than the 3rd order low pass filter reported in [227], has been proposed to date based on this approach.

Finally the translinear synthesis method [247] has only been demonstrated for the analysis of the Sinh bandpass biquad presented in [169] and not for the synthesis of practical Sinh topologies. This is possibly due to the complication added by step 3 (section 4.1.2).

4.3 Systematic synthesis for high order Sinh filters

The only practical CMOS Sinh integrator to date [154] is based on the synthesis method described in [156] and was presented in detail in Chapter 3. The Sinh filters designed, studied and tested experimentally in this Thesis employ this practical CMOS Sinh integrator. To facilitate the discussion, its block diagram is repeated in Figure 4.3 below. The basic characteristics of the integrator can be summarized in: a) it is a current-input current-output ELIN topology composed following Tsividis' synthesis method for an ELIN integrator [156] and b) it employs only p-type devices in its TL loops, which favours matching and good logarithmic conformity and implementation in twin-well CMOS processes.

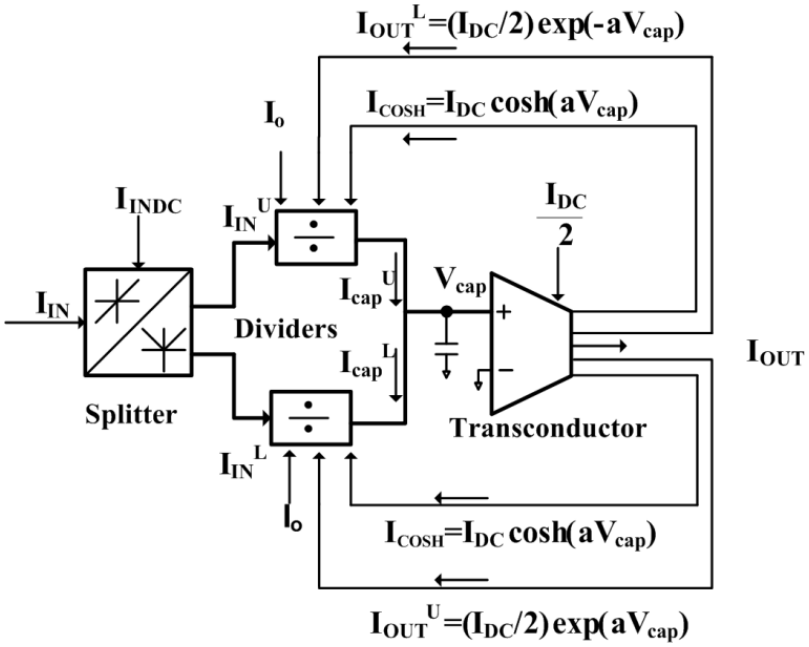


Figure 4.3: Block diagram of the Sinh lossy integrator [154].

An input current splitter which complies either with the Geometric Mean Law (GML) or the Harmonic Mean Law (HML) [207] decomposes the input current into two strictly positive phases termed upper (U) and lower (L). The output current of the integrator is the hyperbolic-sine expansion of the sole capacitor's voltage V_{cap}, $I_{OUT}=I_{DC}sinh(aV_{cap})$ with

$a=1/nV_T$ where n is the sub-threshold slope parameter and V_T is the thermal voltage. The overall input-output linearity of the integrator is ensured by means of translinear dividers which generate appropriate (non-linear) upper and lower phases I_{cap}^{U}, I_{cap}^{L} (Figure 4.3), of the capacitor current. The integrator realizes the transfer function: $I_{OUT}(s)/I_{IN}(s)= (I_{o1}/I_{o2})/(s+I_{o2}/nV_T)$ and lends itself naturally for the realization of class-AB Sinh filters of any state-space description.

Step 1: Consider the state-space description of an N-th order, stable, single-input-single-output (SISO) system:

$$\dot{x}_i = \sum_{j=1}^{N} \alpha_{ij} x_j + b_i u \tag{4.22}$$

$$y = \sum_{j=1}^{N} c_j x_j + du \tag{4.23}$$

Step 2: Let the input and output to be currents denoted as I_{IN} and I_{OUT} respectively and the state variables to also be currents related to integrating (capacitor) voltages through the Sinh mapping:

$$x_i = I_i = I_{DC} \sinh(aV_{ci}), i = 1...N \tag{4.24}$$

Step 3: Substitute (4.24) into (4.22), (4.23), multiply with appropriate constants C_i and rearrange to obtain (4.25),(4.26):

$$C_i \dot{V}_{ci} = \sum_{j=1}^{N} \frac{C_i \alpha_{ij} I_j}{\alpha I_{DCi} \cosh(\alpha V_{ci})} + \frac{C_i b_i I_{IN}}{\alpha I_{DCi} \cosh(\alpha V_{ci})} \tag{4.25}$$

$$I_{OUT} = \sum_{j=1}^{N} c_j I_j + dI_{IN}; \tag{4.26}$$

Step 5: For class-AB operation, define the input and state-currents as $I_{IN}= I_{IN}^{U}- I_{IN}^{L}$ and $I_i= I_i^{U}- I_i^{L}$ respectively with $I_i^{U,L}>0$ and $I_{IN}^{U,L}>0$. This leads to:

$$I_{capi} = C_i \dot{V}_{ci} = \sum_{j=1}^{N} \frac{\frac{C_i \alpha_{ij}}{a}(I_j^{\,U} - I_j^{\,L})}{I_{DCi}\cosh(\alpha V_{ci})} + \frac{\frac{C_i b_i}{a}(I_{IN}^{\,U} - I_{IN}^{\,L})}{I_{DCi}\cosh(\alpha V_{ci})} \tag{4.27}$$

Step 6: Bear in mind the sign of a_{ij} and b_i and set $C_i\alpha_{ij}/\alpha=I_{oij}$ and $C_i b_i/\alpha=I_{bi}$ thus expressing the capacitor currents I_{capi} in (4.27) as the difference of two terms:

$$I_{capi} = I_{capi}^{\,U} - I_{capi}^{\,L} = \frac{\sum_{j=1}^{N} I_{oij} I_j^{\,U}{}_{\{a_{ij}>0\}} + \sum_{j=1}^{N} I_{oij} I_j^{\,L}{}_{\{a_{ij}<0\}} + I_{bi} I_{IN}^{\,U}{}_{\{b_i>0\}} + I_{bi} I_{IN}^{\,L}{}_{\{b_i<0\}}}{I_{DCi}\cosh(\alpha V_{ci})} - \frac{\sum_{j=1}^{N} |I_{oij}| I_j^{\,U}{}_{\{a_{ij}<0\}} + \sum_{j=1}^{N} |I_{oij}| I_j^{\,L}{}_{\{a_{ij}>0\}} + |I_{bi}| I_{IN}^{\,U}{}_{\{b_i<0\}} + |I_{bi}| I_{IN}^{\,L}{}_{\{b_i>0\}}}{I_{DCi}\cosh(\alpha V_{ci})} \tag{4.28}$$

Relation (4.28) expresses the capacitor currents needed for the realization of the transfer function of the SISO system described in (4.22) and (4.23) by means of class-AB Sinh integrators like the one shown in Figure 4.3. The numerator of each of the terms in (4.28) comprises only products of positive quantities. In other words, $I_{capi}^{\,U}$, $I_{capi}^{\,L}$ in (4.28) remain positive at all times and can thus be realized by a transistor current ensuring class-AB operation. Following a similar procedure to the one described above, it can also be shown that the output current (4.26) can be expressed as the difference of two positive current quantities.

In the proposed method, the specific filter signal flow graph (SFG) is realized by combining appropriately the two output phases from each of the integrators, as dictated by the prototype state-space (or SFG), thus creating the required capacitor currents given by (4.28) for the specific linear targeted response. The fact that each of the phases is a strictly positive current facilitates signal sign inversion (in difference mode).

The reader can confirm that the resulting high order ELIN Sinh filter topology will employ only one splitter block at the input. When state-currents are fed to subsequent stages,

a splitter is not necessary, since the two phases of the state currents are directly generated from the capacitor voltages by means of exponential transconductors. This would not be the case if the ELIN integrator of Figure 4.3 was directly substituted in the corresponding SFG.

Other positive features of the resulting topologies which employ the proposed synthesis path are: a) $\sinh^{-1}$ I_{IN}-to-V_{IN} blocks are not needed; consequently, the resulting topologies do not suffer from the inaccuracies (e.g. offsets) of the particular blocks which affect linearity, an issue difficult to avoid with standard Sinh mapping treatments which necessitate complementary blocks which employ both n- and p-type devices in a symmetrical about ground arrangement to perform the $\sinh^{-1}$ operation [227,246], although PMOS only $\sinh^{-1}I_{IN}$-to-V_{IN} blocks with good performance have been proposed [157] (Chapter 3) and b) the absence of tanh transconductors requiring non-linear (e.g. cosh type) tail currents [169,211,227] which both do not favour a high DR and intensify the optimization effort. It can be confirmed that the proposed synthesis path leads to topologies different from all those that would result from the reviewed methods in section 4.1, which for example can use only one device type in their TL loops if practical integrators such as the one presented in [154] are employed as building blocks.

The above Sinh filter synthesis procedure is best illustrated by means of the typical 2nd order state-space example codified by equations (4.1)-(4.4). When the state variable x_1 is chosen as output (i.e. $y=x_1$) then a BP response is realized. Choosing x_2 as output (i.e. $y=x_2$), a LP response is realized. Proceeding as explained before yields:

$$y_{BP} = I_1 = I_1^U - I_1^L \tag{4.29}$$

$$y_{LP} = I_2 = I_2^U - I_2^L \tag{4.30}$$

$$I_{cap1} = C_1 \dot{V}_{c1} = \frac{\overbrace{\frac{\omega_o}{Q}\frac{C_1}{\alpha} I_1^{\,L} + \frac{\omega_o C_1}{\alpha} I_2^{\,L} + \frac{\omega_o C_1}{\alpha} I_{IN}^{\,U}}^{I_{cap1}{}^{U}>0}}{I_{DC}\cosh(\alpha V_{c1})} - \frac{\overbrace{\frac{\omega_o}{Q}\frac{C_1}{\alpha} I_1^{\,U} + \frac{\omega_o C_1}{\alpha} I_2^{\,U} + \frac{\omega_o C_1}{\alpha} I_{IN}^{\,L}}^{I_{cap1}{}^{L}>0}}{I_{DC}\cosh(\alpha V_{c1})} \tag{4.31}$$

$$I_{cap2} = C_2 \dot{V}_{c2} = \frac{\overbrace{\frac{\omega_o C_2}{\alpha} I_1^{\,U}}^{I_{cap2}{}^{U}>0}}{I_{DC}\cosh(\alpha V_{c2})} - \frac{\overbrace{\frac{\omega_o C_2}{\alpha} I_1^{\,L}}^{I_{cap2}{}^{L}>0}}{I_{DC}\cosh(\alpha V_{c2})} \tag{4.32}$$

Figure 4.4 illustrates the block diagram of two Sinh CMOS integrators [154] (Chapter 3) appropriately interconnected in order to realize relations (4.29)-(4.32). It is assumed that $C_1=C_2=C$. The factor $\omega_o C/\alpha$ has dimensions of current and can be realized by means of a dc current I_o. Both the input current splitter and the output sinh/cosh transconductors are employing blocks where operation relies on the GML.

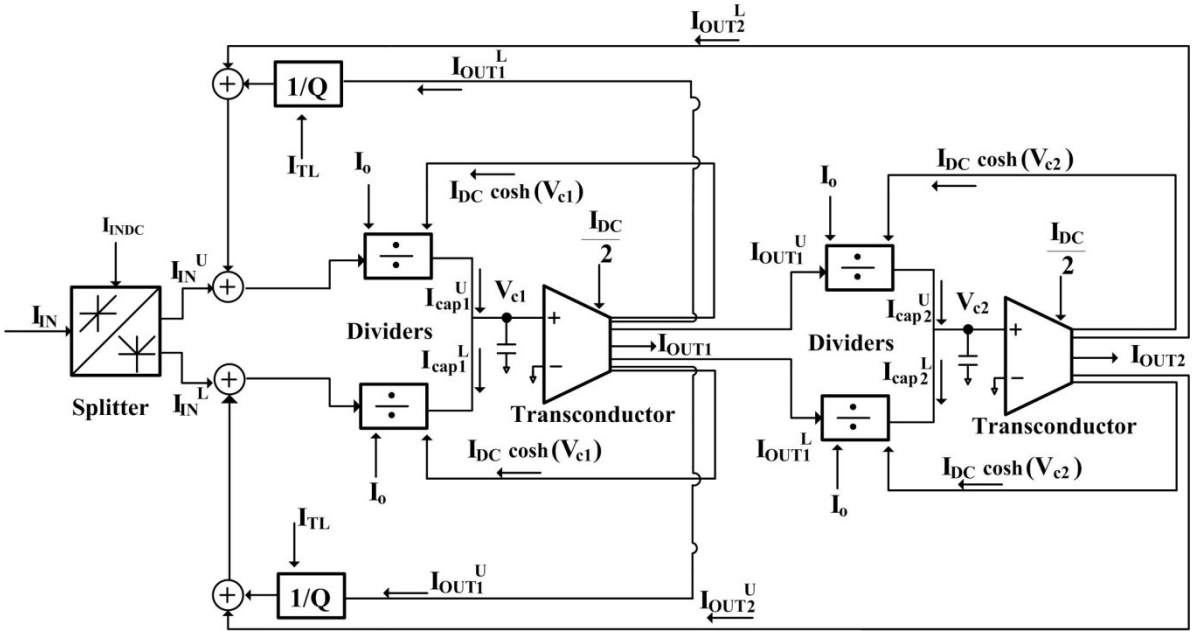


Figure 4.4: Block diagram of a practical CMOS Sinh biquad based on the integrator in [154]. The transistor level schematics for all blocks forming the biquad can be found in Chapter 3. The *1/Q* divider is implemented by means of a TL loop.

4.4 An 8Hz, 0.1μW, 110+ dBs CMOS Sinh Bessel filter for ECG processing

Filters of Bessel approximation are important [257-260] for the processing of bio-signals due to their property of delaying all frequencies by the same amount thus preserving the wave shape of the filtered signal. Despite the fact, they are not often incorporated in the analogue front end of ECG processing systems. Furthermore -as discussed in Chapter 1- with a few exceptions [147,260-261] the filters used in the front-end of fully integrated ECG systems, adopt the switched capacitor approach [146,148]. The suitability of Sinh CMOS filters for low frequency applications and in particular for ECG processing is investigated through the design of high order Bessel low pass filters by means of the synthesis method presented in section 4.3 and employing the practical all-PMOS Sinh integrator Figure 4.3 as building block.

4.4.1 Synthesis

A 3rd order Bessel filter was designed for a normalized 1s delay at DC and for flat group delay within 1% of its dc value up to 6Hz. The normalized transfer function for such a response is given as G(s) =15/ [s^3+6s^2+15s+15]. The denormalized transfer function stems from G(s) by substituting s for s*[1.3/(2$\pi f_{cut\text{-}off}$)] according to standard tables. Figure 4.11 illustrates the block diagram realisation of the desired transfer function by means of a pair of lossy integrators and a lossless one in a leapfrog configuration. It can be confirmed that (4.33) is realized by the Sinh block diagram of Figure 4.5. The capacitor current equations required to implement the 3rd order topology are summarized by equations (4.34)-(4.36). For the derivation of equations (4.34)-(4.36), refer to section 4.3. The block diagram of the Sinh topology is illustrated in Figure 4.11 where three tuning currents $I_{o1,}$ $I_{o2,}$ I_{o3} correspond to the first lossy, the second lossless and the 3rd lossy integrator respectively. With all three

integrator capacitors set equal to 50pF, I_{o1}=39.9pA, I_{o2}=181.26pA and I_{o3}=206.9pA, the topology of Figure 4.11 realizes the targeted Bessel response which is characterized by a group delay of 34.5ms.

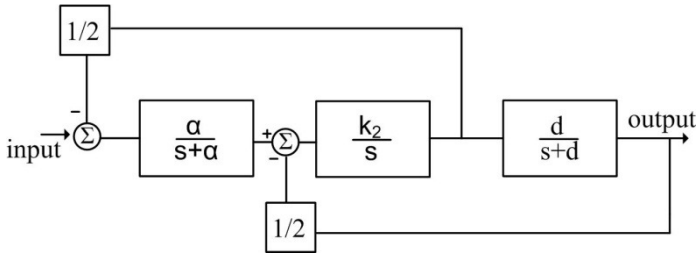


Figure 4.5: Block diagram of a leapfrog 3rd order low pass filter

$$H(s) = adk_2 / [s^3 + (a+d)s^2 + (ad + \frac{k_2(a+d)}{2}s + adk_2) \tag{4.33}$$

$$I_{c1} = \frac{I_{o1}(I_{out1}^{L} + \overbrace{\frac{I_{out2}}{2}}^{I_{c1}{}^{U}{}_{>0}}{}^{L}) + I_{o1}I_{IN}^{U}}{I_{DC}\cosh(aV_{c1})} - \frac{I_{o1}(I_{out1}^{U} + \overbrace{\frac{I_{out2}}{2}}^{I_{c1}{}^{L}{}_{>0}}{}^{U}) + I_{o1}I_{IN}^{L}}{I_{DC}\cosh(aV_{c1})} \tag{4.34}$$

$$I_{c2} = \frac{I_{o2}(I_{out1}^{U} + \overbrace{\frac{I_{out3}}{2}}^{I_{c2}{}^{U}{}_{>0}}{}^{L})}{I_{DC}\cosh(aV_{c2})} - \frac{I_{o2}(I_{out1}^{L} + \overbrace{\frac{I_{out3}}{2}}^{I_{c2}{}^{L}{}_{>0}}{}^{U})}{I_{DC}\cosh(aV_{c2})} \tag{4.35}$$

$$I_{c3} = \frac{I_{o3}(I_{out2}^{U} + \overbrace{I_{out3}^{L}}^{I_{c3}{}^{U}{}_{>0}})}{I_{DC}\cosh(aV_{c3})} - \frac{I_{o3}(I_{out2}^{L} + \overbrace{I_{out3}^{U}}^{I_{c3}{}^{L}{}_{>0}})}{I_{DC}\cosh(aV_{c3})} \tag{4.36}$$

4.4.2 **Simulated results**

The 3rd order low pass Bessel filter was synthesized in Cadence IC Design Framework and simulated using commercially available 0.35μm AMS CMOS process parameters. All PMOS devices were sized 60μm/1μm apart from the devices of the dividers; the upper transistors were sized 5μm/9μm and the lower 120μm/0.35μm. The level shifters (devices Q_{5a} and Q_{6a} of the transconductors, see Chapter 3) had sizes 4μm/12.5μm. All NMOS devices were sized 25μm/1μm apart from the mirror that carries the capacitor current I_{cap2} which was sized 1μm/20μm. The gain factor 1/2 is obtained by sizing the required transistors to half the width value of the ones carrying the split phases of the output current to the previous stage (see Figure 2). All I_{DC} currents were set to $2*I_o$ while the splitter's I_{INDC} to 0.01nA to minimize the power consumption. This biasing choice does not affect the performance of the circuit thanks to the decoupled nature of the splitter from the rest of the circuit. Finally The dc current I_{bias} of the level shifter was set to 10nA.

Frequency Response: Figure 4.6 illustrates confirming simulation results in the frequency domain. Observe the very good agreement between simulated and theoretically predicted responses both for the magnitude and phase response of the filter. Referring to Figure 4.7, the filter exhibits the anticipated group delay value of 34.5ms at dc and deviates less than 1% from this value up to the frequency of 6Hz. Figure 4.8 presents indicative frequency-domain responses tuned to different cut-off frequencies by varying the value of the current I_o. For I_o varying from 20pA to 620pA the 3dB frequency varies from 4-120 Hz respectively. Figure 4.9 illustrates the Monte Carlo simulation results up to 1000 runs: The group delay error [GD(DC)-GD(6Hz)] normalized to GD at dc exhibits 0.53% standard deviation (Std).

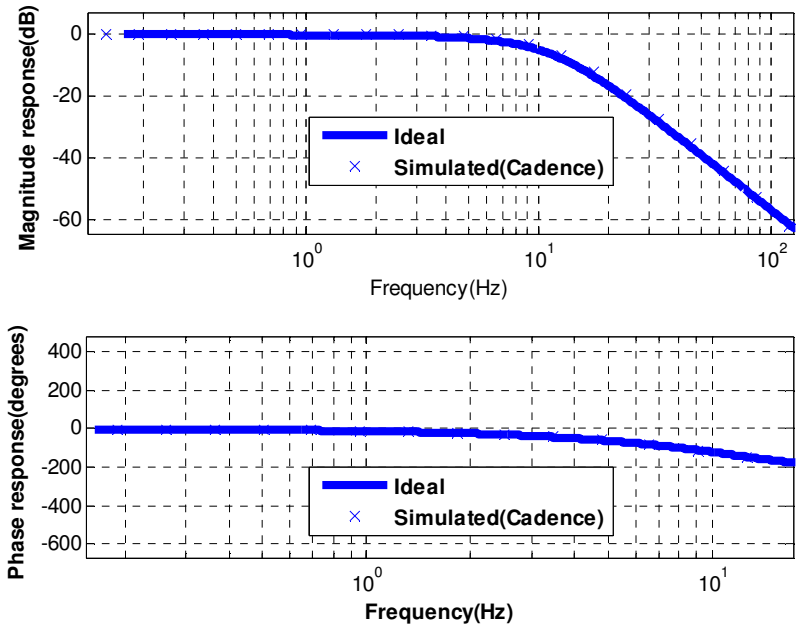


Figure 4.6: Simulated and ideal AC small signal frequency responses of the 3rd order Sinh Bessel filter.

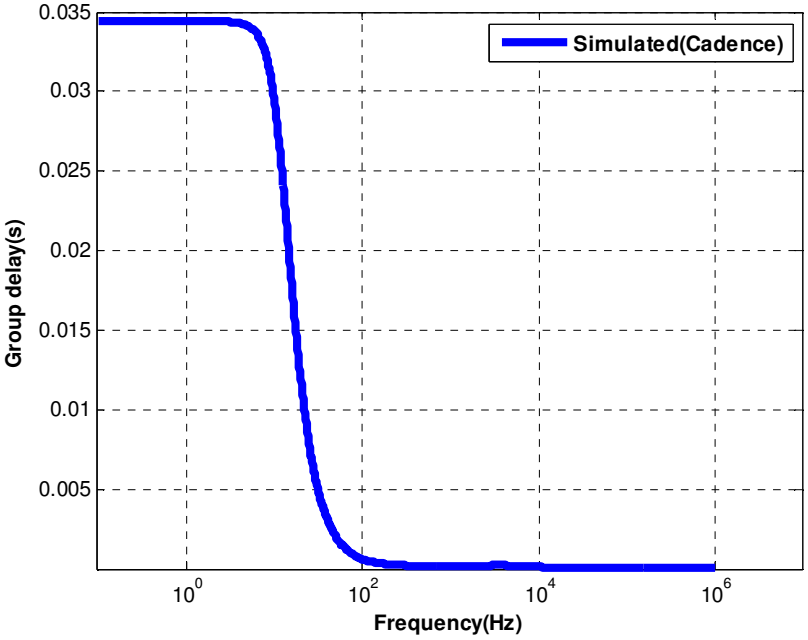


Figure 4.7: Group delay of the 3rd order Sinh Bessel filter (<0.1% deviation of the nominal group delay of 34.5 ms (dc) up to 6Hz).

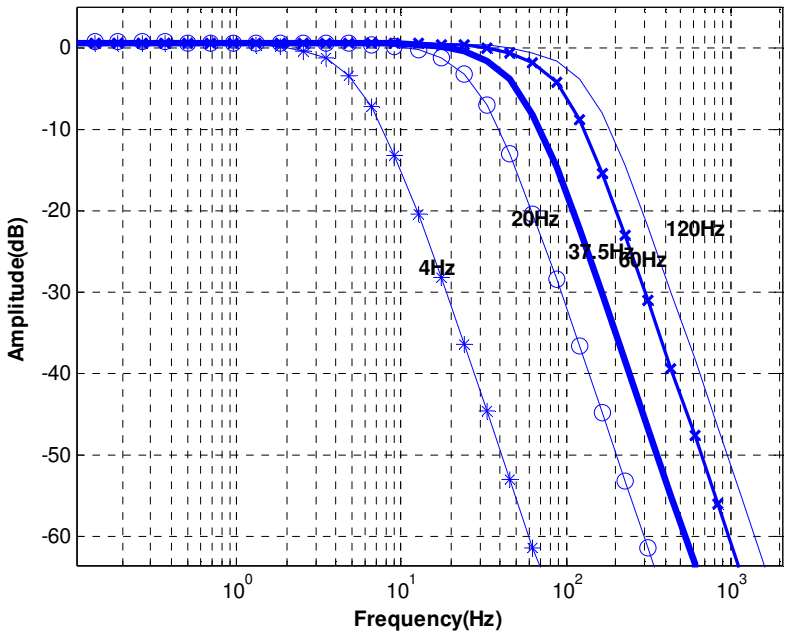


Figure 4.8: Tuning of the cut-off frequency (by means of I_o) ranging from 4 to 120Hz (and likely to be used in ECG front-end low pass filters) is achieved.

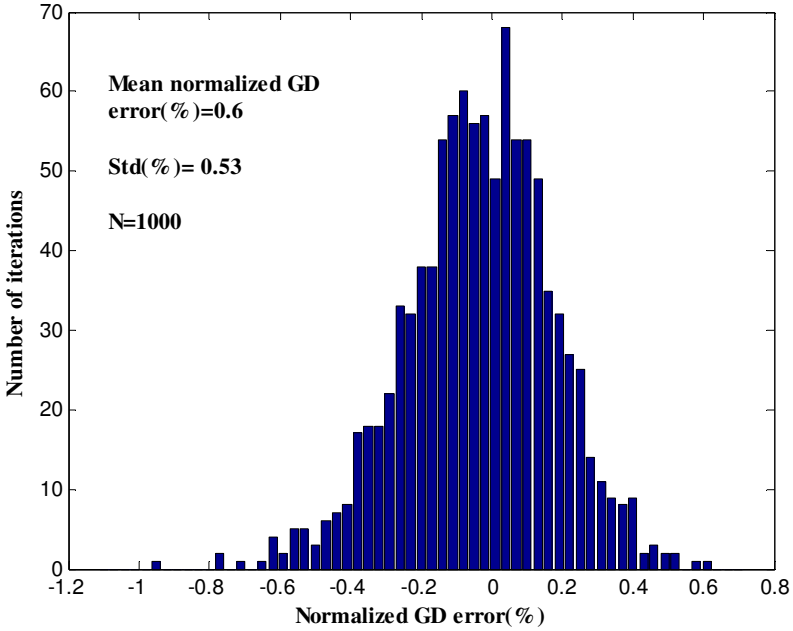


Figure 4.9: Variation of the normalized group delay error (GD (DC)-GD (6Hz) to the group delay at dc (34.5ms).

Linearity, Noise, Dynamic Range: The Sinh integrator building blocks of the filter have been optimized for the low I_o values dictated in turn from the low cut-off frequency values. The interested reader can confirm that had the optimization in [154,157] been adopted, for the current filter, the overall output would exhibit a noticeable offset linked to a voltage offset appearing at the capacitor node. In general it has been confirmed that when low I_o values are needed, the bias currents of the circuit should adjust accordingly to similar low levels. This empirical observation is also true for logarithmic CMOS filters which also rely on the exponential behaviour of weakly inverted MOS devices [262]. Figure 4.10 reports the THD (%) for single input tones at 5,8,10 and 15Hz. The filter is tested at those frequencies because they contain useful information of the ECG signal (the peak of the QRS complex lies in the 10-15Hz frequency range [107]). Observe that for modulation index values up to 1000, the THD remains below 1%. Table 7 summarizes the performance of the filter.

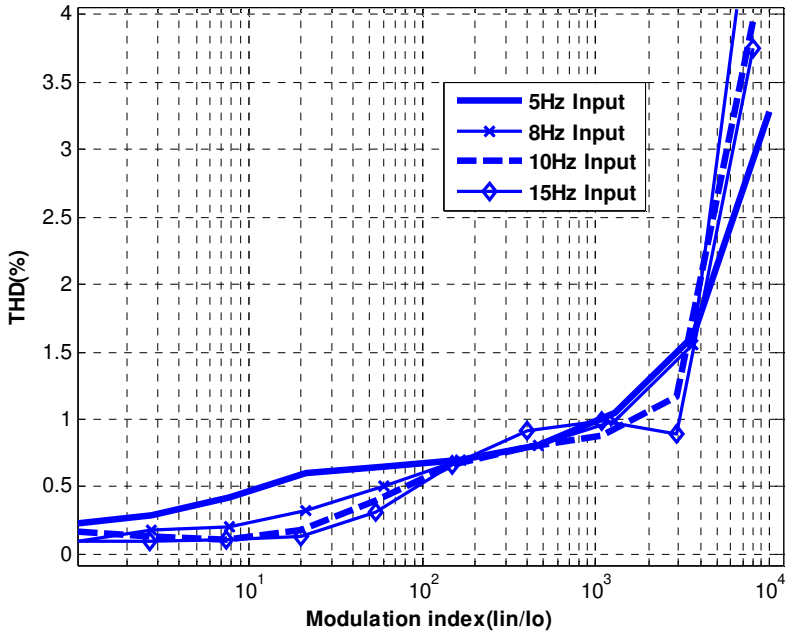


Figure 4.10: Total harmonic distortion (THD) versus modulation index (M.I. $m=I_{in}/I_o$) for the 3rd order Bessel filter. THD is tested for input sinusoids at frequencies within the ECG spectrum.

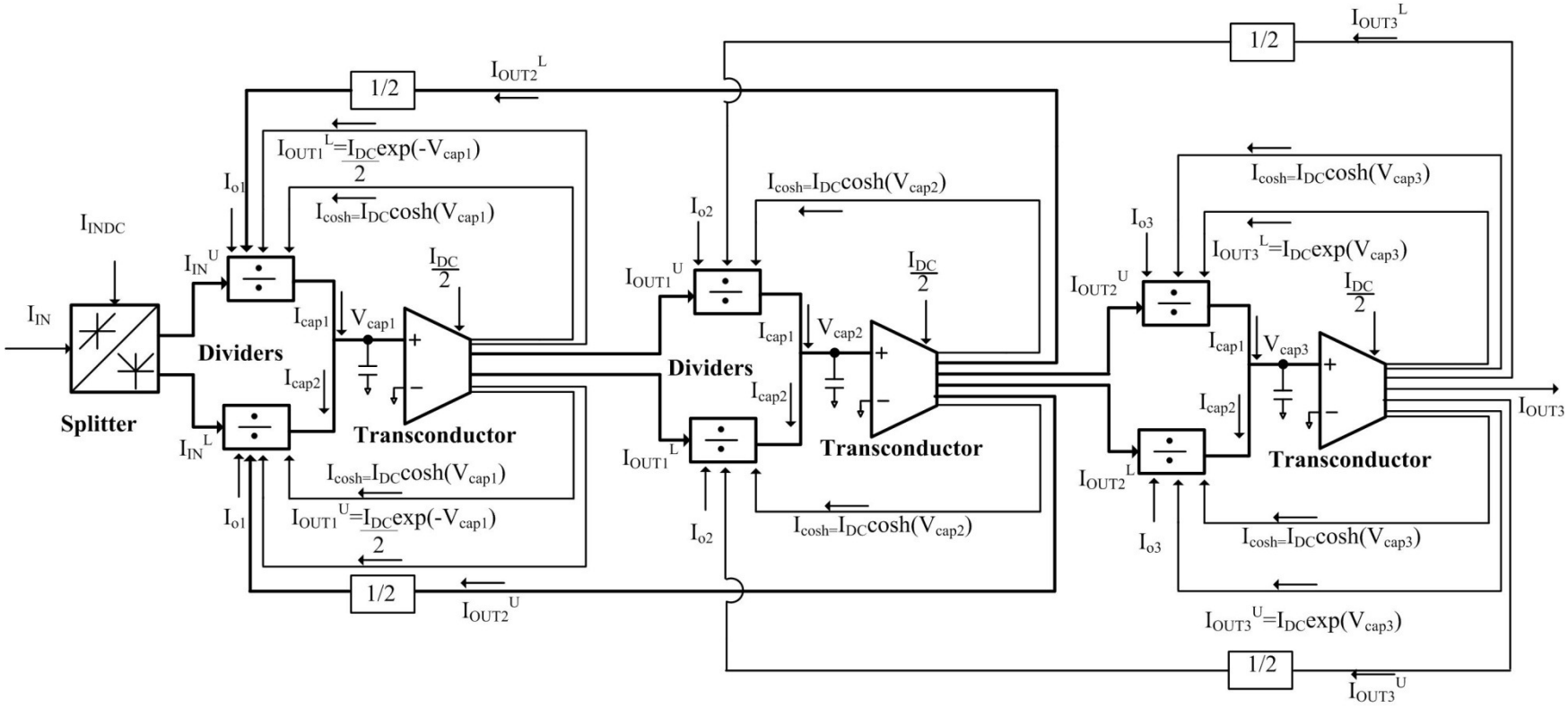


Figure 4.11: Block diagram of the 3rd order Sinh Bessel filter comprising a pair lossy Sinh integrators and a lossless one.

For the transistor level implementation of each building block refer to Chapter 3.

4.5 A 6th order low pass CMOS Sinh Bessel filter

The performance of a 2.4Hz 6th order Bessel filter built by cascading two 3rd order Bessel filters like the one described in 4.4.2 is investigated here. Table 7 compares its performance with that of a 6th order Bessel of the same cut-off frequency reported in [260], which was designed for similar applications and implemented by means of the G_m-C approach: with the capacitors set equal to 20pF each (see Figure 4.12) and a total static power consumption almost ten times lower than that reported in [260], the Sinh filter exhibits similar or better dynamic range. Increasing the capacitor value to 50pF each (total of 300pF) improves noticeably the linearity levels for modulation indices higher than 1000 (see Figure 4.12). Referring to Table 7 again note the much smaller chip area occupied by the Sinh filter. Figure 4.13 illustrates the output of the filter when artificial [148] ECG signals contaminated with various noise sources are fed into Cadence by means of a piecewise linear current source.

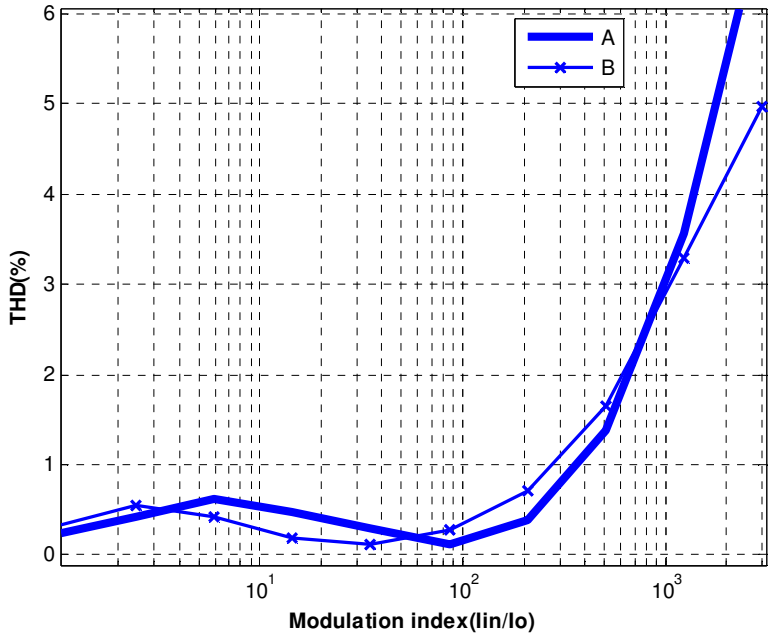


Figure 4.12: THD versus M.I. for the 2.4Hz 6th order Bessel filter wthen the input tone at 0.5Hz. A: Corresponds to C=20pF (total=120pF), I_o=8pF, I_{dc}=5nA, B: Corresponds to C=50pF (total=300pF), I_o=0.016nA, I_{dc}=5nA.

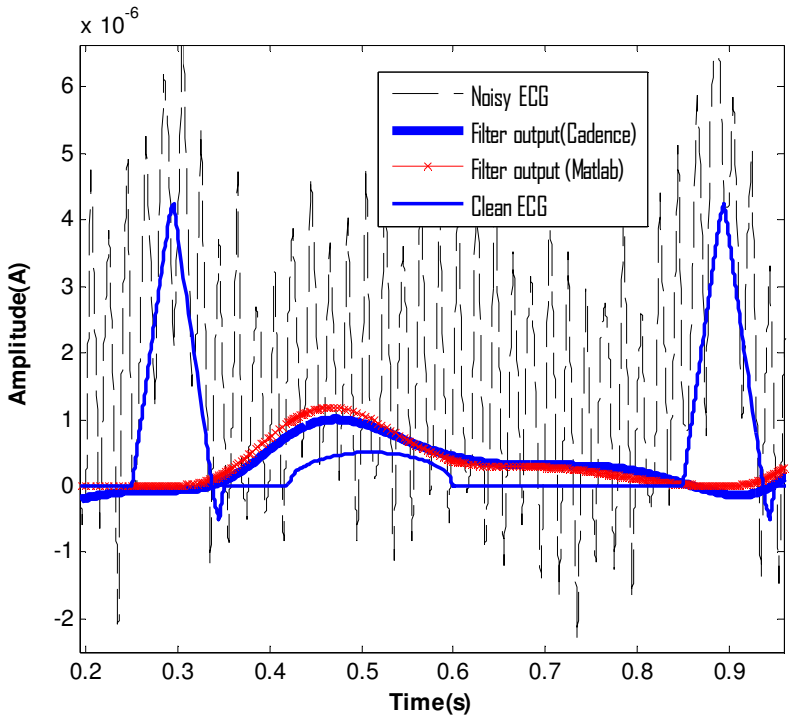


Figure 4.13: Artificial ECG [148] signal contaminated with base line wander and motion artefacts at 5% of the peak of QRS of the clean signal (4mV) and by mains noise and EMG artefacts at 50% of the QRS peak. Noisy ECG (5s duration, 72bpm) was fed as input. The MatLab™ filter response and the Cadence output of the 6th order Bessel filter (F_{cut}= 2.4Hz) is illustrated. The first period of the signal is illustrated for clarity). The clean ECG is also featured in order to indicate the sensing of the T-wave.

Table 7: Simulated performance of the 3rd and 6th order CMOS Sinh Bessel topologies.

Filter	[260]	This work	This work
Technology	0.8µm	0.35µm	0.35µm
Order	6th	6th	3rd
Bandwidth (Hz)	2.4	2.4	8
Total Cap. (pF)	N/A	120-300	150
Chip area (µm^2)	1000	0.14-0.34	0.17
Power supply (V)	±1.5	±1	±1
DR@0.5Hz (dB)	60(1%THD)	66(4%THD	117(4%THD)
Static Power (µW)	10	1.5	0.1
Group delay error	N/A	0.2%	0.1% (<6Hz)
Input Noise Floor over BW(3dB)	50 µV	16pA	0.54pA
Measured	YES	NO	NO

4.6 A 5th order CMOS Sinh low pass Chebyshev filter

4.6.1 Synthesis

A 5th order CMOS Sinh Chebyshev all-pole filter with 1dB pass band ripple was designed from its LC ladder prototype. Following the method described in Section 4.3 and using equation (4.28), the 5th order Chebyshev with the transistor-level diagram shown in Figure 4.24 is synthesized. The capacitor current relations needed for the realization of the Chebyshev response are summarized in equations (4.37)-(4.41).

All PMOS devices were sized 60µm/1µm with the exception of the shifters which were sized 1µm /120µm and the devices of the dividers which were optimized to 40µm /1µm for the upper and 100µm/1µm for the lower devices accordingly. All devices of the NMOS mirrors were set to 24µm/1µm with the exception of the mirrors sourcing the lower phase of the capacitor current which were optimized to an aspect ratio of 1µm/24µm. The I_{DCi} and I_{biasi} currents of the Sinh/Cosh transconductor of each integrator comprising the 5th order filter were set to 1nA. The I_{oi} currents which in combination with the capacitor values determine the cut-off frequency have all chosen to be equal to 1nA. The corresponding capacitor values for the 5th order Chebyshev with 1dB pass band ripple and cut-off at 100Hz have been calculated as*:* $C_{1,5}$=105.6pF, $C_{2,4}$=53.9pF and C_3=148.5pF.

$$I_{c1} = \frac{\overbrace{I_{o1}(I_{out1}{}^{L} + I_{out2}{}^{L}) + I_{o1}I_{IN}{}^{U}}^{I_{c1}{}^{U}>0}}{I_{DC}\cosh(aV_{c1})} - \frac{\overbrace{I_{o1}(I_{out1}{}^{U} + I_{out2}{}^{U}) + I_{o1}I_{IN}{}^{L}}^{I_{c1}{}^{L}>0}}{I_{DC}\cosh(aV_{c1})} \tag{4.37}$$

$$I_{c2} = \frac{\overbrace{I_{o2}(I_{out1}{}^{U} + I_{out3}{}^{L})}^{I_{c2}{}^{U}>0}}{I_{DC}\cosh(aV_{c2})} - \frac{\overbrace{I_{o2}(I_{out1}{}^{L} + I_{out3}{}^{U})}^{I_{c2}{}^{L}>0}}{I_{DC}\cosh(aV_{c2})} \tag{4.38}$$

$$I_{c3} = \frac{\overbrace{I_{o3}(I_{out2}{}^{U} + I_{out4}{}^{L})}^{I_{c3}{}^{U}>0}}{I_{DC}\cosh(aV_{c3})} - \frac{\overbrace{I_{o3}(I_{out2}{}^{L} + I_{out4}{}^{U})}^{I_{c3}{}^{L}>0}}{I_{DC}\cosh(aV_{c3})} \tag{4.39}$$

$$I_{c4} = \frac{\overbrace{I_{o4}(I_{out3}^{\ U} + I_{out5}^{\ L})}^{I_{c4}U_{>0}}}{I_{DC}\cosh(aV_{c4})} - \frac{\overbrace{I_{o4}(I_{out3}^{\ L} + I_{out5}^{\ U})}^{I_{c4}L_{>0}}}{I_{DC}\cosh(aV_{c4})} \tag{4.40}$$

$$I_{c5} = \frac{\overbrace{I_{o5}(I_{out4}^{\ U} + I_{out5}^{\ L})}^{I_{c5}U_{>0}}}{I_{DC}\cosh(aV_{c5})} - \frac{\overbrace{I_{o5}(I_{out4}^{\ L} + I_{out5}^{\ U})}^{I_{c5}L_{>0}}}{I_{DC}\cosh(aV_{c5})} \tag{4.41}$$

4.6.2 **Simulated results**

The Sinh 5th order Chebyshev topology of Figure 4.24 was simulated using Cadence IC Design Framework (IC 5.1.4.1, Hit-Kit version: 3.70) and the commercially available 0.35μm AMS CMOS process parameters. Moreover, the Sinh topology was compared head-to-head with a 5th order pseudo-differential Class-AB CMOS Log-domain implementation corresponding to the same specifications. For the design of the Log-topology, two class-A 5th order Chebyshev filters were designed using the Bernoulli cell approach [183,262]. The two class-A branches were then subtracted to obtain the class-AB output as shown in Figure 4.25. It is worth noting that the two class-A WI Log-filters do not employ any E- Log-domain cells; the realization of the conditions which would necessitate impractical (when in CMOS WI) E- cells are achieved by means of simpler (than E- cells) and practical WI four-transistor TL loops. The measured results from a CMOS class-A Log domain filter of Bessel approximation are presented in [262] and prove the validity of this approach in WI. All PMOS devices have been sized 60μm/1μm and all NMOS mirrors 24μm/1μm. The devices of the dividers have also been sized as their counterparts in the Sinh topology. The I_{Qi} currents which provide the loss at the first and last cell of the Bernoulli backbone have been set to 1nA. The dc current of the splitter at the input of the filter is set to 1nA as in the Sinh topology and the I_{Bi} and I_{oi} currents are set equal to 1nA. The values of the capacitors are the same as in the Sinh filter.

Frequency Response: Both small signal AC and large signal PAC analyses were performed in order to investigate the filter responses. Figure 4.14 shows the almost three orders of magnitude that the cut-off frequency of the Sinh topology can be tuned by varying I_o from 0.1nA to 100nA with the capacitor values fixed. Note the close agreement of the simulated response at 100Hz with that of the ideal MatLab™ response of a 5th order low pass Chebyshev filter. The pass band ripple exhibits a slight peaking as the frequency is tuned towards higher cut-off values. For the filter tuned at 100Hz, the pass band ripple behaviour deviated from the ideal 1dB pass band ripple only by 2%. The deviation from the pass band ripple behaviour is slightly smaller for the Log-topology, however, the tuning range of the Log-topology is found to be less than that of the Sinh (see Figure 4.15). Figure 4.16 shows the frequency response obtained from PAC analysis for various *m* values when the filter is tuned at 100Hz and for an input in the pass band (at 10Hz). Note that the response of the filter resembles the ideal behaviour even for large *m* values.

Total Harmonic distortion (THD): Figure 4.17 and Figure 4.18 depict the THD[10] versus increasing input amplitude for various input frequencies for the Sinh and Log topologies accordingly. Note that both topologies achieve THD below 4% for large *m* values for most frequencies. Deep in the pass band the Log topology exhibits slightly lower distortion.

Dynamic Range (DR), Signal-to-Noise-Ratio (SNR) and Signal-to-Noise-plus-Distortion-Ratio (SNDR): In ELIN structures the noise increases with the amplitude of the input signal and consequently SNR and DR differ [156]. Figure 4.20 and Figure 4.21 were obtained by performing single-tone P-Noise and PSS simulations deep in the pass band (5Hz) and at 1/5 of the cut-off frequency (100Hz) for both topologies. Distortion power was calculated by adding the harmonic powers up to the 5th. Note that the noise increases linearly

[10] THD has been calculated by taking into account harmonics up to the 5th

with the power of the fundamental resulting in a constant SNR of about 60dB for m>10 for the Sinh topology and 63dB for the Log-topology accordingly. The DR on the other hand reaches at 122dB for the Sinh compared to 72dB for the Log topology. Observe that the noise starts at a lower value for the Log topology, but the distortion, on the other hand, rises to 4% faster for the Log rather than the Sinh, which explains the better DR figure the latter achieves. This can be better visualized in Figure 4.19 where the SNR and SNDR figures for an input sinusoid at 20Hz are illustrated for both topologies. Note that both SNR and SNDR start from the same value for small signals for both topologies. This corresponds to 22dB for the Sinh and 34dB for the Log filter. The SNR curve then keeps increasing for both topologies until m=10 and then becomes almost constant for three decades of m for both topologies with the Log SNR outperforming that of the Sinh by almost 3dB. This is attributed to the better noise performance of the Log filter. On the other hand, although the SNDR for small m values (class-A) is better for the Log, soon after the input becomes greater than m=1(i.e. onset of class-AB), the SNDR of the Log topology begins to decrease at a higher rate than its Sinh counterpart and ends up saturating to a value of 20dB for m>100 which is by 10dB less than what the Sinh topology achieves.

Table 8 summarizes the main comparative simulation results between the 5^{th}-order Chebyshev Sinh and Log topologies. Observe the higher input DR for the Sinh deep in the pass band. Also the Sinh topology uses only half the capacitor chip area, but its power consumption is 2.4 times higher than its Log counterpart.

Mismatch: Two worst case Monte-Carlo simulations were also performed to assess the effects of both process and mismatch variations on the 3dB bandwidth of the filter. Figure 4.22 and Figure 4.23 show respectively the f_o distributions for 400 runs for both topologies. It can be observed that the Log topology exhibits a slightly lower standard deviation.

Table 8: Sinh versus Log 5th-Order Chebyshev Simulated Results.

Simulated results (f_o=100Hz) 1dB ripple		
5th order Chebyshev (LP) Topology	Sinh	Log
Power consumption (nW)	297	119
Power supply (V)	±1	±1
Simulated pole frequency(f_o) (Hz)	100.5	96.7
Total capacitance (pF)	467.5	935
Deviation from nominal f_o (%)	0.5	3.3
Deviation from pass band ripple of 1dB (%)	2	1.8
Integrated input referred noise floor (pA)	5.6	1.8
Input DR @ 1/100(ω_o) (THD=4%) (dB)	138	130
Input DR @ 1/10(ω_o) (THD=4%) (dB)	138	120
Input DR @ 1/3(f_o) (THD=4%) (dB)	88	74
Input DR @ 2/3(f_o ω_o) (THD=4%) (dB)	107	124
Input DR @ ω_o (THD=4%) (dB)	105	134
SNR @ 20Hz for m>10 (dB)	56-64	62-64
SNDR @ 20Hz for 100<m<1000 (dB)	30	20

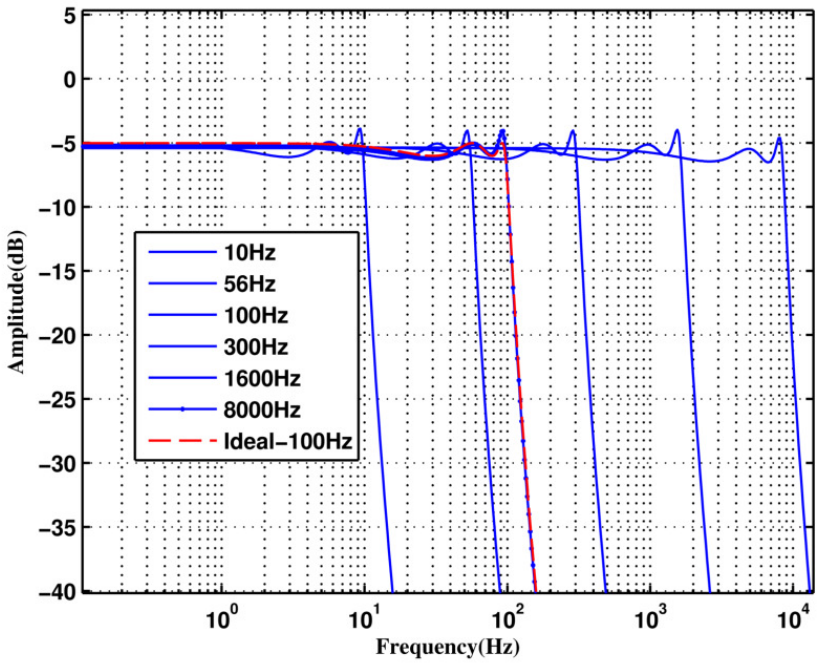


Figure 4.14: Small-signal AC Analysis – Sinh 5th order low pass Chebyshev tunability by means of I_o. The simulated response for f_o=100Hz coincides with the ideal one, calculated in MatLab™.

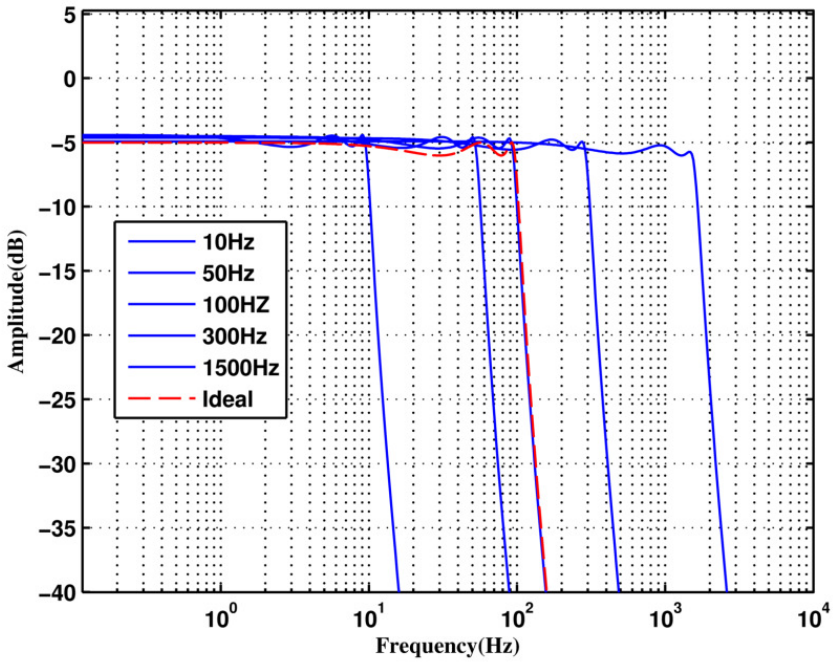


Figure 4.15: Small-signal AC Analysis – Log 5th order low pass Chebyshev tunability by means of I_o. The simulated response for f_o=100Hz coincides with the ideal one, calculated in MatLab™.

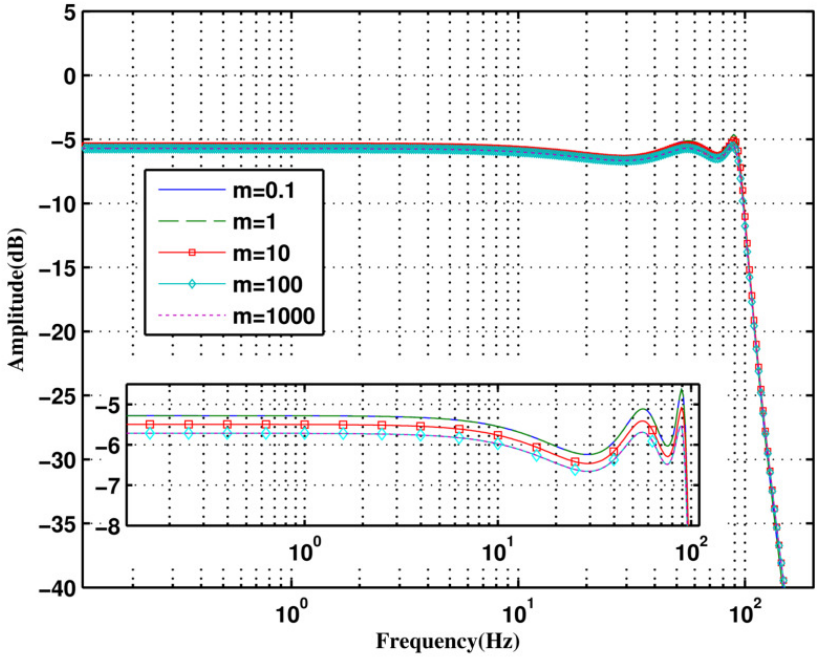


Figure 4.16: PAC-Analysis – Frequency response of the Sinh topology with varying *m* and the input tone at 10Hz. The area of the pass band is zoomed in to illustrate the detail of the passband ripple.

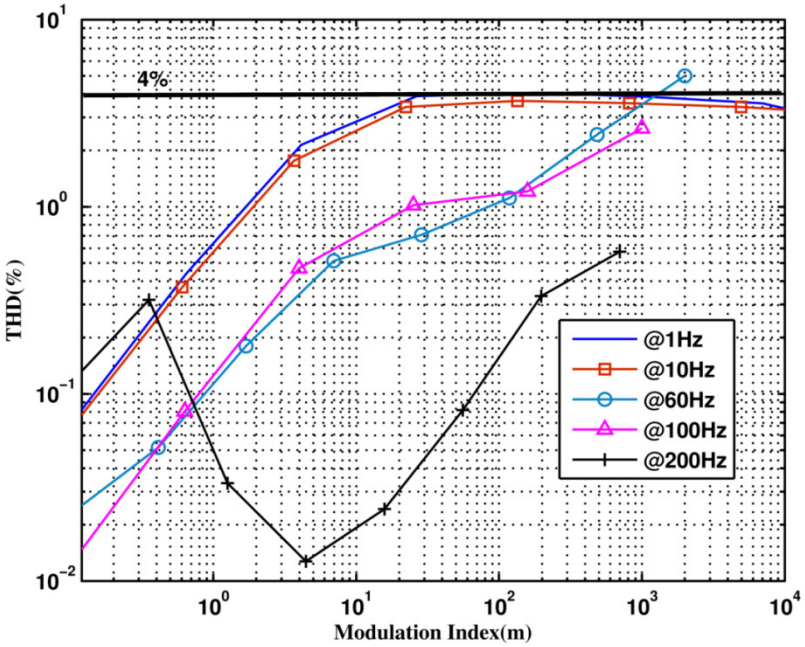


Figure 4.17: THD versus *m* for the 100Hz Sinh topology for input tones in the passband, cut-off and stopband.

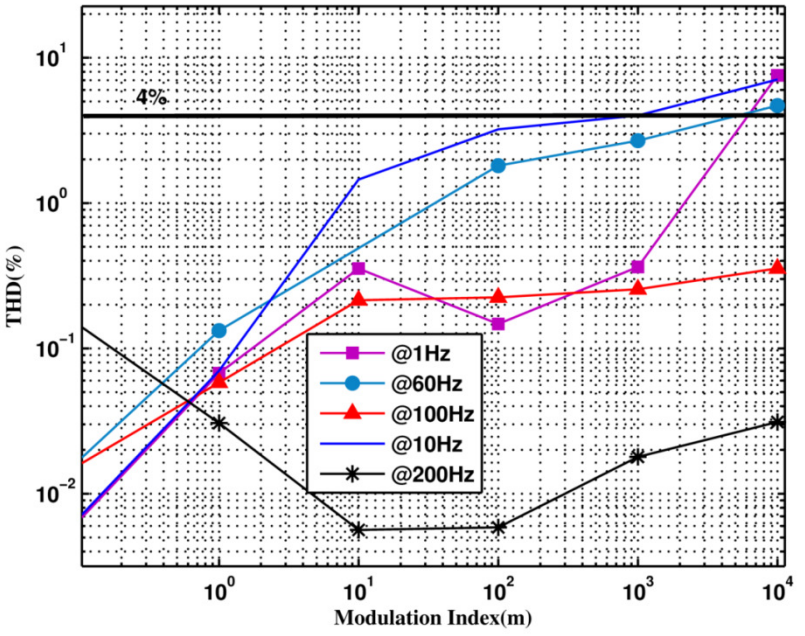


Figure 4.18: THD versus *m* for the 100Hz Log topology for input tones in the pass band, cut-off and stop band.

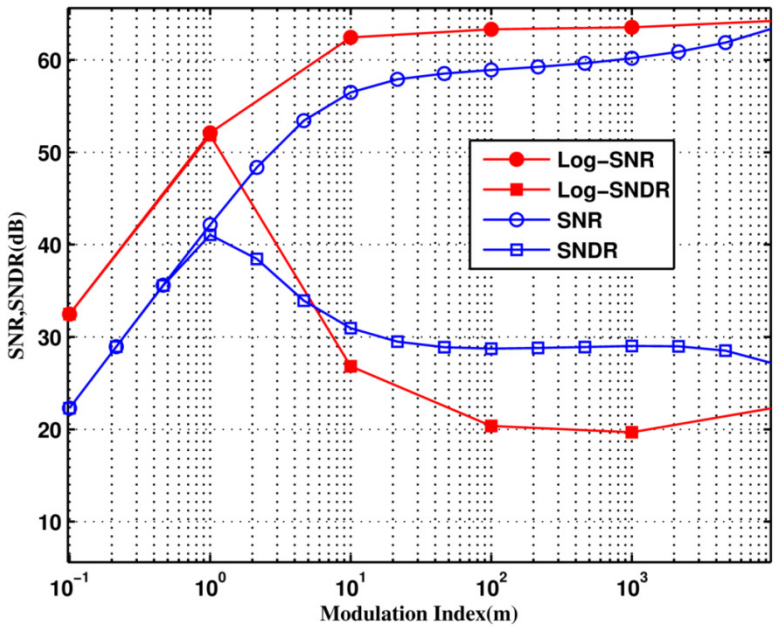


Figure 4.19: PSS and P-Noise Analysis – SNR and SNDR vs. *m* for both topologies with an input tone at 20Hz.

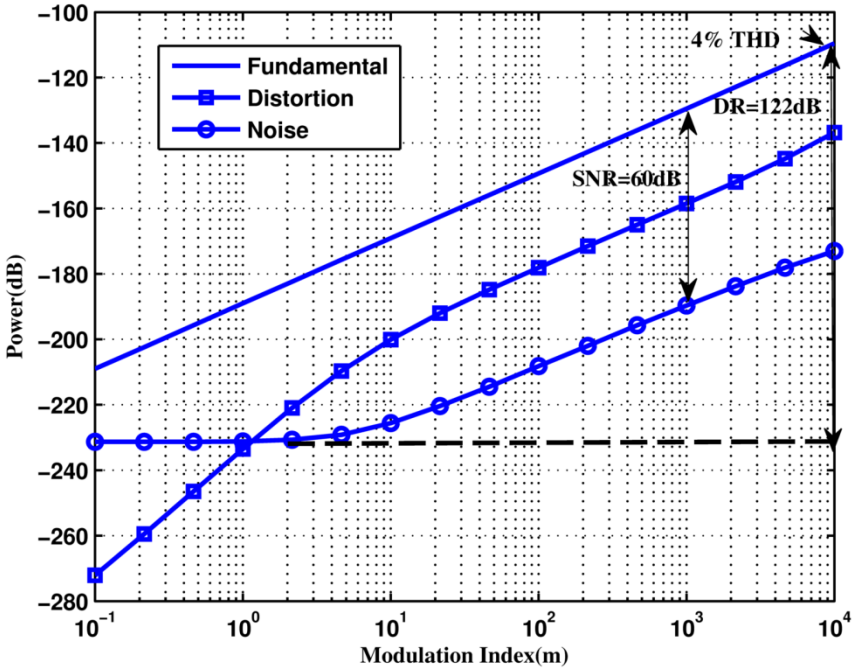


Figure 4.20: PSS and P-Noise Analyses – Fundamental, noise floor and total output distortion vs *m* for the Sinh topology. Power levels are referred to a load of 1Ω and the input tone is at 20Hz.

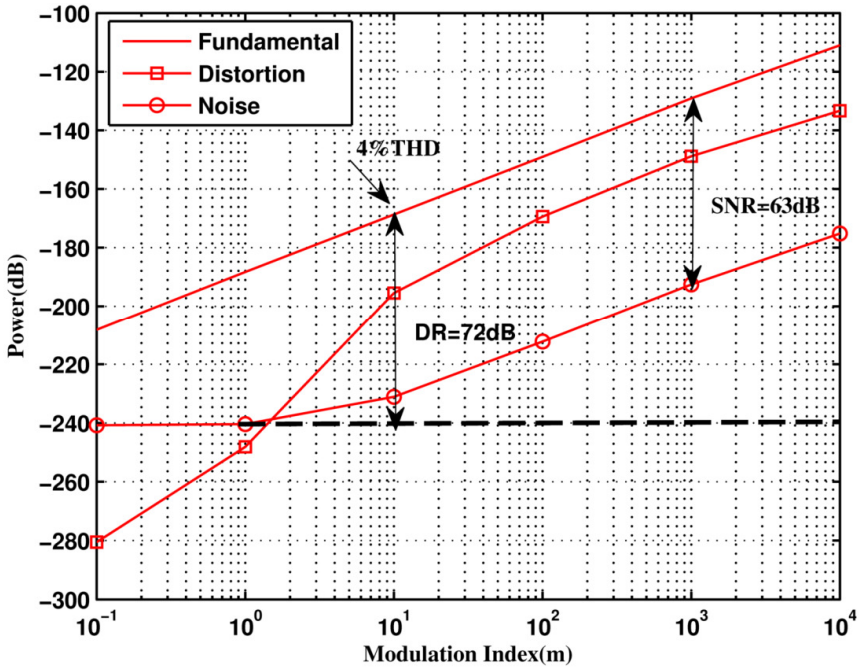


Figure 4.21: PSS and P-Noise Analyses – Fundamental, noise floor and total output distortion vs *m* for the Log topology. Power levels are referred to a load of 1Ω and the input tone is at 20Hz.

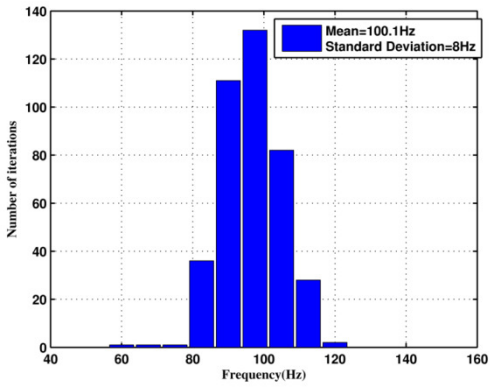


Figure 4.22: Small–signal AC Monte-Carlo analysis showing the Sinh 5th order Chebyshev pole frequency (f_o) distribution for 400 runs. The nominal value of f_o was set equal to 100Hz.

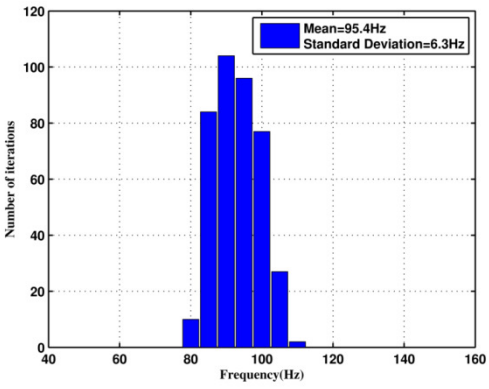


Figure 4.23: Small–signal AC Monte-Carlo analysis showing the Log 5th order Chebyshev pole frequency (f_o) distribution for 400 runs. The nominal value of f_o was set equal to 100Hz

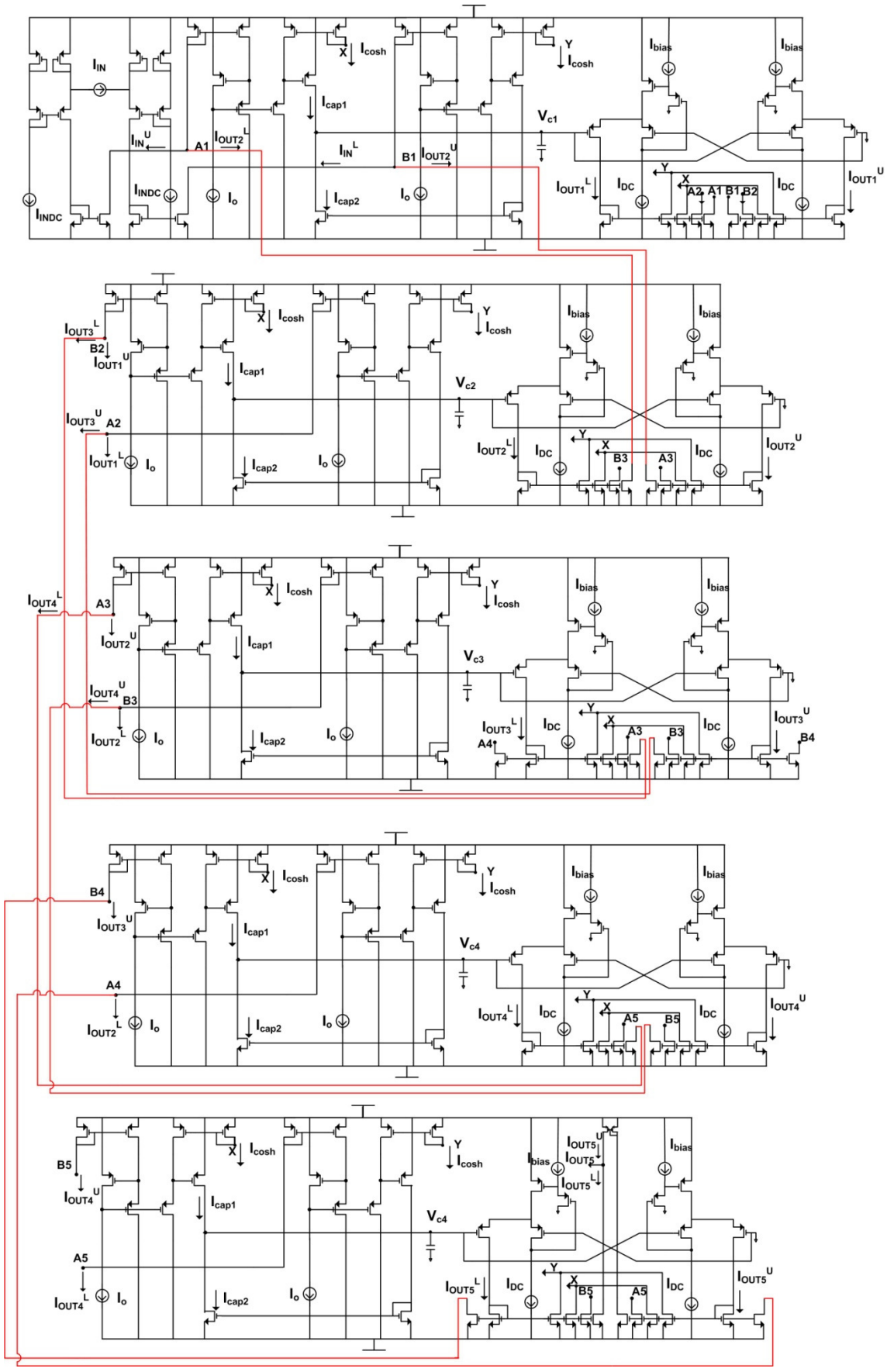


Figure 4.24: The transistor level diagram of the 5th order Sinh Chebychev filter with 1dB pass band ripple.

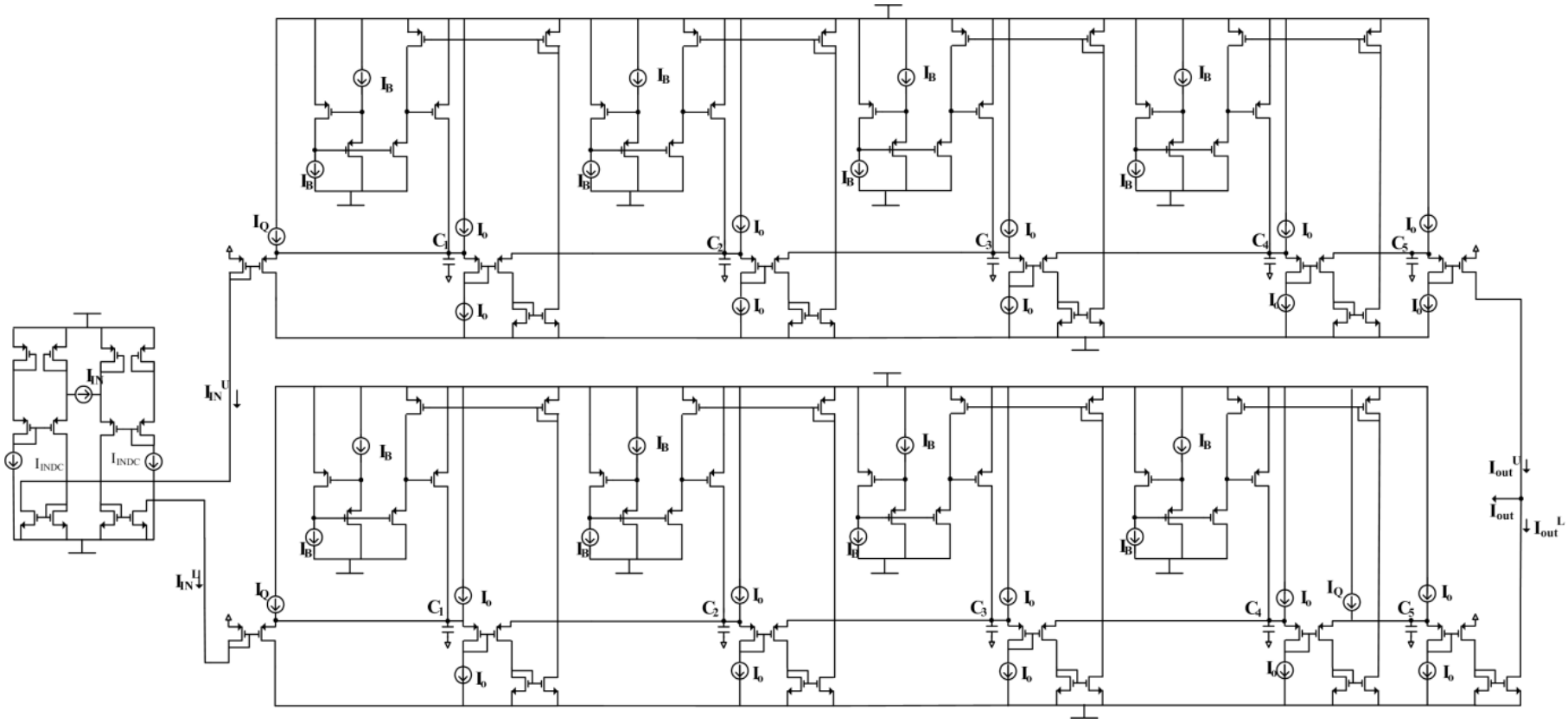


Figure 4.25: Transistor level design of the 5th order class-AB pseudo-differential Log-Domain 5th order Chebyshev filter implemented based on the Bernoulli-cell method and without any E- cells.

4.7 Conclusion

Recognising that no other synthesis method can lead to the systematic design of practical high order Sinh topologies, a distinct path for the synthesis of high order Sinh filters has been presented. The proposed methodology has been demonstrated through the synthesis of high order Sinh topologies which differ from the ones derived by means of existing synthesis approaches. The method is tailored for the synthesis of original circuit blocks comprising only p-type devices in their TL loops. The synthesis of a biquadratic Sinh filter has been presented in detail. Moreover, a 3rd order leapfrog low pass filter of Bessel approximation has been designed and it is dedicated to low frequency ECG processing. The design and detailed simulation results of the CMOS Sinh 3rd order Bessel, class-AB filter have been presented. Two 3rd order filters were cascaded to implement a 6th order Bessel with flat group delay up to 2.4Hz. The 6th order filter consumes 1.5μW and exhibits a dynamic range of 59-66dB. The 3rd order filter, exhibits a dynamic range of 95dB for 1% THD and more than 110dBs for 4% THD. Finally, a 5th order CMOS Sinh filter of Chebyshev approximation has been designed based on the operational simulation of an LC ladder prototype for a cut-off frequency of 100Hz and a 1dB pass band ripple. It exhibits a good - both large and small signal- frequency response. The head-to-head comparison with its pseudo-differential class-AB Log domain counterpart of the same specifications has confirmed that Sinh filters can achieve moderate SNR values of the order of 60dB, like their Log counterparts, and SNDR values greater by up to 10dBs. On the other hand the Log-domain filters (of the particular structure that has been used for the comparison presented here), enjoy a simpler design (less transistors), have lower power consumption by approximately 2.4 times from the same power supply (±1V) and are slightly less sensitive to process parameter and mismatch variations. In other words, when compared with class-AB Log-filters, high-order Sinh CMOS filters seem to constitute a solution of lower capacitor

area, similar or better SNR, SNDR and mismatch performance at the expense of higher power consumption.

Having presented a) a practical Sinh integrator building block which has been thoroughly studied b) a systematic synthesis method for high order filters tailored to the use of building blocks comprising only one type of devices such as the aforementioned integrator, c) a number of high order CMOS Sinh topologies synthesized by means of the proposed systematic method exhibiting excellent simulated performance (+100dB DR and μ-power consumption) and d) a simulation study which compares a high order Sinh topology with its pseudo-differential counterpart (an also novel Log topology), the reader should have been convinced of the potential of the Sinh filtering paradigm. The practical performance of high order CMOS Sinh topologies is presented in the following Chapter.

5 A high order 10Hz-1kHz CMOS Sinh 8th order notch filter for 50/60Hz

The aim of this Chapter is to evaluate the practical performance of Sinh topologies through an example that has been designed to fit the scope of the specifications required for the front-end processing of WBANs. More specifically, an 8th order notch filter based on 10 modified (universal 1st order filters) Sinh integrators, presented in section 3.2.1, has been fabricated in the 0.35μm CMOS technology and its practical performance is evaluated here. Measured results from high order CMOS inherently class-AB Sinh filters are presented in this work for the first time. The notch filter is dedicated to the rejection of 50/60Hz noise from bio-signals processed in a commercial WBAN product (Toumaz Sensium™ [63]) with the specifications listed in Table 9. The fabricated CMOS Sinh notch chip is characterized by means of linearity, frequency and noise measurements, which serve for the practical evaluation of the CMOS Sinh filtering approach as well as provide useful insights on the feasibility of the hardware implementation of specific low frequency biomedical applications by means of the Sinh approach. The material is organised as follows: A brief review of mains noise rejection methods is given, highlighting the importance of notch filters. The notch transfer function that has been implemented by means on the Sinh approach is introduced. The details of the circuit implementation are clarified and the choice of component values is explained while critical points of the design and optimization are discussed. The measured results from the fabricated chip are presented and conclusions are drawn.

Table 9: Specifications for the notch filter to be incorporated on the 0.13μm Toumaz Sensium™ chip[63].

Voltage supply (V)	1-1.8
Notch frequency (Hz)	50/60
Notch attenuation (dB)	45-80
SNR (dB)	>60dB
Power consumption	nW-μW

5.1 A 50/60Hz noise rejection brief

All biomedical systems which rely on electrode-based measurements from the human body are subject to external sources of electromagnetic interference. The most harmful one for bio-potentials is the power line interference, widely known as “mains noise”. Mains noise is caused mainly by induction whereby a conductor present within a varying magnetic field, develops an induced electromotive force. The magnetic field is created by the alternating current flowing in the mains cables and hence is directly linked to the mains power distribution. Alternatively, in the case of electrostatic induction, the electric field associated with the mains supply is capacitively coupled to the subject [263]. Mains noise is usually modelled as a sinusoid whose frequency is dictated by the frequency at which the power is generated (i.e. 50Hz in Europe and 60Hz in the US) and it usually contains harmonics at higher frequencies [107,264].

A variety of methods have been suggested for dealing with the problem [265]. Trying to prevent the signal from picking up the noise in the first place, has been one of the first attempts. However, neither this approach nor impedance matching between electrode and skin, seem to suffice [264]. Research into increasing the CMRR of the amplifier [263,266-268] present at the front-end of the bio-signal measurement has also been suggested as a solution. However, the signal quality achieved is not adequate for all applications. For example, experiments strongly suggest that including a 50Hz notch filter in the signal processing chain can significantly improve the quality of ECG measurements [115]. Hence the mainstream of the research efforts aiming at tackling the problem focuses on filtering out the 50Hz noise from the spectrum of the signal.

A notch or a low-pass filter of high order is usually inserted in the signal processing chain of systems handling bio-potentials. Sometimes a combination of the two is used to achieve higher rejection. Traditionally the filter is a 2^{nd} order twin-T notch [243,269]

implemented off-chip due to the large capacitor values required. Digital notch filters have also been proposed. Subtraction [270] and adaptive cancelling techniques have been reported. In [271] an improvement of as much as 30dB in signal quality by means of adaptive methods has been reported. Despite the efforts for the design of both digital and analog filters suitable for 50Hz noise, research indicates the advantage of including an analogue notch filter in particular for the processing of ECG measurements for heart-rate variability studies [114]. The practical potential of incorporating CMOS Sinh notch filters in biomedical systems which are susceptible to mains noise is explored in the following sections.

5.2 A versatile high order notch transfer function

The notch transfer function implemented was initially proposed for an image rejection application, which can achieve more than 80dB of attenuation at the unwanted image frequency [272]. The original transfer function has been modified in order to obtain a unity gain instead of 0.5 proposed originally in [272]. Figure 5.1 illustrates the blocks which compose the transfer function of the filter codified by equation (5.1).

$$\frac{N(\omega)}{D(\omega)} = \frac{s^2+1}{s^4+4s^3+6s^2+4s+1} \tag{5.1}$$

As indicated in Figure 5.1 the noise is cancelled upon subtraction at the output of two pathways due to the noise signal having the same magnitude and phase. One pathway is composed of the cascade of the two 2nd order responses (one of which is low-pass while the other one is high-pass). The second pathway is composed of a low-pass biquad and an all-pass 1st order section. It can be electronically configured into either a symmetric or a low pass notch frequency response upon the choice of the poles and zero frequencies of the individual blocks which compose the transfer function (5.1). This feature can be particularly attractive when the same front-end is shared between more than one different bio-signals. For example

a symmetric notch response can be realized in the case of ECG signals whose bandwidth extends up to 120Hz but a low pass notch might be sufficient for EEG applications of smaller bandwidth [77]. Figure 5.1 illustrates a block diagram corresponding to the notch transfer function codified by (5.1). The low pass and high pass 2nd order responses can be built by means of simple 1st order sections since only real poles need to be implemented.

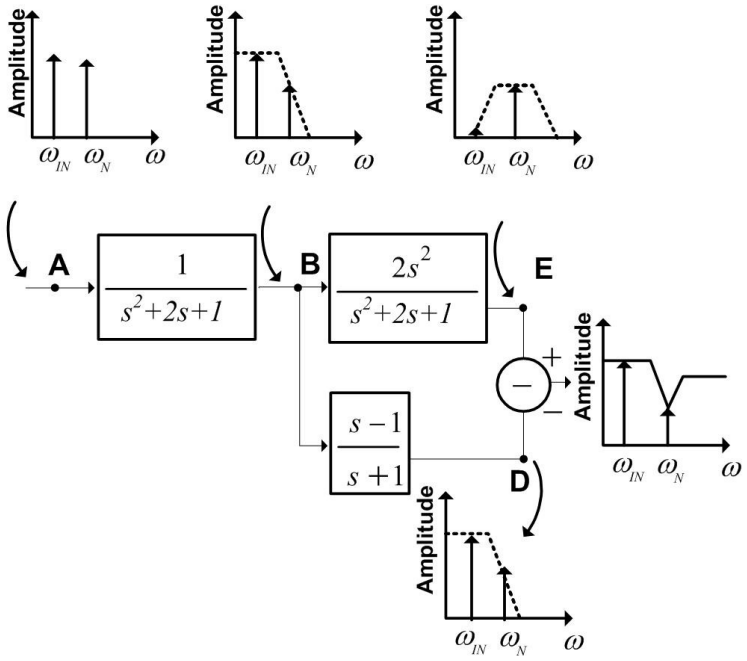


Figure 5.1: Block diagram of the 4th order notch filter indicating the amplitude of the noise at the output and input of each block. Upon subtraction at points E and D, the frequency response of the overall system output is that of a deep notch at the noise frequency (ω_N).

Referring to Figure 5.1 and assuming that a) the de-normalized response of the low pass block $(s^2+2s+1)^{-1}$ is realized by a cascade of 1st order sections with poles at frequency f_{o1} and b) that the de-normalized response of the high pass block $[2s^2/(s^2+2s+1)]$ is realized by a cascade of 1st order blocks with poles at frequency f_{o2}, then the general de-normalized transfer function realized by means of the block diagram of Figure 5.1 is codified by (5.2) with the frequency f_{o3} referring to the first order all pass section.

$$N(s)=\frac{1}{\left(\left(\frac{s}{2\pi f_{o1}}\right)+1\right)^2}\left[\frac{2\left(\frac{s}{2\pi f_{o2}}\right)^2}{\left(\left(\frac{s}{2\pi f_{o2}}\right)+1\right)^2}-\frac{\left(\frac{s}{2\pi f_{o3}}\right)-1}{\left(\frac{s}{2\pi f_{o3}}\right)+1}\right] \tag{5.2}$$

When $f_{o1}>f_{o2}=f_{o3}=f_o$, the de-normalized transfer function (5.2) reduces to (5.3) which corresponds to a symmetric notch response up to the frequency set by the poles (f_{o1}) of the low pass 2nd order response. In (5.3) $\omega_1=(2\pi f_{o1})$ and $\omega_o=(2\pi f_o)$. When ω_o in is close to ω_1 then the frequency response (5.3) obtains a low pass characteristic after the notch. Figure 5.2 illustrates two indicative MatLab™ notch responses corresponding to (5.3) with f_o equal to 50Hz and 500Hz while f_{o1} remains at 2.2kHz. With f_o=50Hz and f_{o1}=2.2kHz, a symmetric notch response is obtained with the pass band at the right of the notch extending up to 1kHz.

$$N(s)=\frac{\omega_1^2}{(s+\omega_1)^2}\frac{s^2+\omega_o^2}{(s+\omega_o)^2} \tag{5.3}$$

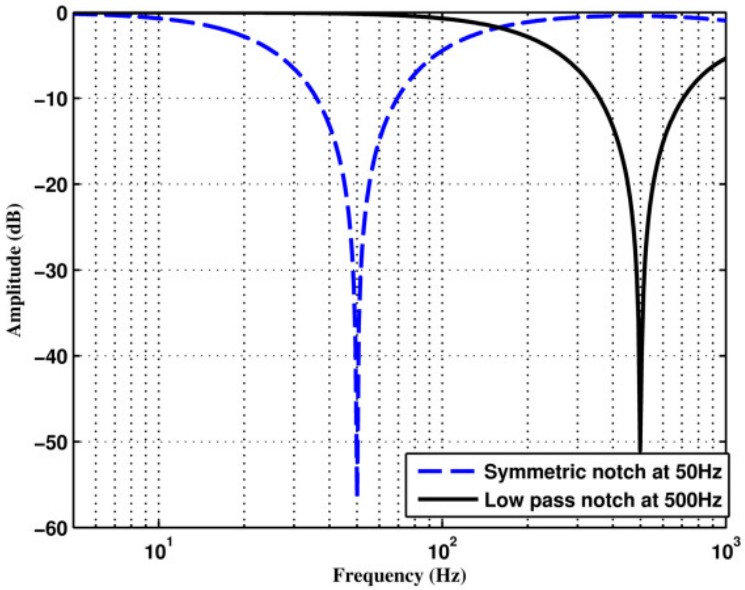


Figure 5.2: Indicative MatLab™ notch frequency responses. The symmetric notch response is obtained from (5.3) for f_o (=f_{o2}=f_{o3}) equal to 50Hz and f_{o1}=2.2kHz and can be tuned to different notch frequencies by means of f_o.

From the above it should be clear that the specific notch transfer function: a) can provide sufficiently deep notch, b) is versatile, allowing for flexibility in the determination of the appropriate bandwidth, depending on the application c) can be implemented by means of 1st order sections. The attempt reported here for a fabricated high order Sinh CMOS filter topology allows for a first assessment of the Sinh CMOS approach beyond simulated results.

5.3 Circuit implementation

5.3.1 1st order universal output Sinh filter: The building block

The implementation of the practical CMOS Sinh lossy integrator used as building block was presented in detail in Chapter 3. This work is extended by realizing high-pass and all-pass responses from the same first order section which will be employed in the implementation of the notch transfer function (5.3). To facilitate the discussion, Figure 5.3 repeats the main blocks used for the realization of the Sinh integrator while Figure 5.5 depicts its transistor–level schematic. All PMOS devices forming part of translinear loops must operate in weak inversion in order for exponential conformity to be ensured. Referring to Figure 5.3 and Figure 5.5, as already explained in Chapter 3, the input current I_{IN} is split by means of a geometric mean splitter into two phases (I_{IN}^{U}, I_{IN}^{L}) as codified by (5.4). The exponential transconductors at the output sense the capacitor voltage V_{cap} and produce an output current I_{OUT} which is related to V_{cap} through the sinh function (5.5) with the upper phase I_{OUT}^{U} of I_{OUT} realized as in (5.6) and the lower phase I_{OUT}^{L} as in (5.7).

$$I_{IN} = I_{IN}^{U} - I_{IN}^{L} \tag{5.4}$$

$$I_{OUT} = I_{DC}\sinh(aV_{cap}) \tag{5.5}$$

$$I_{OUT}^{U} = \frac{I_{DC}}{2}\exp(aV_{cap}) \tag{5.6}$$

$$I_{OUT}^{L} = \frac{I_{DC}}{2}\exp(-aV_{cap}) \tag{5.7}$$

The factor α equals $(nV_T)^{-1}$, where n denotes the sub-threshold slope factor and V_T, the thermal voltage. The two translinear dividers produce, by means of an array of current mirrors which deliver the appropriate currents to them, the two phases I_{cap}^{U} and I_{cap}^{L} of the capacitor current I_{cap} as shown in (5.8). Bearing in mind (5.9) and (5.10), it can be verified that the integrator realizes an input-output linear first order differential equation which

corresponds to the lossy integrator transfer function (5.11) with the capacitor voltage V_{cap} always complying with the sinh law (5.5). Note that by eliminating the connections at points A, B in Figure 5.5, the topology realizes a lossless integrator.

$$I_{cap} = I_{cap}{}^{U} - I_{cap}{}^{L} \tag{5.8}$$

$$I_{cap} = C\left[dV_{cap} / dt\right] = I_{cap}{}^{U} - I_{cap}{}^{L} \tag{5.9}$$

$$I_{cap} = \frac{[I_o I_{IN} - I_o I_{OUT}]}{I_{DC}\cosh(aV_{cap})} \tag{5.10}$$

$$H(s) = \frac{I_o / nCV_T}{s + I_o / nCV_T} \tag{5.11}$$

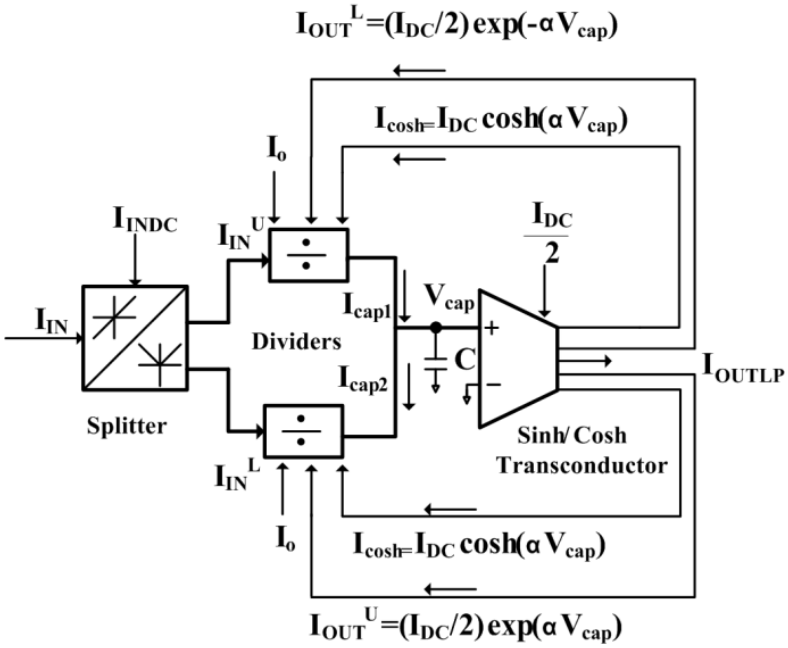


Figure 5.3: Block diagram of the Sinh lossy integrator [154].

The inherent class-AB nature of the lossy integrator facilitates the addition and subtraction of phases by means of (class-A) current mirrors. In order to obtain the high-pass response (5.12) and (5.13), the low-pass output (5.14) is subtracted from the input (5.4) resulting in (5.15).

$$H(s)_{HP} = \frac{s}{s+1} \tag{5.12}$$

$$I_{OUT_{HP}} = I_{OUT_{HP}}{}^{U} - I_{OUT_{HP}}{}^{L} \tag{5.13}$$

$$I_{OUT_{LP}} = I_{OUT_{LP}}{}^{U} - I_{OUT_{LP}}{}^{L} \tag{5.14}$$

$$I_{OUT_{HP}} = \overbrace{I_{IN}{}^{U} + I_{OUT_{LP}}{}^{L}}^{I_{OUT_{HP}}{}^{U}} - \overbrace{(I_{IN}{}^{L} + I_{OUT_{LP}}{}^{U})}^{I_{OUT_{HP}}{}^{L}} \tag{5.15}$$

Four NMOS transistors are added to the lossy integrator of Figure 5.5 as mirror outputs which provide the input and low-pass output phases for the high-pass output described (5.15) and an additional PMOS mirror performs the subtraction of the two phases of the high-pass output according to (5.13) (see Figure 5.6). In a similar way, for the all-pass output (5.16) and (5.17) to be formed, the low-pass output (5.14) is subtracted from the high-pass output (5.13) resulting in (5.18). At circuit level, six more transistors provide an extra set of input and output low-pass split phases and realize the all-pass response as described by (5.17) and (5.18). The block diagram of the universal output 1st order filter is depicted in Figure 5.4 and its transistor-level details in Figure 5.6 and Figure 5.5. The circled NMOS devices in Figure 5.6 have double the aspect ratio of the NMOS in their corresponding mirror arrays to account for the factor of 2 in (5.18). The transfer functions of the realized high-pass and all-pass filters are given by (5.19) and (5.20) accordingly.

$$H(s)_{AP} = \frac{s-1}{s+1} \tag{5.16}$$

$$I_{OUT_{AP}} = I_{OUT_{AP}}{}^{U} - I_{OUT_{AP}}{}^{L} \tag{5.17}$$

$$I_{OUT_{AP}} = \overbrace{I_{IN}{}^{U} + 2I_{OUT_{LP}}{}^{L}}^{I_{OUT_{AP}}{}^{U}} - \overbrace{(I_{IN}{}^{L} + 2I_{OUT_{LP}}{}^{U})}^{I_{OUT_{AP}}{}^{L}} \tag{5.18}$$

$$H(s)_{HP} = \frac{s}{s + I_o / nCV_T} \tag{5.19}$$

$$H(s)_{AP} = \frac{s - I_o / nCV_T}{s + I_o / nCV_T} \tag{5.20}$$

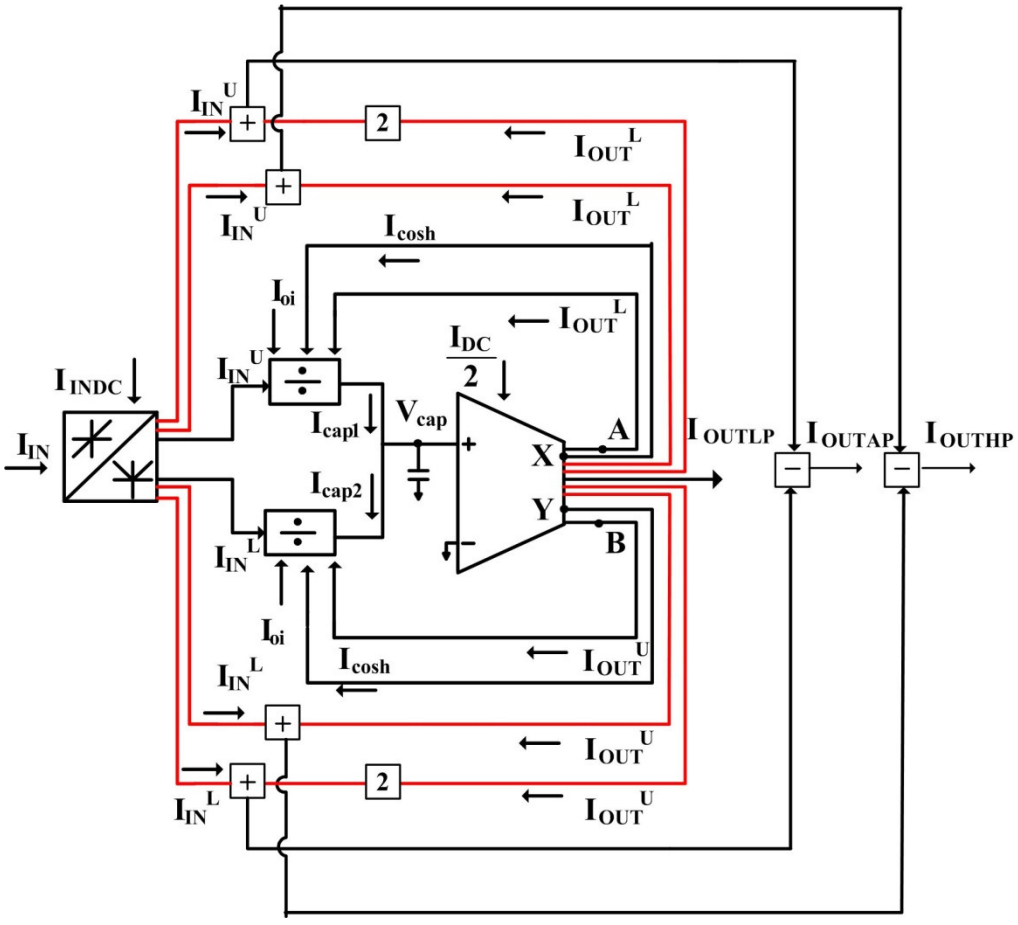


Figure 5.4: Block diagram of a universal output 1st order Sinh filter realizing low-pass, high-pass and all-pass outputs. The basic corresponding transistor level diagram is illustrated in Figure 5.5.

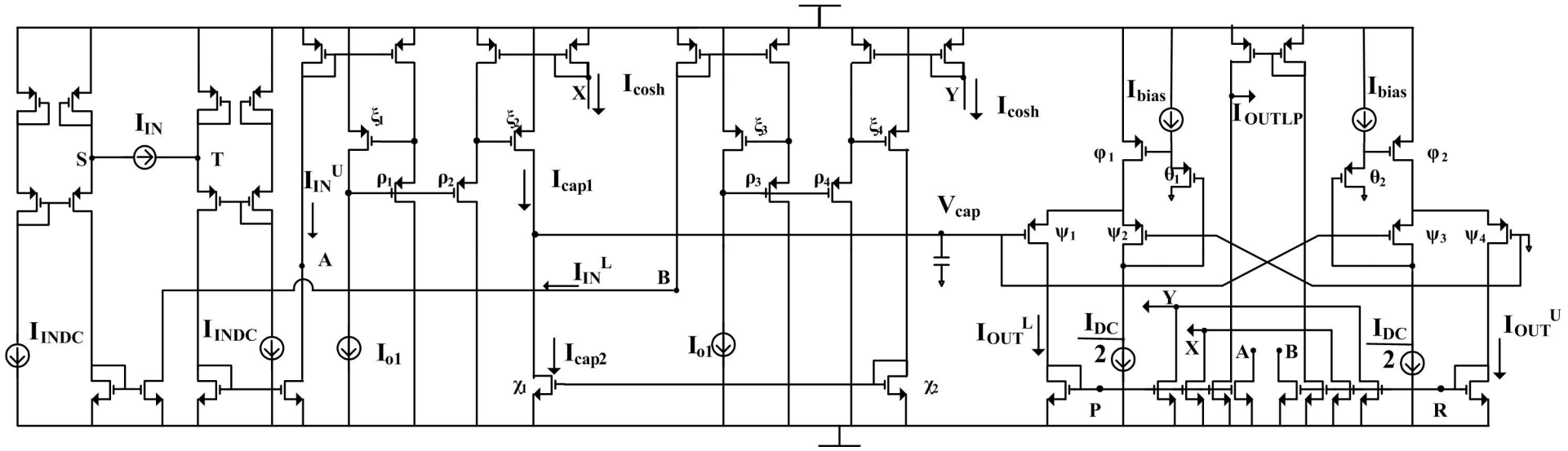


Figure 5.5: Transistor level design of the Hyperbolic-Sine (Sinh) lossy integrator. Compare with the block level representation of Figure 5.3. Note that for schematic clarity, the connections from the NMOS mirrors of the transconductor to the inputs of the dividers are indicated by the labels A, B. Similarly, the connections between the I_{cosh} outputs of the trasconductor to the dividers are denoted with labels X, Y.

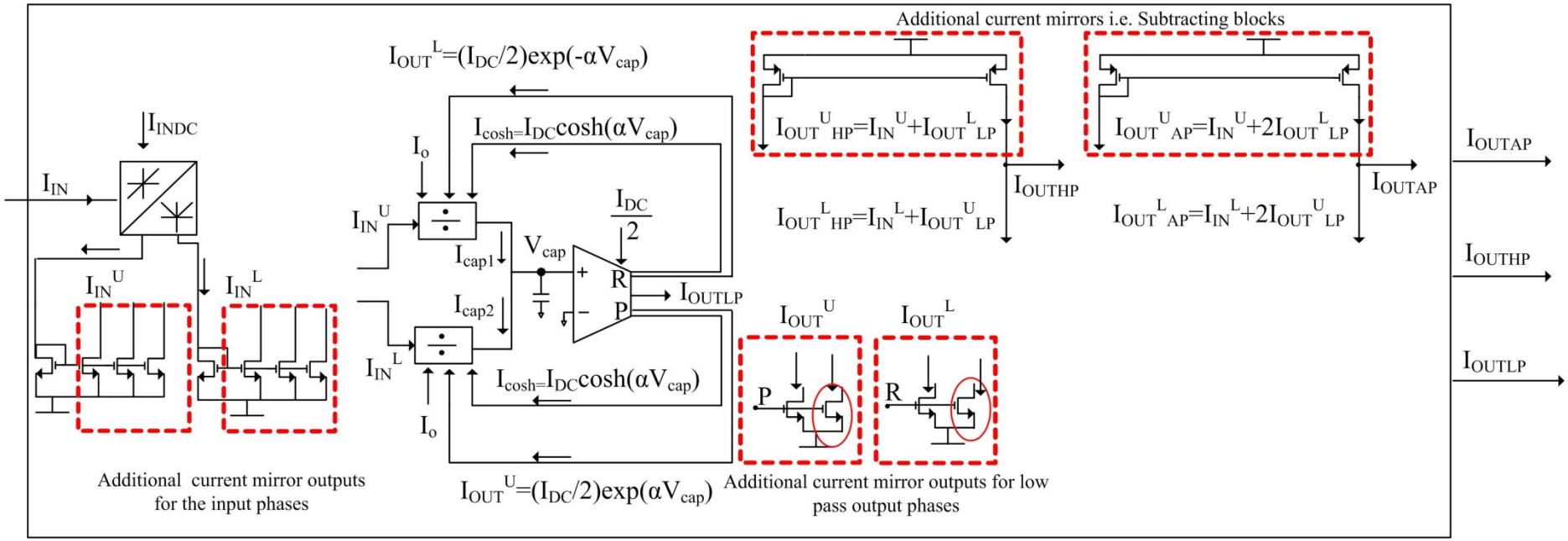


Figure 5.6: Transistor level design of a universal output 1st order Hyperbolic-Sine filter realizing low-pass, high-pass and all-pass outputs. The core of the topology remains that of the low-pass Sinh integrator (Figure 5.5). Additional PMOS current mirrors provide the AP and HP outputs by subtracting the lower from the upper phase of the HP and AP outputs accordingly. Moreover, additional NMOS current mirror output devices provide the necessary additional copies of the upper and lower phases of the input and low-pass output. Points P, R refer to the point of connection of the additional low-pass output NMOS devices to the NMOS mirrors of the transconductor (see Figure 5.5 for the position of the connections P, R).

5.3.2 An 8th order CMOS Sinh notch filter

Two notch filters as those described by (5.3) and Figure 5.1 have been cascaded in order to provide larger attenuation at the notch frequency. Each 4th order notch filter is implemented by cascading appropriate 1st order sections such as those shown in Figure 5.4. For the entire notch, whose block diagram is illustrated in Figure 5.11, only one input current splitter is required which provides the two phases of the input current to the first lossy integrator in the cascade. The two phases of the low pass output of the first integrator in the cascade are then directly passed on to the dividers of the following first order sections in order to form the second order low-pass, high-pass and all-pass filters. The overall notch output is formed by subtracting the outputs as illustrated in Figure 5.11. All the NMOS and PMOS mirrors have been cascoded. The sources and bulks of all the PMOS transistors are connected together. The gain of two in the high-pass filter (see Figure 5.1) is realized by doubling the aspect ratio of the respective devices which form the high pass output phases. All first order section capacitors are equal to 20pF while the device sizes are summarized in Table 10.

Large devices have been preferred over smaller geometries (see Table 10) in order to decrease errors due to mismatch and to reduce flicker noise (Chapter 2). In addition using large devices, the large signal frequency response of the individual integrators -and consequently of the whole notch topology- is more robust to variations of the bandwidth with increasing input signal strength. This non-ideal behaviour of the dependence of the bandwidth of the Sinh integrator on the input signal strength has been observed for the case of the integrator in [157]. Simulations have confirmed that it can be attributed to the deviation of the devices of the dividers (devices $\rho_{1\text{-}4}$ and $\xi_{1\text{-}4}$, in Figure 5.5) and transconductors (devices $\psi_{1\text{-}4}$ and $\varphi_{1\text{-}2}$ in Figure 5.5) from their ideal exponential behaviour necessary to compute the correct capacitor current (5.10). The errors introduced for large signals by the

dividers affect the frequency response. Likewise, when the devices of the TL loop of the sinh/cosh transconductor do not conform to the exponential law, an error is introduced to both I_{cosh} and I_{OUT} currents which in turn affects the frequency response, causing the bandwidth to decrease from its nominal value for large input signals. It has been verified through simulations that the variations in the bandwidth of the integrator which are manifested as a shift-to-the-left of the cut-off frequency as the modulation index m increases, can be almost eliminated when the width of the critical devices in the dividers and the transconductors increases (see Table 10). More specifically: when the size of the devices $\psi_{1\text{-}4}$ and $\varphi_{1\text{-}2}$ (see in Figure 5.5) increases to 100/1 (from 60/1) and the size of the devices $\rho_{1\text{-}4}$ and $\xi_{1\text{-}4}$, increases to 300/1 (from 60/1) then the large signal PAC simulation results of Figure 5.7 show that the reduction of the bandwidth for large m does not take place.

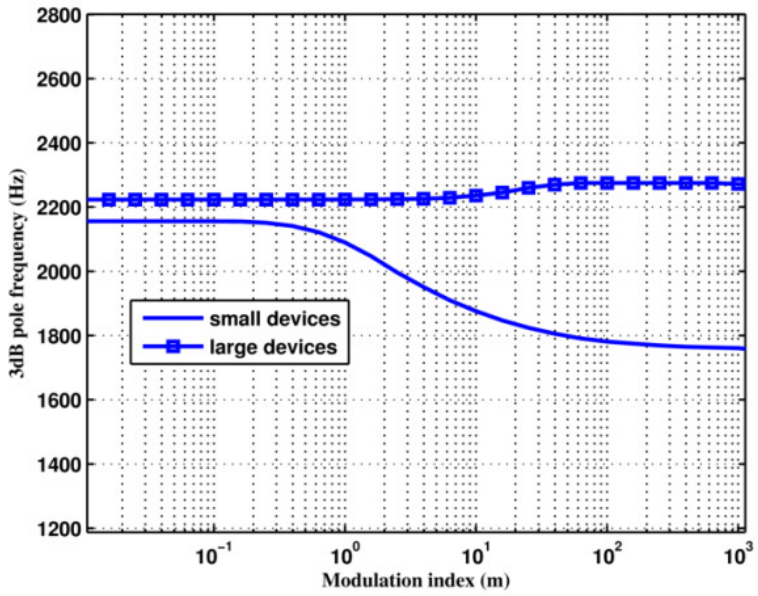


Figure 5.7: Simulated 3dB bandwidth versus modulation index (m) for the Sinh integrator of Figure 5.3: Block diagram of the Sinh lossy integrator [154]. Large signal PAC frequency response data are presented. Small device widths result in a ~400Hz shift-to-the left of the pole frequency of the integrator for m>10. Using large W/L values for the dividers and transconductors eliminates the shift-to-the-left for large and very large m values.

This choice of large devices for the fabrication of the Sinh notch chip has also been justified by Monte-Carlo simulation results performed to assess the effect of the two sizing

schemes of Table 10. The larger devices reduce the standard deviation of the notch frequency by 50%. On a final note, critical for the successful operation of such an internally non-linear topology, have been the matching techniques used during layout. Compact layout, common centroid techniques and the use of dummies, have all been adopted as common practice.

Table 10: Device sizes of the fabricated Sinh notch filter.

Device	Small devices [μm/ μm]	Device sizes of the fabricated notch filter [μm/ μm]
PMOS	60/1	300/1
NMOS	25/1	115/1
Level shifter (see Figure 5.8)	4/12.5	2/115
I_{cap}^{L} NMOS mirror (see Figure 5.10)	1/20	10/0.35
PMOS upper divider (see Figure	5/9	5/9

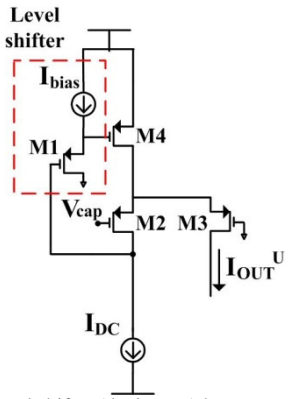


Figure 5.8: The level shifter (device M_1) has an aspect ratio of 2 μm /115 μm. The devices M_2-M_3 of the E-cells as well as the tail device M_4, have an aspect ratio of 300 μm /1 μm (Table 10,Figure 5.5).

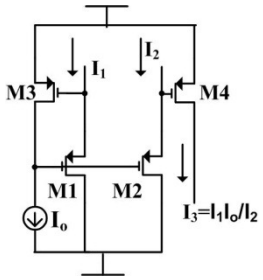


Figure 5.9: The upper (M_3-M_4) and lower (M_1-M_2) PMOS devices of the divider. The W/L of the upper devices is 5 μm /9 μm. The lower devices have an aspect ratio of 300 μm /1 μm (see Table 10,Figure 5.5).

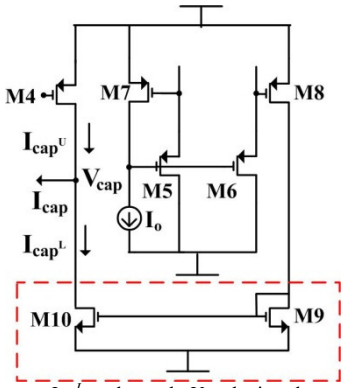


Figure 5.10: The NMOS devices M_9-M_{10} which convey I_{cap}^{L} to the node V_{cap} devices have aspect ratio 10 μm /0.35μm (Table 10,Figure 5.5).

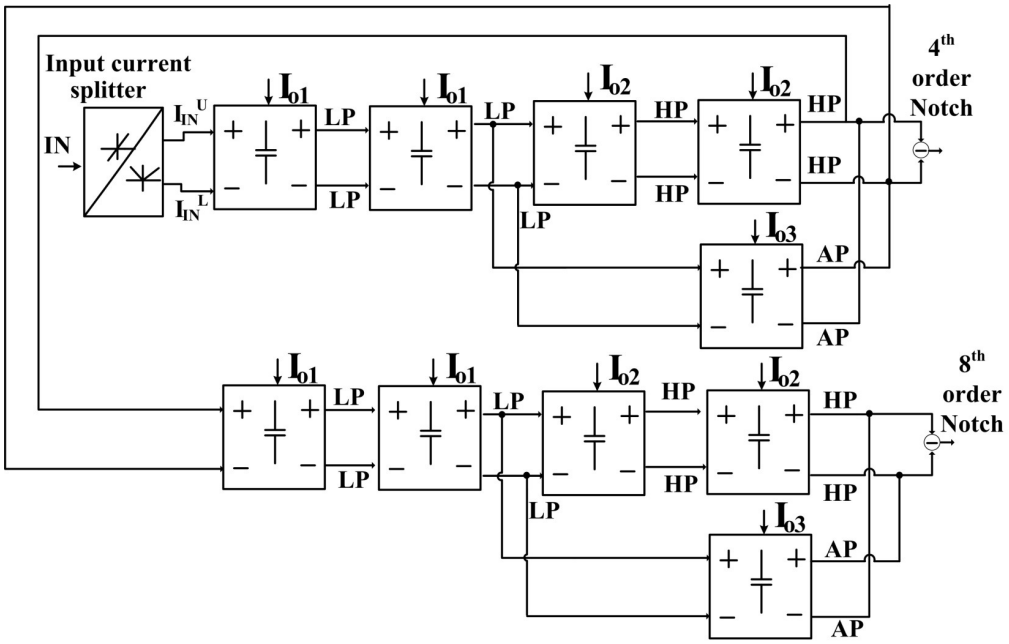


Figure 5.11: Complete block diagram of the fabricated 8th order notch Sinh filter. Each of the blocks represents the Sinh universal 1st order filter (see Figure 5.6) of the appropriate output. The plus (+) sign refers to the upper phase while the minus (-) to the lower phase. Note that only one input current splitter is used in the entire architecture to provide two strictly positive input phases. The output phases of each previous cell are fed to the appropriate inputs of the subsequent cell at points A or B at the dividers (see Figure 5.5). The topology is tuned by means of currents $I_{o1\text{-}3}$ with all capacitors being equal.

5.4 Simulation results

Prior to fabrication, the performance of the Sinh notch filter has been assessed by means of Cadence IC Design Framework simulations. Referring to (5.11), (5.19) and (5.20), the poles and zero (f_{oi}) of the low-pass, high-pass and all-pass outputs of the multiple output first order section (Figure 5.4) are determined by $I_{oi}/(2\pi nCV_T)$. Setting I_{o1} to 10nA places the poles of the low-pass filter (Figure 5.1) at the nominal frequency of 2200Hz. Electronic tuning of the notch frequency response (5.3) is then achieved by varying $I_{o2}=I_{o3}=I_{o.}$ While I_o remains less than 1nA, the notch response has unity gain at both sides of the notch (i.e. symmetric notch) up to 1kHz. Figure 5.12 depicts the tuning of the frequency response corresponding to the values of I_{oi} currents summarized in Table 11 and with all biasing currents I_{DC}, I_{INDC}, I_{bias} set equal to 10nA. Monte-Carlo simulation results (1000 runs) show that for matched mirrors, 33% of the responses have attenuation of >70dB within ±2Hz away from 50Hz. Finally, for 80% of the responses, the attenuation remains >60dB within ±2Hz away from 50Hz.

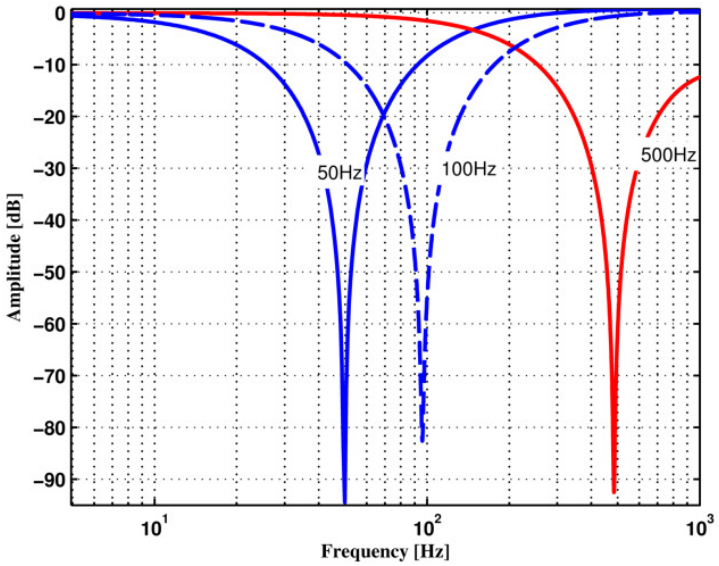


Figure 5.12: Simulated notch frequency responses corresponding to relation (5.3) for the values of the tuning currents listed in Table 11 (see Figure 5.11). All individual capacitors are equal to 20pF. For all three depicted frequency responses, I_{o1} is set equal to 10nA corresponding to ω_1= 2π(2.2kHz) in (5.3) and allowing for tunable symmetric (up to 1kHz) notch responses in the range of 10Hz -100Hz.

Table 11:Tuning currents for the 8th order notch frequency response.

f_{notch}(Hz)	I_{o1}	I_{o2}	I_{o3}
50	10(nA)	250(pA)	250(pA)
100	10(nA)	500(pA)	500(pA)
500	10(nA)	2.1(nA)	2.1(nA)

Two-tone tests were also performed whereby one input signal was placed in the pass band, (at 10Hz) while the second one was placed at the notch frequency of 50Hz. This test allows the quantification of possible distortion introduced to signals in the passband of the filter while it rejects large signals. With reference to Figure 5.13, it can be observed that for a 10Hz input tone of amplitude 1μA (m=100)[11], the THD (at 10Hz) remains below 1% so long as the rejected signal (at 50Hz) remains less than 1 μA in amplitude (i.e. its amplitude doesn't exceed that of the passband signal). The THD (at 10Hz) increases thereafter but remains below 3.5% even for 50Hz notched signals of amplitude 40 times larger. When the amplitude of the passband signal is lower (100nA at 10Hz) corresponding to m=10, the THD (at 10Hz) remains below 2% for amplitudes of notched 50Hz signals up to 100 times larger.

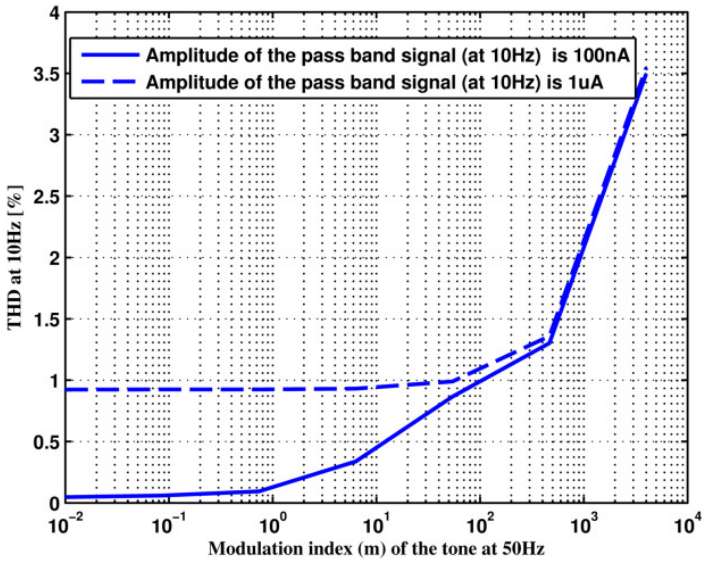


Figure 5.13: Large signal PSS analysis was performed to assess the impact of THD on an input tone in the passband of the filter while the amplitude of a second tone placed at 50Hz is rejected by the 8th order notch tuned at 50Hz. The amplitude of the THD is plotted versus the m of the rejected signal for two different amplitudes of the pass band signal (at 10Hz). Here m refers to the amount by which the amplitude of the signal at 50Hz is larger than the dc current I_{o1}=10nA.

[11] Strictly speaking the definition of m as I_{IN}/I_o applies to a first order filter. However, here the same definition is used for the notch filter with $I_o=I_{o2}=I_{o3}\ll I_{o1}$.

5.5 Measured results

5.5.1 Measurement set up

The microphotograph of the chip is illustrated in Figure 5.14. The performance of the filter has been assessed in both frequency and time domain, including measures of noise performance and linearity. Six off-chip current sources namely I_{INDC}, I_{DC}, I_{bias}, I_{o1}, I_{o2} I_{o3} (see Figure 5.6, Figure 5.11) are needed for the testing of the chip. An array of well-matched, multiple-output, cascoded mirrors ensures the distribution of the remaining biasing currents at the desired positions throughout the filter. The biasing currents I_{DC} and I_{INDC} are both set to 100nA in order to improve linearity (according to the discussion in Chapter 3) while I_{bias} is set equal to 10nA. The basic set-up used for acquiring small-signal frequency response employs a transformer (A262A2E) to output two balanced AC voltage signals. The voltage V_{IN} at the input of the transformer is sourced from the source channel of a Stanford Research SR785 spectrum analyzer. The middle point of the transformer is set at 1.67V (Figure 5.16) in order to ensure that the devices of the splitter remain biased in weak inversion (WI). For all linearity and time-domain tests, a pair of GPIB-synchronized -using MatLab™- Keithley 6221 AC/DC current sources generated a pair of (anti phase) balanced input current signals of appropriate frequency and amplitude. Large-signal frequency response curves have also been obtained by point measurements using synchronized Keithley current sources as input. The experimental set-up of this measurement is illustrated in Figure 5.15 and Figure 5.17.

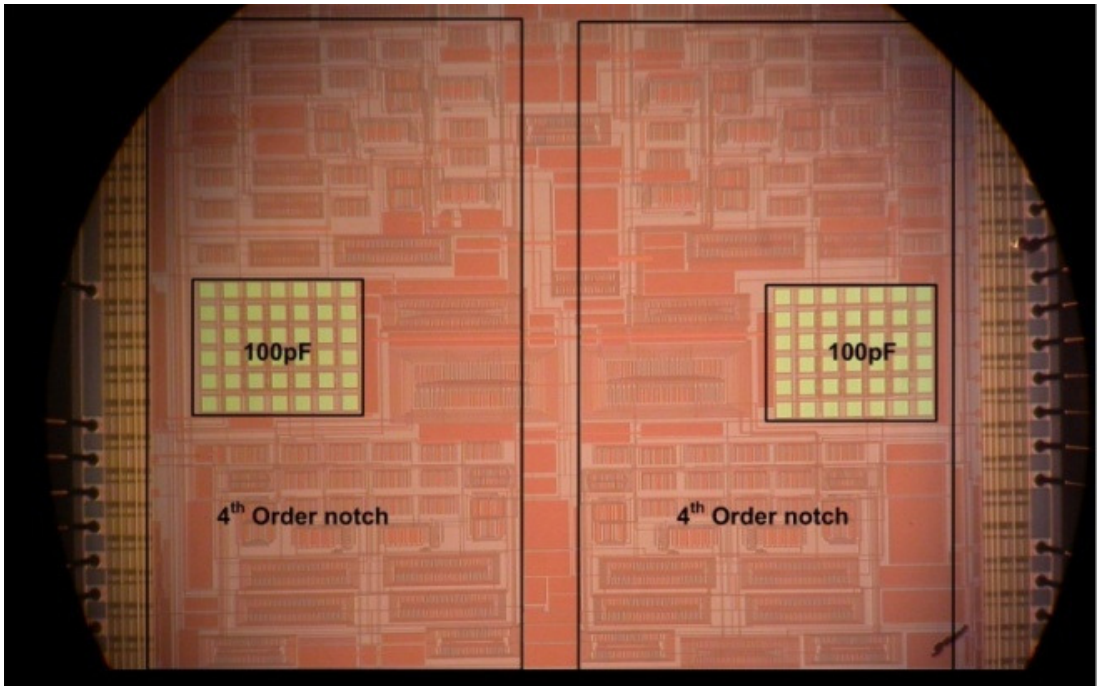


Figure 5.14: Microphotograph of the fabricated Sinh $4^{th}/8^{th}$ order Sinh notch filter in the 0.35µm CMOS process. The chip occupies $12.5mm^2$ and has a total capacitance of 200pF.

Figure 5.15: Snapshot of the experimental set up.

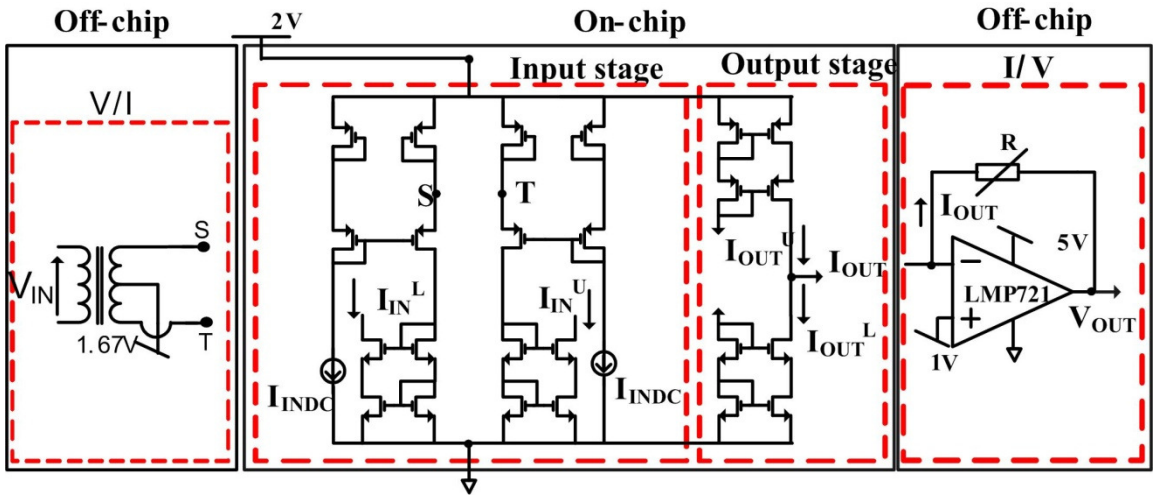


Figure 5.16: Measurement set up for small signal frequency response results.

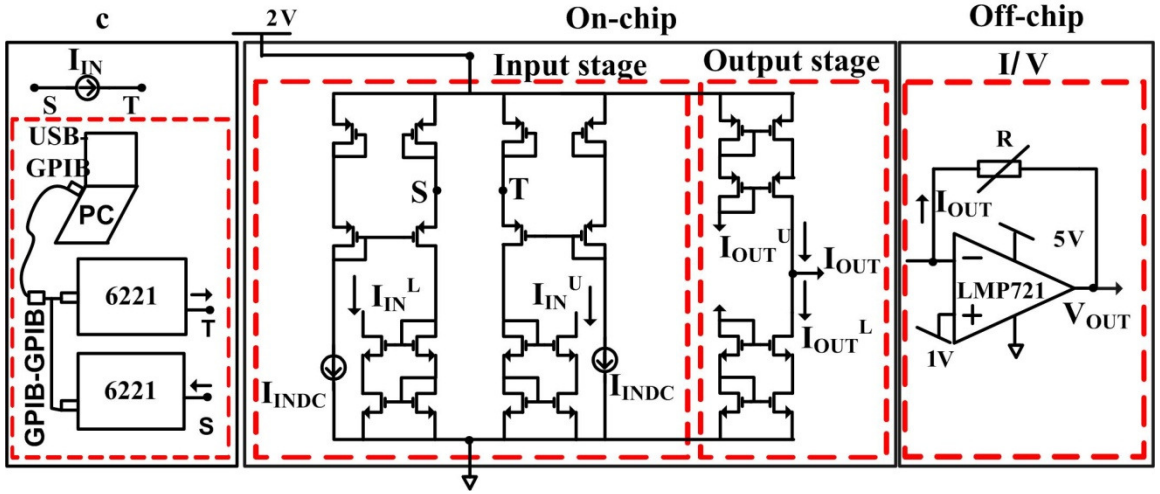


Figure 5.17: Measurement set up for large signal frequency response, noise and linearity results.

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5.5.2 **Frequency domain results**

Figure 5.18 shows the tunability of the 8th order notch frequency response over one decade. The notch frequency is tuned by altering the currents $I_{o2}=I_{o3}=I_o$ while I_{o1} remains at 10nA to obtain a symmetric notch response (5.3). The corresponding I_{oi} current values are listed in Table 12. Observe that there is a deviation of the order of 43-100pA between the values of the tuning currents $I_{o2,3}$ used for the measurements and simulations. This can be attributed to process variations. All notch responses illustrated in Figure 5.18 have attenuation >50dB at the notch frequency while reaching -80dB for the target range of 20-50Hz. Note the good agreement of the measured with the simulated responses denoted with dashed lines. Two measured notch frequency responses with a low-pass characteristic are illustrated in Figure 5.18 in order to verify experimentally the ability of the notch transfer function (5.3) to produce both symmetric and low pass notch responses. Taking into account the low pass notch responses corresponding to a notch at frequencies greater than 100Hz (see Figure 5.19), the 8th order Sinh notch filter can be tuned for almost two decades maintaining attenuation higher than 50dB.

Table 12: Tuning currents of the 8th order notch frequency response.

f_{notch}(Hz)	I_{o1}	I_{o2}	I_{o3}
11	10(nA)	57(pA)	57(pA)
25	10(nA)	100(pA)	100(pA)
50	10(nA)	207(pA)	207(pA)
100	10(nA)	407(pA)	407(pA)
500	10(nA)	2(nA)	2(nA)
750	10(nA)	4(nA)	4(nA)

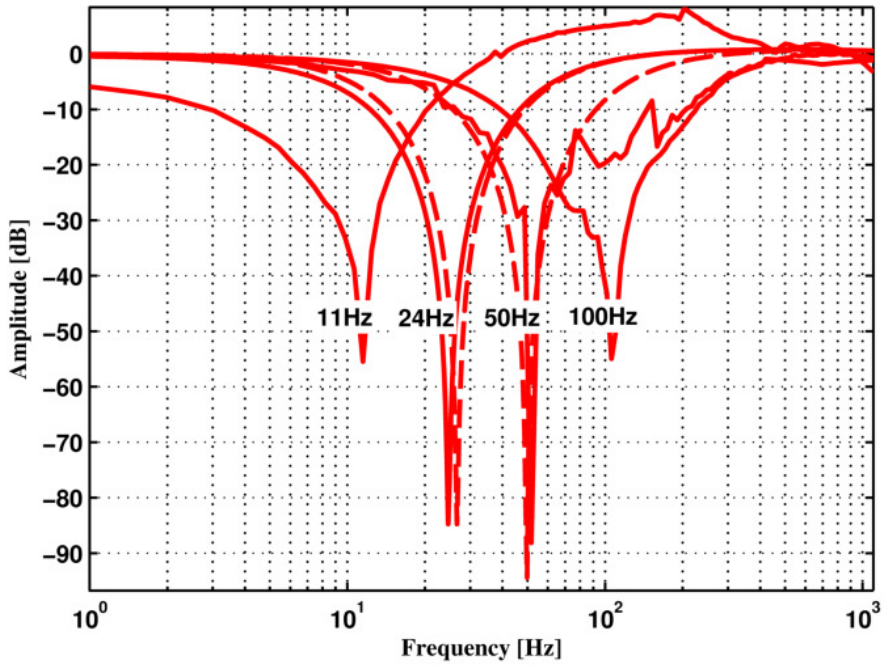


Figure 5.18: Tuning of the 8th order notch response (5.3) by means of the I_{o1}, I_{o2}, I_{o3} currents (all capacitors are 20pF). Here I_{o1} is kept at 10nA and I_o (=I_{o2}=I_{o3}) tunes the notch frequency. The results are obtained for a value of m=20. Simulated results are represented with dashed lines. The tuning currents are listed in Table 12 (see Appendix A).

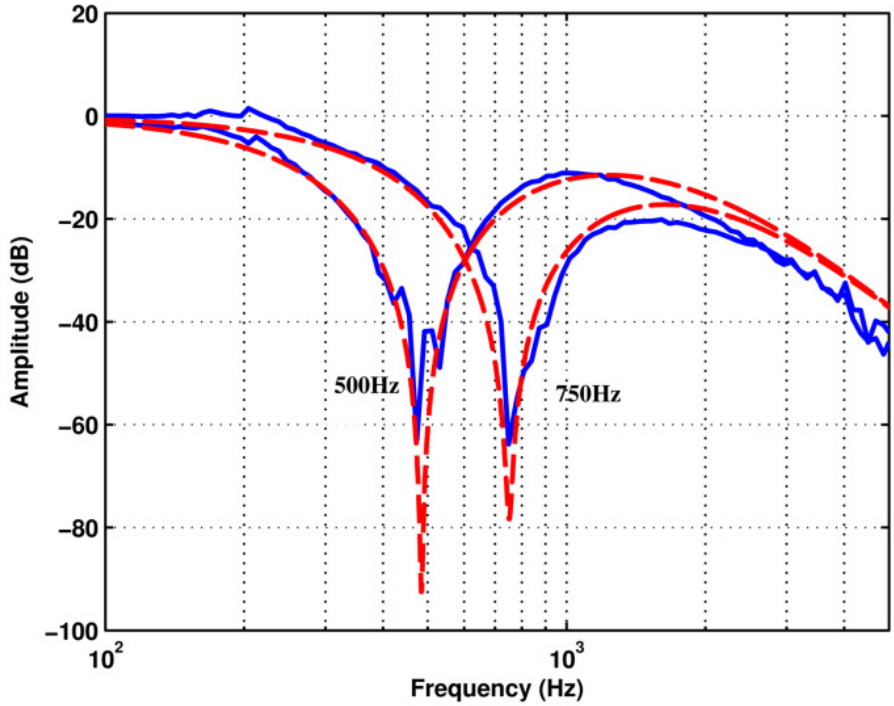


Figure 5.19: Tuning of the 8th order notch response (5.3) at higher frequencies by means of the I_{o2}=I_{o3}=I_o current while I_{o1} =10nA and (all capacitors are 20pF. The notch frequencies are set at 500Hz and 750Hz indicating that the 8th order notch response (5.3) can be tuned for almost two decades. Simulated results are represented with dashed lines. The tuning currents are listed in Table 12.

The variation of the measured notch responses for 8 chips at 50Hz is illustrated in Figure 5.20. The gain variation on the right and left passband of the notch does not exceed 2dBs. Moreover, the responses do not vary by more than 3-4Hz in the notch frequency while the variation in the notch attenuation does not exceed 10dB for either of the responses.

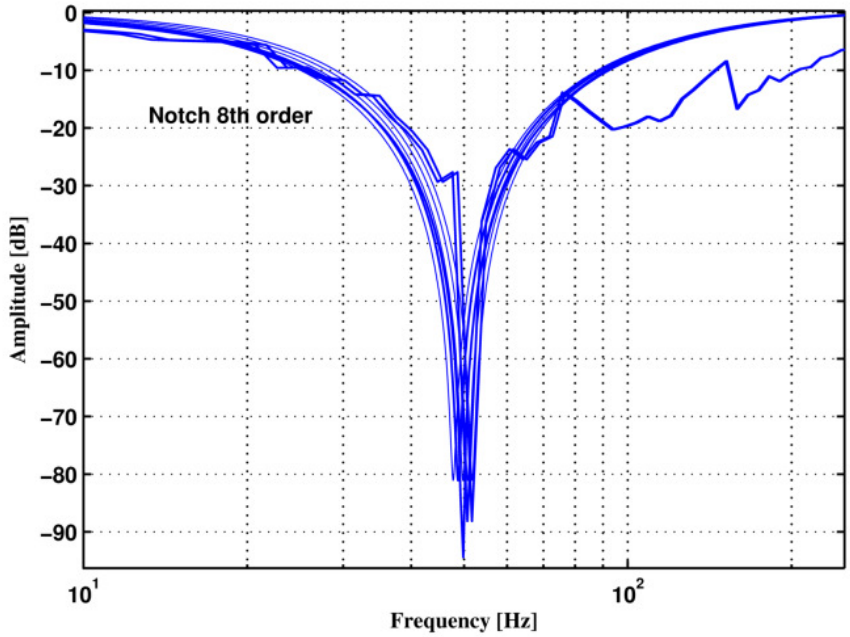


Figure 5.20: Measured variation across 8 chips. The notch is tuned at 50Hz (see, Table 11, Appendix A).

5.5.3 Linearity and noise measurements

Since an ELIN system is assessed, it has to be verified that its transfer function remains unaltered for small and large modulation indices m [157]. Figure 5.21 illustrates measured 60Hz notch responses for small (m<1) and large (m=54) modulation index values. Both responses have been obtained by point measurements by means of the set up illustrated in Figure 5.17 and are in good agreement with each other. This confirms that with the use of large device sizes, the non-ideal shift of the frequency response for large input signals is mitigated.

Single input tone linearity tests at various test frequencies in the pass band with the notch tuned at 100Hz[12] have been performed (see Appendix B). For the pass band on the left of the notch, we have chosen test frequencies at 10Hz and 15Hz have been chosen due to the important medical information they contain for bio-potentials like an ECG signal (the peak of its QRS complex is contained between 10-15Hz). The measured dynamic range (DR)[13] for the 8th order notch tuned at 100Hz was found to be 102dB for both input frequencies (10Hz and 15Hz). For an input amplitude of 1μA (corresponding to a modulation index of 100) the THD is below 3% while for an input amplitude of 100μA (corresponding to a modulation index of 10000) the THD remains below 4%. It should be noted that the filter can operate with 89dB DR and almost ten times less power consumption (8μW) by setting the biasing currents I_{DC}, I_{INDC} and I_{bias} equal to 10nA.

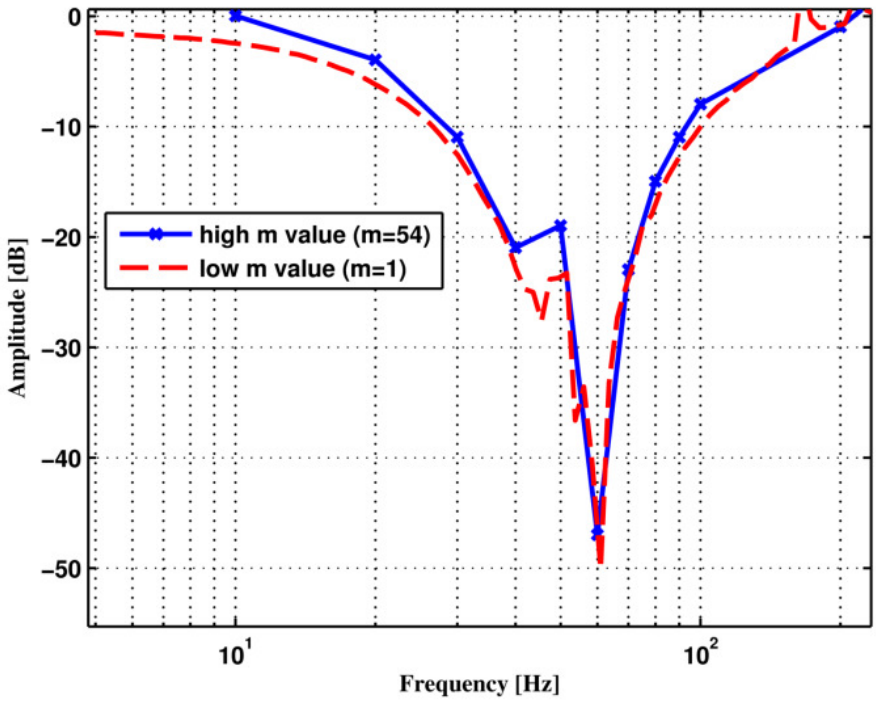


Figure 5.21: Notch responses tuned at 60Hz for low (m=1) and high (m=54) modulation index value accordingly. The responses confirm the validity of the ELIN character of the topology.

[12] The linearity tests have been performed with the notch frequency tuned at 100Hz to ensure that we report fair results. Note that for a 15Hz input and a notch frequency of 50Hz, most of the signal harmonics would fall in the stop band.

[13] The DR is defined throughout the paper as the ratio of the maximum input signal (for THD<4%, unless mentioned otherwise) to the noise integrated over a bandwidth of 0.01-30Hz (in the absence of input signal). This is the useful bandwidth for many bio-signals.

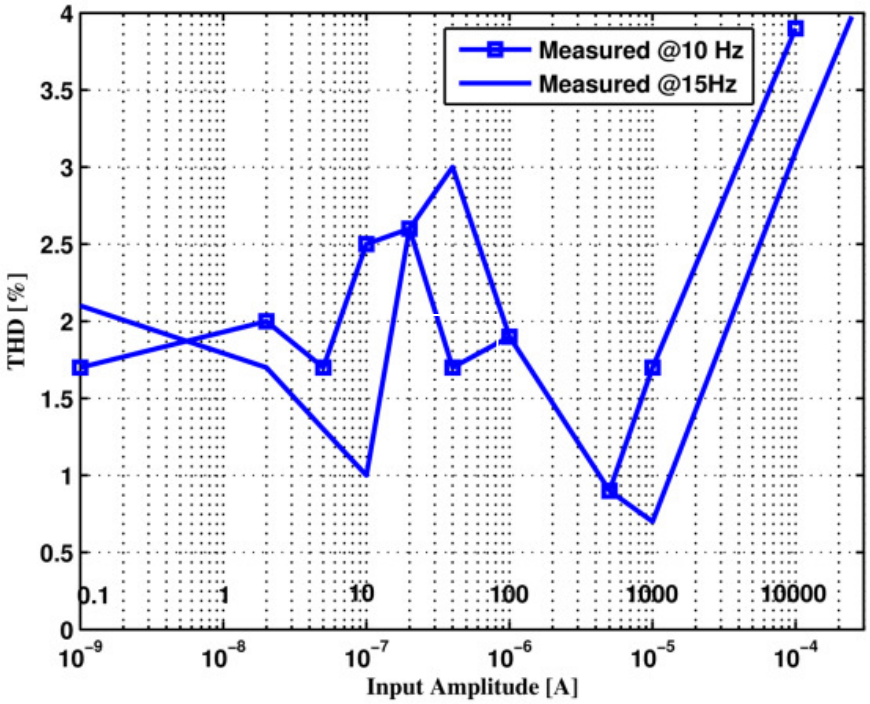


Figure 5.22: THD versus increasing input current amplitude for single input tone frequencies in the pass band of the filter. The notch is tuned at 100Hz. Five harmonics have been taken into account (For an input tone at 500Hz see Appendix B).

A common feature of the measured THD levels for both the 10Hz and 15Hz signals is that they exhibit a peak for *m* values between 10 and 100 followed by an area for which the THD levels decrease for increasing *m* values. Observe the decrease after the peak for *m*=20 (10Hz) or *m*=40 (15Hz). However such a drop for increased *m* values has been observed previously in measured results from class-AB log-domain filters [195]. Moreover, it is worth commenting that the small dip in distortion levels between *m* values 1 and 10 for both frequencies is verified by the behaviour of the 3rd ad 5th harmonic distortion simulated results for the notch filter. For very high *m* values (*m*>500) the THD levels increase with *m* for both inputs since the distortion mechanism is exercised more strongly.

It is worth reporting that during measurement the dominant harmonic was the 2nd with the 3rd increasing for certain range of *m* values as in [205]. In [160] the dominance of the 2nd harmonic of the class-AB topology reported there was attributed to mismatch despite the use

of BJTs and the low order of the response. Given the high order of the reported notch filter, its cascaded nature and the use of weakly inverted MOS devices, mismatch provides a reasonable explanation for the strength of the 2nd harmonic.

Due to the signal-dependent noise behaviour of companding filters [156], the impact of a strong signal placed at the notch frequency of the 8th order notch upon an in-band tone, has been examined. Given the unusual noise properties of ELIN topologies and the nature of the specific response (notch) such a test is meaningful since it tests the ability of the filter to treat in-band signals while rejecting large signals at the notch. The notch was tuned at 100Hz. A two-tone test was performed using an in-band signal with peak amplitude of 200nA (m=20) placed at 10Hz. The following behaviour was observed (see Figure 5.23): the noise power increases by approximately 20dB as the amplitude of the second signal placed at the notch (i.e. at 100Hz) increases from 20μA to 200μA. This is consistent with the calculations and measured results reported in [195,205]. Note that, the filter is able to reject noise of amplitude much larger than the in-band signal. The SNR of the 8th order notch at 15Hz reaches the value of 53dB for m>10. The respective value for the 4th order notch output (see Figure 5.23) amounts to 57dB. Table 13 summarizes the measured performance of the 8th order notch filter.

Table 13: Measured performance summary of the 8th order notch.

Technology	CMOS 0.35μm
Active area (mm^2)	12.5
Power supply (V)	2
Total capacitance (pF)	200
Tuning range	10Hz-1kHz
Attenuation (dB) (f_o=50Hz)	80
PSRR (dB)	>100
DR[a] (dB) @10Hz /15Hz	102 /111
SNR (dB) @ 10Hz with 1μA input signal	53
Power consumption (μW) (f_o=50Hz)	74

a The integrated noise is calculated for a bandwidth of 0.01-30Hz at the absence of input signal and the maximum signal is defined for THD<4%. The measured output noise density at 10Hz amounts to 145 pA/√Hz.

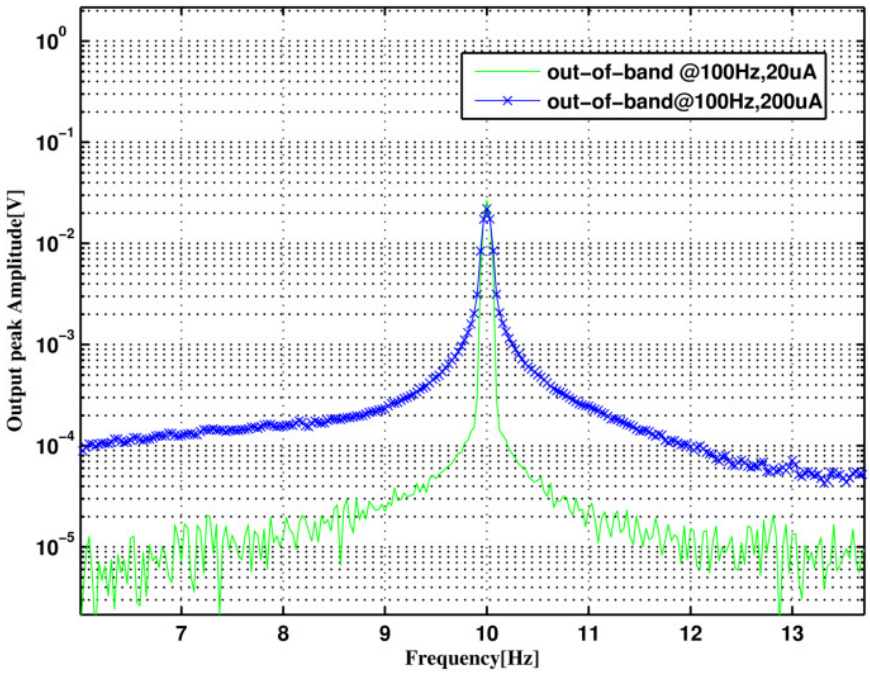
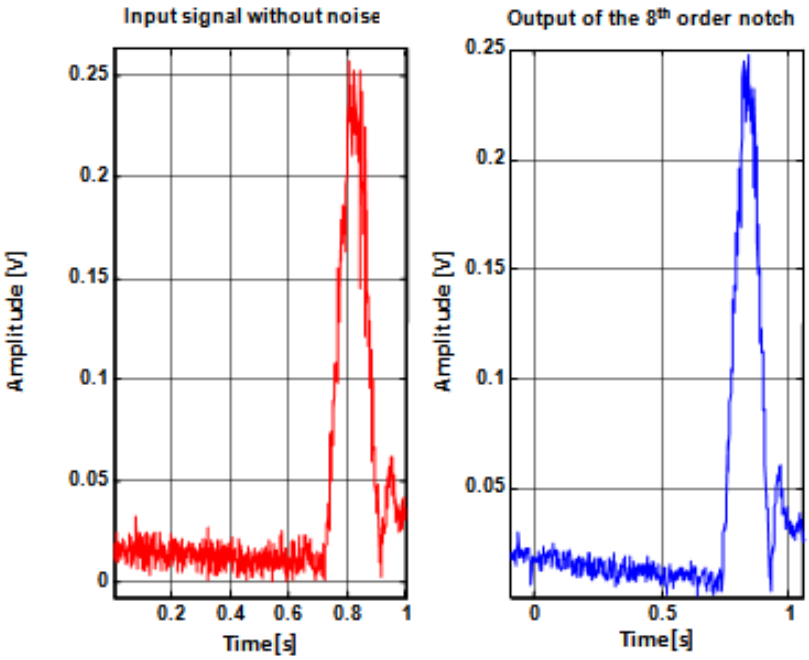


Figure 5.23: A sinusoid at 10Hz with amplitude of 200nA is fed at the input of the 8th order notch tuned at 100Hz together with an out-of-band 100Hz signal in order to assess the impact of increased out-of-band signal amplitude upon the noise floor. The increase of the out-of-band signal amplitude from 20μA to 200μA leads to an approximate ten-fold increase in the noise amplitude.

5.5.4 **Measured ECG signal transient**

In order to demonstrate the performance of the filter in practical situations, the filter output was tested by means of an ECG signal affected by 60Hz noise and fed as input to the 8th order notch filter tuned at 60Hz. An artificially generated ECG signal in MatLab™ [258] has been used. Figure 5.24 a) shows the input ECG signal without noise and Figure 5.24 b), the output of the 8th order filter tuned at 60Hz. The ECG signal corresponds to a heart rate of 72bpm (beats per minute). The peak of the QRS is at 250mV corresponding to 250nA. Mains noise was modelled as a 60Hz sinusoid. The 60Hz noise amplitude contaminating the clean ECG signal was of amplitude 10 times larger than the peak of the QRS complex of the clean ECG. The transient results are obtained via the Stanford Research SR785 spectrum analyzer (only one period of the signal is illustrated). The performance of the filter is also tested when the noise amplitude is 100 times larger than the peak of the QRS complex and the results are presented in Figure. 5.25. Both tests confirm the good operation of the notch filter.



a) b)

Figure 5.24: Measured ECG signal without noise (on the left) and output of the 8th order notch (on the right) when the noisy ECG signal is fed into the filter tuned at 60Hz. The noisy ECG has 72bpm and 100Hz sampling frequency generated in Matlab™ with the noise modelled as a sinusoid at 60Hz whose amplitude is ten times larger than the peak of the QRS complex of the clean signal (250mV corresponding to 250nA). A 1MΩ resistor has been used at the output (Figure 5.17). The results are presented for the duration of one period.

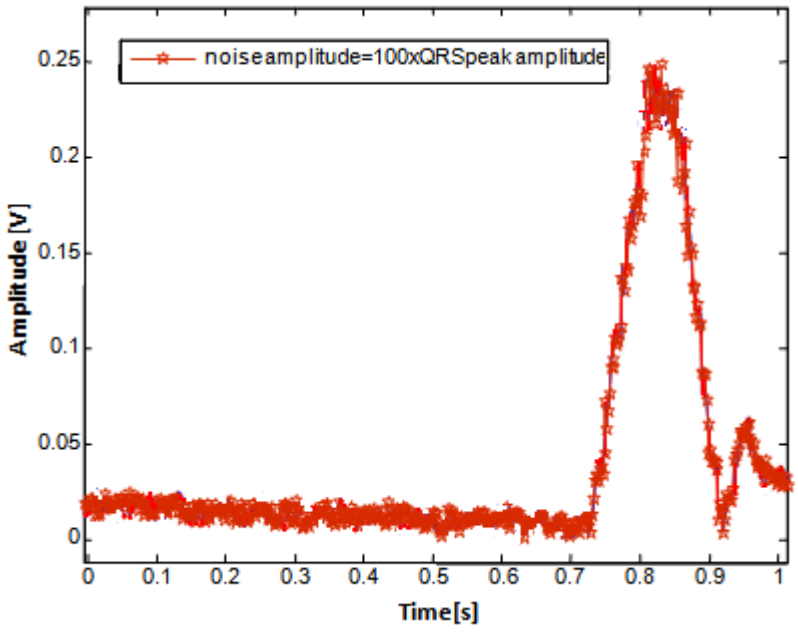


Figure. 5.25: One period of the ECG signal at the notch filter output when the noisy signal has amplitude 100 times the peak of the QRS of the clean ECG signal (check the left of Figure 5.24)

5.6 Discussion & conclusions

An 8th order class-AB notch filter realized as a cascade of ten 1st order sections has been designed and fabricated in the 0.35μm CMOS AMS technology. Universal 1st order Sinh filter sections, based on a modification of the lossy Sinh integrator proposed in [154] and realizing all-pass, high-pass and low-pass outputs, have served as the building blocks for the notch filter.

The presented results are the first measured results from fabricated high order CMOS Sinh topologies. The 50Hz 8th order notch consumes 8μW from a 2V power supply level and incorporates a total capacitance of 200pF while achieving a dynamic range of 89dB. A DR of 102dB in the ECG frequency range can be achieved at the expense of a higher power consumption of 74μW. While the 4th order notch attains a moderate attenuation of 50dB (see Appendix A), the 8th order on the other hand achieves an attenuation of 80dB at 50Hz and retains attenuation (at the notch frequency) higher than 50dB for the tuning range of 100Hz to 1 kHz.

Given that the presented chip is the first fabricated and tested CMOS high order Sinh ELIN topology and the aim was to test it under a variety of conditions, extra emphasis was placed on matching (resulting in large devices). In addition, large capacitors of 20pF per integrator were intentionally used to reduce the impact of parasitics. However, simulations indicate that there is no deterioration in the performance of the integrator when each capacitor is reduced to 10pF (50% capacitor area savings). Moreover, large devices at the obvious cost of power consumption and chip area were used to keep the large signal notch frequency response unaffected by large input amplitudes for a wide range of notch frequencies. Tuning by means of different biasing current values dictates not only that the logarithmic/ exponential conformity for each individual device should hold for the range of tuning currents but also that it should be matched for all devices, a requirement which leads to large

devices. In practice, however, a notch filter would be designed for a very specific frequency thus allowing for reduction and optimization in the size of not only the capacitors but also in the transistors. If for example large dimensions were used only for the critical devices such as those of the dividers, the non-linear transconductors and certain current mirrors, then considerable chip area savings in excess of 40% would be achieved. Finally if the attenuation requirements are not very high, the order can be lowered. Though the presented measured results have focused mostly on the 8^{th} order response, measured results corresponding to the 4^{th} order response have also been collected and show that the 4^{th} order response achieves an attenuation of 50dB at 50Hz at half the power consumption and chip area of the 8^{th} order notch response (see Appendix A).

The measured results presented here verify: a) the feasibility of CMOS Sinh low-power designs and b) their class-AB nature. Table 14 compares the presented experimental design with other notch designs of various synthesis techniques. It is clear the Sinh notch topology compares well in terms of tuning range, notch depth, DR and power supply requirements. It should be emphasized that no other IC notch filter has been characterized by the plethora of measured or simulated results that are presented for the characterization of the here-presented notch filter. However, the aim of this Thesis was to evaluate the feasibility of ELIN CMOS Sinh filters through this particular application and therefore as many aspects of the simulated and measured performance of the proposed design as possible, have been reported.

Table 14: Comparison of the 8th order notch Sinh filter with other notch implementations.

	[239]	[77]	This work
Technology	0.35µm CMOS	0.35µm CMOS	0.35µm CMOS
Results	simulated	measured	measured
Topology	2nd order class-AB Log	5th order OTA-C	8th order Sinh
Notch attenuation	>50 (dB)	>65(dB)	>70dB
Total capacitance	300 (pF)	100 (pF)	200 (pF)
Area	N/A	0.25 (mm^2)	12.5 (mm^2)
Power supply (V)	2	±1.5	2
Static power consumption/pole/f_{notch}	< 2 (nW/Hz)	44 (nW/Hz)	16-148 (nW/Hz)
Tuning range	500kHz-4MHz	30-67Hz	10Hz-1kHz
Max DR (dB)	60,THD<1%, BW=N/A	40@ 8Hz,THD<0.5%, BW=[0.01-37Hz]	102 @10, THD<4%, BW=[0.01-30Hz][a] 88 @10Hz, THD<2.5%, BW=[0.01-30Hz] 102 @15Hz, THD<3%, BW=[0.01-30Hz] 111 @15Hz, THD<4%, BW=[0.01-30Hz] 88 @10/15Hz, THD<3% , BW=[0.01-100Hz]

a Note that that there will be a 6dB drop in the reported DR when a large BW of [0-100Hz] is considered.

6 Conclusions and future directions

6.1 Summary and achievements

6.1.1 The problem: Trade-off between linearity and low power

The population aging and the prevalence of chronic diseases as a consequence, have placed substantial pressure for the shift of current healthcare systems towards a more proactive service which relies on early detection and timely treatment of diseases therefore reducing costs and most importantly saving lives. Long-term, continuous and unobtrusive monitoring through devices that can be worn or carried around patients (and non-) without disturbing their daily activity or necessitating frequent visits in hospitals or other healthcare settings, have been considered as a possible solution to the healthcare challenges and needs of modern societies.

The design of the analogue integrated circuits for wearable and implantable devices faces a lot of challenges which directly affect the specifications of the circuits that are to be incorporated in such systems and which in turn affect the performance and functionality of the systems. For example minimal power consumption is required in order to ensure that the heat dissipation would not damage the surrounding tissues. Low power consumption in combination with on-sensor node signal processing is also required in order to make better use of the limited available power budget. This in combination with energy harvesting could increase the functionality of the devices which is currently restricted due to battery technology since the need for bulky batteries or their frequent replacement would be eliminated.

Moreover, due to the nature of the physiological signals, which are typically low amplitude and low frequency signals and almost always affected by large dc signals, noise

and interference, pre-processing with good linearity and low noise is required. To further complicate matters, the low frequency nature of those signals requires frequency shaping networks with low cut-off frequencies. Such filters require large resistances and/or large capacitors which can be easily achieved with discrete components but are however difficult to fabricate on-chip directly due to the large area they would occupy.

Although lowering of the supply voltage as either a means to reduce the power consumption or due to scaling laws dictated by the trend towards smaller feature sizes of the active devices, is useful for the digital part of the typically mixed IC designs of such systems, it introduces further challenges to the analogue front-end design. Limited voltage headroom is the consequence of the necessary proportional scaling down of the supply voltage with feature size. The supply voltage severely restricts the maximum DR achievable when using conventional filter implementation techniques ($DR \sim V^2_{DD}C$) [161]. It is clear that if power supply limitations apply for the reasons explained, the only way to increase the DR is through an increase in the capacitance with direct consequences in chip area increase. Bearing in mind that 100pF capacitor corresponds to roughly $0.1mm^2$ [273], in order to achieve a DR of 105dB, from a 10pF capacitor, the power supply required would be no smaller than 5V [161]. This leads to the compromised performance of even the most sophisticated biomedical systems [63] which cannot afford the on-chip integration of useful filters such as notch filters for 50/60Hz rejection when conventional filter implementations are used.

6.1.2 A proposed solution: Class-AB Sinh companding signal processing

The continuous efforts of the CAS community to deal with the trade-off of good linearity and low power consumption, has led to a solution which tackles the problem at circuit level. The development of a class of circuits which do not require linearization of the individual active devices in order to achieve a large DR and which use the non-linear exponential large signal *I-V* characteristics of translinear devices (i.e. diodes, bipolar devices and weakly inverted MOS devices) to their advantage, is one such solution. These circuits, despite including non-linear elements, they exhibit input-output linearity. The importance of this is that non-linear transconductors (which can be as simple as a common emitter bipolar device) can be used in co-ordination with an appropriate input pre-distortion block in order to achieve a perfectly linear overall operation from input to output without necessitating power to be spent on linearising individual devices. This wide category of circuits which is not limited to filters [156], allows for the signal processor to ensure that internal signals a) remain above noise levels and b) below overload levels imposed by power supply levels and individual element non-linearities. This concept is often termed companding i.e. compressing and expanding and can be used to relax the internal noise requirements thus making the use of smaller capacitors and hence savings in chip area and power consumption possible. This technique is even more powerful when combined with class-AB operation which can further increase the DR without increase in power consumption [195,203] since the bias currents can be set much lower than the expected maximum input signal swing.

The most popular of the so-called ELIN [156], ESS [169] or Translinear [178] filters employ companding by means of the exponential function and are therefore termed Log-domain filers. Implementations of class-AB Log-domain filters in sub-threshold region of operation have allowed for powerful performances in terms of low voltage, low power

consumption and high DR [76,226,206,274-275]. However they suffer from two main limitations:

a) Due to the pseudo-differential class-AB structure they adopt, they utterly rely on the perfect matching of the two class-A systems.
b) Most importantly, they require two capacitors per pole therefore increasing costs due to chip area increase.

An even more promising engineering solution to the bottleneck of the dynamic range under a low power regime is provided by another sub-class of ELIN companding filters which are termed Hyperbolic-Sine (Sinh) filters since they rely in companding by means of the hyperbolic-sine function. The advantage of Sinh filters over the already powerful class-AB Log-domain filters is that they are inherently class-AB structures due to the odd symmetry of the sinh function at the heart of their companding operation. This implies that for class-AB operation, they only require one capacitor per pole. The potential of this filtering technique has been recognised by various researchers early on [156,169,211,227-228]. However the lack until recently [154,207,209] of practical building blocks and of a straightforward systematic synthesis approach for the design of high order topologies, have been the possible reasons behind the reluctance of the CAS community to investigate further the potential of Sinh filters. Prior to the CMOS Sinh integrator in [154] which has achieved +100dB DR confirmed by measured results [229], the reported Sinh topologies with <70dB DR [209,227-228] had not matched the capabilities of their pseudo-differential Log-domain counterparts (+110dB [226]).

6.1.3 Contributions

The work presented in this Dissertation a) has built upon the expertise of the Bio-inspired VLSI Circuits and Systems Group of Imperial College on Sinh filters [154,157,207,227,229230,244] and b) has been inspired by the observation that such a filtering modality could not only be useful for the implementation of bio-inspired circuits such as cochlea implants but also for the signal processing at lower than audio frequencies where the savings in chip area are even more important.

The scope has been a dual one: firstly to evaluate through simulations the potential of the Sinh filtering paradigm based on first order building blocks [154] which suit a CMOS implementation in standard twin-well processes and which have reached the theoretical potential attributed to the inherent class-AB nature of Sinh companding early on [156,169]. These building blocks, which benefit from a design based on translinear loops comprising only one type of devices (PMOS), -hence permitting a short between gate and bulk in an n-well process-, have been thoroughly studied, optimized and tested [157,229-230,244]. Secondly, having recognised through the simulation studies presented both in this work and prior work [157,229-230,244] that Sinh filtering modality constitutes a potential solution for the analogue front-end part of systems such as WBANs, the aim was to validate through measured results the performance of high order CMOS Sinh topologies for such applications. For these reasons,

- A mathematical framework for the systematic synthesis of high order Sinh filters comprising only p-type devices in their TL loops and originating from any state space description, has been provided.

- A number of examples of high order filters have been designed and simulated in Cadence Design Framework using the commercially available 0.35μm AMS CMOS process

parameters in order to validate the aforementioned synthesis approach. More specifically, a 0.1μW, 6Hz, 3rd order Bessel filter with a total capacitance of 150pF has been designed for ECG processing. Based on the cascade of two 3rd order sections, a 2.4Hz, 6th order CMOS Sinh Bessel filter has also been designed. The 3rd order topology achieves 110dB DR for <4% THD.

- A simulation study has been conducted for a 100Hz, 5th order CMOS Sinh low pass filter of Chebyshev approximation. The Sinh filter has been compared head-to-head with its pseudo-differential Log-domain class-AB counterpart of the exact same specifications, implemented by means of the Bernoulli-cell approach [217,262]. The comparison concluded that the SNR and SNDR performance achieved by the Sinh filters designed by means of the aforementioned methodology is similar to their Log-domain pseudo-differential class-AB counterparts but at the expense of higher power consumption from the same power supply level. This study is in agreement with the findings of the comparison of the CMOS Sinh building block itself with a 1st order pseudo-differential class-AB Log-domain topology of different implementation [157]. Therefore combining the results from both simulation studies, it can be safely deduced that CMOS Sinh filters constitute a solution of lower capacitor area, similar or better SNR and SNDR and mismatch performance at the expense of higher power consumption.

- An 8th order CMOS Sinh notch filter for 50/60Hz noise has been fabricated in the 0.35μm AMS technology and measured results from the fabricated chip have been reported. The Sinh filter was designed to fit the scope of state-of-the art commercial WBAN systems (e.g. Sensium™ [63]). Besides being the only measured high order CMOS Sinh topology which on its own is a significant research endeavour, it proves the excellent simulated

performance of its building blocks. It comprises 10 universal output first order sections based on a modification of the Sinh integrator in [154]. It is electronically tuneable over 2 decades and consumes 8μW at 50Hz from a 2V supply with a total capacitance of 200pF while achieving a DR of 89dB. A measured DR of +102dB has been recorded at the expense of 10 times higher power consumption. The notch achieves attenuation of 80dB at 50Hz. Despite its relatively large area (12mm^2), which was unavoidable due to the experimental character of the filter, the performance of the measured CMOS Sinh filter has verified the feasibility of CMOS Sinh low power designs and their inherent class-AB nature.

6.1.4 List of publications

- E. M. Kardoulaki*, et al.*, "An 8Hz, 0.1μW, 110+ dBs Sinh CMOS Bessel filter for ECG signals," in *Intl. Conf. on Microelectronics (ICM)*, 2009, pp. 14-17.
- E.M. Kardoulaki *et al.* "A Simulation Study of CMOS High-Order Hyperbolic-Sine Filters", *International Journal of Circuit Theory and Applications,* 2011, **under review**
- E.M. Kardoulaki *et al*. "A High Order 10Hz-1kHz CMOS Hyperbolic-Sine Notch Filter for 50Hz/60Hz Noise", *IEEE Transactions on Circuits and Systems- I*, 2011, **under review**

6.2 Future work

Although the work presented here has confirmed the potential of the Sinh filtering paradigm and in particular for low power, low-audio frequency applications there is a lot of margin for further optimisation/improvement and a number of possibilities to take this research further will be stated in this section. It is the hope of the author that this work will motivate others to conduct further research on Sinh topologies.

6.2.1 An 8th order CMOS Sinh notch for 50/60Hz noise

As explained, the notch filter presented in Chapter 5 was designed in order to meet the specifications of a commercial product (Sensium^{TM} [63]). The experimental character of the chip and for the reasons explained, the large chip area was inevitable. This is the main drawback of the topology for the particular application since the Sensium chip itself occupies almost the same area as the proposed notch filter [63]. In order for it to be suitable for the Sensium chip, it should not only be optimised for smaller device sizes and smaller capacitors but it should also be implemented in the 0.13μm CMOS technology under 1-1.8V at most of power supply. Lower power supply can be achieved by using alternating TL loops (such as those presented in Chapter 3) for the implementation of the GMS and the multipliers/dividers. Moreover, all the current sources have to be made PTAT in order for the chip to be temperature insensitive. Finally due to the harmonic content of the 50/60Hz mains noise, it would be useful for the notch filter to be adaptive [118,276-278]. An adaptive Log-domain filter has been presented in [279].

6.2.2 CMOS Sinh integrators

The practical CMOS Sinh integrator in [154] which has been the building block of all novel topologies presented in this work has been thoroughly investigated [157] and its simulated performance has been confirmed with measured results [229]. It is currently the only Sinh topology with +110dB DR and which only comprises p-type devices in its TL loops. However, there are a number of possibilities to be explored in order to improve its performance. Besides using alternating TL loops for lower power supply, the GMS could be substituted by a HM splitter in order to reduce cross-over distortion [207]. This is possible due to the current splitter being de-coupled from the rest of the topology. A fully HM Sinh integrator has been presented in [207] but its simulated performance could not justify its complexity when compared to the GM integrator. This could be attributed to the complexity of the HM sinh/cosh transconductor itself as well as to the necessary subtraction of a dc current from each of the multipliers. If however a HM splitter is used in combination with the GM sinh/cosh transconductor, the improvement in the cross-over distortion might be significant without an increase in the power consumption, noise and complexity of the topology.

Moreover, in order to improve the noise performance of the topology, it might be useful to include -depending on the power budget- a noise cancelling technique for the current splitter such as the one reported in [281]. An improvement in the DR by 13dB has been reported but at the penalty of 15% increase of power consumption. Other noise cancelling techniques could be investigated.

A fully differential topology could also further improve the linearity of the integrator taking care of the more accurate cancelling of the even order harmonics. A fully differential sinh/cosh transconductor could be possible by employing two sinh/cosh transconductors [154] and a sinh inverter [246] to apply $-V_{cap}$ to the second transconductor. The increase in

the power consumption and chip area will be inevitable but it is worth investigating the improvement in the DR for applications with the required power and area budget that would benefit from a further increase in DR.

Another interesting point in the topology of the Sinh integrator [154] is that its multipliers rely on pseudo-differential class-AB operation unlike the topologies of the GM splitter and sinh/cosh transconductor which are inherently class-AB. This implies that the accurate performance of the integrator relies entirely on the tight matching of the two class-A multipliers. Alternatives to the implementation of a class-AB multiplier have been suggested in [252-253] and might suit better the scope of an inherently class-AB Sinh integrator and should be further investigated.

6.2.3 CMOS Sinh biquadratic filters

Work on biquadratic CMOS Sinh filters has been conducted in [230]. In order for the complete validation of the performance of Sinh filters, biquadratic Sinh topologies need to be fabricated and tested. Moreover, high order topologies need to be designed, fabricated and tested based on cascades of biquadratic and 1st order Sinh sections. The possible challenge in the performance of biquadratic Sinh filters in achieving high Q's. The accuracy of the programmable gain which is implemented by means of a TL loop (stacked or alternating) of CMOS weakly inverted devices will play an important role in the performance of CMOS Sinh biquads. Alternative implementations of the programmable gain should be investigated in order to overcome the susceptibility of the performance of the integrator to the exponential conformity of the MOS devices forming the dividers. This would improve the linearity of the topology and would allow for high Q biquadratic structures.

6.2.4 **Integrated Sinh filters for high frequency applications**

The suitability of weak inversion CMOS Sinh filters for low power and low frequency applications was the topic of this research. However, a lot of possibilities open for the applicability of the Sinh filtering paradigm for high frequency applications when they are implemented in bipolar or BiCMOS technologies where they can benefit from the wide range of exponential conformity and the large f_T values of the devices. An area where Sinh filtering could be particularly attractive compared to standard methods is in the implementation of active complex (polyphase) filters for Low-IF receivers (Figure 6.1) for Bluetooth/Zigbee specifications. In a low-IF receiver topology, a complex filter (Figure 6.2) helps attenuate the image signal and the folded-back strong interference after the down-conversion. The design of a low power complex filter with sufficient image attenuation is very difficult to achieve while the IF is low. Upon mixing the RF signal passed through the LNA with two quadrature LO outputs, both signal and its image are downshifted to the IF at the outputs of the I and Q mixers. If I and Q are viewed as the real and the imaginary part of a complex signal, the wanted signal will be situated at the centre of frequency ω_{IF} while the image signal at frequency - $\omega_{IF.}$ The image rejection can be performed successfully using a complex filter.

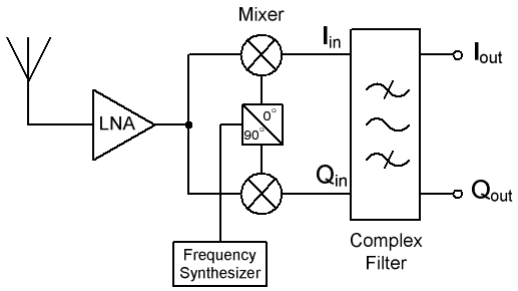


Figure 6.1: Front-end topology of a low-IF receiver [282].

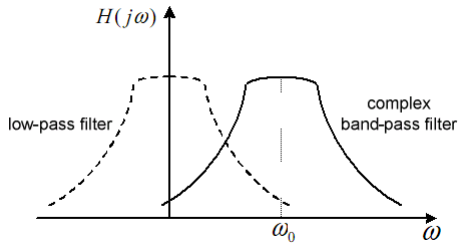


Figure 6.2: Transfer function of a low-pass filter and its derived complex band pass filter [282].

Conventionally, active-RC or g_m-C topologies are used for implementing complex filters on chip with CMOS technologies. An active-RC 4th order complex filter based on a class-AB opamp with centre frequency at 2MHz has been proposed in [284]. It operates from

1.8V supply, consumes less than 4.5mW while achieving more than 40dB rejection of the image frequency. The DR of the filter is 80dB. The chip has been implemented in the 0.18µm technology. Another complex filter topology is presented in [282] and has adopted the G_m-C approach making use of linearized transconductors in order to improve the linearity and DR of the filter. The topology has been implemented in the 0.18µm RF CMOS process and operates from 1.8V consuming less than 5mW while achieving attenuation of 60dB at the image frequency. A 12^{th} order OTA-C complex filter centred at 2MHz has been proposed in [284]. The filter has been implemented in 0.35µm CMOS technology and is capable of more than 45dB rejection of the image frequency. It operates from 2.7V supply and consumes 4.7mA.

Recently Log-domain complex filters have also been proposed [285-287]. The 12^{th} order leapfrog Log-domain complex filter presented in [287] has been simulated in the 0.35µm BiCMOS AMS process and operates from 1.2V supply consuming 10mW. Its total capacitance is however unacceptably large for integration on chip (1600pF). Another realisation of a 12^{th} order complex filter has been presented in [288]. The topology is a 6^{th} order leapfrog filter where each integrator is a complex lossy /lossless integrator implemented by means of Wilson current mirrors and capacitors in the 0.35µm CMOS technology. It operates from 1.5V supply and consumes 3.2mW. It is also worth mentioning that he implementation of analogue gammatone filters for cochlea implants based on G_m-C complex filters has been reported in [289].

Due to the importance of high DR, low power and small integration area required for the particular applications, Sinh topologies with their inherent class-AB companding properties and electronic tuning ability would be a good solution for the implementation of active complex filters and further investigation is justified.

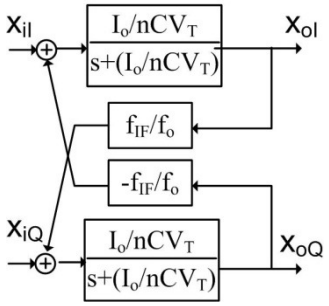


Figure 6.3: Functional block diagram of a complex 1st order lossy integrator. Each real lossy integrator can be realized by means of a bipolar/BiCMOS Sinh lossy integrator [290-292] and the gain cells (f_{IF}/f_o) and ($-f_{IF}/f_o$) can be implemented by means of four programmable multipliers each to multiply the upper and lower phases of the real (x_{oI}) and imaginary (x_{oQ}) outputs respectively prior to their addition to the two inputs as indicated.

Another area where Sinh filters implemented in bipolar or BiCMOS technologies could be particularly attractive is for the implementation of the beamformers in medical ultrasound imaging systems. Ultrasound is one of the fastest-growing medical imaging modalities [293-295] due its relative simplicity, low cost, and radiation-free operation. Small, portable ultrasound machines can now be found in the operating rooms for needle guidance as well as in emergency rooms and on ambulances. Regardless of their size, cost, or clinical use, ultrasound machines have three distinct subsystems: the transducer and its cable assembly, the front-end electronics, and the back-end computer with its user interface and display. One of the most critical components of the front-end electronics is the beamformer.

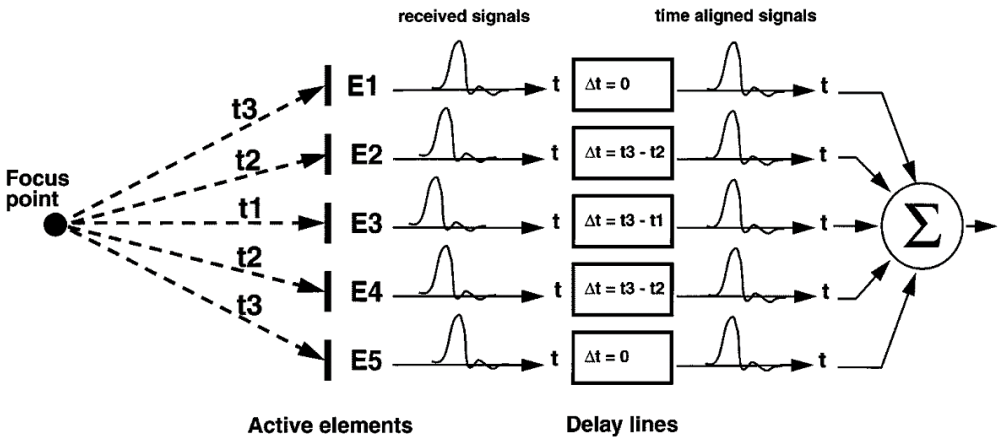


Figure 6.4: Receive beamforming process [296].

Beam formation and focusing is a common signal-processing technique used in various applications such as wireless communications, (radar and sonar) that use an array of sensors (or elements) of any geometry for transmitting and receiving radio or sound waves. Beamforming enables directional (or spatial) selectivity of the signal transmission and/or reception. In medical ultrasound, beamforming is used to focus the echo signals received as reflections from different tissue structures in the region of interest by appropriately delaying echo signals arriving at different transducer elements in order to align them in a way that an isophase plane is created. These aligned echoes are then all summed coherently (Figure 6.4). On the transmit side, focused beams of ultrasound are generated in order to be steered over the volume being imaged. They are created using a phased array by providing a high voltage pulse or a series of coded pulses to each of the transmitting array elements [297]. Each pulse is appropriately delayed relative to each other to create a beam in the desired direction of a focal point. The more the elements used for the transmission, the better the image SNR. The receiving electronics typically include, preamplifiers, time-gain compensation (TGC) to equalize the amplitude of the echoes received from different distances and the receive beamformer (Figure 6.4). ADCs convert the signals to digital for further processing. In systems with few receiving elements, it is possible to convert the received signals to digital prior to receive beamforming with a reasonable amount of resources and power consumption [298]. For large 2-D arrays however, providing ADCs to every element is not practical [299].

3-D ultrasound imaging systems have become progressively important since they can form 2-D image planes in any orientation relative to the ultrasound transducer array and can acquire volumetric images. These capabilities simplify the image acquisition and aid making quantitative measurements quickly based on the acquired image data while reducing the degree of dependence on the skills of the sonographer [298]. State-of-the art 3D medical ultrasound imaging requires transmitting and receiving ultrasound signals using 2-D arrays of

ultrasound transducers with hundreds or thousands of elements. Early 3-D ultrasound systems used sparsely populated 2-D arrays or mechanically scanned 1-D arrays. Modern systems however, use fully populated 2-D arrays in order to increase the image quality which is dependant on the number of the elements in the array. Connecting to and processing of the signals from the elements requires sophisticated packaging and electronics. Incorporating some of the electronics into the hand-held part of the system, improves the receive sensitivity and results in fewer cables. Furthermore compact connection between the array of transducers and the electronic system can result in even higher integration and hence drive the cost of the whole system down even further. A combined IC and transducer array, can lead to a portable, high performance and inexpensive 3-D ultrasound imaging system [300-301]. Micro machined [300] and polymer-based transducer technologies allow for the direct fabrication of the transducer array on integrated circuits [298].

A number of analogue implementations of beamformers based on the delay and sum architectures (Figure 6.4) have been proposed [296,303-305]. However all of the implementations are characterized by large power consumption (100s mW-W). Large power consumption is a limiting factor to the integration of the beamformer in the probe handle due to the strict requirements regarding heat generation in such an application [281].

Analogue delay lines based on cascades of all-pass filters implemented by means of class-AB companding filters would be an attractive solution to a high DR performance while low power consumption under low power supply is achieved. A fully differential class-AB log-domain microbeamformer has been proposed by Halvorsrod *et al.* [281]. The demonstrated microbeamformer has been implemented in the 60GHz Si-Ge BiCMOS process and consists of three cascaded delay cells and four input signals. All inputs can be connected to an arbitrary delay tap on the delay line. The simulated global DR amounts to 60dB at a

power consumption of 3.2mW from a 2.5V power supply which is significantly better than all other analogue beamformer implementations reported to date [296,303-305].

This has motivated the implemention the proposed system in [281] by means of Sinh all pass filters implemented in the 0.25 μm Si/Ge bipolar technology [291-292]. Work on bipolar Sinh implementations has been carried out under the author's co-supervision of an MSc project firstly in order to exploit the full potential of Sinh filters by means of bipolar technology where the devices in the TL loops are expected to operate over a wider current range. Bipolar Sinh integrator, biquadratic and high order Sinh filters have been designed and simulated [290]. The CMOS Sinh integrator topology in [154] has been mapped into a bipolar implementation comprising npn devices in the TL loops and pnp and npn current mirrors where necessary. The only difference between the CMOS [154] and the bipolar Sinh integrator topologies is that in the bipolar implementation, alternating TL loops are used for the multipliers/dividers in order to minimize the errors due to base currents. The bipolar Sinh integrator is able to reach cut-off frequencies up to 100MHz while its DR is as high as 90dB. The implementation of the proposed Log-domain delay line system in [281] by means of bipolar Sinh filters (Figure 6.5) and the comparison of the two systems is reported in two BEng projects [291-292] carried out under the author's co-supervision. The Sinh implementation was found to outperform the pseudo-differential Log-domain class-AB implementation in both DR and power consumption. Indicative results from the transient simulation of the block diagram of Figure 6.5 which illustrates the implementation of a Sinh delay and sum beamformenr topology are presented in Figure 6.6.

Due to these promising results, it is worth further investigating the performance of a Sinh micro-beamformer. More optimisation is required for the bipolar Sinh implementations in order to match the high DR performance of their CMOS counterparts. In addition, different

implementations of a programmable delay [303] or different beamformer architectures could be investigated.

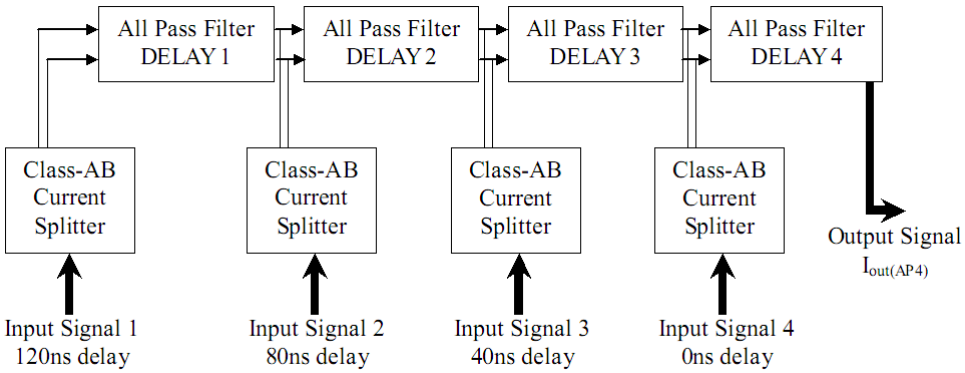


Figure 6.5: Sinh micro-beamformer with four cascaded all pass cells and four inputs successively delayed by increments of 40ns [291].

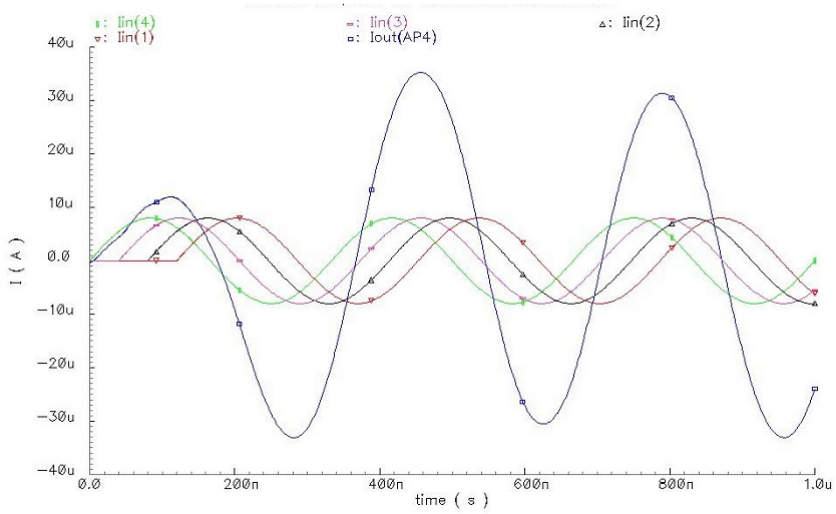


Figure 6.6: Transient response of the beamformer in Figure 6.5 with 2mW static power consumption [291].

Appendix A

The measured small-signal frequency responses from the 4th order output of the Sinh notch filter are illustrated in Figure 6.7 (red). While eight responses from the 4th order output of the filter are depicted in Figure 6.8.

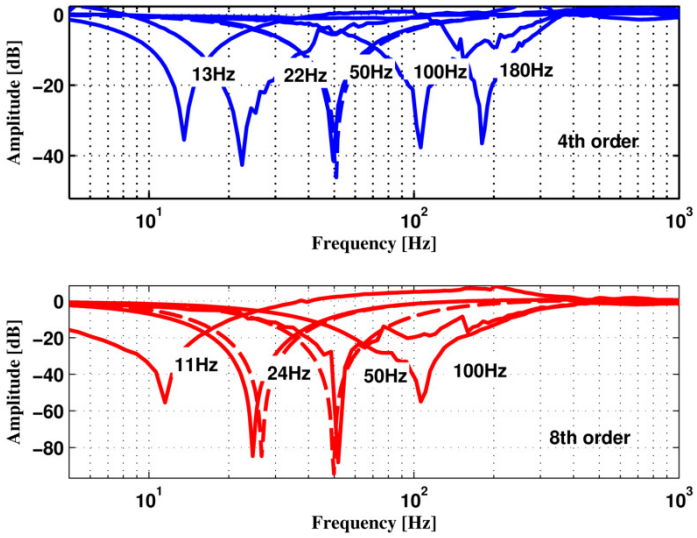


Figure 6.7: Tuning of the 4th /8th order notch by means of $I_{o1\text{-}3}$ currents (all capacitors are 20pF). Here I_{o1} is kept at 10nA and I_{o2}, I_{o3} vary to tune the notch frequency. The results are obtained for a value of M.I. m=20. The simulated results are represented with dashed lines.

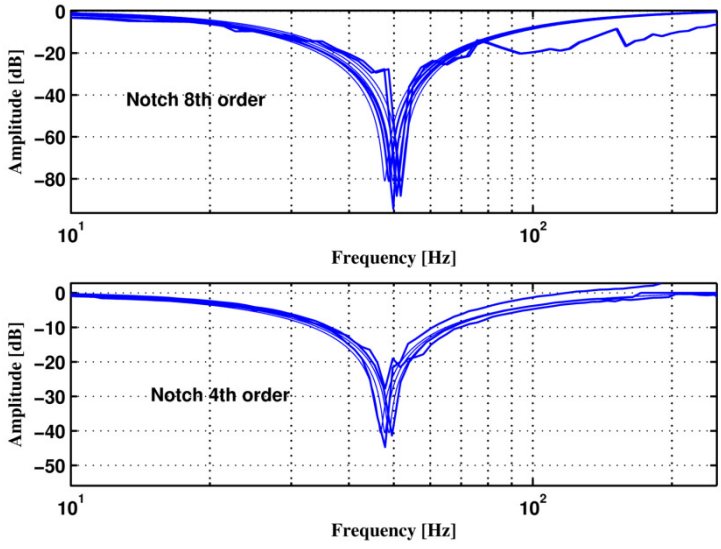


Figure 6.8: Variation across 8 chips. Both 4th and 8th order outputs at 50Hz are illustrated. Note that these graphs correspond to the selected best results out of 20 fabricated Sinh notch chips.

Appendix B

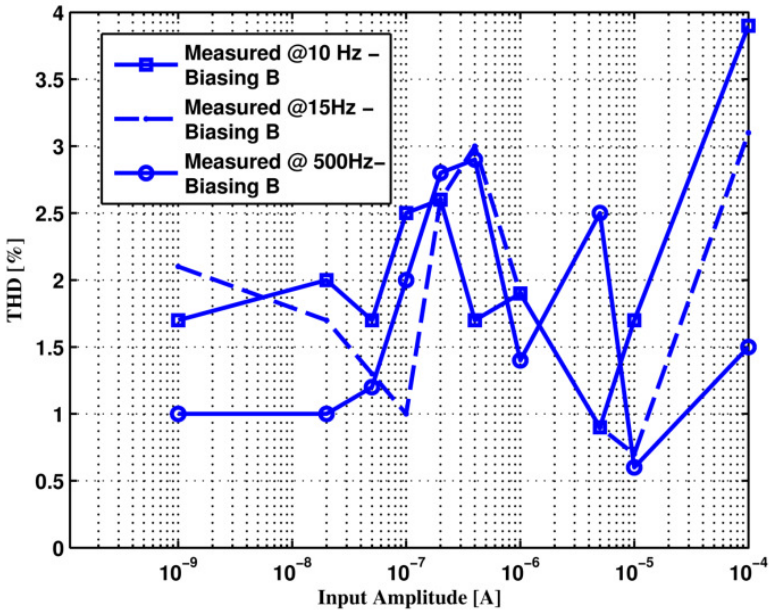


Figure 6.9: THD versus increasing input current amplitude for various input frequencies in the passband of the notch filter tuned at 100Hz.

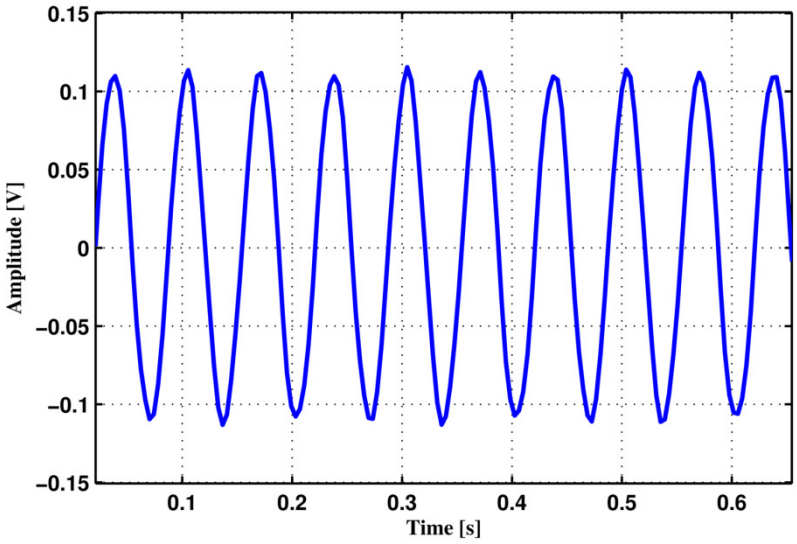


Figure 6.10: Recorded transient response at the output of the 8th order notch tuned at 100Hz. The input tone is a 15Hz sinusoid of 1μA amplitude. The output current is converted to voltage through a 100kΩ resistor. The output waveform corresponds to a THD value of 1.43%.

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