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Effect of a Polywell geometry on a CMOS Photodiode Array

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PROCEEDINGS



September 27-29, 2010
Bally's
Las Vegas, Nevada, USA.

PROCEEDINGS

IEEE International SOC Conference

September 27-29, 2010
Bally's
Las Vegas, Nevada, USA.

Editors

Thomas Buechner
IBM Corp.

Andrew Marshall
Texas Instruments

Ramalingam Sridhar
University at Buffalo

Norbert Schuhmann,
Fraunhofer Institute for Integrated Circuits

The SOC Conference is sponsored by the IEEE Circuits and Systems Society

IEEE International SOC Conference
Digest of Technical Papers

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Message from General Chair

On behalf of the Organizing Committee, I am delighted to welcome you to the 23rd IEEE International SoC Conference (SOCC 2010) in Las Vegas, Nevada.

During the last three decades, application specific microelectronics has grown from a small market to one of the most important economic factors, dominating most parts of our work and life. Consequently, IEEE SOCC and its predecessors IEEE ASIC/SOC and IEEE ASIC have accompanied engineers and engineering managers for more than two of these three decades now, always showing the latest trends of our times.

In the meantime, ubiquitous computing, mobile communication, and their underlying hardware are about to change our society and the way we communicate and interact with each others. While in the nineties of the last century, the rise of the Internet and the “dotcom” revolution were fueling the growing demand for high speed networks and high performance computing, it is now the new and fast growing “always on” generation that drives the development of new devices and applications that have already started to pervade all parts of our daily lives.

You, the engineer of the 21st century, have the responsibility to provide the hardware for this networked society. The integration of an entire system onto a single silicon chip is one of the driving factors behind this electronic revolution and has become a major requirement to tackle the increasing cost of manufacturing those ever shrinking transistors - and to keep Moore's Law alive for many more years.

From the highly integrated Systems-on-Chip (SoC) needed for smart handheld devices, high definition video processing, home automation, or car electronics, over bio electronics revolutionizing our medicine, to high performance computers to simulate climate change, there is a wide spectrum of applications - and also of knowledge that you need to gain and maintain to stay competitive as an engineer in a global market.

In addition to that, nowadays not only function and performance but also environmental issues play an important role in our industry. Issues like low power consumption, “green” manufacturing, and a low carbon footprint over the whole lifetime of a product are becoming more and more important. The way we are developing and manufacturing our systems today will affect the way we and our children will live in the future - and help us and them to build and shape a smarter planet.

To help you to achieve these goals, SOCC 2010 provides a forum for sharing recent progress and discussing new challenges in SoC research and development, bringing together experts from both industry and academia to discuss and solve critical hardware and software issues in SoC technologies. Our Technical Program Chairs, Prof. Ramalingam Sridhar from the University of Buffalo, and Norbert Schuhmann from the Fraunhofer Institute for Integrated Circuits in Germany have put together a comprehensive technical program covering all aspects of SoC development.

We are as well excited to welcome our distinguished keynote speaker, Prof, Alberto Sangiovanni-Vincentelli, Professor, University of California at Berkeley & Chief Technology Advisor, Cadence Design Systems, our two plenary speakers, Michael Keating, Fellow, Synopsys, Inc, Sandra Woodward, Senior Technical Staff Member, IBM Corp., Jo Dale Carothers, Partner, Covington & Burling LLP and our Luncheon Speaker, P.R.Mukund, President and CEO of NanoArk Corp.

It is worth to mention that even during these times of economic depression, job insecurity and globalization pressure, IEEE SOCC continues to be a stable and reliable source for you to stay competitive in a rapidly changing engineering environment. I am especially proud that this year we were able to increase the number of paper submissions, in spite of the trend we see at many other



conferences. Being able to select the best papers from a large number of high quality submissions helps us to maintain the quality that our conference attendees are expecting from us.

Therefore, my first and sincerest thanks go to our authors and attendees. This conference is made for you and it is first and foremost you who make this conference a success.

I also would like to express my sincere gratitude to the members of the Organizing, Technical Program, and Local Committees. Without your generous contribution of time and effort this conference would not have happened.

In this spirit, I wish you all a productive and enjoyable stay in Las Vegas

Thomas Büchner
IBM Germany Research & Development
SOCC 2010 General Chair

Andrew Marshall
Texas Instruments
SOCC 2010 General Co-Chair

Message from Technical Chair

On behalf of the Technical Program Committee we welcome you to the 23rd IEEE International System-on-Chip (SOC) Conference (SOCC 2010), held this year in Las Vegas, Nevada, USA. This Conference has grown along with the tremendous growth of ASICs and System on Chips over the years. This conference continues to be a premier forum for education and dissemination of new ideas and research in all aspect of System on Chips.

We understand the importance of a strong technical program to the success of the conference, and hence we strive hard to bring quality to the program and value to the conference attendees. We are thankful to all the area track chairs and co-chairs, for their valuable time and hard work in putting together this technical program that addresses many facets of SOC technology, design and applications. Quality submissions and review will not be possible without the help of our Technical Program Committee members and 115 reviewers. This year we received a total of 150 high quality submissions from 24 countries, from which we have selected 62 papers for regular presentation and 29 for poster presentation. Regrettably, many of the papers of high quality could not be accommodated due to time and space limitations.



The program comprises of two plenary sessions, one on Monday and the other on Wednesday, fifteen technical sessions in two parallel tracks, three embedded tutorials, a poster session and a panel discussion. We are privileged to have many eminent speakers with enormous experience in diverse topics of SOC to be participating as the Keynote, Plenary and Luncheon speakers and as panelists in the panel discussion. We are very thankful to Dr. Alberto Sangiovanni-Vincentelli, who has been at the forefront of VLSI and SOC for many decades, and has a unique perspective as a highly accomplished Professor of University of California at Berkeley and as the co-founder of two of the most successful CAD companies, Cadence and Synopsys. The first plenary speaker, Michael Keating, Synopsys Fellow, with expertise in IP based design, low power and reuse methodology will focus on code-based scalable design, whereas the second plenary speaker with expertise in the area of Microprocessor and Memory Hierarchy Architecture will talk about technical challenges of a large complex SOC (PowerEN) for next generation systems. Our luncheon speaker Dr. P. R. Mukund and the third plenary speaker Dr. Jo Dale Carothers both return to SOC Conference in their new role after many years of service to this conference. Dr. Mukund will talk about his novel venture in using Silicon wafers to store and preserve archival manuscripts. Dr. Carothers in her new role as a legal professional in Intellectual Property litigation talks about our role in patent litigation. Our panel with participation from many of these experts and others will focus on the importance of software and hardware in future SOC designs. We are confident that the entire program will provide the audience with great value and vision of the future directions of the SOC.

We also thank the entire Organizing committee for their numerous contributions throughout the development of this program. Also, we thank Wendy Walker for her administrative support.

SOCC is sponsored by the IEEE Circuits and Systems Society

Ramalingam Sridhar,
University at Buffalo, The State University of New York, Buffalo, NY
SOCC 2010 Technical Program Chair

Norbert Schuhmann,
Fraunhofer Institute for Integrated Circuits, Germany
SOCC 2010 Technical Program Co-Chair

PROGRAM-AT-A GLANCE

Monday, September 27

Registration	7:00 a.m. – 5:00 p.m.
Plenary Session	8:30 a.m. – 12:00 noon.
Open Lunch	12:00 noon – 1:00 p.m.
Technical Sessions	1:00 p.m. – 2:40 p.m.
Embedded Tutorial	2:55 p.m. – 3:45 p.m.
Technical Sessions	3:45 p.m. – 5:00 p.m.
Embedded Tutorial	5:00 p.m. – 6:00 p.m.

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Registration	7:30 a.m. – 5:00 p.m.
Technical Sessions	8:00 a.m. – 9:40 a.m.
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Panel Discussion	6:00 p.m. – 7:30 p.m.

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Technical Sections	1:00 p.m. – 2:40 p.m.
Conference ends	2:40 p.m.

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MPL SESSION

Keynote/Plenary Session

General Chair: Thomas Büchner, IBM
Co-Chair: Andrew Marshall, Texas Instruments

Keynote Speaker

Alberto Sangiovanni-Vincentelli

**Professor, University of California at Berkeley, and
Chief Technology Advisor, Cadence Design Systems**

“SoC Design as an Example of Component-Based Design of Distributed Systems”



Alberto Sangiovanni Vincentelli holds the [Edgar L. and Harold H. Buttner Chair](#) of [Electrical Engineering and Computer Sciences](#) at the [University of California at Berkeley](#). He has been on the Faculty since 1976. He obtained an electrical engineering and computer science degree ("Dottore in Ingegneria") *summa cum laude* from the Politecnico di Milano, Milano, Italy in 1971. In 1980-1981, he spent a year as a Visiting Scientist at the Mathematical Sciences Department of the IBM T.J. Watson Research Center. In 1987, he was Visiting Professor at MIT. He has held a number of visiting professor positions at Italian Universities, including Politecnico di Torino, Università di Roma, La Sapienza, Università di Roma, Tor Vergata, Università di Pavia, Università di Pisa, Scuola di Sant' Anna.

He was a co-founder of [Cadence](#) and [Synopsys](#), the two leading companies in the area of Electronic Design Automation. He is the Chief Technology Adviser of Cadence. He is a member of the Board of Directors of Cadence and the Chair of its Technology Committee, UPEK, a company he helped spinning off from ST Microelectronics, Sonics, and Accent, an ST Microelectronics-Cadence joint venture he helped founding. He was a member of the HP Strategic Technology Advisory Board, and is a member of the Science and Technology Advisory Board of General Motors and of the Scientific Council of the Tronchetti Provera foundation and of the Snaidero Foundation. He consulted for many companies including Bell Labs, IBM, Intel, United Technologies Corporation, COMAU, Magneti Marelli, Pirelli, BMW, Daimler-Chrysler, Fujitsu, Kawasaki Steel, Sony, ST, United Technologies Corporation and Hitachi. He was an advisor to the Singapore Government for microelectronics and new ventures. He consulted for Greylock Ventures and for Vertex Investment Venture Capital funds. He is a member of the Advisory Board of Walden International, Sofinnova and Innogest Venture Capital funds and a member of the Investment Committee of a novel VC fund, Atlante Ventures, by Banca Intesa/San Paolo. He is the founder and Scientific Director of the Project on Advanced Research on Architectures and Design of Electronic Systems (PARADES), a European Group of Economic Interest supported by Cadence, Magneti-Marelli and ST Microelectronics. He is a member of the Advisory Board of the Lester Center for Innovation of the Haas School of Business and of the Center for Western European Studies and is a member of the Berkeley Roundtable of the International Economy (BRIE). He is a member of the High-Level Group, of the Steering Committee, of the Governing Board and of the Public Authorities Board of the EU Artemis Joint Technology Initiative. He is member of the Scientific Council of the Italian National Science Foundation (CNR).

In 1981, he received the Distinguished Teaching Award of the University of California. He received the worldwide 1995 Graduate Teaching Award of the IEEE (a Technical Field award for “inspirational teaching of graduate students”). In 2002, he was the recipient of the Aristotle Award of the Semiconductor Research Corporation. He has received numerous research awards including the Guillemin-Cauer Award (1982-1983), the Darlington Award (1987-1988) of the IEEE for the best paper bridging theory and applications, and two awards for the best paper published in the IEEE Transactions on CAS and CAD, five best paper awards and one best presentation awards at the Design Automation Conference, other best paper awards at the Real-Time Systems Symposium and the VLSI Conference. In 2001, he was given the Kaufman Award of the Electronic Design Automation Council for “pioneering contributions to EDA”. In 2008, he was awarded the IEEE/RSE Wolfson James Clerk Maxwell Medal “for groundbreaking contributions that have had an exceptional impact on the development of electronics

and electrical engineering or related fields” with the following citation: ”For pioneering innovation and leadership in electronic design automation that have enabled the design of modern electronics systems and their industrial implementation.” In 2009, he received the first ACM/IEEE A. Richard Newton Technical Impact Award in Electronic Design Automation to honor persons for an outstanding technical contribution within the scope of electronic design automation. In 2009, he was awarded an honorary Doctorate by the University of Aalborg in Denmark.

He is an author of over 850 papers, 15 books and 3 patents in the area of design tools and methodologies, large-scale systems, embedded systems, hybrid systems and innovation.

Dr. Sangiovanni-Vincentelli has been a Fellow of the IEEE since 1982 and a Member of the National Academy of Engineering, the highest honor bestowed upon a US engineer, since 1998.

Abstract:

As the complexity of IC design grows, component-based design and correct-by-construction techniques become indispensable to make it possible to develop new application specific designs or even new high volume devices such as microprocessors. While many design methods have been proposed over the years to solve the cost and time-to-market issues, industry is still not able to deploy widely new methods. However, research in recent years has made important inroads, semiconductor companies have implemented more structured design methodologies and EDA/IP enterprises have made significant investment in new tools and design environments. In this talk we will review some of the most interesting approaches that are based on interconnect and communication design as well as heterogeneous composition of components with the goal of pointing out some promising avenues to make SoC design economically attractive for a wide variety of applications

Plenary Speaker

Michael Keating

**Fellow,
Synopsys, Inc.**

"Third Revolution: The Search for Scalable Code-Based Design"



Mike Keating is a Synopsys Fellow. He has been with Synopsys for 13 years, focusing on IP development methodology, hardware and software design quality and low power design. His current research focuses on high level design and the challenges of designing extremely complex systems. Mike received his BSEE and MSEE from Stanford University, and has over 25 years experience in ASIC and system design. He is co-author of the *Reuse Methodology Manual* and the *Low Power Methodology Manual*. In 2007, ISQED gave Mike the Quality Award for contributions to quality in electronic design.

Abstract:

Over the last 25 years, there have been two major revolutions in how we do digital design: the move to language/synthesis based design (starting in 1986) and design reuse (starting around 1996). We are well overdue for a third revolution. Current design methods are not meeting the needs dictated by the complexity and size of today's SoC designs, much less the designs of the future.

This talk will describe the current candidates for the next revolution in digital design: high level synthesis, chip generators, and radical extensions to the synthesizable subset of current RTL languages. It will also describe how the economics of SoC design and manufacturing, as well as the economics of EDA, will affect and possibly de-rail the third revolution.

Plenary Speaker

Sandra Woodward

**Senior Technical Staff Member, Prism WSP SOC Chip Technical Lead
IBM Corp.**

"A Wire-Speed Processor System-on-a-Chip (SOC): Technical Overview and Challenges for a Large Complex SOC used in Next-Generation Systems"



Sandra Woodward is a Senior Technical Staff Member at IBM and is currently the Chip Technical Lead for the Wire-Speed Processor System-on-a-Chip (SOC) development. She is an expert in the area of Microprocessor and Memory Hierarchy Architecture, Design and Methodology. She has experience in System-on-a-Chip (SOC) design, ASIC design, Power(TM) architecture, and Cache and Coherency function design. Mrs. Woodward holds a B.S. degree in Electrical Engineering (EE) from the University of Nebraska and an M.S. degree in EE from Syracuse University

Abstract:

This presentation will give a technical overview on one of the most complex chips IBM has ever built: the Wire-Speed Processor (WSP) System-on-a-Chip (SOC). This includes the general purpose processing subsystem, the special purpose accelerator subsystem, the network I/O subsystem, and the interconnect for on-chip and off-chip coherency. It will explore the challenges and trade-offs made on the WSP SOC which is integrated into a Next-Generation System. This includes items such as lower power, increased computational performance, and heterogeneous compute elements. It will also discuss the implications of technology advancement on architectural and functional design decisions and point out problems requiring solutions for the large, complex System-on-a-Chip designs in the future.

Effect of a Polywell Geometry on a CMOS Photodiode Array

Paul V. Jansz, Steven Hinckley and Graham Wild

Optics Research Laboratory, Centre for Communications Engineering Research,
Edith Cowan University, Joondalup, WA, Australia.
(p.jansz@ecu.edu.au)

ABSTRACT

The effect of a polywell geometry hybridized with a stacked gradient poly-homojunction architecture, on the response of a CMOS compatible photodiode array was simulated. Crosstalk and sensitivity improved compared to the polywell geometry alone, for both back and front illumination.

Keywords- CMOS; crosstalk; polywell; stacked gradient poly-homojunction; quantum efficiency; wavelength sensitivity

I. INTRODUCTION

The need for CMOS photodiode structures with enhanced UV/blue responsivity has led to the development of polywell structures [1]. The polywell geometry involves having multiple wells per pixel rather than just one well. This geometry has this benefit because each pixel is depleted up to the frontwall and 99.9% of UV/blue light is absorbed within the first $1\mu\text{m}$ depth of the device.

Such photodiodes could be used for micro-bioluminescent assays [2]; biosensors based on absorption photometry [3]; Blue Ray optical data storage devices, for which data rates over 500 Mb/s as well as sufficient sensitivity at 410 nm [4] are needed; and for scintillation detector applications [5]. Imaging in the ultra-violet (UV) is of interest to many areas, including particle detection, plasma spectroscopy, astrophysics, and dosimetry [6], as well as to biomedical areas including electrophoretic band detection [7].

Multi-pixel imaging requires enhanced sensitivity and crosstalk suppression. Such polywell photodiodes may benefit quantum efficiency (QE) as well as crosstalk suppression across a broader wavelength band than for conventional PD geometries [8] – [10].

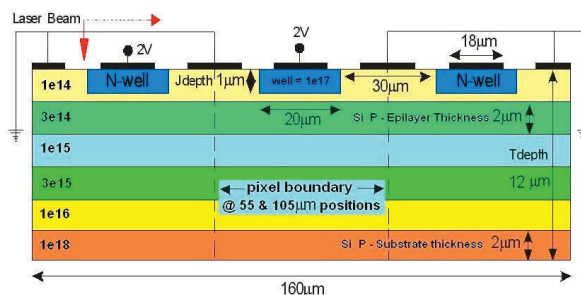


Figure 1. The primitive staG Photodiode array [12].

The stacked gradient poly-homojunction (staG) architecture (Fig. 1) has demonstrated improved sensitivity and crosstalk suppression [11] – [12]. Adding this structure to the polywell device may benefit the hybrid in improved response resolution. Complicating the architecture with nested ridges or boundary trenches [13] – [15] only serves to reduce fill factor slightly.

As in previous work, backwall illumination (BW) of such photodiode geometries is of interest due to the ability to tailor individual photodiodes to a specific wavelength band. [16]. To date, studies on polywell photodiodes have only considered frontwall illumination (FW).

This investigation adds to other work performed to achieve devices that balance the maximization of response resolution with the minimization of device fabrication complexity [12] – [21]. Though the staG genre have excellent response characteristics, their fabrication is still complex [15].

Investigated here is the effect on the photodiode's response resolution of the width and spacing of the polywells. This is with and without the staG geometry. This is investigated at three wavelengths: 400, 633 and 850 nm. The Ghazi [1] geometry is adapted for a three pixel lateral array.

The polywell photodiode responsivity was compared with the staG photodiode geometries

[15] as well as other simulated vertical single junction photodiode (SJPD) geometries, including the guard junction or double junction photodiode (DJPD). Due to the advantages of back illumination [4], both illumination modes were investigated.

II. METHOD

The crosstalk and maximum quantum efficiency of the central pixel of the three pixel array (Fig. 2) was simulated using SEMICAD DEVICE (v1.2). This geometry allowed comparison with previous simulated photodiodes [12] – [21]. The p-well and n-substrate doping were 10^{17} and 10^{15} cm^{-3} and the reverse bias voltage was 3 volts.

As previously [12] – [21], the simulated array was scanned at 5 μm intervals along the front and back of the array, using a simulated laser beam of 5 μm width and 0.1 μW power.

Crosstalk was compared using the Relative Crosstalk parameter: The Normalized quantum efficiency (QE) produced at the central Pixel for illumination just outside the central pixel at the 50 μm position.

Sensitivity was defined as the maximum QE produced at the central pixel for illumination over the central pixel.

Three, four, six and nine polywell geometries were simulated at incident wavelengths of 400, 633 and 850 nm, with and without a bilayer StaG architecture.

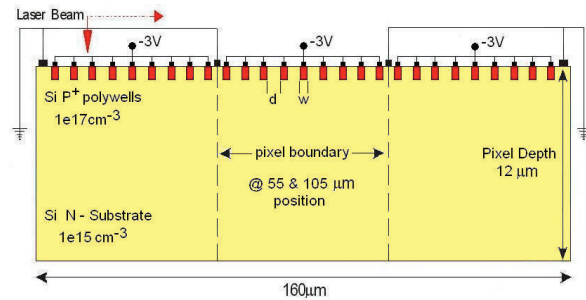


Figure 2. The polywell photodiode array without the epilayer which would make it a bilayer StaG polywell photodiode.

III. THEORY

Increasing the number of polywells will deplete more of the pixel volume between each polywell. This will benefit crosstalk and sensitivity. With the given bias and doping the width of the space charge region (SCR) is 2.207 μm benefiting the

shorter wavelength light. Carriers generated outside the SCR will undergo diffusion, resulting in a portion being swept into the SCR while the rest either recombine, or contribute to crosstalk.

The StaG geometry affects the carrier distribution by making it energetically more favorable for diffusing carriers to migrate in the direction of decreasing doping. This produces a potential gradient that drives the carriers towards the SCR [15] benefiting crosstalk and sensitivity.

IV. RESULTS AND DISCUSSION

A. Response Resolution at 400nm

The front (FW) and back (BW) illumination response is juxtaposed on the array geometry: Fig. 3 and Fig. 4, respectively.

The front illumination response was affected most by the placement of polywells. At 400 nm, most of the photocarriers were generated within 1 μm of the front wall, which is in the SCR for light falling over a polywell. This results in efficient collection by that polywell, while reducing the central pixel carrier capture. Alternatively, light falling between the polywells allows some portion of the carriers to diffuse into and be captured by the nearest central pixel's polywell. This becomes less pronounced as the number of wells increases and the substrate is more depleted.

Back illumination at 400nm shows no effect from polywell placement because carriers are generated near the back wall. The result is a diffusion dominated response and elevated crosstalk. The effect of the bilayer StaG geometry improves crosstalk and sensitivity, especially for front illumination.

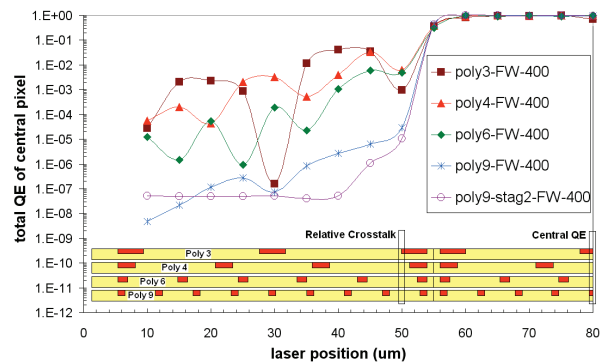


Figure 3. The effect of well and placement on FW polywell photodiode array response resolution. A Bilayer StaG polywell PD FW response is included for comparison.

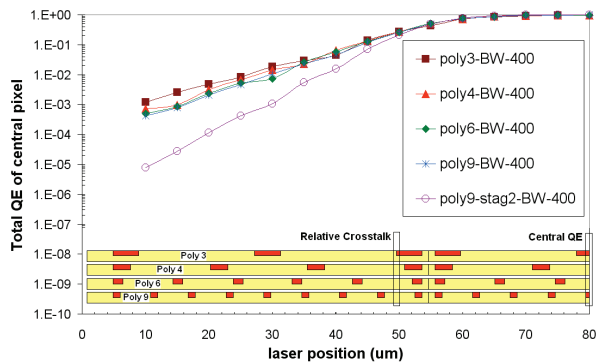


Figure 4. The effect of polywell number and placement on BW polywell photodiode array response resolution. A Bilayer Stag polywell 9 PD BW response is included for comparison.

B. Effect of wavelength on Poly 9 PD response.

Adding the StaG geometry immediately improves the crosstalk and QE for both modes of illumination. Secondly, as wavelength increased, the illumination response profile across the array moved closer together.

Not surprisingly, front illumination always shows healthier response resolution. The non-StaG, poly 9 FW 400 is elevated above the StaG 2 Poly 9 FW 400. StaG dynamics, operating in the later, reflect diffusing carriers back towards the SCR, benefiting response resolution.

C. Effect of Wavelength on Relative Crosstalk.

Fig. 5 shows little dependence on the wavelength for all of the back illuminated photodiodes, irrespective of the number of polywells per pixel. The slight reduction in crosstalk with wavelength increase is due to the longer wavelength light generating photocarriers closer to the SCR, increasing carrier capture. Front illuminated pixel crosstalk is dependent on wavelength and the

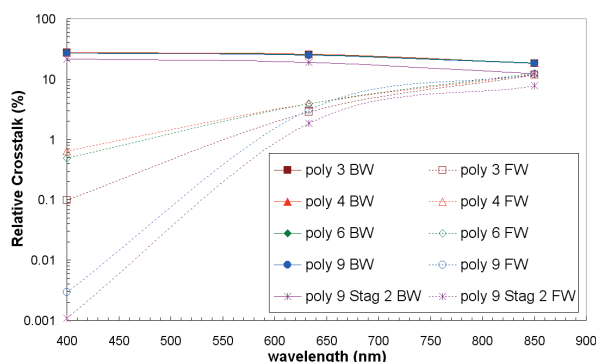


Figure 5. The effect of wavelength on crosstalk for the polywell PD and Polywell 9 StaG 2 layer photodiode.

number of polywells. As wavelength increases, less photo-carriers are generated in the SCR, adding to a diffusion response that increases crosstalk. The greater the number of polywells, the more extensive is each pixel's SCR, resulting in lower crosstalk and greater maximum QE.

D. Effect of Wavelength on Sensitivity.

Fig. 6 shows a decreasing trend in sensitivity with increasing wavelength because less light is absorbed. At 400 nm, the wavelength at which the photodiodes have demonstrated optimal response, the front illuminated (FW) pixels show marginally better sensitivity than the back illuminated (BW) pixels. This margin decreases with longer wavelength.

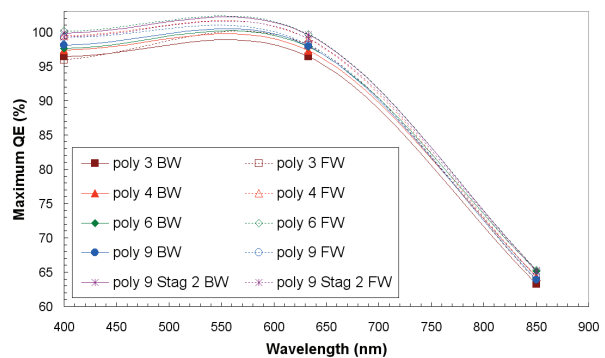


Figure 6. The effect of wavelength on sensitivity for the polywell PD and Polywell 9 StaG 2 layer photodiode.

E. Comparing response of polywell photodiodes with other geometries, at 633 nm.

Comparing the polywell and polywell-StaG hybrid with previously simulated photodiodes [15] having the same array dimensions, light and bias conditions is noteworthy. For crosstalk and sensitivity, the hybrid is a better performer at 633 nm than the polywell alone. For crosstalk, both are low in ranking as the geometries are designed to be operated optimally at shorter wavelengths, especially for front illumination. The polywell and polywell-StaG hybrids are able to operate effectively at other wavelengths, just as there are other photodiode geometries that have broadband sensitivity. They include variations on the PIN photodiode geometry [22] – [24].

This research has demonstrated the benefit of the StaG architecture to reducing crosstalk for the polywell photodiode geometry by giving more control of carrier transport to each pixel. Further

research will investigate the affect of additional StaG layers on the polywell-StaG hybrid, with different doping and biasing regimes.

V. CONCLUSIONS

Our research has shown that there is improvement in polywell photodiode crosstalk and sensitivity at 400 nm for the StaG-polywell hybrid over the generic polywell architecture. Though rise and fall times were not obtainable, it is clear that there is a close relationship between crosstalk and pixel rise and fall times, as they both relate to the way a pixel manages its efficient capture of all photocarriers generated in its volume.

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