Analogue-to-digital conversion and image enhancement using neuron-mos technology

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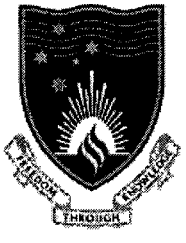
ANALOGUE-TO-DIGITAL CONVERSION AND IMAGE ENHANCEMENT USING NEURON-MOS TECHNOLOGY

A thesis submitted as the requirement
for the award of
Master of Engineering Science

Joseph William Austin-Crowe



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SCHOOL OF MATHEMATICS AND ENGINEERING

Abstract

This thesis describes the development of two novel circuits that use a newly developed technology, that of neuron-MOS, for the purposes of analogue-to-digital conversion and image enhancement. Neuron-MOS has the potential to redcue both the complexity and number of transistors required for analogue and digital circuits. A reduced area, low transistor-count analogue-to-digital converter that is suitable for inclusion in a massively parallel array of identical image processing elements is developed. Supporting the function of the array some fundamental image enhancement operations, such as edge enhancement, are examined exploiting the unique features of neuron-MOS technology.

DECLARATION

I certify that this thesis does not, to the best of my knowledge and belief:

(i) incorporate without acknowledgement any material previously submitted for a degree or diploma in any institution of higher education;

(ii) contain any material previously published or written by another person except where due reference is made in the text; or

(iii) contain any defamatory material.

Signature..

Date..25 January 2000

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GLOSSARY OF TERMS AND ABBREVIATIONS

A/D converter	Analogue-to-Digital converter.
ADC	Analogue-to-Digital Converter.
CMOS	Complementary Metal-Oxide Semiconductor
D/A Converter	Digital-to-Analogue Converter.
FET	Field Effect Transistor
FGPD	Floating Gate Potential Diagram. Graphical representation of the potential of the floating gate relative to ground, in νmos circuits.
JFET	Junction Field Effect Transistor
LSB	Least Significant Bit.
MSB	Most Significant Bit.
neu-MOS	see neuron-MOS
neuron-MOS	A method of providing a floating gate to a transistor that causes it to behave in much the same way as a biological neuron.
Pixel	Picture Element. The smallest part of an image that has been decimated spatially.
Smart Pixel	A hardware element, which is designed to process information locally as part of a focal plane array.
VLSI	Very Large Scale Integration
νmos	see neuron-MOS

ACKNOWLEDGEMENTS

The conduct of any research is often dependent upon the assistance of many individuals. This project is no exception.

My principal supervisor, Professor Kamran Eshraghian, must be the first to be thanked for his tirelessness and never-ending enthusiasm, which he imparts to those fortunate enough to be guided by his vision. Kamran has 'pulled the rabbit out of the hat' on many occasions as the leader of the Centre for Very High Speed Microelectronics at Edith Cowan University in Joondalup. Apart from establishing the Centre, he has provided valuable ideas, infrastructure and financial support to this and many other projects.

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My other student colleagues and friends must also be thanked for their support and encouragement, these are (in no particular order): Vis Ramakonar, Geoffrey Alagoda, Edward Gluszak and Alex Rassau who have all been 'in the thick of things' for a large part of this project.

To my family Philip, Marion, Guy and Cathy, go my thanks for being there. Most importantly, thanks go to my wife, Lynette, for putting up with me during the whole thing.

Chapter 1

Introduction

The design of electronic circuits often seeks to exploit any of a wide range of components, techniques and technologies. New technologies are of particular interest to the research engineer. Any new technology will be assessed as having more or less relevance to certain types of applications or being more or less suited to being within the bounds of a number of constraints for a given problem.

Typical constraints that are imposed include power consumption, speed of operation, energy efficiency, area utilisation and cost effectiveness. The nature of the problem may obviate one parameter as being of overriding importance, or at least holding considerable weight.

To a large extent the field of electronic engineering has been divided into either analogue or digital. A new enabling technology, termed Neuron-MOS, seeks to combine the two aspects into one functional unit, the neuron-MOS transistor. This circuit element promises to add new functionality to certain circuit configurations by virtue of its operation [1].

This thesis gives details of research that seeks to exploit neuron-MOS technology. neuron-MOS can achieve a reduction, for example, in the number of transistors used in the operation of analogue-to-digital conversion [1]. Such a reduction is a fundamental method of minimising power consumption. Another method for minimising power consumption to reduce the supply voltage to the circuit. Minimising the amount of switching activity to reduce dynamic power consumption is a third method [2, p8].

The process of analogue-to-digital conversion is a well-established field. Advances are being made in size, power consumption, speed and resolution. The research concentrates on developing a reduced-area analogue-to-digital converter using neuron-MOS technology. Reducing the power consumption of an element is one method to reducing the power consumed by an array of identical circuit elements.

This analogue-to-digital converter is intended to be included in an array of image processing elements [3]. The principle constraints in the design of an analogue-to-digital converter are the speed, the circuit area and the power consumption. The speed is not a primary priority in our design because we intend to use an in-pixel A/D converter. The speed is therefore compensated for the high level of parallelism. In this situation the silicon area of the A/D is the first concern since a higher fill-factor is obtained if the design of a high density A/D converter is achieved.

Also related to the application of the processing of an image is the enhancement of the human perception of that image, with the aim of improvement of the image quality. Image enhancement operations, such as contrast enhancement and edge detection, may also benefit from some of the unique features of neuron-MOS. The potential simplicity of using neuron-MOS in a locally connected array for fundamental operations is attractive.

The subjectivity of image reproduction has led to a large amount of research into image enhancement. The algorithmic improvement of a picture relies principally on the lack of human intervention in conducting the operation. The need for

enhancement comes about from a number of factors, such as the loss of image quality from the initial capture, the reduction in resolution or addition of noise in transmission, and the method of reproduction of the image, for example using cathode ray tube or liquid crystal display.

Increasing the discernment of the edges of the objects in the image is one method that may be used to improve the human perception of an image. Adjusting the contrast is another method that can be used to increase the perceivable detail.

Thus, the research is divided into two areas that support one another in that they aim to investigate the application of neuron-MOS technology using novel circuits for well-established applications. The first is the analogue-to-digital converter with its reduced area and power consumption. The second is using neuron-MOS to perform the fundamental image enhancement operation of edge enhancement/detection.

This chapter introduces the concept of the Smart Pixel and shows the necessity for the research into an area efficient analogue-to-digital converter. The main driving aim of this research was to develop an analogue-to-digital converter that is suitable for such an array.

Chapter 2 describes neuron-MOS technology, its applications, limitations and its methods of design. This chapter summarises the state of the art in neuron-MOS and details the available literature on the topic.

Chapter 3 describes fundamentals of analogue-to-digital conversion, performance parameters and the current state-of-the-art for each of the main methods of conversion. Because the field of A/D conversion is a vast one, and the thrust of the research is focussed on the application of νMOS, the chapter deals with the latest literature in the field, along with well-established practice. The chapter provides a basis for the understanding of A/D conversion and the issues associated with it.

Chapter 4 gives details of a proposed method of analogue-to-digital conversion using neuron-MOS technology. This is the presentation of the novelty in the research. A number of improvements of current designs are apparent, the suitability of practical circuit implementations are examined in this context.

Chapter 4 also discusses the implementation of the circuit in VLSI. The circuit layouts of a number of simple neuron-MOS circuits and the improved A/D converter are presented. Issues concerning the extraction of the capacitances, which are critical to the operation of neuron-MOS, are discussed.

The simulation results of the extracted SPICE file from the VLSI layout are also presented in Chapter 4. This chapter confirms the operation of the device to a resolution of 6 bits. The factors and limitations of the scheme are detailed.

Chapter 5 covers edge enhancement in images and proposes and examines a novel circuit, which uses neuron-MOS technology to achieve this in a simple, voltage-mode format. Allied with the A/D converter the image enhancement circuit is related in the research in two ways; the first is the relevance to the Smart Pixel device, which uses human perception of an image to convey meaning because edge enhancement increases the human perception of an image; the second is the nature of the circuit, which also uses νMOS to achieve its functionality.

Chapter 6 summarises the outcomes of the research conducted. Future work, which may be used to further develop the research presented in this thesis is recommended.

1.1 INTRODUCTION TO THE SMART PIXEL PARADIGM

With the increasing popularity of mobile communications contemporary research aims at providing more features to the user. For market acceptance size, weight and features have great importance. As yet a personal mobile videophone has not been developed. This application demands more efficient use of circuit area, lower power technology and the design of circuit elements that have not previously been necessary. Smart Pixel Multimedia Technology challenges present-day technology by providing image capture compression and display on a per-pixel basis [4].

Transmission of video information is bandwidth-intensive. Techniques, such as the wavelet transform, aim to reduce the amount of information while attempting to preserve image quality. The operation works by processing the image as an array, so that the Smart Pixel architecture may exploit this physical connectivity and organisation. Figure 1 shows the functional elements of the operation, which includes motion compensation, image transformation, and coding.

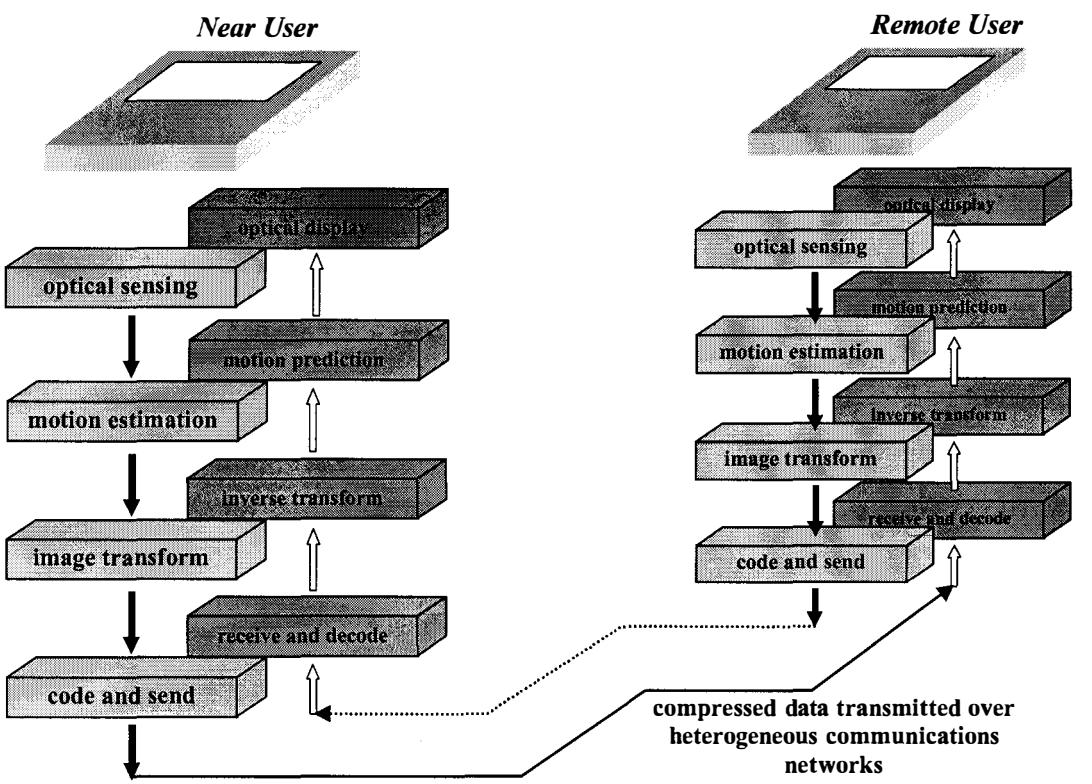


FIGURE 1 FUNCTIONAL ELEMENTS OF THE MOBILE MULTIMEDIA COMMUNICATOR

The Smart Pixel paradigm intends to provide a method of image capture and display using aspects of the same circuitry to perform both functions in a large, locally connected array.

1.2 SMART PIXEL ELEMENT

Figure 2 shows the architecture of a smart pixel that, when configured in an array, is capable of performing the forward and inverse 2D wavelet transform. Because the wavelet transform and its inverse are symmetrical operations each pixel is capable of both image capture and display with very little extra processing circuitry [5].

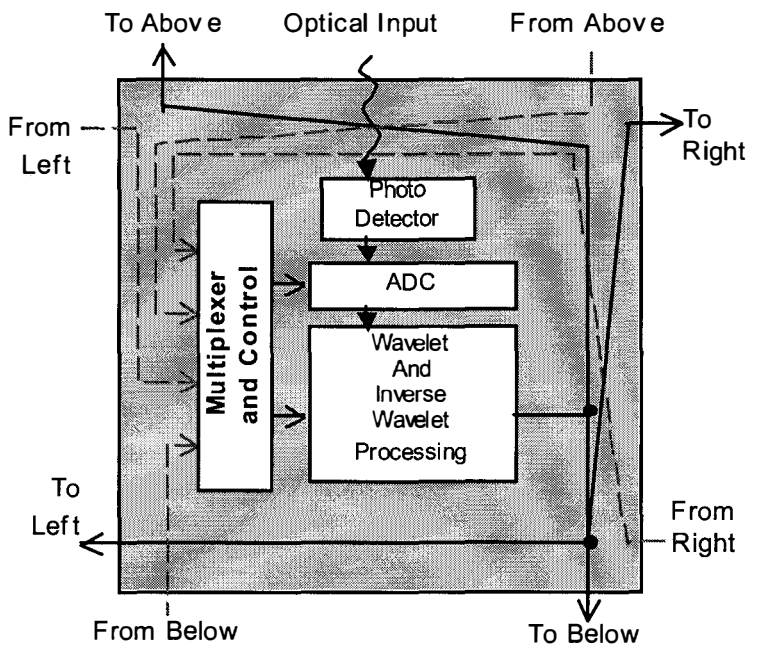


FIGURE 2 SCHEMATIC OF SMART PIXEL ARCHITECTURE

Light is to be converted into electrical energy using a photodetector. The transform processing expects the image data to be in digital form, whereas the light transduced by the photodetector is in an analogue form. Thus, an analogue to digital converter (A/D) would be a significant component of the architecture, as one A/D is provided per pixel. Some basic analogue processing may also be performed to enhance the edges of the image, increasing image quality.

1.3 LIQUID CRYSTAL OVER SILICON

In order to have the capture and display elements coexist on the same substrate the Smart Pixel uses liquid crystal over silicon (LCOS). Liquid crystal (LC) displays use alignment of crystals to block or transmit polarised light. Usually a mirror is provided to increase the amount of light that is reflected back to the observer. Typically LC displays consume little power and have simple driving circuitry. These features make them suitable for the Smart Pixel.

It is proposed that the Metal-3 layer will be used to form the mirror over the circuitry see Figure 3. The mirror will not be able to obscure the photodetector. Increasing the ratio of mirror area to photodetector area increases the contrast ratio.

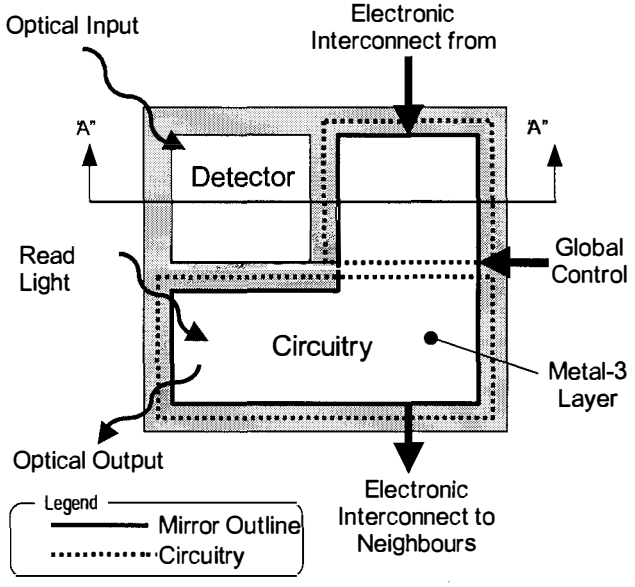


FIGURE 3 SCHEMATIC OF SMART PIXEL LAYOUT

COS is comprised of the mirror and associated driving circuitry bathed in non-luctive LC material. Posts are to be used to separate this liquid from a sheet of hat has a conductive ITO (Indium Tin Oxide) coating (Figure 4).

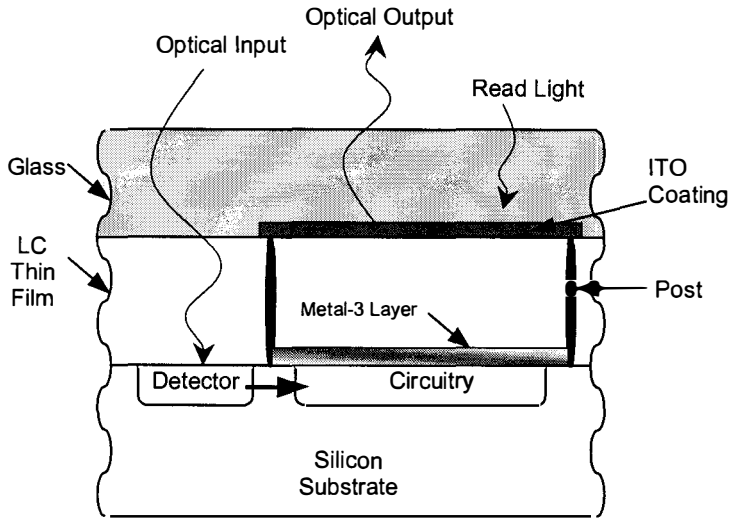


FIGURE 4 CROSS-SECTION OF LCOS TECHNOLOGY

The LCOS circuit is then completed by the addition of the low-current driver circuitry that can supply a digital signal to form the image by the modulation of the relevant metal areas that, collectively, will form a grey-scale image.

1.4 IMAGE DISPLAY AND CAPTURE LENS

Because the image capture and display operations are physically interleaved a lens for image capture and display share the same optical path a novel lens structure will need to be developed. As shown in Figure 5 the integrated lens structure based on concentric compound lenses is comprised of a central region which is the display lens *(a)* while the peripheral ring forms the detector lens *(b)*.

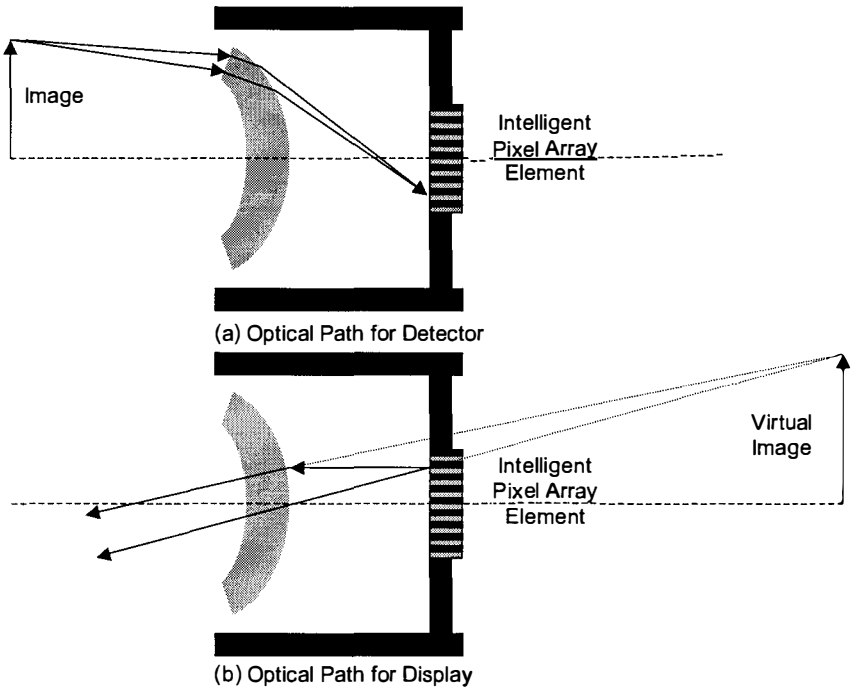


FIGURE 5 NOVEL INTEGRATED LENS STRUCTURE

1.5 AREAS OF RESEARCH

The research presented here concentrates on firstly enhancing the perception of edges using analogue pre-processing in a locally connected configuration and secondly providing the function of analogue-to-digital conversion which is performed on the edge-enhanced intensity quantity. Figure 6 shows the placement of these components in the smart pixel.

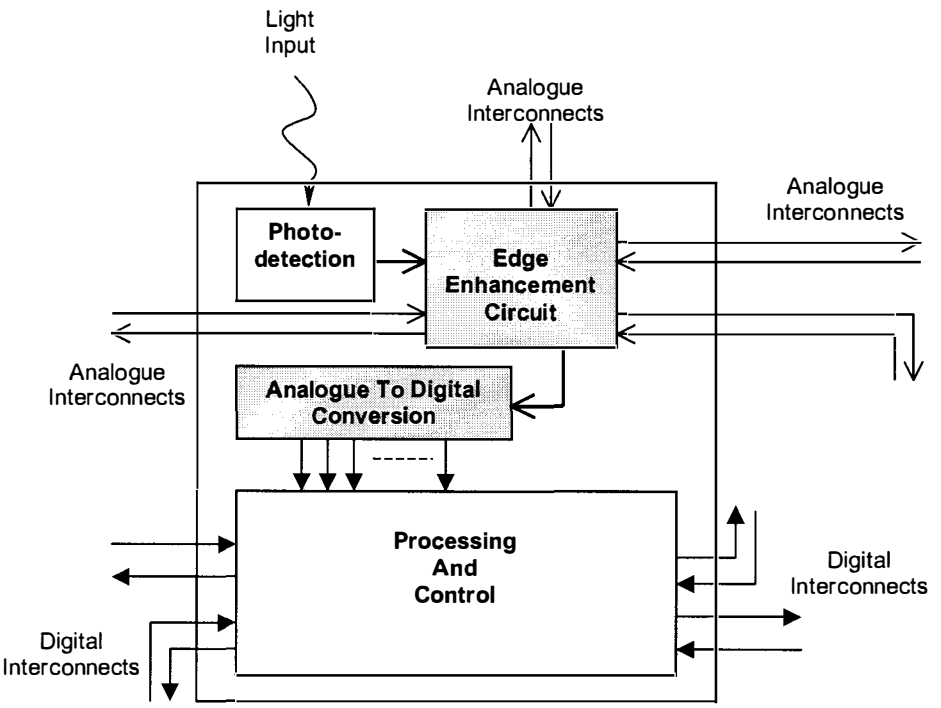


FIGURE 6 SCHEMATIC OF SMART PIXEL SHOWING AREAS OF RESEARCH COVERED

1.6 CONCLUSIONS

This section gave an overview of the Smart Pixel and the Mobile Multimedia Communicator. Areas of interest to researchers were discussed, with two subcircuits of the Smart Pixel being identified for the research contained in this thesis.

Whilst the operations of edge enhancement and analogue-to-digital conversion are dissimilar, the application dictates that they share common constraints. The use of neuron-MOS technology goes some way toward addressing a number of issues such as compactness and the ability to operate without complex control.

Chapter 2

neuron-MOS Technology

2.1 INTRODUCTION

Enhancing the functionality of integrated circuits has primarily been due to the reduction of the minimum feature size and the maximum manufacturable chip area. There are limitations on the reduction of scale of the available technologies, where integrated circuit designers are at the mercy of the foundries upon which they rely. An increase in the capabilities of the components of which circuits are comprised affords an increase in effective functionality per unit area.

Classically, integrated circuit design is composed of either analogue or digital components. Enhanced functionality may be gained from a device that has the characteristics of both. Such a component, that is described as behaving more intelligently than a mere switching device, is the Neuron-MOS (Neu-MOS or νMOS)

transistor described by Shibata and Ohmi [1]. The name is brought about because of its similarity in behaviour to a biological neuron.

The νMOS transistor may be implemented using conventional discrete components using n- and p-type MOSFETs and capacitors. Although simulation results generally agree with those obtained using discrete components (ie. 'breadboarding'), there are severe limitations in using such a technique to replicate the operation of a VLSI circuit. These include the inability to determine the necessary transistor length-to-width ratios for threshold-critical operations and the effect of input floating-gate capacitances on slew rate of the circuit.

Utilisation of a technology such as νMOS may enable a compact implementation of circuit elements such as analogue-to-digital converters [3] and those using analogue neural processing, lateral inhibition for example.

This section gives a survey of the current state-of-the-art in νMOS technology, according to available literature. Complete design methodologies for full-custom VLSI design and layout of νMOS circuits are not readily accessible, this is due to the relatively recent introduction of νMOS and the small number of research groups devoted to its application.

2.2 TECHNOLOGY DESCRIPTION

νMOS technology gives a flexible configuration for an inverter that allows operation dependent on the status of a set of inputs, each of arbitrary weighting. The configuration is similar to a standard CMOS inverter, but extends the gate region, to which a capacitively coupled set of inputs is applied. Each input gate is of an area, and hence capacitance, proportional to its weighting. Figure 7 shows this schematically [1].

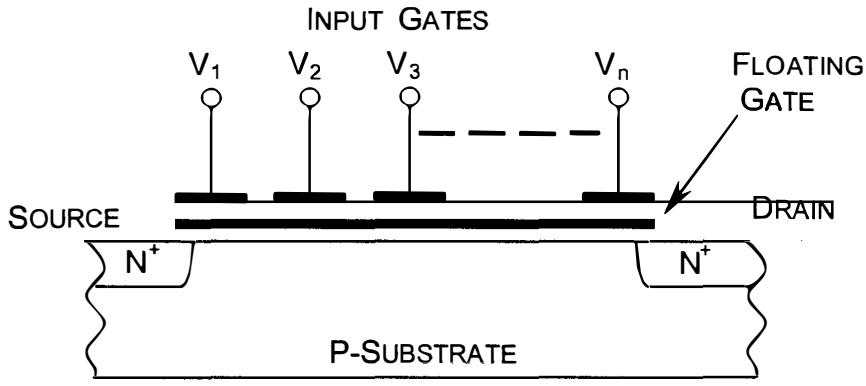


FIGURE 7 SYMBOLIC REPRESENTATION OF VMOS TRANSISTOR

Because the operation is using a voltage mode summation, power dissipation is minimal. This is in contrast to a current-mode (wired) summation [1].

The charge on the floating gate, Q_F, is dependent on the charge stored between the input gates and the floating gate [6]

$$Q_F = Q_0 + \sum_{i=1}^{n}(-Q_i) = \sum_{i=0}^{n} C_i(\phi_F - V_i) = \phi_F \sum_{i=0}^{n} C_i - \sum_{i=0}^{n} C_i V_i \tag{1}$$

where C_i is the capacitance of the i^{th} gate and V_i is the voltage applied to the i^{th} gate. Q_i is the charge on the i^{th} floating gate, Q_0 is the charge stored by the capacitance, C_0, due to the capacitive coupling between the floating gate and the substrate. The total capacitance includes this value

$$C_{TOT} = \sum_{i=0}^{n} C_i \tag{2}$$

The inverter changes state once the weighted sum of the inputs, the floating gate potential, ϕ_F exceeds a threshold value, V_{TH} [1]

$$\phi_F = \frac{C_1 V_1 + C_2 V_2 + \ldots + C_n V_n}{C_{TOT}} \tag{3}$$

If ϕ_F exceeds the threshold voltage V_{TH} then the transistor is turned on. Typically V_{TH} is equal to $V_{DD}/2$. Note that this is the weighted sum, as the capacitances of each gate may be varied. γ is the floating-gate gain [6]

$$\gamma = \frac{C_1 + C_2 + \ldots + C_N}{C_{TOT}} \tag{4}$$

The standard design parameter is to have the principle gate as half of the total capacitance [7]

$$C_1 = \frac{\gamma C_{TOT}}{2} \tag{5}$$

2.3 νMOS INVERTER

This section describes the use of the νMOS technology to achieve an inverter that will provide a digital voltage output for a computation performed on the weighted-set of voltage inputs.

The layout of the neuron-MOS inverter is shown in Figure 8.

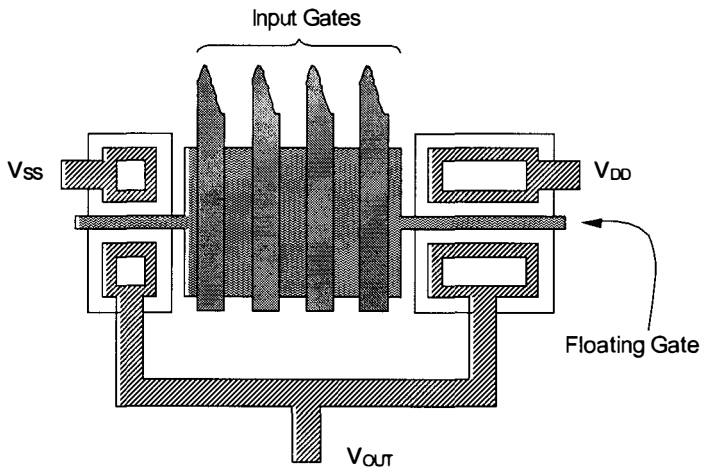


FIGURE 8 TYPICAL LAYOUT OF NEURON-MOS INVERTER

The symbolic representation is shown in Figure 9 below.

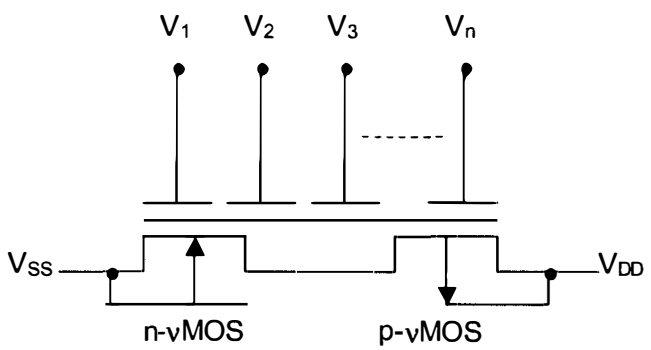


FIGURE 9 SYMBOLIC REPRESENTATION OF NEURON-MOS CONFIGURATION

The analysis begins with the fundamental operation of the device, where the output is determined by the weighted sum of the inputs, compared to the switching threshold. The inverter switching threshold is given by

$$V_{INV}^{*} = \frac{V_{DD} + \sqrt{\beta_R} \cdot V_{T_n}^{*} + V_{T_p}^{*}}{\sqrt{\beta_R} + 1} \tag{6}$$

where V^{*}_{Tn} and V^{*}_{Tp} are the n- and p-channel threshold voltages, β_R is the beta ratio

$$\beta_R \equiv \frac{\beta_n}{\beta_p} = \frac{(W/L)_n \mu_n}{(W/L)_p \mu_p} \tag{7}$$

the *n* and *p* subscripts denoting the n- and p-channels, μ_n and μ_p being the electron and hole surface mobilities. For a value of β_R equal to unity, equation (6) becomes

$$V_{INV}^* = \frac{1}{2} V_{DD} + \frac{V_{T_n}^* + V_{T_p}^*}{2} \tag{8}$$

considering the substrate potential, which is not zero for the p-νMOS transistor due to the n-well being connected to V_{DD}, ϕ_F is modified to

$$\phi_F = \frac{\sum_{i=1}^{n} C_i V_i + C_{0p} V_{DD}}{C_{TOT}} \tag{9}$$

with C_{0p}, the substrate capacitance of a p-νMOS transistor, being approximated by the gate oxide capacitance when the p-νMOS is on, giving the revised relation

$$\frac{C_1 V_1 + C_2 V_2 + \cdots + C_n V_n}{C_{TOT}} > V_{INV}^* - \frac{C_{0p}}{C_{TOT}} \cdot V_{DD} \tag{10}$$

The threshold of the inverter, as seen from gate 1 of the νMOS transistor is

$$V_{INV}^{(1)} = \frac{C_{TOT}}{C_1} \cdot \left(V_{INV}^* - \frac{C_{0p}}{C_{TOT}} \cdot V_{DD} \right) - \frac{C_2}{C_1} \cdot V_2 - \frac{C_3}{C_1} \cdot V_3 - \cdots - \frac{C_n}{C_1} \cdot V_n \tag{11}$$

Taking V_{INV}^* as

$$V_{INV}^* - \frac{C_{0p}}{C_{TOT}} \cdot V_{DD} = \frac{1}{2} \gamma V_{DD} \tag{12}$$

reduces (11) to $V^*_{INV} = V_{DD}-V_2$.

For example, for the three-input circuit in Figure 10, the switching threshold is

$$V^{(1)}_{INV} = V_{DD} - \frac{1}{3}(2 \cdot V_a + V_b) \tag{13}$$

showing how $V^{(1)}_{INV}$ can change due to the states of the control signals V_a and V_b. This technique is used to achieve the Soft-Hardware Logic Circuit as described by Shibata and Ohmi in [6], analysed later in this thesis.

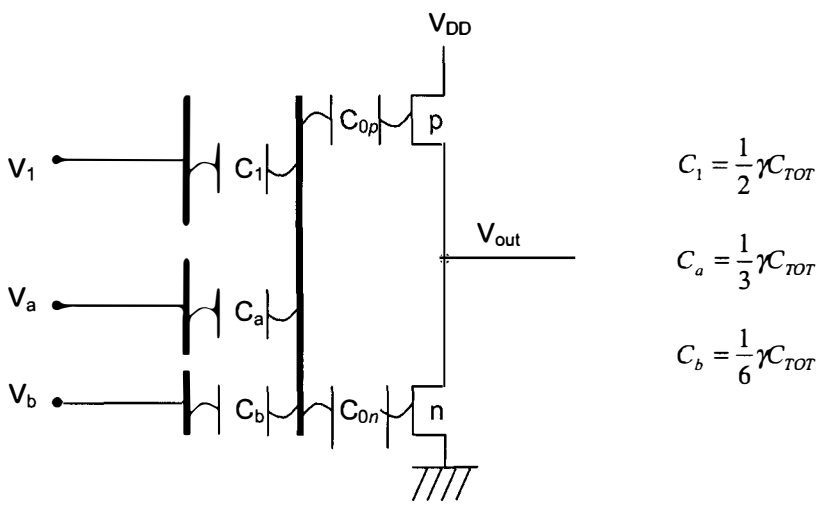
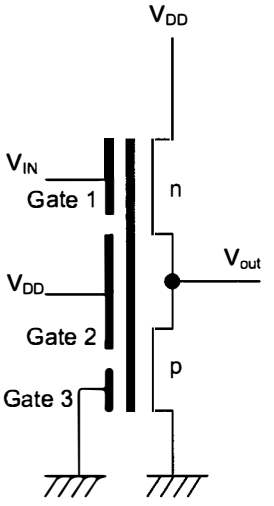


FIGURE 10 CAPACITANCES PRESENT IN NEU-MOS CIRCUIT

2.4 VARIABLE THRESHOLD INVERTER

The problem of creating inverters with a number of different threshold voltages in the same design is either the requirement of varying the doping levels of channel regions, which complicates the manufacturing process, or by providing a resistive voltage divider, which consumes power constantly. Another method involves changing β_R, but the range of switching voltages available using this method is limited. Indeed, modification of β_R is invaluable in being able to make fine adjustment of the switching threshold. Instead a variable threshold νMOS transistor can be configured by adjusting the capacitance sizes of the gates. Figure 11 shows a

diagram of a variable threshold inverter, which has three input gates, the first is connected to the input, the second is connected to the supply rail and the third is connected to ground. Alternatively, the same effect may be gained by combining the latter two gates into a single gate and attaching to a voltage in the range of [0,V_{DD}] volts. In this case the computation of the voltage and gate size is different. Connecting two gates to either of the supply rails addresses the difficulty of supplying a variety of arbitrary voltages in a VLSI circuit.



$$C_2 + C_3 = \frac{1}{2}\gamma C_{TOT}$$

$$C_1 = \frac{1}{2}\gamma C_{TOT}$$

FIGURE 11 VARIABLE THRESHOLD INVERTER

The floating gate potential diagram in Figure 12 shows the potential of the floating gate, and is used as a design aid. The state of the inverter is determined by the relationship of the heavy line (floating gate potential) and the inverter threshold line (typically $V_{DD}/2$). The base line is when the principal gate voltage is varied from 0 to V_{DD} as the other gates are held at zero. If the gate potential is above the threshold line, then the inverter is considered to be in the 'on' state.

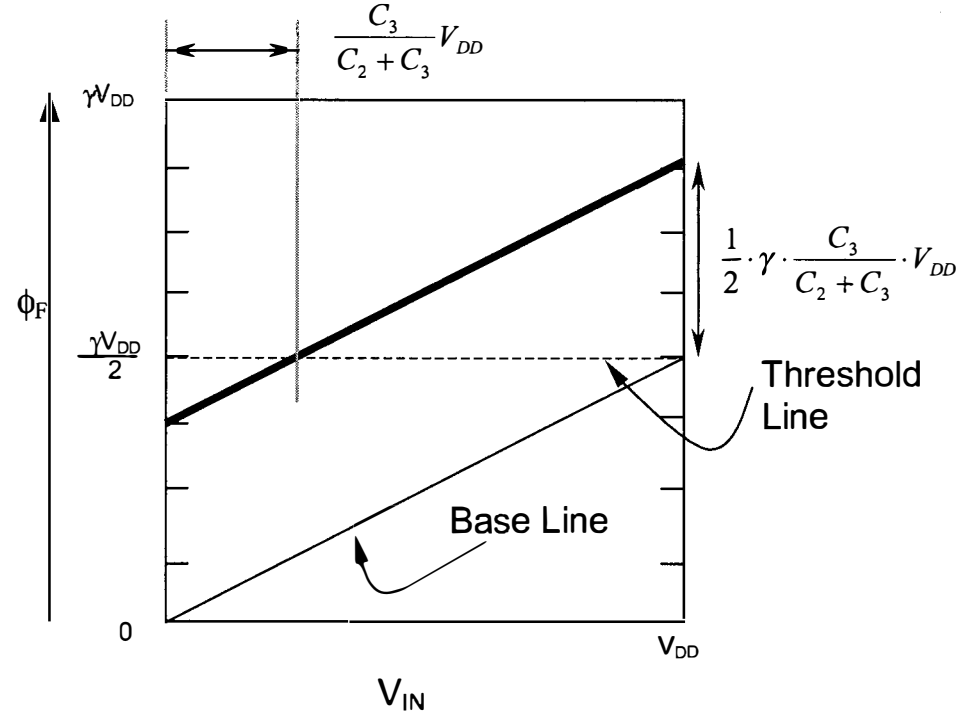


FIGURE 12 FLOATING GATE POTENTIAL DIAGRAM

Figure 12, above, shows how adjustments may be made to gates 1 and 2, again with the assumption that the capacitance of gate 1 is half of the total capacitance [7].

Because this method relies on the ratio of capacitor sizes, and VLSI fabrication defines minimum feature sizes, and hence a minimum capacitance, a large disparity in capacitor ratios will result in a capacitor occupying a large chip floor area.

By modifying the voltage applied to the second gate from a value other than V_{DD}, the threshold can also effectively be altered. Note that this will also change the output voltage swing, which may be a problem in using a series connection of these devices.

2.5 SIMULATION OF NEURON-MOS CIRCUITS

Neuron-MOS circuits are simulated by configuration of the circuits as n-MOS and p-MOS transistors, in series to ground from the supply rail with the output being derived from the centre of the pair. The gates of both transistors are connected. Standard SPICE capacitors are used for the floating gate capacitances, with one

(common) node connected to the transistor gates, the other being connected to the inputs of the νMOS subcircuit. A typical SPICE subcircuit is listed below for a two-input νMOS inverter:

```
.SUBCKT NM_2 IN1 IN2 OUT VDD VGND
+{P_L=2U P_W=4U N_L=4U N_W=4U GCAP1=1P GCAP2=2P}

M21    VDD VGATE OUT  VDD  P_TYPE W={P_W} L={P_L}
M22    OUT VGATE VGND VGND N_TYPE W={N_W} L={N_L}

C1     IN1 VGATE {GCAP1}
C2     IN2 VGATE {GCAP2}

RNM_2 VGATE VGND 1E12

.ENDS
```

By way of explanation, input capacitances for the above subcircuit are by default, 1pF for input gate 1, and 2pF for gate 2. These values are arbitrary, with the actual values chosen dependent upon the design used. The capacitance value is not scaled or modified from the values that are chosen using the basic design equations.

Transistor width-to-length ratios are set to common quantities for a CMOS inverter. Transistor models are those that are supplied by the manufacturer for a chosen technology.

Resistor `RNM_2` is provided to allow for DC convergence during the initial analysis, as it alleviated the need for manually configuring initial operating conditions when the DC analysis is disabled. Resistor `RNM_2` is set to a sufficiently high value as to bleed the charge from the input capacitances very slowly and thus not affect the simulation to any appreciable extent.

2.6 ANALOGUE CONFIGURATIONS

This section describes the configurations presented in the literature that use νMOS technology in the source-follower configuration. The output of the circuit is an analogue quantity and is hence termed 'analogue mode'.

2.6.1 Source-Follower Configuration

The output of the νMOS inverter is digital; however, by implementing a νMOS circuit using the source-follower configuration then the output may be over a range of values that are determined by the input gate voltages and their relative weightings.

Figure 13 shows the diagram of an ideal source-follower, which has high input resistance and unity gain.

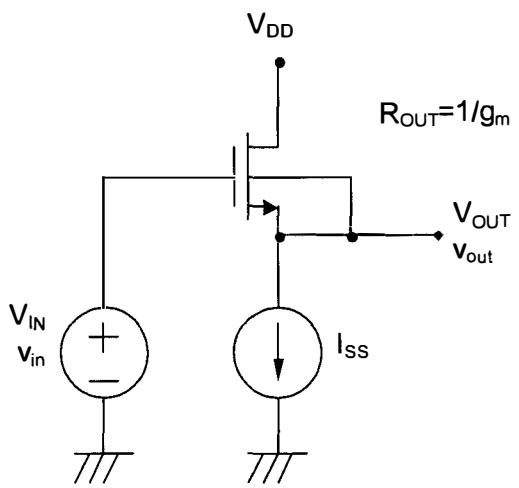


FIGURE 13 SOURCE FOLLOWER CONFIGURATION

This case uses a p-well n-type MOS transistor where the bulk is connected to the source, meaning that the body effect does not apply [8, p36]. The value of v_{OUT}, for both DC and AC is

$$v_{IN} - v_{OUT} = v_{GS} \tag{14}$$

For the case where the bulk is connected to ground the small signal voltage gain is not unity, but given by

$$A_v = \frac{\frac{1}{g_{mb}}}{\frac{1}{g_{mb}} + \frac{1}{g_m}} = \frac{1}{1 + \frac{g_{mb}}{g_m}} \tag{15}$$

where g_{mb} is the so-called bulk transconductance from the bulk-input node voltage, v_{bs}, to the output current i_{ds}, which is the transconductance of the parasitic JFET. The output resistance is

$$R_{OUT} = \frac{1}{g_m + g_{mb} + g_o} \tag{16}$$

where $g_o = 1/r_o$, which is negligible. An expression for g_{mb} is given in [8,p25]

$$g_m = 2 \cdot \frac{KP}{2n} \cdot \frac{W}{L}\left(V_{GSQ} - V_T\right) \tag{17}$$

The dependence on the width (W) to length (L) ratio is apparent. V_{GSQ} is the gate-source voltage at the quiescent operating point. V_T is the threshold voltage, KP is the transconductance parameter and n represents a quantity dependant on fast surface states.

For a MOS transistor driving a resistive load, the output to input is described by

$$\frac{v_{OUT}}{v_{IN}} = \frac{R_L}{R_L + R_{DS}} \tag{18}$$

where R_{DS} is primarily dependent on the width-to-length ratio, and a solution is best found using SPICE [8,p39]. The circuit in Figure 14 was simulated using SPICE.

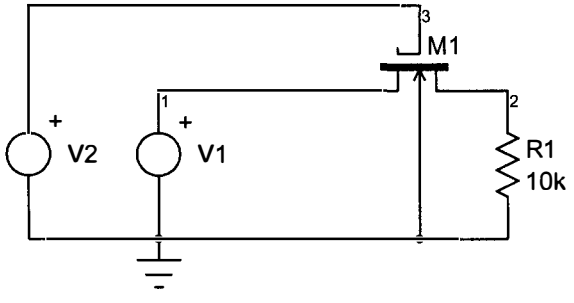


FIGURE 14 TEST CIRCUIT FOR VARYING W/L RATIO

Then a DC sweep was performed for varying W/L ratios using a minimum value of L as 10μm-

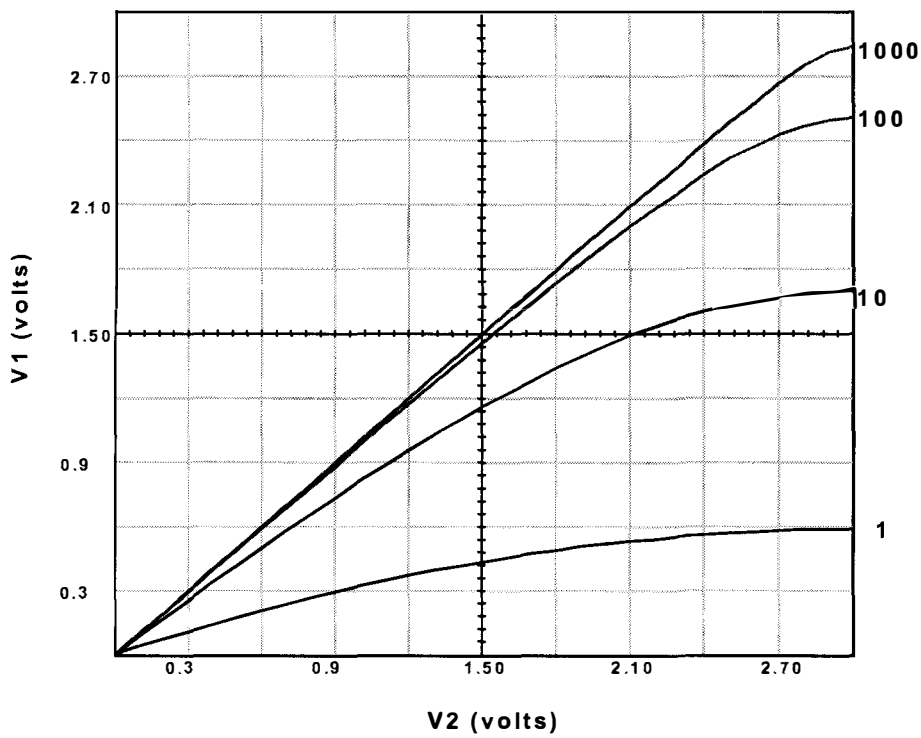


FIGURE 15 OUTPUT VOLTAGE FOR VARYING W/L RATIO

For VLSI implementation a particular production technology has a minimum feature size. This, in turn, imposes a minimum length for a MOS transistor. Thus large W/L ratios are impractical if conservation of area is a consideration. Generally the W/L ratio is expressed not as a scalar, but as the actual multiples of the minimum feature size available for the chosen technology. An example is 4:2 or 4:4, quoted for the nMOS and pMOS transistors respectively in a CMOS inverter pair. The mobility of the substrate being the main factor in the ratio decision.

Although the size of vMOS gates can become a major factor in the overall size of an vMOS circuit, the issues of accommodating the transistors in as small a region as possible is good design technique. This allows for more flexibility in the routing of signal lines and gate geometry.

2.6.2 νMOS Source-Follower Configuration

The analysis of the technology is developed further, now using an n-type νMOS transistor with *n* floating gates, as shown in Figure 16. A resistor that is much larger than the on-resistance of the transistor is used as a load in series to ground.

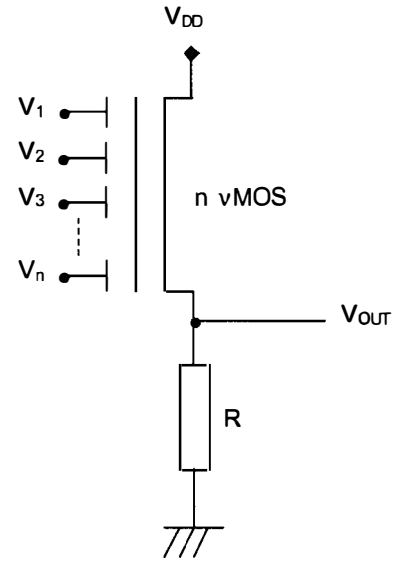


FIGURE 16 NEURON-MOS SOURCE-FOLLOWER CONFIGURATION

The output voltage is then described by the relation

$$V_{OUT} = \phi_F - V_{TH}^{*} \tag{19}$$

Setting the threshold voltage to zero reduces to make V_{OUT} to equal to ϕ_F. The DC power dissipated is still described by the simple factor of V_{OUT}^2/R, however reduction in R degrades the gain and hence the noise margin of this configuration.

If the inputs are digital, described as their status by the variable X_n, and the binary quantities are $X_n \in \{0,1\}$, then the device may be used to implement a D/A converter simply if the capacitances are related by $C_{i+1} = 2 \cdot C_i$. The output of an *n* input circuit may then be described by

$$V_{OUT} = \frac{\gamma \cdot V_{DD}}{2^n - 1}\left(X_1 + 2 \cdot X_2 + \cdots + 2^{n-1} \cdot X_n\right) \tag{20}$$

the quantity γ being the floating-gate gain factor as described by equation (4).

To address the issue of the static power dissipation due to R, a complementary structure can be used. Instead of the resistance R, a p-type MOS transistor is used as an active load (Figure 17).

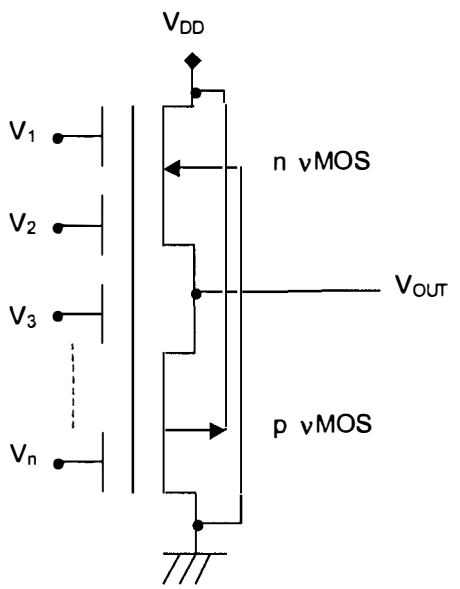


FIGURE 17 USING P-TYPE MOS TRANSISTOR AS ACTIVE LOAD

Speed of operation, stability and noise margins are increased by the circuit conducting DC current [6]. The trade-off between performance and static power dissipation must be addressed if an array of such devices is to be constructed, or power is a major consideration.

To illustrate the operation of the vMOS source-follower configuration, the circuit in Figure 17 was simulated using SPICE. The power supply value of 3V was chosen, however the operation is similar for a 5V supply. Transistor width-to-length ratios similar to those that are used in many VLSI implementations are used. A number of devices and transistor width-to-length ratios were simulated, all yielding very similar results. The parameters chosen in the design of such a circuit are chosen with concern for the expected current and space available to a particular application.

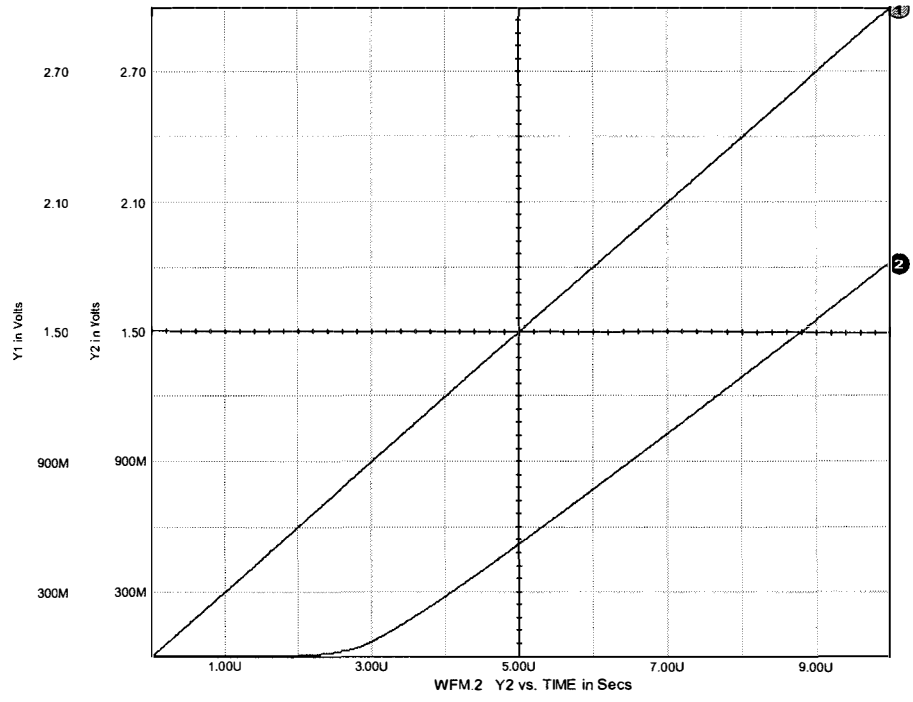


FIGURE 18 INPUT/OUTPUT CHARACTERISTIC IN SOURCE-FOLLOWER CONFIGURATION

In Figure 18 a ramp function (trace 1) was input to a single-gate νMOS device, the output is shown as trace 2. The voltage drop across the source-follower shows a fundamental difficulty in using the νMOS device in the source-follower mode. A slightly different interpretation may be made, however, when using the inputs digitally.

A SPICE simulation was conducted using the scheme in Figure 17 for a 4-bit D/A converter. The gate sizes were (2,1,0.5,0.25)pF, with digital inputs (V_i=V_{DD}=3V). The results are shown in Figure 19.

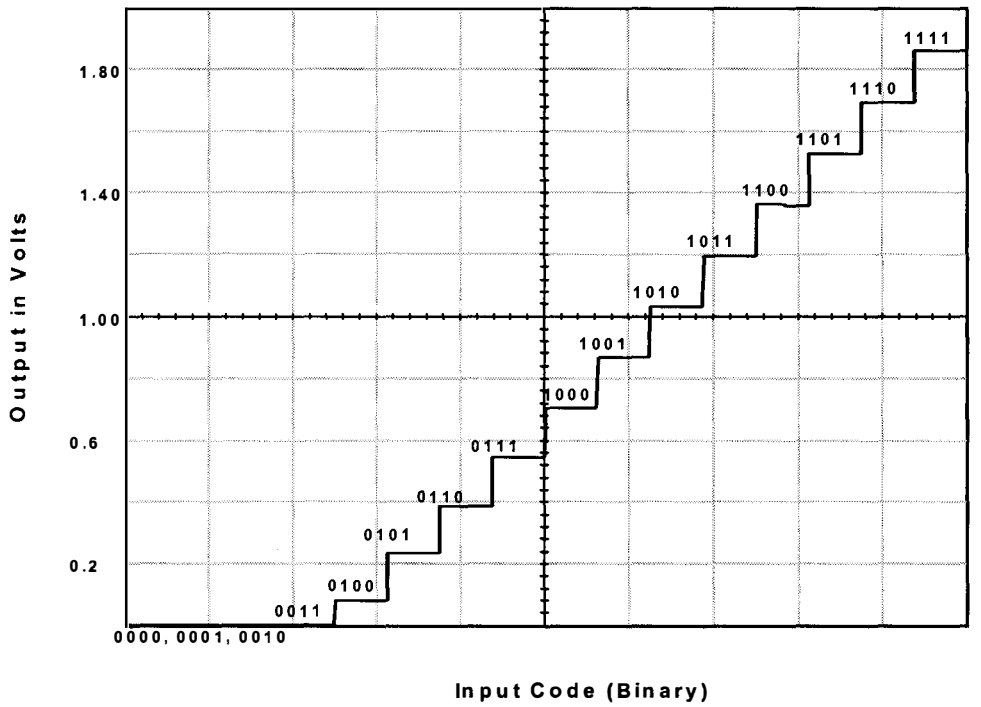


FIGURE 19 OUTPUT OF D/A CONVERTER

It can be seen that the output for several of the input codes remains at zero, thus the circuitry dependent on the output of the source-follower may need to account for this. The limitation is primarily on the output range, which is not full scale. Connection to further νMOS circuits need as large an input sweep as possible to reduce the effects of noise and to allow a large input voltage swing to maximise switching efficiency.

2.6.3 Schmitt Trigger

To illustrate the large variety and flexibility of νMOS circuits a bistable circuit may also be configured. The Schmitt trigger is a circuit which exhibits hysteresis. Classically this may be configured using an op-amp, with positive feedback as shown in Figure 20 [9, p864ff].

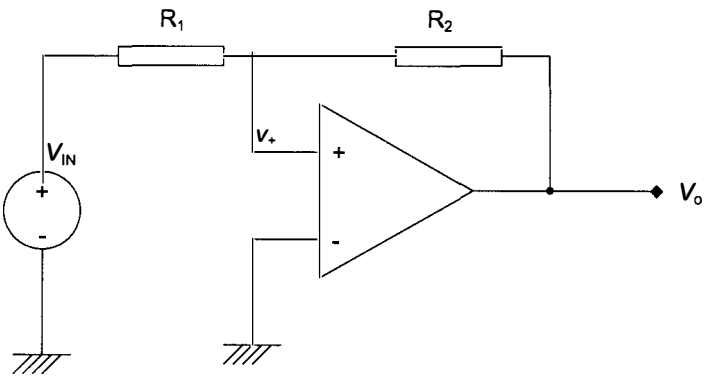


FIGURE 20 BISTABLE CIRCUIT

The transfer characteristic is shown in Figure 21.

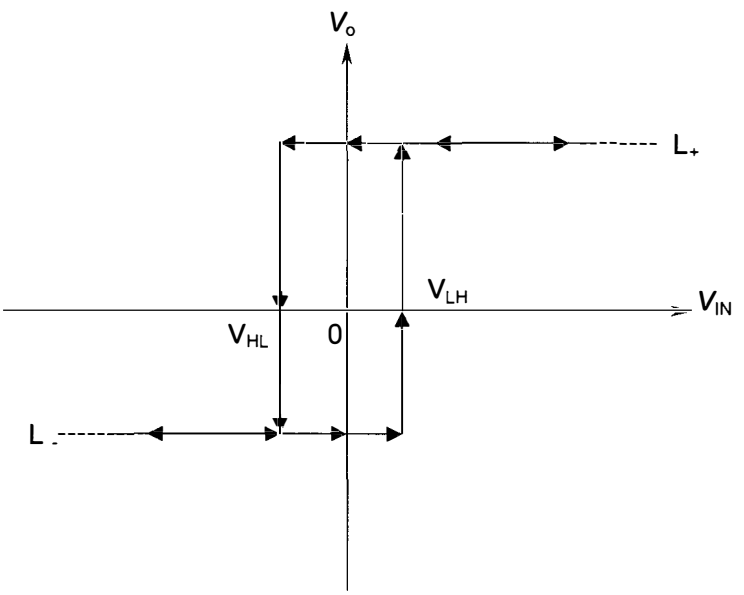


FIGURE 21 SCHMITT TRIGGER TRANSFER CHARACTERISTIC.

The transfer characteristic is obtained by using superposition of the linear circuit formed by R_1 and R_2, the voltage v_+ is expressed as follows

$$v_+ = V_{in} \cdot \frac{R_2}{R_1 + R_2} + V_o \cdot \frac{R_1}{R_1 + R_2} \tag{21}$$

When the circuit is in the positive stable state where $V_o = L_+$, the cases where V_{in} is positive cause no change in output. If V_{in} is made sufficiently negative, that is, makes v_+ less than zero, the circuit will trigger. The low voltage

threshold is thus found by substituting in (21) for V_o to be L_+, v_+ to be zero and V_{in} to be the threshold voltage itself, V_{HL}, giving

$$V_{HL} = -L_+ \cdot \frac{R_1}{R_2} \tag{22}$$

The same is true when in the lower threshold region, to find the upper threshold voltage the values substituted in (21) are V_o=L_-, v_+ to be zero and the voltage at which switching from low to high (V_{LH}) occurs to be V_{in}, yielding

$$V_{LH} = -L_- \cdot \frac{R_1}{R_2} \tag{23}$$

The circuit is termed 'non-inverting' because a positive trigger signal is needed to switch it to the positive stable state.

Figure 22 shows a Schmitt trigger that is configured using a νMOS inverter coupled to a standard CMOS inverter. This inverter is used to provide the correct logic to the input of the νMOS gate, and to improve the drive capability of the circuit [10]. This is analogous to the positive feedback representation shown in Figure 20.

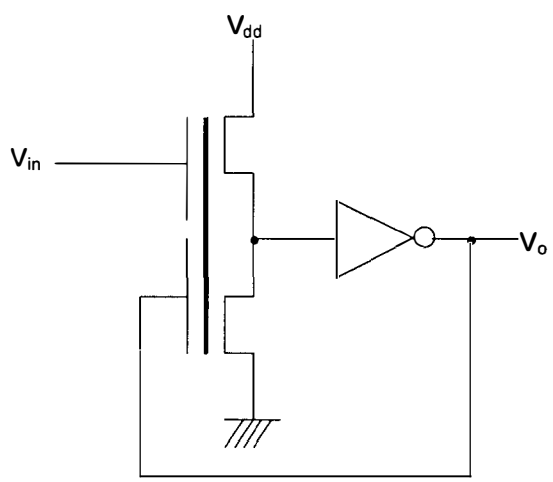


FIGURE 22 NEURON-MOS SCHMITT TRIGGER

The operation of this circuit is described by the relation

$$\frac{C_{in}}{C_{TOT}} \cdot V_{in} + \frac{C_0}{C_{TOT}} \cdot V_o \geq V_{TH}^* \tag{24}$$

With V_o being the inverter output voltage, V^*_{TH} being the νMOS inverter threshold, C_{TOT} being the sum of the capacitances of the input gate (C_{in}) and the feedback gate (C_o).

The high-to-low switching voltage, as described by (25), is determined by consideration of the initial state of the νMOS inverter. This is with the input held to ground, causing a high output. The standard inverter thus has a low output, giving all inputs to the νMOS inverter as ground.

$$V_{LH} = \frac{C_{TOT}}{C_{in}} \cdot V_{TH}^* \tag{25}$$

The high-to-low switching voltage is described by (26).

$$V_{HL} = \frac{C_{TOT}}{C_{in}} \cdot V_{TH}^* - \frac{C_0}{C_{in}} \cdot V_{dd} \tag{26}$$

Subtracting (26) from (25) gives the hysteresis width, (27).

$$V_{HW} = \frac{C_o}{C_{in}} \cdot V_{dd} \tag{27}$$

Simulation results presented in [10] confirm that the first order analysis is very close to those results gained from SPICE.

Comparison of circuit complexity to the operational amplifier presented as the initial example indicates that the implementation of such a circuit using νMOS technology is liable to yield reductions in both the VLSI layout circuit area and the number of transistors.

2.6.4 Controlled Gain Amplifier

Capacitor ratios may be used to control the gain of a νMOS amplifier, as discussed in [10]. Two methods may be employed, the first using one n-νMOS and one p-νMOS linear grounded resistor, this is shown in Figure 23.

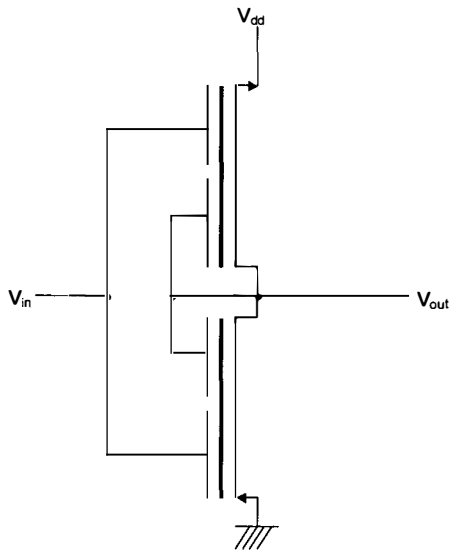


FIGURE 23 NEURON-MOS CONTROLLED-GAIN AMPLIFIER

After making a number of assumptions relating to switching thresholds the operation may be described by (28).

$$V_{out} = -\frac{C_{in}}{C_o} \cdot V_{in} \tag{28}$$

Another alternative method uses one νMOS inverter with a slightly different feedback configuration, this is shown in Figure 24.

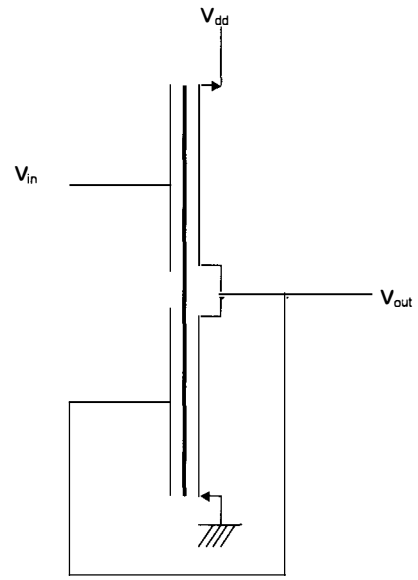


FIGURE 24 ALTERNATIVE NEURON-MOS CONTROLLED GAIN AMPLIFIER

A special case is where $C_{in} = C_o$, which is an inverting analogue buffer circuit. This has linearity that is independent of transistor parameters [10]. This circuit is used in the lateral inhibition circuit, which is described later in this thesis.

2.7 SEMI-ANALOGUE IMPLEMENTATION

This section gives examples of how some common digital functional elements may be implemented using νMOS. This section is part of the progression from using νMOS in a purely analogue mode, such as the source-follower configuration, into providing digital functions. The term semi-analogue is used to distinguish the operation of these circuits, which perform operations on analogue quantities *outside of the νMOS device*, yet yield a digital result from digital inputs.

2.7.1 Common Digital Functions

Digital functions may be simply implemented using the scheme shown in Figure 25. Inclusion or omission of the variable threshold inverter ('A'), is dependent on the presence of a discontinuity in the floating-gate potential diagram, explained later in this section.

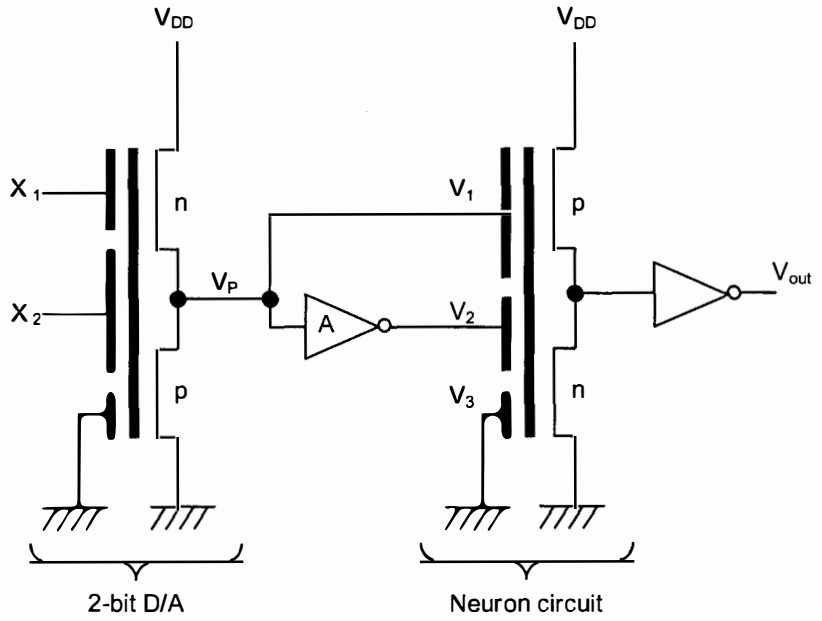


FIGURE 25 SEMI-ANALOGUE IMPLEMENTATION

Inputs X_1 and X_2 are attached to gates 1 and 2 of the D/A converter, which have capacitances of C_1 and C_2 respectively. $C_2 = 2 \cdot C_1$, thus ϕ_F is proportional to $X_1+2 \cdot X_2$. Adjusting the design parameters of the n and p channel νMOS transistors allows the output, V_P to be

$$V_P = \left(\frac{1}{4}X_1 + \frac{1}{2}X_2\right)V_{DD} + \frac{1}{8}V_{DD} \tag{29}$$

X_1 and X_2 are either 1 or 0. Evaluating all of the possibilities -

X_1	X_2	V_P
0	0	$1/8 \cdot V_{DD}$
1	0	$3/8 \cdot V_{DD}$
0	1	$5/8 \cdot V_{DD}$
1	1	$7/8 \cdot V_{DD}$

TABLE 1 THRESHOLD QUANTITIES FOR SEMI-ANALOGUE IMPLEMENTATION

A floating-gate potential diagram may be used to visualise the behaviour of such circuits. Figure 26 shows an example of a floating-gate potential diagram for an exclusive-or (XOR) gate.

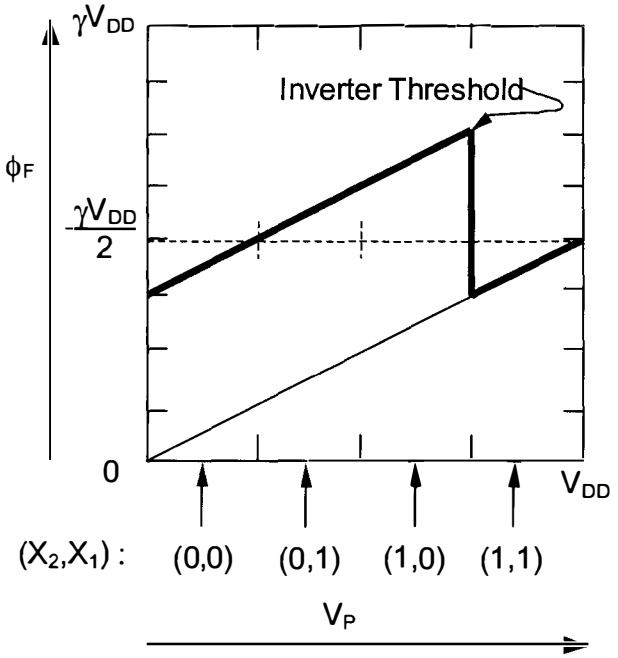


FIGURE 26 FLOATING GATE POTENTIAL DIAGRAM OF XOR FUNCTION

The heavy line represents the variation in the floating-gate potential. The inversion threshold of inverter 'A' is ¾· V_{DD}, this is the initial offset of the potential. As V_P passes the threshold of inverter 'A', it drops to zero. Below is a graph showing the contribution of the two components-

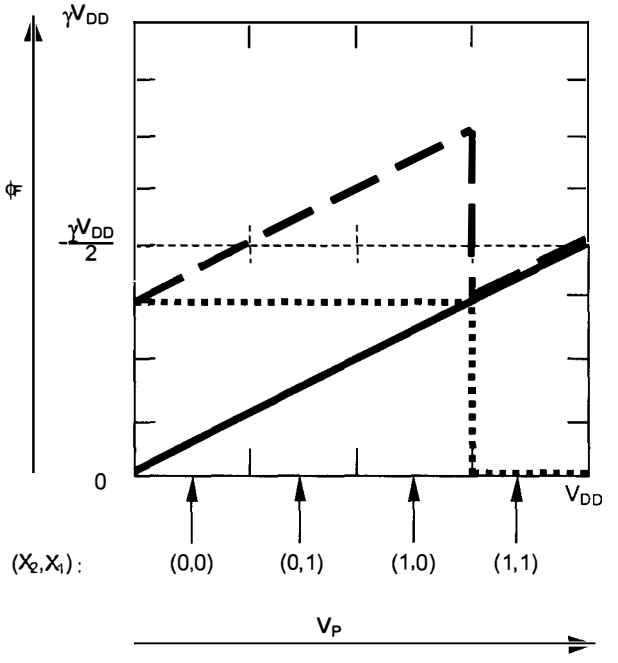


FIGURE 27 SEPARATED COMPONENTS OF FGPD OF XOR FUNCTION

The dotted line represents the contribution of the variable threshold inverter and the heavy line shows the increasing V_P. The dashed line is the total

floating gate potential. Examining the output states of the inverter shows the operation is equivalent to that of the XOR function. The floating-gate potential diagrams of other logic functions are shown below-

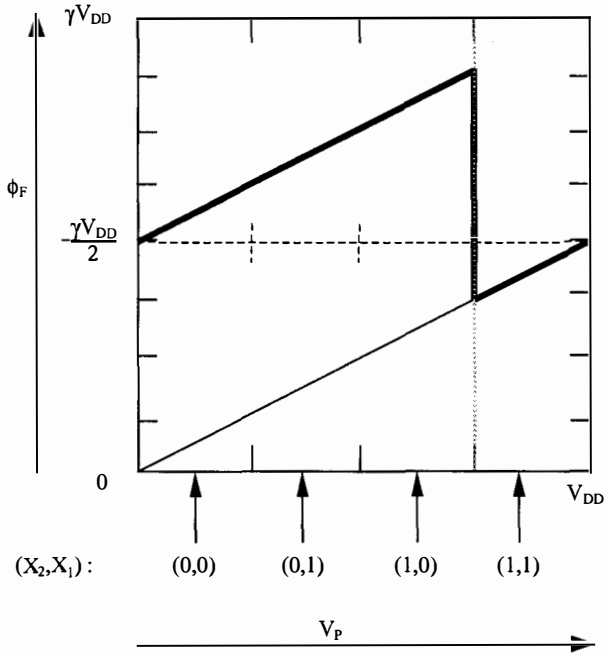


FIGURE 28 NAND

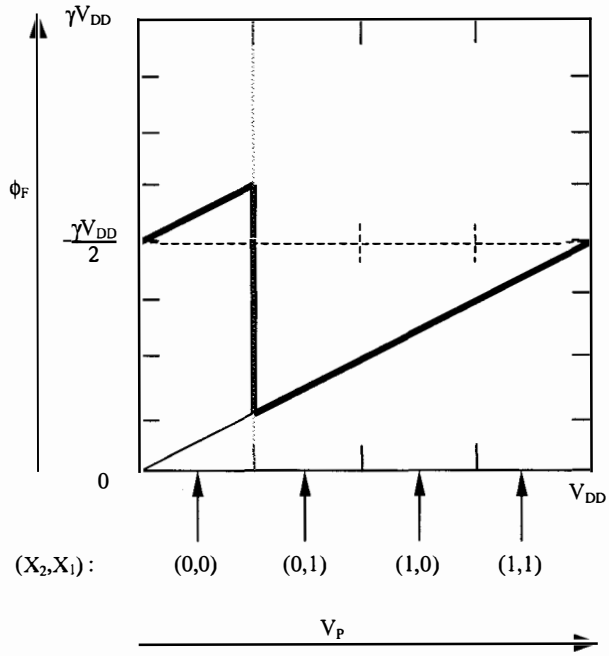


FIGURE 29 NOR

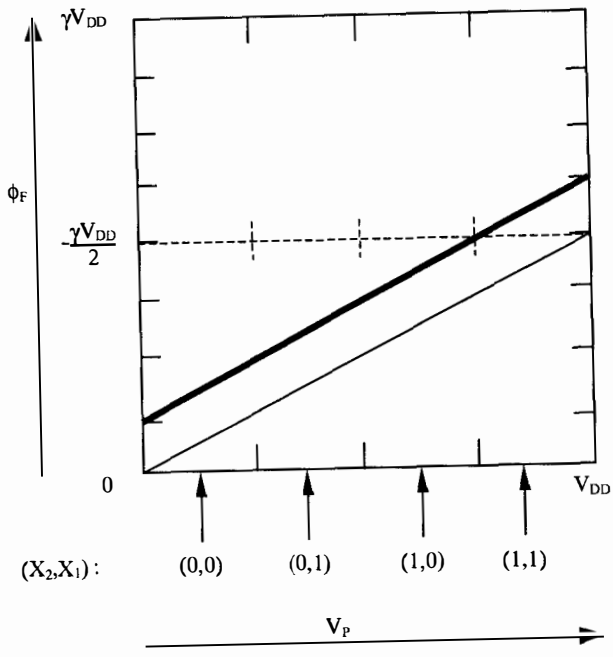


FIGURE 30 AND

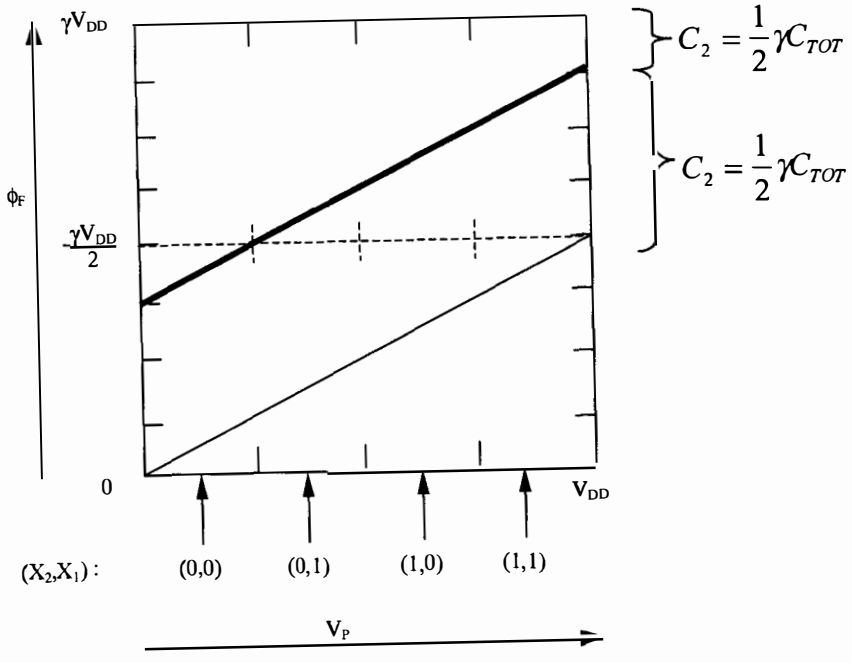


FIGURE 31 OR

Note that the NAND and OR gates do not have a discontinuity in their FGPDs therefore they do not need the variable threshold inverter or the floating gate attached to it as shown in Figure 25.

2.7.2 Soft-Hardware Logic Circuit

This configuration [6] extends the semi-analogue method used above so that the logic function is dynamically reconfigurable. The circuit uses both the source-follower νMOS transistor configuration and the standard νMOS inverter. Figure 32 also shows how variable-threshold inverters are used.

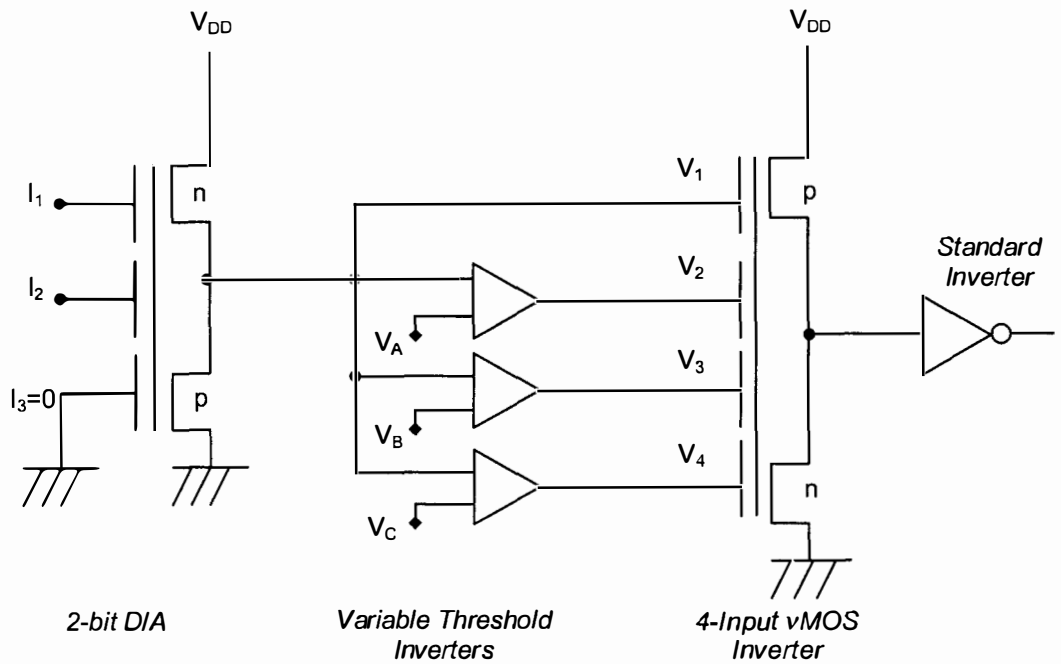


FIGURE 32 SOFT-HARDWARE LOGIC CONFIGURATION

The inversion thresholds of the three variable-threshold inverters (A, B and C) are equal to V_{DD}-V_A, V_{DD}-V_B and V_{DD}-V_C, respectively. The capacitor sizes of the 4-input νMOS inverter are

$$\begin{aligned} C_1 &= \frac{1}{2}\cdot\gamma\cdot C_{TOT} \\ C_2 &= \frac{1}{4}\cdot\gamma\cdot C_{TOT} \\ C_3 &= C_4 = \frac{1}{8}\cdot\gamma\cdot C_{TOT} \end{aligned} \tag{31}$$

Other design parameters are:

$$V^*_{TN} + V^*_{TP} = 0$$

And

$$\beta_R = 1$$

hence $V^*_1 = \gamma \cdot V_{DD}/2$. Inputs I_1 and I_2 are binary quantities that are converted into an analogue voltage by the D/A converter [6]

$$V_1 = V_{DD} \cdot \left(\frac{1}{4} \cdot I_1 + \frac{1}{2} \cdot I_2 \right) + \frac{1}{8} \cdot V_{DD} \tag{32}$$

Control signals, V_A, V_B and V_C determine the digital inputs presented to the 4-input νMOS inverter, allowing up to 16 different logic functions to be performed. The values to achieve this are $\{V_A, V_B, V_C\} = \{ ¼ , ¼, 1 \} \cdot V_{DD}$,

This technique allows an appreciation of the flexibility available when combining the νMOS devices in analogue and digital modes.

2.8 DIGITAL IMPLEMENTATIONS

Removing the D/A converter from the above circuit decreases the number of interconnects and increases circuit density and speed. This technique uses the variable threshold inverter technique. Instead of the single signal input line multiple lines are used, and the XOR gate is then connected as shown in Figure 33.

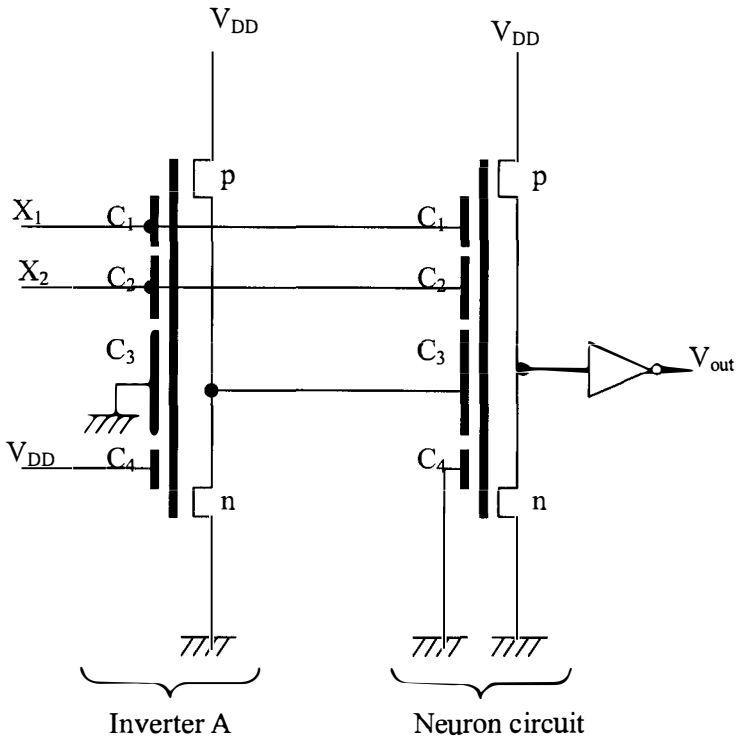


FIGURE 33 DIGITAL IMPLEMENTATION OF XOR GATE

A modified floating gate potential diagram is used to describe the behaviour [7]. But this is somewhat difficult to conceptualise, so Shibata's method recommends using the original format and then converting it to the modified version.

It should be noted that the above scheme uses inverter *A* simply as an element that will provide a discontinuity in the potential of the gate at the right (the neuron circuit). One such inverter is needed for every discontinuity in the floating gate potential diagram.

2.8.1 Full Adder Implementation

As an example of the reduction in complexity that can be achieved using νMOS the full adder circuit is presented below. Figure 34 shows a typical implementation using standard CMOS. Figure 35 is the same circuit using νMOS, where the reduction in the number of transistors used is significant [11].

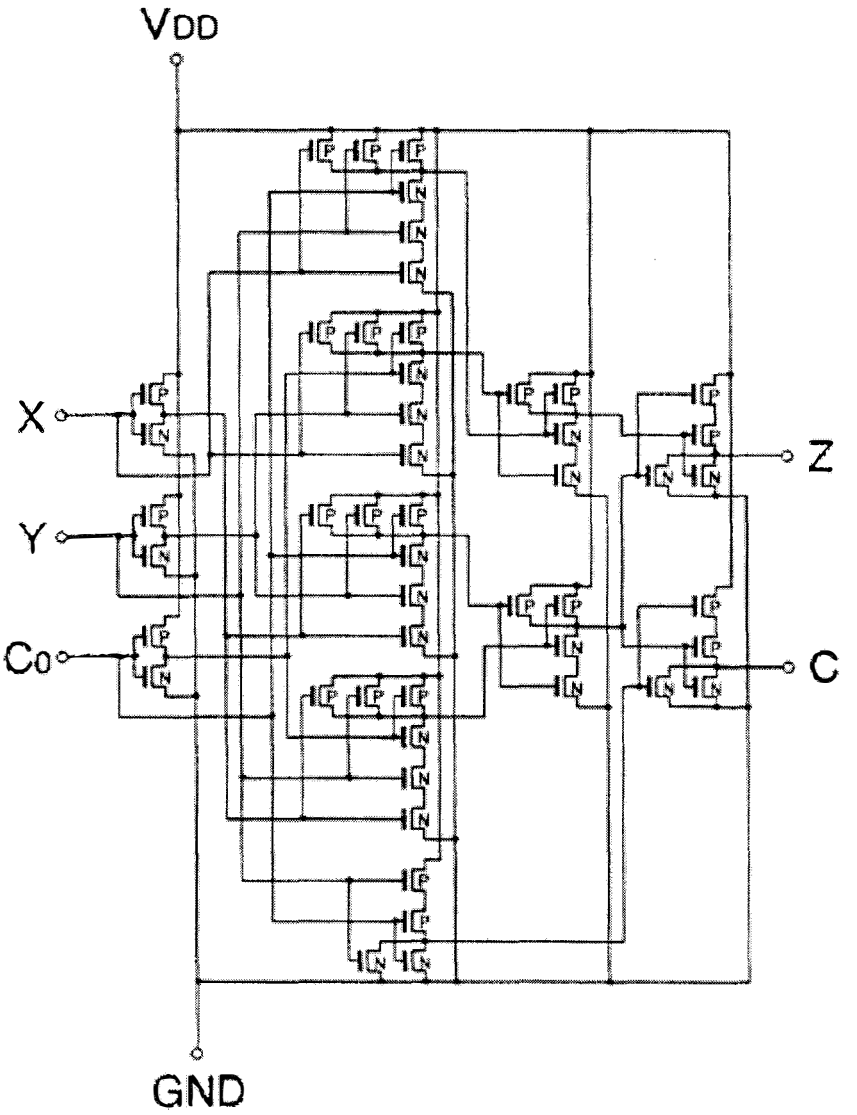


FIGURE 34 CMOS FULL ADDER

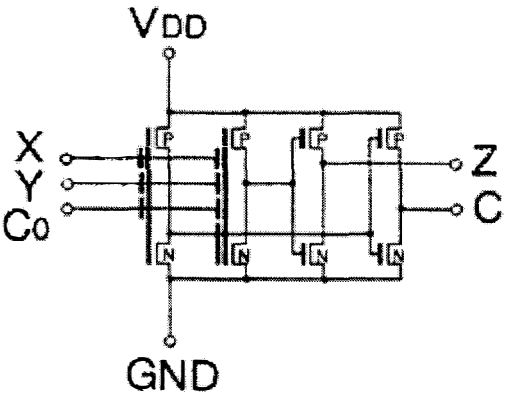


FIGURE 35 VMOS FULL ADDER

A notable feature of the νMOS circuit is the low number of transistors, using a total of eight, in the form of two normal CMOS inverters and two νMOS inverters [12]. The circuit design is simplified due to the symmetric nature of the operation, that is, the order of the inputs is unimportant to the result. It is highly important to note that area is *not* compared here. There are also many non-static implementations of the full adder that are very efficient in terms of the number of transistors. The example is mainly illustrative in its comparison.

2.8.2 Multiplier Design

The operation of multiplication in CMOS can be an area-consuming task that is required in, for example, Digital Signal Processing. This example [13] is for a one-bit multiplier cell, having inputs

- a_1 and a_2, which are to be multiplied,
- the sum bit s_i, and,
- the carry bit c_i, which are from preceding cells in the multiplier array.

These are used to calculate the sum and carry outputs, which are s_{i+1} and c_{i+1}. The operation is performed by the logical AND of a_1 and a_2, forming a partial product, which is added to the sum and carry, bits s_i and c_i. Such an element is used in the scheme for a binary multiplier, or for the two's complement multiplier that is shown in Figure 36 [14].

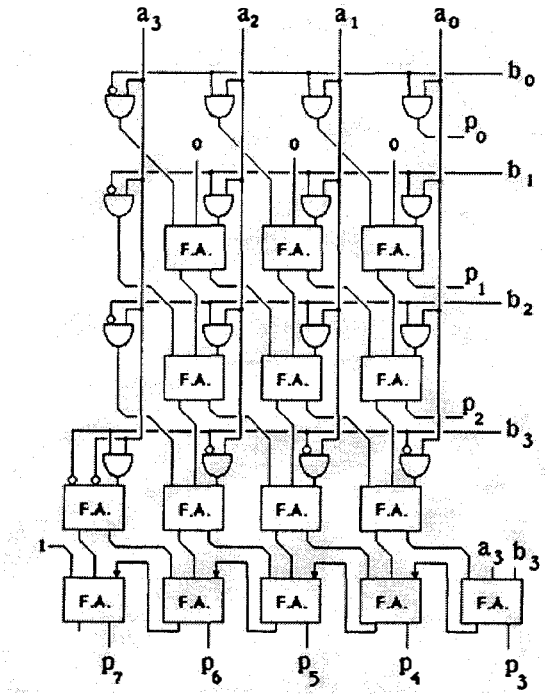


FIGURE 36 TWO'S COMPLEMENT MULTIPLIER CONFIGURATION

The truth table for the circuit is shown in Table 2.

a_1	a_2	s_i	c_i	s_{i+1}	c_{i+1}
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	0	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	0	1
1	0	0	0	0	0
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	0	1
1	1	1	0	0	1
1	1	1	1	1	1

TABLE 2 TRUTH TABLE FOR ONE-BIT MULTIPLIER CELL

Two designs are considered. The first, which has some speed, power and stability considerations, is shown in Figure 37. This is just one of the cells in

the diagram of Figure 36. Note that an array of such cells is needed for multi-bit implementation .

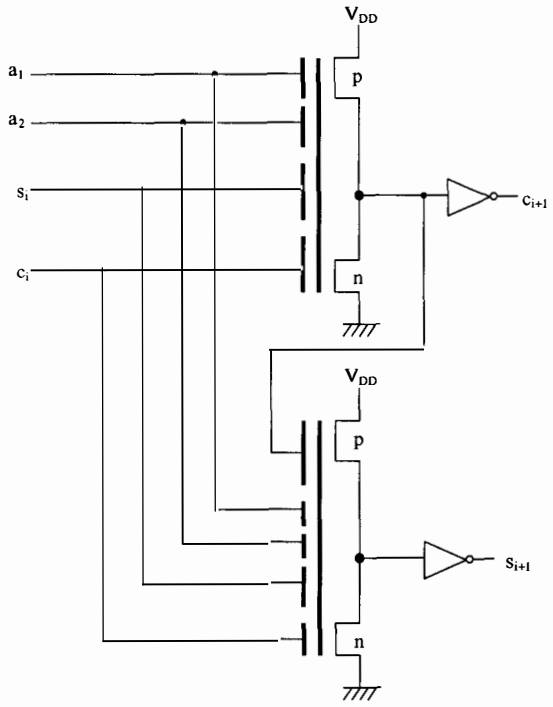


FIGURE 37 NEURON MOS MULTIPLIER CELL

This configuration uses approximately 30% of the area of a standard, optimised CMOS cell [13]. An improved circuit that uses positive feedback and two clock signals is shown in Figure 38. This circuit has improved robustness against parameter fluctuations, where only the matching of the n-MOSFETs having importance. Clock signals Φ_c and Φ_s trigger the evaluation cycle, until which time the output signals are stable. The carry bit must be available before evaluation of the sum bit can be conducted. The reference voltage can globally adjust the switching voltage, which is used to counteract the effects of process variations.

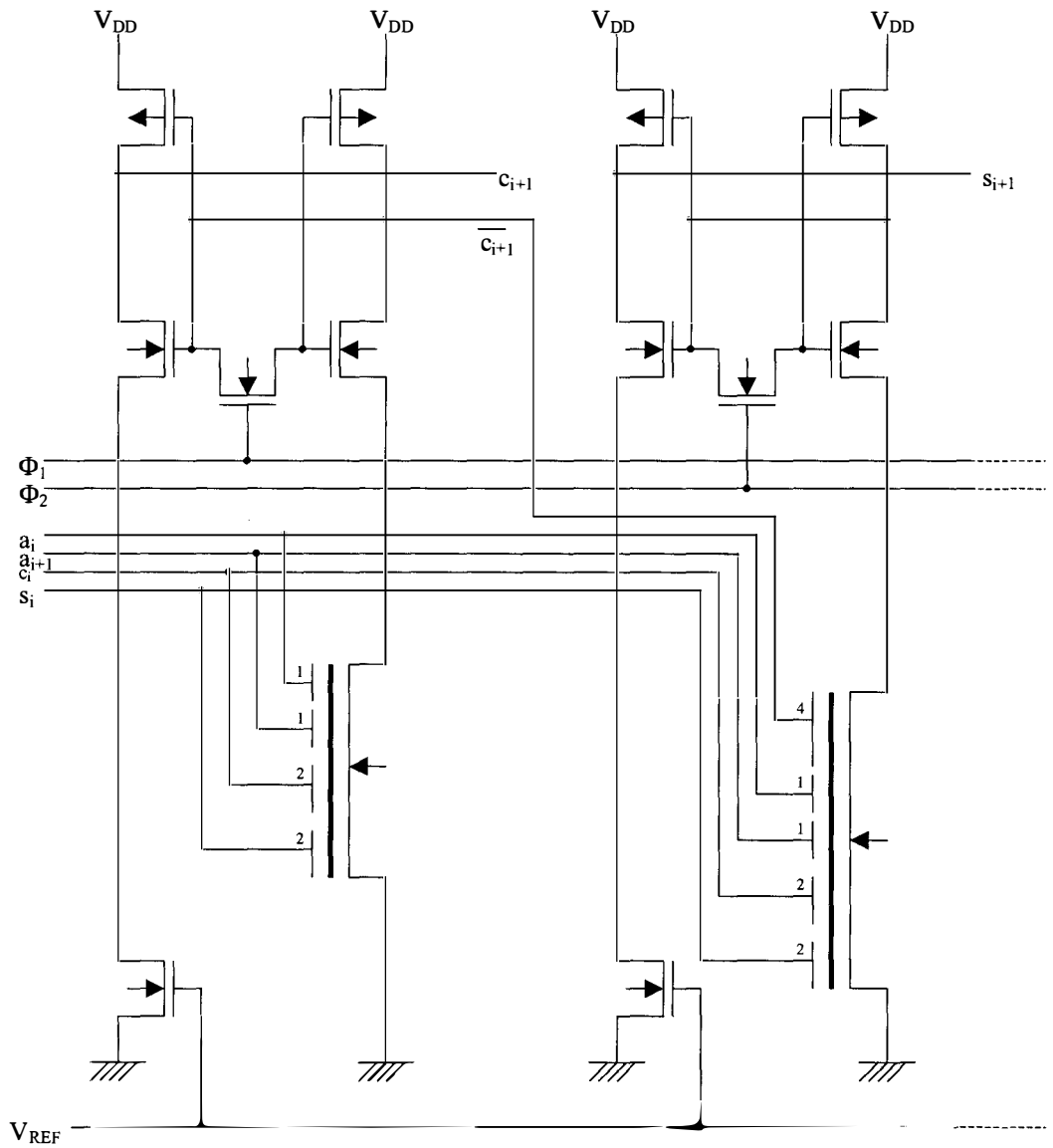


FIGURE 38 IMPROVED NEURON-MOS MULTIPLIER CELL

This configuration results in a 50% larger chip floor area than the previous multiplier, which, however, is still an improvement over standard CMOS implementations. The speed is comparable to that of the CMOS versions, and exhibits less frequency-dependent power consumption [13].

2.9 THRESHOLD ADJUSTMENT

Kotani et al. [8] address the possibility of inverter threshold changes by providing a so-called 'auto threshold adjustment'. This operates by switching the floating gate to the output terminal when the inputs are switched to either ground or V_{DD} in order to

achieve an average for the inputs to $V_{DD}/2$. This scheme is used primarily for device fabrication parameter fluctuations, and complicates the circuit considerably in that a previously completely asynchronous circuit now has a reset clock cycle. This method is neither redundant nor undesirable however, as the application and setup conditions of the νMOS circuit may dictate that the auto-threshold-adjustment is necessary.

2.10 CLOCKED NEURON-MOS CIRCUITS

In [15] the floating gate charge is initialised via a clock-driven switching transistor. This also has the purpose of adjusting the switching threshold, alleviating the fluctuations that arise from fabrication. Figure 39 shows a three-input XOR gate using two νMOS inverters and six switches, SW_1 to SW_6. $SW_1 - SW_3$ and SW_5 bring the input terminals to ground or V_{DD} in order to create an average of $V_{DD}/2$ on the inputs. SW_4 and SW_6 simultaneously connect the floating gate to their respective inverter outputs. This biases the inverters at the most susceptible point in the transition region. Thus both the floating gate charge and the switching threshold are biased optimally at the end of each reset cycle.

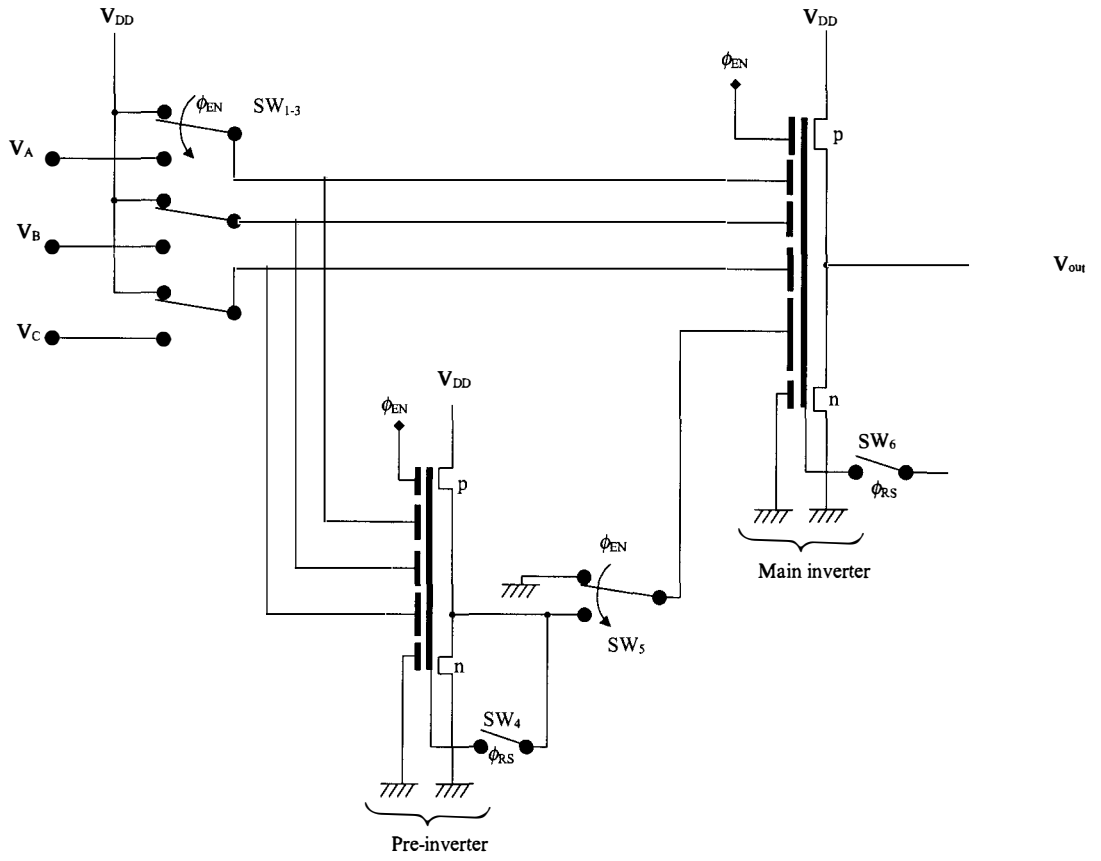


FIGURE 39 CLOCKED VMOS XOR CIRCUIT

The scheme is further extendable into the so-called 'pipelined vMOS logic' via the inclusion of latches as an intermediate stage between the two inverters. The biasing of the inverters leads to a DC path during the reset and evaluation cycles. This is addressed by the self-threshold adjustment circuit shown in Figure 40.

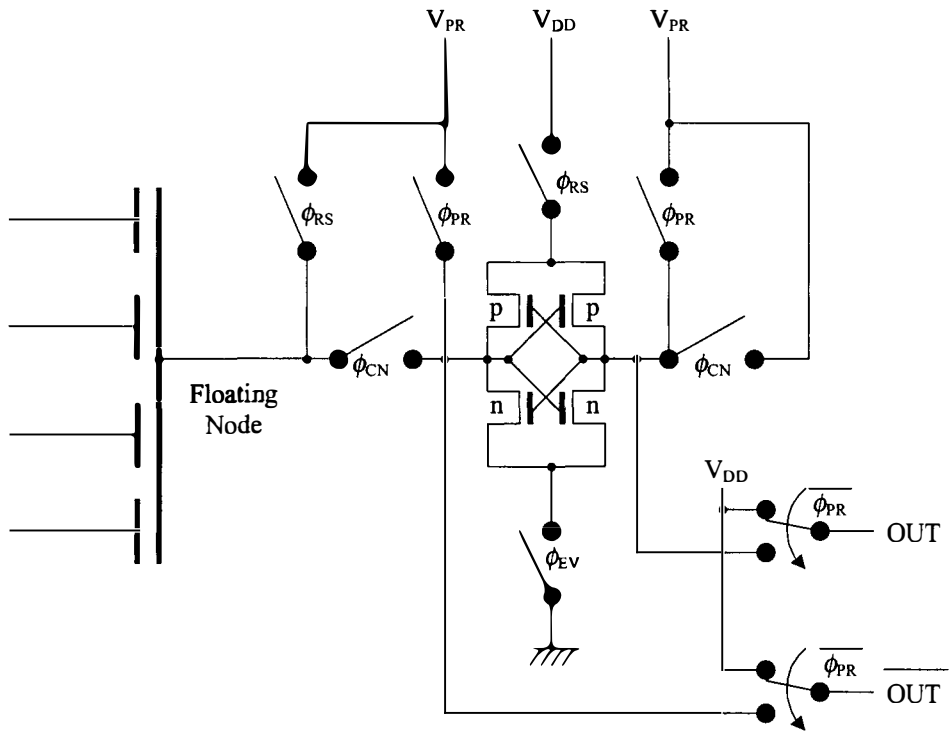


FIGURE 40 SELF-THRESHOLD ADJUSTMENT CIRCUITRY

The circuitry connected to the floating gate is a dynamic sense amplifier that is commonly found in DRAMs. The νMOS circuit is quote as having an advantage over standard CMOS implementations in both power and circuit simplicity [15].

2.11 CONCLUSIONS

This section outlined the theory behind neuron-MOS technology. Visualisation tools such as the floating gate potential diagram (FGPD) were discussed. Some limitations of the technology were also detailed.

Part of the application envisaged for the A/D converter is in a massively parallel array of 'Smart Pixels'. Removing the need for a set of global control signals in such an array reduces interconnection complexity. Maintaining an asynchronous nature for the smart pixel array would eliminate clock skew for this subcircuit.

This chapter showed how the use of νMOS can reduce the number of transistors that are used in some common digital operations. However, a more meaningful

comparison would be based on silicon area required to implement the circuit. But this would involve the design of all circuits to be compared using the same CMOS process; this, however, is outside the scope of this thesis. There is a lack of information contained in the literature addressing this issue.

The literature which concerns νMOS technology and its application was covered with attention to scope and depth. The scarce amount of information on design methodology and implementation-specific techniques is apparent from the extent of the available literature.

Chapter 3

Analogue to Digital Conversion

3.1 INTRODUCTION

Analogue to digital (A/D) conversion is the process of quantising an analogue value, usually a potential, into a number of digits, usually binary, in discrete time. A/D conversion is a fundamental signal processing operation, without which the interface of digital circuitry to the 'real world' would not be possible. The sheer vastness of literature on the subject is testament to the importance of the process of quantising an infinitely variable source into a finite range of values.

In view of the immensity of the task of assessing all of the literature available on the topic, this chapter does not attempt to provide an exhaustive survey of the history and

development of A/D conversion. Instead, the types of A/D converter that are available, as well as the current state-of-the-art of the literature concerning A/D conversion are presented. This provides a basis upon which the novel A/D converter, which is the topic of the research, may be compared.

3.2 PERFORMANCE SPECIFICATIONS

The accuracy of an analogue-to-digital converter (ADC) is the maximum sum of all errors, including the quantisation error. The sources of error and the performance specifications are listed below [16]. It should be noted that neither the literature nor commercial A/D converters do not quote all of the figures listed below. Rather, a selection of, perhaps, 'favourable' figures of merit are given. Nevertheless, certain figures are fundamental to the operation, these are resolution, speed of conversion and linearity.

3.2.1 Resolution

This is the smallest incremental change in input that can cause the output to change to the next adjacent code. An n-bit ADC can resolve 1 part in 2^n. The general case is that the resolution is not exceeded by errors that would corrupt more than ½ the least significant bit. Another general rule is that with increasing resolution, the slower the rate of conversion and the greater the expense.

3.2.2 Quantising Error

If an ADC had infinite resolution then the numerical values of the output, for all given inputs possibilities, would resemble a straight line when plotted. ADCs have a finite resolution (as a design parameter), and thus will deviate from this line. It is desirable to have the ADC output offset by ½ LSB, as shown in Figure 41 [16].

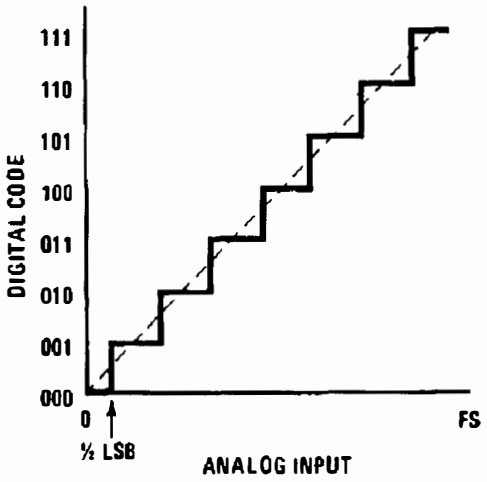


FIGURE 41 QUANTISING ERROR IN A/D CONVERTERS

3.2.3 Scale error

The difference between the actual input voltage at full scale and the actual full-scale output code. A loss in dynamic range is experienced for A/D converters that do not achieve full scale output for a full scale input. Conversely, for circuits which cannot account for the case where the full scale output is exceeded for a less than full scale input then 'dead-zones' exist, and the effect of noise is increased.

3.2.4 Offset error

Also referred to as a zeroing error, this is the required voltage change to get a zero value reading when the input is at the minimum. This is expressed as a percentage of full scale or a fraction of LSB.

3.2.5 Hysteresis error

A dependence on the direction of voltage swing for output code change. This error should not exceed ½ LSB.

3.2.6 Linearity

A measure of how the transfer characteristic differs from a linear slope. This does not include quantising, zero, or scale errors. This error, when quoted, is in addition to quantising or resolution errors.

3.2.7 Monotonicity

If an ADC is monotonic then it will not change the direction of the output slope for an unchanging input slope. For example, if the input is increasing linearly then no codes are present at the outputs that decrease from a previous code.

3.2.8 Temperature coefficient

Every specification other than design specifications is potentially affected by temperature variation.

3.2.9 Long-term drift

This is a result of changes in characteristics due to aging of components. Most commonly affected parameters are linearity, monotonicity, scale and offset.

3.2.10 Supply rejection

The ability to withstand changes in supply voltage fluctuation. This figure is represented by a percentage change of full scale at room temperature.

3.2.11 Conversion rate

The number of conversion per second for repetitive calculations. The time taken for conversion may be either independent or dependent on the input voltage swing between conversion instants, this is a feature of the ADC technology chosen. The conversion times should be measured at full resolution.

3.2.12 Input impedance

The load the ADC places on the input source.

3.2.13 Output drive capability

The driving capability of the digital outputs. This may be given as a current, or voltage into a given load. Another method is the number of standard TTL loads that may be driven.

3.3 OUTPUT CODES

The application may dictate the desired format of the digital output word. The configuration of the A/D converter may also influence the output word format. The expense of arranging the circuit to provide a certain type of output code may make the circuit unsuitable for a particular application. The possible codes are –

3.3.1 Natural Binary

This is where zero signal is represented by all 0's and full scale is all 1's. This is shown in Figure 42. This format is most suitable for applications that require positive quantities only, or those that involve only a single rail power supply.

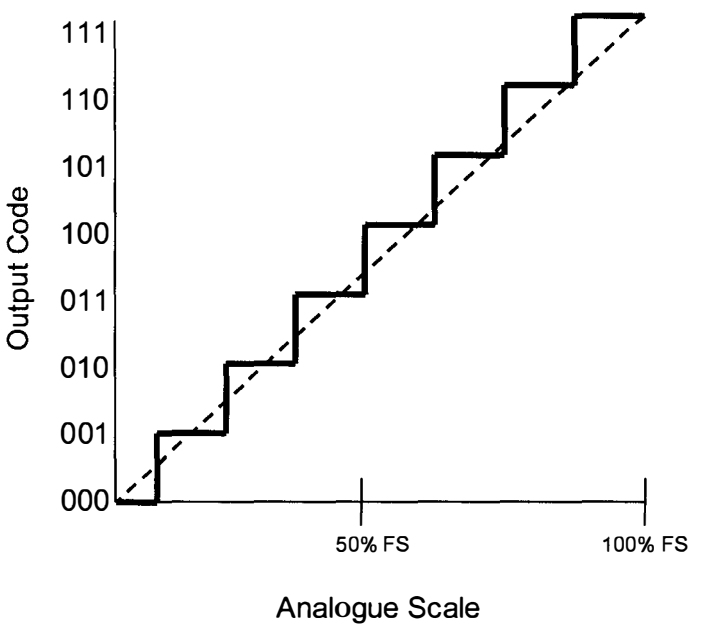


FIGURE 42 NATURAL BINARY A/D CONVERTER REPRESENTATION

3.3.2 Complementary Binary

The inverse of natural binary. Full scale is all 0's and zero signal is all 1's output. This type of code is only included in this section for completeness, where the possible applications are those that involve a separate A/D converter for negative quantities or those that need negated values.

3.3.3 Binary Coded Decimal (BCD)

Four binary digits are used to represent one decimal digit. This is used in systems where the output is intended for direct decimal digit output. The loss in resolution from using BCD instead of binary increases as more digits are resolved. The use of BCD is not entirely incompatible with microprocessors, as a BCD arithmetic mode is often available. However, the configuration of a circuit that can produce BCD without an intermediate result that is normal binary is not covered by the literature.

3.3.4 Offset Binary

The scale is offset by ½ full scale in order to represent positive and negative values. The maximum negative number is all 0's; zero scale is a leading 1 followed by all 0's; and full positive scale is all 1's. Refer to Figure 43 for a representation of this scheme.

3.3.5 2's Complement

This scheme involves the representation of positive values results in standard binary, but negative values are represented by quantities that exceed 2^{n-1}, n being the number of bits resolution. To get the 2's complement form of a number that is intended to be negative, the individual bits forming the positive-binary representation of the word are inverted and then the quantity 1 is added. To add two 2's complement numbers, whether positive or negative, a simple binary numerical addition is used, yielding a correct result. Thus the code segment concerned with the addition does not need to differentiate

between positive and negative numbers. This scheme is compared to others in Figure 43.

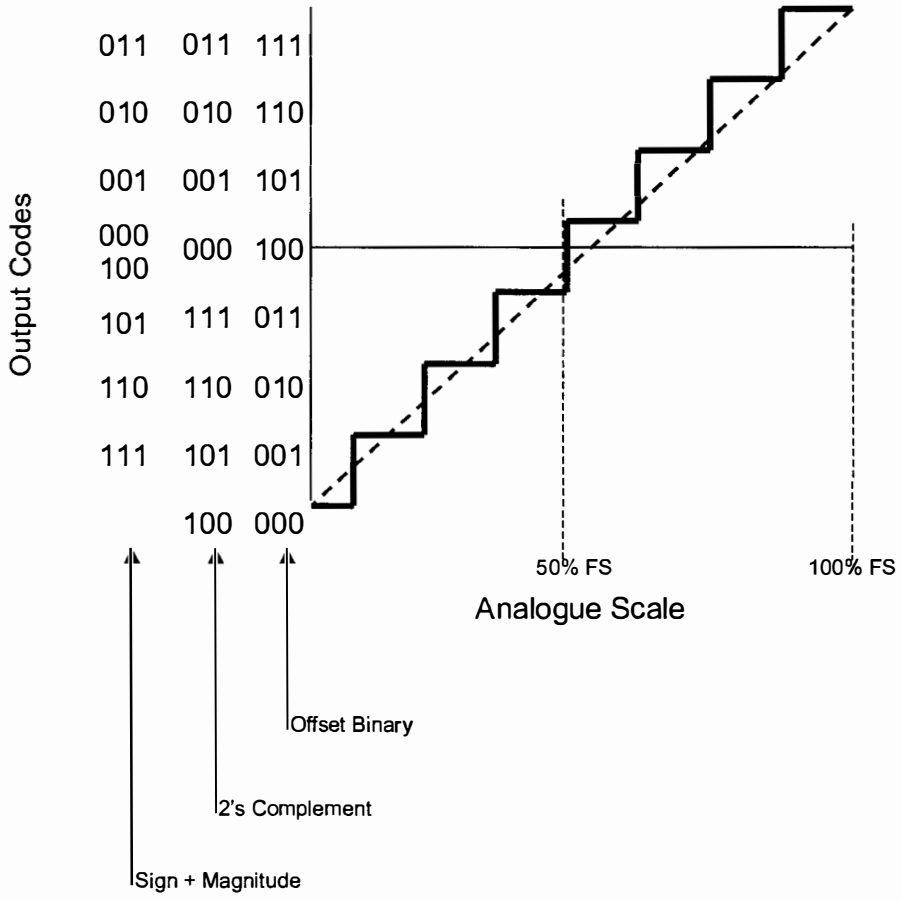


FIGURE 43 ADC OUTPUT CODES

3.3.6 Sign Plus Magnitude

This uses the least significant bits to represent the magnitude of the absolute value of the signal, with the MSB used to denote the sign. One of the codes is 'wasted' in providing a 'negative zero', also shown in Figure 43. The advantage to this method is that only one bit needs to be changed for small variations about zero. A typical example of an application that may use this scheme is a digital voltmeter.

3.4 A/D CONVERTER TYPES

There are a number of types of A/D converter [17]; these are detailed in the following sections. The rationale behind choosing one method over another is determined by design parameters such as speed of operation, number of bits of resolution, desired accuracy and available circuit area.

3.4.1 Flash converter

The circuitry performs the conversion in one cycle of operation. This is generally the fastest method of conversion. For n bits resolution it uses 2^n number of comparators. It is usually characterised by high-speed operation at the expense of circuit area. The input is fed to all comparators simultaneously, the output being decoded digitally. Each comparator must be supplied with a precise reference voltage for correct operation, which can be provided by a resistive ladder.

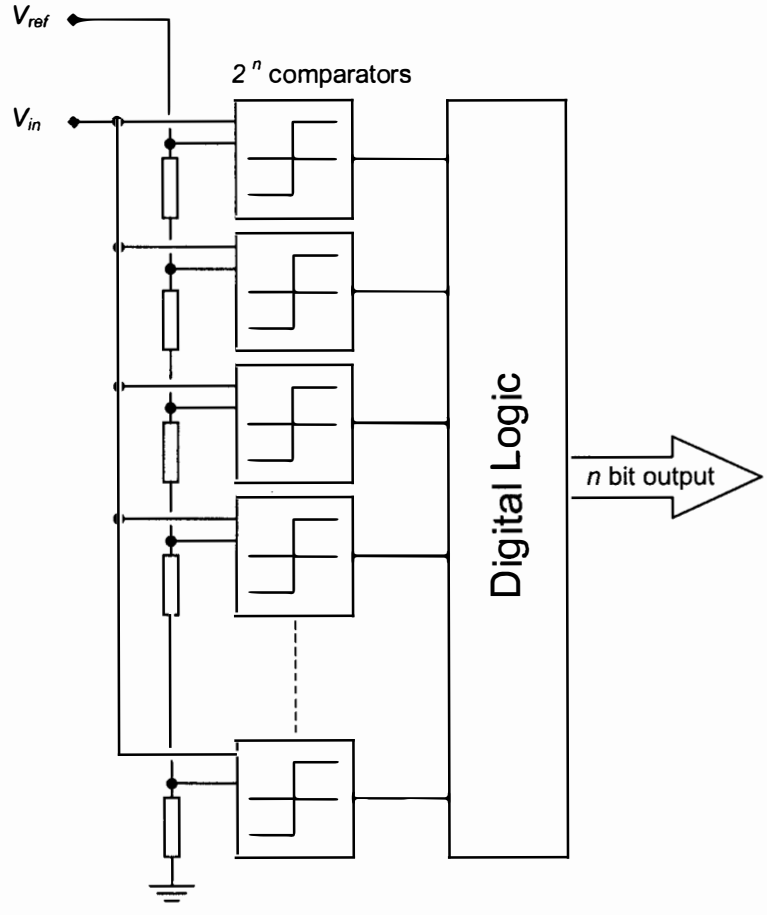


FIGURE 44 FLASH CONVERTER

3.4.2 Two-step flash

This type of flash converter is divided into two stages for fine and coarse conversion. The first, coarse conversion stage, resolves the most significant bits. This result is then converted into an analogue form suitable for conversion by the second stage in the ADC, which resolves the remaining, lower order bits.

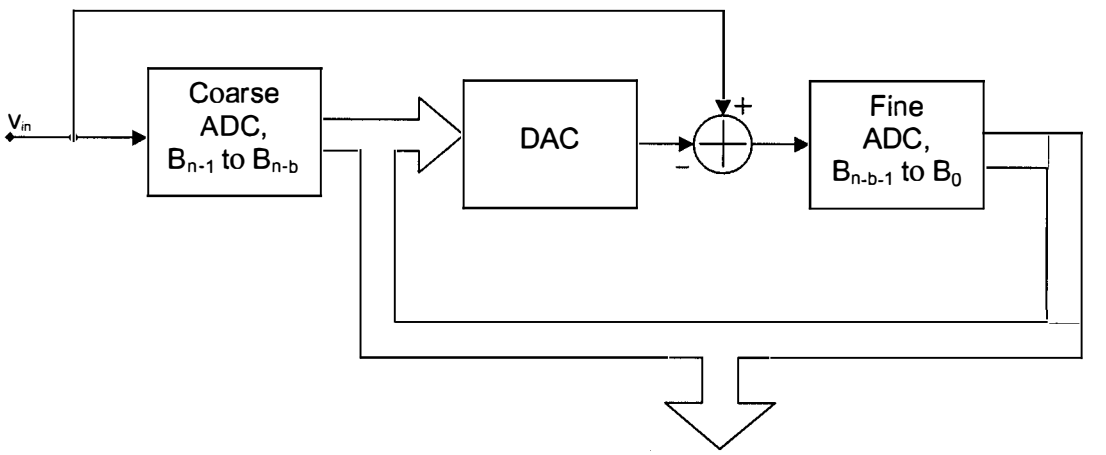


FIGURE 45 TWO-STEP FLASH CONVERTER

3.4.3 Monotonic ADC

This converter uses a counter, which is reset to zero at the beginning of every conversion cycle, to provide an input to a digital to analogue converter. The analogue result of this conversion is compared to the input using a comparator. Once the comparator changes state, the counter is halted and the result is available as a digital word. This scheme is shown in Figure 46 [18].

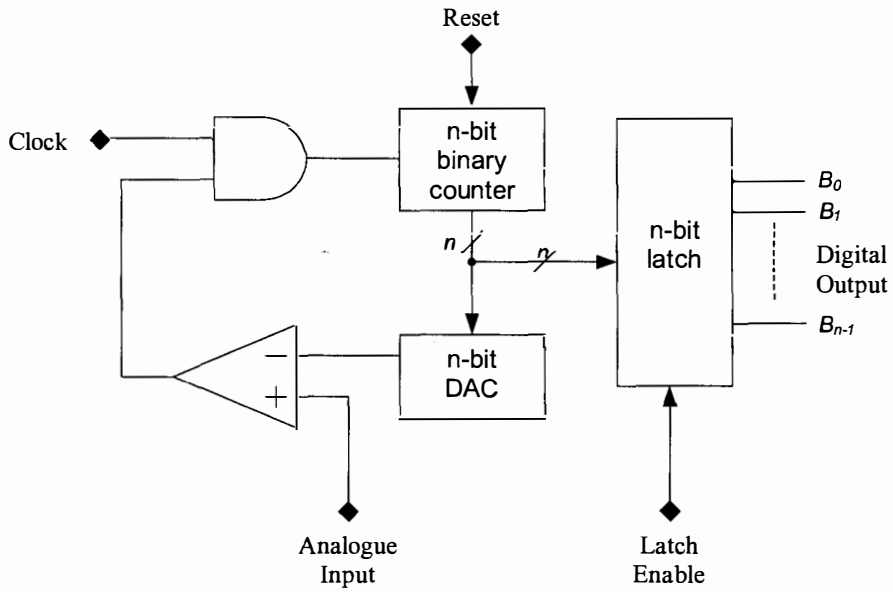


FIGURE 46 MONOTONIC ADC

The conversion time for this scheme is variable, being directly proportional to the input value. The operation is described in Figure 47.

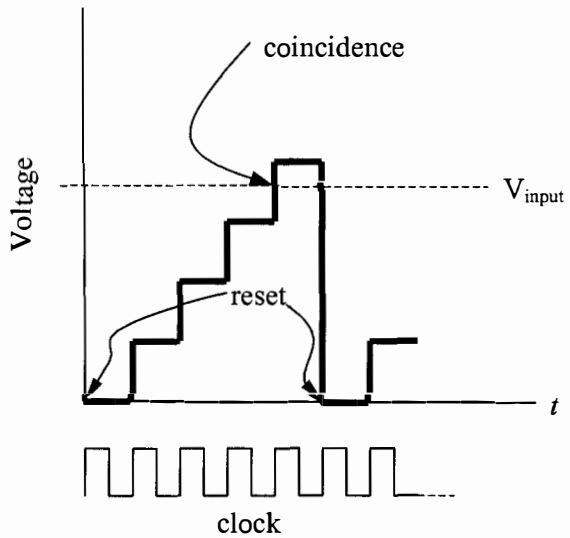


FIGURE 47 SIGNALS IN MONOTONIC ADC

3.4.4 Tracking ADC

The inefficiency of the monotonic ADC is addressed by provision of the ability to not only count upwards, but downwards as well. The block diagram appears as Figure 48.

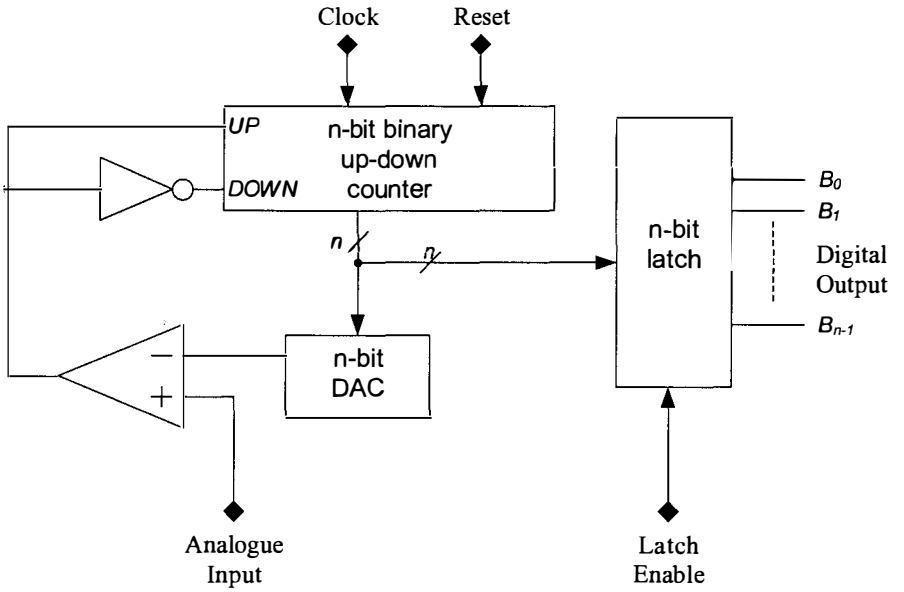


FIGURE 48 TRACKING ADC

The conversion process starts with the counter reset to zero, and an upward count initiated. Upon coincidence, which in upward count mode means that the DAC output is greater than that of the analogue input, the digital output is obtained. The counter is then placed into downward-counting mode, until coincidence is again obtained. Coincidence for downward counting mode is when the DAC is less than the input. The signals are shown in Figure 49 [18].

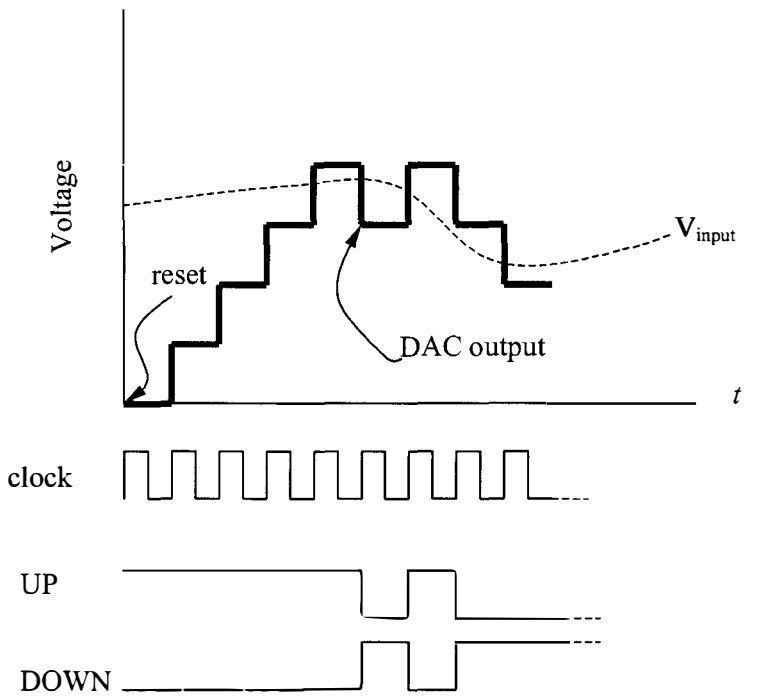


FIGURE 49 SIGNALS IN TRACKING ADC

3.4.5 Recursive ADC

This converter type provides serial data output by using one comparator and resolving bits consecutively. This method has simple circuitry but is slow. The accuracy relies principally on the ability to continually amplify the addition of the 1-bit DAC and input voltage by two. Theoretically this converter can resolve an infinite number of bits, but is limited due to the nature of its analogue processes.

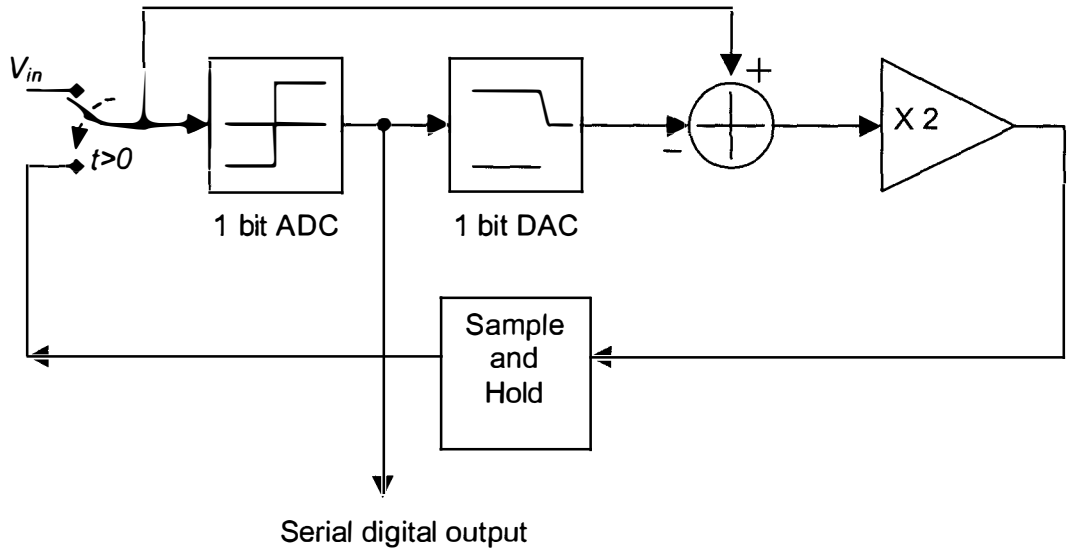


FIGURE 50 RECURSIVE ADC

3.4.6 Successive approximation

This involves using a number of cycles to provide an increasing number of bits of resolution. This method is similar to the recursive ADC, but the entire word is available, with a bit being resolved each clock cycle. The resolution is limited by the digital to analogue converter stage. The word is available throughout the conversion process, increasing in accuracy as the cycle approaches completion. Usually the most significant bit is resolved first.

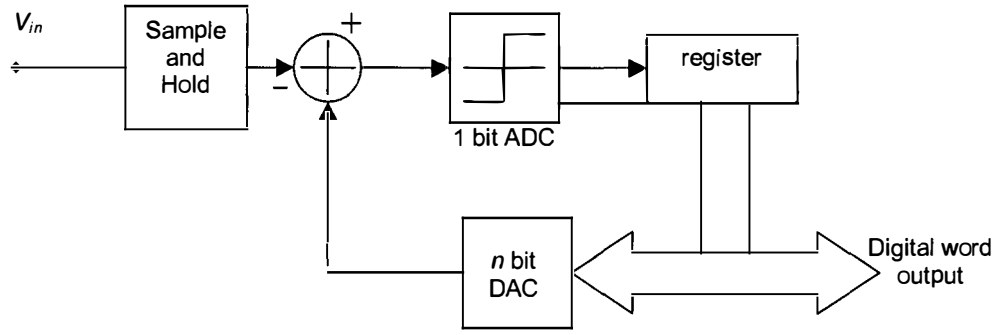


FIGURE 51 SUCCESSIVE APPROXIMATION ADC

3.4.7 Dual Slope ADC

This uses an internally generated reference signal compared to the input signal, the conversion being a result of the reference signal equalling the input [9, p748]. This provides faster conversions for small changes of input than for large changes. The input is allowed to charge C through R for a fixed amount of time. The control circuit then discharges C via V_{REF} which has a fixed slope independent of the input. The time taken to discharge is proportional to the charge on C. The counter is clocked until C is discharged and provides a digital value which is the result of the conversion.

Figure 52 shows this scheme. Note that the exact values of R and C are unimportant.

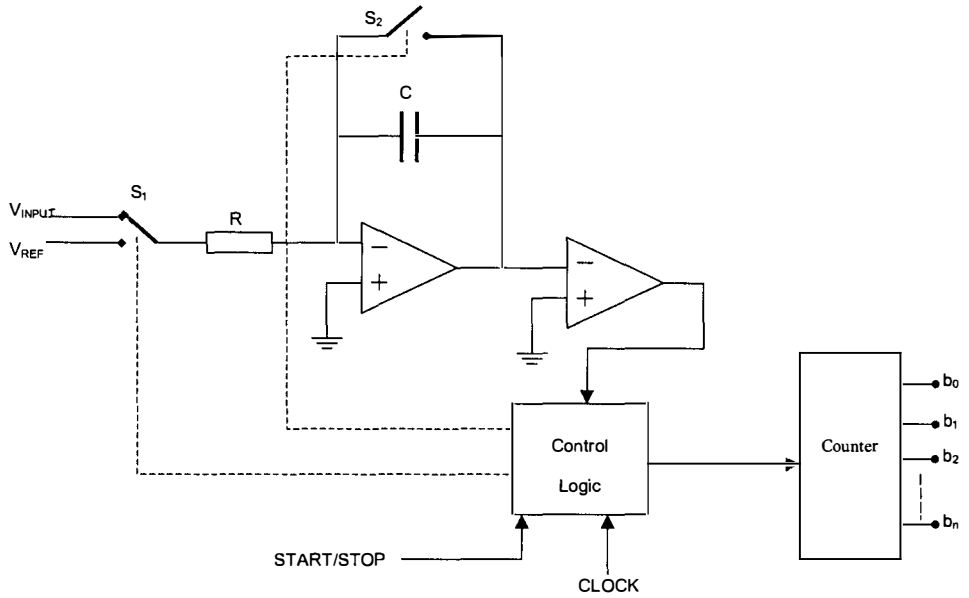


FIGURE 52 DUAL-SLOPE ADC

A single slope version of this circuit is possible, but suffers from the same speed penalty as the monotonic converter. Effectively this is the analogue version of the tracking ADC.

3.4.8 Sigma-Delta modulator

This uses an internally generated difference signal to determine the output. Feedback of a DAC is used to gain increased converter resolution of an ADC. This scheme has no advantage over a dual slope ADC for uncorrelated data.

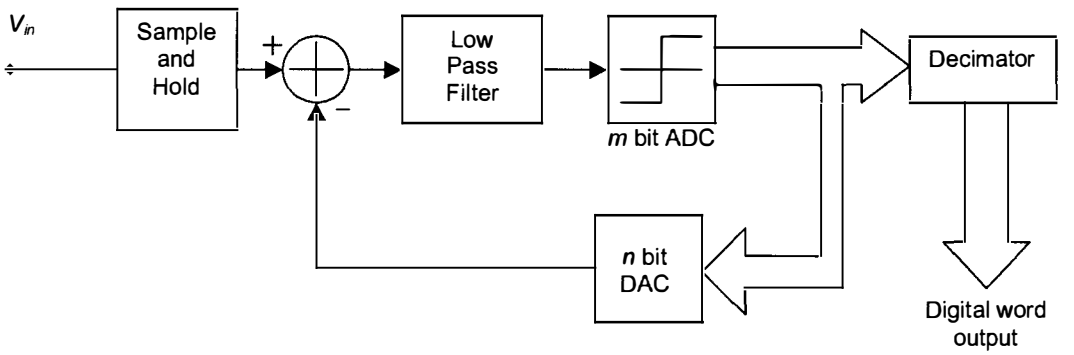


FIGURE 53 SIGMA-DELTA MODULATOR

3.5 CONTEMPORARY METHODS OF ANALOGUE-TO-DIGITAL CONVERSION

Contemporary research aims at providing improvements in speed, area efficiency, accuracy and precision of the analogue-to-digital conversion process. This section covers the methods that have recently been presented in the literature.

Ogawa et. al. [19] describe an algorithm for successive A/D conversion that uses a sample and hold circuit in conjunction with a serial D/A subconverter to generate a threshold voltage sequence. The (serial) process of successive approximation is exploited by the use of the serial D/A converter, each bit being loaded into it, the MSB first, as the conversion takes place. The serial D/A converter is intended to aid in a reduction of chip area. This scheme is shown in Figure 54.

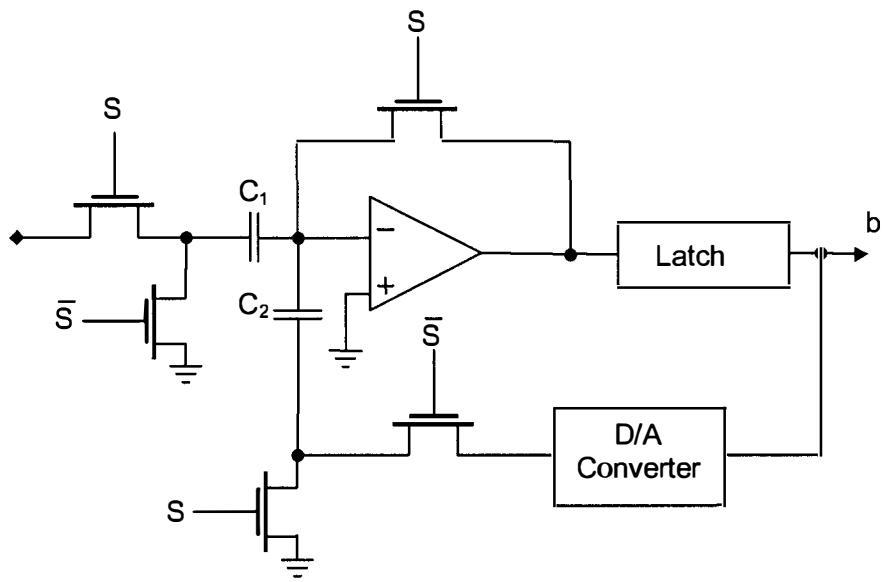


FIGURE 54 OGAWA'S SERIAL A/D CONVERTER

Control signal *S* is used to switch between the initial loading of the input voltage into C1, and the subsequent operation of successive approximation. Once the conversion is complete, S is again pulsed to load the next analogue input value.

Analogue pre-processing is used in [20] to achieve higher conversion speed. The function of conversion is derived from a *subranging* cell acting as a front end to a standard flash A/D converter, which is of less bit resolution than the overall circuit. The subranging circuit is comprised of a comparator array, a subtracter circuit, switch array and a digital encoder. This produces the most significant bits. The subtracters are used to relocate the input analogue signal into a range that can be converted by the circuitry responsible for the least-significant-bits. This is a flash A/D converter. Figure 55 shows this scheme.

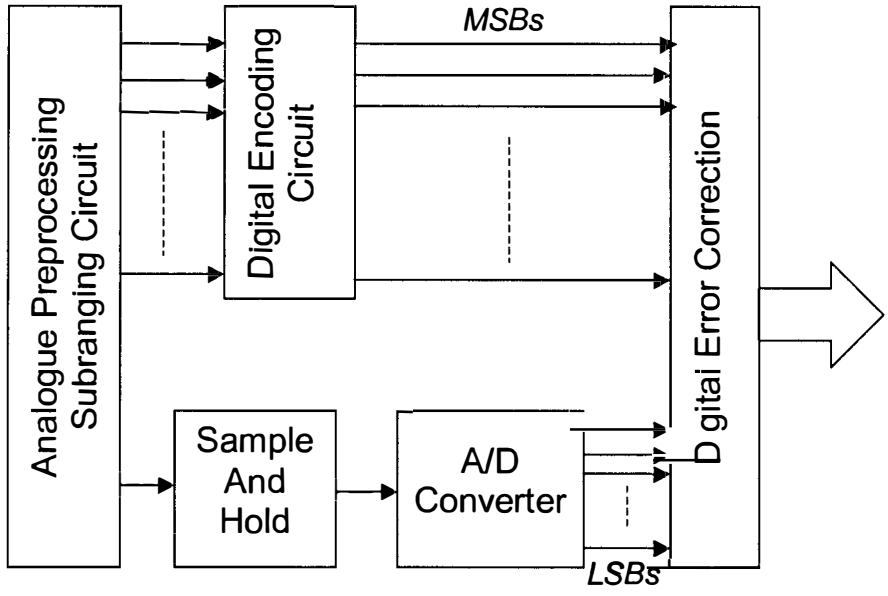


FIGURE 55 SUBRANGING A/D CONVERTER

This implementation achieves 11 bit resolution at 20MHz with a 3-bit analogue preprocessor and 8 bit fine flash A/D converter.

A two-step flash A/D converter using the folding and interpolating method is presented in [21] that achieves 70 megasamples per second. This again uses the concept of 'coarse' and 'fine' conversion stages. The folding is used to convert the input signal into a form that is acceptable to the fine A/D converter. This implementation uses 3-bit coarse and 5-bit fine conversion stages. The folding is achieved by analogue means, but this can introduce nonlinearities in the folded signal. This is addressed, however, by using multiple folding amplifiers with overlapping linear regions.

Cyclic A/D conversion is used in [22] in a manner that does not require ratio-matched components, a factor due to the need for a precision reference element. The configuration appears simple, Figure 56, but each node must be supplied with one of a set of complex control signals. This would be unsuitable for the Smart Pixel as the circuit area required by the comparators and the generation of the control signals locally would occupy too much chip floor area.

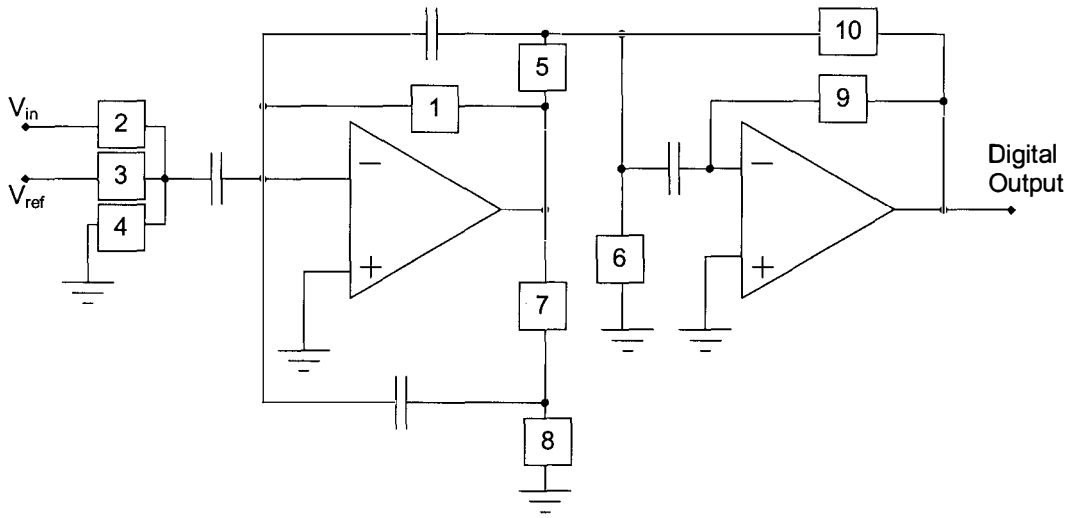


FIGURE 56 CYCLIC A/D CONVERTER

A current mode cyclic A/D conversion is described in [23] which does not require precise analogue or ratio-matched components. 8 bits resolution at 40kHz is achieved in .024mm^2 using a .8μm CMOS process. This equates roughly to 190λ x 190λ.

A 4-bit A/D converter using artificial neural networks has been simulated in [24]. This approach takes a large number of iterations to train the neural network (typically in the order of 10^5 iterations). The complexity of training a large array of such converters in the Smart Pixel may prohibit such an approach.

3.6 νMOS A/D CONVERSION

For an array as large as the Smart Pixel scheme, power dissipation is an important factor. Reducing the number of transistors can also reduce power consumption. By exploiting νMOS technology, a dramatic reduction in the transistor count occurs. Table 3 gives examples of this [12]-

Circuit	Conventional CMOS	νMOS
3-bit A/D	174	16
4-bit A/D	398	28
Full Adder	50	8

TABLE 3 TRANSISTOR COUNT FOR CONVENTIONAL AND IMPROVED νMOS A/D CONVERTERS

Note that, again, this is compared to conventional CMOS transistor counts, not other implementations of non-static CMOS circuits. Shibata and Ohmi [25] present a 3-bit flash analogue to digital converter that uses vMOS gates to provide decoding of the input signal, this is shown in Figure 57. This circuit uses 16 transistors.

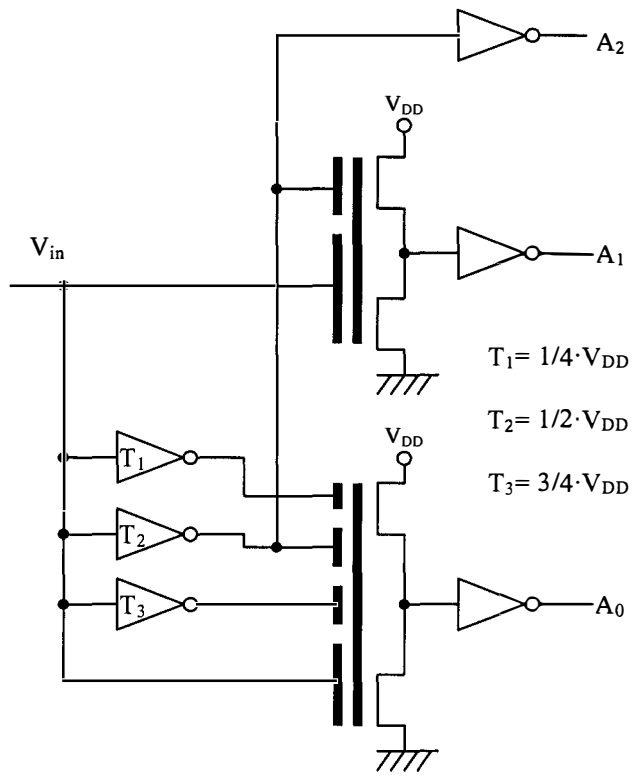


FIGURE 57 SHIBATA AND OHMI'S A/D CONVERTER

Variable threshold inverters (T_1 to T_3) are used to modify the behaviour of the main vMOS transistors in relation to the magnitude of the input signal. These inverters are constructed using a vMOS transistor with additional gates connected to the supply rail (V_{DD}) and/or ground to achieve the desired switching threshold. The operation of these circuit elements is primarily dependent on the ratio of gate sizes. Due to process constraints, a minimum gate size exists for a given technology, thus a minimum overall vMOS variable threshold inverter size. As the number of bits resolution, n, increases for a scheme such as presented in [25], so the size increases, as a $1:2^{n-1}$ ratio is always needed for the vMOS transistor connected to the least significant bit. This limits the density available to an array of such A/D converters in VLSI.

A scheme presented in [3] uses two 3-bit A/D converters to perform a 6-bit operation in a hybrid fashion that exploits νMOS in both digital (inverter mode) and analogue (source-follower mode) configurations. This method partially addresses the logarithmic increase in gate sizes as resolution increases, yet still includes variable threshold inverters, albeit with inversion thresholds near to $V_{DD}/2$ avoiding the need for large input gates.

In another νMOS method Shibata and Ohmi in [26] use a high-frequency clock to achieve capacitive voltage division. For 4-bit conversion the circuit in 3μm CMOS technology occupies 1.4mm x 1.0 mm. Scaling this to technology constrained minimum feature length gives a geometry of approximately 460λ x 330λ.

3.7 CONCLUSIONS

This chapter reviewed the common methods of performing analogue-to-digital conversion. The contemporary methods presented in the literature are also discussed, including a νMOS A/D converter. One of the characteristics of an A/D converter is the silicon area it occupies when implemented in VLSI. The literature generally does not contain size information for many converters. This is due, in part, to the fact that A/D converters are mainly fabricated as a single circuit (or collection of A/D circuits) on a chip.

Chapter 4

Proposed Analogue to Digital Converter

4.1 ALTERNATIVE A/D METHODS

This section presents two novel, alternative, methods of achieving analogue-to-digital conversion using νMOS technology.

4.1.1 Introduction

This section introduces a novel variation of the A/D converter presented in [27]. Circuit schematics, simulation results, and VLSI layout are presented in order to assess the suitability of the circuit for inclusion in the Smart Pixel array.

Two alternative methods of A/D converter are discussed. The first is termed a 'hybrid' A/D converter and is used to illustrate a method of a folding A/D converter. The second is a simpler method that uses intermediate results to progressively resolve the conversion from most significant to least significant bit.

4.1.2 Hybrid A/D Converter

The use of νMOS transistors in a hybrid analogue/digital implementation allows reduced interconnections as well as reduced circuit complexity. The conventional νMOS flash A/D converter uses variable threshold inverters to obtain the output bit pattern [12]. For example the configuration for a 3-bit converter has only 16 transistors. However when the word length increases, the number of inputs to the νMOS transistors increases logarithmically. By using a hybrid A/D and D/A scheme it is possible to maintain low device count.

4.1.2.1 Circuit Description

A hybrid scheme that uses two separate A/D converters and the principle of 'folding' to achieve greater resolution has been described [3]. This is illustrated in Figure 58. The conversion is performed using two 3-bit A/D converters. The first for 'coarse' quantising of the most significant bits, the second for the least significant bits. This 'fine' resolution A/D converter operates in a defined range. The input voltage is shifted near to V_{DD} by analogue addition. The variable threshold inverter is exploited to simplify the partitioning of A/D conversion into 'coarse' and 'fine' operations. A floor function is implemented by quantising the input voltage and then passing this result to a D/A converter, which is achieved by operating the νMOS transistor in source-follower mode [1]. The input to the 'fine' A/D is always within the range $(7/8)\bullet V_{DD}$ to V_{DD}.

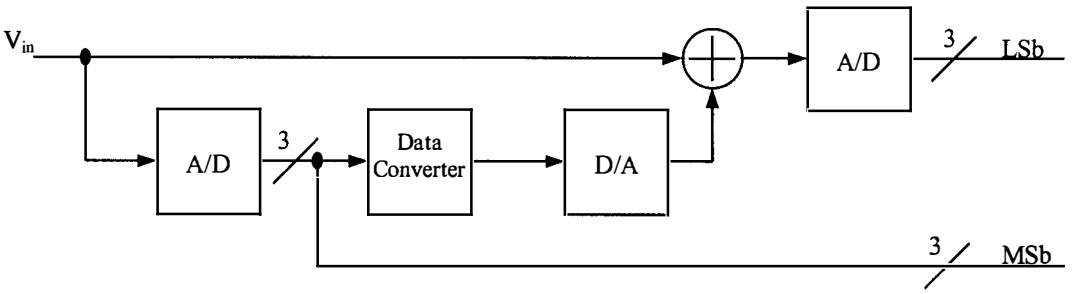


FIGURE 58 SCHEMATIC DIAGRAM OF 6-BIT A/D CONVERTER

The circuit diagram illustrating the concept is shown in Figure 59. $T_1 - T_6$ are variable threshold inverters, implemented also in νMOS technology, each configured to invert equidistantly throughout the coarse range (T_1-T_3) and the fine range (T_4-T_6).

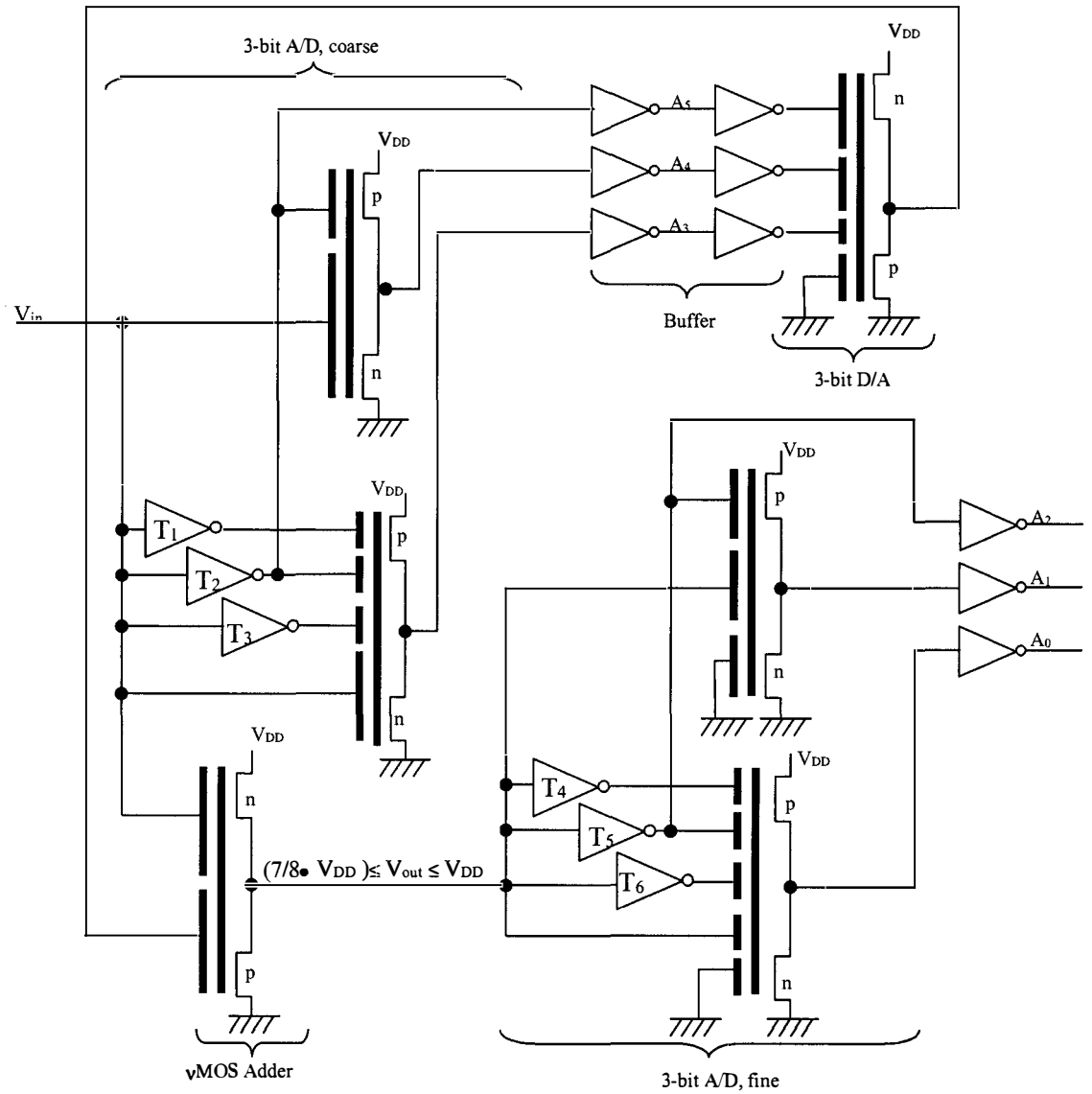


FIGURE 59 6-BIT HYBRID A/D CONVERTER

4.1.2.2 Simulation Results

The circuit in Figure 59 was simulated using HSpice. Simulation results show that the A/D operation is satisfactory for both the fine and coarse sections of the circuit, when considered in isolation. Results also show, however, that the configuration of the νMOS adder is critical to the operation of the fine converter.

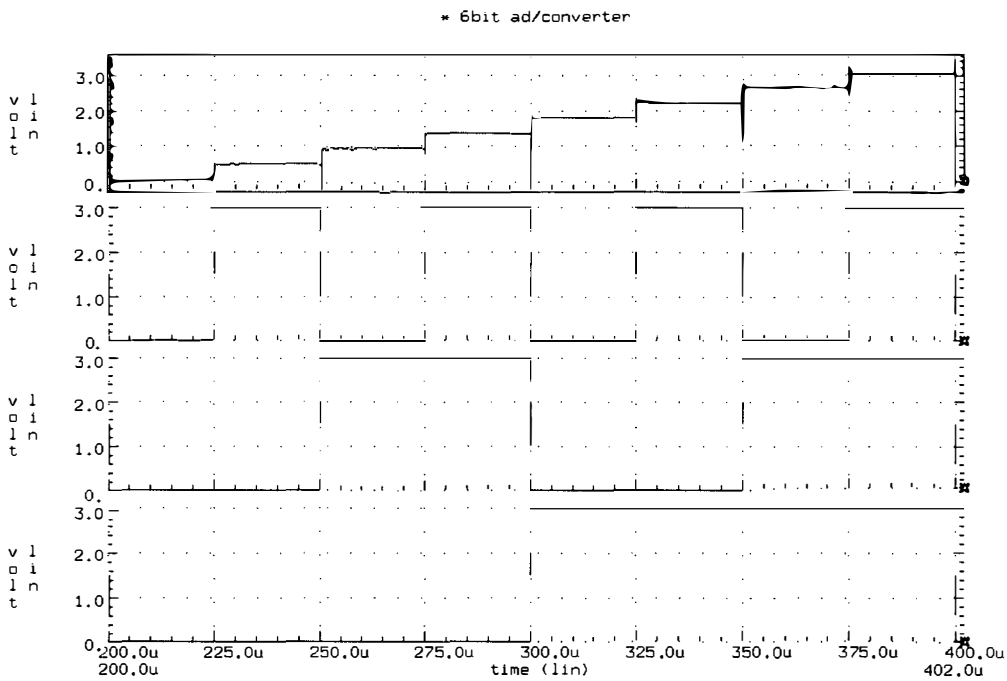


FIGURE 60 D/A CONVERTER OUTPUT

Figure 60 shows the operation of the 3-bit D/A converter section. Output zero-offset may be adjusted as needed by modifying the size of the grounded gate. It was observed that the operation of the A/D converters is aided by reduction of the linear operating regions of the p- and n-type transistors. As the gate potential varies primarily in this region, and its variance is inversely proportional to the number of gate capacitors, a limit to the number of input gates exists due to the reduced noise margin typical of such configurations.

4.1.2.3 Limitations of the Technique

The situation where there is a requirement for a number of variable threshold inverters is not completely addressed. The output drive capability for the D/A converter is limited, and simulation results confirm this by showing incorrect operation once the D/A and fine converters are connected. The conclusion that a simple method of providing sufficient current to drive the fine conversion stage was unavailable obviated the need for an alternative scheme.

4.1.2.4 Application to Smart Pixel Array

The νMOS A/D converter may have its aspect of partitioning the fine and coarse operations exploited to further reduce the component count for a two-dimensional array of image capture elements. The circuit does have merit, however, as part of an array where access to the incident intensity levels of nearby image capture elements are available. Thus, the coarse converter may be shared among a number of elements.

Figure 61 shows how the coarse converter may be shared within a regular block of pixels, which need only devote floor space to the fine operation and associated, localised, multiplexing circuitry. Dedicating the photodetector associated with this coarse converter to a given region may introduce blocking effects. Low spatial frequency errors may be reduced by interpolation.

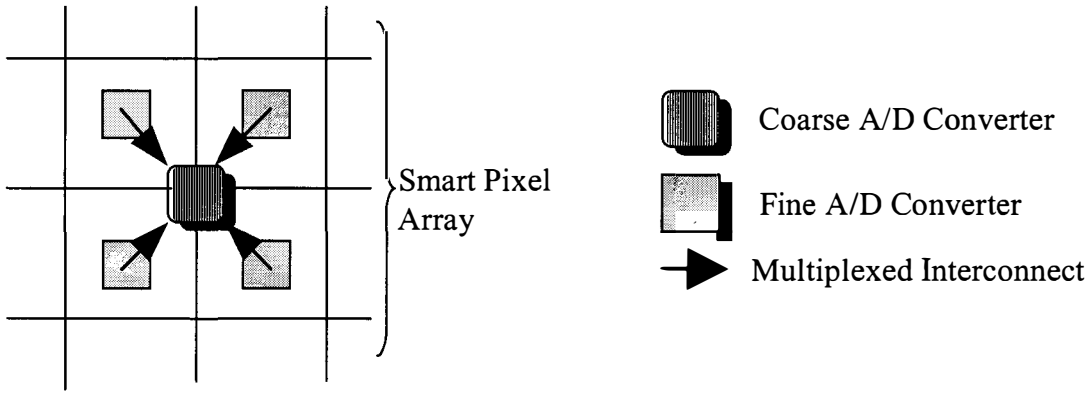


FIGURE 61 MULTIPLEXING COARSE CONVERTER FUNCTION

Note that this method does not address changes in the most significant bit amongst shared pixels.

4.1.3 Improved νMOS A/D Circuit Description

The second circuit operates in a different way to the hybrid A/D converter by resolving the most significant bit (MSB) first and then the lower order bits successively, using the result from higher order bits to determine the lower order ones. This method effectively performs the D/A conversion for every

bit resolved, except that the hybrid technique is modified to exploit the voltage addition that is inherent to the operation of the floating gate.

4.1.3.1 Description of Operation

The result from the highest order bit is then added it to the input quantity using the floating-gate voltage addition function. This function is achieved by using a binary-weighted νMOS inverter. This addition is necessary to shift the value of the input to be nearer to the switching threshold of the inverter. Note that the shift is purely a translation and that scaling is not an intentional feature of the method. Further bits are resolved by the addition of more gates to subsequent νMOS inverters to accommodate the greater number of more significant bits previously resolved. This is represented as a block diagram in Figure 62.

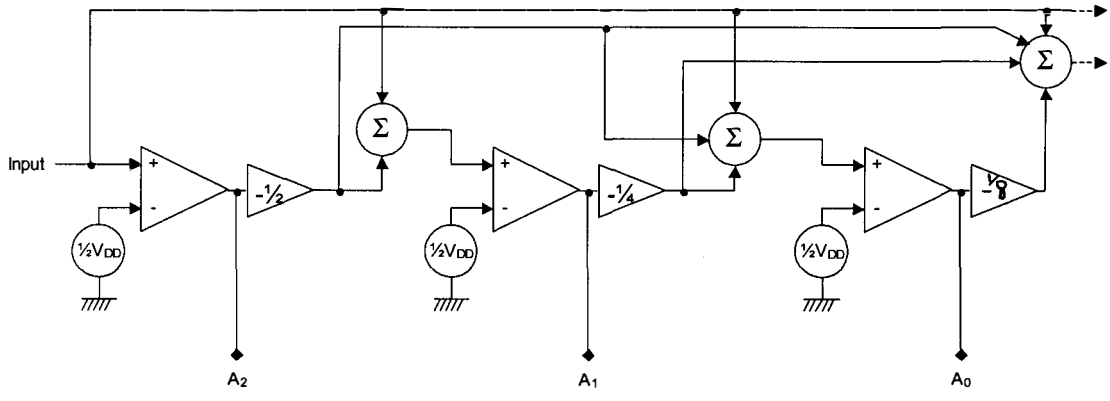


FIGURE 62 REPRESENTATION OF CIRCUIT

As no feedback paths exist a simple transformation affords the diagram as shown in Figure 63. This shows a slightly modified form, in that the scaling factors are not shown as being strictly as they are in the circuit implementation.

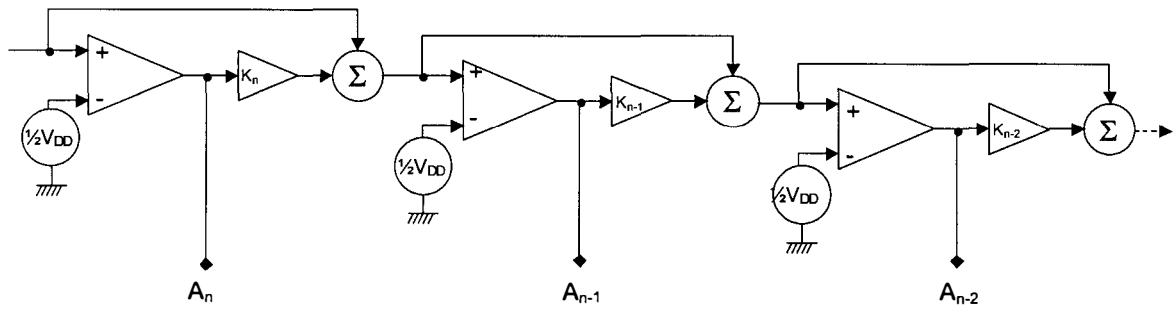


FIGURE 63 SIMPLIFIED REPRESENTATION OF CIRCUIT

This diagram is useful to show that no feedback paths exist, simplifying understanding, and that an individual bit need not be concerned with the existence or otherwise of lower order bits. This is limited by the driving capability of the standard CMOS inverter that is connected to a lower-order floating gate. This arrangement also highlights the need for accuracy of the higher-order bits to reduce the propagation of errors to the lower order bits.

The scheme presented here makes more efficient use of intermediate results than the scheme presented in [3] and [25]. Its operation is based on using the A/D conversion result of a particular bit to modify the operation of all lower-order bits, working to 'fold' the voltage to be near the switching threshold. In other terms, the input voltage is adjusted to be in the conversion range of the A/D converter concerned with the next least significant bit. Hence the variable-threshold inverters are unnecessary. This scheme is shown in Figure 64.

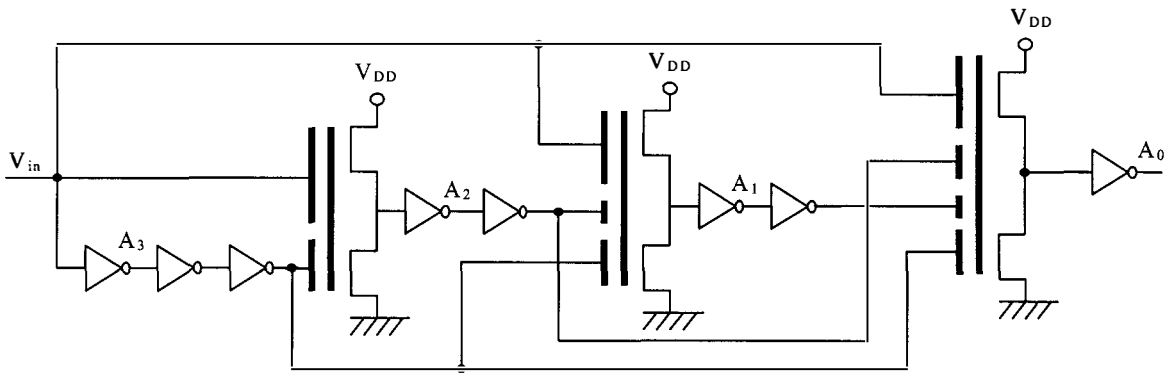


FIGURE 64 PROPOSED IMPROVED A/D SCHEME

The extra inverters between the νMOS transistors are used to improve the shape of the output, effectively reducing the range in which the floating gate inputs are operating in a non-linear region. The νMOS transistor operation in the linear region increases as conversion resolution increases. This is due to the floating gate potential variation becoming more reduced and confined to the inversion threshold. All inverters are configured to have a threshold voltage as close to $V_{DD}/2$ as process parameters allow. Deviation from this value affects monotonicity and linearity. The net effect is to cause erroneous operation for lower order bit conversions.

The four-bit A/D converter in Figure 64 can be extended further to increase resolution, the upper limit of which depends on the ability to achieve accurate switching at precisely $V_{DD}/2$. Simulations suggest that 4-bit resolution is achievable with careful selection of transistor width-to-length ratios.

As the resolution increases the device operates closer to the switching threshold, thus the noise margin becomes of more concern. The technique does not amplify the voltage-translated quantity, and as such the noise margin remains similar to that of a standard inverter with an analogue input quantity near the switching threshold.

4.1.3.2 Classification of Conversion Method

The classification of the device is complicated by the nature of its operation. It is reasonable to describe it as a multi-step folding flash converter. The result of the conversion is dependent on the higher order bit being resolved before the lower order bit. In this way it is somewhat like a successive approximation converter, yet it is also like a flash converter because it requires no control circuit, unlike traditional successive approximation converters. In another way it is like a folding A/D converter, where a partial result is modified to fit within the bounds of another dedicated lower order A/D converter. In this case there are a number of such dedicated converters. Because the number of dedicated A/D converters is equal to the number of bits resolution, the distinction between this converter and normal folding converters is grey.

4.2 NEURON-MOS VLSI IMPLEMENTATION

4.2.1 Introduction

As the aim of the research is to provide a device that may be realised, an evaluation of an implementation is appropriate. VLSI layouts were constructed using the public domain package MAGIC. The basic circuits that were presented in earlier chapters are described again as their VLSI layout counterparts in this section.

4.2.2 neuron-MOS Inverter

To gain an understanding of the layout principles the fundamental νMOS circuit, the νMOS inverter, is shown in Figure 65 and Figure 66 for two test circuits that have different input gate sizes. This is one of the more simple configurations to understand. The configuration of a source-follower is achieved by reversing the power supply connections, V_{DD} and GND.

The different layers that are created during fabrication are shown as coloured regions, as shown in Figure 67.

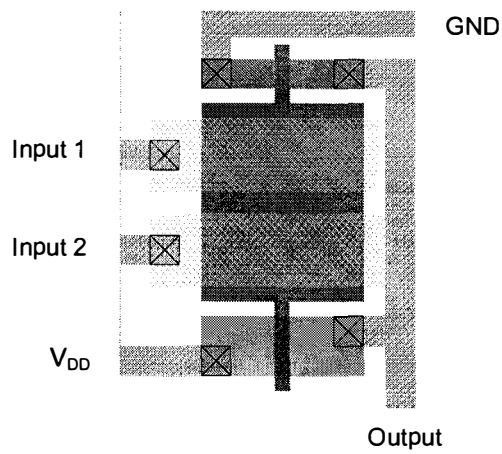


FIGURE 65 NEURON-MOS INVERTER WITH EQUAL GATE SIZES

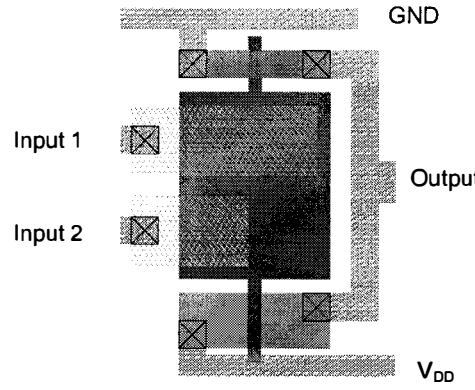


FIGURE 66 νMOS INVERTER WITH UNEQUAL GATE SIZES

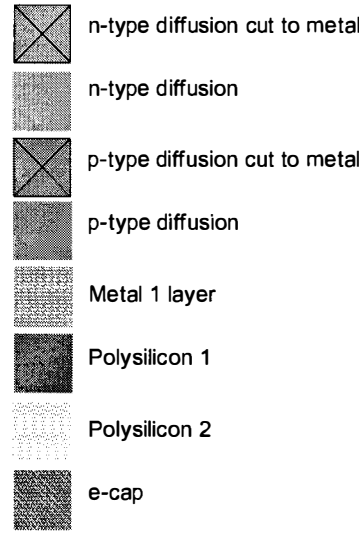


FIGURE 67 LEGEND FOR VLSI LAYER COLOUR CODES

The layer 'e-cap' is the so-called electrode capacitance that is formed when the poly-1 layer is overlaid the poly-2 layer. The stated poly-1/poly2 capacitance is 462aF/μm^2.

4.2.3 6-bit νMOS A/D Converter

The VLSI layout of a 6-bit νMOS A/D is shown in FIGURE 68. Outputs are provided at the perimeter of the device for the 6 bits, A_5 to A_0, which range from the most significant bit (MSB) to the least significant bit (LSB) respectively.

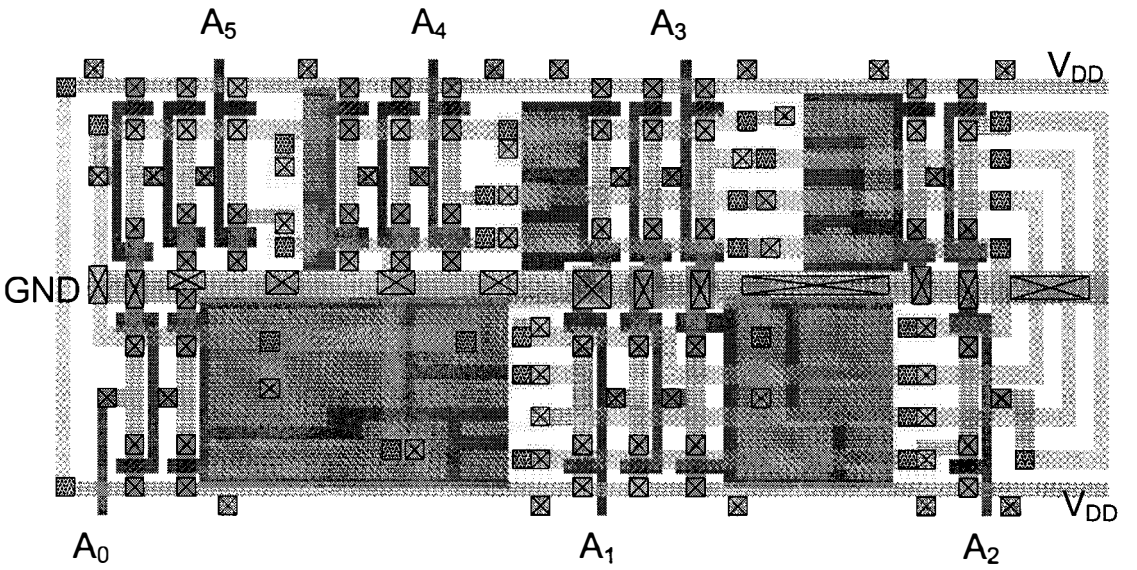


FIGURE 68 VLSI LAYOUT OF 6 BIT A/D CONVERTER

The circuit is ideal for VLSI implementation because of its scalable nature. The rectangular outline and high density provide for efficient area utilisation. The layouts for 4-bit, 5-bit and 6-bit versions are of similar geometry.

The number of transistors for the improved scheme is less per-bit resolution than extensions of the Shibata and Ohmi's method as shown in Table 4.

RESOLUTION (BITS)	SHIBATA & OHMI METHOD	IMPROVED vMOS METHOD
3	16	16
4	28	22
5	48	28
6	84	34

TABLE 4 COMPARISON OF NUMBER OF BITS RESOLUTION VERSUS TRANSISTOR COUNT FOR CONVENTIONAL vMOS METHOD VERSUS IMPROVED vMOS METHOD.

The layout for a 4-bit A/D converter is presented in [27]. This scheme can also be extended linearly in the horizontal direction, at the expense of a small amount of unoccupied chip area.

4.2.4 SPICE Extraction from MAGIC

This section discusses the results of the extraction of the VLSI layout into a SPICE form. This is accomplished by the MAGIC command `:extract` and

the UNIX utility `ext2spice` to produce the SPICE format circuit file (.sp). This is included as Appendix 1.

The most important feature of the layout is the predicted capacitance for the poly1/poly2 capacitors. The file was used to produce the matrix of capacitances shown in Table 5. This shows the size, in femtofarads, of each of the capacitors connected to the gates of each νMOS inverter.

The nomenclature used is that the inverted output of the conversion result is denoted as A_n_inv, where *n* is the bit that is resolved, which is connected to the floating gate of the subordinate bit's νMOS transistor, denoted as A_n_fg, where *n* is the number of the bit that is resolved as a result of the action of the respective νMOS transistor.

	A4_fg	A3_fg	A2_fg	A1_fg	A0_fg
Input	45.1	64.8	108.2	215.7	432.7
A5_inv	22.9	32.7	54.5	107.8	216.2
A4_inv		16.8	27.3	55.6	107.8
A3_inv			14.1	28.6	53.9
A2_inv				14.9	26.9
A1_inv					13.5

TABLE 5 CAPACITOR SIZE MATRIX FOR A/D CONVERTER

The circuit was then modified to scale all dimensions by a factor of two in order to investigate the relationship between scaling and extracted capacitance. This was achieved by doubling all numerical quantities in the MAGIC data file, which represented cartesian coordinates of the differing regions. The SPICE file of the scaled version is shown in Appendix 2. The capacitance table is shown in Table 6.

	A4_fg	A3_fg	A2_fg	A1_fg	A0_fg
Input	180.2	259.3	432.8	862.9	1730.6
A5_inv	91.6	130.9	217.8	431.0	865.0
A4_inv		67.2	109.4	222.2	431.0
A3_inv			56.3	114.5	215.5
A2_inv				59.8	107.8
A1_inv					53.9

TABLE 6 CAPACITOR SIZE MATRIX FOR SCALED VERSION OF A/D CONVERTER

The relative percentage error that occurs between a capacitor size and its lower-order capacitor is shown in Table 7 for the unscaled A/D converter. This was calculated using the formula shown in (33).

$$Error\% = \frac{\left(2 - \frac{C_n}{C_{n-1}}\right)}{2} \cdot 100\% \tag{33}$$

Where C_n is the input gate capacitance of bit n. Thus C_n is expected to be twice the size of C_{n-1}.

	A4_fg	A3_fg	A2_fg	A1_fg	A0_fg
Input	1.5284%	0.9174%	0.7339%	-0.0464%	-0.0694%
A5_inv		2.6786%	0.1832%	3.0576%	-0.2783%
A4_inv			3.1915%	2.7972%	0.0000%
A3_inv				4.0268%	-0.1859%
A2_inv					0.3704%

TABLE 7 RELATIVE ERROR MATRIX FOR CAPACITORS IN A/D CONVERTER

The relative error matrix for the scaled A/D converter is shown in Table 8.

	A4_fg	A3_fg	A2_fg	A1_fg	A0_fg
Input	1.6376%	0.9549%	0.6428%	-0.1044%	-0.0347%
A5_inv		2.6042%	0.4570%	3.0153%	-0.3480%
A4_inv			2.8419%	2.9694%	0.0000%
A3_inv				4.2642%	0.0464%
A2_inv					0.0000%

TABLE 8 RELATIVE ERROR MATRIX FOR CAPACITORS IN SCALED A/D CONVERTER

Note that the errors are similar, but not equal for the original and scaled versions. This section has showed that the area of a capacitor constructed in a VLSI layout is similar to expected values, based on relative sizing (i.e. number of squares), but fine adjustment of the VLSI layout is necessary in order to reduce small variations.

The technology used was a 2μm Supertex (formerly Orbit), double-poly two metal process. The modification of the extracted capacitances assisted in improvement of the operation under simulation of the device, in particular the

least significant bit, the final values are included in the appendix, as the VLSI layout can be adjusted to achieve the same result. The area of the A/D converter in Figure 68 is 85λ x 225λ, which translates to 85μm x 225 μm for the chosen technology.

4.3 SIMULATION RESULTS

This section gives details of simulations that were conducted using HSPICE. The extracted SPICE file was used, but with modifications made to a small number of capacitors that formed inputs to the floating gates of the least significant bits. The output of the device was examined for a ramp-input function ranging from zero to three volts over 100μs. The duration of 100μs was chosen as it approached the fastest conversion rate that could be achieved reliably.

4.3.1 Analyses of Individual Bit Outputs

For the purposes of generating diagrams that may compare the actual response to the ideal a pulse source was configured for each bit as a standalone element. This voltage source was chosen to reflect the expected response of an ideal A/D converter.

In each of the diagrams in this section the ramp function is superimposed over two traces – the output of the A/D converter for a particular bit, and also the 'ideal' output waveform. The output trace is indicated by a bold trace and the ideal A/D converter is included on the same plot as a thin trace.

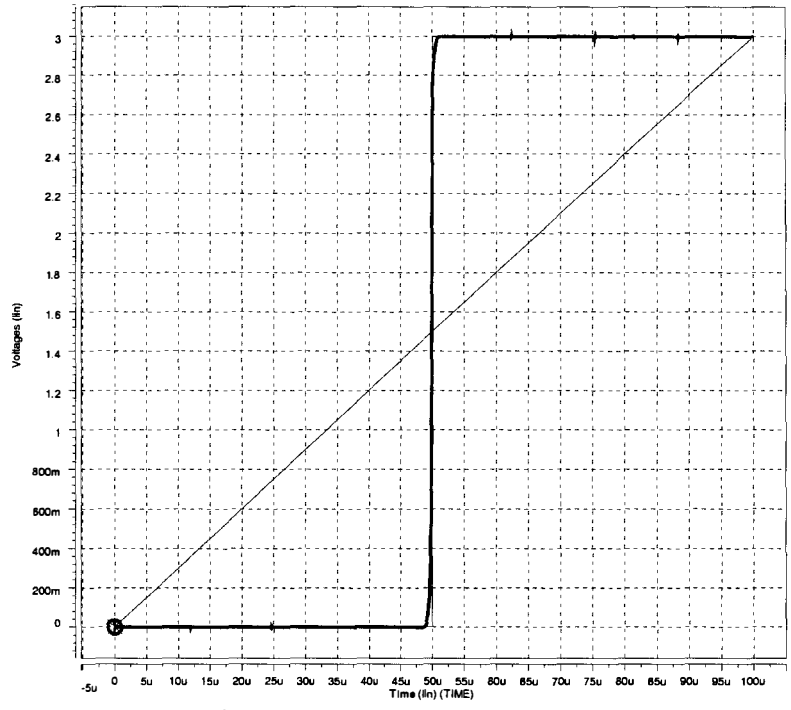


FIGURE 69 OUTPUT OF BIT 5 OF A/D CONVERTER

Figure 69 shows the output of the most significant bit of the A/D, denoted as bit 5 (of bits 5 through 0 inclusive). There exists a small 'error' in the operation of the device, which is small. It is due to the switching threshold not being precisely $V_{DD}/2$. Adjusting the transistor length to width ratio of both the n-fet and the p-fet controls the switching point. In this case the W/L of the p-fet was 6:3 and the n-fet was 4:2. Manufacturing variations also affect this figure, so that even if the precise switching threshold could be chosen then the variation in the switching point makes such a method unreliable. Because the area devoted to the circuit is of major importance, a complex dynamic adjustment method is not considered. Instead, the results are presented in a refined but static configuration. The most significant bit differs from the lower order bits in that it does not use a floating gate, but is a standard CMOS inverter. Nevertheless, the chosen width-to-length ratios afford a switching point very close to $V_{DD}/2$ (within 0.01V).

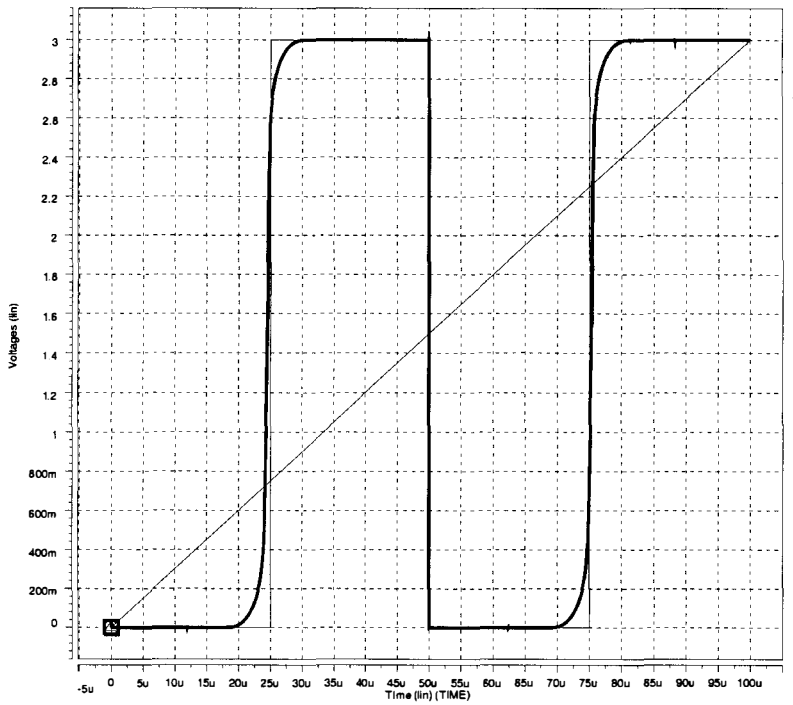


FIGURE 70 OUTPUT OF BIT 4 OF A/D CONVERTER

Figure 70 shows the output for the highest order bit that uses a νMOS transistor, bit 4. The switching threshold is also adjusted by selection of the width to length ratios of the CMOS transistor pair attached to the floating gate. All transistors use the same width-to-length ratios as that for the most significant bit.

For the purpose of the simulation, the floating gate potential needs to be initialised to a value of around 0.5V. The cumulative error that propagates through to the lower order bits is seen in these plots, where the highest order bit introduces an error that may not be removed as more bits are resolved.

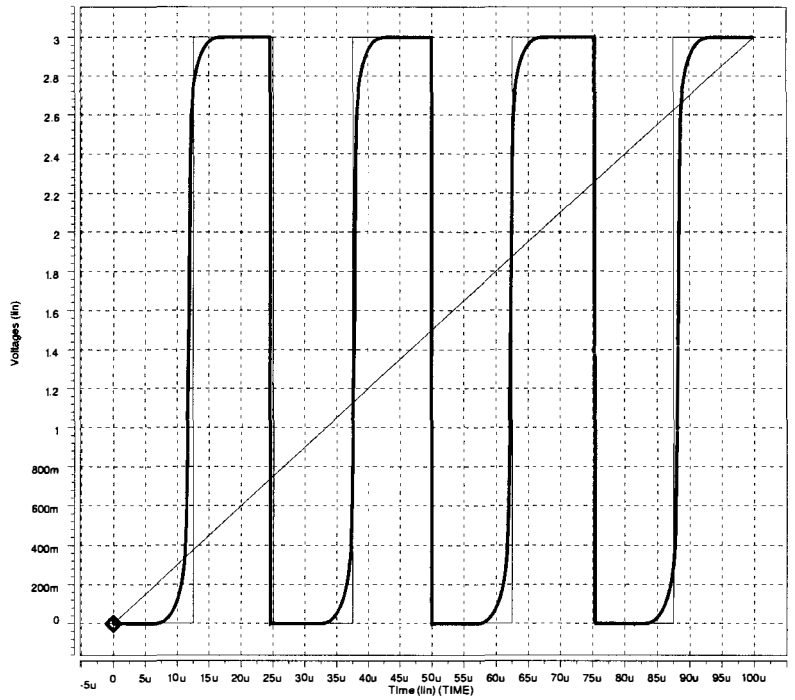


FIGURE 71 OUTPUT OF BIT 3 OF A/D CONVERTER

Figure 71, the plot for bit 3, shows some errors being introduced that affect linearity. Each bit, when considered in isolation, is capable only of showing its contribution to the overall circuit non-linearity. The combination of bits to form the output word is needed to show lack of monotonicity.

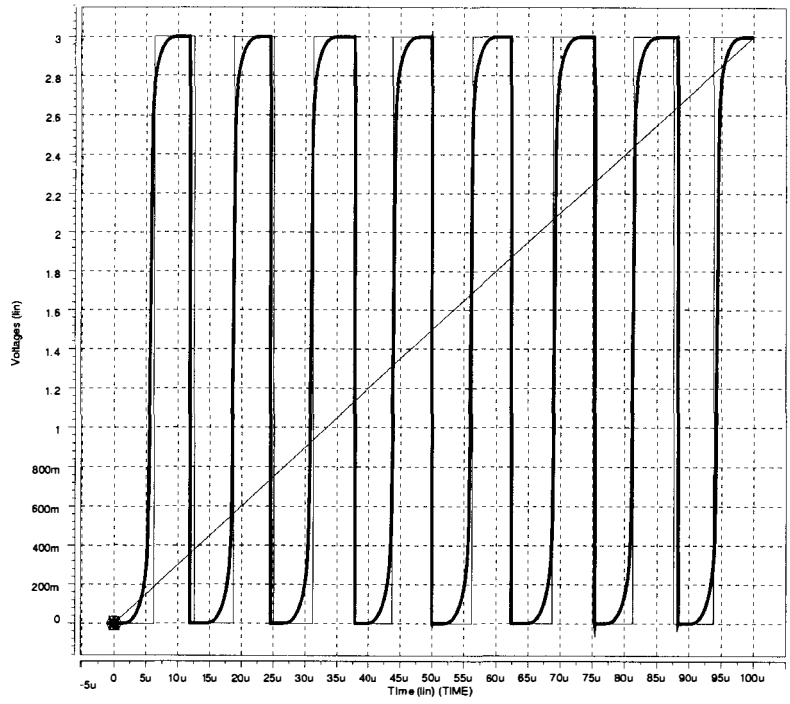


FIGURE 72 OUTPUT OF BIT 2 OF A/D CONVERTER

Figure 72 represents bit 2. At this stage, the output does not show great non-linearity, but the effects of the errors in the higher order bits are becoming more evident.

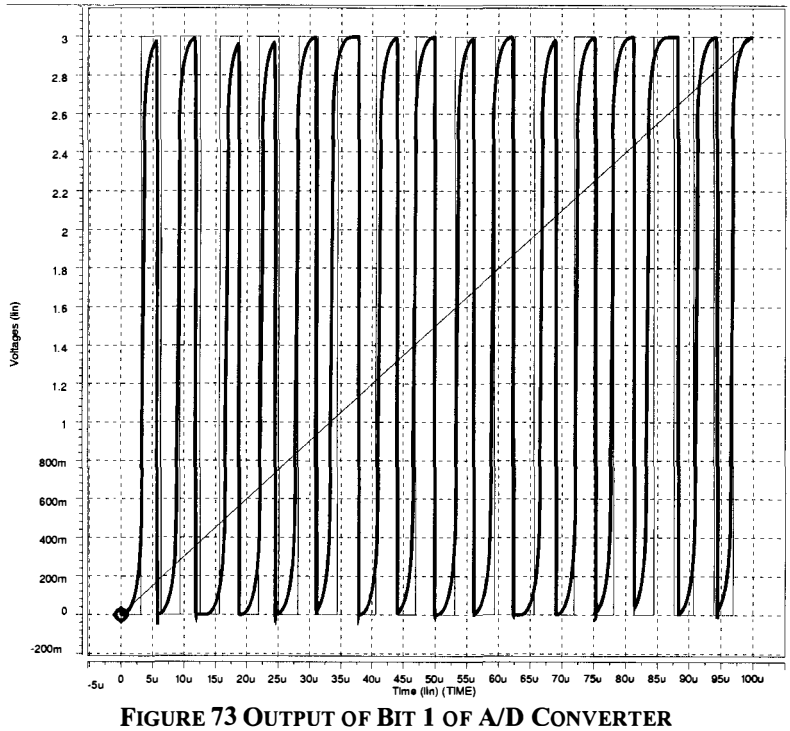


FIGURE 73 OUTPUT OF BIT 1 OF A/D CONVERTER

Bit 1 is shown in Figure 73. Increasing evidence of nonlinearity is shown; however, switching still occurs for all expected codes.

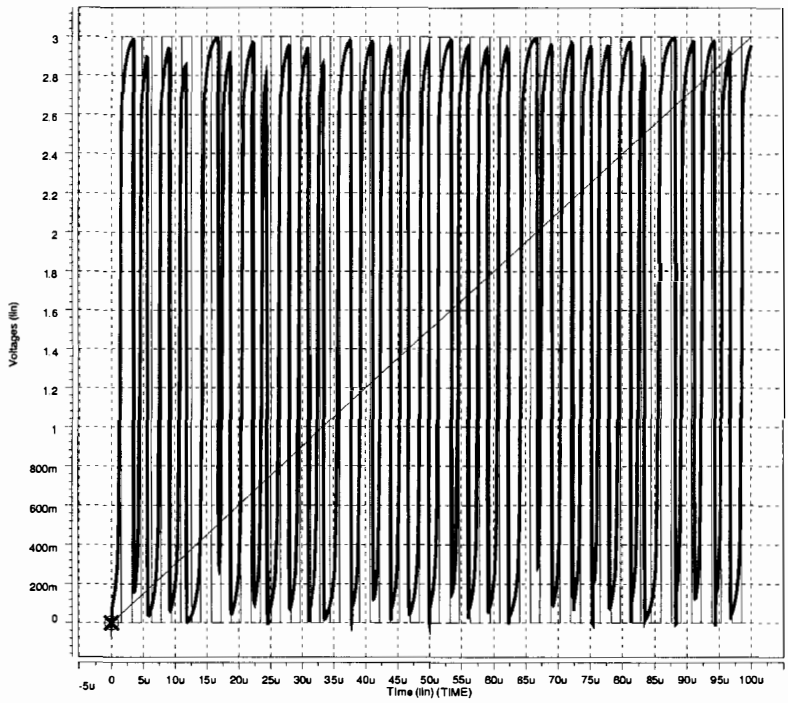


FIGURE 74 OUTPUT OF BIT 0 OF A/D CONVERTER

Figure 74, shows the least significant bit. At this point, the non-linearity introduced by the switching threshold error must not exceed the voltage difference for that bit to switch. The error cannot exceed $V_{DD}/2^{-n}$ volts otherwise the code will not occur. The plot shows evidence of incomplete switching. Errors propagate through to the lower order bits, and thus the limit for this the device in its current configuration has been approached.

4.3.2 Analysis of Floating Gate Operation

This section discusses the operation of the floating gates, which assists in the understanding of some of the inherent problems associated with the technique used. Figure 75 shows the potentials existing on each of the floating gates of the four most significant bits for the vMOS transistors. The amplitude variation can be seen to diminish as the significance of the bit decreases. This is due to the increase in the number of input gates, and the operation of the converter dictates that the potential shall be kept near to the switching threshold. The least significant bits are omitted from this plot for clarity, but are shown in Figure 76.

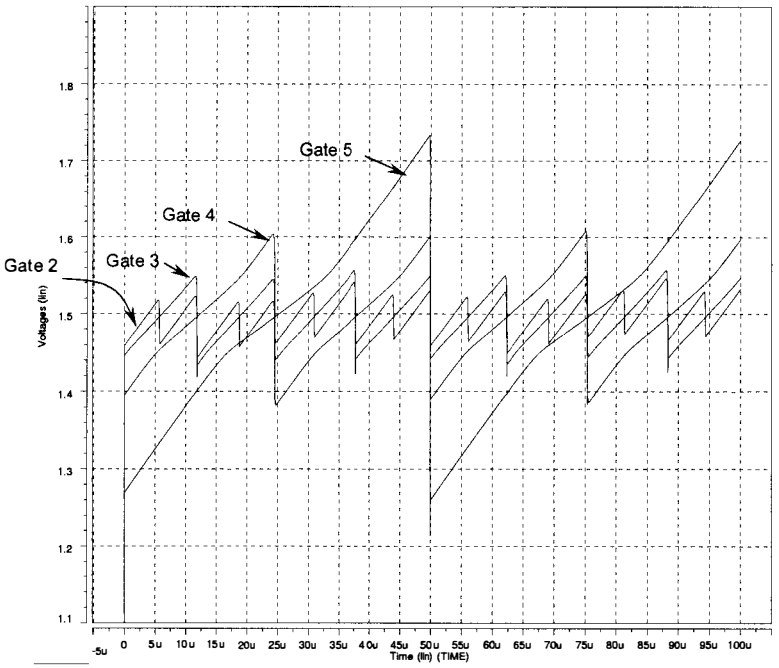


FIGURE 75 POTENTIALS OF FLOATING GATES 2,3,4 AND 5

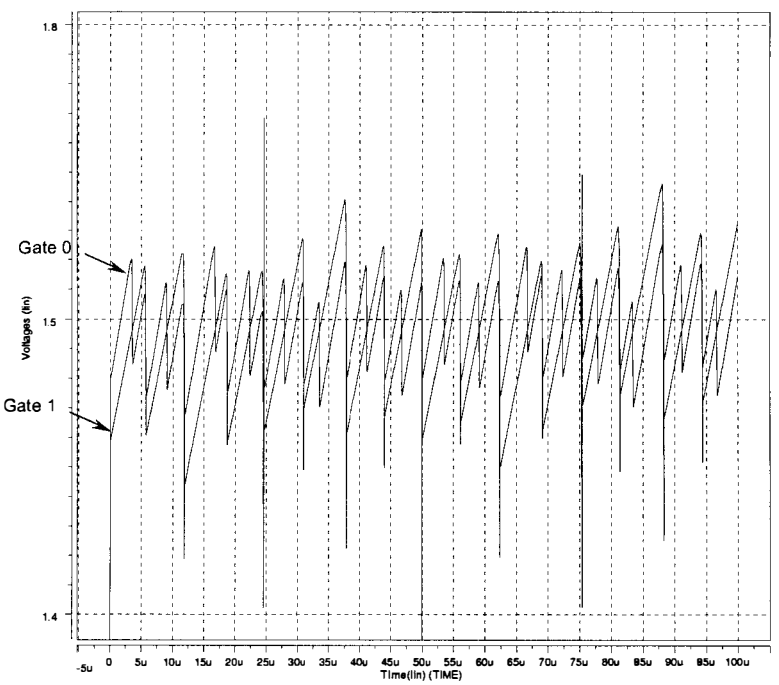


FIGURE 76 POTENTIALS OF FLOATING GATES 0 AND 1

Potentials that do not span the non-linear region of the νMOS inverter's switching region do not effect complete switching. This is generally not a problem if the resulting output spans a standard CMOS inverter's switching region, but the susceptibility to noise is increased if using such a method is necessary for correct operation.

4.3.3 Power Consumption

The current drawn from the single power supply is plotted in Figure 77. The power, which was computed by multiplying the current drawn by the supply voltage of three volts, is shown in Figure 78. The plots show a somewhat steady current draw, but with 'spikes' of current where switching activity in the nonlinear regions occurs.

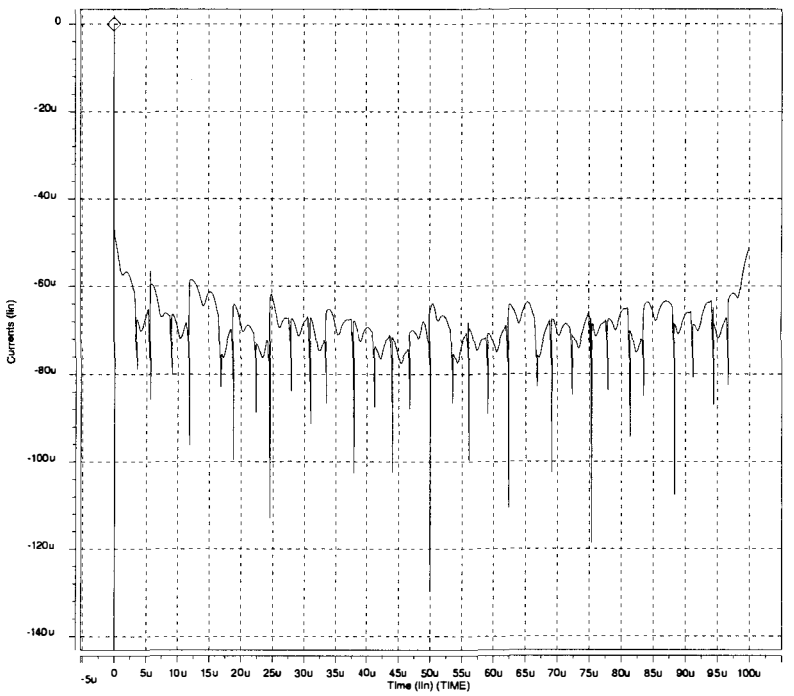


FIGURE 77 CURRENT DRAWN BY POWER SUPPLY

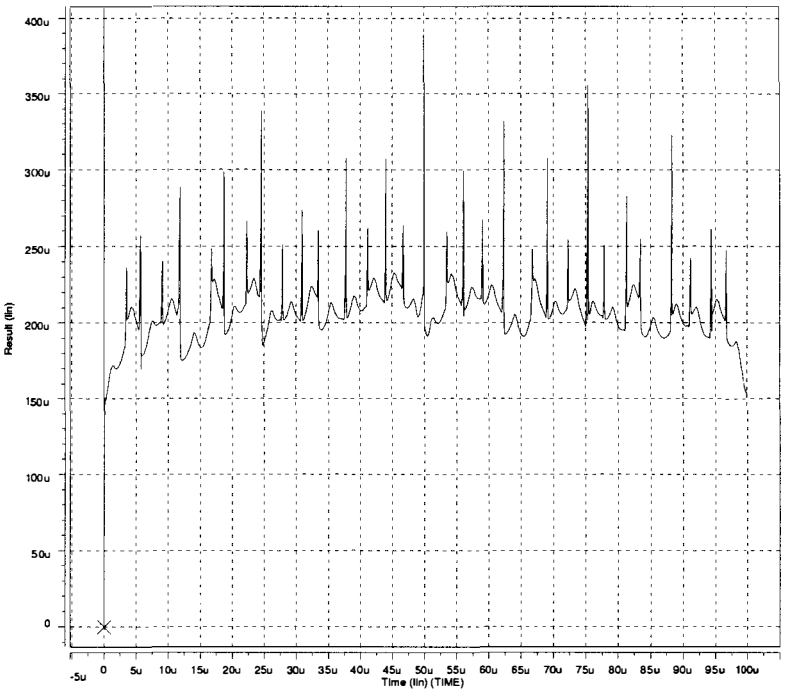


FIGURE 78 POWER DRAWN BY CIRCUIT

4.3.4 Analysis of Output Word

This section analyses the output of the A/D converter in terms of the overall A/D conversion. The individual bits are collected into the output word, which is computed by (34),

$$y = \sum_{0}^{n} b_n \cdot 2^n \tag{34}$$

where b_n is the binary value of the n^{th} bit, which is *1* if the output bit exceeds a threshold value, or *0* otherwise. The threshold was assumed to be $V_{DD}/2$ for the purposes of the generation of Figure 79 and Figure 80, the ideal and the simulated outputs. The ideal bit outputs are formed using the pulse voltage sources.

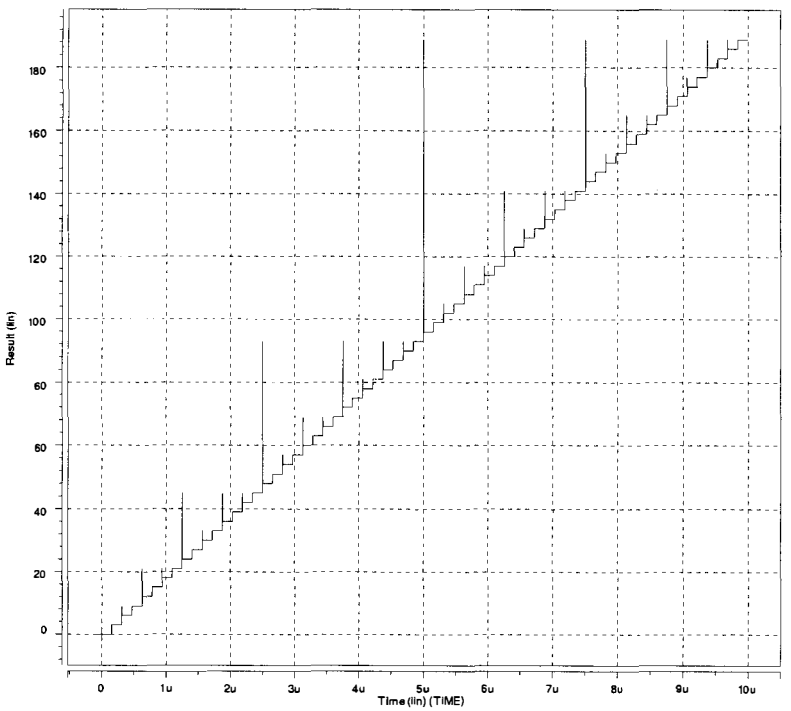


FIGURE 79 NUMERICAL OUTPUT OF 'IDEAL' 6-BIT A/D CONVERTER FOR RAMP INPUT

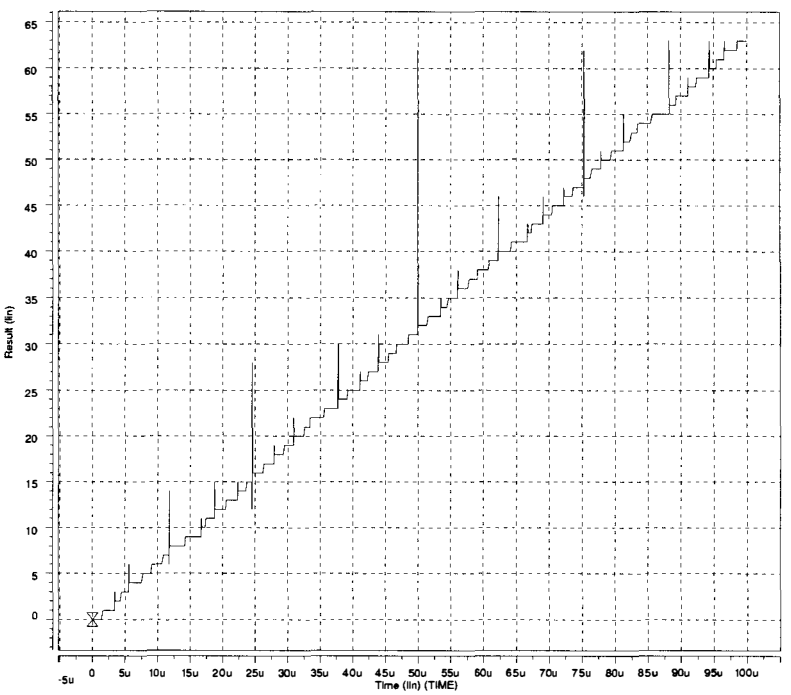


FIGURE 80 NUMERICAL OUTPUT OF VMOS 6-BIT A/D CONVERTER FOR RAMP INPUT

A notable feature of this plot is the existence of 'spikes' which are due to the incorrect switching of the higher order bits. The fact that the errors are all positive indicates only that the higher-order bits switch lower than the lower order bits.

The error is plotted in the graph of Figure 81 was calculated by subtracting the ideal output trace from the actual output trace. The absolute value of this error is shown in Figure 82. The narrow, negative spikes are due to the errors present in the 'ideal' output characteristic. These errors occur when a zero-rise-time pulse is interpreted by SPICE as having a plotted rise time of one data point, as the data points cannot have two values simultaneously.

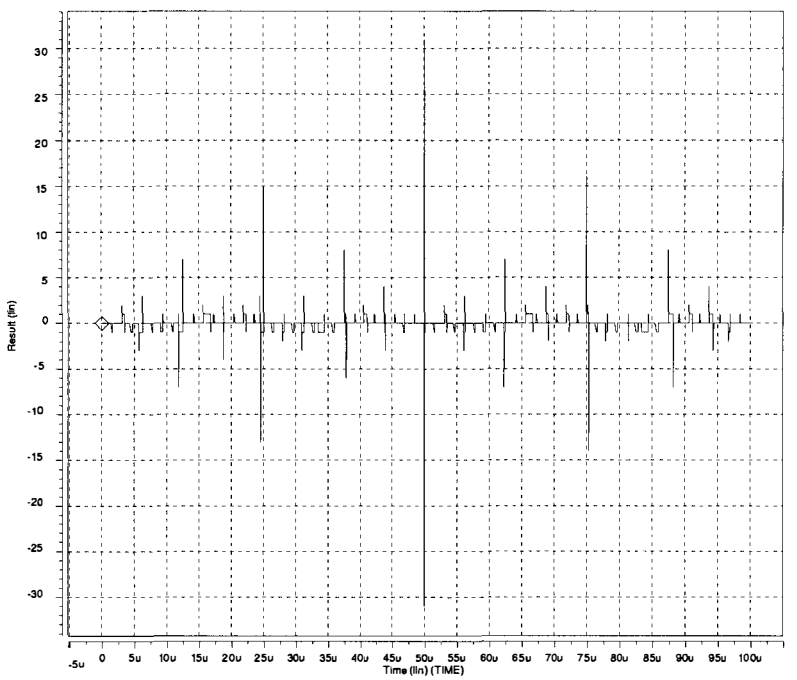


FIGURE 81 ERROR OF NUMERICAL OUTPUT FOR VMOS A/D CONVERTER

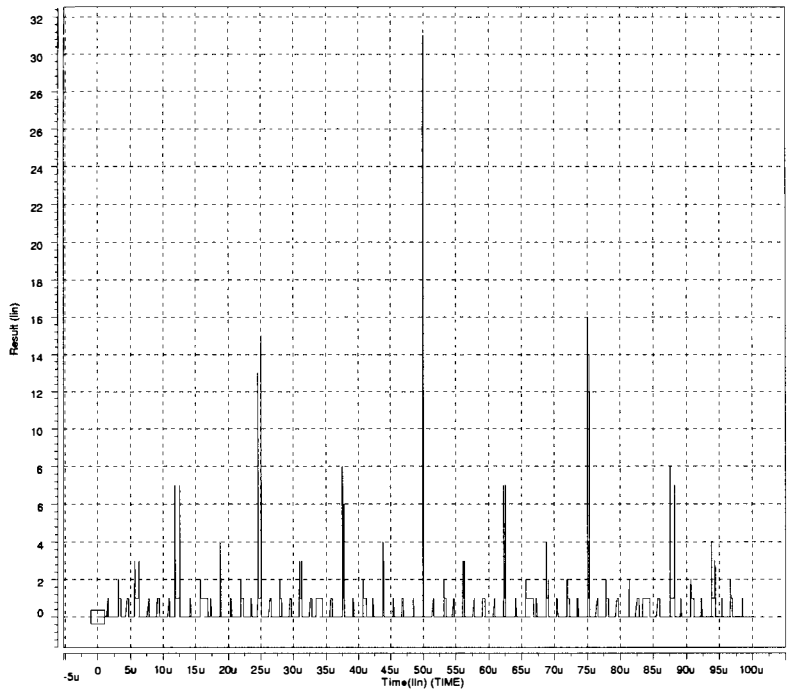


FIGURE 82 ABSOLUTE NUMERICAL ERROR FOR VMOS A/D CONVERTER

4.3.5 Standard Performance Specifications

This section characterises the device in terms of standard performance specifications for A/D converters. These are derived from a previous chapter relating to the issue.

4.3.5.1 Resolution

The resolution is six bits. The fact that not all codes are present in the least significant bit is irrelevant. Only the presence of the outputs affects this specification.

4.3.5.2 Quantising Error

The quantising error of any 6-bit A/D is half of the least significant bit, which is 20 $\log_{10}$ (0.5/64) = -42.14dB.

4.3.5.3 Scale Error

The device achieves full scale output for a full-scale input, as shown in Figure 80. Thus there is no scale error.

4.3.5.4 Offset Error

All inputs are at zero when the input is at zero and the input rises once the missing codes are exceeded, thus the offset error is 0% of full scale.

4.3.5.5 Hysteresis Error

Through simulations the completely static operation of the device was observed, and thus there was no noticeable hysteresis error.

4.3.5.6 Linearity

This is difficult to quantify for this device, as large, highly localised, errors occur. An appropriate measurement of linearity for this device is not immediately apparent.

4.3.5.7 Monotonicity

The device is not monotonic. This parameter is not specified as a quantity but as a quality of the converter.

4.3.5.8 Conversion Rate

The quantification of this parameter is highly subjective. It is erroneous to apply a square wave of increasing frequency to this device, as this is not representative of the correct operation of the device. The device can consistently and repeatedly convert a ramp function with slew rate of 3V/10μs, with some performance degradation evident above this rate. Thus the conversion rate is at least the inverse of this period, which is 100kHz.

4.3.5.9 Output Drive Capability

The device uses standard CMOS inverters to drive the outputs. The floating-gate inputs are buffered by a separate standard CMOS inverter, thus the drive capability is that of a standard CMOS inverter.

4.3.6 Implementation-Specific Analysis

The application is for quantisation of a sequence of time-varying images that is subject to human perception. The performance specifications traditionally applied to A/D converters may not be totally representative of the perceived effects on a captured image.

The absolute error was integrated to find the total error for the device. This plot is shown in Figure 83. The maximum value approximates the total error over the device for the entire input range.

The integration is performed by a summation, as shown in (35),

$$E = \frac{t}{n} \cdot \sum_{i=1}^{n} y_i \tag{35}$$

where t is the total time, n is the number of data points and y_i is the i^{th} absolute error amplitude.

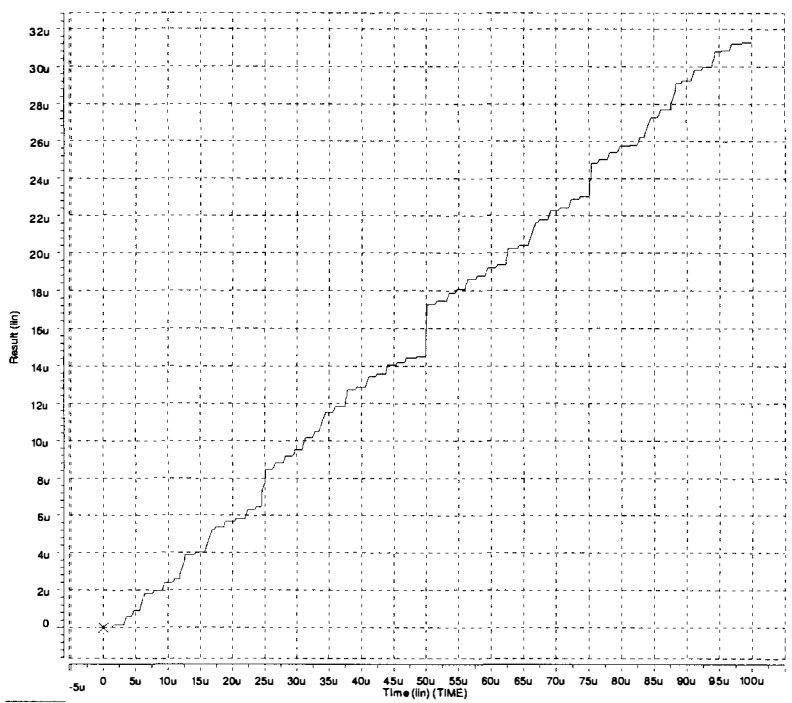


FIGURE 83 INTEGRATION OF ABSOLUTE NUMERICAL ERROR

From the plot, the value of the integration is 31.2×10^{-6}. Normalising the time to one period by dividing the result by 100×10^{-6}, gives an average error of 0.312. The maximum amplitude is 64, thus the percentage error is 0.312/64 = .49%. In decibels this is $20 \log_{10}(0.312/64) = -46.24$dB. This is an additional error that is superimposed on the quantising error which is $20\log_{10}($ ½*(1/64)/64) = 42.14dB. The peak error of the device is considerably greater due to the non-monotonicity introducing 'speckles' in the picture.

4.4 CONCLUSIONS

This chapter demonstrated through simulation of an extraction of a VLSI layout the operation of a novel 6-bit A/D converter. The input was subjected to a full-scale sweep over 100µs where the operation was verified for all 6 bits. The circuit also works successfully at increasing the speed tenfold, with a ramp period of 10µs, yielded correct operation for all but the least significant bit. The transfer characteristic of the device was plotted.

Chapter 5

Image Enhancement Operations

5.1 INTRODUCTION

Lateral inhibition is a biological mechanism whereby neighbouring cells exert mutual antagonistic interactions. In vision, this antagonistic mechanism results in sharpening of contrast and edge enhancement. Here the implementations of both one-dimensional and two-dimensional arrays of laterally inhibited neurons are described and simulation results demonstrating contrast and edge enhancement are presented. This research develops a novel asynchronous implementation of lateral inhibition using Neuron-MOS (νMOS) technology

For real time image processing, it would be more convenient if some simple operations such as contrast and edge enhancement are performed locally at the pixel level. This would improve the image quality, and using CMOS based technologies the cost and power dissipation of imaging devices would be reduced. Lateral inhibition is well suited for focal plane operations. It provides edge and contrast enhancement and is based on the principle of local interactions, where adjacent cells interact with one another to suppress each other's response to incoming light intensity. The lateral inhibition operation may be performed using FETs operating in the linear region, but these techniques often draw large amounts of static current [28]. The source-follower configuration of νMOS may be employed to implement a lateral inhibition circuit for edge enhancement and edge detection.

Because the technique is relevant to the Smart Pixel project, simulations of enhancement operation on images that are of typical size for the application are conducted to provide a subjective appraisal of the method.

5.2 LATERAL INHIBITION

Lateral inhibition plays an important role in the processing of sensory information by the visual systems of animals. The studies of Hartline and Ratliff in the 1950's revealed that inhibitory interactions are exerted mutually among neighbouring ommatidia in the lateral eye of Limulus. Hartline and Ratliff described the phenomenon by a system of linear equations, once a threshold had been reached [29]. For nearest neighbour interactions the Hartline-Ratliff equation is given by

$$e_i = a \cdot I_i - K\left(f(I_{i-1}) - V_{th}\right) - K\left(f(I_{i+1}) - V_{th}\right) \tag{36}$$

where I_i is the input to the i^{th} cell, e_i is the output of the cell, a is a positive constant, V_{th} is the threshold voltage and K is a positive constant, called the inhibition factor. This provides nearest-neighbour interaction.

5.2.1 Relationship to Shunting Inhibition

Shunting inhibition is used to compress the range of input values into a smaller range, aiding in post-processing, either in the brain for the biological eye, or for computation using an electronic eye.

The process of lateral inhibition may be adapted to shunting inhibition, where the output of a pixel is modified not only by its neighbours' outputs, but its resultant value. This gives rise to a differential equation of the form [30]

$$\frac{de_i}{dt} = I_i - b \cdot e_i - k \cdot e_i \cdot (e_{i-1} + e_{i+1}) \tag{37}$$

where for cell I, e_i is the output, I_i is the input, b is the decay factor and k is the inhibition factor. Shunting inhibition may be achieved to a functionally similar circuit to lateral inhibition, and is dealt with later in this section.

5.2.2 Description of Operation

Figure 84 shows the effect of lateral inhibition on a one-dimensional input signal, where the horizontal axis represents the pixels arranged linearly. The amplitude of the output of a given pixel is dependent not only upon its own incident amplitude, but also on the input values of adjacent pixels.

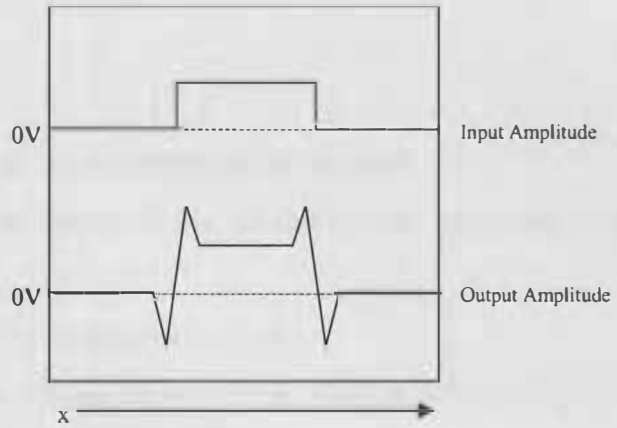


FIGURE 84 INPUT/OUTPUT CHARACTERISTIC FOR A LINEAR ARRAY OF DETECTORS

Figure 85 shows the effect of LI on a simple grey scale image. It is clear the boundary of the lighter region at the centre is enhanced.

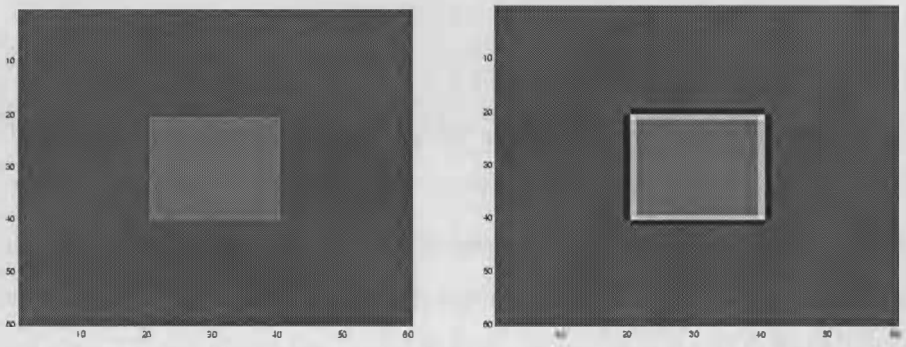


FIGURE 85 ORIGINAL (LEFT) AND ENHANCED (RIGHT) GREY-SCALE IMAGE

5.2.3 LI Operation in Parallel

Computational methods may be employed outside of the sensor array or the operation can be performed in parallel on a per-element basis. The operation is well suited to the second method as the interactions do not need to extend past the neighbouring pixels. The parallel operation can also be implemented using synchronous or asynchronous techniques. The method presented here is asynchronous. Good results can be obtained by using the intensities of the adjacent pixels as modifiers of the output of the pixel in question, giving a first-order equation-

$$V_{out} = a \cdot V_i + K \cdot (2 \cdot V_{th} - V_{i-1} - V_{i+1}) \quad (38)$$

Where

- V_{out} is the output amplitude of the pixel
- V_i is the output of the photodetection subcircuit, in the range of $[0,V_{th}]$
- V_{th} is the maximum amplitude
- *a* is the scaling factor for the photodetection subcircuit, realised in hardware by modifying the capacitance of the νMOS adder input gate.
- K is the scaling factor for adjacent pixels, also dependent upon gate capacitances of the νMOS adder

5.2.4 Configuration of Interactions

The operation may be performed by treating the image as an array of discrete spatial units (i.e. pixels). Two mechanisms may be used. The first, linear lateral inhibition, uses the scaled quantities of neighbouring pixel inputs, as well as its own input, to determine an output value. The second, shunting inhibition, uses both the neighbouring pixel inputs *and* their outputs. For simple linear lateral inhibition the diagram as in Figure 86. For the one-dimensional case the functional diagram of shunting inhibition is shown in Figure 87, which has feedback added from adjacent pixel outputs. The quantities are related to those in (36).

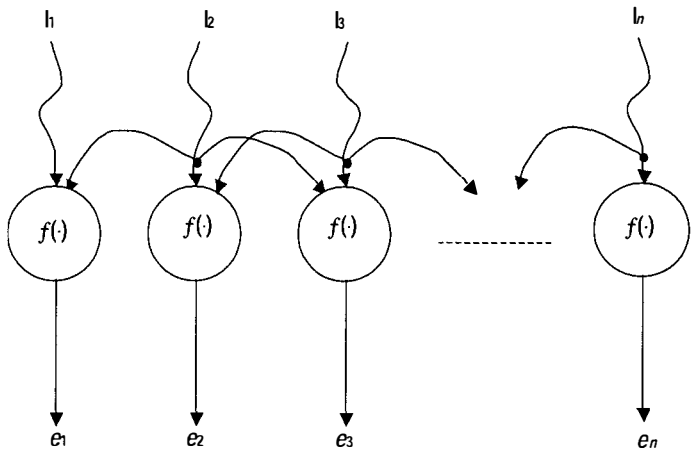


FIGURE 86 LINEAR LATERAL INHIBITION CONFIGURATION

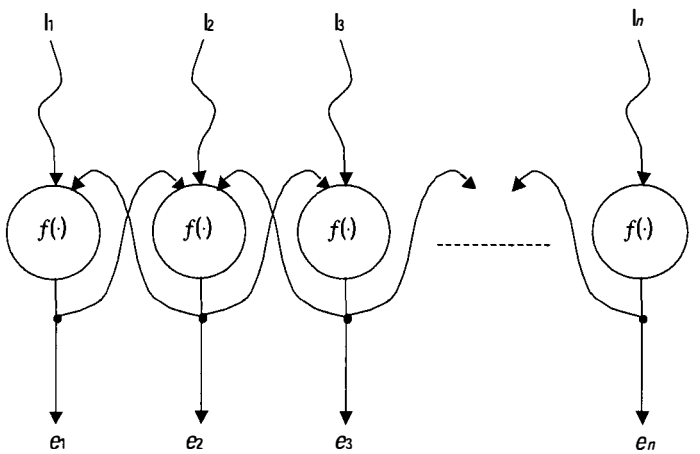


FIGURE 87 SHUNTING INHIBITION CONFIGURATION

5.2.5 Contemporary Hardware Implementations

The implementation of the operation digitally may be performed using an iterative method. In order to reduce the complexity of the control circuit, an analogue solution can be used. This reduction is based on the local interaction between the pixels in a large array. For a digital solution, the method may involve the complete readout of the pixel intensities, then applying repeated iterations until a threshold is reached. Although this is effective, the solution does not lend itself to the Smart Pixel array, which is concerned with a number of control-intensive operations such as filtering and transformation. Thus the area devoted to edge enhancement must be minimised as a major consideration in choosing a design.

A current-mode one-dimensional implementation by Nilson is shown in Figure 88 [31].

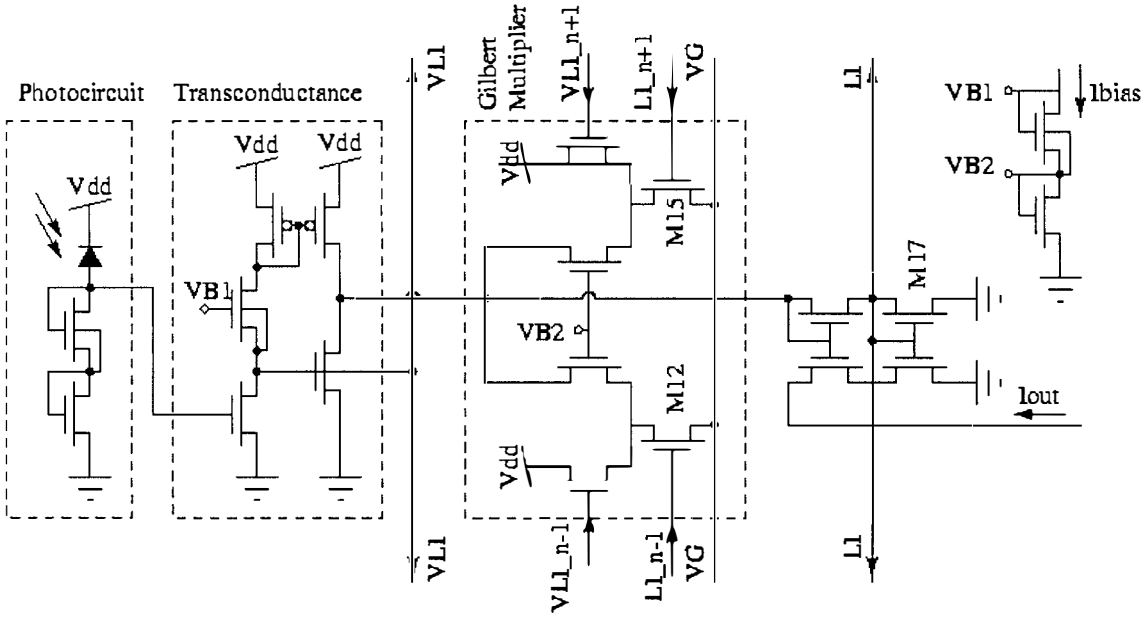


FIGURE 88 NILSON(ET AL)'S SHUNTING INHIBITION CIRCUIT

The circuit uses a four-quadrant Gilbert multiplier, and weighting adjustment is static, achieved by adjustment of the sizes of transistors M_{12} and M_{15}. Some dynamic weighting control may be made by varying the voltage V_G.

5.3 PROPOSED HARDWARE IMPLEMENTATION

This section proposes hardware implementations for one- and two-dimensional arrays of shunting-inhibition pixels. The inputs to the circuit elements are photodetectors that are buffered and scaled to the range of $[0,V_{DD}]$. Simulations are provided to demonstrate the operation of the circuits.

5.3.1 One-Dimensional Configuration

This section discusses the lateral inhibition function that is achieved using νMOS devices arranged in a one-dimensional array

5.3.1.1 Circuit Description

Two νMOS components are used. The first performs the analogue addition of the inputs. The second is derived from the programmable gain amplifier presented by Al-Sarawi et. al. [10]. The amplification factor is very near to –1, effectively inverting the analogue input quantity.

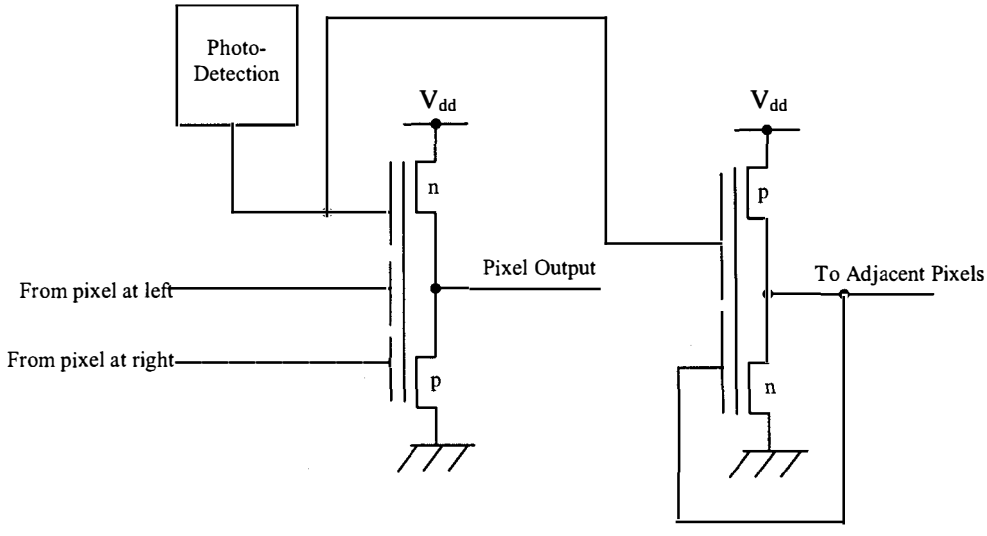


FIGURE 89 SINGLE LATERAL INHIBITION PIXEL

5.3.1.2 Simulation Results

The circuit in

Figure 91 was simulated using SPICE. The SPICE model for a single element is described by the subcircuit below:

```
.SUBCKT PIX_2 IN IN_E IN_W OUT OUT_NEG

M1 VPOWER G1 OUT OUT N_TYPE W=4U L=4U
M2 OUT    G1 0   OUT P_TYPE W=4U L=2U

C1 IN_E   G1 1P
C2 IN_W   G1 1P
C3 IN     G1 6P
R1 G1     0  1E12

M3 VPOWER    G2 OUT_NEG   VPOWER P_TYPE W=8U L=2U
M4 OUT_NEG   G2 0         0      N_TYPE W=4U L=4U

C4 IN        G2 1P
C5 OUT_NEG   G2 1P
R2 G2        0         1E12

V1 VPOWER 0 3V

.ENDS
```

Where the capacitor C3 can be modified to adjust the amount of inhibition that occurs. This was done for a range of values, ranging from 1pF to 6pF. These values show a wide range of characteristics, where the output function goes from inversion of the original input sequence (1pF) to near edge-detection (2pF) to edge enhancement of both 'bright' and 'dark' sides (3pF and 4pF) to enhancement of the bright edge only (5pF and 6pF). The other capacitor sizes that affect the transfer function are 1pF each for the inputs from adjacent pixels, which were kept constant for each simulation.

Intensity inputs were simulated using V_{DD} (3 volts) for pixels 1 to 4 inclusive, and zero volts for the remaining pixels (5-8 inclusive). Figure 90 shows the output intensity in volts for the linear array of pixels numbered 1-8.

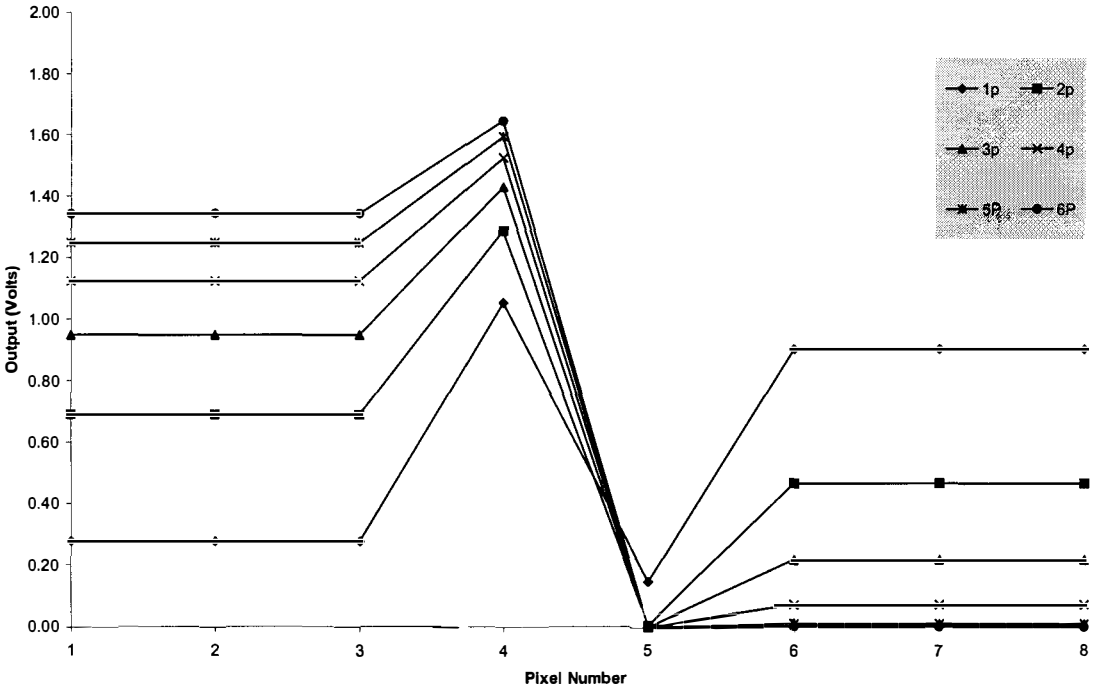


FIGURE 90 OUTPUT AMPLITUDES FOR LINEAR ARRAY OF LI PIXELS

The method of processing the image is to input the intensity values for each pixel of an image to each element of an array of inhibition pixels. Each circuit is identical and only connected to adjacent pixels. Thus the architecture is easily scalable. The SPICE format file is included as Appendix 4

5.3.2 Two-Dimensional Configuration

The technique of the previous section may be simply modified to accommodate two-dimensional configurations.

5.3.2.1 Circuit Description

Extra input floating gates are provided to accommodate the pixels that are located adjacent to the pixel in the second dimension. This is shown in Figure 91, and has the following interconnections;

- the input intensity, which in this simulation ranges from 0v to the supply voltage,

- an inverting output that has a transfer function approximately equal to the inverse of the input value,
- a set of four inputs, which are connected to adjacent pixels in order to inhibit the pixel output.

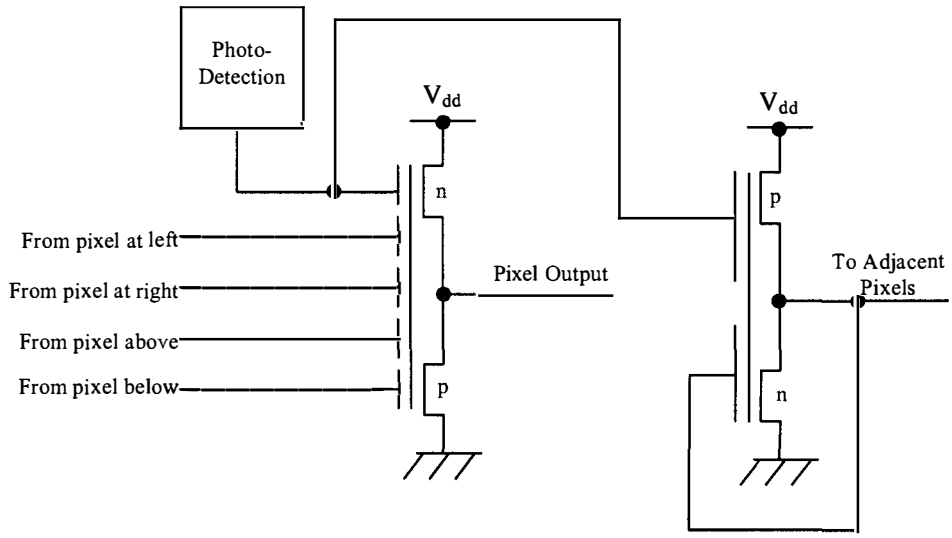


FIGURE 91 CONFIGURATION OF EDGE ENHANCEMENT CIRCUIT

This scheme may be applied not only to two- and four-dimensional pixel organisations, but also to hexagonal layouts, and those schemes that use information from pixels located diagonally. The weightings from the adjacent pixels are determined by the relative size of the input gates to the νMOS source-follower.

5.3.2.2 Simulation Results

A 2-dimensional array was simulated using SPICE. Input capacitances of 1pF for each of the four negating inputs from adjacent cells were used, the intensity-input capacitance varied to get different effects. The input image was comprised of a bright (3 volts) square applied to the centre cells ((3,3) to (6,6)), and 0v for the other inputs. Pixels at the edge of the array had their boundary negating inputs tied to their opposit non-boundary input. 3 volts was the peak input amplitude for the circuit, which was supplied power via a 3 volt rail.

The output from an 8x8 array of identical circuits produced the following results-

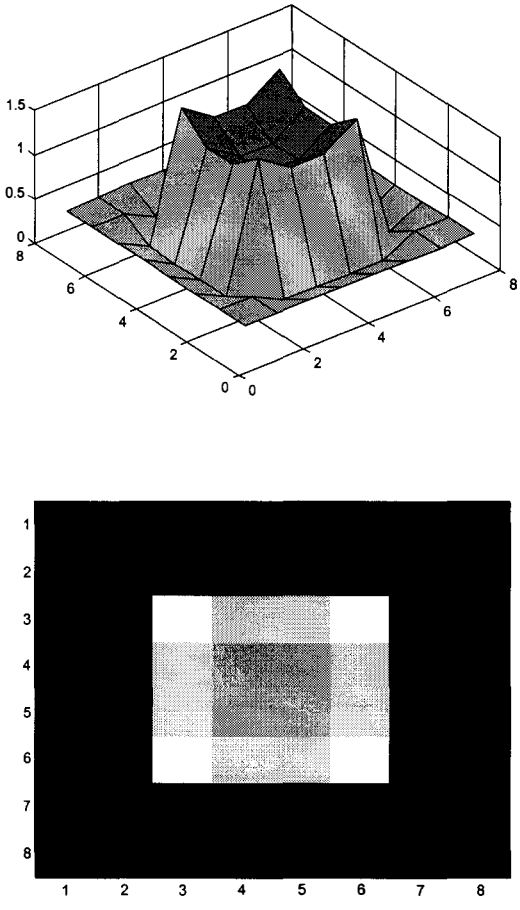


FIGURE 92 NON-NEGATING INPUT OF 6PF – SPICE SIMULATION RESULTS

The 3D plot in Figure 92 shows the output amplitudes of the array, with voltage as the vertical scale. A grey-scale image was generated from the pixel intensities, shown at the right of Figure 92.

The ratio of the sum of the negating inputs to the non-negating input varies the amount of enhancement. In Figure 93 the gate sizes for the simulation were 1pF for each of the negating inputs to 4pF for the non-negating input, giving evidence of a greater degree of inhibition.

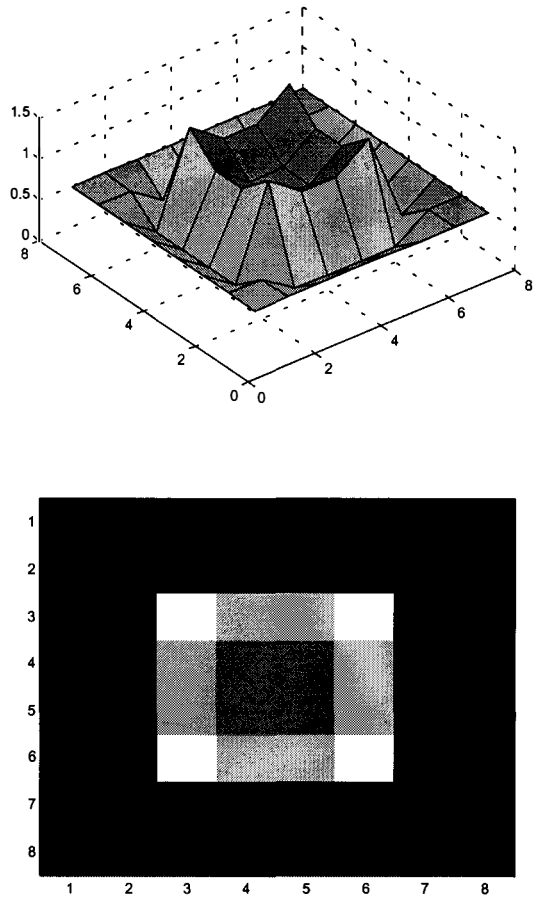


FIGURE 93 NON-NEGATING INPUT OF 4PF - SPICE SIMULATION RESULTS

5.3.3 Modelling

To achieve a simulation in SPICE for an image, which has sufficient resolution to represent a photographic grey-scale image the run times and resource usage was too prohibitive. A 64x64 pixel image was subjectively considered the minimum. This needed a 4096-element array of enhancement circuits, which could not be performed using a number of computer platforms, which were available. The simplicity of the transfer function with no feedback path enabled a simulation in a mathematical modelling environment.

The behaviour of the circuit was determined using SPICE. Two aspects were modelled, the first was that of the inverting output function. The input quantity was varied over the supply range and then the output examined. A 6^{th} order polynomial was generated to fit the resulting curve which yielded a

high correlation. This polynomial was used in conjunction with a mathematical model to generate the inverted output array.

The input was again varied from 0v to the supply voltage. The output transfer function, which works on the values of five sets of inputs (adjacent pixel outputs and the 'own pixel' photodetector') for a two-dimensionally connected array, was also fitted to a 6^{th} order polynomial. The pixel input intensity was multiplied by its weighting factor, which is realised in hardware by varying the size of the appropriate input capacitor, and the inverting inputs were added and averaged before being applied to the pixel output transfer function. This addition and averaging are a feature of neuron-MOS technology.

Figure 94 and Figure 95 show the polynomials fitted to the SPICE data output using the mathematical modelling tool.

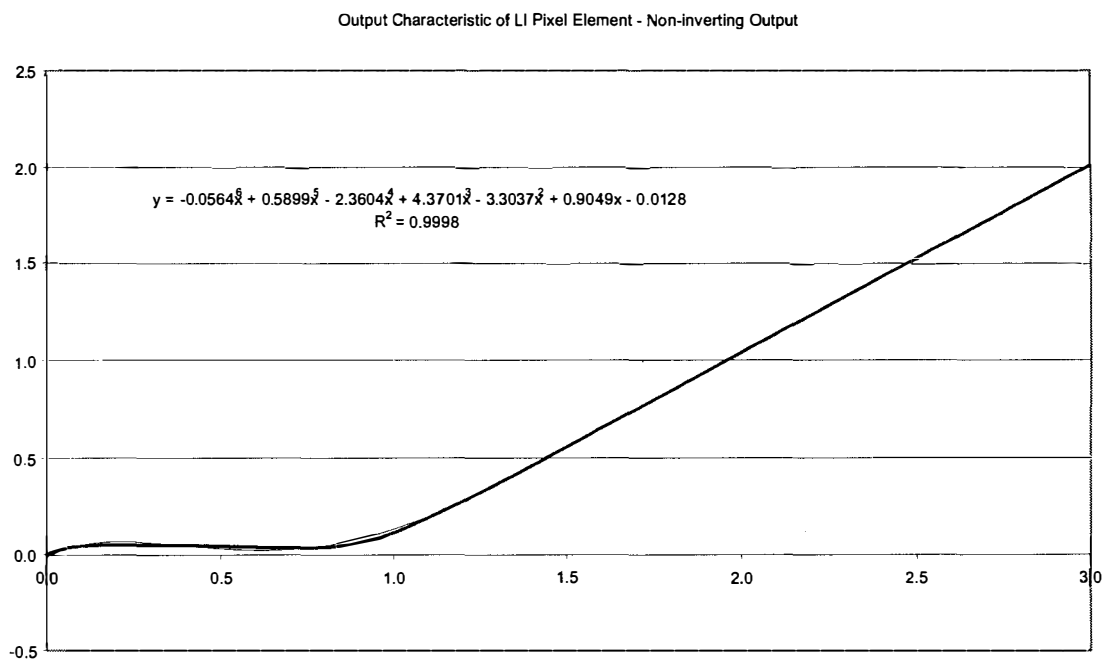


FIGURE 94 MODEL OF SUMMING OPERATON OF ENHANCMENT CIRCUIT

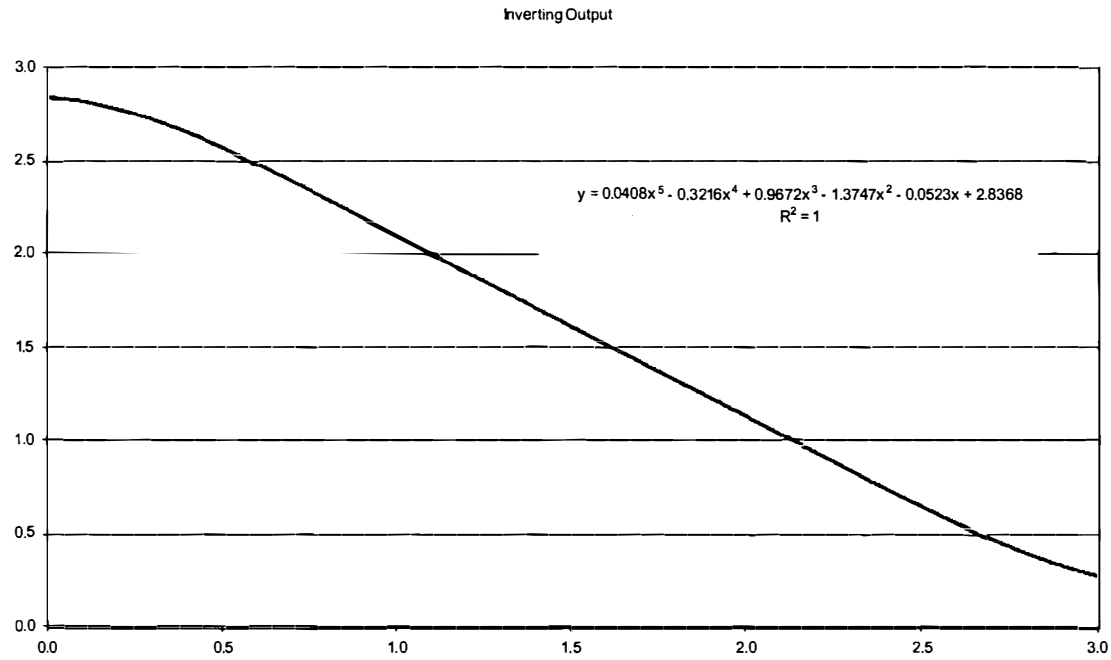


FIGURE 95 MODEL OF INVERTING OPERATION OF ENHANCEMENT CIRCUIT

5.3.4 Method of Simulating Larger Arrays

An intensity image was converted to an array of values ranging from zero to three, representing volts. This file was then loaded into a mathematical modelling package. The first operation was to produce the negated-output array, using the model developed in the previous section. These values were summed for each pixel, along with the non-negating input (the original 0-3V value) and then produced into a final array that was then applied to the output transfer function also developed from the model above.

This procedure was compared to the results from the SPICE simulations for an 8x8 array, and achieved high correlation.

5.3.5 Intensity Image Results

This section presents the results of simulations conducted on grey-scale images in order to determine the effectiveness of the lateral inhibition circuit when implemented using neuron-MOS technology.

The results of performing the operation on a 64x64 grey-scale intensity image (Figure 96) were generated with the size of the incident intensity input gate being varied. This was performed in order to determine the effects of enhancement due to negating/non-negating input gate ratios.

The first results show the effect of an almost exclusively inverting-input dominated picture. The incident intensity has little effect on the output, instead the output is a blurred negative image, with each pixel being an averaged result of the negated adjacent pixels. Figure 99, Figure 98 and Figure 99 show these results for non-negating input sizes of 1, 2 and 3 pF respectively. The negating input gate sizes were all 1pF.

FIGURE 96 THE ORIGINAL IMAGE

FIGURE 97 NON-NEGATING INPUT SIZE OF 1PF

FIGURE 98 NON-NEGATING INPUT SIZE OF 2PF

FIGURE 99 NON-NEGATING INPUT SIZE OF 3PF

As the weighting increases, the edges are enhanced without the output image appearing to be a 'negative' of the original image. The transfer function also has the effect of reducing the dynamic range into a median value. Analogue hardware processing can address this issue by scaling and translating the image to perform the operation of contrast enhancement, note that the images presented here are not contrast adjusted unless otherwise stated.

The image using a 4pF non-negating input is termed the equally-weighted image because the sum of the negating inputs is equal in weight to the non-negating input.

The following figures show the unadjusted image outputs for 4-, 6- and 8pF weightings:

FIGURE 100 THE ORIGINAL IMAGE

FIGURE 101 NON-NEGATING INPUT SIZE OF 4PF

FIGURE 102 NON-NEGATING INPUT SIZE OF 6PF

FIGURE 103 NON-NEGATING INPUT SIZE OF 8PF

The 4pF image, Figure 101, has the greatest edge enhancement. This image was contrast adjusted using a simple linear scaling and translation yielding the results of Figure 104.

FIGURE 104 THE 'EQUALLY-WEIGHTED' IMAGE, CONTRAST ADJUSTED

5.4 CONCLUSIONS

This section gave details of a proposed hardware method that can perform edge enhancement using lateral inhibition.

A method of asynchronously performing edge enhancement was presented. The method uses vMOS technology that not only allows a small number of transistors, but also operates asynchronously. The circuit works in a completely analogue mode. By varying the size of the input gates of a cell, the amount of edge enhancement can

be adjusted. The operation of edge detection can be accomplished by selecting an appropriate value for these gates.

Chapter 6

Conclusions and Future Work

This thesis described two novel applications of a new technology called neuron-MOS. Both circuits are involved in the front-end processing section of light input to a massively parallel focal plane array. A novel analogue-to-digital converter that is area efficient and operates without a control circuit or clock was developed. A circuit that performs edge enhancement was also developed.

6.1 CONCLUSIONS

The simulation stage of the research was comprised of two parts, the first being concerned with the simulation of the circuits at their simplest. Published results for νMOS circuits are usually only concerned with this aspect. These simulations form the basis of fundamental designs that will be implemented.

The second was oriented toward VLSI extraction of the practical circuits. The purpose of these simulations was to determine the areas of concern that may arise during manufacture. The theory level simulations do not include the capacitances and resistances that may be encountered after circuit layout and extraction to a SPICE file. The simulation results that were obtained from the SPICE file extracted from a VLSI layout agreed with those of the initial designs.

The work has achieved the following:

- A review of νMOS transistors, including their operation, circuit configurations, advantages, limitations.
- A review of methods of designing νMOS circuits using the FPGD (floating gate potential diagram).
- A review of methods of analogue-to-digital (A/D) conversion, the parameters used in evaluating A/D converters, and the contemporary methods of the converters presented in the literature.
- The development of a novel, small, low transistor count analogue to digital converter. This converter uses νMOS technology. The converter is suitable for inclusion in an array of identical Smart Pixel devices. The circuit showed successful operation for 6 bits resolution. The VLSI layout of the circuit was successfully simulated.
- The development of a novel, simple, area-efficient method of providing linear lateral inhibition that may be applied at the pixel level in a large array. The circuit performs edge enhancement as a result of its lateral inhibition function.

6.2 FUTURE WORK

The structures developed in the preceding were sent for fabrication. The technology was a Supertex 2μm double-poly CMOS process. This was chosen as it allowed economical evaluation of the νMOS devices.

The νMOS circuit structures fabricated were -

- 6-bit A/D converters of two different scalings but otherwise identical,
- inverters of differing input gate sizes,
- source-follower,
- Full adder, and
- D-latch.

The limitation of fabricating a large number of test devices on a single chip was the number of I/O pads that could be accommodated around its perimeter. To alleviate this, large areas for metal contacts that could easily be probed using the appropriate equipment were implemented to allow better use of the silicon area available.

A range of minimum capacitor sizes will be yielded from the results from SPICE simulations extracted from the VLSI layout editor, and the test results from the fabricated devices. These will be used to provide a set of minimum, median and maximum scalings for the devices. The overall number of test structures was not limited to available chip area, but instead to the packaging available which had 40 pins.

The three main topics dealt with in this thesis should be considered for future work: that of νMOS in general; the analogue-to-digital converter; and the lateral inhibition circuit in both one and two dimensions.

SPICE simulation procedures require work for this stage and should concentrate on the following aspects -

- Investigation of the problems associated with the analogue mode of νMOS devices, such as those encountered in [3].
- Evaluation of capacitor size effects for the νMOS structures. This includes the process parameters such as size and geometry tolerances.
- The effect of variation in the transistor width-to-length ratios.
- The effects of noise in the power supply to the circuit.
- The current-handling ability of the νMOS circuit in source-follower mode.

The lateral inhibition circuit may perform shunting inhibition with a small modification, that is, to provide a different method of feedback. This is more intensive in terms of simulation computations and thus may form the basis of future research.

Appendix 1

```
* HSPICE file created from adc6_2.ext - technology: scmos

.option scale=1u

m0 Vdd Input a5_n Vdd pfet w=5 l=3
+ ad=340 pd=306 as=20 ps=18
m1 Vdd a5_n a5 Vdd pfet w=5 l=3
+ ad=0 pd=0 as=20 ps=18
m2 Vdd a5 a5_inv Vdd pfet w=5 l=3
+ ad=0 pd=0 as=20 ps=18
m3 Vdd a4_fg a4_nm Vdd pfet w=5 l=3
+ ad=0 pd=0 as=20 ps=18
m4 Vdd a4_nm a4 Vdd pfet w=5 l=3
+ ad=0 pd=0 as=20 ps=18
m5 Vdd a4 a4_inv Vdd pfet w=5 l=3
+ ad=0 pd=0 as=20 ps=18
m6 Vdd a3_fg a3_nm Vdd pfet w=5 l=3
+ ad=0 pd=0 as=20 ps=18
m7 Vdd a3_nm a3 Vdd pfet w=5 l=3
+ ad=0 pd=0 as=20 ps=18
m8 Vdd a3 a3_inv Vdd pfet w=5 l=3
+ ad=0 pd=0 as=20 ps=18
m9 Vdd a2_fg a2_nm Vdd pfet w=5 l=3
+ ad=0 pd=0 as=20 ps=18
m10 Vdd a2_nm a2 Vdd pfet w=5 l=3
+ ad=0 pd=0 as=20 ps=18
m11 a5_n Input Gnd Gnd nfet w=4 l=4
+ ad=20 pd=18 as=459 ps=304
m12 a5 a5_n Gnd Gnd nfet w=4 l=4
+ ad=20 pd=18 as=0 ps=0
m13 a5_inv a5 Gnd Gnd nfet w=4 l=4
+ ad=20 pd=18 as=0 ps=0
m14 a4_nm a4_fg Gnd Gnd nfet w=4 l=4
+ ad=20 pd=18 as=0 ps=0
m15 a4 a4_nm Gnd Gnd nfet w=4 l=4
+ ad=20 pd=18 as=0 ps=0
m16 a4_inv a4 Gnd Gnd nfet w=4 l=4
+ ad=20 pd=18 as=0 ps=0
m17 a3_nm a3_fg Gnd Gnd nfet w=4 l=4
+ ad=20 pd=18 as=0 ps=0
m18 a3 a3_nm Gnd Gnd nfet w=4 l=4
+ ad=20 pd=18 as=0 ps=0
m19 a3_inv a3 Gnd Gnd nfet w=4 l=4
+ ad=20 pd=18 as=0 ps=0
m20 a2_nm a2_fg Gnd Gnd nfet w=4 l=4
+ ad=20 pd=18 as=0 ps=0
m21 a2 a2_nm Gnd Gnd nfet w=4 l=4
+ ad=20 pd=18 as=0 ps=0
m22 Gnd a0_nm a0 Gnd nfet w=4 l=4
+ ad=0 pd=0 as=20 ps=18
m23 Gnd a0_fg a0_nm Gnd nfet w=4 l=4
+ ad=0 pd=0 as=20 ps=18
m24 Gnd a1 a1_inv Gnd nfet w=4 l=4
+ ad=0 pd=0 as=20 ps=18
m25 Gnd a1_nm a1 Gnd nfet w=4 l=4
+ ad=0 pd=0 as=20 ps=18
m26 Gnd a1_fg a1_nm Gnd nfet w=4 l=4
+ ad=0 pd=0 as=20 ps=18
m27 Gnd a2 a2_inv Gnd nfet w=4 l=4
+ ad=0 pd=0 as=20 ps=18
m28 a0 a0_nm Vdd Vdd pfet w=5 l=3
+ ad=20 pd=18 as=0 ps=0
m29 a0_nm a0_fg Vdd Vdd pfet w=5 l=3
+ ad=20 pd=18 as=0 ps=0
m30 a1_inv a1 Vdd Vdd pfet w=5 l=3
+ ad=20 pd=18 as=0 ps=0
```

```
m31 a1 a1_nm Vdd Vdd pfet w=5 l=3
+ ad=20 pd=18 as=0 ps=0
m32 a1_nm a1_fg Vdd Vdd pfet w=5 l=3
+ ad=20 pd=18 as=0 ps=0
m33 a2_inv a2 Vdd Vdd pfet w=5 l=3
+ ad=20 pd=18 as=0 ps=0

C0 Vdd a3_nm 2.4fF
C1 Vdd Input 4.9fF
C2 a2_fg a5_inv 54.5fF
C3 Gnd a5 2.9fF
C4 Vdd a4_fg 4.9fF
C5 a1_fg a4_inv 55.6fF
C6 a0_fg a1_inv 13.5fF
C7 Gnd a2_nm 2.7fF
C8 Vdd a2 4.2fF
C9 Gnd a4 2.9fF
C10 Vdd a3 3.7fF
C11 a1_fg a2_inv 14.9fF
C12 Gnd a0_fg 17.5fF
C13 Vdd a1_fg 4.6fF
C14 Gnd a4_inv 4.3fF
C15 Input a4_fg 45.1fF
C16 a3_fg a4_inv 16.8fF
C17 Gnd a2_fg 19.5fF
C18 Vdd a5_n 2.4fF
C19 Gnd a0_nm 2.7fF
C20 a4_fg a5_inv 22.9fF
C21 Vdd a1 3.7fF
C22 a0_fg a3_inv 53.9fF
C23 Gnd a4_nm 2.9fF
C24 Vdd a3_fg 3.4fF
C25 Input a1_fg 215.7fF
C26 Gnd a1_nm 2.7fF
C27 a2_fg a3_inv 14.1fF
C28 Vdd a5 3.7fF
C29 a1_fg a5_inv 107.8fF
C30 a0_fg a4_inv 107.8fF
C31 Gnd a3_nm 2.7fF
C32 Vdd a2_nm 2.4fF
C33 Vdd a3_inv 2.2fF
C34 Gnd Input 9.4fF
C35 a2_fg a4_inv 27.3fF
C36 Gnd a4_fg 8.1fF
C37 Vdd a4 3.7fF
C38 Input a3_fg 64.8fF
C39 a0_fg a2_inv 26.9fF
C40 Gnd a2 3.8fF
C41 Vdd a0_fg 8.9fF
C42 Gnd a5_inv 6.5fF
C43 a3_fg a5_inv 32.7fF
C44 Gnd a3 2.7fF
C45 Vdd a2_fg 4.2fF
C46 Gnd a1_fg 17.6fF
C47 Vdd a0_nm 2.4fF
C48 Gnd a5_n 2.8fF
C49 Vdd a4_nm 2.4fF
C50 Input a0_fg 432.7fF
C51 Input a4_inv 4.0fF
C52 Gnd a1 2.7fF
C53 Vdd a1_nm 2.4fF
C54 Input a2_fg 108.2fF
C55 a1_fg a3_inv 28.6fF
C56 a0_fg a5_inv 216.2fF
C57 Gnd a3_fg 13.5fF
C58 a0 GND 4.3fF
C59 a1_nm GND 3.8fF
C60 a1 GND 3.6fF
C61 a0_nm GND 3.5fF
C62 a1_fg GND 11.8fF
C63 a0_fg GND 22.4fF
C64 a2 GND 9.3fF
```

```
C65 a2_nm GND 3.5fF
C66 a3_nm GND 3.5fF
C67 a4_nm GND 2.7fF
C68 a5_n GND 3.1fF
C69 a3 GND 3.5fF
C70 a4 GND 2.7fF
C71 a5 GND 2.7fF
C72 a2_inv GND 3.7fF
C73 a1_inv GND 2.0fF
C74 a4_inv GND 9.6fF
C75 a5_inv GND 8.1fF
C76 a3_inv GND 8.9fF
C77 Input GND 15.6fF
C78 Gnd GND 37.8fF
C79 Vdd GND 38.0fF

** hspice subcircuit dictionary
```

Appendix 2

```
HSPICE file created from adc6x2.ext - technology: scmos

.option scale=1u

m0 Vdd Input a5_n Vdd pfet w=8 l=6
+ ad=1360 pd=612 as=80 ps=36
m1 Vdd a5_n a5 Vdd pfet w=8 l=6
+ ad=0 pd=0 as=80 ps=36
m2 Vdd a5 a5_inv Vdd pfet w=8 l=6
+ ad=0 pd=0 as=80 ps=36
m3 Vdd a4_fg a4_nm Vdd pfet w=8 l=6
+ ad=0 pd=0 as=80 ps=36
m4 Vdd a4_nm a4 Vdd pfet w=8 l=6
+ ad=0 pd=0 as=80 ps=36
m5 Vdd a4 a4_inv Vdd pfet w=8 l=6
+ ad=0 pd=0 as=80 ps=36
m6 Vdd a3_fg a3_nm Vdd pfet w=8 l=6
+ ad=0 pd=0 as=80 ps=36
m7 Vdd a3_nm a3 Vdd pfet w=8 l=6
+ ad=0 pd=0 as=80 ps=36
m8 Vdd a3 a3_inv Vdd pfet w=8 l=6
+ ad=0 pd=0 as=80 ps=36
m9 Vdd a2_fg a2_nm Vdd pfet w=8 l=6
+ ad=0 pd=0 as=80 ps=36
m10 Vdd a2_nm a2 Vdd pfet w=8 l=6
+ ad=0 pd=0 as=80 ps=36
m11 a5_n Input Gnd Gnd nfet w=8 l=8
+ ad=80 pd=36 as=1836 ps=608
m12 a5 a5_n Gnd Gnd nfet w=8 l=8
+ ad=80 pd=36 as=0 ps=0
m13 a5_inv a5 Gnd Gnd nfet w=8 l=8
+ ad=80 pd=36 as=0 ps=0
m14 a4_nm a4_fg Gnd Gnd nfet w=8 l=8
+ ad=80 pd=36 as=0 ps=0
m15 a4 a4_nm Gnd Gnd nfet w=8 l=8
+ ad=80 pd=36 as=0 ps=0
m16 a4_inv a4 Gnd Gnd nfet w=8 l=8
+ ad=80 pd=36 as=0 ps=0
m17 a3_nm a3_fg Gnd Gnd nfet w=8 l=8
+ ad=80 pd=36 as=0 ps=0
m18 a3 a3_nm Gnd Gnd nfet w=8 l=8
+ ad=80 pd=36 as=0 ps=0
m19 a3_inv a3 Gnd Gnd nfet w=8 l=8
+ ad=80 pd=36 as=0 ps=0
m20 a2_nm a2_fg Gnd Gnd nfet w=8 l=8
+ ad=80 pd=36 as=0 ps=0
m21 a2 a2_nm Gnd Gnd nfet w=8 l=8
+ ad=80 pd=36 as=0 ps=0
m22 Gnd a0_nm a0 Gnd nfet w=8 l=8
+ ad=0 pd=0 as=80 ps=36
m23 Gnd a0_fg a0_nm Gnd nfet w=8 l=8
+ ad=0 pd=0 as=80 ps=36
m24 Gnd a1 a1_inv Gnd nfet w=8 l=8
+ ad=0 pd=0 as=80 ps=36
m25 Gnd a1_nm a1 Gnd nfet w=8 l=8
+ ad=0 pd=0 as=80 ps=36
m26 Gnd a1_fg a1_nm Gnd nfet w=8 l=8
+ ad=0 pd=0 as=80 ps=36
m27 Gnd a2 a2_inv Gnd nfet w=8 l=8
+ ad=0 pd=0 as=80 ps=36
m28 a0 a0_nm Vdd Vdd pfet w=8 l=6
+ ad=80 pd=36 as=0 ps=0
m29 a0_nm a0_fg Vdd Vdd pfet w=8 l=6
+ ad=80 pd=36 as=0 ps=0
m30 a1_inv a1 Vdd Vdd pfet w=8 l=6
+ ad=80 pd=36 as=0 ps=0
```

```
m31 a1 a1_nm Vdd Vdd pfet w=8 l=6
+ ad=80 pd=36 as=0 ps=0
m32 a1_nm a1_fg Vdd Vdd pfet w=8 l=6
+ ad=80 pd=36 as=0 ps=0
m33 a2_inv a2 Vdd Vdd pfet w=8 l=6
+ ad=80 pd=36 as=0 ps=0
C0 Input a3_inv 2.4fF
C1 Gnd a1_fg 70.3fF
C2 Vdd a0_nm 9.8fF
C3 Gnd Input 37.5fF
C4 Vdd a2_inv 6.3fF
C5 a3 a4_inv 2.7fF
C6 a2_fg a5_inv 217.8fF
C7 Input a4 2.7fF
C8 Gnd a5_n 11.3fF
C9 Vdd a4_nm 9.8fF
C10 a1 a3_inv 2.7fF
C11 a1_fg a4_inv 222.2fF
C12 a0_fg a1_inv 53.9fF
C13 Input a0_fg 1730.6fF
C14 Input a4_inv 16.1fF
C15 Gnd a1 10.9fF
C16 Vdd a1_nm 9.8fF
C17 Vdd c_n106_n102 2.8fF
C18 Input a2_fg 432.8fF
C19 Gnd a3_fg 54.0fF
C20 Vdd a3_nm 9.8fF
C21 a1 a4_inv 2.6fF
C22 a1_fg a2_inv 59.8fF
C23 Input a0_nm 2.6fF
C24 Gnd a5 11.8fF
C25 Vdd a4_fg 19.6fF
C26 a2_nm a3_inv 2.7fF
C27 a3_fg a4_inv 67.2fF
C28 Input a4_nm 2.7fF
C29 Gnd a2_nm 10.9fF
C30 Vdd a2 16.9fF
C31 Gnd a3_inv 7.0fF
C32 a1 a2_inv 2.6fF
C33 a4_fg a5_inv 91.6fF
C34 Gnd a4 11.8fF
C35 Vdd a3 14.8fF
C36 a2 a5_inv 2.7fF
C37 a2_nm a4_inv 2.7fF
C38 a0_fg a3_inv 215.5fF
C39 Input a3_nm 2.7fF
C40 a4_inv a3_inv 2.0fF
C41 Gnd a0_fg 69.8fF
C42 Vdd a1_fg 18.5fF
C43 Gnd a4_inv 17.1fF
C44 Vdd a1_inv 3.1fF
C45 Vdd Input 19.5fF
C46 a2_fg a3_inv 56.3fF
C47 Input a4_fg 180.2fF
C48 Gnd a2_fg 78.0fF
C49 Vdd a5_n 9.8fF
C50 a1_fg a5_inv 431.0fF
C51 a0_fg a4_inv 431.0fF
C52 a2_inv a3_inv 2.0fF
C53 Input a5_inv 5.2fF
C54 Gnd a0_nm 10.9fF
C55 Vdd a1 14.8fF
C56 a2_fg a4_inv 109.4fF
C57 Input a3 3.2fF
C58 Gnd a4_nm 11.8fF
C59 Vdd a3_fg 13.7fF
C60 a1_nm a3_inv 2.7fF
C61 a2 c_304_n90 2.8fF
C62 a0_fg a2_inv 107.8fF
C63 Input a1_fg 862.9fF
C64 a2_inv a4_inv 2.0fF
C65 Gnd a1_nm 10.9fF
```

```
C66 Vdd a0 7.9fF
C67 Vdd c_n106_68 2.8fF
C68 Vdd a5 14.8fF
C69 a3_fg a5_inv 130.9fF
C70 Input a5_n 2.7fF
C71 Gnd a3_nm 10.9fF
C72 Vdd a2_nm 9.8fF
C73 a1_nm a4_inv 3.2fF
C74 Vdd a3_inv 8.7fF
C75 Gnd a4_fg 32.5fF
C76 Vdd a4 14.8fF
C77 a2_nm a5_inv 2.7fF
C78 a3_nm a4_inv 2.7fF
C79 a2 a3_inv 4.7fF
C80 Input a3_fg 259.3fF
C81 Gnd a2 15.2fF
C82 Vdd a0_fg 35.8fF
C83 Gnd a5_inv 26.0fF
C84 a1_nm a2_inv 2.6fF
C85 Input a5 2.7fF
C86 Gnd a3 10.9fF
C87 Vdd a2_fg 16.8fF
C88 a2 a4_inv 2.7fF
C89 a1_fg a3_inv 114.5fF
C90 a0_fg a5_inv 865.0fF
C91 a1_inv a3_inv 6.7fF
C92 a0 GND 17.0fF
C93 a1_nm GND 15.3fF
C94 a1 GND 14.4fF
C95 a0_nm GND 14.0fF
C96 a1_fg GND 47.3fF
C97 a0_fg GND 89.6fF
C98 a2 GND 37.2fF
C99 a2_nm GND 14.0fF
C100 a3_nm GND 14.0fF
C101 a4_nm GND 10.6fF
C102 a5_n GND 12.2fF
C103 a3 GND 14.0fF
C104 a4 GND 10.6fF
C105 a5 GND 10.6fF
C106 a2_inv GND 14.8fF
C107 a1_inv GND 8.1fF
C108 a4_inv GND 38.4fF
C109 a5_inv GND 32.3fF
C110 a3_inv GND 35.8fF
C111 Input GND 62.3fF
C112 Gnd GND 151.1fF
C113 Vdd GND 151.9fF

** hspice subcircuit dictionary
```

Appendix 3

MOSIS PARAMETRIC TEST RESULTS

RUN: N91W VENDOR: ORBIT
TECHNOLOGY: SCNA20 FEATURE SIZE: 2.0 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: Orbit Semiconductor 2.0 um n-well.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3/2			
Vth		0.84	-0.88	Volts
SHORT	18/2			
Idss		166	-92	uA/um
Vth		0.78	-0.86	Volts
Vpt		10.0	-15.0	Volts
WIDE	50/2		-9.0	Volts
Ids0		0.1	-2.8	pA/um
LARGE	18/18			
Vth		0.81	-0.87	Volts
Vjbkd		14.7	-15.8	Volts
Ijlk		-26.2	-3.1	pA
Gamma		0.47	0.92	V^0.5
K' (Uo*Cox/2)		28.1	-10.1	uA/V^2

POLY2 TRANSISTORS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	6/4			
Vth		0.84	-1.34	Volts
SHORT	12/4			
Vth		0.81	-1.32	Volts
LARGE	36/36			
Vth		0.80	-1.31	Volts
K' (Uo*Cox/2)		21.2	-6.2	uA/V^2

COMMENTS: XL_ORB_SCNA20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>16.4	<-14.2	Volts

BIPOLAR PARAMETERS	W/L	NPN	UNITS
2X1	2X1		
Beta		86	
V_early		69.6	Volts
Vce,sat		0.5	Volts
2X2	2X2		
Beta		77	
V_early		66.2	Volts

Vce,sat	0.2	Volts
2X4	2X4	
Beta	77	
V_early	62.0	Volts
Vce,sat	1.7	Volts
2X8	2X8	
Beta	75	
V_early	61.2	Volts
Vce,sat	1.1	Volts
BVceo	18.4	Volts
BVcbo	21.2	Volts
BVebo	8.4	Volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	MTL1	MTL2	N_WELL	UNITS
Sheet Resistance	30.1	61.3	21.5	21.6	0.06	0.03	2819	ohms/sq
Width Variation	0.04	-0.16	-0.43	-0.29	-0.27	-0.25		microns
(measured - drawn)								
Contact Resistance	12.2	38.2	7.2	7.3		0.05		ohms
Gate Oxide Thickness	406							angstroms

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	MTL1	MTL2	N_WELL	UNITS
Area (substrate)	138	313	55		23	12	23	aF/um^2
Area (N+active)			850	625	45	22		aF/um^2
Area (P+active)			844	621				aF/um^2
Area (poly)				462	41	19		aF/um^2
Area (poly2)					42			aF/um^2
Area (metal1)						31		aF/um^2
Fringe (substrate)	490	322			58	36		aF/um
Fringe (poly)					53	44		aF/um
Fringe (metal1)						56		aF/um
Overlap (N+active)			343					aF/um
Overlap (P+active)			453					aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.16	Volts
Vinv	1.5	2.39	Volts
Vol (100 uA)	2.0	0.25	Volts
Voh (100 uA)	2.0	4.69	Volts
Vinv	2.0	2.54	Volts
Gain	2.0	-9.21	
Ring Oscillator Freq.			
MOSIS (31-stage,5V)		36.62	MHz
DIV16 (31-stage,5V)		40.24	MHz
Ring Oscillator Power			
DIV16 (31-stage,5V)		1.51	uW/MHz/g

N91W SPICE LEVEL3 PARAMETERS

```
.MODEL CMOSN NMOS LEVEL=3 PHI=0.700000 TOX=4.0600E-08 XJ=0.200000U TPG=1
+ VTO=0.8093 DELTA=1.6500E+00 LD=4.1440E-07 KP=5.2580E-05
+ UO=618.2 THETA=5.3110E-02 RSH=1.5840E+01 GAMMA=0.4121
+ NSUB=3.7010E+15 NFS=5.9090E+11 VMAX=1.6760E+05 ETA=6.4270E-02
+ KAPPA=4.5740E-01 CGDO=5.2869E-10 CGSO=5.2869E-10
+ CGBO=3.4581E-10 CJ=1.4229E-04 MJ=6.2160E-01 CJSW=5.0307E-10
+ MJSW=2.4938E-01 PB=3.8328E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.0000E-09
.MODEL CMOSP PMOS LEVEL=3 PHI=0.700000 TOX=4.0600E-08 XJ=0.200000U TPG=-1
+ VTO=-0.8460 DELTA=4.6140E-01 LD=4.9340E-07 KP=1.8388E-05
+ UO=216.2 THETA=1.0720E-01 RSH=5.1170E+01 GAMMA=0.5557
+ NSUB=6.7290E+15 NFS=5.9090E+11 VMAX=2.6220E+05 ETA=7.9790E-02
+ KAPPA=1.0000E+01 CGDO=6.2948E-10 CGSO=6.2948E-10
+ CGBO=3.8539E-10 CJ=3.1476E-04 MJ=5.7042E-01 CJSW=3.1623E-10
+ MJSW=2.4970E-01 PB=8.8539E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 1.6070E-07
```

N91W SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

```
* DATE: Mar 24/99
* LOT: n91w                    WAF: 05
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                          LEVEL   = 49
+VERSION = 3.1           TNOM    = 27            TOX     = 4.06E-8
+XJ      = 2E-7          NCH     = 8E16          VTHO    = 0.7800861
+K1      = 1.3257304     K2      = -0.2663331    K3      = 3.3540235
+K3B     = -5.7456265    W0      = 1E-7          NLX     = 5.017841E-8
+DVT0W   = 0             DVT1W   = 5.3E6         DVT2W   = -0.032
+DVT0    = 0.8934518     DVT1    = 0.3510562     DVT2    = -0.3868226
+U0      = 695.2799467   UA      = 2.564957E-9   UB      = 1.028628E-19
+UC      = 4.805942E-11  VSAT    = 1.099499E5    A0      = 0.5000461
+AGS     = 0.1671009     B0      = 2.068932E-6   B1      = 3.876022E-6
+KETA    = -0.0241171    A1      = 0             A2      = 1
+RDSW    = 1.288299E3    PRWG    = -2.512952E-3  PRWB    = -2.015395E-7
+WR      = 1             WINT    = 2.001109E-7   LINT    = 4.393779E-7
+XL      = 0             XW      = 0             DWG     = -4.181007E-8
+DWB     = 9.275506E-8   VOFF    = -0.1050041    NFACTOR = 0.361228
+CIT     = 0             CDSC    = 1.506004E-4   CDSCD   = 0
+CDSCB   = 0             ETA0    = 2.218414E-3   ETAB    = -9.030716E-4
+DSUB    = 5.04009E-3    PCLM    = 5.478981      PDIBLC1 = 0.4735148
+PDIBLC2 = 1.987973E-4   PDIBLCB = -1E-3         DROUT   = 0.3150364
+PSCBE1  = 4.176147E10   PSCBE2  = 1.217414E-6   PVAG    = 1.7815725
+DELTA   = 0.01          MOBMOD  = 1             PRT     = 0
+UTE     = -1.5          KT1     = -0.11         KT1L    = 0
+KT2     = 0.022         UA1     = 4.31E-9       UB1     = -7.61E-18
+UC1     = -5.6E-11      AT      = 3.3E4         WL      = 0
+WLN     = 1             WW      = 0             WWN     = 1
+WWL     = 0             LL      = 0             LLN     = 1
+LW      = 0             LWN     = 1             LWL     = 0
+CAPMOD  = 2             XPART   = 0.4           CGD0    = 5.29E-10
+CGS0    = 5.29E-10      CGB0    = 0             CJ      = 1.422861E-4
+PB      = 0.383282      MJ      = 0.6215988     CJSW    = 5.030745E-10
+PBSW    = 0.6814339     MJSW    = 0.2493804     PVTH0   = 5.216115E-3
+PRDSW   = -1.96936E3    PK2     = -0.0576815    WKETA   = 0.0466172
+LKETA   = 9.874513E-3    )
*
*
.MODEL CMOSP PMOS (                                          LEVEL   = 49
+VERSION = 3.1           TNOM    = 27            TOX     = 4.06E-8
+XJ      = 2E-7          NCH     = 8E16          VTHO    = -0.826916
+K1      = 0.7250266     K2      = -0.025237     K3      = 8.0698586
+K3B     = -2.3474126    W0      = 2.191076E-6   NLX     = 1.31782E-7
+DVT0W   = 0             DVT1W   = 5.3E6         DVT2W   = -0.032
+DVT0    = 3.3322671     DVT1    = 0.5057503     DVT2    = -0.1240424
+U0      = 283.9100584   UA      = 5.532261E-9   UB      = 3.1826E-18
+UC      = -9.52819E-11  VSAT    = 1.442493E5    A0      = 0.9541691
+AGS     = 0.1224104     B0      = 7.056174E-7   B1      = 4.277515E-7
+KETA    = -4.299405E-3  A1      = 0             A2      = 1
+RDSW    = 2.69947E3     PRWG    = -0.011933     PRWB    = -8.892093E-3
+WR      = 1             WINT    = 2.153686E-7   LINT    = 5.09883E-7
+XL      = 0             XW      = 0             DWG     = -4.372868E-8
+DWB     = 2.597449E-8   VOFF    = -0.053662     NFACTOR = 0.3339533
+CIT     = 0             CDSC    = 1.57364E-4    CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.0210985     ETAB    = 1.54997E-4
+DSUB    = 0.0259152     PCLM    = 6.9799452     PDIBLC1 = 0.3662639
+PDIBLC2 = 0.0099931     PDIBLCB = 0             DROUT   = 4.192685E-3
+PSCBE1  = 2.699703E9    PSCBE2  = 3.839271E-9   PVAG    = 0.7819165
+DELTA   = 0.01          MOBMOD  = 1             PRT     = 0
+UTE     = -1.5          KT1     = -0.11         KT1L    = 0
+KT2     = 0.022         UA1     = 4.31E-9       UB1     = -7.61E-18
+UC1     = -5.6E-11      AT      = 3.3E4         WL      = 0
+WLN     = 1             WW      = 0             WWN     = 1
+WWL     = 0             LL      = 0             LLN     = 1
+LW      = 0             LWN     = 1             LWL     = 0
+CAPMOD  = 2             XPART   = 0.4           CGD0    = 6.29E-10
+CGS0    = 6.29E-10      CGB0    = 0             CJ      = 3.147558E-4
+PB      = 0.885389      MJ      = 0.5704172     CJSW    = 3.162317E-10
```

```
+PBSW    = 0.9895045      MJSW    = 0.2496954      PVTHO   = 0.0684301
+PRDSW   = -1.880324E3    PK2     = -2.514253E-3   WKETA   = 9.4713E-3
+LKETA   = -9.1405E-3      )
*
```

Appendix 4

```
* One-Dimensional Lateral Inhibition Circuit

.TRAN 10M 100M UIC

.MODEL P_TYPE PMOS ( LEVEL=2 VTO=-.9 KP=1.7E-5 GAMMA=.5
PHI=.69 LAMBDA=0.04
+ CGSO=2.8E-10 CGDO=2.8E-10 CJ=0.00033 MJ=.5 CJSW=4.4E-
10 MJSW=.33 JS=0.001
+ TOX=4.25E-8 NFS=1E11 LD=3.5E-7 UCRIT=1000 RSH=45 AF=1
KF=7.2E-29)

.MODEL   N_TYPE NMOS ( LEVEL=2 VTO=.9 KP=5.7E-5 GAMMA=.3
PHI=.7 LAMBDA=0.05
+ CGSO=1.8E-10 CGDO=1.8E-10 CJ=7E-5 MJ=.5 CJSW=3.9E-10
MJSW=.33 JS=0.001
+ TOX=4.25E-8 NFS=1E11 LD=2.2E-7 UCRIT=1000 RSH=25 AF=1
KF=2.3E-29)


*DEFINE PIX_VOLTS=3V


.OPTIONS RELTOL=0.005


.SUBCKT PIX_2 IN IN_E IN_W OUT OUT_NEG

M1 VPOWER G1 OUT OUT N_TYPE W=4U L=4U
M2 OUT    G1 0   OUT P_TYPE W=4U L=2U

C1 IN_E   G1 1P
C2 IN_W   G1 1P
C3 IN     G1 6P
R1 G1     0  1E12

M3 VPOWER    G2 OUT_NEG   VPOWER P_TYPE W=8U L=2U
M4 OUT_NEG   G2 0         0      N_TYPE W=4U L=4U

C4 IN        G2 1P
C5 OUT_NEG   G2 1P
R2 G2        0         1E12

V1 VPOWER 0 3V

.ENDS

*{ PULSE=3 RISE=10U FALL=10U PERIOD=20.01U }
.SUBCKT PULSE#0 1 2
V1 1 2 PULSE 0 3.0000 1U 10.0000U 10.0000U
```

```
+ 5.0000N 20.010U
R1 1 2 1MEG
.ENDS


*DEFINE VAL001 =3V
*DEFINE VAL002 =3V
*DEFINE VAL003 =3V
*DEFINE VAL004 =3V
*DEFINE VAL005 =0V
*DEFINE VAL006 =0V
*DEFINE VAL007 =0V
*DEFINE VAL008 =0V



R1 OUT   0 10MEG
R2 OUTN1 0 10MEG
R3 OUTN2 0 10MEG


R000  OUTW000  0 10MEG


R001  OUT001  0 10MEG
R002  OUT002  0 10MEG
R003  OUT003  0 10MEG
R004  OUT004  0 10MEG
R005  OUT005  0 10MEG
R006  OUT006  0 10MEG
R007  OUT007  0 10MEG
R008  OUT008  0 10MEG
R009  OUT009  0 10MEG

V001  IN001  0 VAL001
V002  IN002  0 VAL002
V003  IN003  0 VAL003
V004  IN004  0 VAL004
V005  IN005  0 VAL005
V006  IN006  0 VAL006
V007  IN007  0 VAL007
V008  IN008  0 VAL008

X001  IN001  NEG002  NEG002  OUT001  NEG001    PIX_2
X002  IN002  NEG003  NEG001  OUT002  NEG002    PIX_2
X003  IN003  NEG004  NEG002  OUT003  NEG003    PIX_2
X004  IN004  NEG005  NEG003  OUT004  NEG004    PIX_2
X005  IN005  NEG006  NEG004  OUT005  NEG005    PIX_2
X006  IN006  NEG007  NEG005  OUT006  NEG006    PIX_2
X007  IN007  NEG008  NEG006  OUT007  NEG007    PIX_2
X008  IN008  NEG007  NEG007  OUT008  NEG008    PIX_2


* X2 IN004  0 PULSE#0
```

```
.PRINT TRAN V(OUT001 )
.PRINT TRAN V(OUT002 )
.PRINT TRAN V(OUT003 )
.PRINT TRAN V(OUT004 )
.PRINT TRAN V(OUT005 )
.PRINT TRAN V(OUT006 )
.PRINT TRAN V(OUT007 )
.PRINT TRAN V(OUT008 )

*.PRINT TRAN IN004


.END
```

Chapter 7

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