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A WIDE DYNAMIC RANGE CMOS IMAGER WITH EXTENDED SHUNTING INHIBITION IMAGE PROCESSING CAPABILITIES

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ABSTRACT

A CMOS imager based on a novel mixed-mode VLSI implementation of biologically inspired shunting inhibition vision models is presented. It can achieve a wide range of image processing tasks such as image enhancement or edge detection via a programmable shunting inhibition processor. Its most important feature is a gain control mechanism allowing local and global adaptation to the mean input light intensity. This feature is shown to be very suitable for wide dynamic range imagers.

1. INTRODUCTION

The concept behind today's ever growing surge of interest in CMOS imager technology is "System-On-Chip". The trend of Digital Imaging Technology is now to build fully integrated camera systems on a single chip, featuring image acquisition and on-chip processing. The fully integrated product results in significant system cost savings but also in improved sensor performance [1] since the acquired image can be processed on chip. For instance, pixel defects in the sensor array (appearing in the image as randomly distributed white or black points) can be detected and canceled by using a simple correction algorithm [2]. Similarly, noise reduction algorithms can be implemented on chip to increase the signal-to-noise ratio. The main aim of on-chip processing is to improve the quality of the acquired image. Additional on-chip processing can also be carried out to perform more specific tasks in many application fields such as robotics, medical imaging, etc.

This paper presents a high dynamic range CMOS imager prototype with such processing capabilities, based on shunting inhibition models of biological vision systems [3][4]. It exhibits local and global adaptation [4][5] mechanisms to improve the quality of the acquired image. Furthermore, it can perform various image processing tasks ranging from edge detection to image enhancement. These visual processing capabilities can be controlled externally via a programmable shunting inhibition mixed-mode analog-digital processor. Its main feature, as compared to previous image processors [6][7], is that the convolution kernels are not predefined but tuned externally via a bias circuitry. As a consequence, any kernel can be set externally enabling a wide range of image processing tasks such as image enhancement or edge detection. In the next section, a brief overview of shunting inhibition and its application to image processing is given. Section 3 describes the integrated 0.7μm

CMOS imager prototype, both its architecture and operation. Section 4 presents the shunting inhibition mixed-mode processor along with simulation results. Finally, concluding remarks are given in Section 5.

2. SHUNTING INHIBITION FOR IMAGE PROCESSING

Shunting Inhibitory Cellular Neural Networks (SICNNs) are a class of biologically inspired neural networks that were originally introduced by Bouzerdoum and Pinter [4] to model the visual system. Each SICNN consists of a two-dimensional array of interconnected processing cells. In this network, interactions can only occur locally within each cell neighborhood. The state of each cell is described by the following differential equation:

$$\frac{dx_{ij}}{dt} = I_{ij} - a_{ij}x_{ij} - \sum_{m,n \in N(i,j)} w_{mn} f(x_{mn})x_{ij} \qquad (1)$$

where the subscripts i,j refer to cell(i,j); x_{ij} is the cell state; I_{ij} is the external input to the cell; $a_{ij} > 0$ represents the decay factor of the activation; f is a non-negative activation function relating the cell's state to its output; $w_{mn} > 0$ is the synaptic weight from cell(m,n) to cell(i,j), and $N(i,j)$ is the interaction neighborhood of cell(i,j). One can see from Equation (1) that the neighborhood of each cell tends to inhibit (since $w_{mn} > 0$) its response to direct excitation in a multiplicative fashion, hence the term "Shunting Inhibition" [4]. Note also that Equation (1) describes the dynamics of a feedback SICNN. In a feedforward network, the state of the cell(m,n) is replaced by the external input I_{mn} to that cell. Consequently, the differential equation describing a feedforward SICNN becomes:

$$\frac{dx_{ij}}{dt} = I_{ij} - a_{ij}x_{ij} - \sum_{m,n \in N(i,j)} w_{mn} f(I_{mn})x_{ij} \qquad (2)$$

The steady state response of the SICNN network described by Equation (2) to a time invariant input, assuming a linear activation function $f(\xi)=\xi$, can be expressed as [4]:

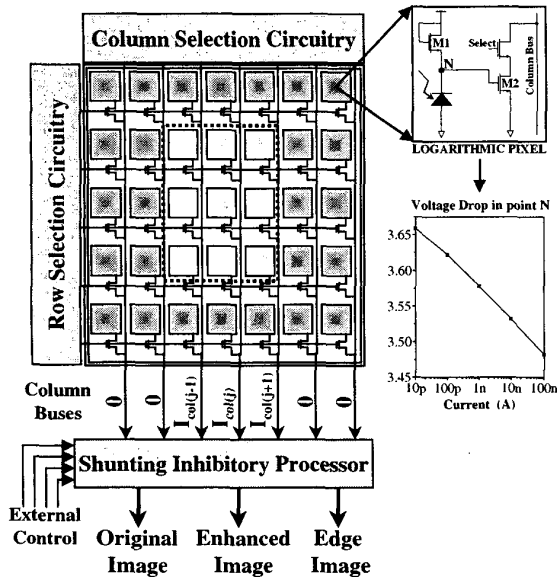$$x_{ij} = \frac{I_{ij}}{a_{ij} + \sum_{m,n \in N(i,j)} w_{mn} I_{mn}} \qquad (3)$$

Figure 1. The 64×64 CMOS imager architecture. The pixel used is "logarithmic": the voltage at the sensing node N is proportional to the logarithm of the light intensity. Note also that a 3×3 window is selected in this pixel array.

SICNNs can be applied to image processing by simply considering that each pixel of the acquired image to be processed is the external input I_{ij} to the cell. The states x_{ij} consequently represent the on-chip processed image, whereas the interaction neighborhood of cell(i,j) would correspond to the chosen window over which the processing is to be carried out. If the decay factor a_{ij} is assumed constant for all cells then the interaction weights w_{mn} will be the only SICNN parameters along with the $k \times k$ window size that determine the properties and the performance of the network. We should note also that the SICNN exhibits a gain control mechanism, which is mediated by the expression in the denominator of Equation (3). The SICNN output will thus adapt to the mean input intensity. This property can be used to perform a wide range of image processing tasks such as dynamic range compression, noise filtering, edge detection and image enhancement [4][5].

3. IMAGER ARCHITECTURE AND OPERATION

The imager has been designed in full custom 0.7μm CMOS technology with n^+p photodiodes as sensing elements. The sensor architecture is given in Figure 1. It comprises a 64×64 pixel array. Each pixel has a size of 30×30μm with a fill factor of 80% and operates as follows. The optically generated charges or photocurrent are continuously converted to a voltage at the sensing node N seen in Figure 1. As the load transistor M1 operates in weak inversion, the light to voltage conversion will be logarithmic [8]. Each pixel can thus cope with over 4 decades
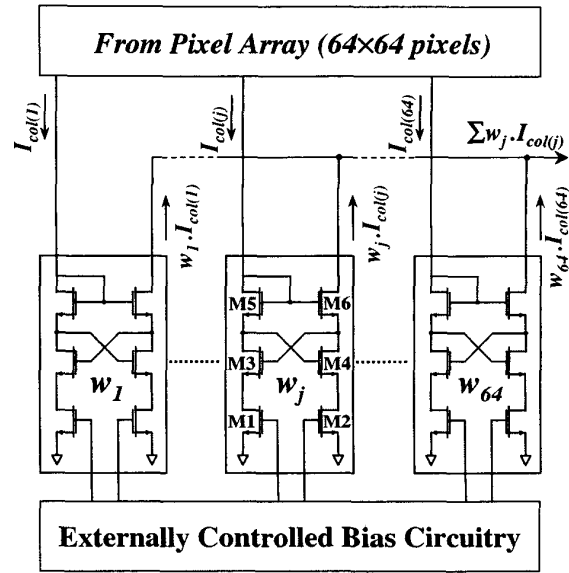

Figure 2. Block diagram of the weighted sum as performed by the Shunting Inhibitory Processor. Note that each column bus is sent to a current mirror whose gain w_j can be adjusted externally via a bias circuitry. Note that w_j refers to w_{mn} in Equation (3).

variations in light intensity as seen in the lower right corner of Figure 1. At the readout stage, the Select transistor is closed and the pixel output current is fed to a column bus to be added to the currents from all the selected pixels within a column. This sum is provided to the Shunting Inhibitory Processor through each column bus. The Shunting Inhibitory Processor computes the SICNN output, Equation (3), by carrying out the overall weighted sum then the division. Any 3×3, 5×5, 7×7 or 9×9 window of the array can be selected for readout by the row and column selection circuitry. The only limitation is that the weights within a column will be constant.

The readout process can be sequential or externally controlled. The automatic sequential scan of the array is implemented by means of a synchronous counter, which generates the address signals to the row and column decoders. Random access, on the other hand, is achieved via two 6-bit address words provided externally to the row and column decoders. The decoder outputs are sent to a second decoder, which in turn can enable window readout over the array. A set of externally controlled switches and multiplexers define the readout mode. Current mirrors are used to buffer the selected output currents so that the readout speed can be increased. Inputs to the imager are 6-bit address words for random readout, a reference bias current, analog voltages to set current mirror gains in the Shunting Inhibitory Processor, select signals to test each imager building block separately and enable signals for each output mode.

The imager features two main modes of operation with the Shunting Inhibitory Processor (**SIP**) enabled or disabled. The first mode (SIP disabled) provides the original input image

unprocessed. Pixel outputs are simply read out with sequential or externally controlled random addressing. In the second mode (SIP enabled), shunting inhibition processing is carried out in two steps. For a $k \times k$ processing window, the central pixel $P_{i,j}$ output is first read out and stored in the SIP. In the second step, all $k \times k$ window pixels are selected simultaneously and their outputs are handed out to the SIP through each column bus. The SICNN output is then computed and used to perform various image processing tasks. For instance, image enhancement is achieved by merging the input image to the SICNN output whereas the edge image is obtained by thresholding the latter [5].

4. THE SHUNTING INHIBITORY PROCESSOR (SIP)

The main function of the SIP is to compute the SICNN output for each acquired image. Its design is based on a mixed-mode approach: analog processing to carry out the weighted sum of the $k \times k$ selected pixels and digital processing to perform the division. This analog-digital implementation is illustrated by the layout view of the SIP given in Figure 3. The layout has been realized in full custom 0.7μm CMOS technology at a 30μm pitch. It exhibits three distinct regions: three pixel rows from the array on top, the SIP analog current mirror network in the middle and the SIP digital circuitry at the bottom. Each column bus is an input to the SIP and is sent (Figure 2) to a programmable gain current mirror so that the sum of weighted column outputs can flow through an external resistor.
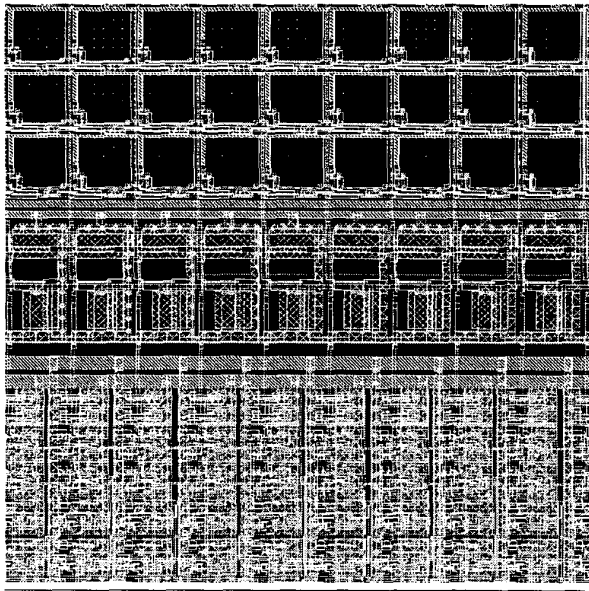

Figure 3. Layout view of the Shunting Inhibitory. Three distinct regions can be seen: three pixel rows from the array on top, the SIP analog current mirror network in the middle and the SIP digital circuitry at the bottom.

The resulting voltage drop across the load is then amplified and digitized before the division is performed. The weight coefficients w_j ($0 < w_j < 1$) are set by the current mirror network shown in Figure 2. The basic element of the network is a programmable gain current mirror in which MOS transistors M3 and M4 are matched to M5 and M6. The gain of the current mirror is a function of transistors M1 and M2 gate voltage ratio, provided that M1 and M2 are operating in the linear region while all other transistors are operating in the saturation region. An externally controlled bias circuitry is thus used to set the current mirror gains and define the SICNN weight coefficients w_j.

A special attention was given to the main non-idealities encountered in the practical implementation of current mirrors. For instance, mismatch error has been minimized by choosing channel lengths greater than the technology minimum feature size, which in fact does not result in appreciable area reduction due to the minimum contact size allowed by the 0.7μm CMOS technology used. Circuitry exposure to light has also been considered since it results in an overall increase in leakage current and in larger MOS threshold voltage dispersions. To minimize light exposure effects, bias currents have been chosen sufficiently large while current mirrors have been placed close to each other so that light intensity gradients are reduced. Additionally, power dissipation has been minimized by disconnecting current bias sources when circuits are not operating.

Figure 4 shows the simulated outputs given by the SIP for a 64×64 input image (Figure 4-a) exhibiting 4 distinct regions of constant intensity. For the sake of clarity, we use an image with vertical edges but with varying peak intensity. The first region corresponds to a 20mV swing at the photodetector sensing node whereas the swing is 40mV in the second region, 80mV in the third and 160mV in the fourth region. Thus, the voltage at the sensing node is doubled from one region to the next and so is the pixel output current as can be seen in Figure 4-a. Note that the value of the photocurrent, inducing each voltage swing at the sensing node N, is given in Figure 1. For instance, a 20mV voltage swing corresponds to a 20pA photocurrent whereas a 160mV voltage swing at the sensing node would be due to 4 decades variations in photocurrent.

The SIP weighted current sum over a 5×5 processing window is shown in Figure 4-b. One can see that the dynamic range remains unchanged if the SICNN weight coefficients w_j are chosen appropriately. Moreover, dynamic range compression can be achieved [4][5]. The SICNN output for the entire input image is given in Figure 4-c. If we consider one row of the SICNN output (Figure 4-d), we can see that the contrast is preserved even though the light intensity is doubled from one region to the next. The SICNN response adapts to the mean input photocurrent intensity via the gain control mechanism [4][5] described in Section 2. It is this feature coupled with a logarithmic pixel architecture that is exploited in this wide dynamic range CMOS imager.
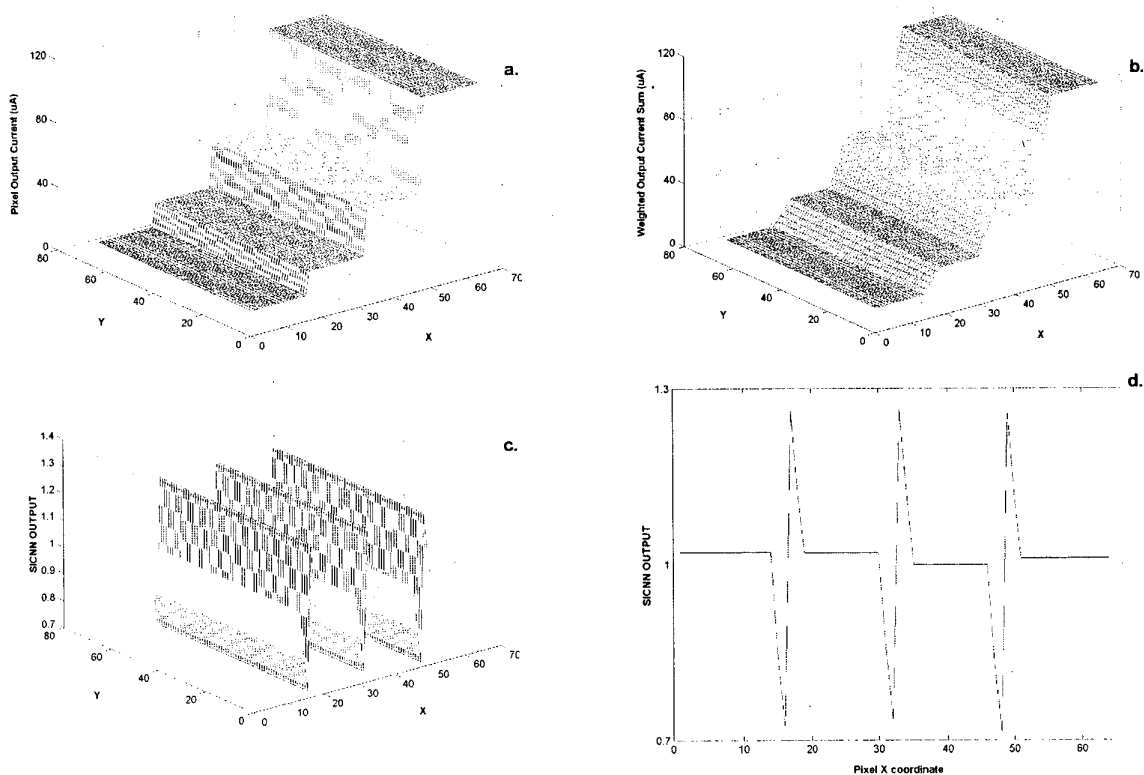
Figure 4. Simulated results from the Shunting Inhibitory Processor **(SIP):** **a.** Pixel output current for 4 decades variations in photocurrent; **b.** Weighted ($w_j = 1/25$) output current sum as performed by the SIP; **c.** SICNN output for the entire input image; **d.** SICNN output for one row of the input image showing the transition from one region to the next.

5. CONCLUSION

A wide dynamic range CMOS imager has been designed in full custom 0.7μm CMOS technology at a 30μm pitch. It can achieve various image processing tasks as image enhancement or edge detection via a programmable shunting inhibitory processor. Its implementation is based on a novel mixed-mode VLSI approach, which uses pixel output current readout to achieve analog and digital processing of the pixel array outputs. As a result, the proposed architecture is shown to be very compact and flexible as the shunting inhibition weights and a user-defined window can be selected externally. Its most important feature is a gain control mechanism, which enables the sensor to adapt to various input conditions. Image contrast can thus be preserved over 4 decades variations in light intensity.

6. ACKNOWLEDGEMENTS

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