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Alistair J. Kitchen
Edith Cowan University

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CMOS Digital Pixel Sensor Array with Time Domain Analogue to Digital Conversion

By

Alistair J. Kitchen

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Principal Supervisor : Assoc. Prof. Abdessalam Bouzerdoum

Co-Supervisor : Dr Amine Bermak

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I certify that this thesis does not incorporate without acknowledgement any material previously submitted for a degree or diploma in any institution of higher education; and that to the best of my knowledge and belief it does not contain any material previously published or written by another person except where due reference is made in the text.

Publications

A 64×64 CMOS digital pixel array based on pulse width analogue to digital conversion, with on chip linearising circuit. *Proceedings of SPIE*, volume 5274, December 2003.

Time domain analogue to digital conversion in a digital pixel sensor array. *Proceedings of IEEE, International Workshop on Electronic Design, Test and Applications*, January 2004.

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Abstract

This thesis presents a digital pixel sensor array, which is the first stage of an ongoing project to produce a CMOS image sensor with on-chip image processing. The analogue to digital conversion is performed at the pixel level, with the result stored in pixel memory. This architecture allows fast, reliable access to the image data and simplifies the integration of the image array and the processing logic.

Each pixel contains a photodiode sensor, a comparator, memory and addressing logic. The photodiode sensor operates in integrating mode, where the photodiode junction capacitance is first charged to an initial voltage, and then discharged by the photodiode leakage current, which is comprised mainly of optically generated carriers. The analogue to digital conversion is performed by measuring the time taken for the photodiode cathode voltage to fall from its initial voltage, to the comparator reference voltage. This triggers the 8-bit pixel memory, which stores a data value representative of the time. The trigger signal also resets the photodiode, which conserves the charge stored in the junction capacitance, and also prevents blooming. An on-chip control circuit generates the digital data that is distributed globally to the array. The control circuit compensates for the inverse relationship between the integration time and the photocurrent by adjusting the data clock timing. The period of the data clock is increased at the same rate as the integration time, resulting in a linear relationship between the digital data and the photocurrent.

The design is realised as a 64 × 64 pixel array, manufactured in 0.35μm 3.3 V CMOS technology. Each pixel occupies an area of 45μm × 45μm with a 12.3% fill factor, and the entire pixel array and control circuit measures 3.7mm × 3.9mm.

Experimental results confirm the operation of the digital pixel, and the linearising control circuit. The digital pixel has a dynamic range of 85dB, and can be adapted to different lighting conditions by varying a single clock frequency. The data captured by the array can be randomly accessed, and is read from the array nondestructively.

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Chapter 1

Introduction

The capturing and processing of images has undergone a revolution in recent years. Personal computers have become commonplace, in turn creating a demand for digital cameras. While these commercial devices have increased remarkably in quality and resolution, they are primarily intended for the production of high quality images and have many drawbacks when they are applied to the task of image processing, particularly in real time. At the heart of this problem is the incompatibility of the processes used to manufacture different sections of the camera. Light sensing is generally performed by a *Charge Coupled Device* (CCD) array, while control, memory and processing is performed using digital *Complementary Metal Oxide Semiconductor* (CMOS) circuits. These systems must be manufactured separately and combined at the board level, resulting in increased production costs, and increased power consumption (an inevitable result of chip-to-chip interfacing). Aside from manufacturing problems, there are other issues relating to the inflexibility in the operation of CCD arrays that makes them less than ideal for applications requiring image processing. (These will be covered more fully in Chapter 2.)

With technology scaling resulting in CMOS devices with sub-micron feature sizes, a preferred solution is to construct the sensor array from the same CMOS technology as the control circuits, employing either *Passive Pixel Sensors* (PPS) or *Active Pixel Sensors* (APS). In this way the light sensing array is integrated with the control circuit in a single *Integrated Circuit* (IC) resulting in the so called 'camera on chip' [11]. The main challenge in this approach is how to convert the image

represented by analogue voltages to a digital value, while maintaining the speed, low noise, and low power consumption that this technique promises. Exploiting the reduction in feature size further, results in the *Digital Pixel Sensor* (DPS), which attempts to overcome some of the weaknesses of earlier designs by digitising the image at the pixel level. This architecture presents its own challenges, many of which are yet to be overcome.

1.1 Thesis Objectives

The objective of this thesis is to develop and test a DPS sensor array, manufactured using a commercial CMOS process. The sensor is to operate over a wide range of illumination robustly, with minimal external control or timing. The digitised image is to be read from the array non-destructively, as if the array was a *Read Only Memory* (ROM) (the control circuit will not be able to write back to the array).

To this end a new implementation of single slope conversion will be presented, which employs time as the conversion variable, rather than voltage. This will allow the *Analogue to Digital Conversion* (ADC) process to be distributed between the control circuit and the pixels themselves. Unlike other forms of single slope conversion, the image is digitised during the exposure period, simplifying the control sequence. This also results in a digital 'electronic shutter speed' control, analogous to the shutter speed setting in a traditional camera.

1.2 Thesis Organisation

Chapter 2 introduces the subject of image sensor arrays, and compares CCD and CMOS pixel sensors, highlighting the advantages of each technology. Current work on CMOS sensor arrays, and in particular DPS arrays is reviewed. Chapter 3 develops a simplified model for the semiconductor sensor element, and uses this to determine the timing and control requirements for the analogue to digital conversion scheme, which is confirmed by simulation. An architecture for the pixel and the control circuit is proposed which is suitable for realisation in digital CMOS

technology. Chapter 4 develops these architectures into working circuits, suitable for manufacture using a standard digital CMOS process. This includes both the schematic design and the hardware layout of the DPS array, and the supporting circuits required to operate it. The system is simulated to confirm the operation of the array, and the time domain ADC process. The manufactured DPS array is tested in Chapter 5, which describes the operation, the test environment, and the test procedures. Results of testing, and sample images are presented. Chapter six concludes the thesis, and discusses future work.

Chapter 2

Review of Digital Image Sensors

2.1 Introduction

This chapter reviews the current state of image sensors, comparing the advantages of each, and how these determine their appropriate use. Terminology particular to image sensor design is also introduced, in order to address and compare important features of each approach.

2.2 Charge Coupled Device Sensors

CCD sensors have been the primary technology for solid state image sensor arrays since their development in the late 1960's. Today they are the sensor of choice for high resolution (both spatial and signal) image sensors. A CCD pixel cannot be considered in isolation, and must be considered as part of a series of pixels, formed from MOS capacitors. Consider Figure 2.1 as part of a row of pixels in a CCD array, with the gates G1, G2 and G3 repeated in sequence along the row. Placing a positive voltage on a gate will deplete p-type substrate around the gate of carriers. Carriers may then be generated thermally, or through interaction with incident photons, optically within the depletion region. The positive potentials are applied to the gates as a series pulses, beginning with G1. Due to the positive potential applied to G1, any carriers that have been thermally or optically generated in the region are trapped within a 'potential well' as a 'packet' of charge. If a second positive pulse

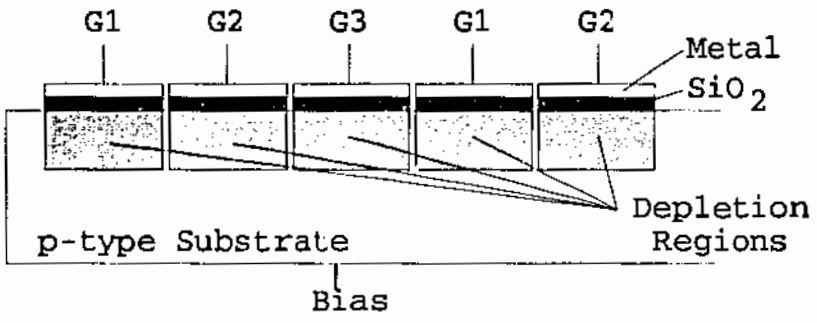


Figure 2.1: Simplified CCD structure, showing a cross section of part of one row. In this example three clock phases are required, each being distributed in turn to the cell gates.

is then applied to the adjacent gate, G2, some of the charge from under G1 will be transferred, and shared between the two MOS capacitors. If the potential on G1 is then removed, all of the charge from the first cell will, in theory at least, transfer to the second cell. The process can then be repeated with G2 and G3, and so on. At the periphery of the array the charge is transferred to another CCD structure, perpendicular to the main array, which can then transfer the charges one 'packet' at a time to a charge amplifier, and from there to an ADC.

CCD's have evolved enormously, and the manufacturing processes for CCD's have become highly specialised. For example the p-type substrate can now be manufactured thin enough to be optically transparent, allowing the array to be 'backside' illuminated. This means that none of the array is obscured by metal contacts, and all of it can generate carriers, increasing its efficiency. As an example, Tower et al. describe a five megapixel, backside illuminated CCD array for used for space surveillance [17].There is little doubt that CCD sensors will continue to be the technology of choice for high sensitivity, high resolution image sensors for some time.

However, from this simplistic description of the CCD operation some of its major drawbacks can be highlighted. The CCD array requires a great deal of switching, as the images must be shifted out pixel by pixel, column by column, row by row. The reading is destructive, requiring external memory to store the image. The timing, conversion and memory circuits must be fabricated on a separate IC, as the CCD

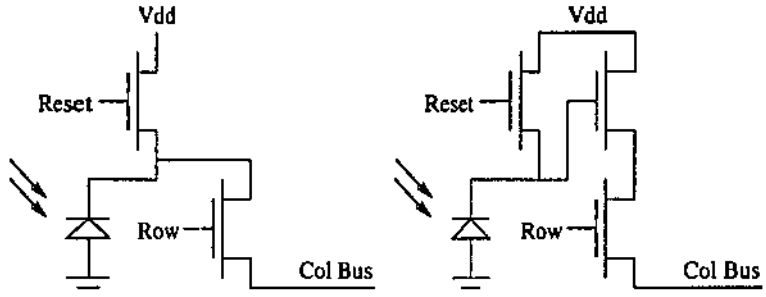


Figure 2.2: (i) Passive Pixel Sensor (PPS). (ii) Active Pixel Sensor (APS). Although showu with photodiodes, photogates can also be used in direct integratiou mode.

manufacturing process is unsuitable to manufacture these devices. This amount of switching activity combined with chip interfacing results in a complex control circuit, slow readout and high power consumption.

2.3 Passive and Active CMOS Sensors

CMOS photo-sensors are formed either from the source/substrate junction of a CMOS transistor (a photodiode), or from the depletion regiou formed at the gate of the transistor (a photogate). (The strncture and performance of these will be examined in detail in the next chapter.) The most common mode of operation is termed 'direct integration'. Put briefly, the reverse biased diode can be considered a system with two parallel components: a current source which is proportional to the illumination, and a capacitance formed by the p-n junction depletion region. To operate in integration modc, the cathode of the diode is first connected to a 'reset' voltage, which rapidly charges the depletion capacitauce. The voltage is then disconnected, and the leakage current, which is mainly due to optically generated carriers, will discharge the capacitor linearly over time. This process 'integrates' the photocurrent over the integration period, and the voltage present at the end of the period is inversely proportional to the illumination (a high illumination results in a low voltage). This voltage is then connected to an ADC, and converted to a digital value. In a (PPS) such as that of Figure 2.2(i), the photodiode is connected

to a charge amplifier, via a row selection transistor and a column bus line, and from there to the input of an ADC. In any CMOS circuit long bus lines represent a large capacitive load, and connecting the sensor results in charge sharing, and significant signal attenuation. To alleviate these effects the APS includes a single voltage follower in each pixel as per Figure 2.2(ii), to increase the ability to drive the bus impedance [11]. Sufficient time must still be allowed for the small voltage follower buffer to charge the large capacitance of the column select line. This is the limiting factor for the image acquisition rate.

2.3.1 Analogue to Digital Conversion

In any solid state array the main challenge is how to convert the analogue signal level present at the sensing element to a digital value, or how to route the sensor to the ADC. The ADC method employed in a CMOS or CCD sensor array depends upon the application and the architecture of the array. An array level ADC (the ADC is shared by the entire array) must digitise one pixel signal at a time, and to maintain a reasonable readout speed, is typically of the flash or half-flash type. These consume large silicon areas, and an acceptable trade off is to provide an ADC of a slower, and physically smaller design, at the column level.

2.3.2 Fixed Pattern Noise

Regardless of the pixel or array design, all CMOS image sensors suffer from *Fixed Pattern Noise* (FPN). Each device created on an integrated circuit has certain characteristics that determine its performance, such as its threshold voltage or terminal capacitance. A commercial CMOS manufacturing process allows for a range of device characteristics which are considered acceptable. These are typically within 2 to 3 standard deviations of the mean, assuming a normal distribution of device parameters [19]. Steps can be taken to minimise the impact of this 'process variation' on the performance of the pixel array, in particular one technique called *Correlated Double Sampling* (CDS). In this technique, the pixel voltage is sampled immediately after reset, and the value stored in a MOS capacitor (at the column level). After the

integration period the pixel voltage is again sampled and the difference between the two signal levels is digitised. This effectively reduces offset FPN due to variations the column selection and buffering circuits, but cannot remove multiplicative FPN due to amplifier gain [11] [7] [5].

2.3.3 Temporal Noise

There are three main sources of temporal noise in a CMOS sensor: shot, thermal and $\frac{1}{f}$ noise. A detailed analysis of these noise sources is beyond the scope of this review, suffice it to say that temporal noise determines the low illumination limit of the sensor [16]. In addition to the noise present in the photo-detector any additional circuitry (such as reset, follower and selection transistors) will also introduce noise. Considering only the photodiode itself, shot noise is the most significant noise source. CDS can also alleviate some temporal noise sources (thermal, reset and $\frac{1}{f}$) [11] [5].

2.3.4 Fill Factor

As additional circuitry is included within the pixel, less and less of the sensor area is devoted to capturing light, which is after all the main purpose of the array. The *Fill Factor* (FF) is the ratio of the light sensitive area to the total area of the pixel, or in some cases, of the array. As stated in the previous section, modern CCD sensors achieve a fill factor of 100%. CMOS PPS sensor arrays sacrifice light sensitive area to selection transistors, power and signal lines, and achieve typically 60 to 70% FF. APS arrays, having the additional buffer transistor, generally achieve 50 to 60% FF.

2.3.5 Spatial Resolution

The sensor array samples an image spatially, and normal sampling theory applies. Given an array with pixel pitch 'x', the Nyquist frequency for the array is $\frac{1}{2x}$ (the pitch is taken as the distance between pixel centers). When an image is focussed upon the sensor array it may contain spatial frequencies which are higher than the Nyquist frequency. For example, a scene may contain dark and light bands which are separated by tens of centimeters, but when focussed down upon the array may

be separated by tens of microns, and are below the pixel pitch. In this case aliasing of the image will occur. The Nyquist frequency is an ideal figure, and the sensor performance is usually less than this.

2.4 Digital Pixel Sensors

A DPS is one in which the analogue to digital conversion is performed at the pixel level. While it is not entirely accurate to state that each pixel contains an ADC, each does contain circuitry which, with the addition of some externally generated signals, can perform the conversion and either transmit or store the result. The reasoning behind this design is that the sacrifices made in the spatial resolution and fill factor will be offset by the improvements in readout speed and dynamic range that come with a minimal signal path. Also, having fast, random access to the array has advantages when processing the image data.

2.4.1 Near Sensor Image Processing

As early as 1994 Forchheimer demonstrated the advantages of processing images at the pixel level [6]. This was a purely theoretical approach with little consideration being given to the ability to realise the hardware with the technology of the day. It was proposed that each pixel could contain a photodiode (operating in integrating mode), a comparator, memory, and a simple digital processor, termed a *Sensor Processing Element* (SPE). The SPE exploited the 'analogue-temporal behaviour' of the photodiode to perform simple image processing operations, including gradient thresholding, histogramming, and median filtering. The goal of a processor per pixel has been at least partially realised by Komuro and Ishikawa [9]. Several issues were raised however, in particular a lack of sensitivity, suggesting local memory and external processing may be a more practical approach. More recently Wandell, Girod, and El Gamal [18] have argued the advantages of local memory, and its importance to sensors which mimic biological vision. Examined from a purely functional level,

the advantages of having memory local to the pixel can be demonstrated by considering some basic image processing techniques. Convolution is one of the most common techniques applied in image processing, and in two dimensions is defined by the equation:

$$H(i,j) = F * G = \sum_m \sum_n F(m,n)G(i-m, j-n) \tag{2.1}$$

where H is the convolution of the image G with function F. A typical application may be the convolution of an image with a rectangular pulse, for 'smoothing' or low pass filtering. It can be seen from this equation that the operation involves addressing each pixel in turn, and repeatedly accessing pixels in the immediate region. Implementing such a system with a CCD, or even an APS sensor array would require a) capturing the image, b) digitising the analogue levels, c) transferring the values to external memory, and d) repeatedly accessing this stored image. Applying a DPS array with local memory to the same task removes steps b) and c), and the need for a secondary image memory. Only memory snfficient for the immediate processing is required, determined by the dimensions of function F(m,n). Also, as the structure of the array memory naturally follows the structure of the image, the task of addressing is simple, and the pro~ssing can be implemented with minimal hardware (or firmware).

Alternatively, DPS arrays can be applied to higher level processing, such as multiple capture dynamic range extension [18]. Multiple images, optimised for varying levels of illumination are combined to extend the intra-scene range of a composite image. DPS arrays, with wide inter-scene dynamic range, fast readout, and flexible control are the obvious choice for these more sophisticated systems.

2.4.2 DPS Architecture Review

Digital pixel sensors using direct integration can be broadly divided into two categories: those that integrate for a fixed period of time, and those that integrate to a fixed reference voltage. The first method is very similar in operation to the active pixel sensor, where after a fixed integration period the terminal photodiode voltage (which is inversely proportional to the photocurrent) is converted to a digital valne.

The array developed by Yang, Fowler and El Gamal contains elements typical of DPS arrays [20]. Four sensors (photodiodes) share a common comparator/latch pair. The array is divided into four 'frames', and although the pixels are exposed simultaneously, they are processed one frame at a time. In a technique described as *Multi-Channel Bit Serial*(MCBS), one photodiode is selected and the signal voltage compared with a reference. The comparison result (true or false) is stored in the latch and the array (one frame) is read. The reference is adjnsted and the comparison is repeated. The final pixel value is determined from the series of comparisons, in a manner similar to a snccessive approximation ADC. The entire procedure is then repeated for the other three photodiodes, and the final image constructed from the four 'frames'. Obviously the ADC method, and the framing technique both require significant post-processing in order to reconstruct the image. This method warrants inclusion in the DPS category as the pixel returns a digital value only (a single bit).

Similarly, the DPS array of KleinFelder, Lim, Liu and El Gamal shares a comparator and 8-bits of memory amongst four photo-gate sensors [8]. The use of a larger pixel memory (8-bit) allows a simpler, and faster, conversion strategy than the MCBS system. Gray encoded data is distributed throughout the array to the pixel memory, synchronised with an equivalent analogue ramp voltage which is distributed to the comparators. When the ramp voltage is equal to the pixel voltage, the data is latched into the pixel memory. The pixel memory array is read, the next frame of sensors is selected, and the procedure is repeated. Again, the image is reconstructed as a composite of the four frames. The ability to share common components amongst sensors in order to increase the fill factor is a distinct advantage of this style of ADC architecture, although complicating the external hardware, and control.

Using the integration time as the conversion variable is the method employed by the 'near sensor image processing' circuits described above [6] [9], using a connting loop within the pixel processor to measure the integration time. Alternative methods have been proposed by Bermak [2] whereby the pixel is permitted to self reset and free-run, the number of pulses produced within a fixed time period being counted and

stored locally. This method has been partially realised by Döge, Schönfelder, Streil and König in the construction of a single row of 128 'spiking' pixels [4]. Although showing excellent dynamic range performance (over 90dB), this circuit demonstrates the major drawback of this system: the power consumption. CMOS circuits consume power during switching, and a sensor array composed entirely of counters represents a great deal of switching activity.

The spiking pixel concept has been developed further by Culurciello, Etienne-Cummings and Boahen, in the 'biomorphic sensor'[3]. The free running pixels, which mimic the firing of biological cells, transmit their firing rate outside of the array using an 'address event' protocol. The address of the firing pixel is communicated out of the array using a complex bus arbitration system termed *Address Event Representation* (AER). The power consumption of the free running pixels is significantly reduced through the use of 'current feedback event generators', which are modified inverters employing positive feedback, used as the threshold detectors. The positive feedback dramatically reduces the transition time of the inverter, the region of operation where most of the power is consumed. Again, the pixel contains no memory, and in fact is not intended to be a DPS array, but a 'biomorphic' sensor. It has been included in this review only due to the many similarities it shares with some DPS designs.

2.5 Conclusion

This chapter has discussed how CMOS sensors are developing towards the ideal of a 'camera on chip': an entire image capturing system manufactured as a single integrated circuit. When the goal of the image capturing process is not just to render an image, but to make the information contained in that image accessible for processing, CMOS sensors show far more promise than their CCD counterparts. Digital pixel sensors are one member of this family that demonstrate a utility in general application that cannot be matched by their analogue predecessors.

Chapter 3

Time Domain Analogue to Digital Conversion

3.1 Introduction

This chapter begins by developing the model that is to be used to simulate the behaviour of the light sensing element within the pixel, taking physical parameters from a commercial CMOS process. This model is then used to derive a method for converting the integration time (described briefly in Section 2.3) to a digital value, giving consideration to the resolution, linearity, and speed of the conversion. Simulations of the conversion process are presented, taking actual images as input, which confirm the theory of operation. The implementation of the algorithm in hardware is then considered, and the conversion algorithm modified, in order to simplify the circuit design. The impact of this approximation, and the quantising process is again analysed, simulated and presented.

3.2 CMOS Image Sensors

There are two types of CMOS sensors commonly used in PPS, APS or DPS arrays: the photodiode and the photogate. The photogate sensor is formed from a modified *Field Effect Transistor* (FET), in which the source and drain regions are left 'floating', or unconnected to bias voltages. The gate of the transistor (an n-channel

device) is taken to a positive voltage, which repels the p-type carriers of the substrate below. This results in a depletion region, and hence a capacitance, which can be employed in manner similar to a CCD cell. The biased gate capacitance forms a potential well, which traps any optically generated carriers in the region under the gate. This charge is then transferred via an adjacent transistor to a smaller capacitive node, which effectively amplifies the voltage (as $V = \frac{Q}{C}$, with Q constant). From there the architecture is the same as the APS array, with the voltage being switched through to the ADC, via row and column selection transistors.

There are several reasons why the photogate is not considered a suitable sensing device for the digital pixel. The photogate displays approximately half the quantum efficiency of the photodiode, and is more susceptible to FPN [10]. Another important consideration is the more complex control sequence, when compared with the photodiode. This would require additional circuitry, or additional control lines, neither of which is desirable. The photodiode, operating in direct integration mode, is therefore considered a more suitable device.

3.3 Photodiode Model

The photodiode is a reverse biased p-n junction diode, which has been optimised for the collection of photons at the junction. It has the same characteristics as any junction diode, but is normally reverse biased, where the leakage current and junction capacitance are the characteristics of most interest.

When a p-n junction diode is reverse biased, the junction area becomes depleted of carriers and only a small leakage current flows, due to thermally generated carriers. In a photodiode the junction is exposed to light which also generates carriers that contribute to the leakage current. Given the correct geometry, the optically generated carriers dominate the leakage current to the point where the thermally generated carriers can be disregarded. The current in the device is given by [15]

$$I_D = I_0(e^{\frac{qV}{kT}} - 1) - I_{OP}, \tag{3.1}$$

where:

I_D: diode current,

I_0: zero bias current,

I_{OP}: optically generated current,

q: elementary charge = 1.60×10^{-19}C,

V: bias voltage,

k: Boltzmann's constant = $1.38 \times 10^{-}23$ J/K,

T: temperature in Kelvin.

Photodiodes are normally only operated with reverse bias, where V is less than zero. The factor multiplying I_0 is the temperature dependent leakage current common to all diodes, and can be disregarded in most cases as it is very much smaller than I_{OP}. However, it cannot be disregarded in cases of very low illumination, where it is comparable to I_{OP}, and for this reason it is referred to as the 'dark current' of the device. When calculating the optically generated current some assumptions are made:

- All light falling on the junction generates carriers.
- The diode is formed from an abrupt p-n junction.
- Induced carrier densities are very much less than the majority carrier densities.
- The dimensions of the diode are smaller than the diffusion lengths of the semiconductor.

It should be noted that the physical constants for junction depth, depletion width and p-well depth apply specifically to the Alcatel 0.35μm CMOS digital process [1]. The figures are either provided explicitly by the manufacturer, or are derived from the design simulation files. These files provide a range of figures termed 'slow', 'typical' and 'fast', to cover the variation in device characteristics inherent in the

CMOS VLSI manufacturing process. Unless otherwise stated the 'typical' figures are used. The current density J_{PH} for a given junction can be determined from [5]

$$J_{PH} = \frac{qF}{\alpha}\left(\frac{(1-e^{-\alpha x1})}{x1} - \frac{(e^{-\alpha x2} - e^{-\alpha x3})}{x3-x2}\right), \tag{3.2}$$

where:

q: elementary charge = 1.60×10^{-19}C,

$x1$: metallurgical junction depth, xj = 2.3×10^{-7}m,

$x2$: xj + the depletion width W, which is determined from the zero bias junction capacitance (refer Eq.(3.3))
= $2.3 \times 10^{-7} + 1.19 \times 10^{-7} = 3.49 \times 10^{-7}$m,

$x3$: p-well depth $\approx 4\mu$m,

F: photon flux (photons/m^2/s),

α: absorption coefficient of silicon = 0.6×10^6/m.

While this is not intended to provide a definitive value for the current, there are far too many assumptions and simplifications for that to be the case, it gives an estimation of the range of current that can be expected: femto, pico or micro-amps. The current density was estimated for full bias voltage and an illumination level of 500 lux (one lux (lx) = 683 W/m^2), and found to be approximately 193mA/m^2. (The illumination level that the sensor can be expected to operate in can vary by many orders of magnitude, from twilight to full sunlight. 500 lx is typical of office level illumination and is taken as a reasonable bottom-end figure). Assuming a pixel with an area in the hundred-μm^2 range results in an anticipated current of tens of pico-amp's.

The second important characteristic of the photodiode is the junction capacitance, which is a fundamental property of a CMOS device, and is well documented by the manufacturer. The junction capacitance is found by summing the capacitance due to the area and the sidewalls of the junction, given by [19]

$$C_J = (A \times C_{JA} \times (1 + \frac{V_J}{V_B})^{-M_J}) + (P \times C_{JSW} \times (1 + \frac{V_J}{V_{BSW}})^{-M_{JSW}}), \tag{3.3}$$

where

A: junction area in m^2,

C_{JA}: zero bias junction capacitance, per unit area = 8.86×10^{-4} F/m^2,

V_J: junction potential, taking V_{dd} = 3.3 V,

V_B: built in potential = 0.904 V,

M_J: grading coefficient of the junction = 0.369,

P: junction periphery in meters,

C_{JSW}: zero bias junction capacitance, per unit length sidewall = 2.65×10^{-10} F/m,

V_{BSW}: bnilt in potential of the sidewall = 0.894 V,

M_{JSW}: grading coefficient of tbe sidewall = 0.356.

For the 0.35μm process this can be simplified to:

$$C_J = A \times (501 \times 10^{-6}) + P \times (152^{-12})F. \tag{3.4}$$

Note that the full rail voltage was used in this and the previous calculation, as it is anticipated that this will be the worst case situation for the photodiode. Again for a photodiode of several hundred-μm^2 the capacitance will be in the order of approximately 150 fF, depending upon the shape. Figure 3.1 combines these two properties into an equivalent circuit, comprised of the leakage current I_D and the junction capacitance C_J, in parallel. The method of direct integration employs these two characteristics to convert the photocurrent to a proportional voltage. If a voltage V_C is placed across the reverse biased diode, the capacitance C_J will be rapidly charged. If the voltage is then removed, the capacitor will discharge, due to the leakage current. The diode is formed from the active region of an n-channel FET (the cathode), and the p-type substrate or well (the anode). The switch for charging the capacitance is formed from an n-channel FET, conveniently combining

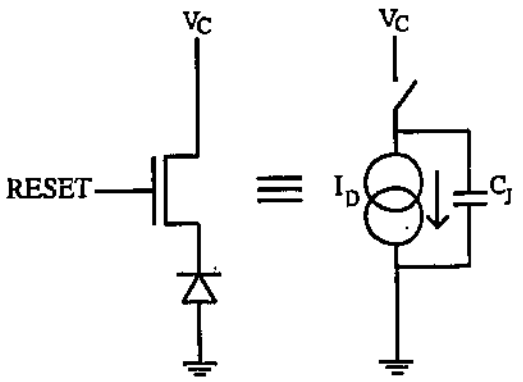


Figure 3.1: A photodiode and equivalent circuit.

the switch and diode in one component. From the familiar capacitor equation with discharge current I_D,

$$I_D = -C_J \frac{dV_C}{dt}. \tag{3.5}$$

Assuming that I_D is constant for a small value of dt this becomes

$$I_D = -C_J \frac{\Delta V_C}{\Delta t}, \tag{3.6}$$

therefore

$$\Delta V_C = -I_D \frac{\Delta t}{C_J}. \tag{3.7}$$

In a normal direct integration process the capacitor is allowed to discharge for some fixed period Δt. The change in the capacitor voltage is proportional to the optically generated current, and assuming this is large enough to disregard the dark current, is also proportional to the illumination. The voltage can then be converted to a digital value using any number of A-D conversion methods. If however ΔV_C is held constant, and Eq.(3.7) is rearranged to become

$$\Delta t = -C_J \frac{\Delta V_C}{I_D}, \tag{3.8}$$

it can be seen that the resulting integration time is inversely proportional to the illumination, and can be employed as the conversion variable in a digitising process.

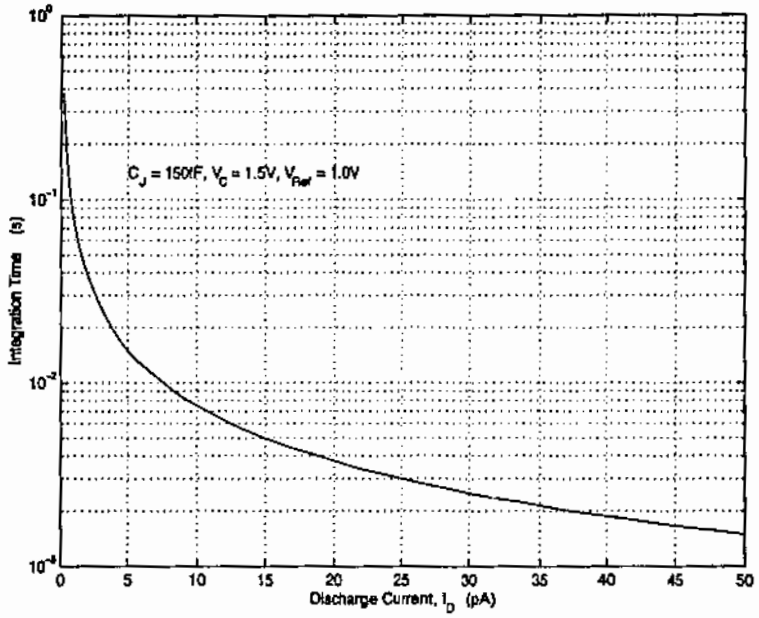


Figure 3.2: Integration time versus photocurrent, $C_J = 150$ fF, $\Delta V = 500$ mV.

Figure 3.2 shows the relationship between the integration time, and the photocurrent, for arbitrary, but realistic circuit values. The degree of nonlinearity in the relationship can be seen by the use of the logarithmic scale on the time (y) axis.

3.4 Time Domain Analogue to Digital Conversion

This section determines how the integration time can be used to produce an analogue to digital conversion of the illumination incident upon the photodiode. In order to digitise the integration time (and hence the photocurrent) several conditions must be met. If the illumination, and therefore the discharge current, is to be converted to a binary digit of b-bits, then the current can be expected to range from 0 to $(2^b - 1)\Delta I$ where ΔI is the smallest value of current that can be resolved. (That is, anything less than $\Delta I = 0$). Due to the inverse relationship between the integration time and the current, the minimum integration time, t_{min}, occurs with the maximum discharge current, I_{max}. It is proposed that the integration time be measured from an initial voltage V_C, to a second reference voltage V_{Ref}, using a binary counter to

count elapsed clock periods, hence digitising the integration period.

3.4.1 Primary Clock Frequency

The first step in digitising the integration time is determining the frequency requirement for the clock, given the resolution of the counter. Noting that the integration time and the discharge current are inversely proportional, a change in current of ΔI does not produce a linear variation of Δt. Therefore the smallest variation in the integration time that must be resolved occurs when $I_D = I_{max} - \Delta I$. Note also that because this is an inverse relationship, it is assumed in the following derivations that a down-counter is used, counting from $2^b - 1$ to zero. (This is a purely practical consideration, as this will produce a positive image when the data is read from the array.) If t_{min} represents the minimum integration time then

$$t_{min} = \frac{C_J(V_C - V_{Ref})}{I_{max}}, \tag{3.9}$$

and given that $I_{max} = (2^b - 1)\Delta I$, this becomes

$$t_{min} = \frac{C_J(V_C - V_{Ref})}{(2^b - 1)\Delta I}. \tag{3.10}$$

The smallest variation that must be resolved, Δt_{min}, is then given by

$$\begin{aligned}
\Delta t_{min} &= C_J(V_C - V_{Ref})\left(\frac{1}{(2^b - 2)\Delta I} - \frac{1}{(2^b - 1)\Delta I}\right) \\
&= C_J(V_C - V_{Ref})\left(\frac{(2^b - 1)\Delta I - (2^b - 2)\Delta I}{(2^b - 1)(2^b - 2)(\Delta I)^2}\right) \\
&= C_J(V_C - V_{Ref})\left(\frac{1}{(2^b - 2)(2^b - 1)(\Delta I)}\right) \\
&= \frac{t_{min}}{(2^b - 2)}.
\end{aligned} \tag{3.11}$$

If this is taken as the period of the clock t_{clk}, then the clock frequency is given by

$$f_{clk} = \frac{2^b - 2}{t_{min}}. \tag{3.12}$$

This will be referred to as the primary clock frequency. It can be seen from Eq.(3.12) that the clock frequency required for a given resolution is dependent upon the minimum integration time, which in turn is dependent upon the illumination. Put

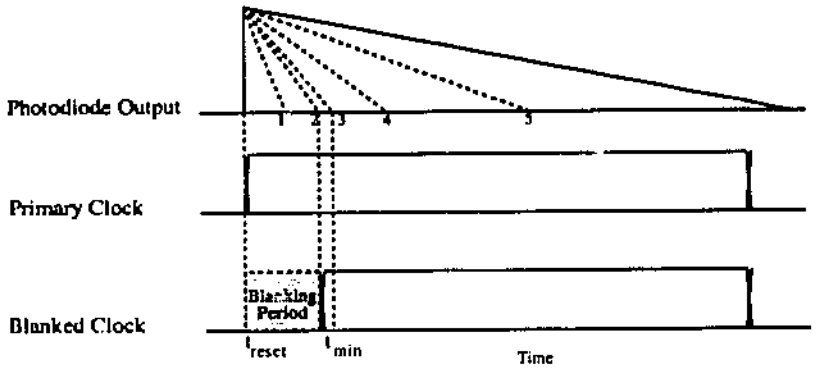


Figure 3.3: Timing diagram, showing the blanking period and a range of discharge curves. High illumination causes faster discharging of the photodiode, and shorter integration periods. The choice of f_{clk} sets the blanking period which determines the highest illumination level, and also the smallest change in illumination, that can be resolved.

another way, the clock frequency can be used to adapt to varying lighting conditions, resulting in an 'electronic shutter speed' control. High light levels require high clock speeds, which result in short exposure times. Low light levels require slower clocks, and longer exposure (integration) times, analogous to a traditional camera.

3.4.2 Minimum Integration Time Offset

It was shown in the previous section that the primary clock frequency can be set to determine the minimum integration time that will be resolved. Any integration time shorter than this interval is considered over-range, and must be ignored. Therefore the start of the clock should be offset, or 'blanked' for a period of time equal to the minimum integration time. As the clock frequency is derived from the minimum integration time, so in turn the blanking period t_{blank}, can be derived from the primary clock as

$$t_{blank} = t_{clk}(2^b - 2). \tag{3.13}$$

When the photodiode commences to discharge, the blanking counter will count the clock pulses. The value $2^b - 2$ is decoded and used to enable the conversion counter, which then measures the conversion time, $t_{int} - t_{blank}$. Figure 3.3 demonstrates the timing involved in the conversion process. The figure shows the photodiode output

voltage (top), the primary clock (center), and the blanked clock (bottom). The five curves in the top figure (the photodiode output) represent different discharge currents within a scene. Curve 1 represents a photocurrent too high to be in the conversion, and its integration time falls during the blanking period. This pixel stores the reset value of the counter. Curve 2 represents a pixel triggering at the minimum integration time, and also stores the reset value of the counter. Curve 3 is the minimum step size that is resolved, where the photocurrent has changed by ΔI, and the Gray counter has decremented by one. The difference between curve 4 and curve 5 is also ΔI, but because of the nonlinear response the increase in the integration time has changed dramatically.

3.4.3 Linear Conversion

As shown by previously in Eq.(3.8) and in Figure 3.2, the integration time is inversely proportional to the discharge current, and the affect that this has upon the conversion is significant. With a fixed clock the conversion counter will overflow long before the appropriate integration time has elapsed. This can be demonstrated by example. In order to produce a realistic simulation, a two dimensional array is created, each element of the array representing a pixel, with an associated discharge current. This is done by taking a grey scale bitmap image (in this case 8-bit) and adding a random fractional value to return the image to pre-quantised levels. These values are then multiplied by ΔI to produce an array of simulated discharge currents. The current array is then converted to equivalent integration times, assuming arbitrary, but realistic, values for V_C, V_{Ref} and C_J. The counting process is simulated by dividing each integration time in the array by the clock period, then rounding the result down to an integer value.

For the following simulations the quality of the conversion process is indicated by the signal to noise ratio. If $Image(m,n)$ is the input image of dimension $M \times N$, and $Image'(m,n)$ is the output from the simulated conversion, then the signal to

Figure 3.4: River.bmp: test image input for the simulated A-D conversion algorithm.

noise ration is given by

$$SNR(dB) = 10log\left(\frac{\frac{1}{MN}\sum_{m=1}^{m=M}\sum_{n=1}^{n=N} Image(m,n)^2}{\frac{1}{MN}\sum_{m=1}^{m=M}\sum_{n=1}^{n=N}(Image(m,n) - Image'(m,n))^2}\right) \quad (3.14)$$

where the denominator represents the mean square error between the input and the output. The smaller the error between the input and the output, the higher the signal to noise ratio.

Figure 3.4 is the original 8-bit grey-scale image. Figure 3.5 is the image converted using a fixed clock frequency, without a blanking period. Figure 3.6 plots the digital value against the discharge current, note that only the highest current at the extreme right of the plot has been converted to a digital level of '1', as the count has overflowed (reached zero) for all but the highest currents. (The bright spots in Figure 3.5 represent a level of '1', and are exaggerated in the display.) This conversion results in an SNR of -23.6 dB. Figure 3.7 simulates the conversion using a fixed clock frequency, but this time with a blanking period. The counter, driven

by the fixed clock quickly overflows as the nonlinear integration time increases, as shown in Figure 3.8. The linear clock conversion with blanking increases the SNR to -17.4dB.

If a linear conversion is to be performed, the period of the clock driving the conversion counter must be increased at the same rate as the integration time. While this could be performed through some analogue means, it is considered preferable to derive the clock period from the conversion count. In this way the range of illumination over which the conversion takes place is still determined by a single parameter: the primary clock frequency. By varying this one factor all other timing control will follow.

Let t_{int} represent the entire integration time from the moment that the junction capacitance begins to discharge, and the counters are reset. Let t_{conv} represent the period in which the conversion counter is enabled, $t_{int} - t_{blank}$. Recalling that the blanking period is the minimum integration period, where $I_D = I_{max}$,

$$t_{conv} = \frac{C_J(V_C - V_{Ref})}{I_D} - \frac{C_J(V_C - V_{Ref})}{I_{max}} \tag{3.15}$$

$$= C_J(V_C - V_{Ref})\frac{(I_{max} - I_D)}{I_{max} I_D}. \tag{3.16}$$

Taking the derivative of this with respect to I_D yields

$$\frac{dt_{conv}}{dI_D} = \frac{-C_J(V_C - V_{Ref})}{{I_D}^2}. \tag{3.17}$$

The smallest variation in I_D that can be resolved is ΔI, so the continuous variables are replaced with their discreet equivalents, with N_i being the index, and $I_D = N_i \Delta I$ ($1 < N_i < 2^b - 1$). Eq.(3.17 becomes

$$\frac{\Delta t_{conv}}{\Delta I} = \frac{-C_J(V_C - V_{Ref})}{(N_i \Delta I)^2}$$

$$\Delta t_{conv} = \frac{-C_J(V_C - V_{Ref})\Delta I}{N_i^2 \Delta I^2}$$

$$= \frac{-C_J(V_C - V_{Ref})}{N_i^2 \Delta I}. \tag{3.18}$$

Given that $(2^b - 1)\Delta I = I_{max}$, and $(2^b - 2)t_{clk} = \frac{C_J(V_C - V_{Ref})}{I_{max}}$, substituting and rearranging Eq.(3.18) leads to

$$\Delta t_{conv} = t_{clk}\frac{(2^b - 2)(2^b - 1)}{N_i^2}. \tag{3.19}$$

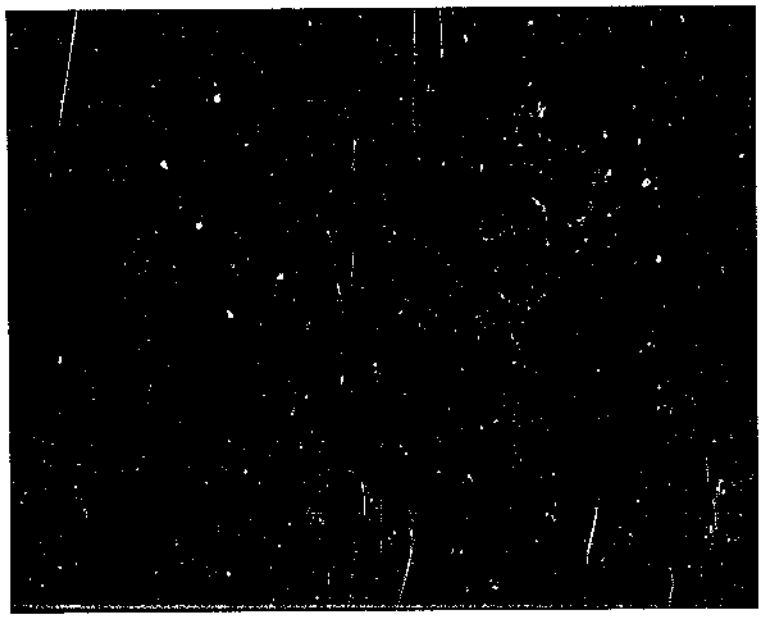


Figure 3.5: Simulated image conversion, without blanking, and using a fixed clock frequency.

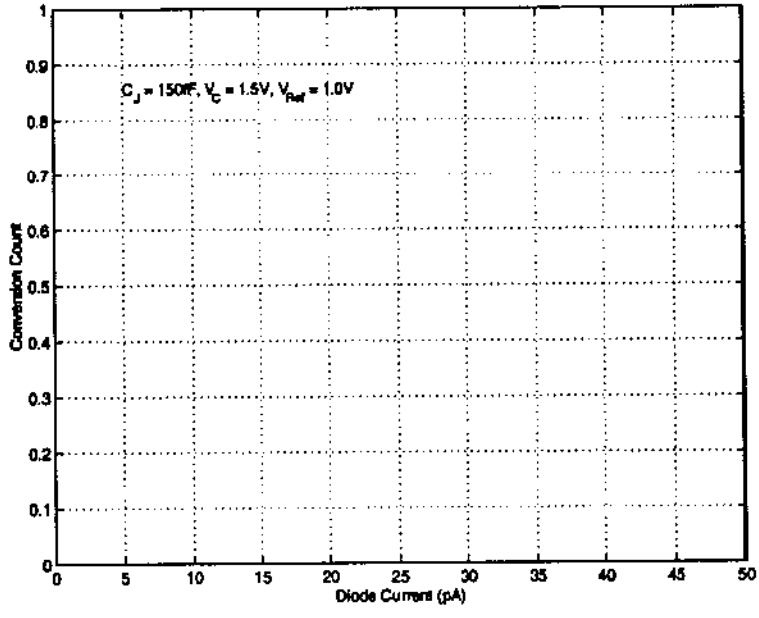


Figure 3.6: Conversion count versus photocurrent, without blanking, and using a fixed clock frequency. A single count has been resolved for the highest photocurrent, 50 pA.

Figure 3.7: Simulated image conversion, with blanking, and using a fixed clock frequency.

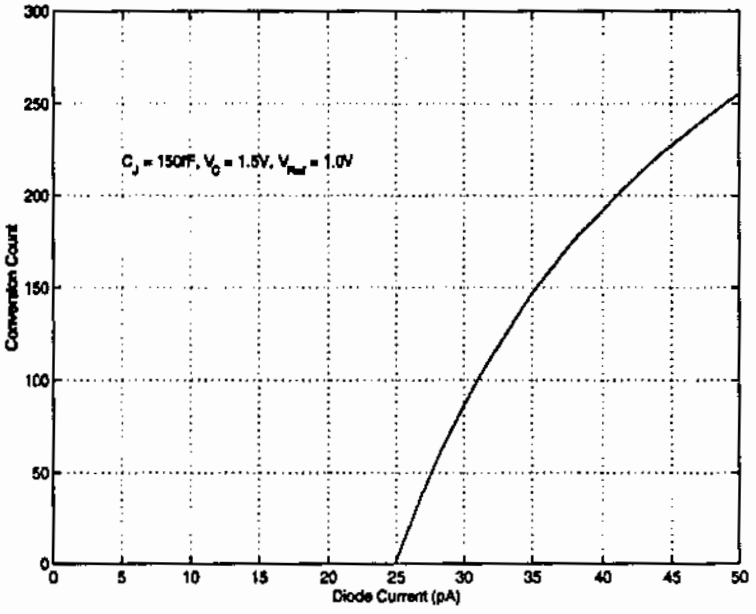


Figure 3.8: Conversion count versus photocurrent, with blanking, and using a fixed clock frequency. The highly nonlinear response results in a reduced intra-scene dynamic range.

This relates the change in t_{conv} to the equivalent digital value of the discharge current, as indicated by N_i. This means that the conversion time will increase by Δt_{conv} for each discrete step of the current ΔI. If a linear relationship is to be maintained between the discharge current and the count, then the period of the clock driving the counter must also increase at this rate. Let t_0 represent a fixed clock period determined in accordance with Eq.(3.12), while t_{clk} represents a variable clock period, used to drive the counter. Expressed as a function of the present count value, the clock period is given by

$$t_{clk}(N_i) = t_0\Big(\frac{(2^b-2)(2^b-1)}{{N_i}^2}\Big) \qquad (1 \leq N_i \leq 2^b - 1). \tag{3.20}$$

As stated previously, a down counter is used as the conversion counter; therefore, N_i can be directly replaced with the value of conversion count which will be termed N_t, resulting in

$$t_{clk}(N_t) = t_0\Big(\frac{(2^b-2)(2^b-1)}{{N_t}^2}\Big) \qquad (1 \leq N_t \leq 2^b - 1). \tag{3.21}$$

This achieves the desired result, where the variable clock period can be related to the primary clock period t_0, by the present value of the conversion counter. The extent of the nonlinearity can be seen, as the multiplier must be twice the resolution of the conversion clock ($(2^b-1)(2^b-2) \approx (2^b)^2 = 2^{2b}$).

Figure 3.9 shows a conversion of the original image, this time using an algorithm derived from Eq. (3.21). It can be seen that the deficiencies of the fixed clock have been overcome, the linearising process increasing the SNR to 22.8 dB, a 40 dB increase when compared to the fixed clock conversion. The correction can be seen more clearly in Figure 3.10, where a full range of currents, and hence illuminations, have been digitised (the same circuit values used in Figure 3.2 apply). There is now a linear relationship between the discharge current and the counter value. While this represents a relatively complex operation to be performed upon the clock, it has several desirable features. Firstly, it can be achieved digitally, using counters as frequency dividers. Secondly, this single clock source is distributed globally to all of the pixels in the array. Figure 3.11 represents the basic architecture of a single

Figure 3.9: Simulated image conversion, with blanking, and a variable clock frequency.

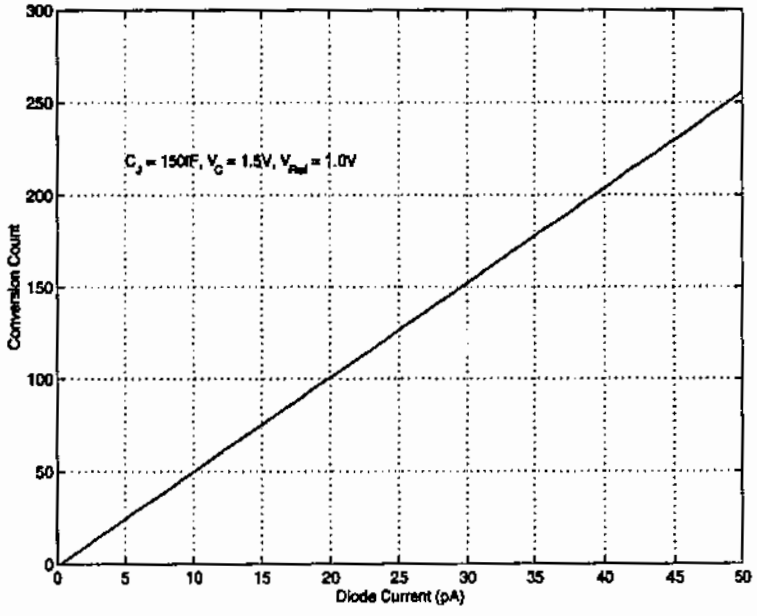


Figure 3.10: Conversion count versus photocurrent, with blanking, and a variable clock frequency, as given by Eq.3.21. Varying the clock frequency maintains a linear relationship between the count and the photocurrent.

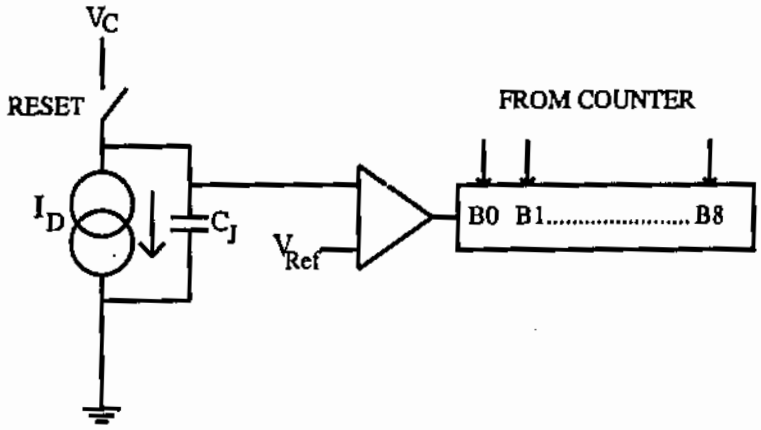


Figure 3.11: Pixel architecture, showing the key components: the photodiode (equivalent circuit), the comparator and the memory.

pixel. When the voltage on C_J crosses the threshold voltage, the value of the count at that instant is stored in local memory.

3.5 Conversion Error Analysis

From Eq.(3.20) it can be seen that the factor multiplying t_0, which will be referred to as M, although derived from integer values, is itself not an integer. However, if the variable clock is to be generated by a digital frequency divider (really just a counter), only integer values for M can be used. This leads to a difference between the ideal value of the multiplying factor M, given by

$$M = \frac{(2^b - 2)(2^b - 1)}{{N_t}^2} \qquad (1 \leq N_t \leq 2^b - 1), \tag{3.22}$$

and the realisable integer values derived from the frequency divider: 1, 2, 3 etc. This can be thought of as a quantisation error in the frequency division, and must be included in the error analysis of the conversion process. In order to analyse the extent of this error, and the affect that it has on the signal conversion, it is first necessary to explain how the frequency division is to be accomplished. Figure 3.12 represents the method proposed for generating the count data, and deriving the

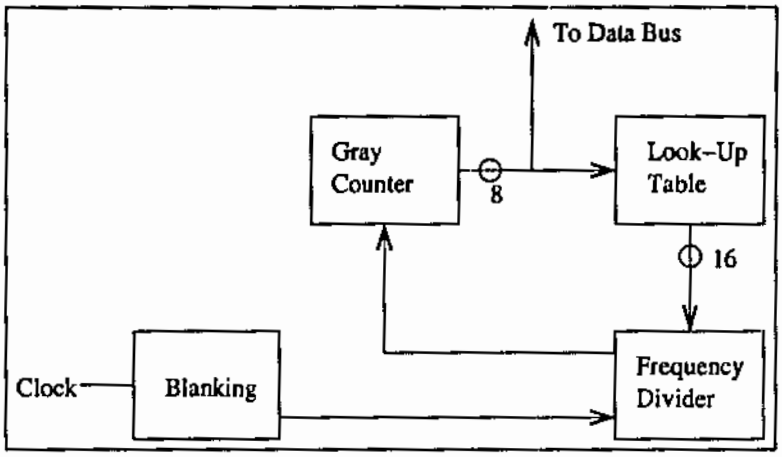


Figure 3.12: Control circuit block diagram, showing how the variable period clock is derived. The Gray counter output is distributed to the pixel array, via the data bus.

variable period clock, assuming eight bit resolution (b = 8). From Eq.(3.22) it can be seen that for every value of N_t there is a corresponding value of M. To simplify the hardware realisation, rather than provide a multiplier for every value of N_t, a multiplier is provided for small, continuous ranges of N_t. These multiplier values are stored in a 'lookup' table, which will output the value of M (in this case a 16 bit digit), given the current value of N_t. This multiplier value is then compared with the output of a 16-bit counter, which is driven by the primary clock. When these two values are equal, the data counter is clocked, and decremented to a new value. While this is more commonly referred to as frequency division, since it is a time period being considered in the conversion process, it is more appropriate to consider it a 'period multiplier'. The restriction upon this method is that the period of the variable clock period can only assume integer multiples of the primary clock period.

The conversion process can be thought of as approximating the actual conversion time t_{conv}, with a value t_{approx}, where $t_{approx} \leq t_{conv}$. The time t_{approx} can be considered the true conversion time plus three errors: the quantisation error e_q, the error due to rounding M to an integer value e_r, and the error due to approximating M in the lookup table, e_a. The approximation time is the integer sum of the clock periods up until the pixel triggers and stores the data counter value. For example, for any

digital value 'N' stored within a pixel, the approximated time that this represents is given by

$$t_{approx}(N) = \sum_{N_t=2^b-1}^{N} t_0 \frac{(2^b-1)(2^b-2)}{N_t^2} + e_a + e_r + e_q \qquad (1 \leq N_t \leq 2^b-1) \quad (3.23)$$

The result of using an approximate value in the lookup table will be examined first. Consider a small range of values of N_t, which in order to simplify the realisation of the hardware, all use the same multiplier value. The error e_a is the difference between the ideal value for the multiplier M, given in Eq.(3.22), and the actual value stored in the lookup table. For any value of N_t,

$$e_a(N_t) = (2^b-1)(2^b-2)\Big(\frac{1}{N_a^2} - \frac{1}{N_t^2}\Big). \quad (3.24)$$

The total error for a range of values approximated by N_a over the range $N = N_1 \rightarrow N = N_2$, is the summation of all the errors in the range. If the total error is expressed as E_a then

$$E_a = \sum_{N_t=N_1}^{N_2} (2^b-1)(2^b-2)\Big(\frac{1}{N_a^2} - \frac{1}{N_t^2}\Big). \quad (3.25)$$

It can be seen from Eq.(3.25) that if $N_a > N_t$, the error will he negative, and if $N_a < N_t$, the error will be positive. It should then be possihle to select N_a and the range of values $N_1 \rightarrow N_2$ such that the error will sum to zero over that range. This will prevent large errors from accumulating during long integration periods. If E_a is set to zero,

$$0 = \sum_{N_t=N_1}^{N_2} (2^b-1)(2^b-2)\Big(\frac{1}{N_a^2} - \frac{1}{N_t^2}\Big)$$

$$0 = \sum_{N_t=N_1}^{N_2} \Big(\frac{1}{N_a^2} - \frac{1}{N_t^2}\Big)$$

$$\sum_{N_t=N_1}^{N_2} N_t^2 = (N_2 - N_1 + 1)\frac{1}{N_a^2}$$

$$N_a = \sqrt{\frac{(N_2 - N_1 + 1)}{\sum_{N_t=N_1}^{N_2} \frac{1}{N_t^2}}}. \quad (3.26)$$

Using Eq.(3.26) values for N_1, N_2 and N_a can be determined iteratively. The error will increase monotonically until $N_t = N_a$, therefore the maximum error can be

found by calculating E_a for the range $N_1 \rightarrow N_a$. Limits can be placed either upon the size of the error, which varies the size of the lookup table, or the size of the range $N_2 - N_1$, which varies the peak error. Note that this error is systematic, and can be determined for all values of N_t.

While it is possible to use the method described above to limit the accumulation of e_a throughout the counting process, it is not possible to apply the same method to minimising the rounding error, e_r. Consider Eq.(3.22), with M set to the first boundary rounding point of 1.5,

$$1.5 = \frac{(2^b - 1)(2^b - 2)}{N_t^2} \tag{3.27}$$

As $(2^b - 1) \gg 2$,

$$1.5 \approx \frac{2^{2b}}{N_t^2} \tag{3.28}$$

and hence

$$N_t \approx \frac{2^b}{\sqrt{1.5}} \approx 0.816\ 2^b \tag{3.29}$$

This means for the first 20 percent of the conversion there is simply no alternative value of M that can be used apart from the smallest integer multiplier: $M = 1$. It is in this region that the largest overall deviations from the ideal multiplier value occur. Also as the rounding error, e_r, falls within the range of ± 0.5, this is where it is most comparable to the multiplier, and therefore most significant.

In any analogue to digital conversion process another source of error is quantisation noise, e_q. This occurs because there is only a finite number of digital values to describe the infinitely variable illumination level. In this case the error occurs when the integration time is digitised to a discrete value, which is marginally different from its true value. It must be noted that the approximation and rounding errors are fundamentally different from the quantisation error. The first two are systematic, and can be determined by comparing a given set of values from a specific design to the ideal situation (where they do not occur). They represent a nonlinear distortion in the transfer characteristics of the converter and do not add 'noise' as such. The nonlinearity at any point can be determined form

$$\mathrm{NL}(\%) = \frac{\text{Actual Value} - \text{Ideal Valne}}{\text{Full Scale}} \times 100 \tag{3.30}$$

The quantisation error e_q, occurs due to the conversion count representing a discrete time which is less than the true integration time by up to one clock period. The difference between the discrete and the analogue signals can be modelled as additive noise, and given certain assumptions, can be expressed as a signal to noise ratio SQNR, where [12]

$$\text{SQNR} = 6.02\text{b} + 1.25\text{db} \tag{3.31}$$

The linearising process does not affect the quantisation error, or the assumptions made in determining equation 3.31.

Using the above analysis, lookup table approximations were calculated for an eight bit resolution conversion. The approximation values were determined using an iterative process, executed in Matlab, in which the multiplier values were calculated for 28 approximated ranges, which are listed in Appendix A. The resulting transfer curve is shown in Figure 3.13, for which the following figures were calculated:

Maximum nonlinearity, NL(max) = 2.9 % @ $N_t = 209$.

Minimum nonlinearity, NL(min) = 0.

Average nonlinearity, NL(mean) = 0.64 %.

Quantisation error, 8-bit conversion, SQNR = 49.4 dB

Repeating the earlier simulations, this time using the 28 approximation values, the SNR was calculated to be 25.6 dB. This represents a 3dB improvement when compared with the conversion using all possible 255 multiplier values.

3.6 Data Encoding

In practice the count value to be stored in the pixel cannot be distributed to the pixels as binary code, due to the asynchronous nature of the pixel operation. If, for example, the count value was in transition from 127 (b 0111 1111) to 128 (b 1000 0000) there would be eight bits in transition. Depending upon the timing of the write signal, some of these bits may be stored as '1', others as '0'. This is a common problem

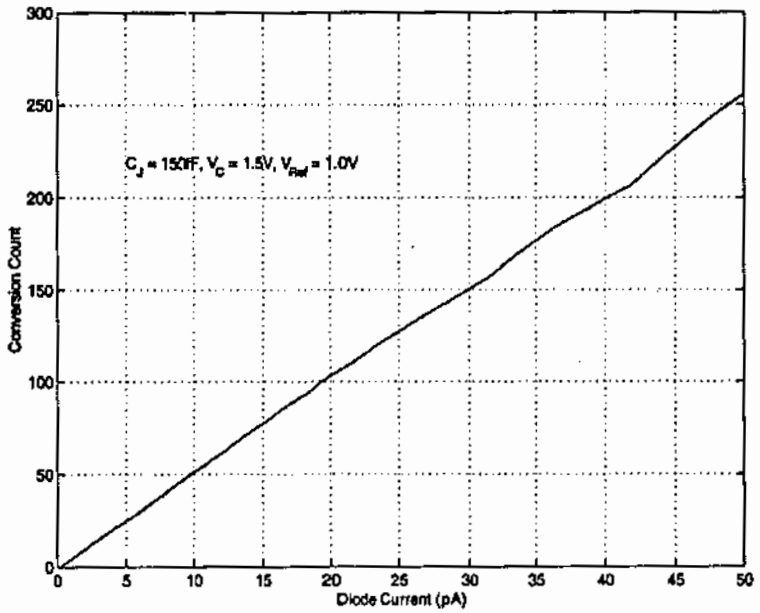


Figure 3.13: Conversion count versus photocurrent, with blanking, generating the variable clock using approximated multiplier values. Note the nonlinearities, particularly for high photocurrents.

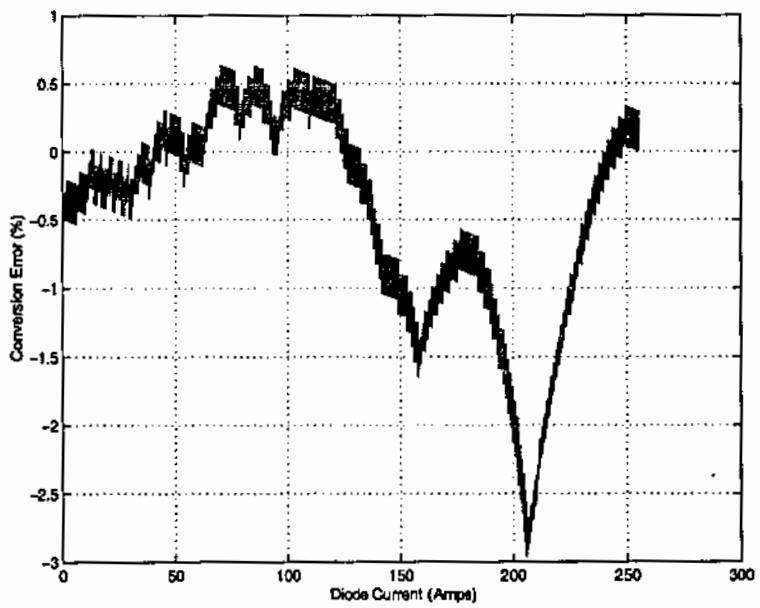


Figure 3.14: Nonlinearity error, using approximated multiplier values. The range and multiplier valnes are determined iteratively by computer simulation, to prevent the error accumulating with time.

in position sensing and encoding, and is usually resolved by the use of Gray code. This is an un-weighted code, not suitable for arithmetic, but designed so that only one bit changes at each step in the sequence. In this way if the triggering occurs during a bit transition, the count can only assume one of two possible adjacent values, both of which can be considered valid. Gray code can be derived from binary code by taking the exclusive OR of adjacent bits, save for the most significant bit, which is unchanged [14]. For example, if the binary bits are $b_0, b_1 ... b_n$, and the corresponding Gray bits are $G_0, G_1 ... G_n$ then

$$G_0 = b_0 \oplus b_1,\ G_1 = b_1 \oplus b_2,\ G_2 = b_2 \oplus b_3 ..... G_n = b_n \tag{3.32}$$

A secondary, but important advantage in the use of Gray code is the reduction in power consumption when driving the data bus. In any CMOS circuit, most power is consumed during state transitions, as capacitive loads are charged or discharged. With Gray code there is only one transition per clock cycle, as opposed to binary code where there may be up to eight. Taking the full range of 8-bit digits in sequence, and considering only transitions from '0' to '1' (where the bus line is charged), Gray code has 128 transitions ($0 \rightarrow 1$), compared to binary which has 256. While it cannot be claimed that this equates directly to a 50% reduction in power consumption, it does represent a significant improvement in the overall power consumption.

3.7 Conclusion

In this chapter the photodiode sensor was determined to be the most appropriate for the digital pixel sensor, due to it's higher efficiency and simpler control sequence. A basic model for the photodiode sensor was developed and analysed, taking parameters from the CMOS process employed to manufacture the device. Using the characteristics of this circuit model, a method for digitising the illumination by measuring the integration time was derived. This digitising process ensures that the full resolution of the conversion is realised by generating a variable period clock, which matches the integration mode characteristic of the photodiode. This was then refined to simplify the manufacture of the DPS array, by approximating the algorithm

with a series of discrete values, that could be stored in a look-up table. It was determined that in order to avoid errors caused by the asynchronous nature of the pixel triggering, that the data should be distributed in Gray code, rather than natural binary. Finally, the conversion process was verified by simulation, and simple circuit models for the pixel and control circuit presented.

Chapter 4

VLSI Implementation

4.1 Introduction

The circuit models used in the previous chapter were adequate to verify the principle of operation of the ADC scheme, but are simplistic in form. This chapter develops these simple models into practical circuits, with the ultimate aim of manufacturing a working DPS array. The chapter begins by proposing an architecture for the DPS array, with an overview of how the different parts of the array interwork. The schematic design of the array follows, beginning with the pixel, divided into separate analogue and digital sections. The analogue section of the pixel is responsible for the conversion of the photocurrent into a proportionally delayed pulse, while the digital section contains the memory and addressing circuits. The control circuit is then described, detailing how the variable period clock, introduced in the previous chapter, is implemented. Simulations are provided at each stage to verify the operation of the pixel, the control circuit and the overall system. Floor-planning and layout issues are then addressed for an array measuring 64×64 pixels, fabricated in a 0.35μm, 3.3V, digital CMOS process.

4.2 Array Architecture

To better describe the operation of the component parts of the array, it is first necessary to understand how the component parts interact. Figure 4.1 shows the

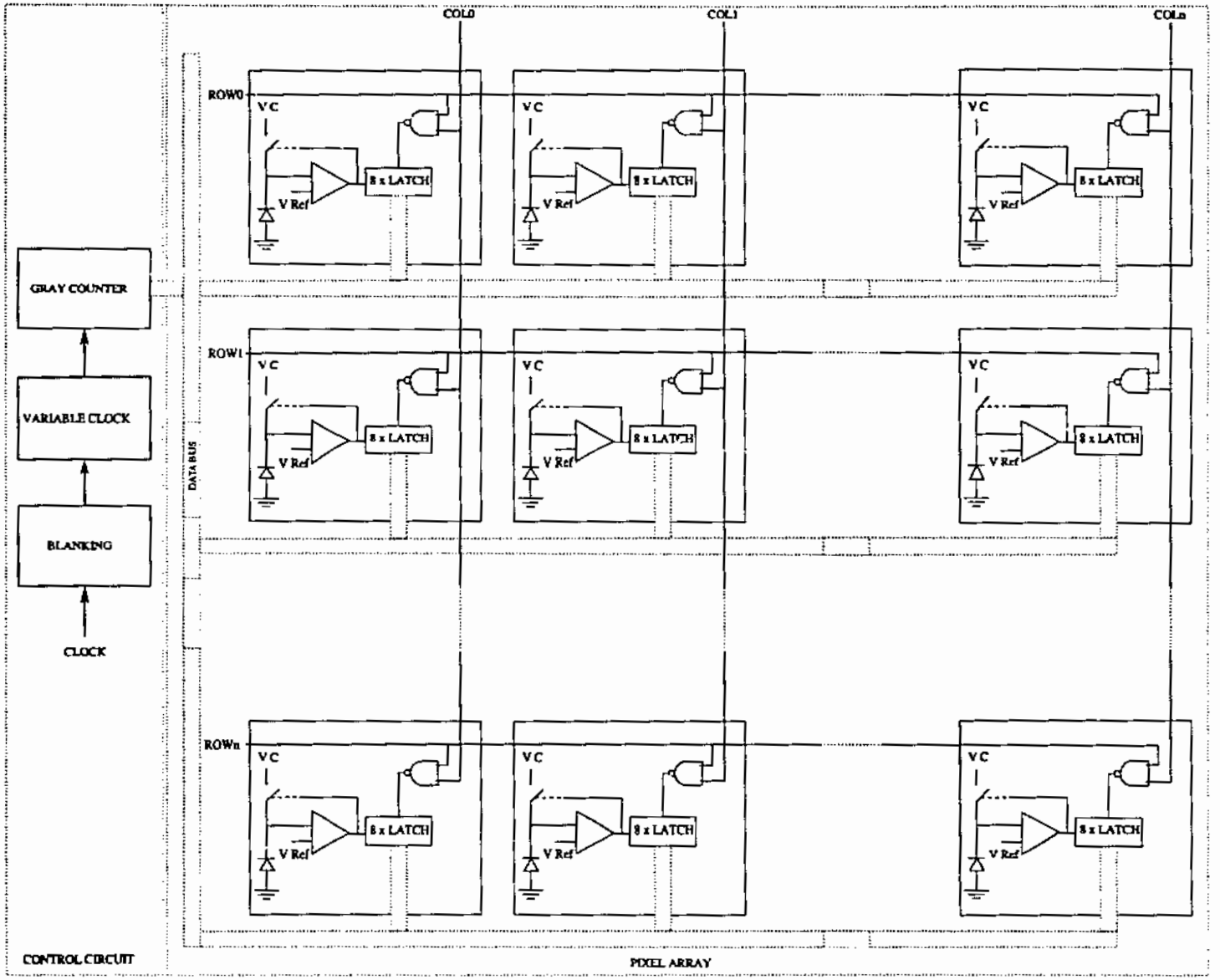


Figure 4.1: Proposed DPS array architecture. The data is generated by the control circuit, and distributed to the pixels over the input data bus. Each pixel can be individually addressed to retrieve the captured data.

proposed architecture of the array, with peripheral components, such as decoders and buffers, removed for clarity. Each pixel consists of a photodiode, a comparator, addressing logic, and memory. The data is generated centrally by the control circuit, in accordance with the principles outlined in the previous chapter, and distributed globally to the array. A reset signal simultaneously initialises the control circuit counters, and disconnects the pixel recharge voltage, commencing the integration period. Within each pixel, as the photodiode voltage falls below the reference voltage, the comparator triggers, and the data value present on the bus at that moment is stored within local pixel memory. After an appropriate exposure time (dependent upon the illumination), the control circuit generates a signal to indicate that the data counter has overflowed, and the data can be read from the array. Each pixel can then be addressed in turn by row and column address lines, and the data retrieved.

4.3 Pixel Architecture

The circuit used to model the pixel in the previous chapter is a simplistic one, consisting only of the following components: a photodiode, a reset switch, a comparator, and memory. While this was useful in order to describe the fundamental characteristics of the conversion process, there are additional control requirements that a realistic system must provide for robust and efficient operation.

It has already been shown that the control circuit must compensate for the $1/I_D$ nature of the integration time (Section 3.4.3). There is another issue that arises from the difference between the extremes of the nonlinear integration time, blooming. Blooming occurs when a photodiode continues to discharge beyond the point where it is reverse biased. The device may then draw charge away from adjacent pixels, degrading the image. Discharging the photodiode below the triggering point is also a waste of power, as the photodiode must be recharged before the next operation, and the junction capacitance is significant, in the order of 100 - 200 fF. Conserving this charge represents a considerable saving in power. Finally, from an operational point of view, the memory write signal produced by the comparison circuit should

take the from of a pulse, the duration of which must be less than one clock period. All of these factors indicate that the pixel must contain logic to reset the photodiode to the recharge state, once the memory has been triggered. An SR latch will provide tbis control (as will be shown in Section 4.4.3).

Stating previously that 'the data is retrieved' from the pixel is a generalisation that ignores the details of how this is accomplished. The pixels are formed as a two dimensional array, with each pixel storing data read from the input data bus during the integration period. After the image is captured each pixel must be addressed in turn, to place the contents of their local memory on the output data bus. Pixel memories which are not being addressed must remain in a high impedance state. As the pixels are formed as a two dimensional array, each will be addressed by a row and column address line. The most obvious and economical (in terms of area) column/row decoder to be included within the pixel is a two input NAND gate, with the memory 'read' operation being active low.

Finally, the comparator is an analogue component which produces an output unsuitable for digital operation. Its output must be buffered to digital levels, to ensure reliable operation of the local memory. It will be shown in Section 4.4.4 that the SR cannot drive the photodiode/FET directly, and a second 'FET switch' stage is required. This results in the pixel being comprised of the six components listed below.

1. Photodiode.
2. Comparator.
3. SR latch.
4. NAND gate.
5. Buffer.
6. Reset Switch.

The final pixel schematic is shown in Figure 4.2. The pixel is divided into two functional sections, analogue and digital, for the purpose of simulation. This scheme will

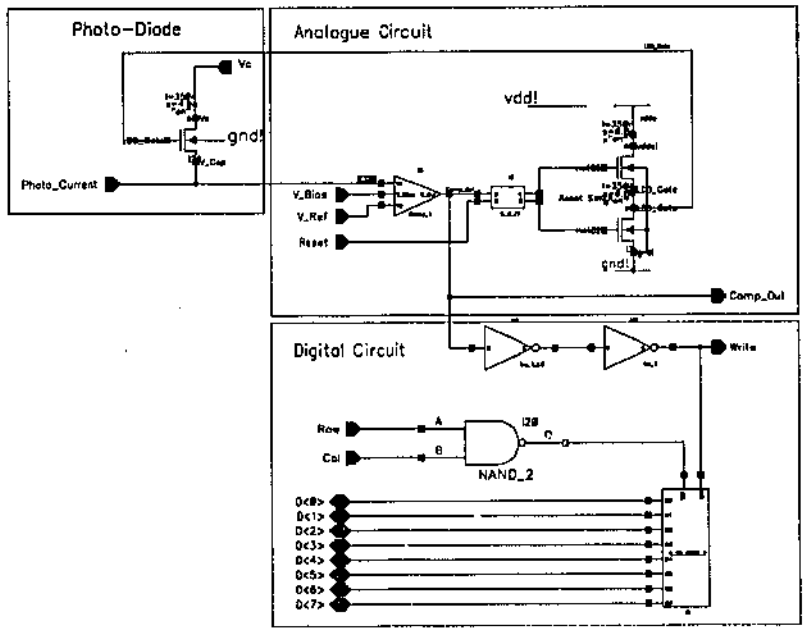


Figure 4.2: Pixel schematic. The complex pixel circuit is divided into analogue and digital sections. The analogue section converts the illumination into a delayed pulse, the digital section latches the resulting data value.

be continued in the description of the operation. (Note also that the Photo_Current pin in the schematic is included for simulation purposes only, to represent the optically generated current that would be present in the actual device).

4.4 On-Pixel Analogue Circuit

The analogue circuit within the pixel is comprised of the photodiode, the comparator, the SR latch, and the reset switch. The purpose of the analogue circuit is to generate a memory write signal when the ramping voltage from the photodiode crosses a threshold level. The threshold voltage is set externally, and can be varied to adjust the integration time. This will allow for 'fine tuning' of the operating circuit, given that prior to manufacturing the array, the photocurrents can only be estimated. The analogue section also controls the self resetting process, which will be described in detail in Section 4.4.3. In the following sections each part of the analogue circuit will be described in detail.

4.4.1 Photodiode and Photocurrent Estimation

The photodiode is formed from the source-substrate junction of an n-channel FET. The n-FET has a higher mobility than the p-FET and therefore better optical characteristics. It is also better suited for the tightly packed pixel, as p-wells in the twin tub process are more compact than the n-wells (as the substrate is p-type). The photodiode and reset FET are combined into one device, an n-FET with an enlarged source-substrate junction. The disadvantage of using an n-channel FET is that the source capacitance can never be charged to a voltage higher than $V_{dd} - V_T$, where V_T is the threshold voltage of the FET. To prevent variations in the recharge voltage, caused by different values of V_T in individual devices, the photodiode is charged to a voltage less than V_{dd}, V_C. V_C is supplied externally, and along with V_{Ref}, can be adjusted to optimise performance. The light capturing area of the photodiode is calculated at $253\mu m^2$, resulting in a pixel fill factor of 12.3%, and a junction capacitance of 172 fF. Using these figures, and the current density estimation of Section 3.3 ($193mA/m^2$), the anticipated photocurrent is approximately 50pA at 500 lux.

4.4.2 Analogue Comparator

The analogue comparator is the most complex single component in the pixel. A continuous time analogue comparator was chosen over a clocked comparator as it does not introduce switching noise into the pixel, and does not require multi phase clocks. This of course means that the pixels run asynchronously, from each other, and the data bus. The comparator has two stages, a differential amplifier followed by a current-sink inverter. Figure 4.4 shows the output of each stage of the comparator versus a differential input signal at the switching point (V_p is fixed at 1V, V_n is ramping from 3.3V, down to 0V). To recall the operation of the pixel, the photodiode is reset to the recharge voltage V_C, and then allowed to discharge to the reference voltage V_{Ref}, where the comparator output will rapidly rise. This will trigger the SR latch, and in turn the reset switch, which will recharge the photodiode to V_C. The rise/fall of the comparator is buffered, and used as the write signal for the

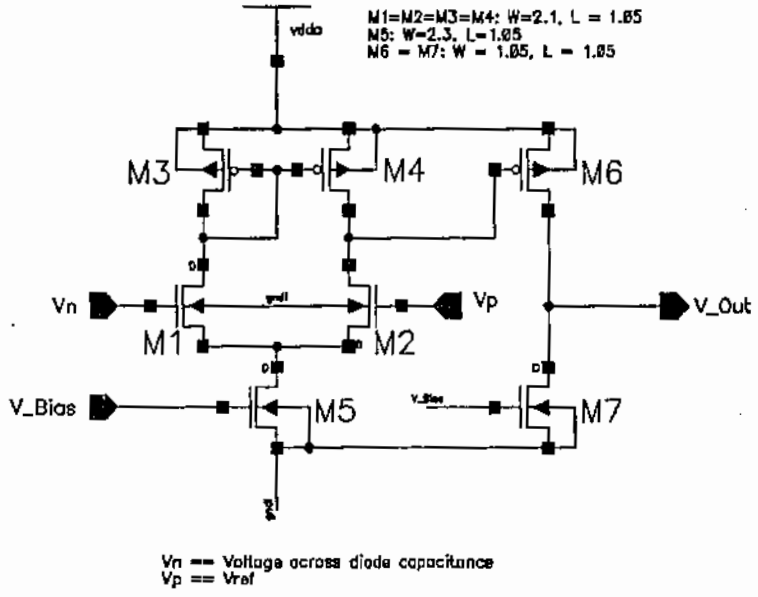


Figure 4.3: Comparator schematic. This is a two stage analogue comparator with current sink inverter output. Device matching in the first stage is critical.

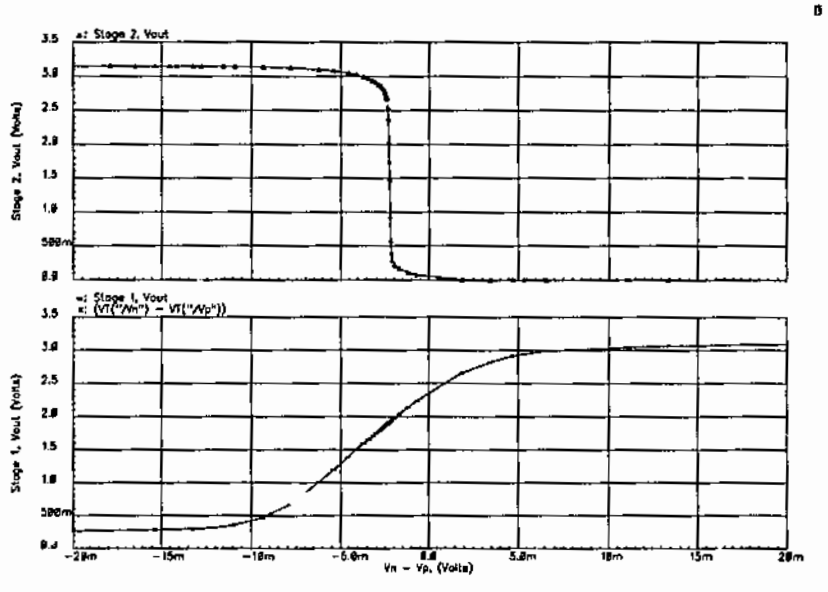


Figure 4.4: Simulation results showing the outputs of comparator stage one (below) and stage two (above) for a differential input signal.

memory, which will store the count on the data bus at that instant. To ensure the resolution of the conversion is not degraded, the width of this write pulse must be less than the data clock period. The main concern here is that the gain of the comparator is sufficient to drive the output above the logic high input level of the SR latch, for the small differential input generated at the instant when the ramping photodiode voltage is almost equal to V_{Ref}. To determine the gain requirement, the system is assumed to be at the beginning of the conversion process, where the clock is at its initial (highest) frequency, and that the photodiode is discharging at the maximum rate ($I_D = I_{max}$). The input high level of the SR latch is taken to be 1.9 V (the reason for this assumption will be explained later in Section 4.4.3). It was determined previously that the clock period required to resolve a current step is (for 8-bit resolution)

$$t_{clk} = \frac{t_0}{254}. \tag{4.1}$$

Considering the relationship between the photodiode voltage and the integration time, the variation in V_{cap} over this time will be

$$\frac{(V_C - V_{Ref})}{254}, \tag{4.2}$$

therefore, the comparator must have at least sufficient gain to reach 1.9 V with this input voltage, from which the gain is determined to be

$$A_v \geq \frac{1.9 \times 254}{V_C - V_{Ref}} = 571 \approx 55dB. \tag{4.3}$$

Both comparator stages are nonlinear, and while there are approximations for calculating the gain in the linear region of operation about the point where $V_p \approx V_n$ [13], a preferred method is to determine the gains from the simulation results. From Figure 4.4

$$A_v = \frac{\Delta V_{Out}}{\Delta(V_n - V_p)}, \tag{4.4}$$

which was found to be 80dB, well above the required gain.

Although there is no switching noise generated within the pixel itself during the integration time, the comparator is powered from a separate analogue supply V_{dda}, to minimise the impact of digital switching in adjacent pixels.

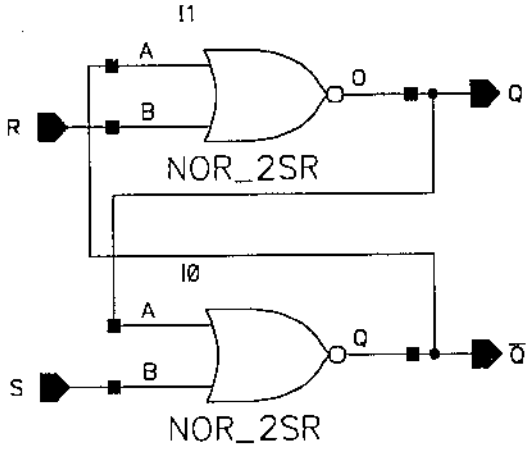


Figure 4.5: SR latch schematic.

4.4.3 SR Latch

It may seem inappropriate to regard an SR latch as an analogue component, however its characteristics significantly affect the operation of the reset loop, and the overall pixel characteristics. The SR latch is a common digital component formed from two interconnected NOR gates, refer Figure 4.5. Figure 4.6 shows a section of the transfer characteristics of the device, with the 'R'(reset) input held at 0 V and the 'S' (set) input being a positive going pulse, forcing the Q output high. It can be seen tbat there is a linear region of operation, midpoint in the switching characteristics, as there is indeed for all CMOS devices. Referring to the signal labels of Figure 4.2, the operation of the SR latch begins with the reset line being taken high which starts the integration time. When $V_{Cap} \approx V_{Ref}$ the comparator output will begin to rise. Once it reaches the input high logic level of the SR, this in turn will begin to change state. The 'Q' output of the SR only has to rise to approximately 0.6 - 0.7 V for recharging the photodiode to occur. V_{Cap} will rise, reducing the differential input to the comparator, and the comparator output will start to fall. This means that the comparator output will never rise very far beyond the logic high input level of the SR. This is significant, as it is at the comparator output that the circuit branches off to the digital section of the pixel. Feedback around the reset loop ensures that all circuits within the loop must switch, but the digital circuits outside of the loop

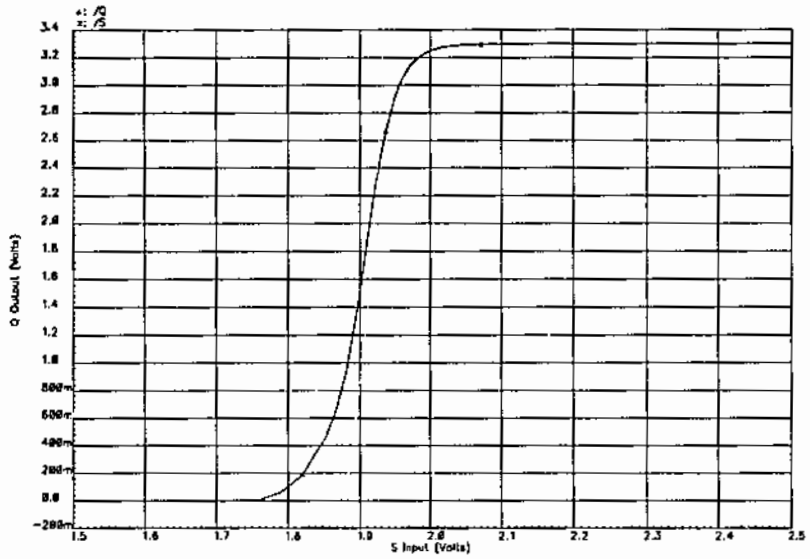


Figure 4.6: Simulation results, voltage transfer characteristic of the SR 'Q' output, 'S' input in transition from low to high. There is a near linear response in the center of the curve.

require true logic input levels to operate reliably. To allow for some noise immunity the output of the SR must be raised, and the switching level of the first digital stage lowered. This is achieved by increasing the size of the p-channel FET's within the SR, raising the operating point, and hence the comparator output voltage, to approximately 1.9 V. In the same way, the buffers between the comparator and the memory have had their operating point lowered to approximately 1.3 V, which will guarantee reliable operation.

4.4.4 Reset Switch

Firstly, the difference between the reset FET and the reset switch should be clarified. The reset FET is the photodiode/FET that is connected to V_G, and the reset switch is comprised of two n-channel FET's driven by the SR latch. It may seem that the reset switch is redundant, and that the reset FET can be driven directly from the output of the SR, however the linear region of the SR transfer characteristics can cause switching reliability problems, especially as all signal voltages within the

circuit tend to stay in the region between 1.5 V and 2.5 V. Without the additional reset switch the circuit tends to behave as a linear regulator, the subthreshold current of the reset FET compensating for the photocurrent, regulating V_{Cap} to V_{Ref}. To overcome this the reset switch is included in the loop, driven by the SR latch's complementary outputs. When the SR 'Q' output begins to rise, the upper FET of the reset switch rapidly charges the gate capacitance of the reset FET to $V_{dd} - V_t$. This holds the reset FET on even when the comparator output begins to fall, as there is no path to discharge the gate capacitance. When the SR latch is reset, '$\overline{Q}$' operates the lower FET in the reset switch, discharges the gate capacitance, and the photodiode is disconnected from V_C. In effect, it adds hysteresis to the reset operation without the need for a more complex comparator. The disadvantage of this approach is that the reset FET cannot reliably switch a voltage higher than $V_{dd} - 2V_t$, which limits the range of V_C.

4.5 On Pixel Digital Circuit

The digital circuit within the pixel is comprised of the buffers, the memory and the column/row decoder. This section of the pixel serves two purposes: the first during image capture, the second during readout. During image capture, the pulse generated by the comparator is buffered, and enables the memory write operation, storing whatever value is present on the data bus. During readout the column and row lines are high, the memory read operation is enabled, and the stored data value is placed on the data bus to be retrieved.

4.5.1 Buffers

As seen previously, the comparator does not produce true logic levels, due to the feedback within the circuit, and the maximum output anticipated is approximately 1.9 V. This signal must be buffered if it is to enable the memory write operation reliably, which is done using two cascaded inverters. The standard practice with CMOS circuits is to make the p-channel FET approximately three times the width of the

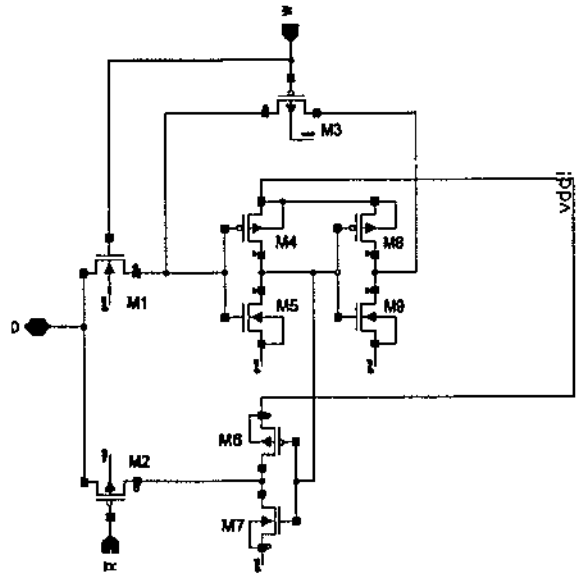


Figure 4.7: Schematic diagram of a single memory cell. Eight such cells are combined for each pixel memory.

n-channel FET, to compensate for the lower mobility of the p-channel device. However, the first inverter in the buffer stage has a wider than normal n-channel FET, which shifts the operating point down to approximately 1.3 V. This ensures that the low comparator output reliably enables the memory during the write operation.

4.5.2 Memory

Each cell of the 8-bit memory is formed from a modified 6T latch, and for several reasons is the weak point in the pixel design. While it is robust, and can reliably drive the data bus during readout, it is physically large, and consumes an undesirable amount of power. The intention of the design was to make these sacrifices, in order to avoid the complications arising from the design of sense amplifiers which fit the pixel pitch, and single bit line S-RAM cells. Whether this conservative approach to the memory design is justified is debatable, but the memory has proved reliable, if inelegant. Referring to Figure 4.7, the memory has two control lines: 'W' enables the cell for writing, and 'R' for reading. 'D', the data line, is common to both the

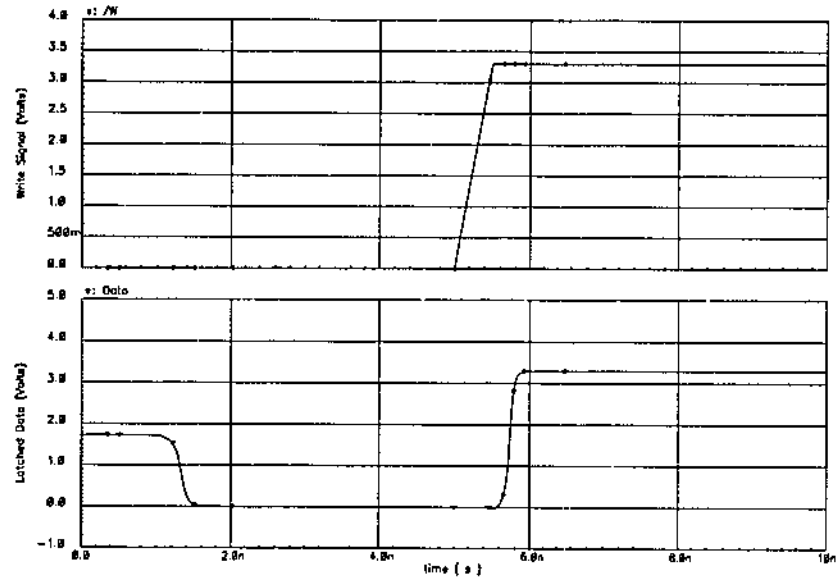


Figure 4.8: Simulation results showing the propagation delay writing a '1' into the memory cell.

reading and writing operations, but the internal data path is not. When writing data to the memory, the circuit appears as a standard 6T latch. When reading data from the memory, the data path also includes a buffer for driving the bidirectional data bus. The propagation delay in the cell is shown in Figure 4.8 which can be seen to be $\approx$ 500ps. As with most of the digital circuitry in the design the propagation delay through the device is insignificant compared with the relatively low speed data that is clocked for the conversion process. Each pixel contains eight such cells, which occupy 50% of the total pixel area.

4.5.3 Column/Row Decoder

Each pixel has a row and column address line. Referring again to Figure 4.7, it can be seen that the memory 'R' (read) line is active low, which allows a NAND gate to be used to enable the memory for reading. When both the column and row lines are taken high, the NAND gate output goes low, and the contents of the memory is buffered onto the data line. During the memory read operation the memory write

data path is disabled by 'W' line, which is held low while the analogue pixel section is inactive. The row and column signals are decoded from binary addresses, by logic at the periphery of the array.

4.6 Pixel Simulation

The simulation results for the pixel are shown in figures 4.9 and 4.10 for a photocurrent of 20pA, V_C = 1.8 V and V_{Ref} = 1.0 V. Note that the maximum value of the comparator output is 1.94 V, while the buffer output is 3.3 V. Figure 4.10 expands the time scale at the switching point, where the slowly rising output of the comparator (due to the input ramp voltage) can be clearly seen. The significance of the gain can be noted by the contribution of the 'on' time compared to the 'off' time of the comparator. The switching delay within the comparator is insignificant compared to the delay caused by the slowly ramping input voltage, and can be disregarded when determining the output pulse width.

4.7 Control Circuit

The control circuit generates the Gray code count, which is distributed to the array. This is the data that is written into the memory of each pixel when it triggers. This data must be generated as per the linearising algorithm determined in the previous chapter, and Figure 4.12 shows how the circuit accomplishes this. The primary clock input is first gated by the blanking circuit for 254 clock cycles, after which time it drives the frequency divider circuit. This circuit divides the primary clock frequency by a 16-bit integer value stored in the lookup table. The lookup table is indexed by the 8-bit Gray counter output, the same value that is distributed to the pixel array. In this way all timing is derived from the primary clock source alone. The control circuit is realised using digital logic gates, all sections of the circuit were designed for a clocking speed of up to 50MHz, well above the predicted operating frequencies. The control circuit schematic is shown in Figure 4.11.

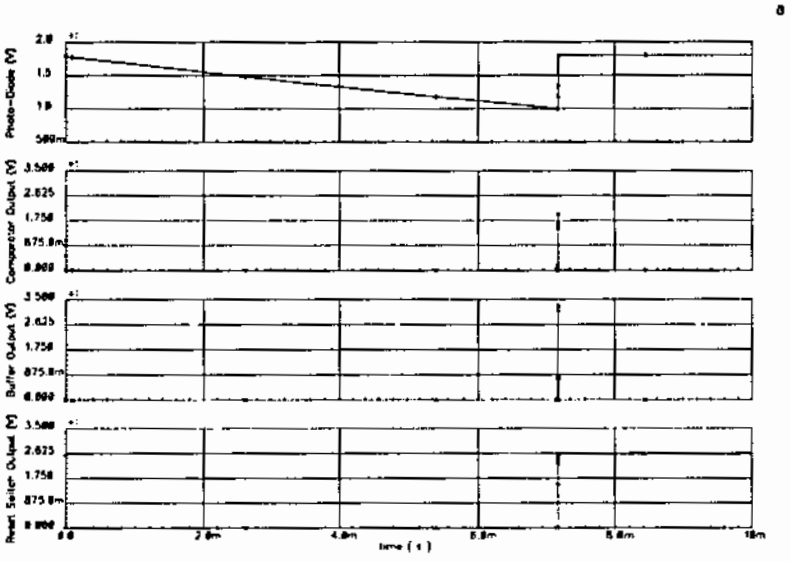


Figure 4.9: Simulation results showing the operation of the pixel analogue section. The photodiode discharges to the reference voltage, and triggers the comparator. The comparator output resets the photodiode, generating the write pulse, which is then buffered for the digital section.

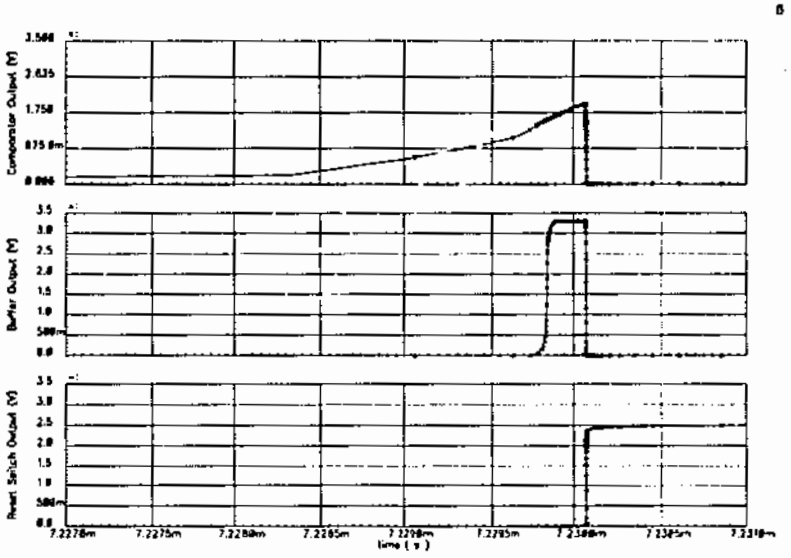


Figure 4.10: The same simulation as figure 4.9, highlighting the switching point. The comparator output only reaches a maximum of approximately 1.8 V; the buffers ensure that a safe noise margin is maintained for the digital section.

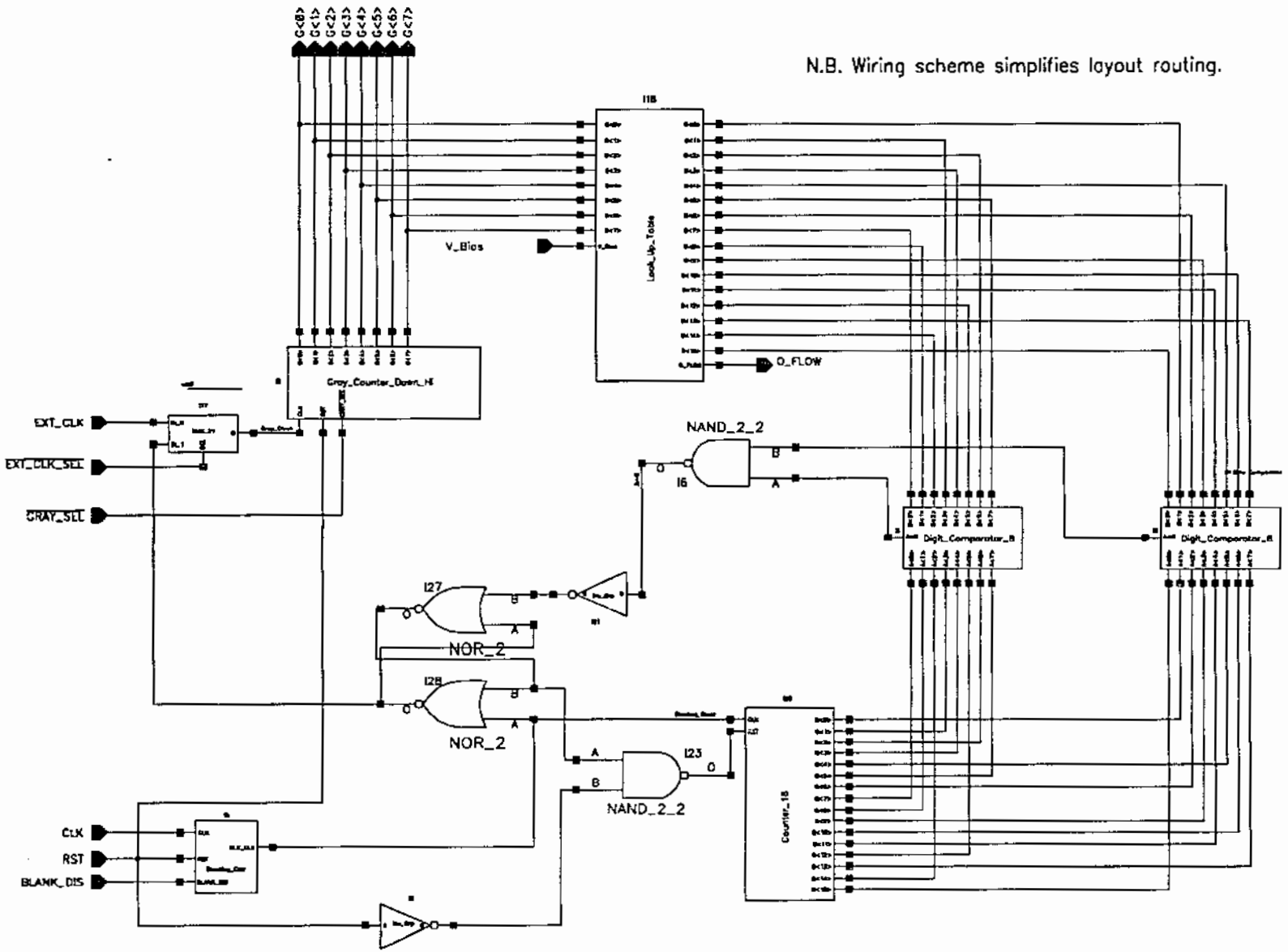


Figure 4.11: Control circuit schematic. Complex components have been replaced with their hierarchical equivalents. The data bus at the top of the figure is distributed to the DPS array, via the data bus and row buffers.

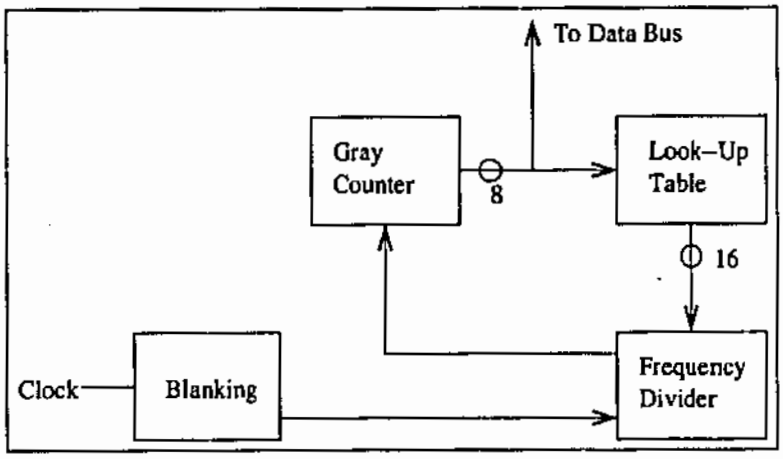


Figure 4.12: Control Circuit Block Diagram.

4.7.1 Blanking Circuit

The blanking circuit generates a delay of $254t_0$ where t_0 is the external clock period. This is achieved by decoding the output of an eight bit counter, and using this to gate the clock to the frequency divider stage. Once this has occurred the clock input to the counter is removed, halting the blanking counter. The counter is a negative edge triggered, series synchronous counter with asynchronous reset (which is also used as the basis for the frequency divider and Gray counters). The blanking function can be disabled during testing.

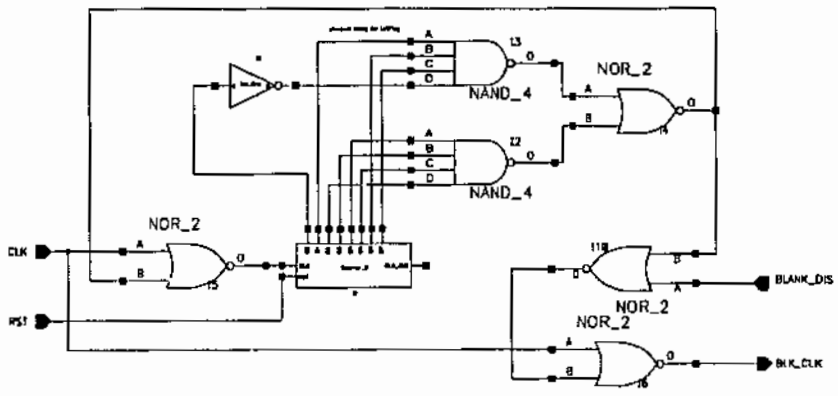


Figure 4.13: Schematic diagram of the blanking circuit, which counts 254 clock pulses before passing the primary clock through to the variable clock generation circuits.

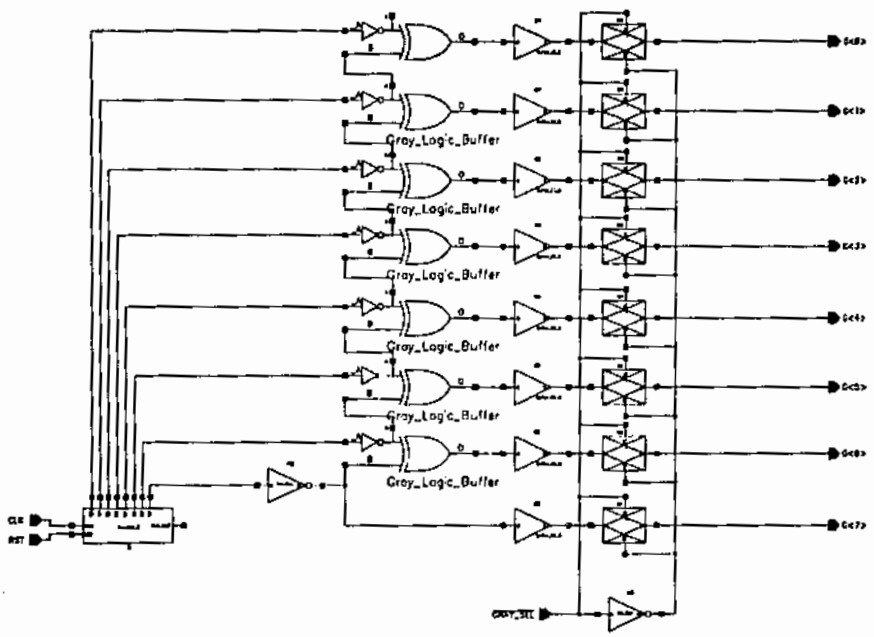


Figure 4.14: Gray counter schematic. The serial-synchronous counter includes buffers for driving the data bus, and transmission gates for isolation.

4.7.2 Gray Counter

The Gray counter is formed from an 8-bit counter with Boolean logic to convert the binary output to Gray code, refer Figure 4.14. Tri-state buffers are also provided for driving the data bus, and can isolate the counter from the bus during testing. The use of a Gray counter is essential for a number of reasons. Primarily, due to the asynchronous nature of the pixel operation, Gray code is required to minimise transition errors, (this is covered more fully in Section 3.6).

4.7.3 Lookup Table

The lookup table is formed from a Boolean decoder and a wired-OR ROM. The decoder first reduces the 256 possible outputs from the Gray counter into 28 ranges. Each range outputs a corresponding 16-bit divisor value, which is stored in a wired-OR ROM, constructed from static n-channel loads with p-channel pull-ups. The Gray value for '0' bypasses the ROM and is extracted as the O_FLOW signal, to indicate that the conversion is complete and will overflow if not terminated. The

values stored in the lookup table are those derived from the analysis in Section 3.5, which are listed in Appendix A.

4.7.4 Frequency Divider

The frequency divider is composed of a 16-bit counter and a binary digit comparator. Once the divisor value has been determined it is input to the 16-bit comparator. The output of the 16-bit counter, which is driven by the 'blanked' clock signal, is also input to the comparator. When the divisor and counter values are equal, the comparator output goes high and sets the SR latch. The SR latch 'Q' then output goes high, causing counter to reset, and in turn the comparator output goes low. The SR latch holds its 'Q' output high until the next clock pulse resets the SR latch, and the Gray counter decrements on this negative edge. The SR latch is provided to ensure the comparator output is held for at least one clock cycle.

4.7.5 Test Selection Circuits

The control circuit has a number of additional circuits to allow for testing and development of the DPS array. This is considered essential, as the staudard operation is 'hardwired' into the lookup table. Also, should any sections of the control circuit become damaged, or fail to perform as expected, the array can function using an external data source. A full description of these circuits, and how they are used in testing is given in Section 5.4, in the following chapter.

4.8 Control Circuit Simulation

Figure 4.15 shows the control circuit simulation output for an input clock frequency of 50 MHz. The upper waveform shows the clock input to the frequency divider, having been 'blanked' for a period of $254 \times 20ns = 5.08\mu s$. The lower waveform shows a section of the clock input to the Gray counter, the clock period increasing under the control of the lookup table and frequency divider. Note the transitions at $6\mu s$ and $8\mu s$, as the divisor value produced by the lookup table changes.

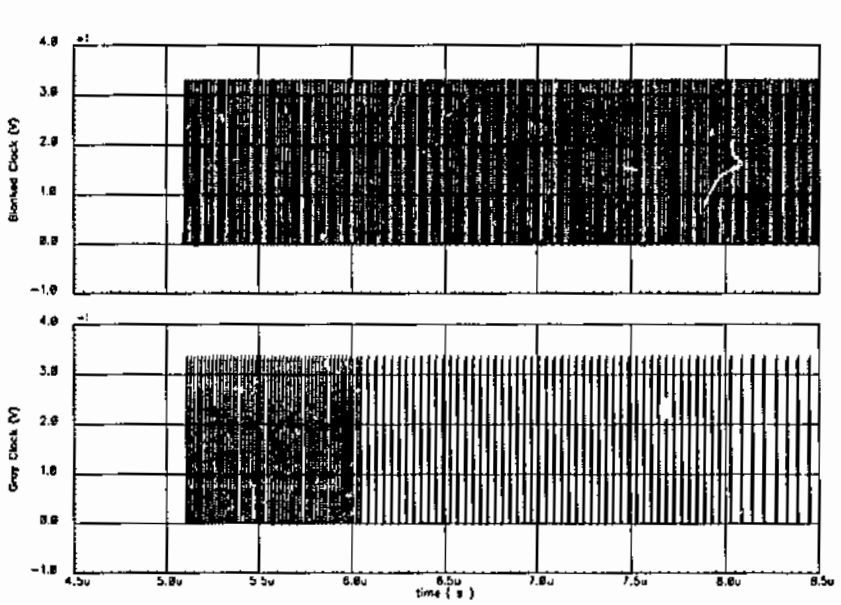


Figure 4.15: Simulation results of the control circuit, showing the blanked primary clock (above), and the variable clock (below). The steps in the lookup table multiplier values can be seen as the clock changes frequency.

By deriving the variable clock in this way, the range of illumination over which the conversion is taking place can be changed by altering only one parameter: the clock frequency. This is provided externally by a control system that will determine the appropriate frequency range from the incident illumination, either through analogue means or by analysing the output of the array.

4.9 System Simulation

Due to the complexity of the array the entire system could not be fully simulated, and had to be reduced to smaller representative examples of the complete system. An array of 4×4 pixels was simulated to test the data paths, buffers, address decoders etc, but even for this small system only short integration times could be simulated. Due to the $1/I_D$ nature of the integration time, and the need for analogue simulations, small photocurrents proved prohibitively long to test.

A simpler system consisting of only the control circuit, and a single pixel, was

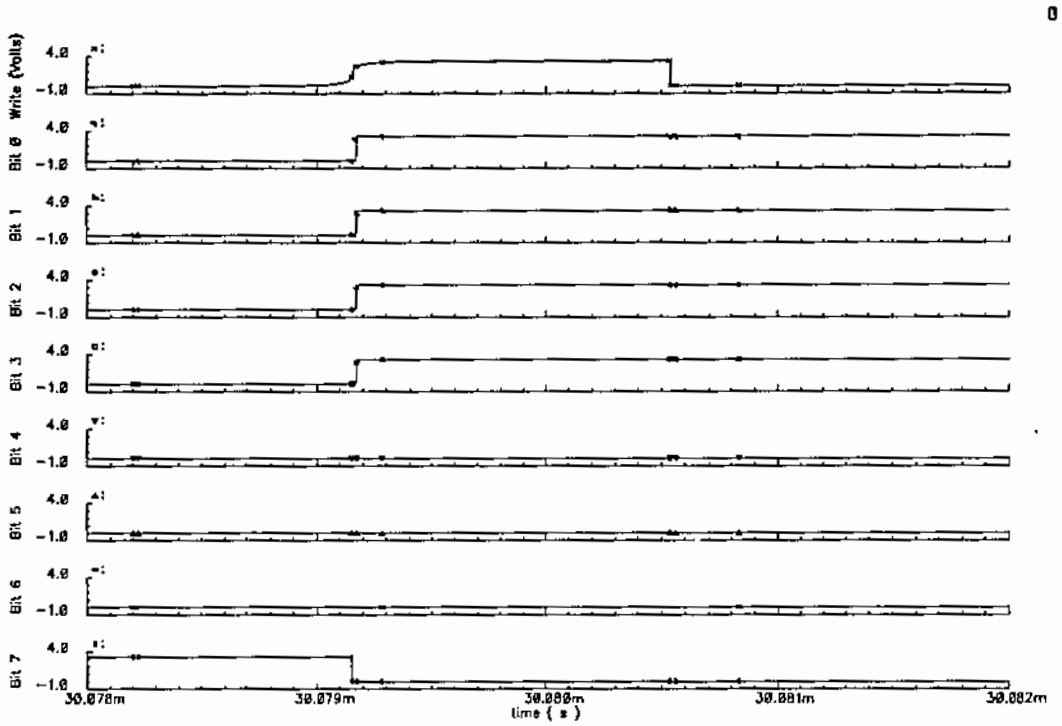


Figure 4.16: Simulation results, showing the data bits latched into pixel memory. The data value stored within the pixel is recorded for a range of photocurrents, to determine the linearity of the conversion process. The simulation circuit consists of a single pixel and the control circuit.

created in order to extend the range of photocurrents over which the tests could provide results in reasonable time. Figure 4.16 is a sample output from the simulation, showing the memory write signal (top), and the memory cell states bit-0 to bit-7 (below). Note how the write pulse is of longer duration than that of Figure 4.10, due to the lower photodiode discharge current (5pA compared with 20pA previously).

The simulation was repeated for a range of currents, the integration time and memory contents recorded and plotted in Figure 4.17. Using linear regression, a line of best fit was added, and the ability of the control circuit to linearise the integration time can be clearly seen. This verifies the derivation of the time domain ADC process, while the ability of the ADC to perform a linear conversion can be seen by comparing the digitised values of Figure 4.17 with the integration times of Figure 4.18.

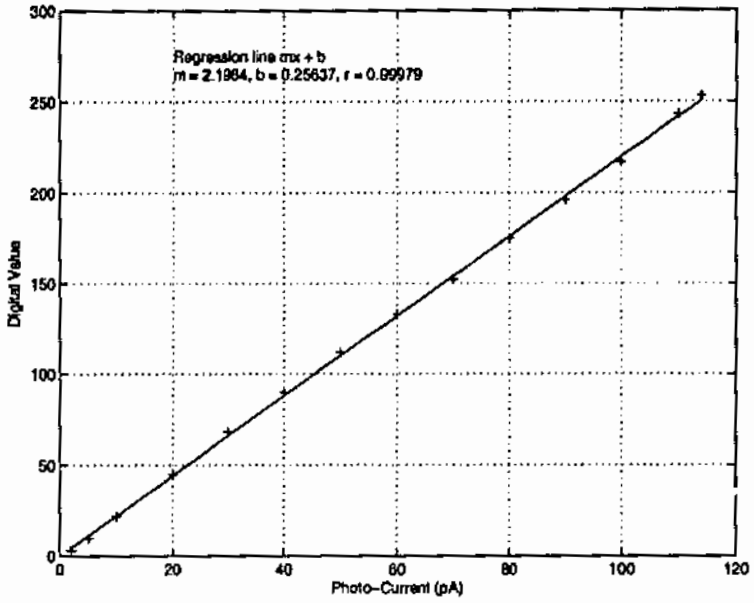


Figure 4.17: Simulation results, conversion count versus photocurrent. The digital values recorded from the single pixel simulation show a linear response against the photocurrent.

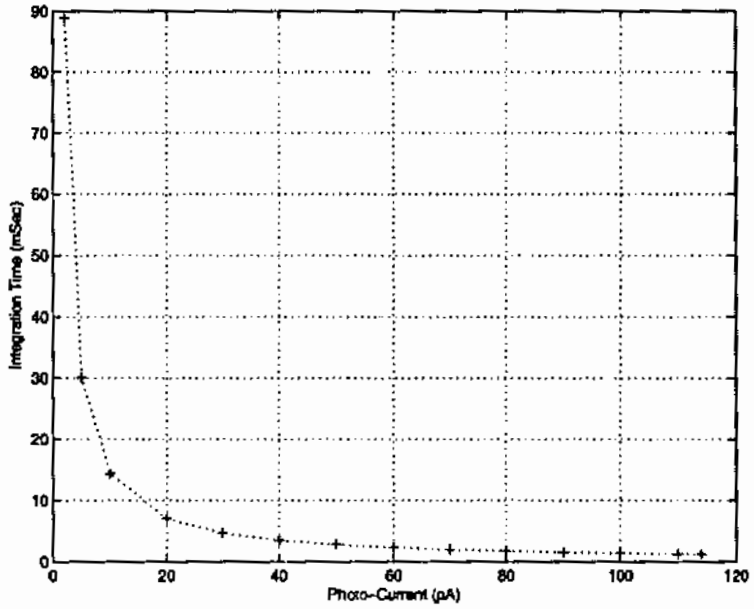


Figure 4.18: Simulation results, integration time versus photocurrent. Due to the nonlinear response of the integration time, the combined results took several weeks of simulation time.

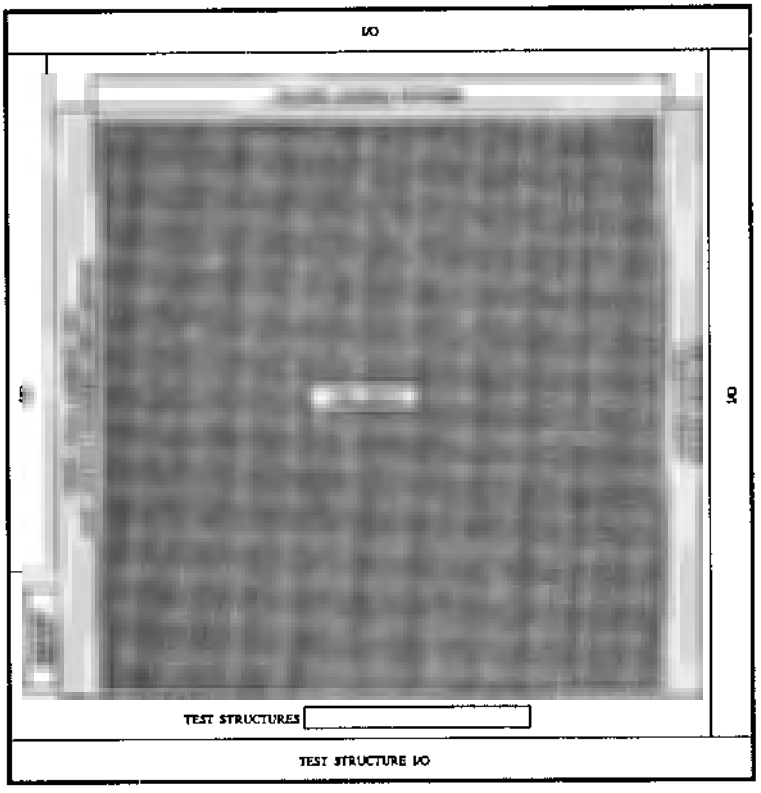


Figure 4.19: Floor-plan for the DPS array chip.

4.10 Floor-planning and Layout

The final array of 64 × 64 pixels was manufactured in the Alcatel 0.35μm, 3.3V digital CMOS process. This is a twin tub, single polysilicon layer, five metal layer standard CMOS process. The only special consideration given to the optical nature of the array is that the active region of the photodiode is unsalicided, and that no dummy metal is deposited over it, both of which are standard design options given by the manufacturer. (Salicide is a treatment of the active region with tantalum, which reduces resistance, but which also renders the region almost opaque, highly undesirable in a photodiode. Dummy metal is deposited in vacant die areas as part of the manufacturing process in order to increase production yields by ensuring that there is an even metal coverage of the die.)

Figure 4.19 shows the floor-plan of the pixel array, which closely follows the

architecture proposed at the beginning of the chapter. Data flow is from left to right, with the pixel array occupying the center of the figure. At the left of the array is the control circuit, input data bus, row buffers, row address bus, and row address decoders. Above the array is the column address bus and column address decoders. To the right of the array is the output data bus, and the row buffers. The core power (V_{dd}) is fed from the left, analogue and reference power ($V_{dda}, V_C, V_{Ref}, V_{Bias}$) is fed from the right of the array. Below the array are a number of test structures, which will be described in the next chapter. Input, output, and power pads are standard cell, provided by the manufacturer.

The physical layout of a single pixel (refer Figure 4.20) measures 45μm $\times$ 45μm, resulting in the 64 $\times$ 64 pixel array measuring 3mm x 3mm. The control circuit measures 140μm $\times$ 470μm. The final die, including the standard cell pads, measures 3.7mm $\times$ 3.9mm.

4.10.1 Substrate Coupling

All of the circuits described in the previous sections share a common substrate, with p-channel devices formed in n-wells, and n-channel devices formed in p-wells. Digital switching circuits can cause currents to flow in the substrate which in turn can cause localised variations in the substrate bias voltage. This 'substrate noise' can cause variation in device threshold voltages, which is of particular concern in a mixed signal design. (*Mixed signal* refers to the combination of analogue and digital circuits in a single IC.)

Extensive use is made of shielding to prevent this coupling from occurring. Shields, or 'guard rings', form low resistance paths to the supply rails, and take two forms: metal-1/n-active/n-well channels connected to V_{dd}, or metal-1/p-active/p-well channels connected to ground. In either case the metal line is tied to the active layer with the maximum number of contacts possible. Large physical separation is also an effective shield, but has limited application, particularly within the densely packed array. Individual parts of the pixel (photodiode, comparator, memory) are all shielded, with the analogue circuit section having a guard ring also. This is

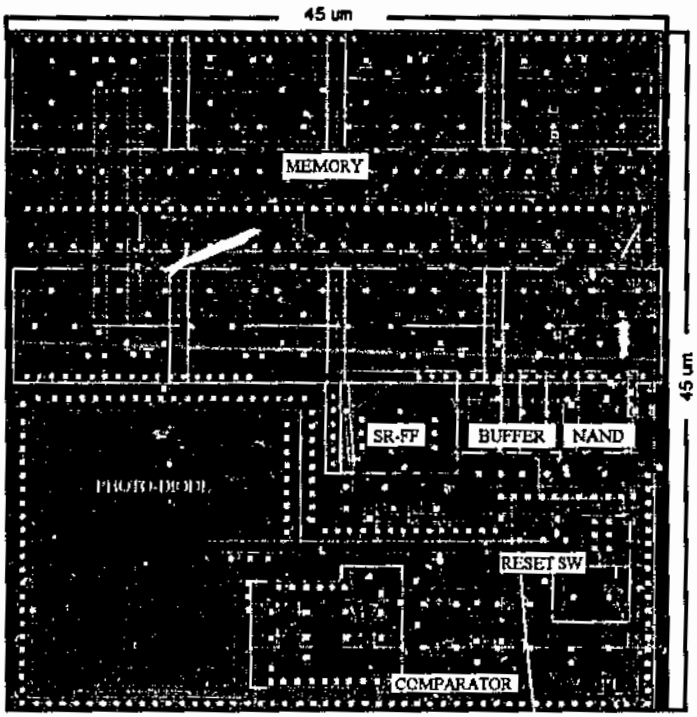


Figure 4.20: Pixel layout, showing dimensions and component parts.

mainly to prevent interference from adjacent pixels, rather than from digital circuits within the pixel as the pixels themselves are electrically 'quiet'. The entire array is then shielded by an n-well guard ring between the array and the large buffers which drive the row data bus. The control circuit is also shielded with an n-well guard ring, and is additionally separated from the array by the width of the power, address and data bus. Figure 4.21 shows a section from the upper left corner of the array, highlighting the guard rings.

4.10.2 Device Matching

The final important issue in the physical layout is the matching of devices in the comparator circuit. In any CMOS circuit there will be variations in device parameters across the circuit, however for the comparator to operate correctly, the devices in the differential amplifier stage need to be closely matched in their performance. There are rules that can be followed to minimise the mismatch betweeu components:

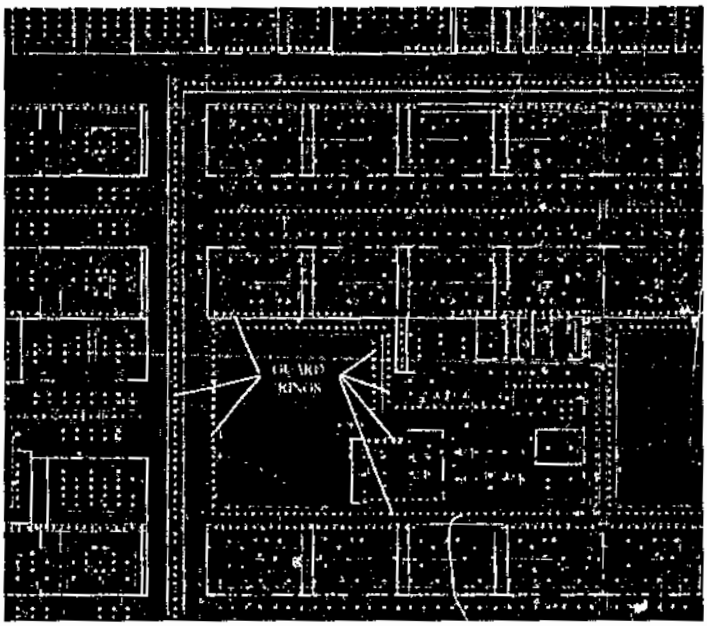


Figure 4.21: Array section, showing the photodiode, pixel, and array guard rings.

1. Devices in the amplifier have a common centroid configuration. This ensures that variations in size and doping are equalised between pairs of transistors in the differential circuit.

2. Transistor widths (W) and lengths (L) are three to four times the minimum feature size: it is at the limits of the process that the variation in size is most pronounced.

3. Transistor W/L ratios are kept below five. If wide transistors are required, smaller devices are connected in parallel.

4. Signal paths for matched devices are made identical, even if this requires dummy interconnections or vias.

It is also recommended in some literature that any voltage used to bias a current source should exceed the device threshold voltage by at least thirty percent, in order to avoid the critical operating region around the threshold voltage. This may be sound advice for small circuits containing tens or even hundreds of current sources,

however, the DPS array contains thousands. Current consumption at these biasing levels is prohibitive, regardless of any benefit that may result.

4.11 Conclusion

This chapter has presented a design which incorporates a photodiode, comparator, memory and addressing logic into a single digital pixel sensor. A control circuit has also been designed which generates data in accordance with the timing algorithm developed in the previous chapter. Simulations have confirmed that the control circuit operated in conjunction with the digital pixel produce a linear conversion of the photocurrent to a digital value. The designs have heen taken from the schematic to a physical level, resulting in a pixel which measures 45μm $\times$ 45μm with a fill factor of 12.3 %; the complete DPS array of 64 x 64 pixels measures 3.9mm $\times$ 3.7mm. The die is mounted in a JLCC-84 chip carrier.

Chapter 5

Operation and Testing of the DPS Array

5.1 Introduction

As the operation and testing of the DPS array are closely related topics, they will both be covered in this chapter. This chapter begins with the description of the test environment, and the interfacing required to control the array, display, and record the results. The procedure for a normal image capture is then described, separating the operation into independent exposure, and read phases.

The chapter then moves on to the testing of the array, beginning with the test facilities that have been built into the chip. The control circuit contains a number of multiplexing circuits that allow alternative clocking strategies to be generated externally, for testing and development purposes. Test circuits have also been included on the chip, isolated from the main array, which give access to different sections of the digital pixel.

The tests have been broadly grouped into functional testing of the control circuit, those which use single pixels (the pixel test circuits), and those which use the entire array. The pixel test circuits are particularly useful for characterising the performance of the digital pixel, while the array tests determine the effect of process variations on the performance of the imager.

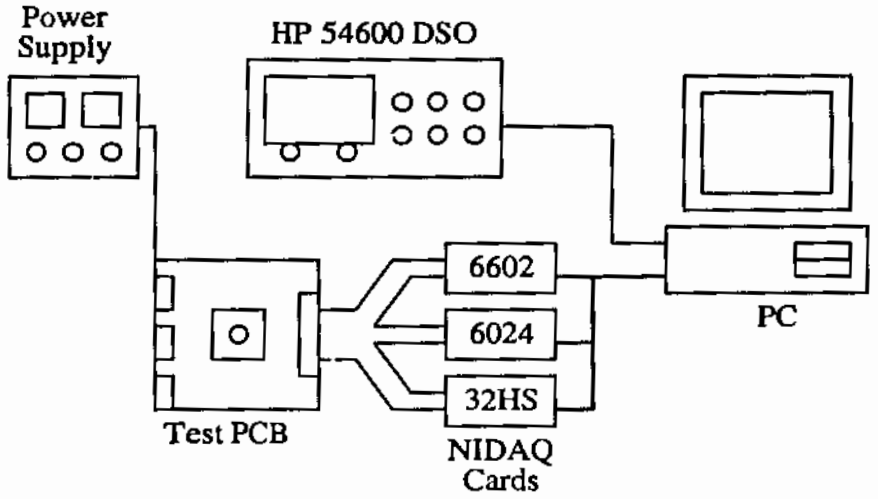


Figure 5.1: DPS array test environment. The chip is interfaced to the PC by National Instruments NIDAQ hardware, with the controlling software written in C++.

5.2 Test Environment

This section describes the equipment used to operate the DPS array, and record the digital and analogue results of the testing. In addition to the normal hardware required to test a CMOS IC, the DPS array also requires test equipment to generate the controlled illumination necessary to characterise its optical performance.

5.2.1 Electrical Test Equipment

The DPS array is controlled by a PC, interfaced via three types of *National Instruments Data Acquisition* (NIDAQ) cards, refer Figure 5.1. The PCI-6602 general purpose timer/counter card is used to generate the primary clock, and the reset pulses. The PCI-6024E multi I/O provides V_{Ref} from a 12-bit digital to analogue converter (DAC), and two PCI-DIO-32HS cards provide all digital control and data I/O. The JLCC-84 package is mounted on a custom made *Printed Circuit Board* (PCB), which provides all voltage rails (except V_{Ref}), and interfaces between the 5 V outputs of the NIDAQ cards and the 3.3 V inputs of the chip. This is done by simple voltage dividers, allowing the lines to be operated bi-directionally if required.

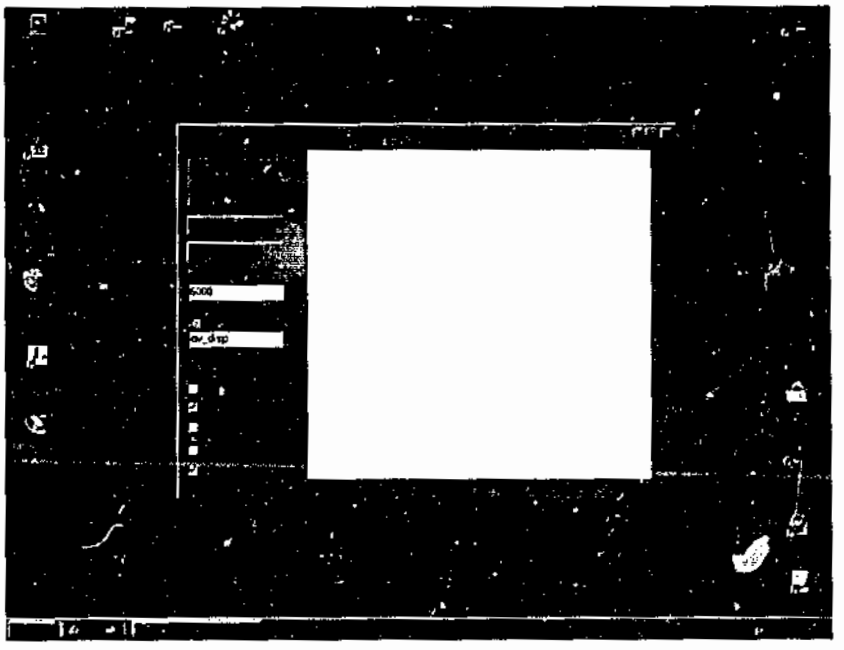


Figure 5.2: Control console.

Analogue signals are measured using a *Digital Storage Oscilloscope* (DSO), which is also interfaced to the PC for recording and display.

The test routine software has been written in C++, using an *Integrated Development Environment* (IDE) with interface libraries provided by National Instruments. The software stores the captured image as an 8-bit, greyscale, Windows compatible bitmap (.bmp) file. A screen shot of the control console is shown in Figure 5.2. Aside from the control console program, a number of simple test routines which do not require a graphical interface have also been written in C++.

Pin Name	Description	Range	Test Setting
V_{dd}	Digital Supply	3.3 +0.3 / -0.6 V	3.3 V
V_{dda}	Analogue Supply	as V_{dd} above	3.3 V
V_{dde}	Pad Supply	as V_{dd} above	3.3 V
V_{Bias}	Comparator Bias	0.3 - 1.0 V	0.33 V
V_C	Photo-diode Reset Voltage	1.0 - 1.8 V	1.3 V
V_{Ref}	Comparator Threshold	0 - 1.8 V	0.4 - 1.3 V

Table 5.1: DPS array power supply requirements.

The five voltage sources required for the normal operation of the array are listed in Table 5.1, along with the settings used in the tests (unless otherwise stated in the test description, for example, low voltage testing). The test PCB is supplied from a single power supply, and adjustable linear regulators on the PCB are used to provide the separate power rails (at least two volts of headroom is required for the regulators). Links are provided to break these supplies for current measurement. V_{dde} is the 3.3 V supply for the digital buffers that drive the bonding pads. It is kept separate from the core digital supply, V_{dd}, to minimise any interference that may be caused by the currents required to drive these large capacitive loads.

5.2.2 Optical Test Equipment

Light is focussed onto the array using a small board mount lens, commonly used in commercial CMOS and CCD camera modules. This proved adequate for testing, but attenuated the light significantly, leading to long exposure times in the ambient office lighting of the lab.

Several specialised pieces of equipment were used for the optical testing. An integrating sphere, with an adjustable light source provided the flat field illumination required for the FPN and linearity tests. The sphere was also used in conjunction with a digital light meter to characterise the illumination/frequency relationship of the digital pixel. The spectral response of the pixel was determined with a monochromator, which was first characterised using the digital light meter.

5.3 Image Capture Operation

A normal image capture can be divided into two phases: the exposure, and the readout phase. Due to the nature of the conversion process, the exposure phase combines what would normally be divided into separate 'integrate' and 'convert' steps. The readout phase is simply accessing the digital data stored in the pixel array memory. Before describing these phases, the operation of the control lines will be reviewed. Figure 5.3 is the block diagram of the array, and symbolically represents

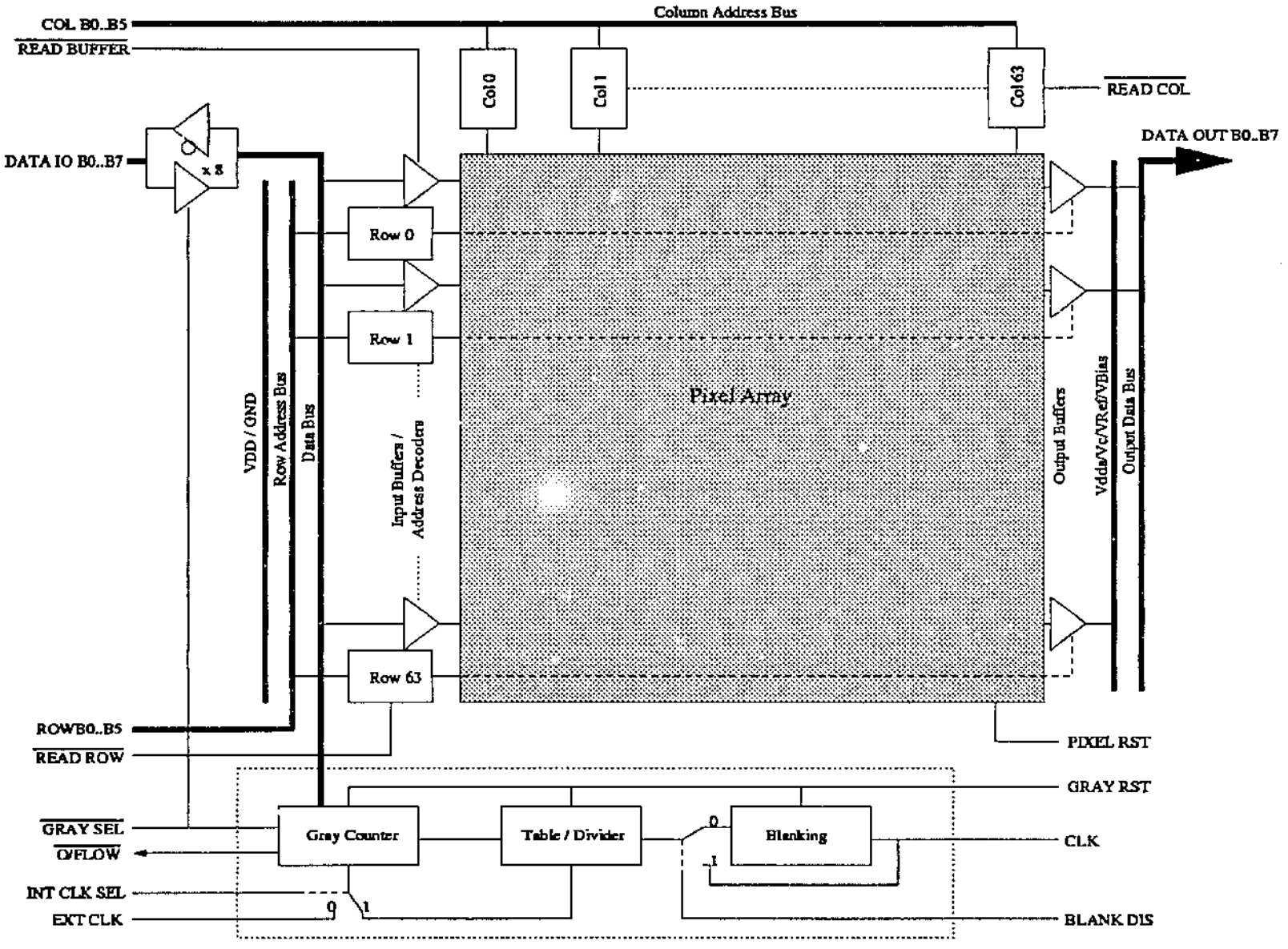


Figure 5.3: Operational block diagram.

the operation of the control lines. It is assumed in the following descriptions that a clock of an appropriate frequency, as determined in Section 3.4.1, is applied at the CLK input, and that the test control lines are set as follows:

$\overline{\text{GRAY SEL}} = 0$: This places the output of the internal Gray counter on the data bus, and sets the I/O port as an output.

INT CLK SEL $= 1$: This enables the internal circuit which produces the variable clock, used to drive the internal Gray counter.

BLANK DIS $= 0$: This enables the blanking counter.

For normal operation EXT CLK is not required, and may be held low, or connected in parallel with CLK. (The purpose of these test lines will be described more fully in Section 5.4).

5.3.1 Exposure Phase

To begin the exposure phase the control lines are set as follows:

$\overline{\text{READ BUFFER}} = 1$: Enables the input row buffers.

$\overline{\text{READ ROW}} = 1$: Disables the row address decoders and the output buffers.

$\overline{\text{READ COL}} = 1$: Disables the column address decoders.

In practice these lines can be tied together and treated as a single control line; they have been extracted individually to assist with the testing.

To begin the exposure phase, PIXEL RST and GRAY RST are pulsed high for not less than 20 ns. In practice this is somewhat arbitrary, as the primary clock period is very much larger than this, and a pulse in the microsecond range is perfectly acceptable. Pulsing the PIXEL RST line changes the state of the SR latch within the pixels, and starts the integration of the photocurrent. Pulsing GRAY RST resets the Gray counter to full scale and the blanking counter to zero.

The exposure can be terminated in one of two ways: by monitoring the $\overline{\text{O/FLOW}}$ line, or by timeout. A high to low transition on the $\overline{\text{O/FLOW}}$ line indicates that the

Gray counter has reached zero and the counter is about to overflow. Alternatively, the exposure can be stopped after a fixed time period, set in the controlling software. In both cases the procedure for terminating the exposure is to stop the primary clock.

If the exposure is halted after a fixed time period, there is one more step that must be performed. Pixels receiving low illumination may not have fired at this point, and may contain random data or data from a previous image. These must be overwritten with the value present on the data bus when the exposure is halted however there is no method to generate a write signal directly. The pixels must be forced to generate a write signal by 'bumping' V_{Ref} to a level very close to, bnt not exceeding, V_C. It is important that V_{Ref} does not exceed V_C, as this will cause all pixels to generate a write signal, destroying the image. In practice bumping V_{Ref} to within 95-97% of V_C is adequate for reliable operation.

5.3.2 Read Phase

Once the exposure phase has terminated, the image data can be read from the array by changing the state of the control lines:

$\overline{\textbf{READ BUFFER}} = 0$: Disables the input row buffers.

$\overline{\textbf{READ ROW}} = 0$: Enables the row address decoders and the output buffers.

$\overline{\textbf{READ COL}} = 0$: Enables the column address decoders.

Each pixel is addressed by its row and column position, and the image data read from the pixel memory. Prior to processing or display, the Gray data must be converted to true binary values. At present this is the only part of the reading process not performed on chip, and is achieved using a lookup table in the test software.

5.4 Control Circuit Test Strategies

As stated in Section 5.3, there are several control lines which are provided to assist in the testing and development of the array. The operation of the switches can be seen symbolically in Figure 5.3, and will be described here.

INT CLK SEL switches the clock input of the Gray counter between the internally generated variable clock (INT CLK SEL = 1), and the EXT CLK input (INT CLK SEL = 0). This is included for testing, fault finding and development. Should some part of the control circuit fail (most likely the lookup table), the algorithm for producing the variable clock can be executed externally, and the Gray counter can be driven by the EXT CLK input. It can also be used for comparison purposes to demonstrate the effect of a fixed clock on the conversion process. Alternatively algorithms which do not use the internal lookup table, but which use Gray encoded data can be tested using this input.

BLANK DIS causes the clock signal to bypass the counters used in the blanking circuit (BLANK DIS = 1), in case of circuit failure or to assist in fault finding. It can also be used in comparison tests, to demonstrate the effect of blanking on the conversion process.

$\overline{\text{GRAY SEL}}$ controls the output of the Gray counter, and the I/O port direction. In normal operation the Gray counter drives the input data bus, and the I/O port is set as an output ($\overline{\text{GRAY SEL}} = 0$). If the entire control circuit, including the Gray counter fails to operate satisfactorily, the output of the counter can be put into a high impedance state, and the I/O port set as an input ($\overline{\text{GRAY SEL}} = 1$). Data for the array can then be generated by a control circuit outside of the chip. This option can be used in testing, fault finding, and development of algorithms which do not use a Gray encoded data.

$\overline{\text{READ ROW}}$ primarily controls the row addressing circuits, however it can also be used in the functional testing of the array. As each row is addressed, the appropriate output buffer is enabled, all others being isolated from the output bus. During testing, the entire data path for each row can be enabled: from the Gray counter, through the input data bus, the row buffer, the pixel row bus, the output buffer and to the output port. This can be used in fault finding and in characterisation of the bus delays.

There are also two output test lines, which for clarity, have not been shown in Figure 5.3: GROUP OUT and ROW OUT. The address decoding for the array is

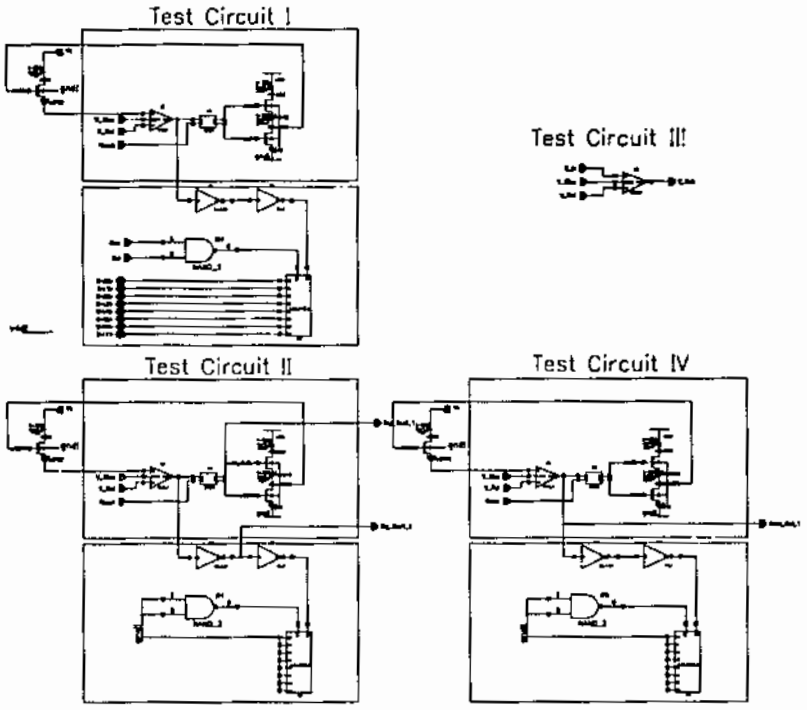


Figure 5.4: Test structure schematics. Test Circuit I is a complete pixel digital pixel. Test Circuit II provides digital access to the first buffer stage, and the SR 'Q' output. Test Circuit III is a single analogue comparator. Test Circuit IV extends the analogue comparator output from the digital pixel.

designed in a modular fashion, to allow for flexibility in the array sizing. Sixteen rows (or columns) form one group, decoding the four least significant bits of the address. Then the next most significant bits in the address are decoded, and used to enable these groups. ROW OUT is the decoded output from the first row decoder (row zero), and GROUP OUT is the output from the last group decoder in the column. These are only included for testing and evaluating the performance of the decoders.

5.5 Pixel Test Structures

Included on-chip, but entirely separate from the array, are a series of test structures which allow access to the pixel circuit at successive points in the signal path, the schematic drawing of the test circuits appears in Figure 5.4. Due to the loading that

bonding pads place upon circuit elements there is almost an uncertainty principle involved in testing, where pads placed to allow monitoring of the circuit inevitably degrade that circuit's performance. This series of test structures provide signals that would almost certainly cause the failure of the pixel in normal operation. These are intended to allow characterisation of the pixel performance, and also as a 'fall-back' in case of catastrophic failure of the main circuits. These circuits are completely disconnected from the main array, having separate power and signal lines.

Test Circuit I is an entire pixel, with all digital lines extended, but without any additional access points. It is intended to test the operation of the digital pixel, should the array fail to operate due to bus loading effects. It can also be used to test the operation of the memory and the address decoding circuits.

Test Circuit II is a single pixel, which allows access to the internal digital outputs from the SR latch, and the first inverter after the comparator. The output of the SR latch can be used as an analogue representation of the integration time that can be measured with a DSO. This is an important characteristic required for linearity testing, and pixel characterisation.

Test Circuit III is a single comparator circuit, extending the input and output through analogue pads. This can be used to characterise the comparator performance, although consideration must be given to the effect of the analogue pad in any tests employing this structure.

Test Circuit IV is a single pixel, extending the output of the comparator through an analogue pad. This can be used to determine the comparator performance, with the photodiode as input. The same consideration must be given to this circuit as Test Circuit III regarding the analogue pad loading effects.

5.6 Control Circuit Testing

The control circuit is tested by driving the CLK input with a series of pulses, while monitoring the data on the input data bus via the I/O port. After each clock pulse, the digital value is read, converted to binary, and stored in a text file. Figure 5.5 is the sorted result, showing the lookup table multiplier for each data value. This test

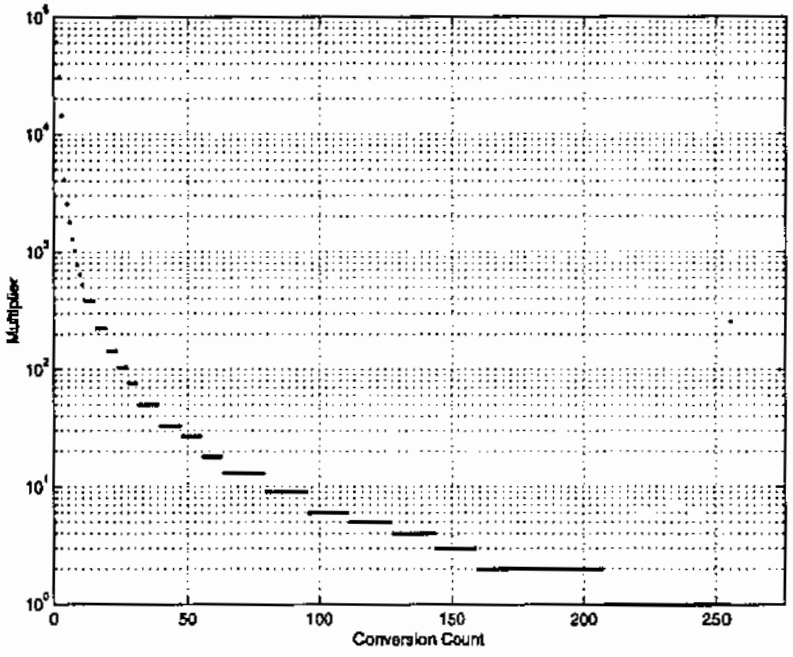


Figure 5.5: Test results: control circuit functional test. Plot of the lookup table multiplier value versus the conversion count.

confirms the operation of the control circuit, including the blanking counter, the lookup table, the period multiplier and the Gray counter. The range and multiplier values are listed in Appendix A.

From these figures the time required for any exposure can be determined, by summing the number of clock cycles that are required for each digit in the conversion. For example, if the exposure is to be terminated when the counter reaches 35 (digit range 255 - 35, or 220 discrete levels), 1862 clock pulses are required. Regardless of the illumination level and the clock frequency required to resolve it, the exposure can be consistently controlled by counting the number of primary clock pulses, rather than the exposure time.

5.7 Digital Pixel Sensor Testing

This section describes the results obtained using the pixel test structure, in particular using the SR 'Q' output of Test Circuit II, which is used to provide an analogue

representation of the integration time. This is used to characterise the response of the pixel itself, without the constraints of quantisation. Each chip contains one test circuit which can provide the latch output signal, so each test is performed on a number of chips to account for variations due to the manufacturing process.

5.7.1 Test Circuit Signals

Outputs from the test circuits which have been captured by the DSO, and formatted for display appear in Figure 5.6. Zero on the time axis refers to the triggering point of the DSO. Figure 5.6(i) is the output of the comparator as it triggers, (ii) is this signal after buffering by the first inverter. Note that the analogue output from the comparator is distorted due to the large loading of the analogue pad, unlike the digital signal which is buffered by the standard cell digital pad.

The integration time, as indicated by the 'Q' output of the SR latch, appears in Figure 5.6(iii). The operation of the ADC can be understood by comparing this with Figure 5.6(iv), which is bit '0' of the data bus, measured at the I/O port of the array. When the pixel is reset, the SR 'Q' output goes low, allowing the pixel to integrate the photocurrent. At the same time the data is being generated by the control circuit, the period of the clock expanding at the same rate as the integration time. When the pixel triggers, the pixel memory stores the state of the data bus at that instant.

5.7.2 Conversion Linearity

One of the primary goals of the design is to linearise the conversion process, in order to compensate for the $1/I_D$ nature of the integration time. Plotting the digital result against the inverse of the integration time should produce a linear response if the ADC is working correctly, which can be seen in Figure 5.7. The integration time is measured using Test Circuit II, while the digital result of the ADC is read from an adjacent pixel at the edge of the array. The chip is uniformly illuminated, and it is assumed that the same illumination falls upon the test circuit and the pixel, due to their proximity. For a given primary clock frequency, the illumination

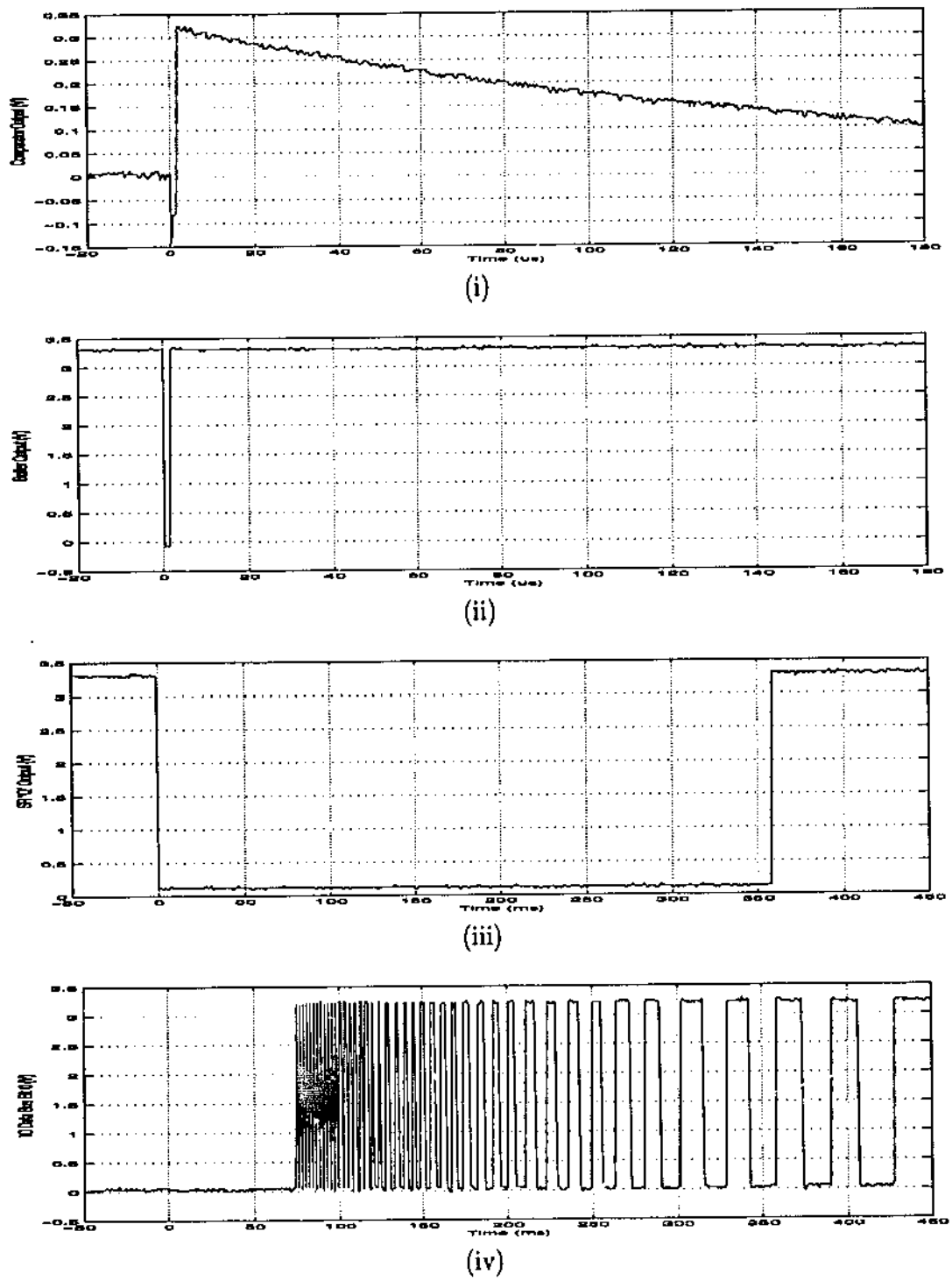


Figure 5.6: Test results: Test circuit outputs captured by the DSO. (i) Comparator output. (ii) Buffer output. (iii) SR 'Q' output, giving the integration time. (iv) Data bit B0.

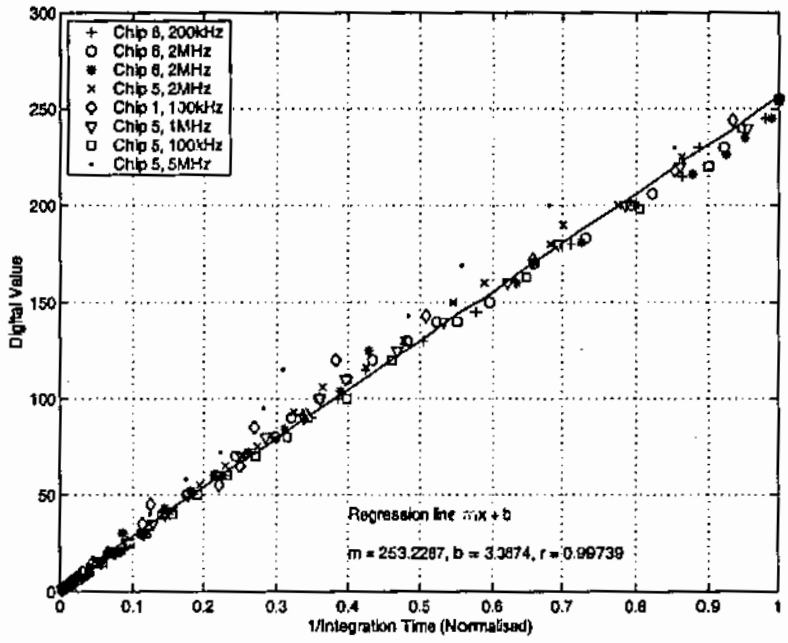


Figure 5.7: Test results: digital pixel value vs 1/integration time, demonstrating the conversion linearity.

is stepped through the full digital range of the ADC, while the integration time recorded at each step. The integration time is then normalised, with the reading at full scale being taken as '1', so that a number of results from different chips and clock frequencies can be plotted on the same axis. Figure 5.7 plots the results for three chips, with clock frequencies ranging from 100 kHz to 5 MHz. A straight line has been fitted to the data using the method of least squares.

5.7.3 Dark Current

The dark current is the leakage current that flows in the photodiode without illumination, mainly due to thermally generated carriers, which sets a lower limit on the operation of the array. It is difficult to measure the dark current in a digital pixel sensor, as there is no direct access to the photodiode, and it can only be derived from other measurements. Consider Eq.(3.5),

$$I_D = -C_J \frac{dV_C}{dt}$$

where dt is the integration time (which in this case will be termed the *dark time*) measured from the 'Q' output of Test Circuit II. The voltage dV_C is the difference between V_C (1.3 V) and V_{Ref} (0.9 V). The junction capacitance, C_J, is estimated from circuit simulations at approximately 172 fF. It is important to note that this is only an estimation, and C_J is subject to the usual uncertainty caused by variations in the manufacturing process. The dark voltage rate has been included to expresses the discharge rate of the junction capacitance in Volts per second, without the capacitance estimation. It is also reasonable to suggest that the dark current determined from these tests is due to several factors, of which the photodiode is only the primary source. The results are intended to demonstrate that the assumption made regarding the photocurrent being the dominant current in the photodiode holds in most cases, where the exposure times are very much less than those recorded here.

The test is performed by blocking all light from the array, resetting the pixel, and measuring the dark time with the DSO. The test is run ten times for each chip, the mean dark time is calculated, and the dark current determined from Eq.(3.5). The results are listed in Table 5.2.

Chip ID Number	Mean Dark Time (s)	Standard Deviation (s)	Dark Voltage Rate (mV/s)	Estimated Dark Current (fA)
1B	37.28	1.0	10.72	1.8
2	39.7	1.0	10.08	1.7
2B	46.8	0.45	8.54	1.5
3	38.75	0.85	10.32	1.8
6B	42.62	1.98	9.38	1.6
Mean Values			9.8	1.68

Table 5.2: Dark current results: chips 1B, 2, 2B, 3, and 6B.

5.7.4 Primary Clock Frequency

Using Test Circuit II, the integration time was calibrated against a digital light meter, using a variable light source, without the board lens or lens mount. Figure 5.8 is the result of three runs, over the maximum range of illumination available,

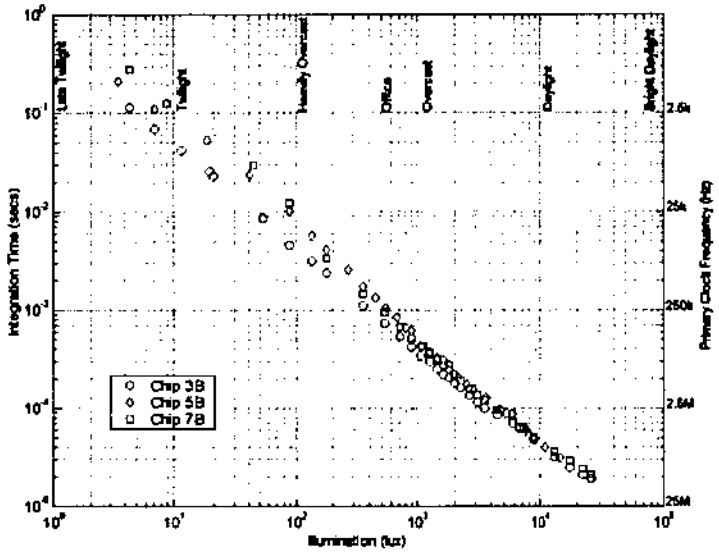


Figure 5.8: Test results: integration time and primary clock frequency vs illumination.

although it appears that the equipment fell short of the maximum illumination that can be resolved by the digital pixel. The figure is plotted in log/log scale due to the range of both the integration time, and the illumination level. The figure has also been annotated with a qualitative appreciation of the illumination (twilight, daylight etc.), and the appropriate primary clock frequency, given by Eq.(3.12). From these results it can be seen that the sensor has a dynamic range of at least 85 dB.

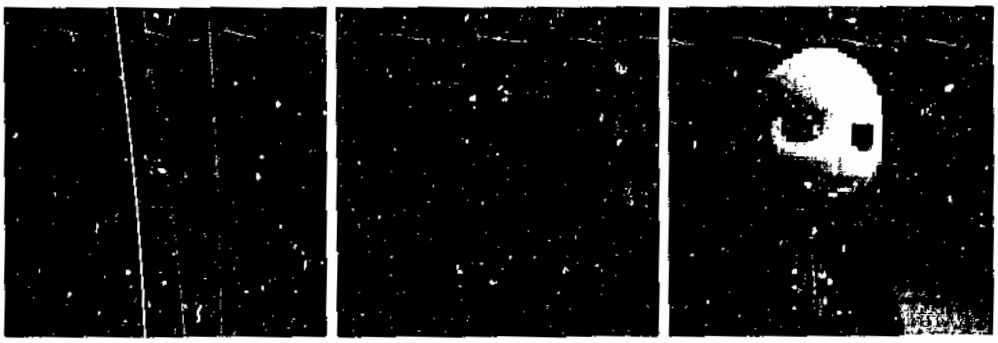
5.8 DPS Array Testing

This section presents results produced by reading the contents of the entire pixel array. In some cases an image is produced, by focussing light onto the array with a lens. In other cases the array is flat field illuminated, where a diffuse light source is to illuminate all pixels in the array uniformly. The captured 'image' shows the variability in pixel characteristics across the array, used in FPN testing, or when averaged gives an mean value for the incident illumination.

Figure 5.9: Closeup image of the Australian fifty dollar note, a portrait of Edith Cowan. This image is read directly from the DPS array with no FPN correction or post-processing. The smaller image gives a better appreciation of the image quality, considering the low resolution of the array.

5.8.1 Image Capture

Images are captured using the method described in Section 5.3.1, stored and displayed as bitmap (.bmp) files. The small board-mount lens attenuates the illumination significantly, resulting in a clock frequency of 2.5 to 8 kHz in office light, depending upon the subject matter. In all of the images presented here the fixed time exposure method is used, terminating the exposure phase typically after approximately 500 ms. This long exposure time is required as the images are captured without any supplemental lighting, relying on the office lighting only. Figure 5.9 is a sample bitmap image, with no post-processing of any kind (save for the Gray to binary conversion required for display). This closeup image of the fifty dollar note was taken with a clock frequency of 2.5 kHz and $V_C - V_{Ref} = 0.8V$. The simulation in Section 3.4.3 which demonstrated the effects of the various timing parameters is repeated using the actual array in Figure 5.10. The images were generated by using the BLANK DIS and INT CLK SEL lines to reconfigure the control circuit. In Figure 5.10(i) the image is captured using a fixed clock, without a blanking period. As



(i) (ii) (iii)

Figure 5.10: Three images of 'Po' repeating the demonstration of Section 3.4.3. The settings are (i) fixed clock without blanking, (ii) fixed clock with blanking and, (iii) variable clock with blanking. Primary clock frequency for all three images is 2kHz, with $V_C - V_{Ref} = 800$mV. The images are read directly from the array with no FPN correction or post-processing.

in the simulation, only the brightest points of the scene appear in the image. With the blanking enabled in Figure 5.10(ii) the conversion now covers the appropriate illumination range, but the nonlinear response of the fixed clock resolves only the brightest regions of the scene. The dynamic range of the conversion is approximately half that of the linear response. Both the variable clock and blanking are enabled in Figure 5.10(iii), with the captured image now displaying the full range of grey levels available from the 8-bit conversion.

5.8.2 Fixed Pattern Noise

The fixed pattern noise for a digital pixel sensor can be defined as the standard deviation of pixel values from the array mean, under flat field illumination. The flat field is generated by an optical sphere, with the illumination level adjusted to give an average array value in the mid range of the ADC. In order to remove any temporal variation caused by the pixels, or by the timing of the operating system, two hundred flat field images were captured, summed and averaged. To minimise any localised variation in illumination, the average array value was calculated over a region of 5 × 5 pixels, centered around the pixel under test. Figure 5.11 plots the histograms for four chips, with $V_C - V_{Ref} = 0.9$ V. The FPN level varies with

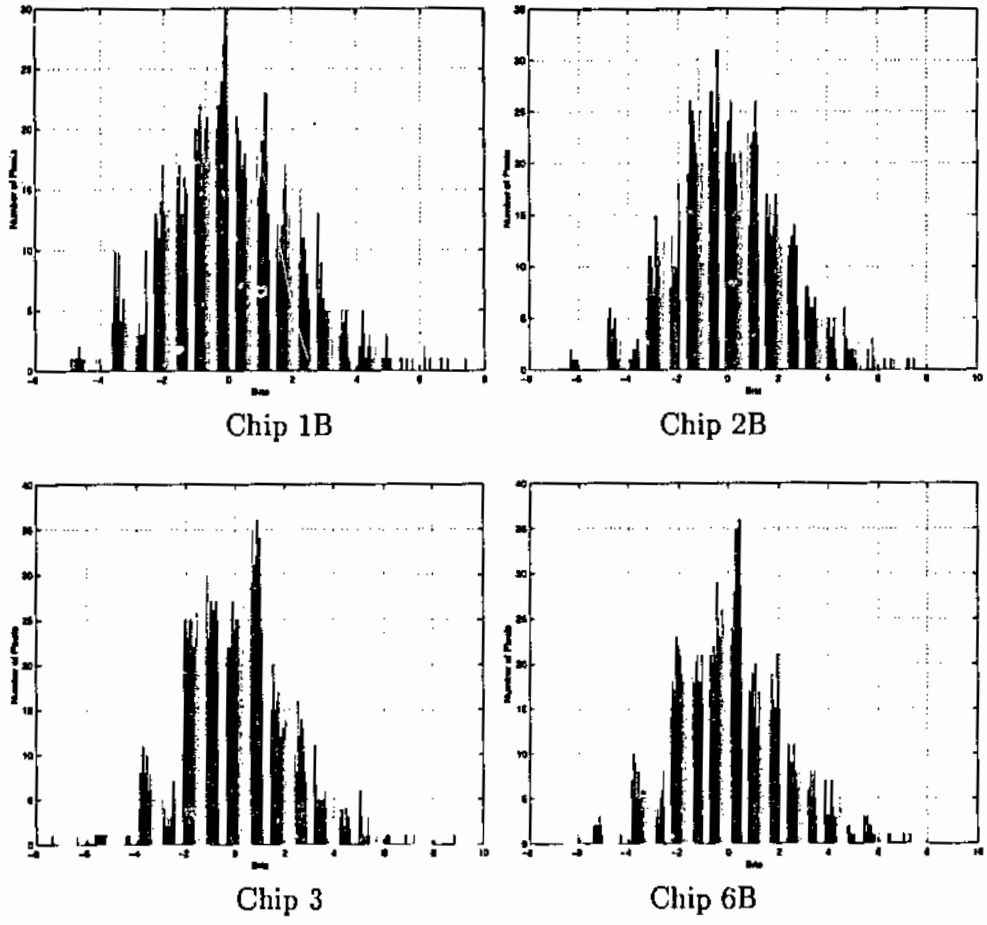


Figure 5.11: Test results: deviation of digital pixel value from local mean, $V_C - V_{Ref}$ = 900 mV

the range of $V_C - V_{Ref}$, the level of FPN increasing as the voltage range decreases. This implies that the FPN is a fixed offset, the most likely source being the reset transistor. This is difficult to verify due to the inability to access any analogue signals from the pixel, and can only be investigated through extensive simulation. The digital value, which is a relative measure, is converted to an absolute value by dividing the voltage range $V_C - V_{Ref}$ by the resolution of the counter, in this case

$$\frac{900 \text{ mV}}{255} = 3.53 \text{ mV/bit} \tag{5.1}$$

and converting the standard deviation figure from bits into Volts. The results for the distributions of Figure 5.11 are listed in Table 5.3.

Chip ID Number	Standard Deviation	
	Bits	Voltage (mV)
1B	1.73	6.10
2B	1.92	6.70
3	1.76	6.20
6B	1.80	6.35

Table 5.3: FPN results: chips 1B, 2B, 3, and 6B, $V_C - V_{ref} = 0.9$ V.

5.8.3 Adaptation

The adaptation mechanism is best demonstrated by example: Figure 5.12 shows a series of views of the courtyard outside the Edith Cowan University Vision Lab window. In Figure 5.12, the exposure is adjusted using only the clock frequency, and begins with the clock set too low for the interior lighting, resulting in the image being overexposed. As the frequency is increased, the exposure is suitable first for the office light, and then for the exterior daylight, seen through the window. Finally, the clock is set too high, and the last image of the courtyard is underexposed. The discrepancy between the frequencies listed in Figure 5.8 and this demonstration is again due to the attenuation of the small 'board mount' lens. Figure 5.13 shows two images of a 20 W halogen lamp, in closeup. In Figure 5.13(i) the lamp is off and the clock is set to 2.5 kHz, for the low ambient light. With the lamp turned on in Figure 5.13(ii), the clock must now be set to 500 kHz, which permits a view of the hot filament of the incandescent bulb. An example of how a wide dynamic range image can be formed is shown in Figure 5.14. The first image in the series, Figure 5.14(i), depicts a normal capture where the scene is uniformly lit, and correctly exposed. The same scene appears in Figure 5.14(ii) and (iii), this time brightly lit from one side. In Figure 5.14(ii) the left region of the image is correctly exposed, while the right region is overexposed, with little detail visible. In Figure 5.14(iii), the blanking counter is disabled by setting the BLANK DIS line high. The previously overexposed side is now visible, the penalty being that the image appears flat, and 'washed' out. Disabling the blanking counter begins the conversion as soon as the array is reset, and the very bright regions that are normally 'blanked out' are now

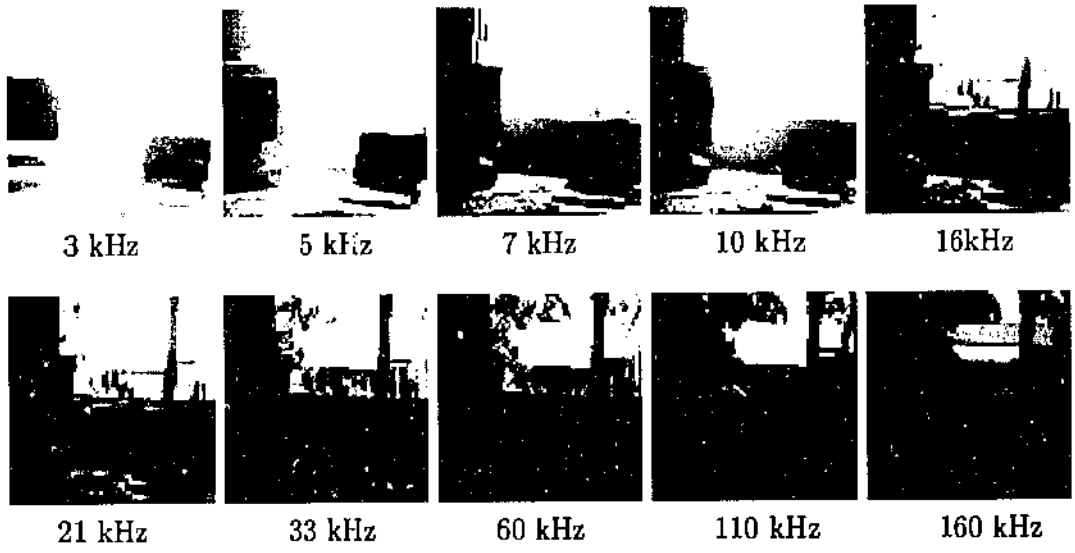


Figure 5.12: The response of the DPS array is adapted to different lighting conditions by changing the primary clock frequency. As the frequency is increased, the level of light being resolved changes from the office lighting of the image foreground, to the bright daylight of the courtyard, seen through the window. Images are read directly from the DPS array, with no FPN correction, or post-processing. $V_C - V_{Ref}$ = 800 mV, and the primary clock frequency appears under each image.

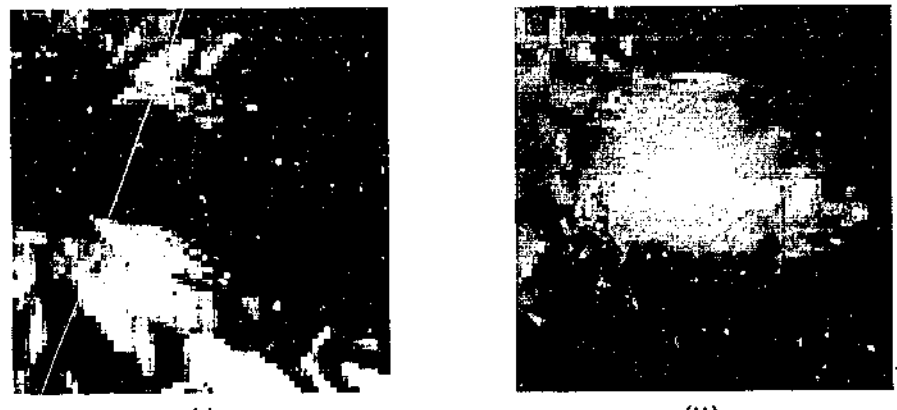


Figure 5.13: (i) Closeup image of a 20 W halogen lamp taken in room light with the lamp off. The primary clock frequency is 2.5 kHz. (ii) Now with the lamp on, and the clock frequency increased to 500 kHz. Images are read directly from the DPS array, with no FPN correction, or post-processing. $V_C - V_{Ref}$ = 800 mV.

(i) (ii) (iii)

Figure 5.14: Three images of 'Po', demonstrating a wide dynamic range capture. (i) Reference image, normal capture and uniform illumination. (ii) A normal capture with the subject brightly lit on one side. (iii) The same lighting as (ii), but this time with the blanking disabled. In all images primary clock frequency = 2 kHz, $V_C - V_{Ref} = 800$ mV.

part of the conversion. The variable clock and the long exposure time mean that a wide range of photocurrents can be converted, but they are not resolved. The primary clock frequency remains the same, so the wide range of photocurrents are not being digitised with a linear response. This extends the upper range of the ADC, but as the pixels only contain 8-bit memories, the quantisation step sizes become large and the image appears 'washed out' or flat. While this severely affects the aesthetic quality of the image, it does have applications in machine vision where a linear response is not always desired.

5.8.4 Spectral Response

To determine the spectral response of the array, a monochromator was first characterised by measuring its output with a digital light meter across the spectrum from $\lambda = 400$nm, to $\lambda = 1000$nm, in 50nm steps. The array was then flat field illuminated using the output of the monochromator, stepped through the spectrum, and the average value of the entire array calculated and recorded for each wavelength. These results were corrected using the characteristics of the monochromator, and normalised, with the maximum response being equal to '1'. The results are shown in Figure 5.15.

Figure 5.15: Test results: spectral response of the DPS array.

5.8.5 Array Power Consumption

The test PCB is provided with removable links, so that a current shunt can be connected in series with each voltage rail, and the current measured. Static current measurements are made using a digital current meter with a full scale deflection of 200 μA, and a resolution of 0.1 μA. Dynamic current measurements are made by placing a resistive shunt in the current path, amplifying the voltage drop across the shunt using an instrumentation amplifier, and recording the amplifier output with the DSO. Table 5.4 lists the results of the static measurements, which are recorded with the array in an idle state (the control lines set for exposure).

It should be noted that the quiescent current drawn from the V_{dda} supply has a strong dependence upon the level of the comparator bias voltage V_{Bias}. This is demonstrated in Figure 5.16, where the importance of operating the array with the lowest possible value for V_{Bias} is obvious. The optimum value was found to be approximately 0.33 V; below this level the operation of some pixels is marginal, and intermittent corruption of the image occurs. The dynamic behaviour of the array

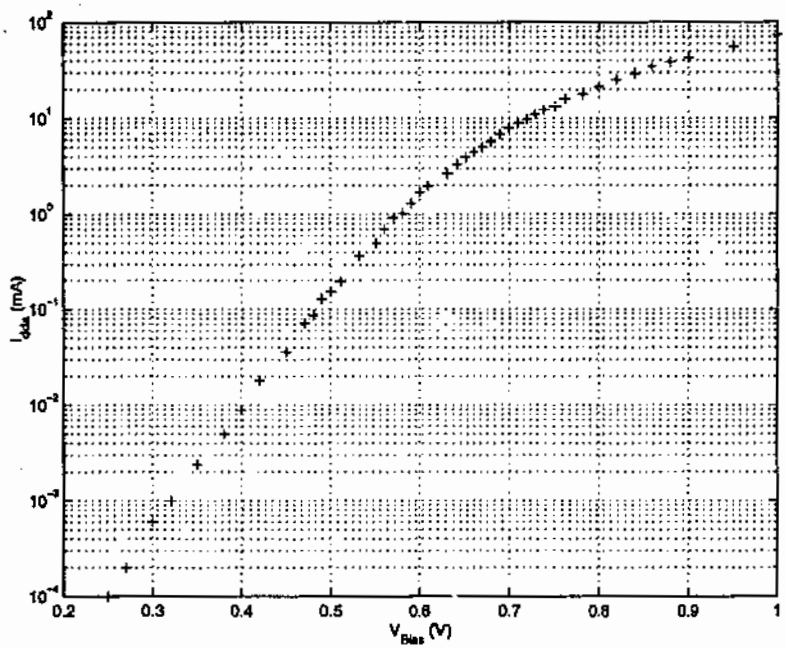


Figure 5.16: Test results: quiescent analogue supply current, I_{dda}, versus the comparator bias voltage, V_{Bias}.

is dominated by the current drawn from the digital supply V_{dd}, which is heavily dependent upon the nature of the image captured, but largely independent of the internal timing of the control circuit. The digital supply current, I_{dd}, is drawn as the pixel comparators are triggered, and the pixel memories store the data. Figure 5.17 shows the current drawn from the V_{dd} supply when exposed to an image containing two distinct regions: 50% light and 50% dark. As the integration time is inversely proportional to the illumination, bright regions appear at the left of the plot, dark

Voltage Supply	Voltage	I_Q
V_{dd}	3.3 V	0.5 μA
V_{dda}	3.3 V	8.8 μA
V_{dde}	3.3 V	5 mA
V_C	1.5 V	$< 0.1\mu$A
V_{Bias}	0.4 V	$< 0.1\mu$A
V_{Ref}	1.3 V	$< 0.1\mu$A

Table 5.4: Test results: supply and bias line quiescent current.

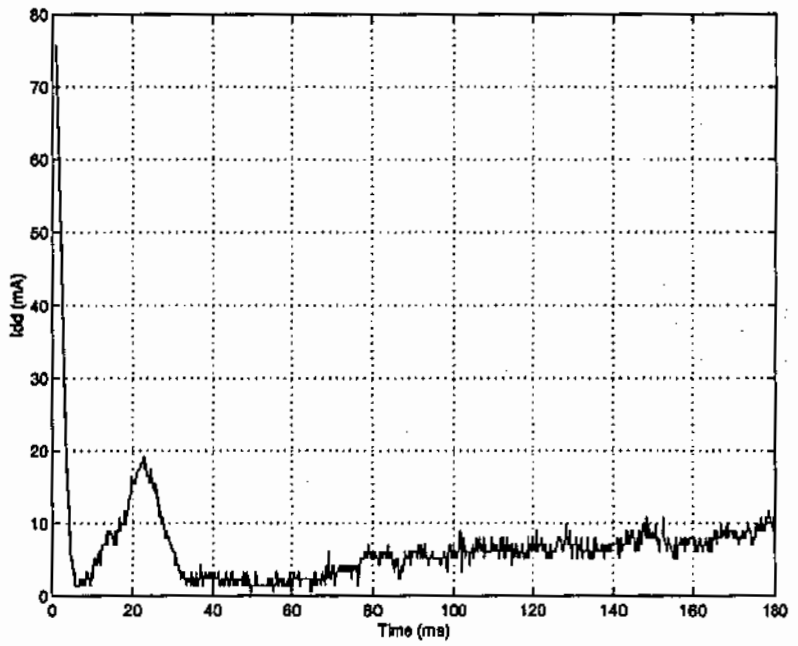


Figure 5.17: Test results: plot of the digital supply current I_{dd}, during the exposure phase. The image contains two distinct light and dark regions.

regions at the right. The dark region is less clearly defined, as the $1/I_D$ nature of the pixel response spreads the current consumed by the pixel memory in time. Figure 5.17 does show some promise as a histogramming function, however several factors must be considered before this can be seriously proposed as a feature of the conversion process:

1. The time scale must be corrected to account for the $1/I_D$ response.

2. The current scale must be corrected to account for the variability of the data ('11111111' draws more current than '00000000', assuming that the memory is initialised with '00000000').

3. This is a by-product of a poor memory design, and would not occur with a memory that is more efficient in power and area.

It should also be noted that the internal control circuit modifies the timing of the data that is presented to the pixel array, but does not change the behaviour of the

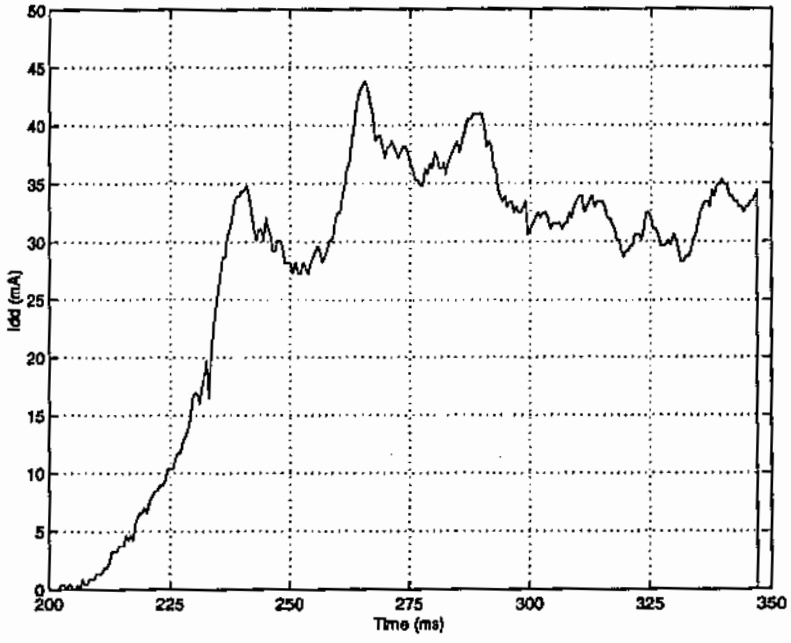


Figure 5.18: Test results: plot of the digital supply current, I_{dd}, during the readout phase.

pixels themselves. For example, in making the plot for Figure 5.17, the array has a primary clock frequency of 6 kHz, and a blanking time of 42 ms, therefore all pixels which trigger before the 42 ms mark store the same digital value, the reset value of the Gray counter. The response of I_{dd} is for the scene, rather than for the representation of the scene that is captured by the array, and the two may be completely unrelated. There is no definitive figure that can be placed upon I_{dd} during the exposure period, but repeated exposures of different scenes indicate that the average falls between 7 mA and 20 mA per image.

Figure 5.18 shows the trace for I_{dd} during the readout phase, indicating an average consumption of between 25 mA and 35 mA. This level could be reduced as it is largely due to the use of transmission gates to isolate the output buffers from the data bus. The nodes between the buffers and the transmission gates still have significaut capacitance, and consume power even when disconnected from the data bus. Alternative designs which actually disable the output buffers, rather than just isolating them, would reduce this consumption significantly. Considering the

two phases together, and including the static consumption of the pad supply, V_{dde}, a pessimistic figure for the power consumption is approximately 110 mW per image.

The array was also tested with scaled voltage supplies and performed successfully down to 2.3 V, without any perceived degradation in the image quality, although no quantitative results were recorded. Below this level the array failed to operate, probably due to the output signals failing to reach the threshold levels of the NIDAQ interface cards. It was considered unwise to continue the test for any length of time, as the logic input levels from the NIDAQ cards could not be scaled without major modification to the test PCB, and at 1 V above V_{dd} were well outside the safe operating range specified by the manufacturer. However, this does demonstrate the ability of the circuit to perform under less than optimal conditions, such as when powered by a portable battery supply.

5.9 Discussion

The testing of the DPS array has confirmed the theory of operation of the ADC process, and the VLSI implementation, with all systems on the chip working as anticipated. However, as with any prototype design, it can only be regarded as a qualified success, with several issues arising from its operation that must receive criticism.

Operating the device has proven to be very simple, with a minimal amount of external control required. The main difficulty in the operation is the process required to clear the memory after a fixed time exposure, where V_{Ref} is raised to force a memory write. At present this is performed using a DAC, but this could be simplified by the use of a FET switch, and a voltage divider. The time domain ADC technique has proven to operate as expected, as demonstrated by the discrete pixel tests, and the quality of the captured images in general. The digital pixel performed very well, considering the modest fill factor of only 12 %, and the 0.35μm technology appears to have excellent optical characteristics. The main advantage of the digital pixel design is the ability for it to cover a wide range of light levels without blooming or saturation, as demonstrated in Section 5.8.3.

The fixed pattern noise level is considered acceptable, in that the array can be used to develop and simulate on-chip processing algorithms, without the need for digital correction techniques that would require a duplicate memory. One issue that has arisen is that if the FPN is to be kept at an acceptable level, $V_C - V_{Ref}$ must be in the order of 0.7 to 0.9 V, resulting in long exposure times.

The power consumption is higher than need be, but this is understandable as it arises from the rudimentary memory design. It has been mentioned several times that the memory design was a compromise, and a matter of expediency, given the time available. It must be stated that it is probably due to this conservative approach that the array performs as well as it does, as most time was spent on the analogue pixel design, which has performed very well. The ability of the array to operate well below the standard 3.3 V logic levels of the 0.35μm technology is one method by which the overall power consumption could be reduced.

5.10 Conclusion

This chapter presented the results of testing the DPS array. Important characteristics of the performance such as dark current, FPN, linearity and spectral response were measured and documented. Sample images were presented and the ability of the ADC to adapt to a wide range of illumination levels using only the clock frequency was demonstrated. The optical results proved to be very good, while the electrical results were as to be expected, considering the decision that were made during the VLSI implementation stage of the design, with particular regard to the memory.

Chapter 6

Conclusion and Further Work

6.1 Thesis Summary

This thesis presented a digital pixel sensor array, in which time is used as the variable in the analogue to digital conversion. The two central elements of the design are the self resetting digital pixel, and the data control circuit. The digital pixel combines a photodiode, a comparator, memory and addressing logic, with each pixel operating asynchronously. The pixel is self resetting, which conserves charge, prevents blooming, and permits the sensor to operate over a wide range of lighting conditions. The control circuit is common to the entire array, and generates data with variable clock timing, to compensate for the inverse photocurrent/integration time relationship.

A 64 × 64 pixel array with 8-bit resolution was manufactured in 0.35μm, 3.3 V CMOS technology. Each pixel occupies an area of 45μm × 45μm, with the total array, including the control circuit and test structures, measuring 3.7mm × 3.9mm. The array has been tested, and found to operate as anticipated, with the control circuit compensating for the nonlinearity of the integration time. Important characteristics such as FPN, dark current, frequency response, dynamic range and spectral response have been measured. Images captured by the array have also been presented that demonstrate the image quality, and the adaptability of the ADC to a wide range of lighting conditions.

6.2 Further Work

Testing of the array has raised several issues regarding the operation of the digital pixel sensor and the time domain ADC process. These will be addressed first, before describing the next stage in the development of the project.

Some obvious and basic improvements are required to increase the electrical efficiency of the design, in particular the digital data path. Improving the memory will require a major redesign of the data path: replacing the data buffers with sense amplifiers, and redesigning the pixel. This is essential if all of the advantages of the CMOS design are to be realised.

It was stated at the beginning of the thesis that the intention of the DPS array is not to produce an imager that can produce high quality, high resolution images, but one which can perform on chip image processing, more applicable to industry than the consumer market. The images produced must be of sufficient quality to reliably perform segmentation, edge detection and other fundamental processes. It was demonstrated in Section 5.8.2 that the fixed pattern noise is related to the difference between the reset voltage, V_C, and the reference voltage, V_{Ref}. This voltage span must be large if the level of FPN is to be kept at an acceptable level, to perform the intended tasks reliably. This leads to long exposure times, which at the moment can only be reduced by supplemental lighting, or off-chip digital correction, both of which go against the intention of the project. In future designs some method of on-chip CDS must be implemented if the FPN is to be reduced, which in turn will allow faster exposures.

Accepting the shortcomings of the present design, the chip does provide a useful prototype for the testing of processing algorithms. The next stages in the project are envisaged to be the following:

1. Replace the current National Instruments interface with a microcontroller, for greater flexibility in its operation and tighter control of the conversion timing.

2. Develop and test nonlinear ADC processes which increase the dynamic range of the image, using both fixed and dynamic data timing.

3. Develop and test processing algorithms, using techniques which can be implemented on-chip.

4. Implement the processing in a larger and more efficient DPS array, with an improved memory design.

6.3 Closing Remarks

The time domain ADC used in this DPS array is not seen as a replacement for traditional voltage based techniques. In some areas it performs very well, in others it does not. However, the architecture of the DPS array is not limited to the ADC technique described here, and operational flexibility is seen as its main advantage. It is foreseen that time domain ADC will be one of many operations that a future design will have at its disposal, in order to provide the greatest possible utility in the widest range of applications.

Appendix A

Lookup Table Entries

This appendix contains the range and multiplier values stored in the internal lookup table, used to approximate the photocurrent/integration time relationship. The table lists the multiplier, and the ranges over which the multiplier applies. (For example, the counter values 79 through to 64 each require 13 clock periods to decrement the Gray counter.)

Counter Range	Multiplier	Counter Range	Multiplier
255 - 208	1	19 - 16	224
207 - 206	2	15 - 12	384
159 - 144	3	11	528
143 - 128	4	10	640
127 - 112	5	9	784
109 - 106	6	8	1024
95 - 80	9	7	1280
79 - 64	13	6	1792
63 - 56	18	5	2560
55 - 48	27	4	4096
47 - 33	33	3	14326
39 - 32	50	2	30720
31 - 28	76	1	61440
27 - 20	144	0	O/FLOW

Table A.1: Lookup table values, listed in descending order.

Appendix B

Pin List

This appendix lists the number, label, direction and description of each pin in the JLCC84 package. The lines are grouped by function: control, addressing, data, and power. Pins accessing the test structures are listed separately. The pin labels refer to figure B.1.

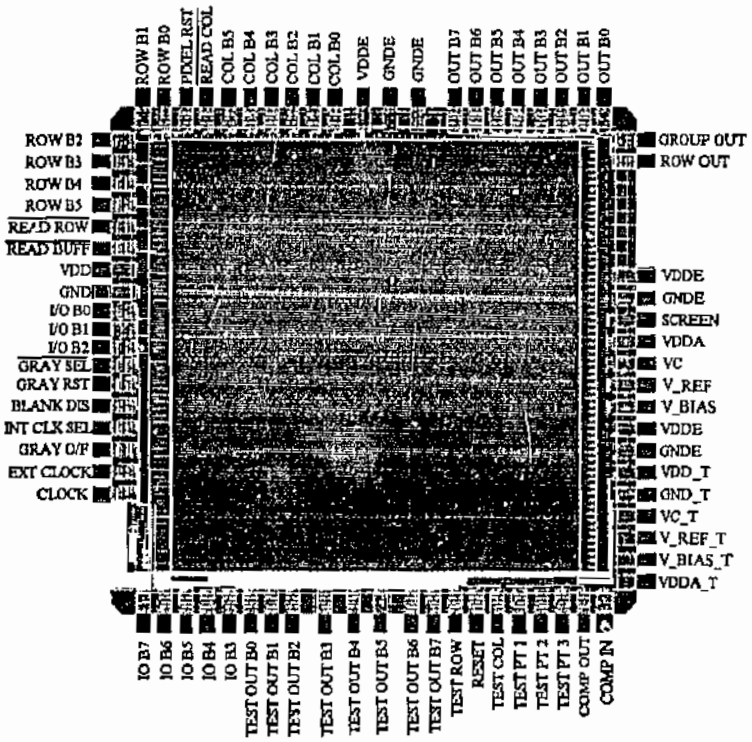


Figure B.1: Bonding pad diagram.

Pin	Label	Direction	Function
2	GRAY SEL	I	Enables Internal Gray Counter.
3	GRAY RST	I	Gray counter reset.
4	BLANK DIS	I	Disables blanking counter.
5	INT CLK SEL	I	Enables internal variable clock generator.
6	GRAY O/F	O	Gray Counter overflow flag.
7	EXT CLOCK	I	Selected when INT CLK SEL = 0.
8	CLOCK	I	Primary clock input.
71	$\overline{\text{READCOL}}$	I	Enable column addressing.
72	PIXEL RST	I	Pixel array reset.
79	$\overline{\text{READROW}}$	I	Enable row addressing.
80	$\overline{\text{READBUFF}}$	I	Enable output buffers.

Table B.1: Control pin table.

Pin	Label	Direction	Function
65 - 70	COL B0 - B5	I	Column address lines, bit 0 - bit 5.
73 - 78	ROW B0 - B5	I	Row address lines, bit 0 - bit 5.

Table B.2: Address pin table.

Pin	Label	Direction	Function
1	I/O B2	I/O	Data bus I/O port bit 2.
12	I/O B7	I/O	Data bus I/O port bit 7.
13	I/O B6	I/O	Data bus I/O port bit 6.
14	I/O B5	I/O	Data bus I/O port bit 5.
15	I/O B4	I/O	Data bus I/O port bit 4.
16	I/O B3	I/O	Data bus I/O port bit 3.
83	I/O B0	I/0	Data bus I/O port bit 0.
84	I/O B1	I/O	Data bus I/O port bit 1.
54 - 61	OUT B0 - B7	O	Output bus bit 0 - bit 7.

Table B.3: Data pin table.

Pin	Label	Direction	Function
39	GNDE	I	Bonding pad ground.
40	VDDE	I	Bonding pad power.
41	V_BIAS	I	Pixel comparator bias, V_{Bias}.
42	V_REF	I	Pixel comparator reference, V_{Ref}.
43	VC	I	Photodiode reset voltage, V_C.
44	VDDA	I	Core analogue supply, V_{dda}.
45	SCREEN	I	Not used.
46	GNDE	I	Bonding pad ground.
47	VDDE	I	Bonding pad power.
62	GNDE	I	Bonding pad ground.
63	GNDE	I	Bonding pad ground.
64	VDDE	I	Bonding pad power.
81	VDD	I	Core digital supply, V_{dd}.
82	GND	I	Core ground.

Table B.4: Power pin table.

Pin	Label	Direction	Function
17 - 24	TEST OUT B0 - B7	I/O	Test pixel I/O bit 0
25	TEST ROW	I	Row address line.
26	RESET	I	Test pixel reset.
27	TEST COL	I	Column address line.
28	TEST PT 1	I	Pixel SR 'Q' output.
29	TEST PT 2	I	Pixel Inverter output.
30	TEST PT 3	I	Pixel comparator output.
31	COMP OUT	I	Comparator output.
32	COMP IN	I	Comparator input.
33	VDDA_T	I	Test circuit analogue supply.
34	V_BIAS_T	I	Test circuit bias voltage.
35	V_REF_T	I	Test circuit reference voltage.
36	VC_T	I	Test circuit photodiode voltage.
37	GND_T	I	Test circuit ground.
38	VDD_T	I	Test circuit digital supply.

Table B.5: Test circuit pin table.

Appendix C

Sample Images

Images captured by the DPS array.

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