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Experimental Demonstration of High-Speed Full-Duplex Reconfigurable Free-Space Card-to-Card Optical Interconnects

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Abstract: A high-speed full-duplex free space based card-to-card optical interconnect architecture with flexibility and reconfigurablity is proposed and experimentally demonstrated. 3×3 10Gb/s data transmission for up to 30cm is achieved with receiver sensitivity better than -11.5dBm.
OCIS codes: (060.4510) Optical communications; (200.4650) Optical interconnects.

1. Introduction

The interconnect bandwidth requirement in data-centers and high-performance computing applications has increased considerably over the past decade, mainly due to the continuous miniaturization of transistors and the widely usage of multi-core architecture [1-3]. Conventionally, copper based cables are used for data transmission between cards and racks. However, the electrical technologies are not suitable for future high-speed interconnects due to the fundamental limitations such as power consumption, heat dissipation, and transmission latency [4].

The use of parallel short-range optical links for high-throughput interconnections has been proposed and widely studied [5-7]. Most of the reported optical interconnect architecture is based on polymer waveguides or multi-mode fiber ribbons. However, these point-to-point schemes are inherently non-reconfigurable and their flexibility in dynamically interconnecting electronic cards is highly limited.

In this paper, we propose and demonstrate a novel high-speed full-duplex free space based reconfigurable card-to-card optical interconnect architecture providing flexibility. A 3×3 10 Gb/s small-sized reconfigurable free space optical interconnect demonstrator is developed, demonstrating up to 30 cm full-duplex card-to-card interconnects with a bit-error-rate (BER) < 10^{-6} and a receiver sensitivity better than -11.5 dBm.

2. Architecture of proposed reconfigurable optical interconnect

The proposed full-duplex reconfigurable free space card-to-card optical interconnect architecture is shown in Fig. 1, where a dedicated optical interconnect module is integrated onto each electronic card (typically printed-circuit-board (PCB)). This optical interconnect module mainly consists of a VCSEL array, a photodiode (PD) array, two micro-lens arrays, and two MEMS-based steering mirror arrays.

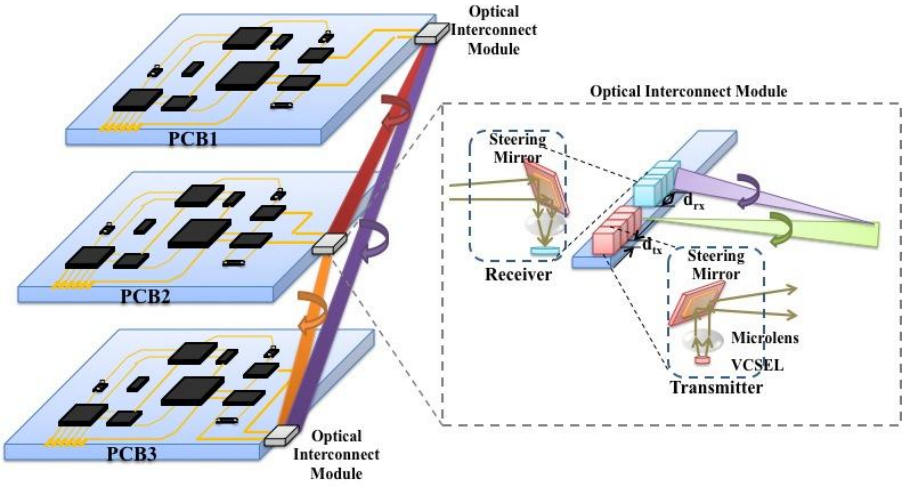

Fig. 1 Architecture of proposed reconfigurable card-to-card optical interconnects.

At the transmitter side, the electrical data from the attached card first modulates the VCSEL, and the modulated optical beam is then collimated by the associated micro-lens to minimize the VCSEL beam divergence. Subsequently, the optical signal is steered towards the corresponding receiver with a MEMS steering mirror element. At the receiver side, the modulated optical signal is appropriately steered with another MEMS mirror element and focused onto the corresponding PD element. With analog steering mirrors being used, the transmitted optical beam can dynamically be steered along arbitrary directions, realising reconfigurable and flexible optical interconnects.

In the proposed reconfigurable optical interconnect architecture, since the VCSEL beams propagate in free space, their diameter expands as the transmission distance increases. Therefore, severe inter-channel crosstalk is induced, leading to a degraded BER performance. This crosstalk issue can be suppressed by using a receiver MEMS steering mirror array with a large spacing between the elements. This is because (i) the intensity of a Gaussian beam drops rapidly with the radial distance from the centre of the beam and (ii) the crosstalk signal induced by a Gaussian beam illuminating a MEMS element does not strike the other MEMS elements at their optimum incidence angles that maximize the optical coupling efficiency and signal detection by their associated PD elements.

3. Experiments and discussions`

Experiments have been carried out to demonstrate the feasibility of our proposed full-duplex free space reconfigurable card-to-card optical interconnect architecture and the setup is shown in Fig. 2. An optical interconnect module was designed, fabricated and integrated onto a PCB, as displayed in the inset of Fig. 2. Specifically, a 1×4 VCSEL array, the corresponding VCSEL driver circuits (4 packaged IC drivers), a 1×4 PD array, and 4 trans-impedance amplifier (TIA) chips were integrated onto a single small-sized PCB. A micro-lens array was then aligned and mounted on top of the VCSEL array and the PD array to collimate the VCSEL beams and focus received optical beams onto the active windows of the PD elements. In real applications, the micro-lens array can be placed on a spacer with a height equals to the focal length of the micro-lenses. Furthermore, separate MEMS steering mirror chips were used and they were attached to XYZ translational stages and dynamically steered by changing the voltage applied.

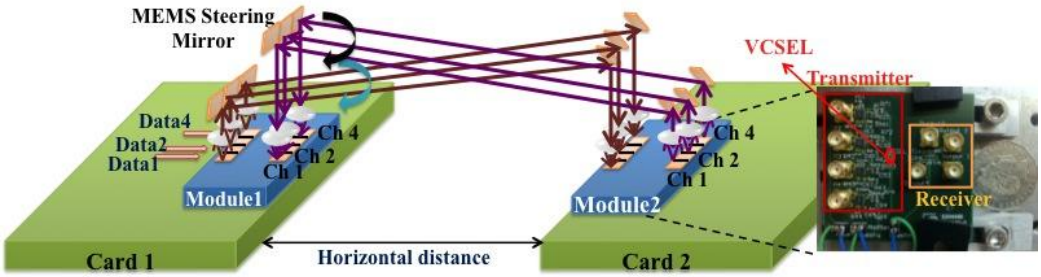

Fig. 2 Experimental setup.

Conventionally, VCSEL and PIN-PD arrays operating at the same wavelength are employed in optical interconnects [5-7]. The same approach was adopted in our experiments because it (i) is cost-effective; (ii) eliminates the need for complex circuitry for the precise control of the wavelength of the VCSEL elements; and (iii) increases the aggregate bit rate.

In the experiment, an 850 nm VCSEL array with a 250 μm pitch was used and wire-bonded to the PCB. The average divergence angle of the VCSEL beams was ~17^{o} and it varied slightly among the 4 elements of the array. The maximum bit rate of VCSEL driver chips was 11.3 Gbps. The VCSEL and PD micro-lens arrays had a pitch of 250 μm, a clear aperture of ~ 236 μm and a focal length of ~ 656.5 μm. The PD array had a pitch of 250 μm. Each PD element had an active aperture diameter of 60 μm and a responsivity of ~0.61 A/W at 850 nm, and was wire bonded to a TIA chip. The 3-dB bandwidth of the TIA was ~12.6 GHz and its differential trans-impedance was ~5 kΩ. In addition, the size of the MEMS mirror was larger than the pitch of VCSEL and PD arrays, so only three out of the four available channels were used (the third VCSEL and PD elements were not used as shown in Fig. 2).

During the measurements, the bit rate of each channel was set to 10 Gbps and on-off-keying (OOK) modulation was used. The output power from each VCSEL was set to 2.5 mW. At the receiver side, to suppress the crosstalk, 2.5 mm spacing between the MEMS steering mirrors was chosen. Furthermore, the vertical distance between the micro-lens array and the MEMS steering mirror array was ~1 cm at the transmitter side and ~ 10 cm at the receiver side. The larger distance used at the receiver side was necessary to increase the spacing of the receiver MEMS

mirrors. While this approach led to reduction in detected signal power due to the longer propagation distance between the interconnected VCSEL and PD elements, it reduced the crosstalk significantly.

In the first measurement, VCSEL element n (n=1, 2, or 4) was interconnected to PD n. The measured BER performance of the three used channels in both directions with respect to the horizontal distance between the transmitter and receiver PCBs is shown in Fig. 3. It is clear that the BER in two directions is similar and by increasing the horizontal distance between the VCSEL and PD PCBs, for all channels the BER also increases. This is because the diameter of the Gaussian beam increases with the propagation distance, resulting in a smaller collected signal power and stronger inter-channel crosstalk power. In addition, it can be seen that the performance of channel 4 is much better than the other two channels. This is because channel 4 is relatively far from other channels and it is less susceptible to crosstalk. Furthermore, for all the three channels, even when the horizontal distance is 30 cm, which is typical for data center card-to-card interconnects, a BER < 10^{-6} can still be achieved.

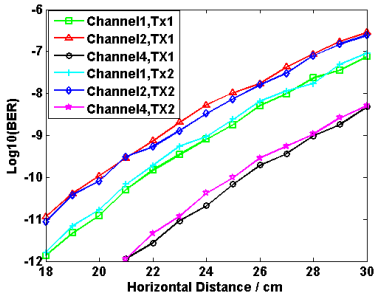

Fig. 3 BER with respect to horizontal distance.

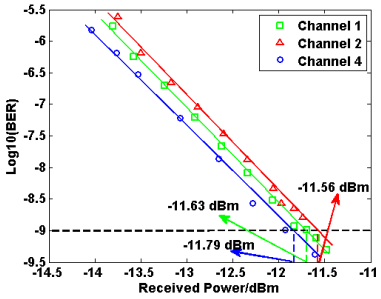

Fig. 4 Receiver sensitivity.

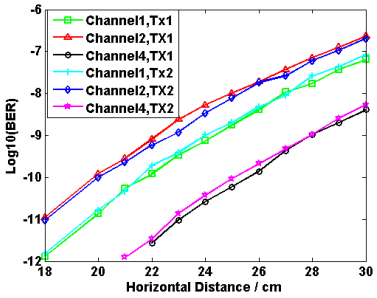

Fig. 5 BER of reconfigured interconnect.

Experiments have also been carried out to measure the receiver sensitivity (at BER<10^{-9}) of the PDs on module 2 when the horizontal distance between the transmitter and receiver PCBs is 30 cm and the results are shown in Fig. 4. It can be seen that receiver sensitivity better than -11.5 dBm is achieved for all channels. Furthermore, channel 4 has the best receiver sensitivity, consistent with the results shown in Fig. 3.

To demonstrate the reconfigurability of proposed card-to-card optical interconnect architecture, another scenario was considered, where VCSEL 1, 2, and 4 were interconnected to PD 2, 4, and 1, respectively. The measured BER in both directions versus the horizontal distance between the transmitter and receiver PCBs is shown in Fig. 5. Comparing the results shown in Fig. 3 and Fig. 5, insignificant difference in the BER performance is displayed, demonstrating that the proposed free space based reconfigurable card-to-card optical interconnect architecture can connect the VCSEL and PD elements arbitrarily to provide flexibility.

4. Conclusions

In this paper, a full-duplex free space based 3×3 10 Gb/s reconfigurable optical interconnect architecture employing VCSEL, PD, micro-lens and MEMS-based steering mirror arrays has been proposed and demonstrated. A small-sized PCB-based integrated optical interconnect demonstrator has been developed and up to 30 cm full-duplex interconnects have been experimentally achieved with a receiver sensitivity better than -11.5 dBm. The reconfigurability and flexibility of the proposed architecture has been verified as well.

5. References

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