Annealing Studies and Electrical Properties of SnS-based Solar Cells

Ogah E. Ogah[a], Kotte Ramakrishna Reddy[b], Guillaume Zoppi[a], Ian Forbes[a], Robert W. Miles[a,*]

[a] *Northumbria Photovoltaics Applications Centre, Northumbria University, Ellison Building, Newcastle-upon-Tyne, NE1 8ST, UK*
[b] *Department of Physics, Sri Venkateswara University, Tirupati-517502, India*

Abstract

Thin films of SnS (tin sulphide) were thermally evaporated onto glass and CdS/ITO (cadmium sulphide/indium tin oxide) coated glass substrates and then annealed in vacuum with the aim of optimising them for use in photovoltaic solar cell device structures. The chemical and physical properties of the layers were determined using scanning electron microscopy, energy dispersive x-ray analysis, x-ray diffraction, and transmittance versus wavelength measurements. "Superstrate configuration" devices were also made using indium tin oxide as the transparent conductive oxide, thermally evaporated cadmium sulphide as the buffer layer and evaporated copper/indium as the back contact material. Capacitance-voltage data are given for the fabricated devices. Capacitance-voltage, spectral response and I-V data are given for the fabricated devices.

Keywords: thermal evaporation, tin sulphide, SnS, solar cells, absorber layers

1. Introduction

Tin sulphide (SnS) is a promising new material for photovoltaic applications. With a direct energy bandgap, near to 1.3 eV, it has a high optical absorption coefficient for photons with energies greater than the energy band-gap. It is also amphoteric giving flexibility to device design such that a range of device structures can be envisioned[1]. These include p-type SnS/n-type window layer hetero-junction devices, buried SnS homo-junction devices and p-i-n structure devices where the i-layer is SnS. It is also possible that grain boundary passivation is feasible by counter-doping or oxidising the grain boundaries in this material[2]. SnS also consists of abundant elements[3]. Large scale production processes already exist for producing thin films of tin and for converting metals into the corresponding sulphide using a range of sulphidisation processes.

*Corresponding author. telephone: +44 191 243 4594; fax: +44 191 227 3650
Email address: robert.miles@northumbria.ac.uk (Robert W. Miles)

In the literature thin films of SnS have been deposited using a variety of techniques including spray pyrolysis [4], electrodeposition [5], chemical bath deposition [6, 7] and vacuum evaporation [8]. The attempts to use the SnS in device structures are limited but previous studies have shown that cells with efficiencies $> 1.3\%$ can be produced [4, 9]. In previous work we have investigated how the chemical and physical properties of the layers deposited using thermal evaporation varied with the deposition conditions, including substrate and source temperatures and film thickness [10]. In this work the effects of post-deposition annealing on the properties of the layers were investigated. Superstrate configuration devices were also fabricated and investigated.

2. Experimental

The evaporations were carried out in an oil pumped vacuum system operated in the 10^{-5} to 10^{-6} torr range of vacuum pressures. Both the substrate and the source material were heated using resistive elements with a shutter incorporated to control the deposition time. The 99.99% purity SnS source material was obtained from Testbourne Ltd. The substrates were either soda-lime glass microscope slides or tin-doped In_2O_3-coated glass slides. Each substrate was cleaned in an ultrasonic bath containing a mixture of Decon 90 and de-ionised water solution for one hour. After a rinse with de-ionised water, the substrate was washed in propan-2-ol (IPA) to remove any remaining contamination. The evaporation source was a quartz, bottle-shaped crucible that was heated by a cylindrical tantalum heating element supplied by the R.D. Mathis Company.

The SnS evaporant was placed in the crucible and quartz wool placed above it to minimise the affects of "spattering", *i.e.* the ejection of molten lumps of material from the source that can damage the growing film. Films were then deposited using source temperatures in the range 250°C to 600°C and for substrate temperatures in the range 100°C to 400°C. These temperatures were measured by thermocouples in direct contact with the crucible and substrate respectively. The deposition time was typically less than 5 minutes.

The post-deposition annealing was carried out in vacuum using temperatures in the range 300°C to 500°C and for times in the range 15 minutes to 3 hours. The ramp time used was 15°C/min and the samples were taken out 5 minutes after anneal time to cool down in ambient air. The solar cell structures were made using 300 nm of indium tin oxide deposited onto glass using RF magnetron sputtering, followed by the thermal evaporation of CdS onto the ITO using a substrate temperature of 200°C and deposition time of 5 minutes. Prior to the deposition of the SnS, the substrates were annealed in forming gas (5% of H_2 in N_2) at 400°C for 10 minutes.

A Siemens D5000 X-Ray diffractometer (XRD), with a CuKα radiation source ($\lambda = 1.5406\,\mathring{A}$), was used to identify the phases present and structure of each phase. The optical transmittance and reflectance versus wavelength measurements were made using a Shimadzu SolidSpec 3700 UV-VIS-NIR spectrophotometer. Observations of the surface topology and topography were carried out using an FEI Quanta 200 ESEM, while energy dispersive x-ray analysis

(EDS) analysis was done using an Oxford Instruments energy dispersive x-ray analysis EDS system. The solar cell measurements were made using a simulated AM1.5 spectrum set to $1000\,\mathrm{Wm}^{-2}$ and the C-V measurements using a Hewlett-Packard LCR measurement unit.

3. Results and discussion

A detailed investigation of how the chemical and physical properties of the tin sulphide layers deposited vary with substrate temperature, source temperature and with thickness have been reported previously [10]. These results showed that for a wide range of conditions it was possible to deposit thin films that were conformal to the substrate, free from pinholes and that consisted of densely packed columnar grains. The ratio of Sn:S in the layers decreased with an increase in substrate temperature and increased with an increase in source temperature. Although the layers were predominantly SnS, other phases were detected in the layers including SnS_2 and Sn_2S_3.

Fig. 1(a) shows an SEM micrograph of an as-deposited layer and fig. 1(b) the same layer annealed in vacuum at 400°C for 3 hrs. It can be observed that annealing at a sufficiently high temperature for a sufficiently long period of time resulted in densification of the material and a significant increase in grain size.

Fig. 2(a) shows an x-ray diffractogram of an as-deposited layer and fig. 2(b) an x-ray diffractogram of the layer annealed in vacuum at 400°C for 30 mins. Table 1 gives a list of the reflections observed and possible interpretations as to their origin. Both the as-deposited layers and annealed layers were predominantly SnS, with SnS_2 and Sn_2S_3 phases present to some extent. The annealing caused an increase in the intensity of the main reflections corresponding to the layers becoming more orientated and possibly more crystalline. The EDS data for the annealed samples indicated that the ratio of Sn:S had decreased compared to the as-grown sample and that for substantial annealing the layers tended toward a stoichiometric ratio of 1:1.

Transmittance versus wavelength measurements for the as-grown sample before and after annealing in vacuum at 400°C for 30 mins are shown in fig. 3. It is evident from the figure that the main effect of the annealing is to narrow the optical absorption edge toward that which corresponded to the energy bandgap of SnS (1.35 eV). This is associated with an increase in grain size, densification of the layers, and a reduction in the presence of minority phases. The reduction in transmittance after annealing is due to the corresponding increase in optical absorption of the annealed layers.

Resistivity measurements were also made for the as-deposited layers (i.e. SnS on glass) using different values of substrate temperature. As shown in Fig. 4, the resistivity increased with an increase in substrate temperature following the way the Sn:S ratio varied with the deposition conditions [10] the resistivity was also found to decrease with an increase in annealing temperature and time.

Superstrate configuration solar cell devices were produced by thermally evaporating either CdS or ZnSe onto indium tin oxide coated glass substrates using

a substrate temperature of 200°C and a deposition time of 5 minutes and then thermally evaporating SnS onto the CdS/ITO substrates using a substrate temperature of 350°C, a source temperature of 300°C and a deposition time of 2 minutes. Prior to the SnS deposition, the CdS/ITO/Glass layers were annealed in forming gas (H_2/N_2) at a temperature of 400°C for 5 minutes to produce a Cd-rich surface, remove oxygen from the grain boundaries in the CdS and to lower the CdS resistivity. The back contact was made by thermally evaporating copper or indium onto the SnS surface.

The spectral response of a CdS/SnS device is given in fig. 5. As expected most of the spectral response occurs between the wavelengths that correspond to the energy bandgaps of the materials used (2.42 eV to 1.3 eV). An interesting feature of the long wavelength response is that there is a small response for photons with wavelengths > 954 nm (1.3 eV) and which extends to approximately 1100 nm (*i.e.* 1.1 eV) in all the devices studied. Such a feature could be due to the SnS and CdS interacting at the interface to form an alloy or compound with a 1.1 eV energy bandgap or due to the back contact material interacting with the SnS to form a 1.1 eV energy bandgap compound or alloy at the back interface. However the extended response is still observed when the CdS is replaced by ZnSe and for a range of different back contact materials. There are some reports in the literature that SnS has an indirect energy bandgap of 1.1 eV in addition to the direct energy bandgap of 1.3 eV [11]. It is hence possible that the long wavelength absorption is due to transitions across the 1.1 eV indirect energy bandgap.

Fig. 6(a) gives the variation of capacitance (±5% measurement error) with reverse bias voltage using different frequencies and fig.6 (b) a plot of $\frac{1}{C^2}$ versus reverse bias voltage (for 100 kHz) for a SnS/CdS solar cell in the dark. The former plot shows that there is some effect of measurement frequency on the capacitance measured. This data can be used to estimate the density of interface states present in the junction region using:

$$N_{IS} = \frac{C_{LF} - C_{HF}}{Ae} = 4.1 \times 10^{11}\, FC^{-1} cm^{-2} \qquad (1)$$

where N_{IS} is the density of interface states, C_{LF} is the low frequency capacitance, C_{HF} is the high frequency capacitance, A is the cross-sectional cell area, and e is the electronic charge.

Fig. 6(b) shows that the doping in the tin sulphide layer is non-uniform, it being resistive at the CdS/SnS interface and less so further from the interface. Assuming a n^+p device the slope of the graph of $\frac{1}{C^2}$ versus V corresponds to a doping concentration of $10^{15} - 10^{16}\, cm^{-3}$ near to the interface with a doping concentration up to $10^{17} - 10^{18}\, cm^{-3}$ for V > 0.9 Volts. If the doping is assumed to be uniform between 0 and 0.1 volts then extrapolating onto the voltage axis gives a built-in voltage of 1.6 volts for the SnS/CdS junction. The depletion region width is typically approximately $0.4\,\mu m$ for zero bias.

When illuminated in the AM1.5 simulator the photovoltaic effect was observed in most of the devices fabricated. The best open circuit voltage of the

SnS/CdS cells was found to be 200 mV, the best short circuit $J_{sc} = 16\, mA/cm^2$ and the best fill-factor $FF = 0.3$ (in separate devices). The most significant problem is that the shunt resistance is too low in the devices fabricated. The values reported are comparable to the best values previously reported in the literature, given in Table 2.

4. Conclusions

The resistivity of the layers annealed increased with an increase in substrate temperature and it decreased with an increase in source temperature. The post-deposition annealing also increased the grain size, improved the crystallinity of the layers and it also caused a shift in the optical absorbtion edge toward that expected for SnS. Superstrate configuration devices were successfully fabricated using the thermally evaporated SnS layers confirming yet again that the photo-voltaic effect can be observed in devices made with SnS. The short circuit current observed suggests that the crystalline quality of the SnS produced is promising for making good devices if the high degree of shunting that is reducing V_{OC} and FF can be eliminated.

[1] K. T. R. Reddy, P. Pratap, R. W. Miles, *In: H. Tanaka, K. Yamashita (eds.), Photovoltaics: Development, Applications and Impact, Nova Science Publishers Inc.,* (2010) 1 – 27.

[2] R. W. Miles, G. Zoppi, K. T. R. Reddy, I. Forbes, *In: S. Zhang (ed.), Organic Nanostructured Thin Film Devices and Coatings for Clean Energy, CRC Press,* (2010), 1 – 56.

[3] J. J. Scragg, P. J. Dale, L. M. Peter, G. Zoppi, I. Forbes, *Phys. Status Solidi* 245 (9) (2008) 1772 – 1778.

[4] K. T. R. Reddy, N. K. Reddy, R. W. Miles, *Sol. Energy Mater. Sol. Cells* 90 (18-19) (2006) 3041–3046.

[5] M. Gunasekaran, M. Ichimura, *Sol. Energy Mater. Sol. Cells* 91 (2007) 774–778.

[6] D. Avellanneda, G. Delgado, M. T. S. Nair, P . K. Nair, *Thin Solid Films* 515 (2007) 5771–5776.

[7] W. Li, S. Wei-Ming, Q. Juan, Q. Yong-Hua, W. Lin-Jun, W. Guang-Pu, *Technical Digest of the 18th International Photovoltaic Science and Engineering Conference,* Kolkata, India (2009).

[8] H. Noguchi, A. Setiyadi, T. Nagamoto, O. Omoto, *Sol. Energy Mater. Sol. Cells* 35 (1994) 325–331.

[9] B. Ghosh, J. Pal, P. Banerjee, S. Day, S. Das, *Proc. of the 19th European Photovoltaic Solar Energy Conference,* Paris, France (2004) 1757 –1759.

[10] R. W. Miles, Ogah E. Ogah, G. Zoppi, I. Forbes, *Thin Solid Films* 517 (2009) 4702–4710.

[11] B. Thangaraju, P.J. Kaliannan, *Phys D: Appl. Phys.,* 33 (2000) 1054.

5. List of Figures

Figure 1: Scanning electron micrograph of (a) an as-deposited layer and (b) a layer that had been annealed in vacuum at 400°C for 3h.

Figure 2: X-ray diffractograms of (a) an as-deposited layer (b) the layer after it had been annealed at 400°C for 30 min.

Figure 3: Transmittance versus wavelength data for (a) an as-grown sample and (b) the sample annealed in vacuum at 400°C for 30 min.

Figure 4: Variation of resistivity with substrate temperature for an as-deposited layer.

Figure 5: Spectral response of a SnS/CdS device

Figure 6: (a)The variation of capacitance C with reverse bias voltage V measured using different frequencies, (b) a plot of how $\frac{1}{C^2}$ varies with reverse bias voltage for a CdS/SnS solar cell.

6. List of Tables

$2\theta\,(degrees)$	d	$\frac{I}{I_0}$	$Reflections$
26.49	3.36	0.13	$Sn_2S_3(111)$
30.95	2.89	0.33	$Sn_2S_3(310)$
31.89	2.80	1.00	SnS(111), SnS(040), $Sn_2S_3(211)$
39.19	2.30	0.19	SnS(131)
45.14	2.01	0.09	$Sn_2S_3(430)$
49.19	1.85	0.13	$Sn_2S_3(421)$
51.28	1.78	0.08	SnS(112), SnS(151), SnS(122)
53.21	1.72	0.1	SnS(122)
64.17	1.45	0.07	SnS(212), SnS(251)

Table 1:

SnS growth technique	CdS growth technique	$V_{oc}(mV)$	$J_{sc}(mA/cm^2)$	Fill Factor	Efficiency $\eta(\%)$	Ref.
Spray Pyrolysis	Vacuum evaporation	260	9.6	0.53	1.3	[4]
Electrochemical deposition	Photochemical deposition	170	3.3	0.37	0.20	[5]
Chemical bath deposition	Chemical bath deposition	340	6.0	–	–	[6]
Chemical bath deposition	Vacuum evaporation	200	13.2	0.31	0.81	[7]
Vacuum evaporation	Vacuum evaporation	120	7.0	0.35	0.3	[8]
Chemical Plating	Vacuum evaporation	500	10	0.5	2.5	[9]

Table 2:

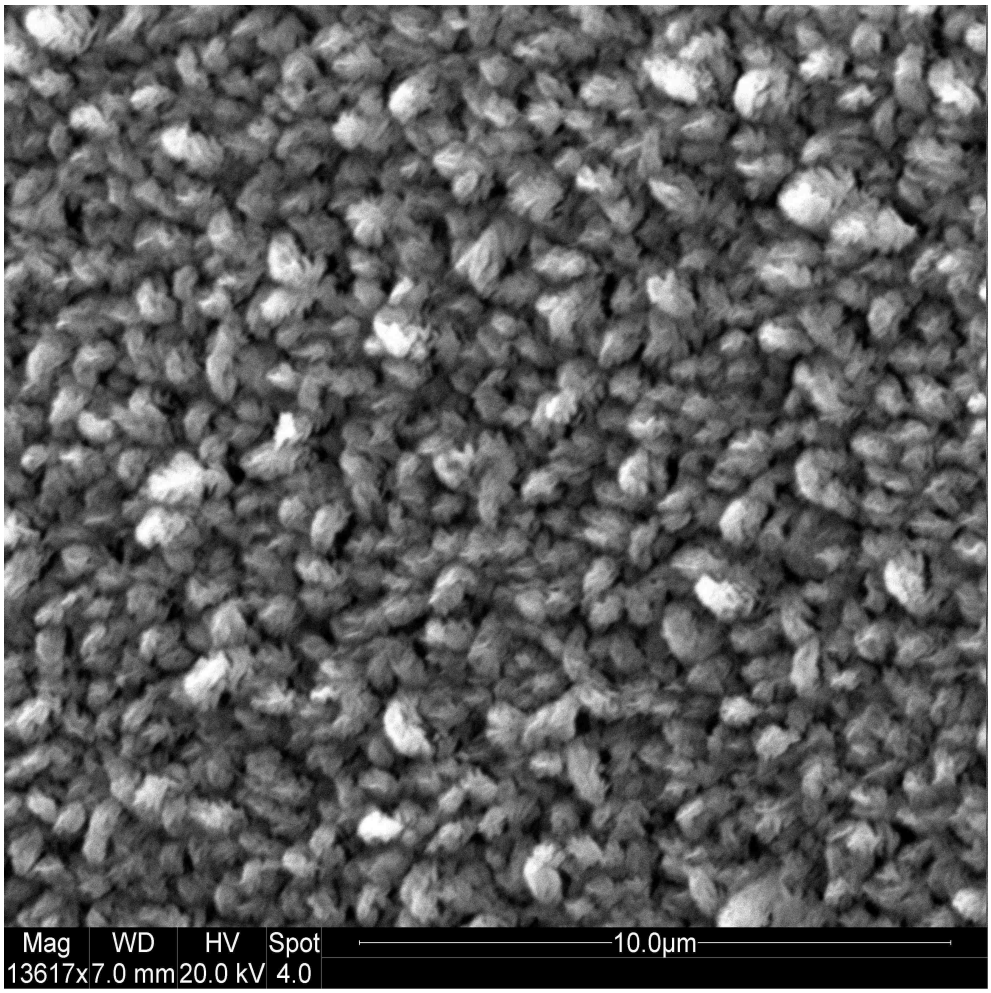

Figure 1(a)

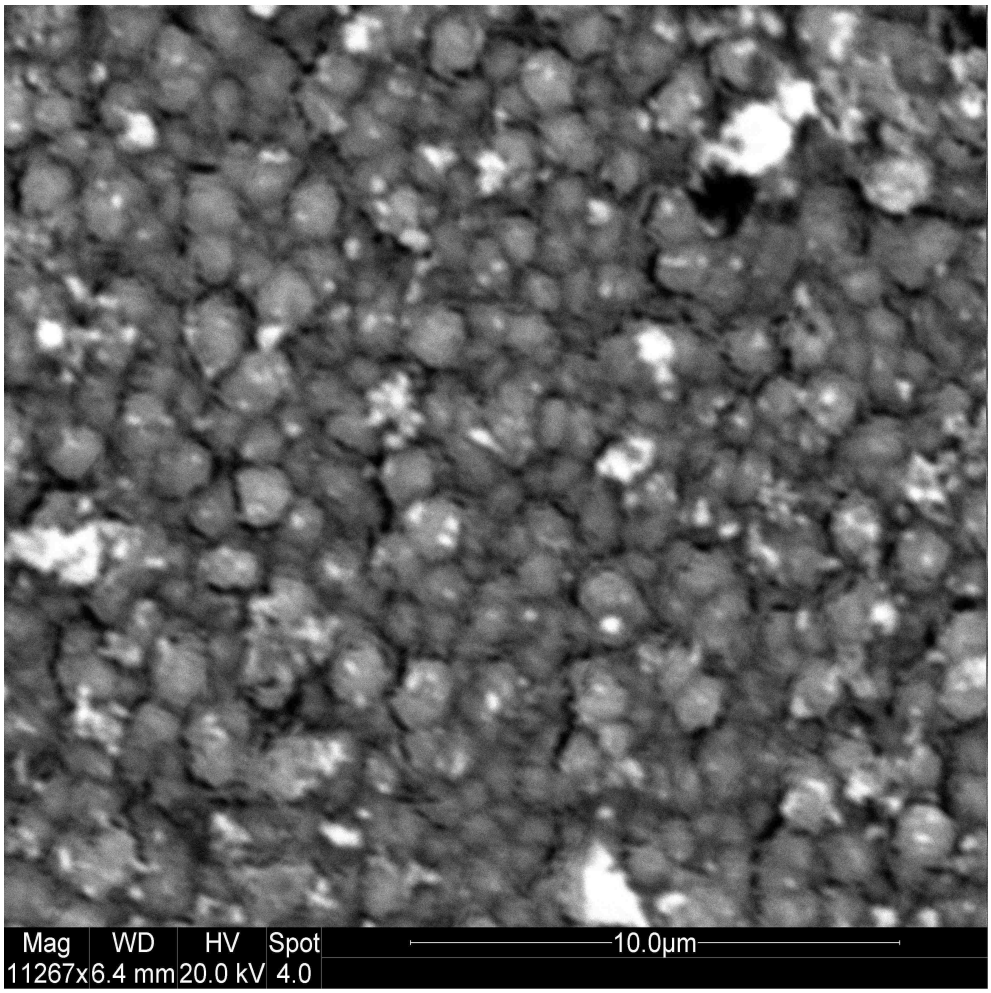

Figure 1(b)

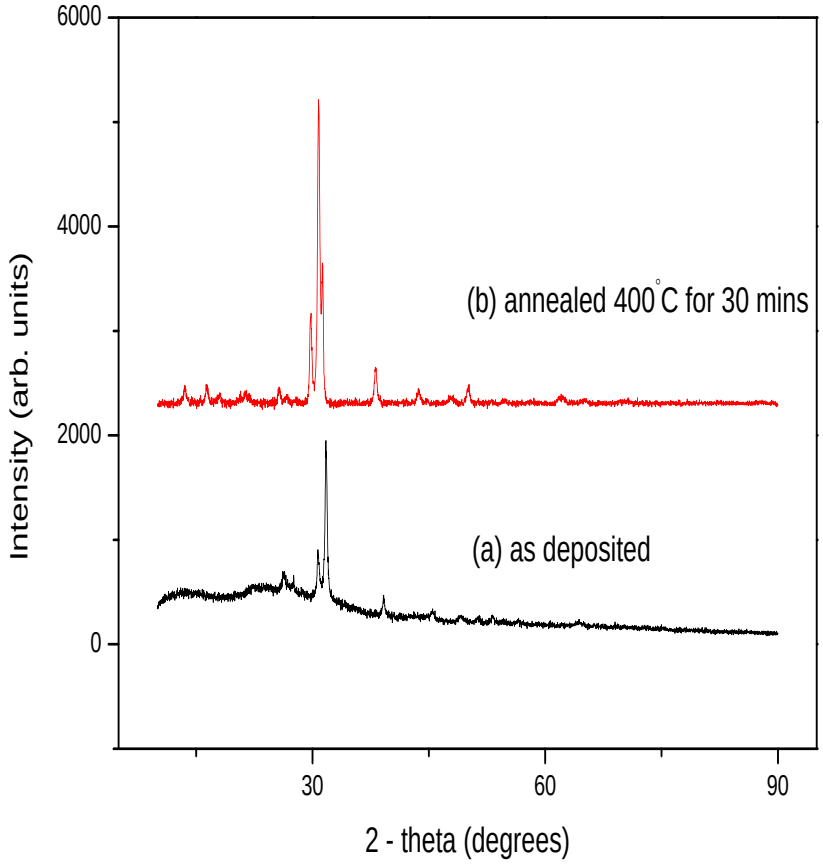

Figure 2(a) and (b)

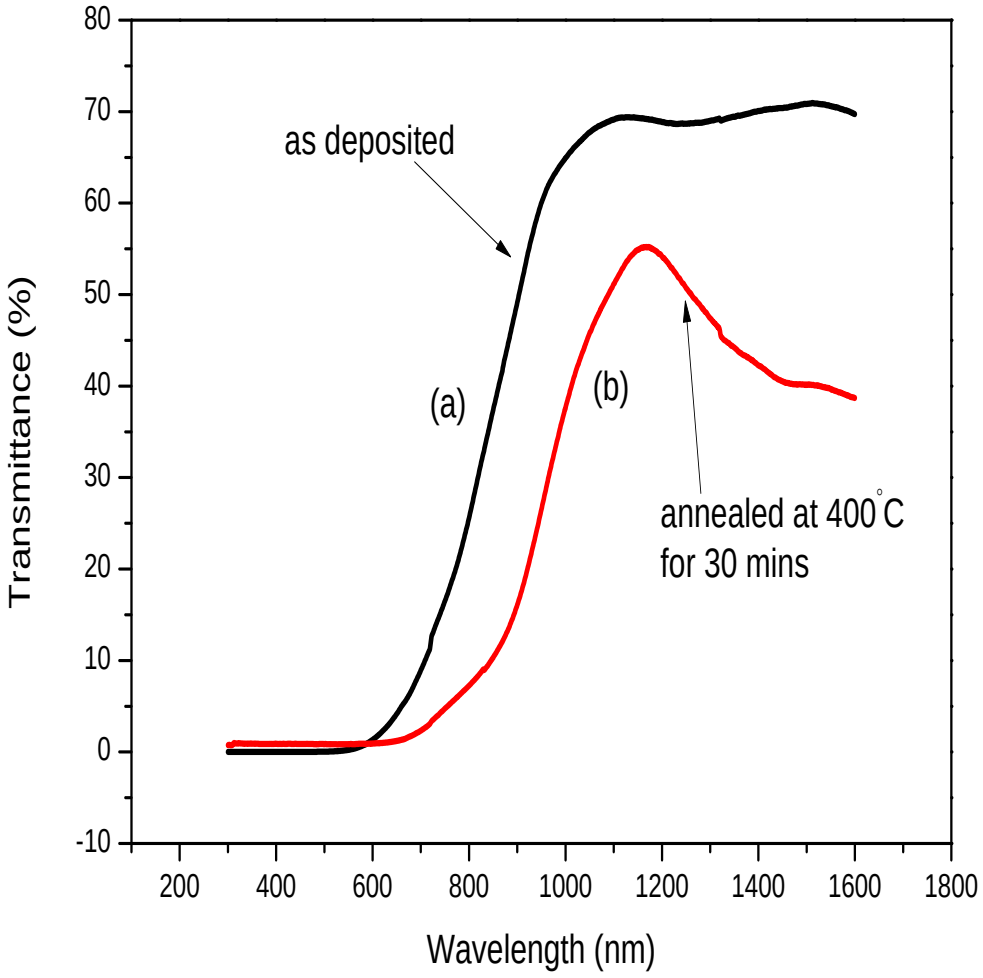

Figure 3(a) and (b)

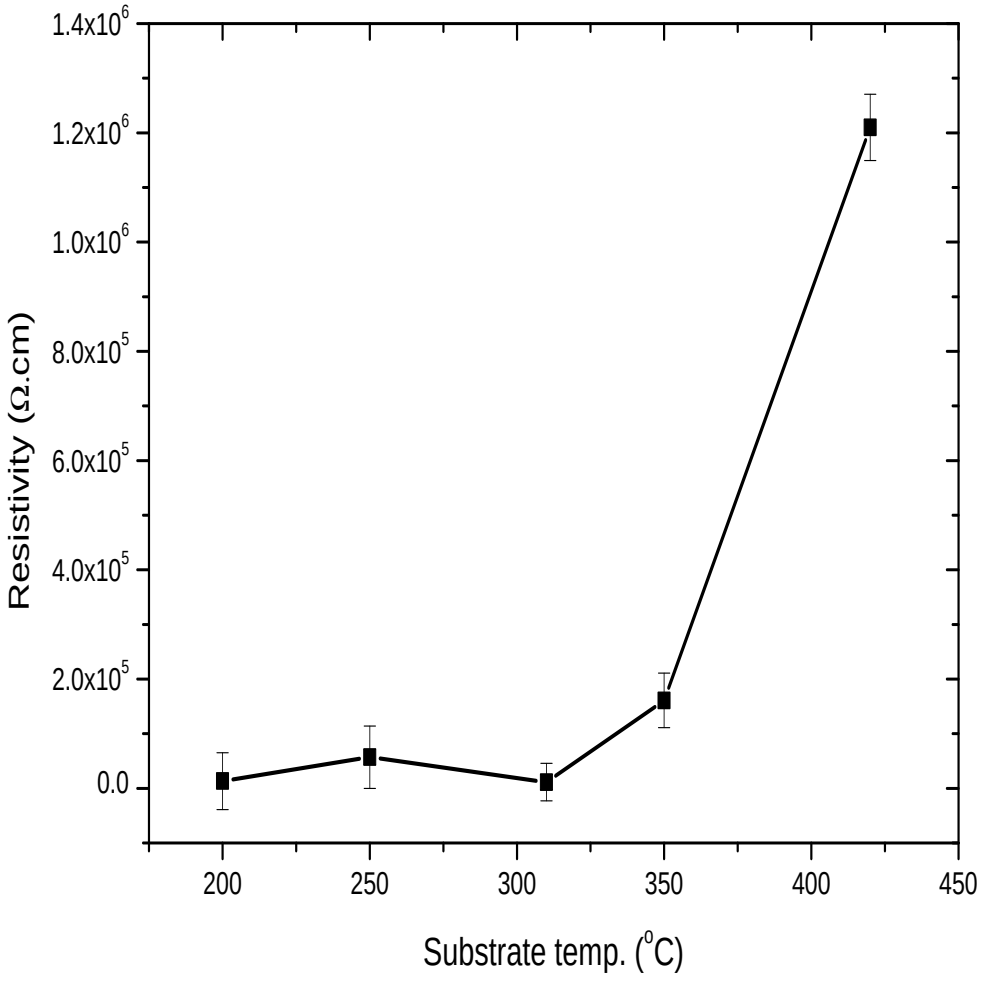
1.4x10^6
1.2x10^6
1.0x10^6
8.0x10^5
6.0x10^5
4.0x10^5
2.0x10^5
0.0
Resistivity (Ω.cm)
200
250
300
350
400
450
Substrate temp. (^0C)

Figure 4

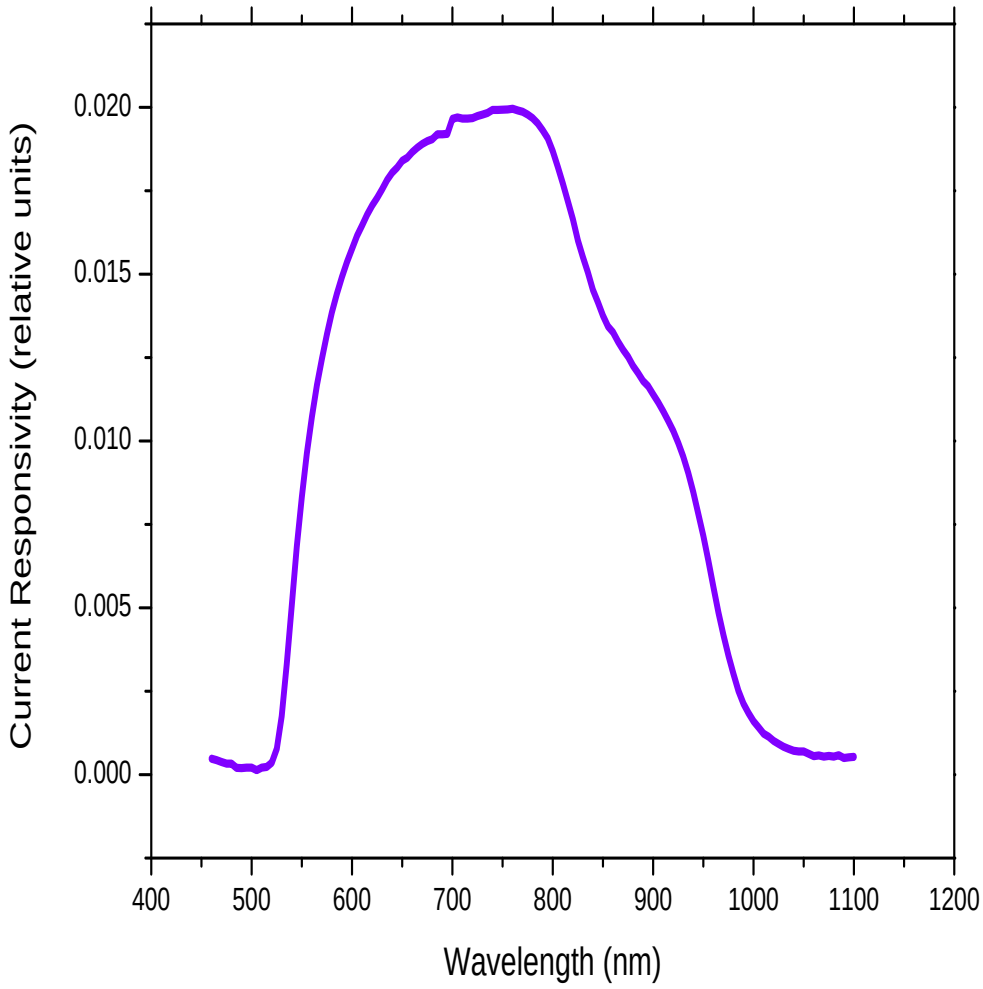
Current Responsivity (relative units)
0.020
0.015
0.010
0.005
0.000
400
500
600
700
800
900
1000
1100
1200
Wavelength (nm)

Figure 5

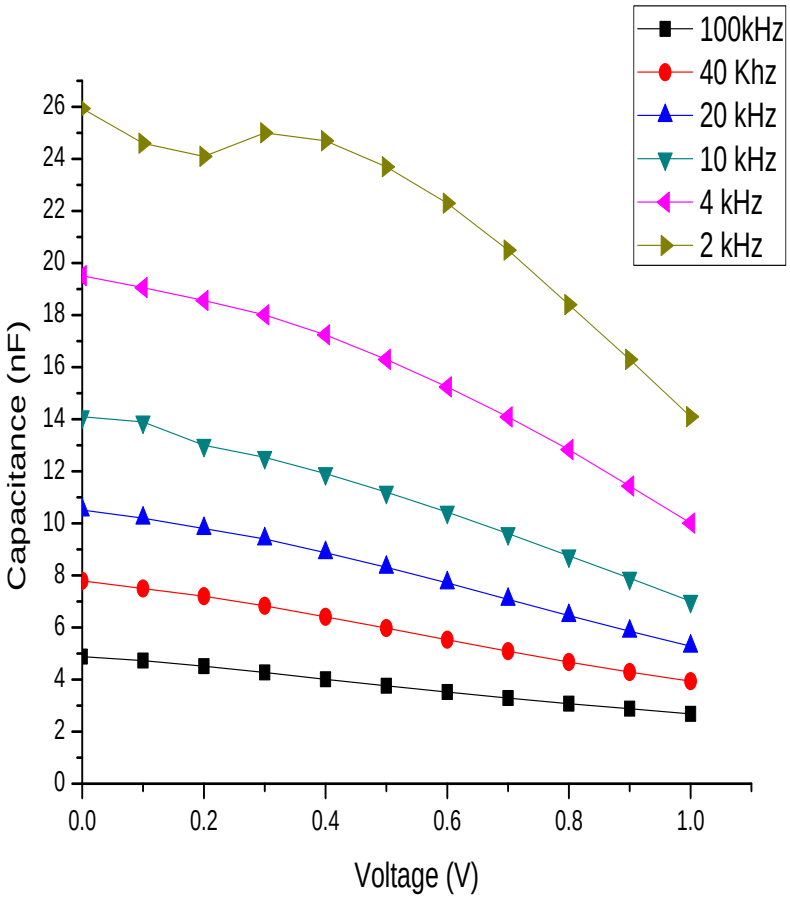
100kHz
40 Khz
20 kHz
10 kHz
4 kHz
2 kHz
Capacitance (nF)
Voltage (V)
0
2
4
6
8
10
12
14
16
18
20
22
24
26
0.0
0.2
0.4
0.6
0.8
1.0

Figure 6(a)

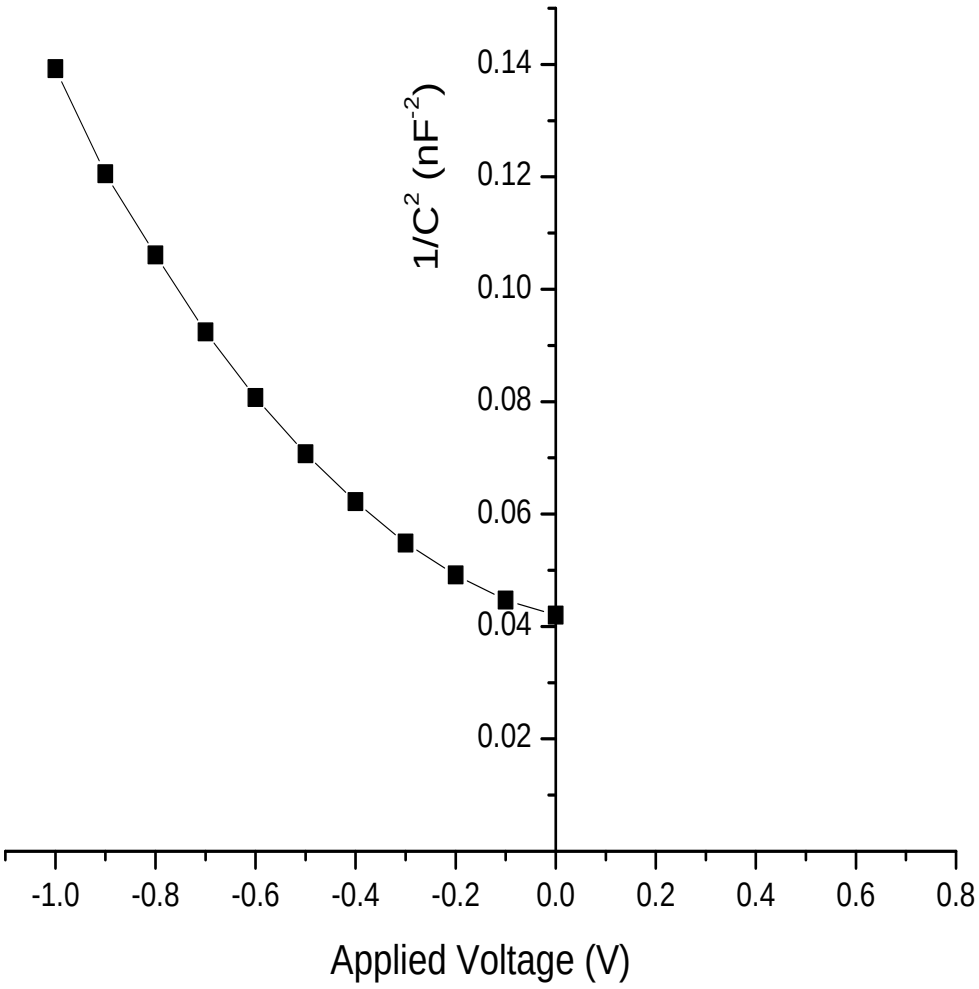
0.14
0.12
0.10
0.08
0.06
0.04
0.02
1/C^2 (nF^-2)
-1.0
-0.8
-0.6
-0.4
-0.2
0.0
0.2
0.4
0.6
0.8
Applied Voltage (V)

Figure 6(b)