Simulation of an All-Optical 1 × 2 SMZ Switch with a High Contrast Ratio

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***Abstract*— An all-optical 1×2 high contrast ratio (*CR*) switch based on the symmetric Mach-Zehnder (SMZ) interferometers is presented. Simulation results show a remarkable improvement of the inter-output *CR* (~25 dB) between the two outputs compared with an existing SMZ switch. It is shown that the proposed switch offers high values of inter-output *CR* (> 32dB) over a wide range of input powers using appropriate power of the control pulses.**

I. INTRODUCTION

Optical fibre communication system has become the backbone behind the Internet due to the huge capacity it offers. However, the switching process in conventional optical networks is still performed in the electrical domain requiring optical/electrical/optical (O/E/O) conversion [1]. O/E/O conversion not only requires extra power, but also induces speed bottleneck due to the data processing speed of the conventional electronic components currently limited to 40 Gbit/s [2]. The next generation optical networks are expected to carry out all processing functions in the optical domain [3, 4]. In such networks all-optical switches such as the terahertz optical asymmetric demultiplexer (TOAD) [5] and the symmetric Mach-Zehnder (SMZ) [6] are the key components adopted for switching and routing due to their ultrafast switching time (pico- to sub-picoseconds) [3, 7]. Among the all-optical switches, the SMZ based switches grant the most flexibility, a narrow and square switching window, a compact size, thermal stability and low power operation [8]. SMZ function is based on the cross-phase modulation of semiconductor optical amplifiers (SOAs) [9], where switching is performed by introducing a phase difference between signals propagating in two arms of interferometer [6] by injecting a high power optical control pulse to SOAs. However, in practice, it is not simple to maintain an exact phase shift of 180^{o} in SOAs. Therefore, in most cases, only the output port 1 of SMZs are used (i.e. op1 in Fig. 1) for switching purpose due to its low inter-output *CR* [10]. A practical all-optical 1×2 router employing SMZs, should have a high inter-output *CR* for lower values of output crosstalk (*CXT*).

In this paper, we propose a novel all-optical 1×2 switch with a high inter-output *CR* (> 32 dB) based on three SMZs. The paper is organized as follows: after introduction, the operation principles of the SMZ, an all-optical inverter, and the proposed 1×2 switch are shown in Section 2. Section 3 presents the simulation results and discussions. Finally, Section 4 will conclude the paper.

II. OPERATION PRINCIPLE

A. *Symmetric Mach-Zehnder (SMZ)*

Fig. 1 shows the structure of SMZ switch comprises of SOAs and a number of 3-dB couplers. Injecting two high-power control pulses (CP_1 and CP_2) with a delay T_{SW} to the SOA_1 and SOA_2, respectively, induces the required phase difference between the two arms. Thus creating a switching window (SW), and enabling the SMZ either to be switched ON or OFF. With no CPs, the upper and lower arms are in the balance state and the input signal emerges from the op2. Applying CP_1 changes the gain characteristics of SOA_1, and as a result the SMZ becomes un-balanced and the input signal emerges from the op1. With the arrival of delayed CP_2 to the SOA_2, the SMZ once again becomes balanced (OFF) and the input signal emerges from the op2. In order to distinguish the data pulses from the control signal at the output ports, orthogonal polarisation is introduced between them. At the output ports, polarisation beam splitters (PBS) are used to separate CPs from data pulses. The output power at the op1 and op2 of SMZ are given in [11].

The inter-output *CR* of a 1×2 switch is defined as the power ratio between the switched and non-switched signals outputs$_{ij}$ where i, j = 1 or 2. Typically the value of inter-output *CR* observed at the SMZ output 2 (CR_{21}) is less than 10 dB [10]. Here we propose a 1×2 switch utilizing an optical inverter that offers improved CR_{21}.

B. *Optical Inverter Based on SMZ*

Fig. 2 illustrates the diagram of an all-optical inverter

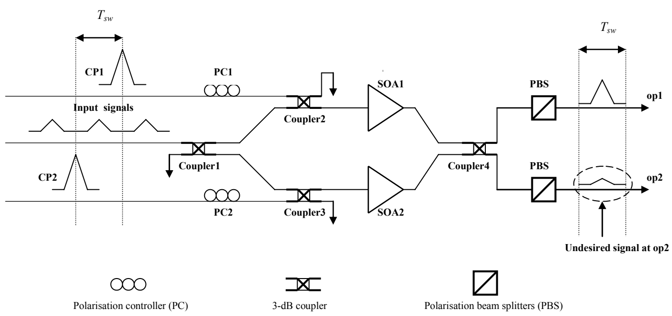

Figure 1. SMZ structure

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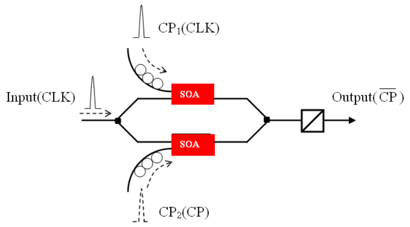


CP	$\overline{CP}$
1	0
0	1

Figure 2. An all-optical inverter based on SMZ

[12] based on the SMZ with only op1 being (see Fig. 1) used. The input clock (CLK) signal is split and applied to both SOAs and is also used as the control pulse CP_1 in the upper SOA. With CP_2 (i.e. CP in Fig. 3) applied to the lower SOA, the SMZ is in a balanced state, thus no signal emerges from the output ($\overline{CP}$). With no CP_2 the SMZ becomes unbalanced, and the input signal emerges from the output port. Note that, there should be no delay between CP_1 (CLK) and CP_2, and both should have the same pulse shape and energy to ensure achieving a balance state.

C. 1 x 2 High Contrast Ratio Switch Based on SMZs

Fig. 3(a) shows a schematic diagram of simulated proposed 1×2 switch. The input packet is applied to the SMZ_1, SMZ_2 and to the clock extraction module (CEM) [13]. The extracted clock signal is used as a CP in the optical inverter. To achieve a high inter-output *CR*, each SMZ only uses its output port 1. In the absence of CP, the input packet is switched to the output 2 since SMZ_1 is in the OFF state. With CP the SMZ_1 is ON and SMZ_2 is OFF, thus the packet is switched to the output 1. Note that the extracted clock and CP should be fully synchronised in time to ensure correct operation of the switch. Fig. 3(b) shows the VPI equivalent of Fig. 3(a).

III. SIMULATION RESULTS AND DISCUSSION

The proposed all-optical 1×2 switch is simulated using the Virtual Photonics™ simulation software and its inter-output *CR* is numerically investigated. All the main simulation parameters used are shown in Tables I and II. The input packet is composed of one clock bit and eight payload bits. Fig. 4(a) illustrates the captured simulated time waveforms at various points. It is clearly shown that with the CP present the input packets are switched to the output 1. Fig. 4(b) shows the output power intensities (in dB) at the outputs 1 and 2, $\overline{CP}$, and SMZ1_op1. It is shown that at the SMZ_op2, CR_{21} of a single SMZ is about 7.5 dB (which is low). This is due to phase shift not being exactly 180° in SOA leading to incomplete destructive signals at the SMZ_op2. By employing an optical inverter and dual SMZs, the CR_{21} has been significantly improved to about 35 dB. Fig. 5(a) and (b) show the inter-output *CR* for $\overline{CP}$, and at the outputs 1 (i.e. CR_{12}) and 2 (i.e. CR_{21}) against the input power and the

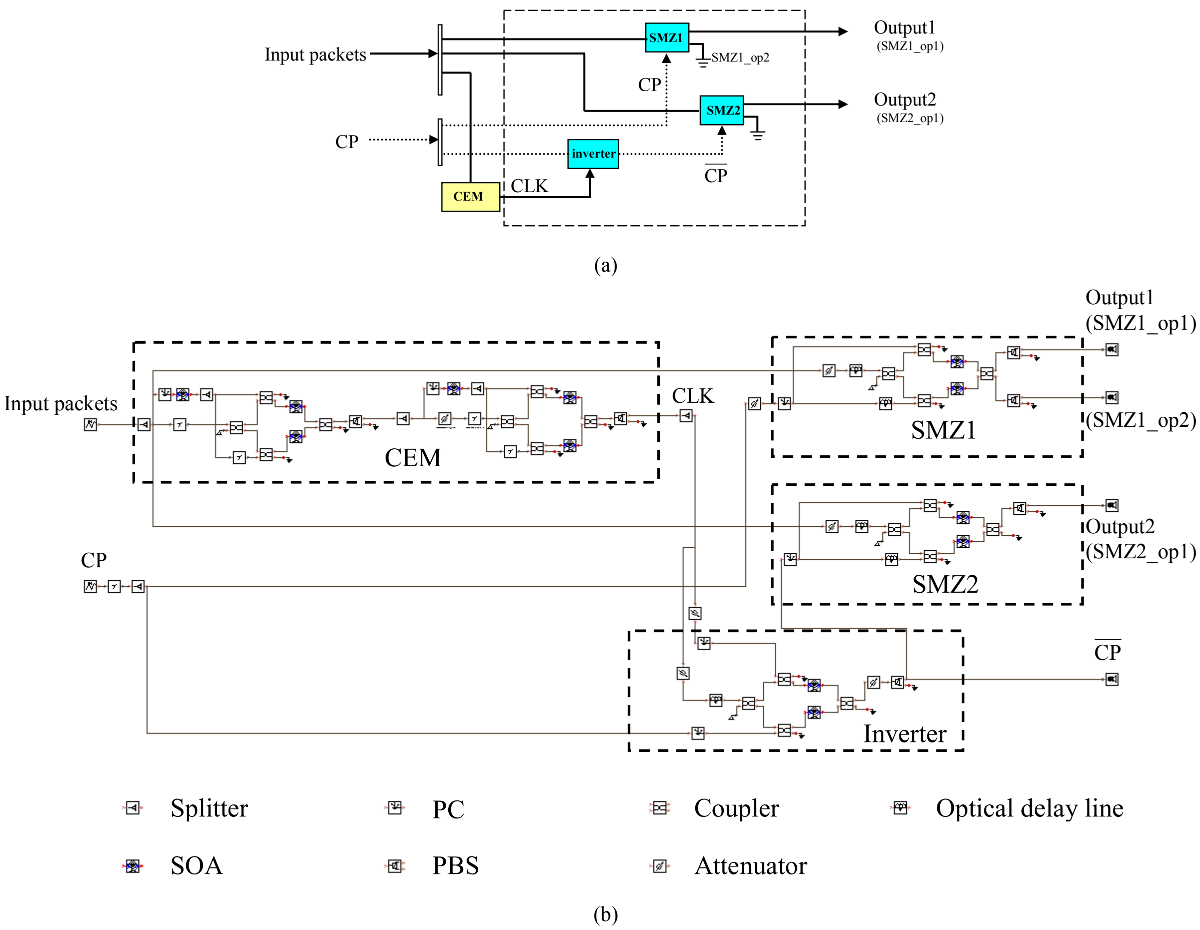
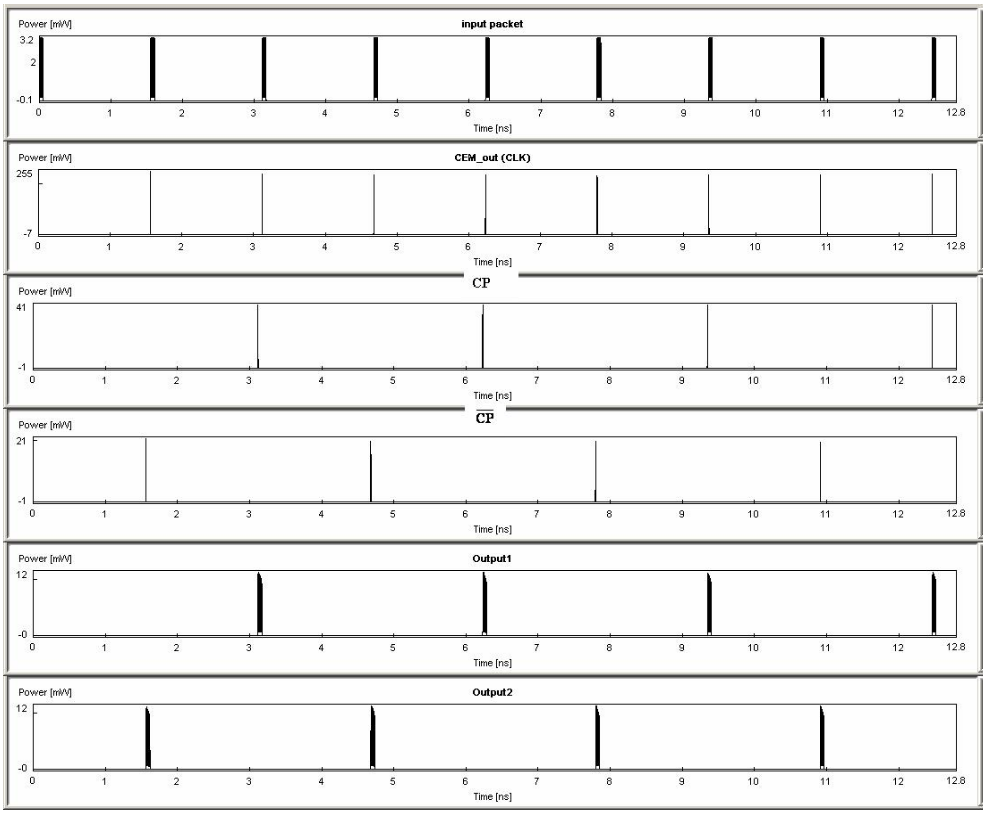
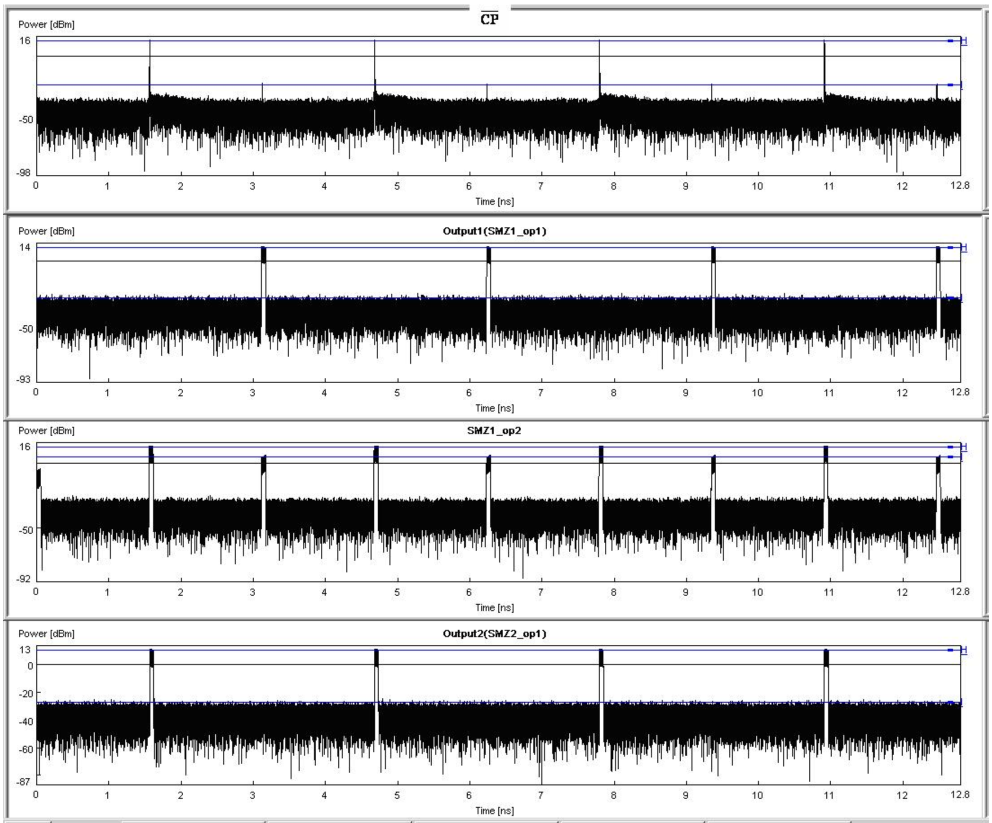


Figure 3. (a) An all-optical 1 x 2 switch, and (b) VPI based model

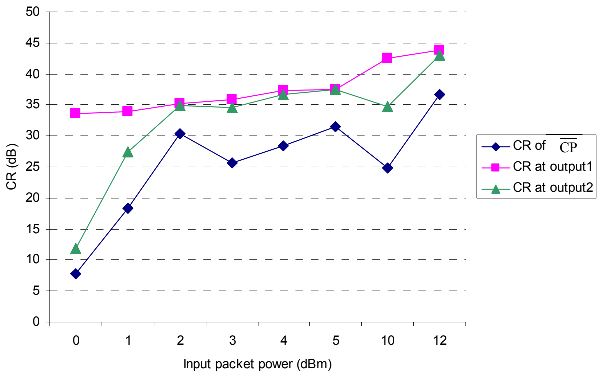


(a)

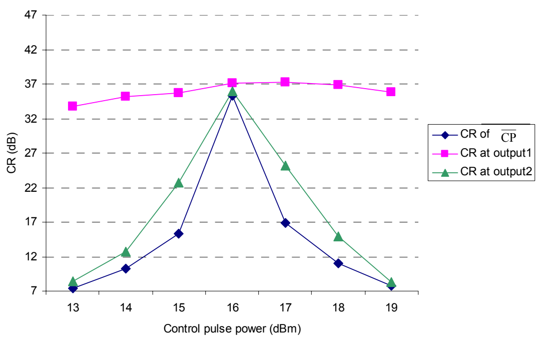


(b)

Figure 4. (a) Output waveforms, and (b) *CR* ratio observed at $\overline{\text{CP}}$, the proposed 1×2 switch output 1, output 2, and SMZ1_op2



(a)



(b)

Figure 5. The observed contrast ratio (*CR*) against (a) the input packet power and (b) the control pulse power

TABLE I.
SOA SIMULATION PARAMETERS

Parameter and description	Value
Inject current	0.15 A
Length	500×10^{-6} m
Width	3×10^{-6} m
Height	80×10^{-9} m
Confinement factor	0.15
Differential gain	2.78×10^{-20} m^2
Carrier density at transparency	1.4×10^{24} m^{-3}
Initial carrier density	3×10^{24} m^{-3}
Linewidth enhancement factor	5
Recombine constant A	1.43×10^{8} s^{-1}
Recombine constant B	1×10^{-16} m^{3}s^{-1}
Recombine constant C	3×10^{-41} m^{6}s^{-1}

TABLE II.
SIGNAL AND CONTROL PULSES DEFAULT PARAMETERS

Parameter and description	Value
Data packet bit rate – $1/T_b$	160 Gb/s
Packet payload length	1 bytes (8 bits)
Packet guard time	1.5 ns
Wavelength of data packet	1554 nm
Data & control pulse widths – FWHM	2 ps
Bit duration T_b	6.25 ps
Control signal (CP) power	40 mW

control pulse power, respectively. The proposed 1×2 switch displays a high inter-output *CR* over a wide range of input powers. However, the *CR* shows high sensitivity to the control power reaching a maximum value of 35 dB at control power of 16 dBm. Note that the *CR* for output 1 is almost flat compared with the others. This is because of a CP with a higher *CR* is applied directly to the SMZ_1. The variation in the *CR* at the output 2 (i.e. CR_{21}) is due to $\overline{CP}$ with different power levels (i.e. varying *CR* values) being applied to the SMZ_2. The result shows that the inter-output *CR* of the 1×2 switch is mainly dependent on the *CR* of optical inverter.

IV. CONCLUSIONS

The paper has proposed and simulated an all-optical 1×2 high contrast ratio switch based on the SMZs. By carefully selecting the power of the control pulses, inter-output *CR* of > 32 dB was achieved over a wide range of input packet power (12 dB). The proposed 1×2 switch offered an improvement in the inter-output *CR* of ~ 25 dB in comparison with a single SMZ switch. The proposed switch could potentially be adopted for high-speed signal processing and packet routing in all-optical networks.

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