

# Simulations and Experiments on the Fabrication of Silicon Tip

Wang Mingliang, Sun Daoheng\*, Wang Yanhua

Dept. of Mechanical & Electrical Engineering, Xiamen Univ. Xiamen, 361005, P.R. China

## Abstract

Simulations and experiments on three kinds of Si tip fabrication techniques had been done, which are Anisotropic Dry Etching (ADE), Anisotropic Wet Etching (AWE) and AWE combining with bonding. The simulation results showed that the parameters applied in the ADE and AWE should be controlled much more precisely than AWE combining with bonding to get expected tips. The experiments prove that the parameters of fabricating silicon tip by ADE and AWE have little tolerance. The conclusions on AWE combining with bonding drew from simulations are verified in the detail experiments. From the simulations and experiments, excellent reliability and controllability are witnessed in AWE combining with bonding and a tip with top diameter within 23.44nm had been achieved.

**Key words:** silicon tip, anisotropic dry etching, anisotropic wet etching, bonding

## 1. Introduction

Micro tip is the most important component in the field of micro/nano. It has been widely used in the STM and AFM since 1980s<sup>1</sup> and has been used successfully in micro tunneling sensors to achieve a very high resolution, such as micromachined electron tunneling infrared sensor<sup>2</sup>, micromachined electron tunneling magnetometer<sup>3</sup>, pressure sensor based on an array of wedge emitters<sup>4</sup> and tunneling-based microaccelerometer<sup>5,6</sup>. It also has been used in vacuum microelectronic devices<sup>7</sup>. In the fabrication of these sensors and devices, the tip is the critical component which affects the performance directly. Micro tip can be made by diamond, metal and semiconductor. Silicon tip has become more and more popular because that it's easily integrated with other components and that it's compatible with IC technology. Many kinds of techniques to fabricating silicon tip had been reported<sup>10,11</sup>. In this paper, simulations and experiments on three kinds of techniques are presented.

## 2. Simulations

Anisotropic Crystalline Etch Simulation (ACES) is designed to provide a convenient way for user to estimate etch results with their mask design. ACES provides the simulations of anisotropic wet etching, RIE, diffusing and passivation on silicon and wet etching on GaAs. Before simulation, a mask file, orientation, process, etchant and etching time should be given in detail.

In our simulations, anisotropic etching is described by different etching rates at different directions which are assumed to be  $1\mu\text{m}/\text{min}$  at  $\{100\}$ ,  $1.414\mu\text{m}/\text{min}$  at  $\{110\}$  and  $0\mu\text{m}/\text{min}$  at  $\{111\}$  respectively. Three masks are designed as Fig.1 shown. In mask1 and mask2, there are two rows of squares and circles, and the sizes of the squares' sides and the circles' diameters both increase from  $3\mu\text{m}$  to  $5\mu\text{m}$  then to  $8\mu\text{m}$ . In the mask3, the  $3\mu\text{m}$  square in the mask2 is skipped.

---

\* **Corresponding author** Tel: 86-592-2185927; Fax: 86-592-2186383; E-mail: sundh@jingxian.xmu.edu.cn

## 2.1 Simulations of ADE

RIE is selected in the simulation of ADE. Etchings under the parameters displayed in Fig.2 and Fig.3 are simulated respectively. By comparison Fig.2 with Fig.3, it can be concluded that the results of RIE etching have nothing to do with the directions of wafer. It also can be seen that, theoretically, vertical sidewalls but not tips are formed by RIE. From Fig.2, it is obvious that the increase of the etching time just deepens the sidewalls vertically. But in practice, the undercut etching should be taken into account in RIE etching. Actually, if etchants with suitable undercut etch rate and down etch rate are selected, tips also can be achieved<sup>8</sup>.

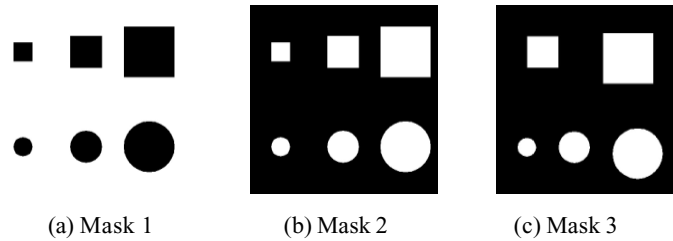


Fig.1 mask figures

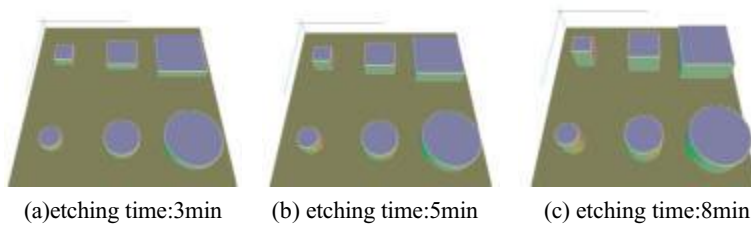


Fig.2 Simulation of RIE etching in (100) wafer and aligned with <110> directions

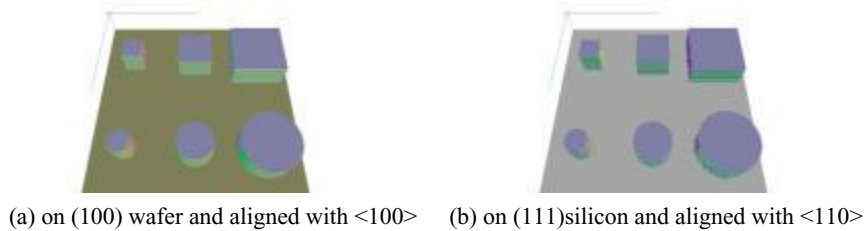


Fig.3 Simulation of RIE for 8min

## 2.2 Simulations of AWE

In these simulations, mask1 is also employed. From Fig.4 and Fig.5, three phenomena can be observed. Firstly, <110> directions must be oriented if we want to get tips through anisotropic wet etching on (100) wafer. Secondly, the etching time should be exactly controlled because over-etching would cause the tips to be shortened or even to be vanished. On the contrary, if the etching is not long enough, truncated pyramids not tips are formed. Thirdly, the circle SiO<sub>2</sub> caps can be stripped off more easily than the square caps.

The simulations results reveal that, in AWE, mask orientation and etching time is critical to acquire tip with expected height.

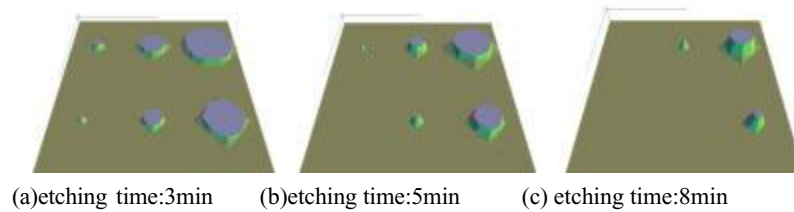


Fig.4 Simulation of AWE on (100) wafer and aligned with <110> directions

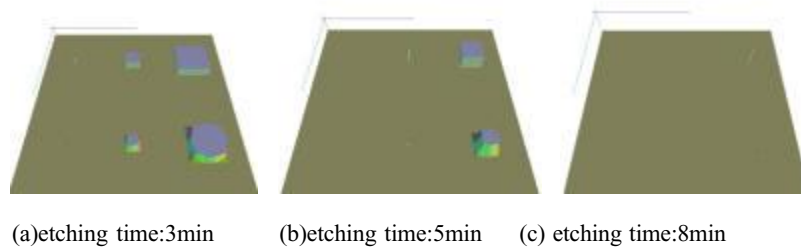


Fig.5 Simulation of AWE on (100) wafer and aligned with <100> directions

### 2.3 Simulations of etching inversed pyramids by AWE

Etching down by AWE to form inversed pyramids had been simulated in this section with Mask2. The results in Fig.6 show that inversed and truncated pyramids formed by square masks and circle masks are the identical, which proves that the contours of masks just affect the depth of the reversed pyramids and that the sidewalls of pyramids are well defined by {111} planes. It also can be seen that if the etching rate of {111} is ignored, the pyramids will not be affected by over-etching.

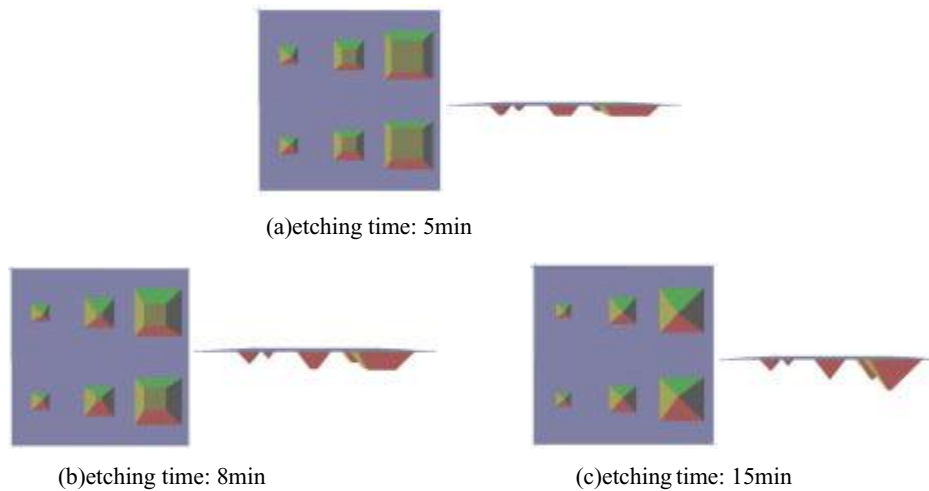


Fig.6 Top view and main view of the simulation results of etching truncated pyramids through AWE on (100) wafer and aligned with <110> directions

In Fig.7, the oriented directions are converted to <100> and mask3 is used. The 3 msquare in mask2 is erased for it is too crowded here. It is obvious that the sidewalls are also defined by {111} planes. The intersections of the sidewalls of pyramids and surfaces of the wafer are made up of the smallest squares that align with <111> and can cover the self-closed

masks<sup>9</sup>, which can explain why the pyramids formed by square are larger than that formed by circle in the corresponding size. That is to say that the etched pits depend on contour and orientation of mask, which can be controlled with much more precisely. In the case of circle mask, for it is around, orientation isn't in need and the height of the pyramid is determined only by the diameter. According to the crystalline structure of silicon, the angle of {100} and {111} is 54.74°. So:

$$h = (D/2) * \tan 54.74 = 0.7072D \tag{1}$$

Where,  $h$  is the height of the pyramid,  $D$  is the diameter of the circle mask.

By analysis and comparison of the simulations results, it is expected that fabricating silicon tips by AWE combining with bonding is much easier and more controllable.

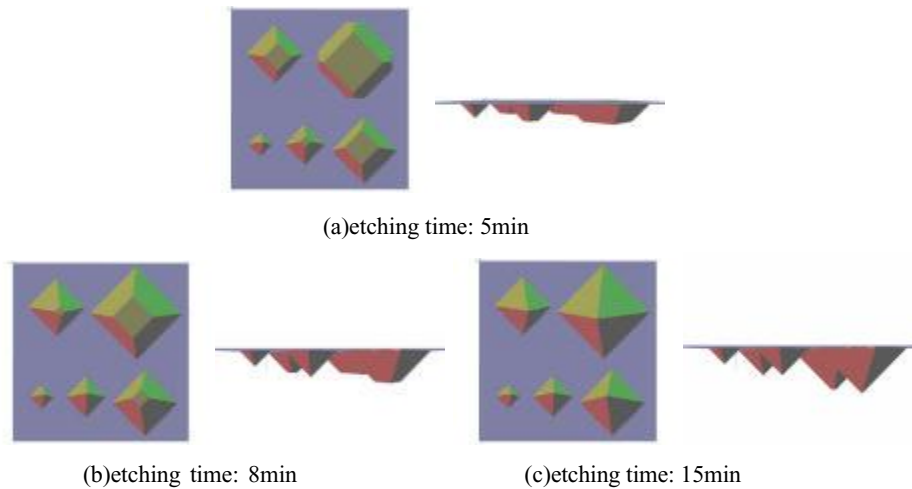


Fig.7 Top view and main view of the simulation results of etching truncated pyramids by AWE on (100) wafer and aligned with <100> directions

### 3. Experiments

Fig.8 shows the process of ADE and AWE to fabricate silicon tip. Firstly, silicon wafer was thermally oxidized. Then photoresist was spun and lithographed, and the oxidization is patterned. Finally, the wafer was etched down by etchant gas in ADE and by etchant solution in AWE respectively.

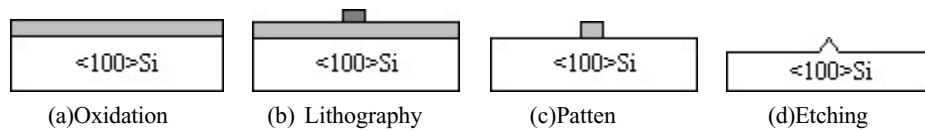


Fig.8 Process of ADE and AWE

#### 3.1 Experiments on ADE

In ADE, SF<sub>6</sub> is selected as etchant for it is un-poisonous and has a comparable high etch rate with undercut etching. Three kinds of dry etching PE, RIE and ICP had been done. The results of PE and the RIE show that the surface of silicon after the etching is very coarse, so the experiments on PE and RIE were suspended. The surface of wafer etched by ICP is more smoothly. Fig.9 is the ICP etching result photo taken through microscope. Compared to simulations above, the etchant SF<sub>6</sub> has undercut etching, so tip not vertical sidewall is formed as shown in the Fig.9.

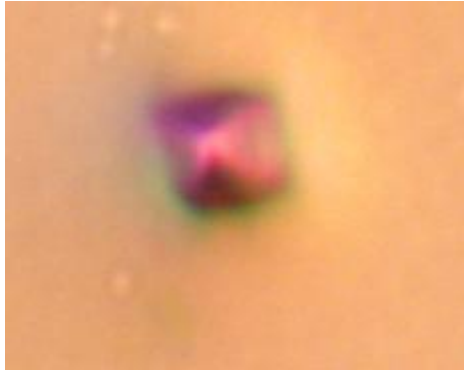


Fig.9 photo of tip by ICP( $\times 500$ )

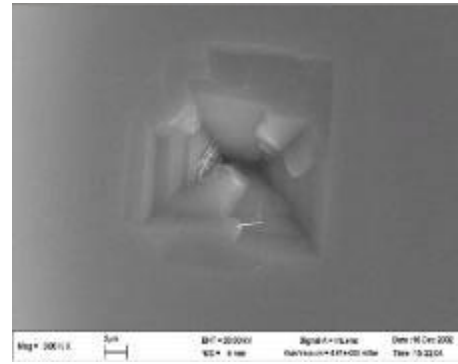


Fig.10 SEM of tip by AWE

### 3.2 Experiments on AWE

In anisotropic wet etching, 25% TMAH is used as etching solution. An irregular tip is shown in Fig.10. This is because that etching on the convex corner is fast and unstable for the etchant encounters no  $\{111\}$  planes<sup>9</sup>, which makes it very difficult to control the contour of the tip in AWE.

### 3.3 Experiments on AWE combining with bonding

The process shown in Fig.11 is designed to reverse the pyramids again to form tips. First, silicon wafer was thermally oxidized. Then photoresist was spun and lithographed, and the oxidation is patterned. The wafer is etched down to form reversed pyramids by 25% TMAH. After AWE is finished, oxidation is stripped off and a layer of  $\text{Si}_3\text{N}_4$  is sputtered to act as isolation. Finally, the wafer was bonded with glass and the silicon is etched off to release the tips.

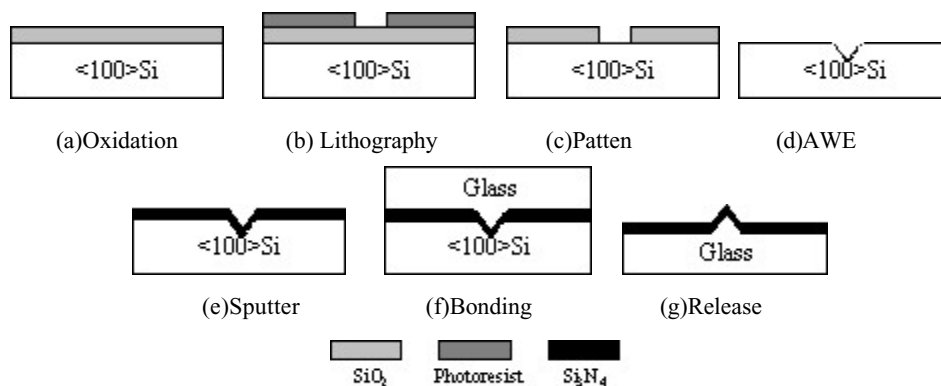
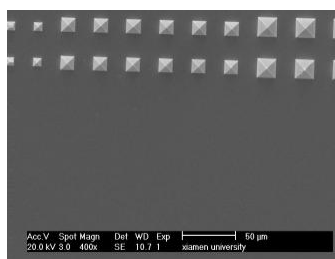


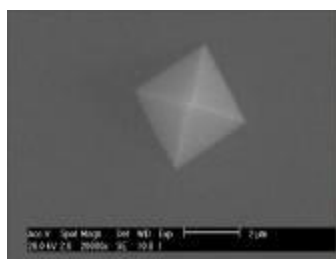
Fig.11 Process of AWE combining with bonding

Through the process described above, an array of tip had been fabricated successfully just as shown in Fig.12(a). The identity of the two rows of tips, which are formed by square mask with side aligned  $\langle 100 \rangle$  and circle mask respectively, verifies the conclusions discussed in the simulation. The height of tip in Fig. 12 (c) is measured by Laser Scanning Confocal microscope OLS1200 which produced by Olympus, and the result is  $3.78\mu\text{m}$ . According to equation (1), the height of tips formed by  $5\mu\text{m}$  is  $3.54\mu\text{m}$ . One reason why the tip is higher than expected is due to long time over-etching which allow enough time to form reversed pyramids for larger mask and, although the etching rate on  $\{111\}$  is very small, it can't be ignored in long time etching. Another possible reason is that the errors accumulated from the former steps. What is more,

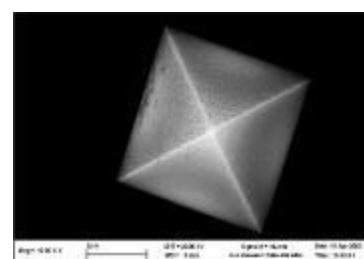
the top diameter of the tip is only about 23.44nm. The experimental results prove that this fabrication technology is a reliable and well controllable technique to fabricate silicon tip.



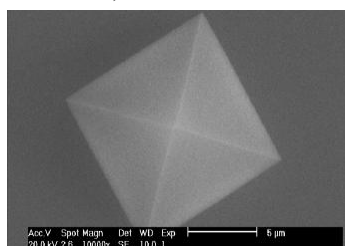
(a) an array of tip (the first row are fabricated with square mask and the second row with circle mask)



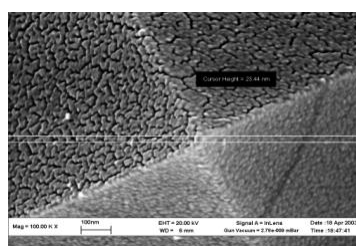
(b) tip by 3 $\mu$ m mask



(c) tip by 5 $\mu$ m mask



(d) tip by 10 $\mu$ m mask



(e) top of the tip

Fig.12 SEM pictures of tips utilizing anisotropic wet etching combining with bonding

#### 4. Conclusions

In this paper, simulations of the three fabrication technologies of silicon tips ADE, AWE and AWE combining with bonding are analyzed and discussed, and experiments had been done to testify the simulations. From the simulation results, in the down etching to form tips directly by either dry etching or wet etching, the mask and the etching time should be controlled precisely to get tips with regular contour and expected height. In AWE, the side of mask should even align with (110). However, in the fabricating tips from reversed pyramids, the mask is the main issue that decides the final tips. If circle mask is employed, the orientation isn't in need and the height of tips has relation only to the diameter. The experiments on ADE and AWE show that the parameters of fabricating silicon tip by these two techniques have little tolerance. The details experiments on AWE combining bonding not only verify the conclusions drew in the simulations, but also prove that it is a reliable technique and can be easily controlled to fabricate silicon tip with very small top radius, in which diameter within 23.44nm had been achieved.

#### Acknowledgement

This work is supported by Fujian Natural Science Fund (A0110003) and Key Project of Science Plan of Fujian, China. (2002H022)

#### Reference

1. C.Julian Chen, *Introduction to Scanning Tunneling Microscopy*, chapter 1, Oxford University Press, London, 1993.
2. Kenny T W, Reynolds J K, Podosek J A, et al. "Micromachined infrared sensors using tunneling displacement".

Transducers Rev Sci Instrum, 67(1):112-113, 1996.

3. Miller L M, Kenny T W, Kovricicb J A. "A u-magnetometer based on electron tunneling". *Proceedings of the 9<sup>th</sup> annual International Workshop on Micro Electro Mechanical Systems* ,2(11-15):467-472, 1996.
4. Margues M I, Serena P A, Nicolaescu D, et al. "Modeling of a pressure sensor based on an array of wedge emitters". *Applied Surface Science*, 146:139-244, 1999.
5. Yeh Chingwen, Khalil Najafi. "A low-voltage tunneling-based silicon microaccelerometer". *IEEE Transactions on Electron Device*, 44(11):1875-1882, 1997.
6. Rockslad H K, Kenny T W, Reynolds J K, et al. "A miniature high-sensitivity broad-band accelerometer based on electron tunneling transducers" . *Sensors and Actuators A*, 43:107-114, 1994.
7. Ivor Brodle, Paul R. Schwoebel. "Vacuum Microelectronic Devices" . *Proceedings of the IEEE*, 82(7):1006-1034, 1994.
8. Marc J.Madou. *Fundamentals of Microfabrication 2<sup>th</sup> edition*. CRC Press, New York, 2002.
9. M.Elwenspoek, H. V. Jansen. *Silicon Micromaching*. Cambridge University Press, Cambridge, 1998.
10. WANG Yanhua. "Research on Fabrication Techniques of Si tip used in Micro Machined Tunneling Gyroscope". Master Thesis. Xaimen University, 2003.
11. WANG Yanhua, WANG Mingliang, SUN Daoheng. "Fabrication and application of silicon tip in sensor technology". *Journal of Transducer Technology*, 22(6):58-61, 2003.