Analysis of a New Family of DC-DC Converters with Input-Parallel Output-Series Structure

by

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CERTIFICATE OF ORIGINALITY

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Juan Carlos Ostos

To Jesus, my guardian Angels, my parents, my wife, my daughter, my friends, Dylan (supervisor) and whom love me.

Abstract

There is an increasing trend of development and installation of switching power supplies due to their highly efficient power conversion, fast power control and high quality power conditioning for applications such as renewable energy integration and energy storage management systems. In most of these applications, high voltage conversion ratio is required. However, basic switching converters have limited voltage conversion ratio. There has been much research into development of high gain power converters. While most of the reported topologies focus on high gain and high efficiency, in this thesis, the input and output ripple currents and reliability are also considered to derive a new converter structure suitable for high step-up voltage conversion applications. High ripple currents and voltages at the input and output of dc-dc converters are not desirable because they may affect the operation of the dc source or the load. A number of converters operating in an interleaved manner can reduce these ripples. This thesis proposes a dc/dc switching converter structure which is capable of reducing the ripple problem through interleaved action, in addition to high gain and high efficiency voltage conversion. The thesis analyses the proposed converter structure through a dual buck-boost converter topology. The structure allows different converter topologies and combinations of them for different applications to be configured. The study begins with a motivation and a literature review of dc/dc converters. The new family of high step-up converters is introduced with an interleaved buck-boost as an example, followed by small-signal analysis. Experimental verifications, conclusions and future work are discussed.

List of Publications

1. J. Ostos and D.-C. Lu. Modeling and analysis of CCM non-isolated high step-up interleaved buck-boost dc/dc converter. *Power and Energy (PECon) on* , 2012 IEEE International Conference, 2012, pp. 28-31.

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It has been an adventure to write this thesis and finally for the special thank you, I am forever indebted to my wife and daughter for the long support and encouragement.

Contents

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List of Symbols

$AERC$	Active auxiliary Edge-Resonant Cell
$BESS$	Battery energy storage system
CCM	Continuous conduction mode
CR	conversion ratio
D	Duty cycle
DCM	Discontinuous conduction mode
DG	Distributed Generation
$FPGA$	Field-programmable gate array
$G2V$	Grid to vehicle
$ICAO$	International Civil Aviation Organisation
$I_{in_{p-p}}$	Peak-to-peak input current
$I_{o_{p-p}}$	Peak-to-peak output current
IT	Information technology
MG	Micro grid
$MISSCO$	Minimum separable switching configuration
$MMCCC$	Multilevel Modular Capacitor-Clamped DC-DC Converter
$MPPT$	Maximum power point tracking
M_{VDC}	Output to line transfer function or $\frac{V_o}{V_{in}}$
PFC	Power Factor Correction
$PHEV$	Plug-in-hybrid Electric Vehicle
PV	Photovoltaic
PWM	Pulse Width Modulation
RPA	Remotely Piloted Aircraft
$SEPIC$	Single-ended primary-inductor converter
SG	Smart Grid
S^2PFC	Single-stage power-factor-correction/ted

TEG	Thermoelectric Generator
T_p	Control to output transfer function or $\frac{V_o}{D}$
UAV	Unmanned Aerial Vehicle
UPF	Unity power factor
UL	Underwriters Laboratories
$V2G$	Vehicle to grid
VSC	Voltage source converter
ZCS	Zero current switching
ZVS	Zero voltage switching
$ZVZCS$	Zero Voltage and Zero Current Switching
Greek Letters	
δ	Perturbation of , e.i. δV_o = perturbation of V_o
Δ	Time used in DCM. i.e. see Figure 3.6

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Chapter 1

Introduction

1.1 Background and Motivation

In recent years, switching mode power supplies have been increasingly applied in many areas, for example in PV power systems [1], hybrid electrical vehicles (HECs), thermoelectric generators (TEGs), aerospace, battery-powered devices, and so on. The switching power supplies provide efficient and high quality power conversion between the source and the loads. One example is the photovoltaic system where the switching power supply tracks the maximum power point and regulates the bus voltage.

Of the switching power supplies, dc/dc converters are used extensively. The dc/dc converters are needed because sources such as fuel cell, PV panels and batteries are of low voltage. Therefore a high step-up conversion is needed.

Unfortunately dc/dc converters have limits when stepping up the voltage. Ideally high-step-up dc/dc converters can achieve infinity voltage but in reality this is limited by the losses in the converter. To mitigate losses some techniques like Zero Current Switching (ZCS) [1] and Zero Voltage Switching (ZVS) can be used. However, they cannot practically eliminate the losses completely. There is a need for a new converter structure which provides high step-up ratio even in the presence of losses.

1.2 Objectives

The objective of this thesis is to introduce and analyse a new family of dc/dc converters with an input-parallel output-series structure. A buck-boost converter topology is used as a case study to verify the converter structure concept and associated implementation techniques.

The new family has the benefit of interleaving the currents at both input and output in order to have smoother input and output currents than that of basic converters. In addition this converter structure presents less losses compared with basic converters because it inherits a direct power transfer property which reduces the amount of power processing by the converter and hence producing high power conversion efficiency.

1.3 Contributions

The contributions of this thesis are related to the development of dc/dc switching power converters for high step-up applications. These includes the following:

- Proposed a non-isolated dc/dc converter structure for high step-up voltage conversion which inherits direct power transfer property.
- Derived a new family of dc/dc converters based on the proposed converter structure.
- Analyzed both steady state and dynamic behaviour of the proposed converter structure based on a buck-boost converter topology.

1.4 Outline of the Thesis

The literature review in Chapter 2 gives insight into the existing topologies and uses of dc/dc converters for high step-up conversion. Some dc-dc converters can be seen coming from other general non-direct current topologies. This is the case of multilevel inverters, where a dc-dc multilevel converter can be derived from. Also dc/dc converter design considerations regarding ripple, components and materials are presented. In addition dc/dc applications regarding to PV/Battery/EV in Smart Grid are shown.

In Chapter 3, a new family of high step-up DC-DC converters is introduced. Steady-state analysis is performed.

In Chapter 4 the small-signal analysis of high step-up dc-dc converters is presented. There are several techniques to produce a small-signal model such as the average circuit, fast analytical techniques [2], Minimum Separable Switching Configuration (MISSCO) technique, and the state-space technique. The average circuit technique, MISSCO technique and the state-space technique are used in this thesis.

In Chapter 5 the experimental verification and discussion are presented on a dual buck-boost prototype.

In Chapter 6 conclusion and future work are discussed.

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[1] H. Abu-Rub, M. Malinowski, and K. Al-Haddad, *Power Electronics for Renewable Energy Systems, Transportation and Industrial Applications.* Wiley, 2014. [Online]. Available: http://books.google.com.au/books?id=KGq8AwAAQBAJ

[2] V. Vorperian, *Fast Analytical Techniques for Electrical and Electronic Circuits.* Cambridge University Press, 2002. [Online]. Available: http://books.google.com.au/books?id=DYgS4nkJ5W8C

Chapter 2

Literature review

2.1 Problem with Basic Converters to Meet High Gain Demand

In contrast to ideal converters which have infinity voltage gain, actual converters have lower gain because they are limited by losses. As we can see from [1], the M_{VDC}[1] and the T_P[2] of a boost converter has limitations.

$$M_{VDC} \equiv \frac{V_o}{V_{in}} = \frac{1}{(1-D)[1+\frac{V_F}{V_o}+\frac{r}{(1-D)^2 R_L}]} \tag{2.1}$$

$$T_{PDC} \equiv \frac{V_o}{D} = \frac{V_{in}}{D(1-D)[1+\frac{V_F}{V_o}+\frac{r}{(1-D)^2 R_L}]} \tag{2.2}$$

As we can see from (2.1) and (2.2) the denominator is affected by R_L and r where R_L is the load resistance and r is the lump-sum stray resistance of the converter. When the duty cycle increases, the associated loss is also increased. This results in a decrease of voltage gain, in particular when duty cycle is close to 1.

[1] M_{VDC} is the output-to-line transfer function or $\frac{V_o}{V_{in}}$

[2] T_{PDC} is the control-to-output transfer function or $\frac{V_o}{D}$

2.2 Review of Existing High Gain Converter Topologies

2.2.1 Cascaded Topology

Cascaded converters are obtained by connecting a number of converters in series. They are used to increase or decrease the range of the conversion ratio. There is a great demand for a non-inverting step-down/step-up dc-dc converter, especially for battery-powered portable electronics applications [1]. For example, the voltage of the lithium-ion battery changes from 4.2 to 2.8 V and the supply voltage of an electronic circuit is 3.3V. A non-inverting step-down/step-up converter can be obtained by cascading the buck and boost converters [1]. The output filter capacitor of the buck converter can be removed, and the buck output filter inductor and the boost input filter inductor can be combined to obtain a non-inverting buck-boost converter as shown in Figure 2.1 [1]. However, this circuit requires twice as many components as a single-stage buck-boost converter, which increases the size, cost and weight [1].

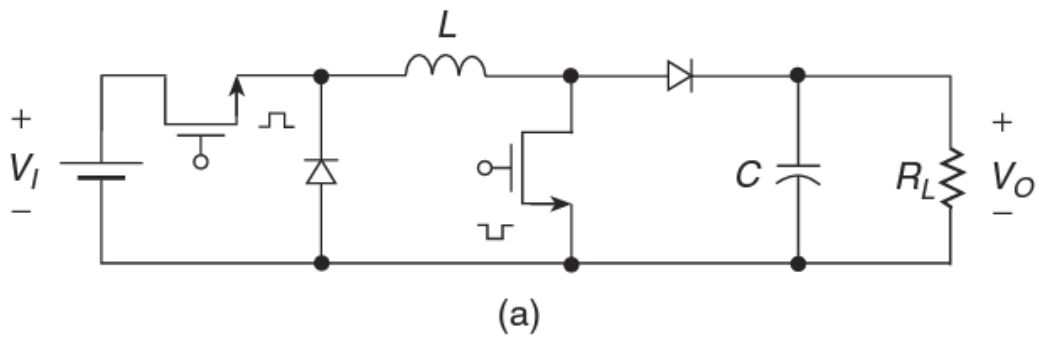

Figure 2.1: Non-inverting buck-boost converter [1].

Buck, boost, buck-boost, Ćuk converters and most converter topologies can be cascaded [2]. The buck-boost and Ćuk topologies are flexible in voltage delivery but they are more expensive than buck or boost due to higher component stresses hence their cost. Nevertheless the efficiency of cascaded converters are limited as the overall conversion efficiency is the product of individual converter efficiencies. The more converters they are cascaded, the lower efficiency the system is.

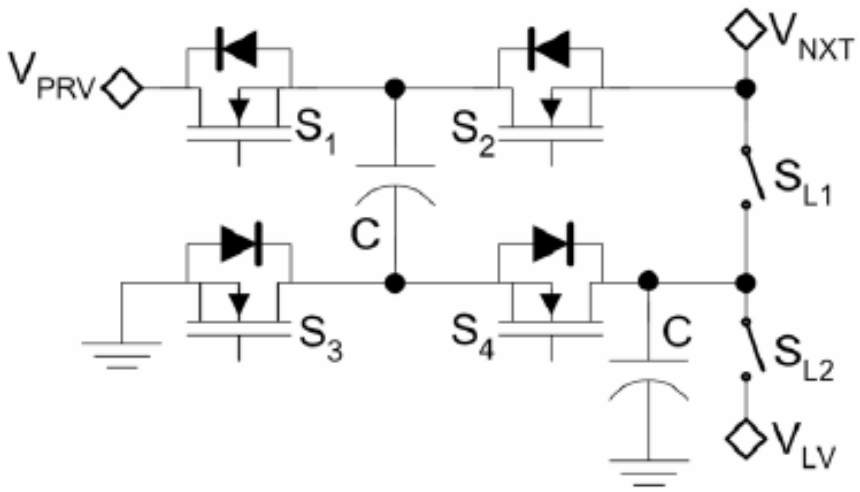

Figure 2.2: Modified module of a Multilevel Modular Capacitor-Clamped DC-DC Converter (MMCCC) [4].

2.2.2 Multilevel Topology

Multilevel converter/inverters have three typical topologies which include the typical cascaded, capacitor clamped and diode clamped multilevel structures [3, page 422]. A generalised multilevel inverter topology unifies the three typical multilevel inverters and has the ability to generate other multilevel topologies, such as modular multilevel converter (M^2C), magnetic-less multilevel converters DC-DC converters, and stacked multicell converters [3]. Therefore the multilevel DC-DC converter can be seen as a special case of multilevel converter/inverters that achieve high-voltage boost factor without magnetic components. The elimination of magnetic components not only reduces the converter's size and loss, but also is more suitable for high-temperature applications, because it avoids the saturation and instability factors owing to the dramatic decline in magnetic permeability with increasing temperature [3]. A magnetic-less 3X dc-dc converter is explained [3]. A 3X's simplified version is also reported [3]. A multilevel modular capacitor clamped dc-dc converter (MMCCC) and the nX converter are explained in [3] [6]. All these converters are suitable for high-power systems.

A multilevel dc-dc converter with programmable conversion ratio (CR) is introduced [4]. This converter is a modified version of an Multilevel Modular Capacitor-Clamped DC-DC Converter (MMCCC). A module and a prototype are shown in Figs. 2.2 and 2.3 [4] respectively.

In [5], another topology is proposed and it can be implemented without magnetic

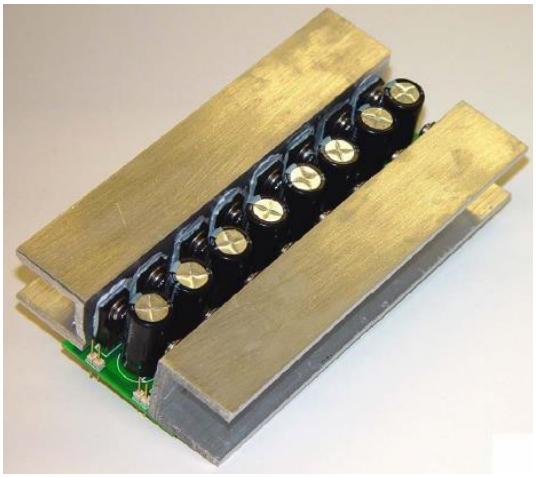

Figure 2.3: 100 W prototype of the universal MMCCC converter [4].

components. These magnetic components are avoided because they are usually bulky, low efficiency, and can not be further integrated [5]. In [5] a switched capacitor dc/dc converter , which consists of only switching devices and capacitors , also called as "charge-pump" is presented.

A N-level multilevel converter [6] simulated in Simulink/Matlab with 2N-1 capacitors, 2N+2 diodes, two inductor and only one switch is presented in Figure 2.5 [6]. The drawback of multilevel is the many components in comparison with interleaved topology.

Another drawback of multilevel converter is the balancing of capacitors, see Figure 2.4 [7]; it is not possible to discharge an individual capacitor of these topologies, to do this is necessary to connect individual loads at each capacitor, despite of this some multilevel converters have available switching states to ensure capacitor voltage balancing, that means, it is possible to charge and discharge the capacitors of these topologies only using available switching states [7]. A topology to investigate the balancing of capacitors is shown in Figure 2.5 [7].

Multilevel topology has variable voltage outputs and can be found in plug-in hybrid electric vehicles because they need fast charging.

Several non-isolated bidirectional dc/dc converters suited for charge station applications that have been reviewed and compared [8] . The recommended converter is shown in Figure 2.6 [8], that is a three-level bi-directional dc/dc converter because the inductor size is only one third of the half bridge counterpart and a $95.1 - 97.9$ full load efficiency can be achieved in charging mode with 180-360V battery voltage. Some more key terms can be found here [8] like "grid support",(see subsection **??** that talks about the grid),

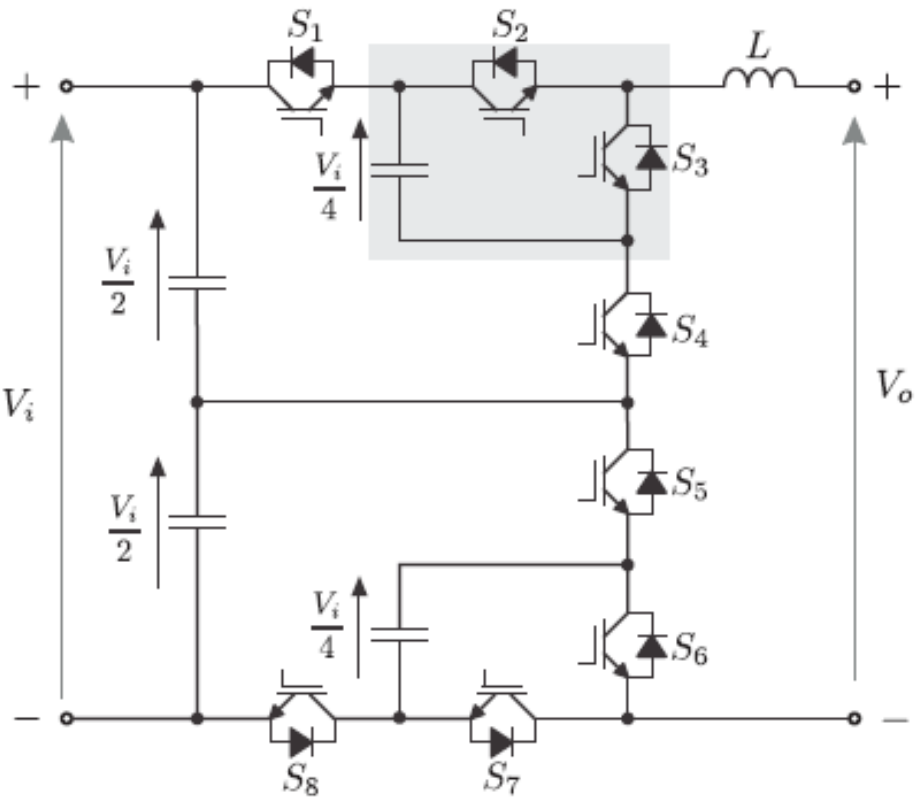

Figure 2.4: Multilevel converter. The balance of voltage of the capacitors is investigated using this topology [7].

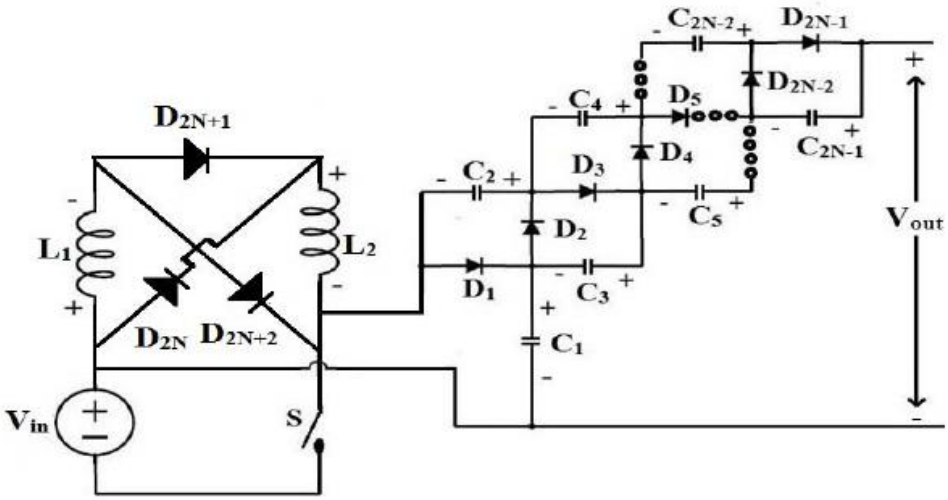

Figure 2.5: Switched inductor floating output n-level dc-dc multilevel converter [6]

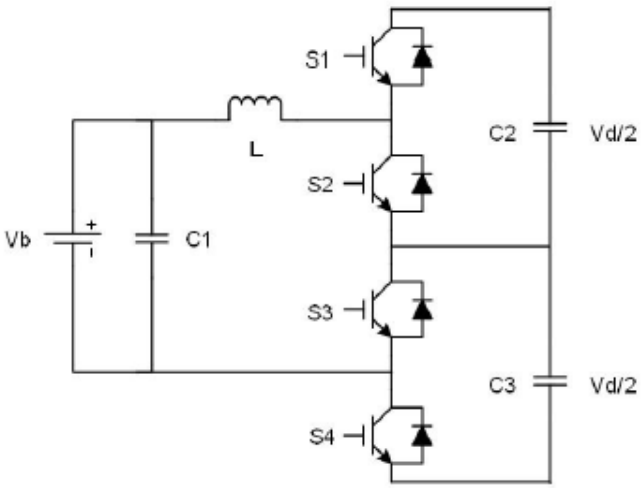

Figure 2.6: A neutral point clamped three level DC/DC converter for plug-in hybrid electric vehicles (PHEV) [8]

such as reactive and real power (V2G) injection[3], "current harmonic filtering" and "load balance". This paper shows the benefits of the interleaving effect because an interleaved half-bridge converter is mentioned as well.

Reference [9] proposed some isolated dc/dc converters for electric vehicles. Here three high-power isolated bi-directional dc/dc converters can be used in PHEV/EV dc charging infrastructure. These are tested and a summary table is published. Some factors to discriminate these findings are number of components, voltage and current stress, light load circulating current, soft switching range, output fault tolerance, control complexity, etc.

Electrical hybrid vehicles can use fuel cells and the integration with a dc-dc converter is shown in Figure 2.7 [10]. There are several options to integrate them using power electronics: series, dc-link, high-frequency ac-link, or multilevel configurations [10]. Although the electrical efficiency of a fuel cell can be theoretically greater that 70%, with current technology it is only capable of reaching 45% [10]. In order to overcome this drawback a multilevel dc/dc converter is introduced in [10]. A multilevel dc-dc converter three-phase inverter is shown in Figure 2.8 [10].

Multilevel dc-dc converters can be cascaded [11]. There are different multilevel dc-dc converter topologies [12] [13] [14] [15] such as general multilevel dc-dc converter and one-to-many topology. Two additional cascaded topologies are presented [11] that can increase the number or output levels.

[3]V2G applies where the vehicle gives back energy to the grid.

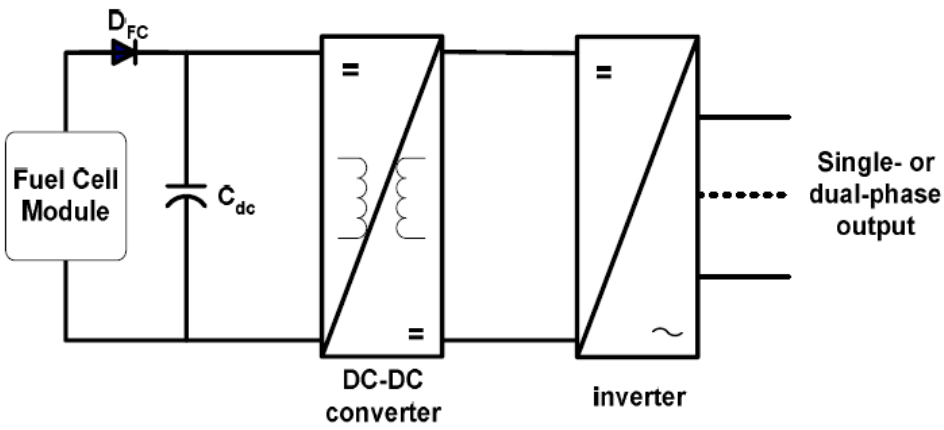

Figure 2.7: Typical fuel cell power electronics interface block diagram [10].

A multilevel boost converter with 3 MOSFETS is introduced for PV applications [16]. This converter as shown in Figure 2.9 is driven in DCM to boost the voltage but this converter has more MOSFETS than the proposed interleaved topology and therefore more losses.

In summary, the multi-level topology has some disadvantages [17]:

- High number of semiconductor devices.
- Complex control as a result of the large number of control devices.
- Large number of gate drive circuits.
- Several DC voltage sources are required.
- Need to balance voltages across capacitors used in voltage divider circuits.
- Large number of components that implies more switching losses.

2.2.3 Resonant Topology

This topology is achieved by adding a L_r and C_r around the switch. For example four (4) stages exist [18] for a buck-boost converter with resonance: Linear, Resonant, Recovering and Free-wheeling. The losses are reduced because the switching devices are forced to turn-on and turn-off at zero current and zero voltage. A disadvantage is the number of components is increased to force turn-on and off the switches.

Even though switching losses are significantly reduced by zero voltage switching (ZVS) or zero current switching (ZCS), where commutations are realised with either by ZVS

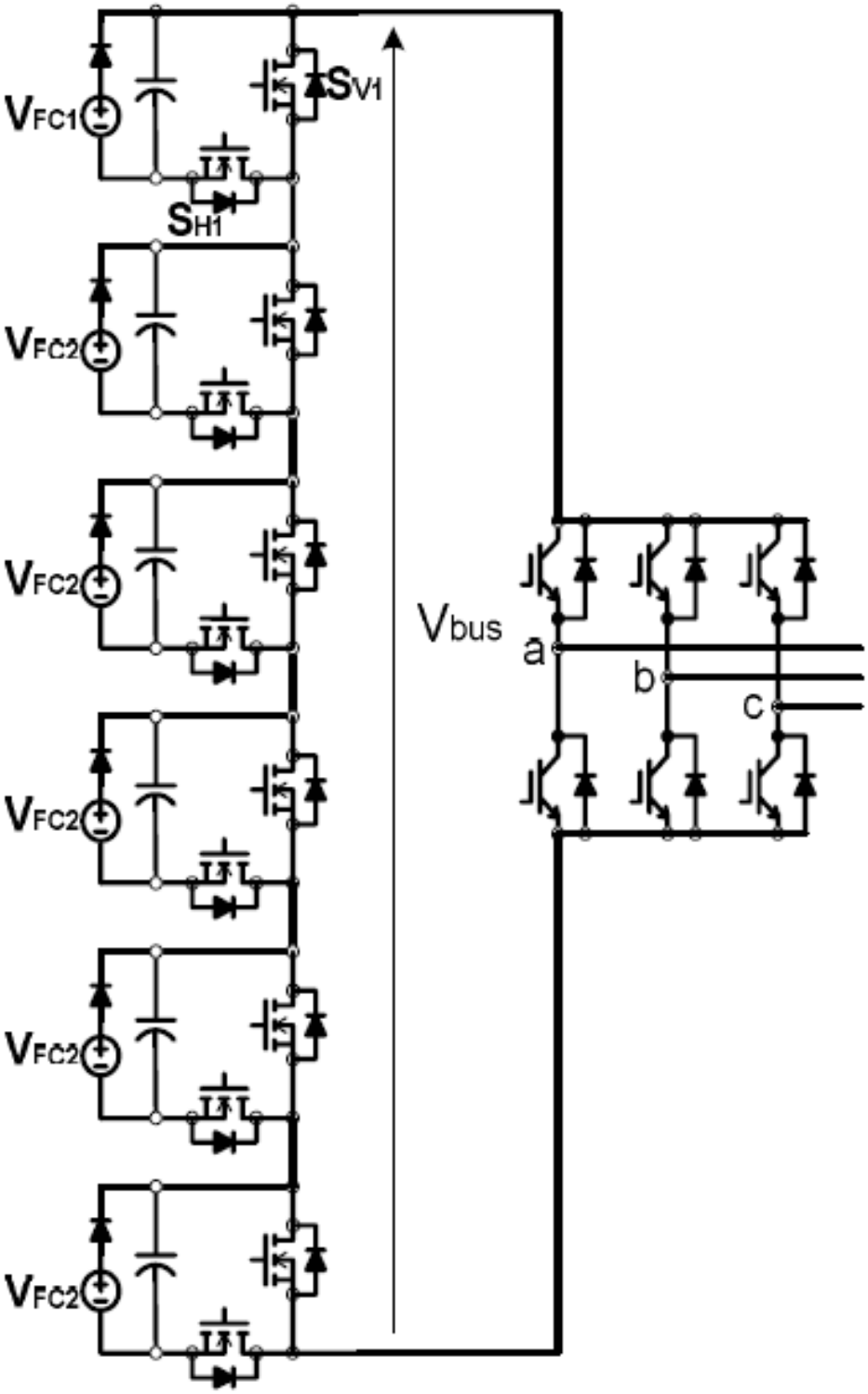

Figure 2.8: Multilevel DC-DC converter connected to a three-phase inverter [10].

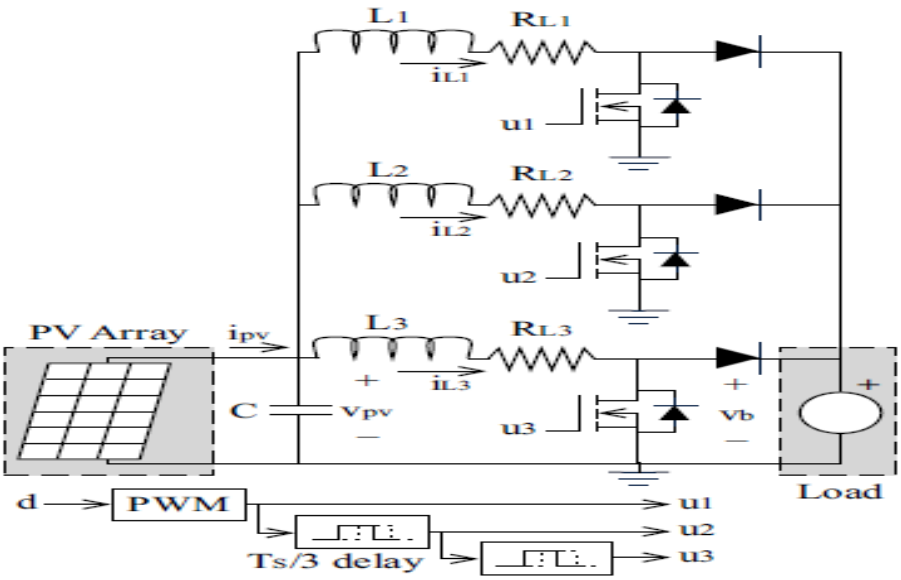

Figure 2.9: Multilevel DC-DC converter for PV use. [16].

or ZCS, resonant converters present excessive voltage and current stresses, power density is lower and control is harder than normal PWM converters [19], [20], [21], [22]. Some researchers have tried to address the aforementioned problems. For example [23] a Zero Voltage Transition-Pulse Width Modulation (ZVT-PWM) DC-DC converter is introduced.

2.2.4 Series Topology

Two integrated-battery boost converters in series are introduced in [24] where some advantages are found over the conventional series connected boost converters such as more steady dc bus voltage even under varying isolation levels. The topology is shown in Figure 2.10 [24]. The interleaving action could be applied to this topology as well.

If the aim is to boost the voltage in a photovoltaic (PV) panel , the string of boost dc-dc converters have disadvantages. The boost converter string cannot always deliver all the power from a mixture of shaded panels and those delivering full power [2]. One typical application of high output voltage is connecting a number of solar panels in series to step-up the voltage and to achieve this, a string of buck converters is used. This string requires more panels but will be the most efficient topology for a given cost [2] as shown in Figure 2.11.

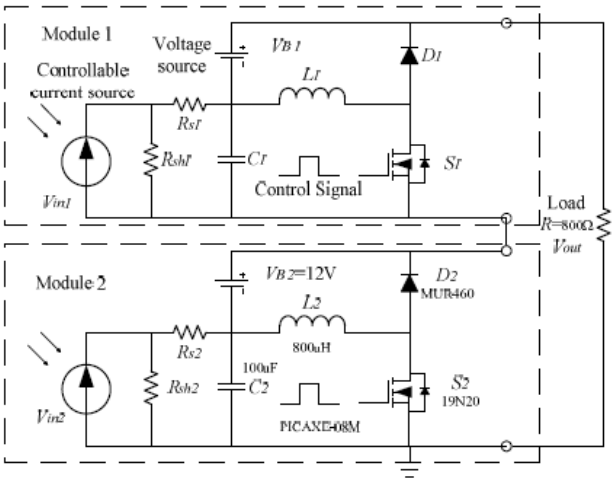

Figure 2.10: Block diagram of battery-integrated boost converter in module-based series connected PV system [24]

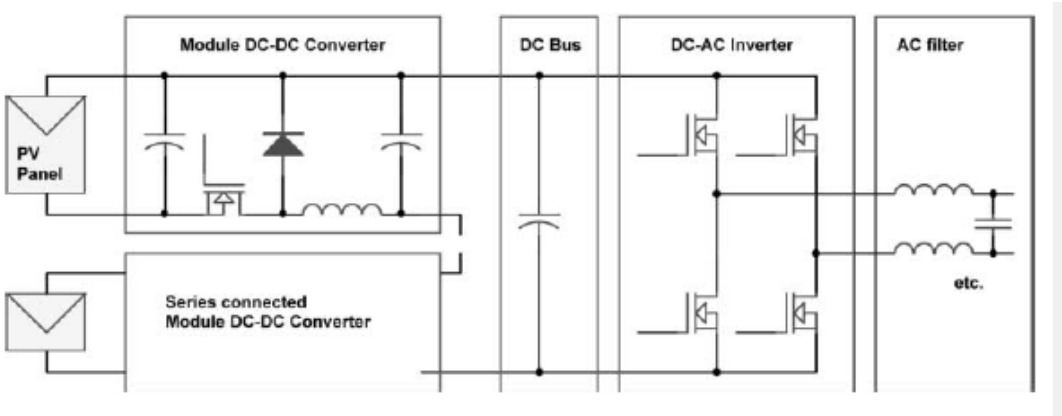

Figure 2.11: Series connected panel integrated dc/dc converters connected to a centralised dc/ac inverter [2].

2.2.5 Transformer Topology

Various converters with transformer isolation are found [25] and some of them are discussed:

- Ćuk with transformer
- Flyback
- Forward
- Full-bridge
- Half-bridge
- Transformer-coupled push-pull

A PWM flyback converter is a transformer (or isolated) version of the buck-boost converter. The transformer performs several functions in the flyback converter as described in [1]):

- Provides isolation.
- It stores magnetic energy.
- It changes the voltage levels.
- The output voltages can be either positive or negative.
- Additional secondary transformer windings and rectifiers may be added to provide more than one output voltage of any polarity.

In Figure 2.12 a non isolated converter based on a flyback topology is introduced in [26] where a transformer is used to step up the voltage. This DC-DC converter uses a reduced repeated power processing technique presented in [27]. This converter has applications in micro-grids and solar electrical energy systems which require high step-up DC-DC converters but may not necessarily require isolation transformer [26]. This configuration could be used with an interleaved topology presented in this thesis in Figure 3.1 on page 34, where the upper and lower stages have direct power processing as well.

To analyse and describe dc-dc converters usually authors begin with buck and boost converters. It is interesting to find another approach to developing dc-dc converters by using the flyback converter [28]. From the flyback other basic non isolated, minimum component (switch, diode and inductor), boost, and buck/boost can be realised [28].

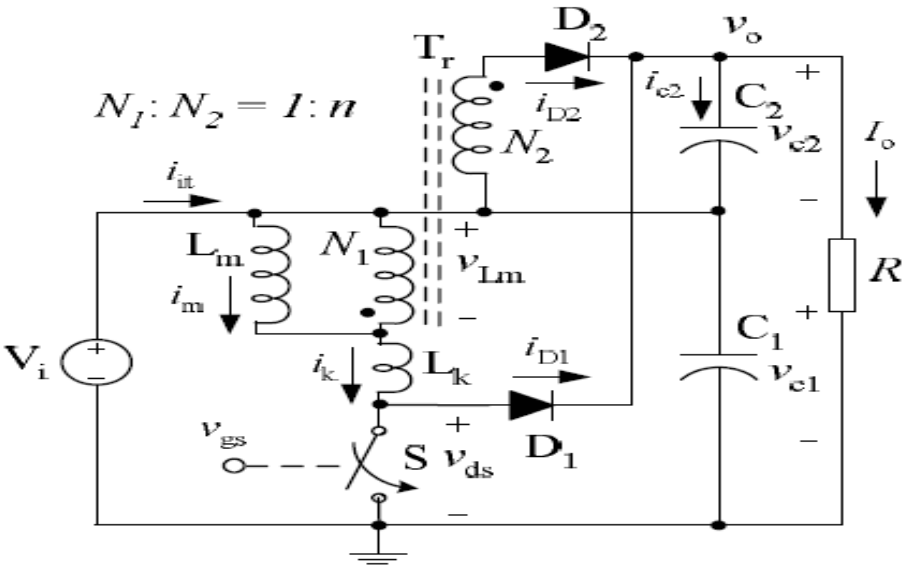

Figure 2.12: DC/DC high step-up with reduced power processing [27]

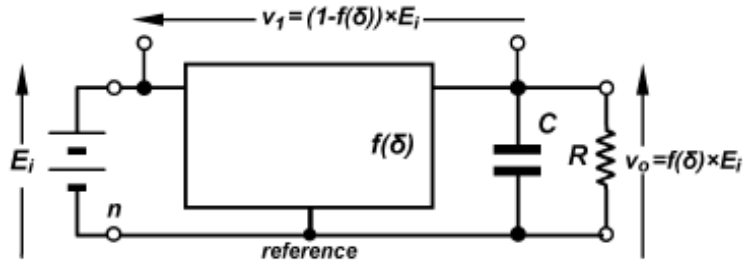

Figure 2.13: General dc-to-dc port to analyse dc-dc converters [28]

The generic three-port representation of dc-to-dc converters, with a negative voltage input node as reference, is shown if Figure 2.13 [28]. Even though interleaving is not discussed [28] other combinations with the generic three-port representation could be achieved.

A battery equalizer with an isolated bidirectional dc-dc converter (flyback) is introduced [29]. Figs. 2.14 and 2.15 are shown, where a dc-dc battery equalizer for 100 cells consisting of a bidirectional isolated dc-dc converter between two packs of cells, two pair of balancing buses, and 110 switches is shown. It is required that no more than two cells can be connected at the same time, otherwise it will cause short circuit because of the main serial buses. This converter could be a H-bridge for large scale applications [29].

Another dc/dc converter that uses transformer is the forward converter. In contrast to the flyback, this converter doesn't store energy during the conduction time of the switching element as transformers cannot store a significant amount of energy, unlike

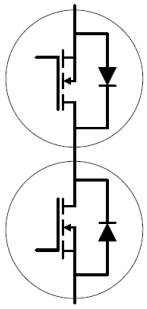

Figure 2.14: Battery equalizer for a battery system of 100 series connected cells [29]

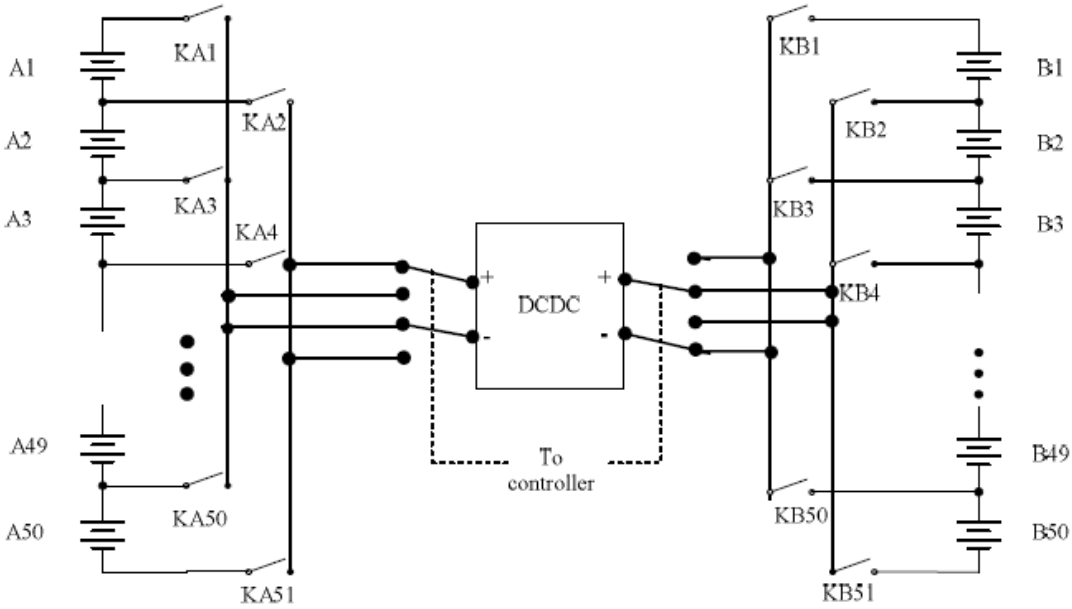

Figure 2.15: Bidirectional switch in equalizer [29]

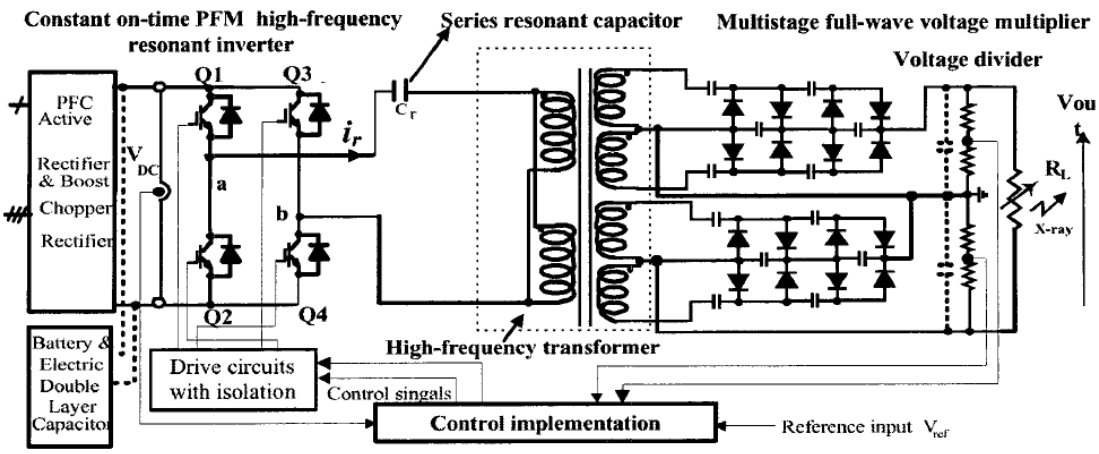

Figure 2.16: Series Resonant High-Voltage ZCS-PFM DC-DC Converter for Medical Power Electronics [30]

inductors. Instead, energy is passed directly to the output of the forward converter by transformer action during the switch conduction phase. This is the reason why flyback converter can be better viewed as two inductors sharing a common core.

A x-ray power generator for medical use is found with full-bridge topology. This is for high-voltage use and it is interesting to analyse the topology for dc-dc conversion. As expected, this topology uses more switches (the full-bridge uses 4 MOSFETS), more diodes and capacitors to increase the voltage and is more complex than the proposed topology in Chapter 3. In Figure 2.16 [30] a full-bridge converter is shown, to its left side there is a rectifier, to its right, the high-frequency transformer and the multistage full-wave voltage multiplier. The paths to charge the inductor are shown in Figure 2.17 [30].

In Figure 2.18 a three-phase current-fed push-pull dc-dc converter [31] that uses a high-frequency three-phase transformer that provides isolation between the power source and the load is shown. The three active switches are connected to the same reference, which simplifies the gate drive circuitry. This converter is suitable for applications where low-voltage power sources are used and the associated currents are high, such as fuel cells, photovoltaic arrays, and batteries [31]. When compare to the proposed topology the high weight of the transformer and the more number of switches is the disadvantage.

The disadvantage of the transformer topology is the high weigh of the transformer especially for applications that require the least weight as possible as planes or Unmanned Aerial Vehicle (UAV[4]) where every drop of weight counts.

[4]UAV, commonly known as drone and referred to as a Remotely Piloted Aircraft (RPA) by the International Civil Aviation Organisation (ICAO), is an aircraft without a human pilot aboard.

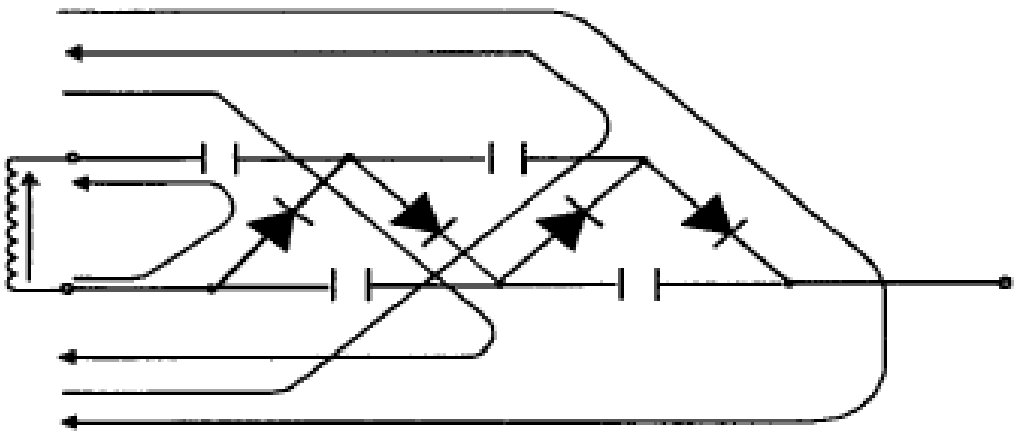

Figure 2.17: The increase in voltage is achieved by the transformer helped with the cascade topology of diodes and capacitors. The arrows illustrate the paths to charge the inductor [30].

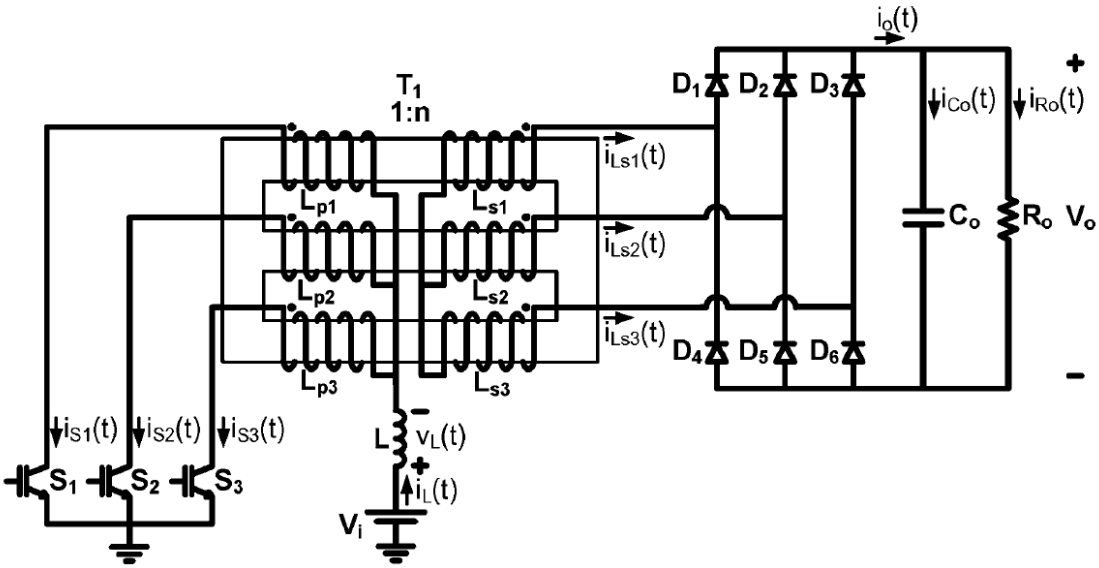

Figure 2.18: Three-phase current-fed push-pull dc-dc converter. [31].

2.2.6 Transformer-less Topology

The interleaved converter mentioned in [32] works without transformer which makes it lighter. In order to comply with the safety standard for most system applications, power supplies should be isolated[5]. This could be a drawback of transformer-less topologies.

2.3 DC/DC Converter Design Considerations

In order to design a proper converter some additional considerations are needed regarding ripple, components and materials.

2.3.1 Current ripples

Input and output current ripples are important for switching power converters design because they ensure the source and the load receives high quality power conversion. One method to achieve this is to arrange a number of identical converters in parallel and have them operate in an interleaved manner. A parallel interleaved topology is discussed in [33] which proposes an inductor current control with just one sensor instead of three sensors as in [34], therefore the weight, cost and volume is less. This kind of dc-dc converter with single sensor can be seen in Figure 2.19 [33] in contrast to Figure 2.20 [34] that uses three. These converters use more switches than the proposed interleaved buck-boost in Figure 3.2 on page 35. Field-programmable gate array (FPGA)[6] technology is used in [34].

In Figure 2.21 a novel algorithm to reduce the ripple is introduced [35] showing the benefits of interleaving helped with and ex-or gates in cascade for different sources and different duty cycles.

2.3.2 Converter components and materials

Not only the topology should be considered to have a high quality dc/dc conversion, but also the inductor, the materials and the integration should be considered.

[5]The safety standard in the US is regulated by the Underwriters Laboratories (UL). For most worldwide system applications, power supplies should satisfy the following safety agency standards: UL1950, VDE0805 (EN60950, IEC950), and CSA C22.2 No. 950-95.

[6]FPGA: According to National Instruments, at the highest level, FPGAs are reprogrammable silicon chips. Using prebuilt logic blocks and programmable routing resources, you can configure these chips to implement custom hardware functionality without ever having to pick up a breadboard or soldering iron.

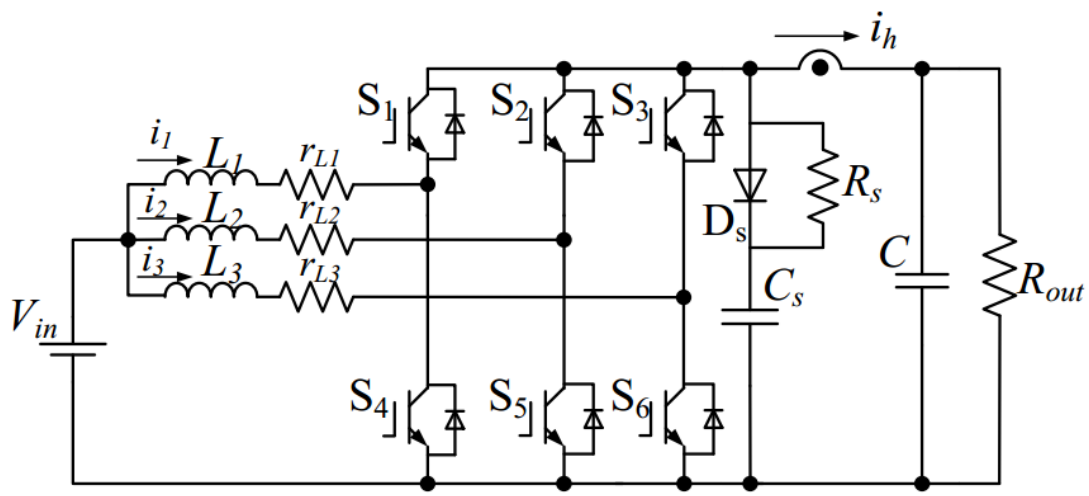

Figure 2.19: Inductor current control of three-phase interleaved dc-dc converter using single dc-link current sensor [33].

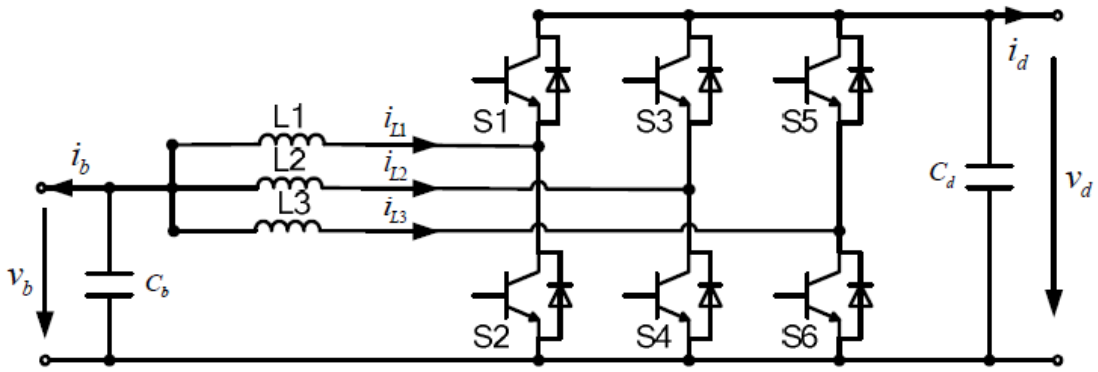

Figure 2.20: Current sharing schemes for three-phase interleaved dc-dc converter with Field-programmable gate array,(FPGA) technology implementation. Here [34] 3 sensors are used in contrast to Figure 2.19 which only uses one.

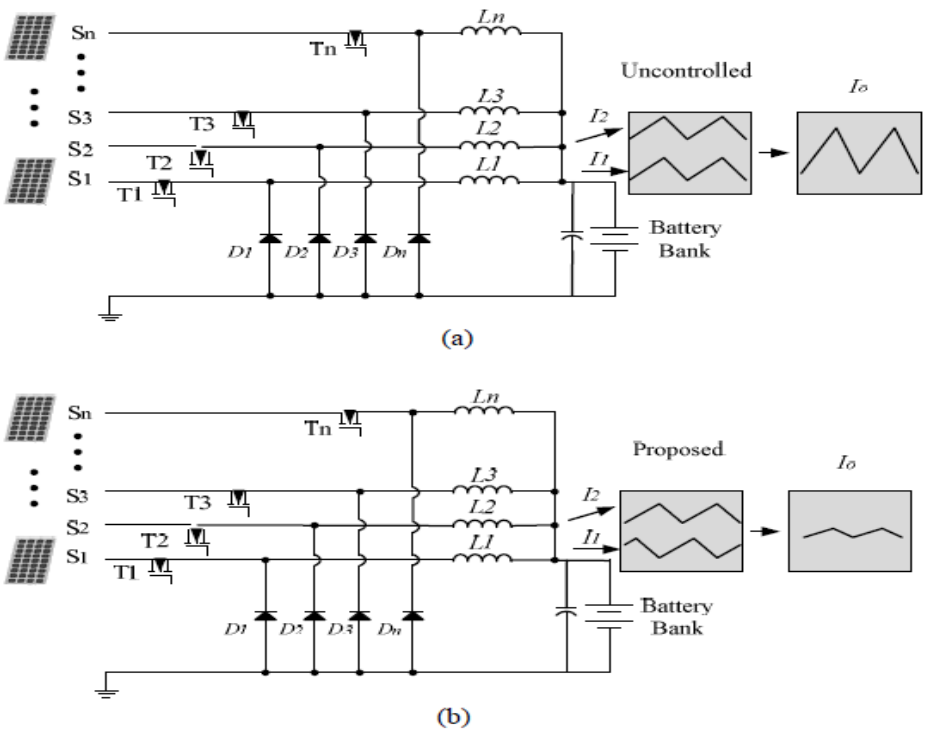

Figure 2.21: Interleaving effect helped with ex-or gates in cascade for photovoltaic applications [35]

The inductor design according to [36] is the main limitation in achieving both high frequency and underline high current in many of today's dc/dc converters. The inductor is typically the largest component in buck converters, and at high frequencies it becomes increasingly difficult to have high current output and remain competitive with the size of silicon. In addition to the inductor, the materials analysed are important. The same paper [36] concludes the Granular film (CoZrO), NiZn ferrite (4FI), ferrite polymer material and thin film alloy (CoNiFe) are the four promising materials for high-frequency applications. Additionally to materials, [36] considers the integration technique. Three integration techniques are mentioned: board-level, wafer-level package-level integration.

To address the switch losses problem (when the switch turns on and off) resonant converters are used. This is explained in subsection 2.2.3. To overcome this problem some Zero Voltage Transfer and Zero Current Transfer techniques have been developed .

On the other hand when applying to high frequency devices, dc/dc converters are also found in electronic devices where there is a need for integration. The main area of a standard dc/dc converter is occupied by passive elements [37] (inductors and capacitors) and one way to reduce their footprint is to increase the switching frequency, leading to reducing the required values. Increasing the frequency will have a negative impact on

switching losses. Here we jump to talk about GaAs and CMOS technology but is also interesting to explore this area. In this paper [37] future work consist on validating the cascoded power stage on semiconductor shown in Figure 2.22 [37] , and then implement the full converter with this power stage using a multi-phase topology, (outside the scope of this thesis), with coupled inductors.

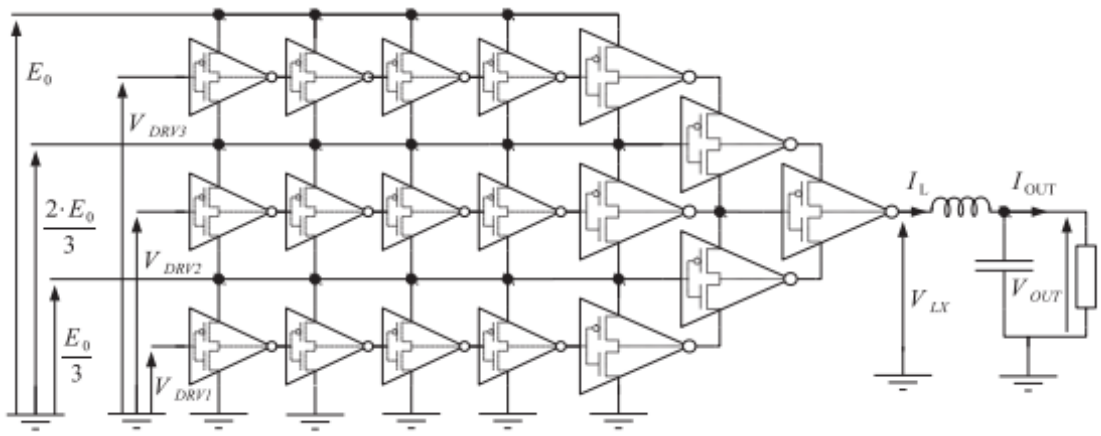

Figure 2.22: Cascoded power stage that work with dc/dc converters that work with GaAS and CMOS technology [37].

Other families of dc-dc converters are found as in Figure 2.23 [38]. A family of soft switching Pulse Width Modulation(PWM) DCDC converters employing a novel Zero Voltage and Zero Current Switching(ZVZCS) Active auxiliary Edge-Resonant Cell(AERC) is introduced [38].The six non-isolated DCDC converters introduced here, buck, boost, buck-boost, Ćuk, Sepic and Zeta work with AERC and can achieve a high frequency ZVS and ZCS operations in a main and an auxiliary switch with minimizing the voltage and current stresses as well as circulating currents. This family could be joined with the proposed family in this thesis.

In addition to the design of a robust, high efficiency or/and low cost converters, reliability should be also considered. This feature, regardless of the topology used, can be achieved introducing redundancy in the system so the uninterrupted operation of the circuit may be ensured when a fault has occurred [39]. The redundancy can be achieved by paralleling multiple converters or using a single modular circuit that can achieve this attribute [39]. A new pair of modular blocks and a new modular clamped dc-dc converter is introduced with redundancy [39] that has many potential uses for the automotive industry.

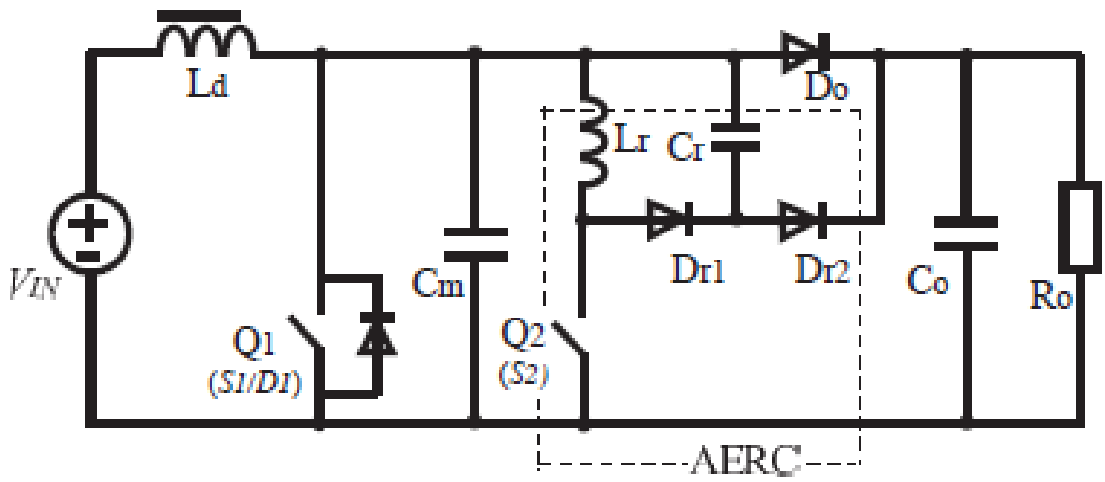

Figure 2.23: ZVZCS-PWM boost DCDC converter with Active auxiliary Edge-Resonant Cell(AERC), which belongs to a Family of DC-DC Converters with AERC [38].

2.4 Applications to PV/Battery/EV in Modern Distribution Power System

New Smart Grid (SG) technologies need to achieve a more intelligent, efficient, reliable and stable distribution system [40]. The components of a modern distribution system - photovoltaic (PV), battery energy storage system (BESS) and electric vehicle (EV) [40] or plug-in hybrid electric vehicles (PHEV) technologies need dc-dc converters.

A power grid is conventionally defined as an interconnected network with three subsystems: generation, transmission and distribution, where the power flow is one-way. Nowadays this has been changing by adding renewable energy sources as PV and wind turbines. This type network is known as distributed generation (DG). In addition, two-way flows of electricity and information are necessary to the created, automated and intelligent network [40]. The two-way next-generation grid of the future is known as SG [40]. This includes telecommunications and control technologies, information technology (IT) and power electronics circuit topologies. Here is where the proposed interleaved topology appears because dc-dc converters need to be ripple free (if possible) to inject less harmonics and disturbances into the system when converting from AC-DC or DC-AC. As we see the integration of DG units have the drawback to create a more complex network. The concept of micro grid (MG) ran into this paragraph as the low voltage network inside the distribution system that contains DG sources with local storage devices and controllable loads [41]. This MG can operate in island mode, with its own generators and loads,

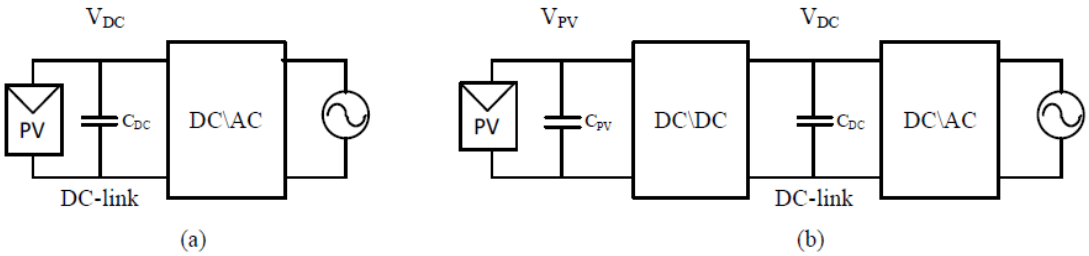

Figure 2.24: Block diagram of (a) single-stage inverter, (b)two-stage inverter [42].

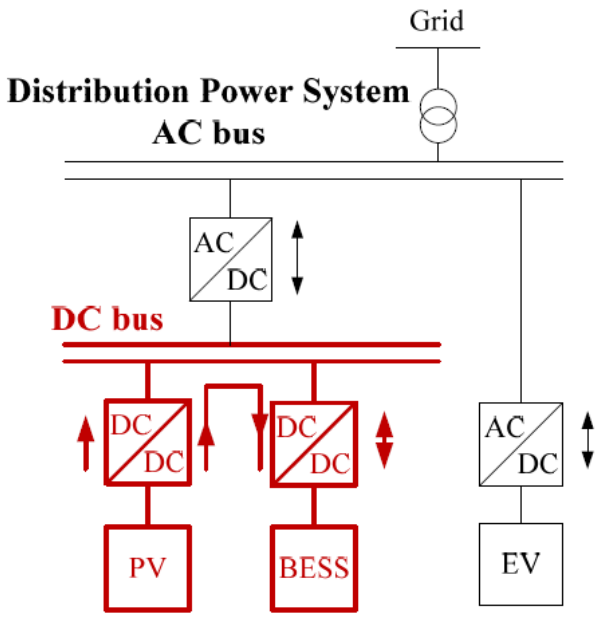

Figure 2.25: Overview of the power flow among the PV, BESS and DC bus [40].

or work in the grid-connected mode as a small power source with ancillary services to support the main grid [40]. Therefore future work would be control and monitoring of the key components of MGs -PV, BESS and EV- where the dc-dc converters are present.

DC-DC converters can be connected to the dc bus to feed a PV as in Figure 2.24 [42] on page 24 or a BESS [40] as shown in Figure 2.25 [42].

The operation of PV sources becomes more challenging because of Maximum Power Point Tracking (MPPT[7]) operations, shading conditions and PV system polarity issues

[7]There are many algorithms for MPPT [43] [44]. The peak point needed is called Maximum Power Point (MPP) and is affected by weather conditions [42] . This occurs at a certain voltage V_{mpp} and current I_{mpp} where the power output of a PV delivers maximum power. The PV inverter extracts the max. amount of power from PV generator and converts the power in an appropriate form for feeding into the grid [42]

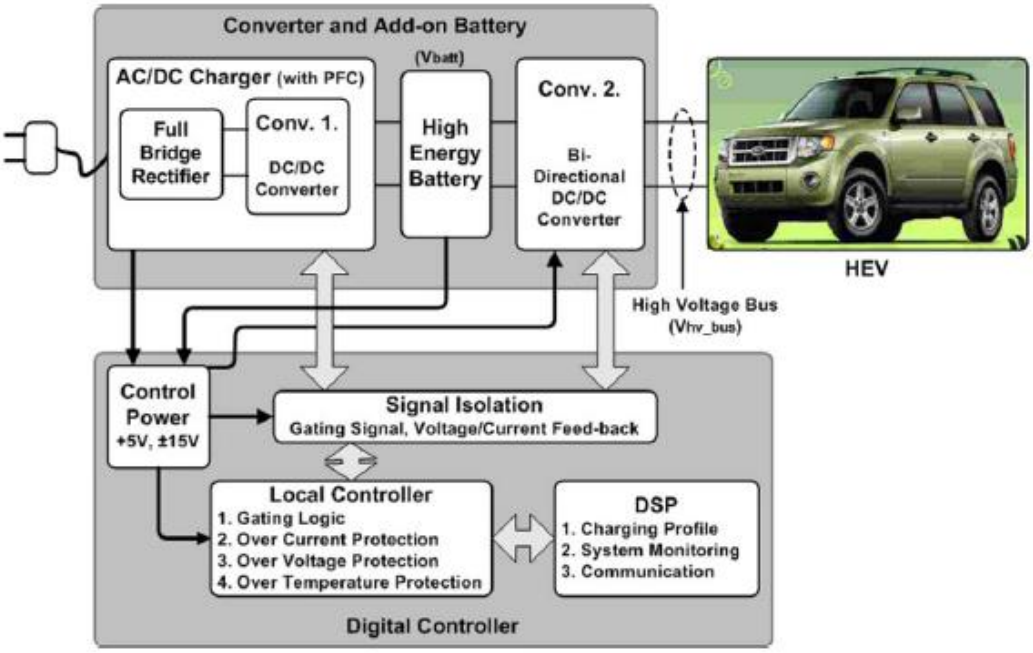

Figure 2.26: Overall configuration of the PHEV [45].

[40]. The classic four-switch buck-boost converter has proved to be the best solution for PV buck-boost applications until now [40]. It can work buck, boost, or buck-boost modes depending of input and output voltages [40]. In any cycle, each of four switches turns on and off precisely on in each cycle, which increases the control complexity, and driver circuits are also costly [40].

Some examples of EV are found: The bidirectional dc-dc converter with a power charging-discharging profile is required to transfer energy between the battery and the electric traction system [45]. The main elements for the conversion comprise an ac/dc charger, high-energy battery added to the HEV, a bidirectional dc-dc converter, and a digital controller with digital signal processing (DSP) [45]. From Figure 2.26 [45] the main elements are in cascade [45], except the digital controller. The plug-in charger is composed of two parts: 1) ac/dc rectifier and 2)dc-dc converter (Conv. 1).

A bidirectional buck-boost dc-dc converter with a storage battery is shown in Figure 2.27 [46] and the whole system with this converter integrated is shown in Figure 2.28 [46]. This topology is more complex than the proposed dual converter, with more elements to dissipate energy.

Some other sources could feed the DG like Thermoelectric Generators (TEG). A high step-up dc-dc converter for TEG based topologies by using the coupled inductor and voltage multiplier is shown in Figure 2.29 [47]. The converter is boosting from 4.2 to

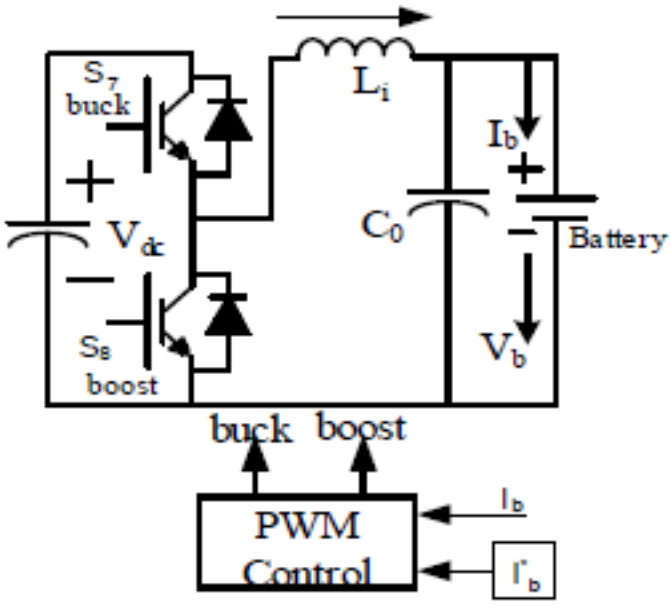

Figure 2.27: Bidirectional buck-boost dc-dc converter [46].

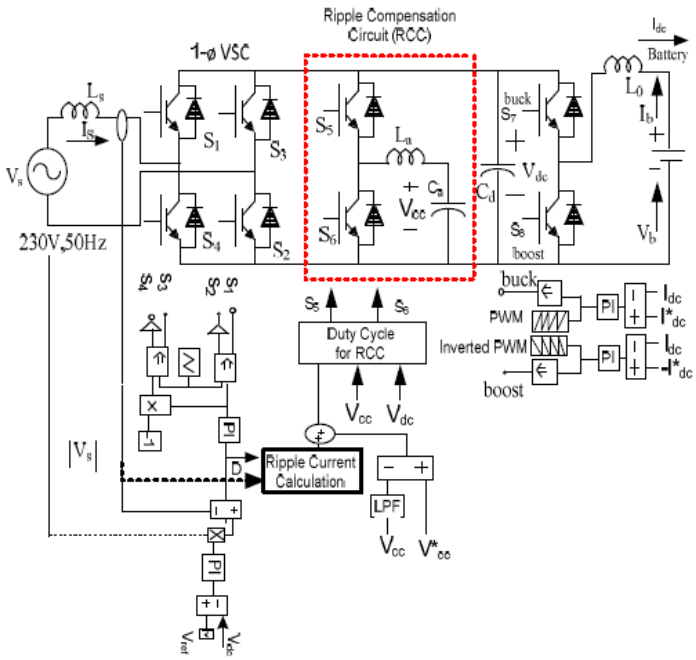

Figure 2.28: Single phase full-bridge bidirectional power converter with an auxiliary circuit for dc ripple compensation and small dc link capacitor with a bidirectional dc-dc converter [46].

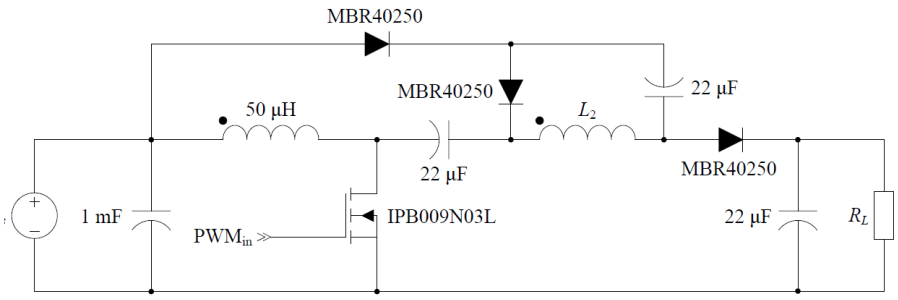

Figure 2.29: Schematic of high step-up dc-dc converter for TEG [47].

180V [47] with efficiency of 90.7%. Maximum Power Point Tracking (MPPT) algorithms are analysed to control the TEG concluding the fractional open-circuit voltage / short-circuit current methods are the best steady state MPPT performance for use with a TEG [47].

The term Combined Heat and Power (CHP) refers to the simultaneous production of electrical (or mechanical) and thermal energy, both intended as useful products, from a single primary energy source [48]. CHP systems can be connected to the DG and could need dc-dc converters if the prime mover[8] or source is a fuel cell. Usually CHP systems are more efficient that a conventional power generation systems. As a variant to CHP, trigeneration systems are formed by adding an absorption chiller to combined heat and power systems to convert some of the recovered heat into required cooling loads. Therefore trigeneration systems are also know as CCHP or combined cooling, heat and power.

2.5 Summary

This chapter summarised existing dc/dc converter topologies based on their converter structures and usage. It is shown that they are being applied in many different areas, from high power distribution system, to transportation, to integrated circuits. Apart from high voltage gain capability, other related design issues have been discussed such as efficiency, component count, isolation and reliability. Although many topologies have been reported, there is no single topology that can fulfil all the design criteria. In other words, there is no unique topology that can apply to all applications. In the following chapters, a new switching converter structure will be introduced. It offers high gain, high efficiency, reduced ripple currents and improved reliability.

[8]The prime mover is the main part of system which utilizes fuel to generate electricity. Prime movers can be reciprocating engines, Stirling engines, gas turbines, steam turbines, microturbines [48].

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Chapter 3

A New Family of High Step-up DC-DC Converters

3.1 General Block and Formulation Process

Based on the literature review in Chapter 2 which shows several important criteria of high quality power conversion for step-up voltage applications, namely, low input and output ripples, low transformer leakage related loss, and less power processing, in this chapter, a new family of DC/DC converters is proposed, as shown in Figure 3.1 on page 34. The proposed converter family inherits basically a parallel-input series-output structure and hence it has three major features as follows:

- They are able to produce higher step-up voltages than conventional boost converters and other transformerless topologies.
- The two converters can operate in an interleaved manner to reduce input and output current ripple, thus reducing the filtering requirement.
- The output is formed by two capacitors connected in series as well as the input voltage, as illustrated in Figure 3.1 on page 34 and (3.1) on page 34. In other words, some input power will transfer to output without any processing, or so-called direct power transfer. Therefore the conversion efficiency is higher than that of conventional cascaded configuration.
- When one of the converters stop operation, the converter structure is still able to perform limited voltage conversion with lesser conversion ratio. This improves the reliability of the power supply.

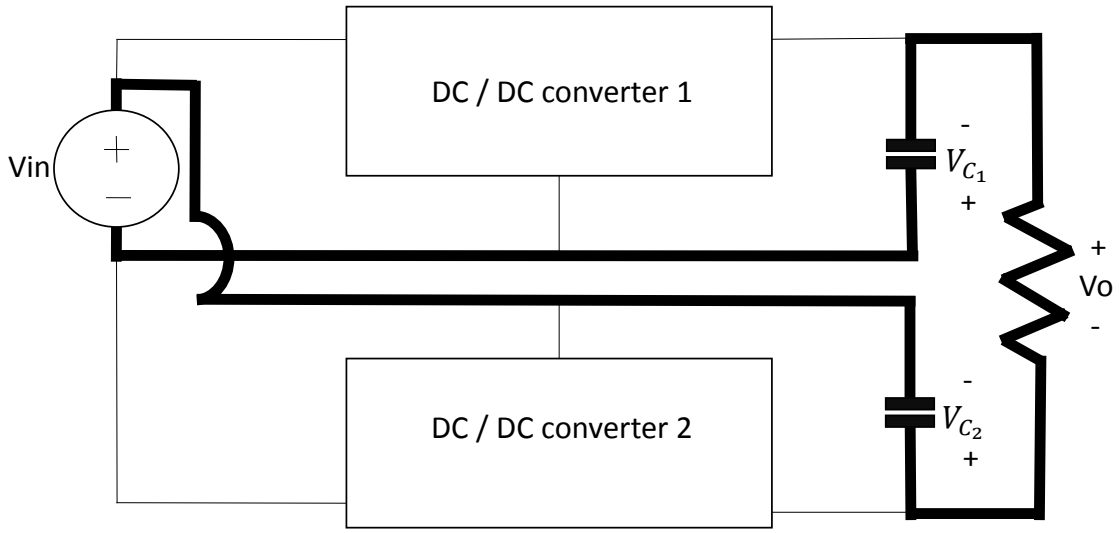

Figure 3.1: General structure of the proposed new high step-up converter structure.

$$V_o = -V_{in} - V_{c_1} - V_{c_2} \tag{3.1}$$

Note that the output voltage has an opposite polarity to that of the input voltage to realize direct power transfer. It is practically implemented through converter topologies with an inverting output. The voltage polarities of both input and output can be the same by using non-inverting topologies which will be shown in later section.

3.2 Dual Buck-Boost Converter Topology Example

The basic topology to realize an inverting output is a buck-boost converter. Two buck-boost dc/dc converters are parallel connected in the input and series connected in the output as shown in Figure 3.2 on page 35.

3.3 Steady-state Analysis

3.3.1 Voltage Conversion Ratio in Continuous Conduction Mode (CCM)

The continuous conduction mode occurs when current in the inductor rise and fall in the time period without arriving to zero current. For the interleaved buck-boost converter two duty cycles exist. One for the upper dc/dc nnd one for the lower dc/dc converter. In the simplest case these duty cycles are equal, therefore the following is found when

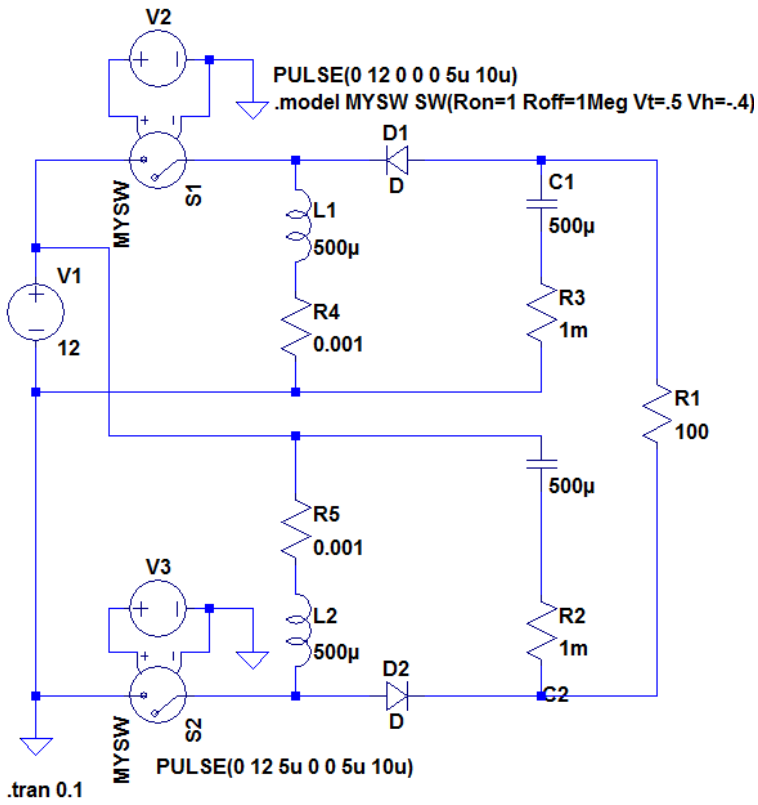

Figure 3.2: Dual buck-boost converter topology for the proposed input-parallel output-series structure

.

the voltage loop, which consists of the output voltage V_o, input voltage V_{in}, and the capacitors C_1 and C_2, is followed.

From each stage, that is a buck-boost converter:

$$V_{c_1} = \frac{D}{1-D} V_{in} \tag{3.2}$$

$$V_{c_2} = \frac{D}{1-D} V_{in} \tag{3.3}$$

Inserting (3.2) and (3.3) into (3.1)

$$-V_{in}(1 + \frac{2D}{1-D}) = V_o \tag{3.4}$$

where the following assumption is made:

$$V_{c_1} = V_{c_2} = V_c \tag{3.5}$$

Hence the voltage conversion ratio of buck-boost topology is given by

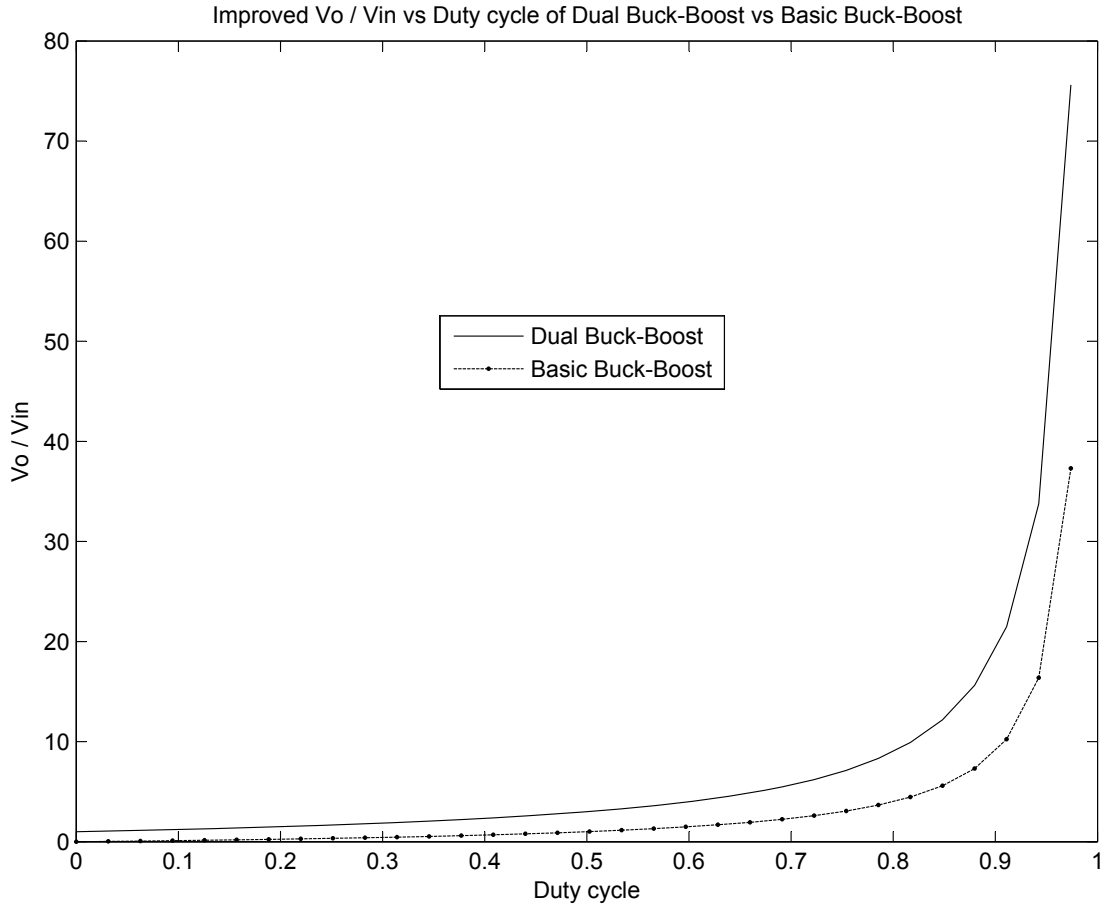

Figure 3.3: $\frac{V_o}{V_{in}}$ vs Duty cycle (CCM). The $\frac{V_o}{V_{in}}$ for the basic buck-boost converter is the dotted line and the $\frac{V_o}{V_{in}}$ for the proposed dual buck-boost is the black line corresponding to equation (3.6). This shows the improvement of stepping up the voltage better than conventional buck-boost converter.

$$\frac{V_o}{V_{in}} = -\frac{1+D}{1-D} \tag{3.6}$$

Figure 3.3 on page 36 shows the plot of voltage conversion ratios of the proposed dual buck-boost converter and basic buck-boost converter operating in CCM. It shows that the proposed converter has a higher gain.

3.3.2 Simulated Waveforms

The simulated waveforms are shown in Figures 3.4 on page 37 and 3.5 on page 38. In Figure 3.4 on page 37 waveforms of different currents in the converter are shown.

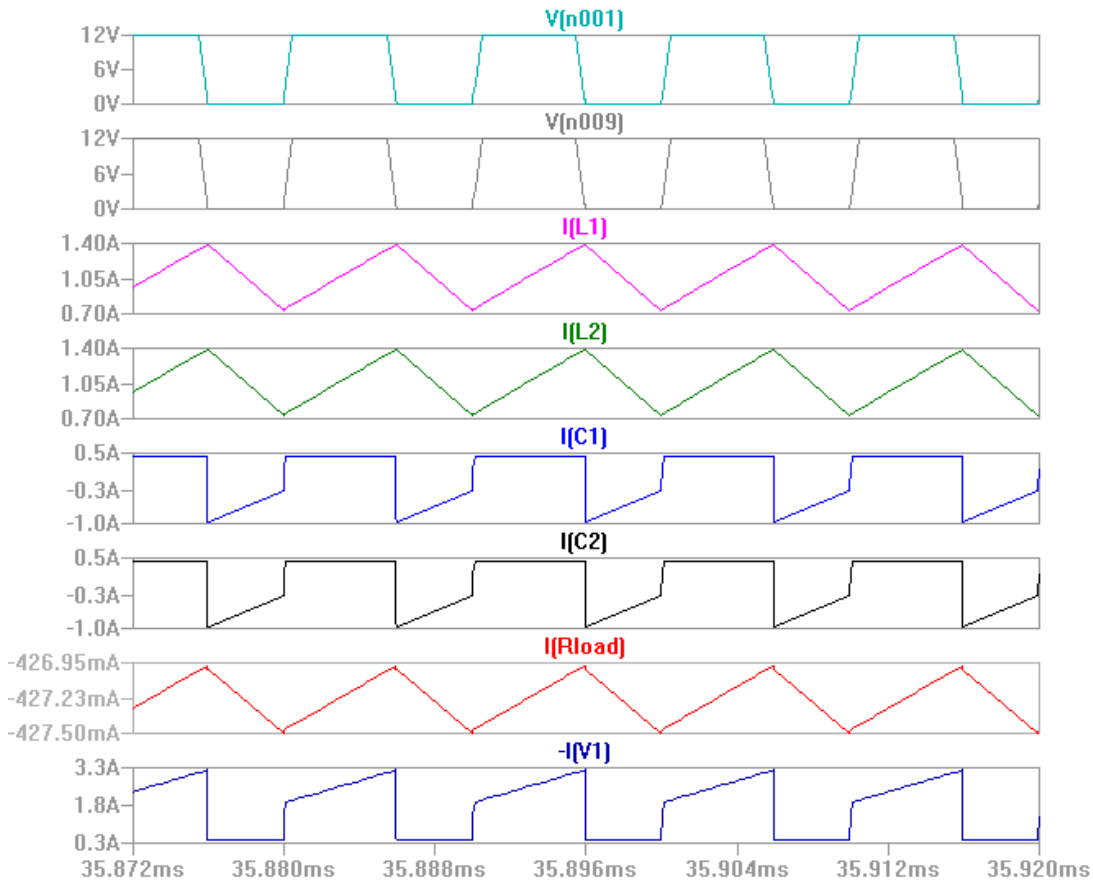

Figure 3.4: From top to bottom: V(n001) = PWM pulses for upper converter; V(n009) = PWM pulses for lower converter; I(L1) = inductor current of L1, I(L2)= inductor current of L2, I(C1)= capacitor current of C1, I(C2)= capacitor current of C2, I(Rload)= load current, -I(V1)= input current, which is the addition of I(L1)+ I(L2)+ I(Rload). Note that currents I_{C_1} and I_{C_2} are equal and are in series with $I_{R_{load}}$ during ON-state of the switches.

3.3.3 Voltage Conversion Ratio at Discontinuous Conduction Mode (DCM)

In discontinuous conduction mode the inductor currents reaches zero before the next cycle begins as shown in Figure 3.6 on page 39. Delta, Δ, shown in Figure 3.6, is the time from t_{on} until the inductor current reaches zero.

From (3.1) the input is connected to the output through the capacitors.

If the capacitor voltages are related to the input:

$$V_{c_1} = \frac{D}{\Delta} V_{in} \tag{3.7}$$

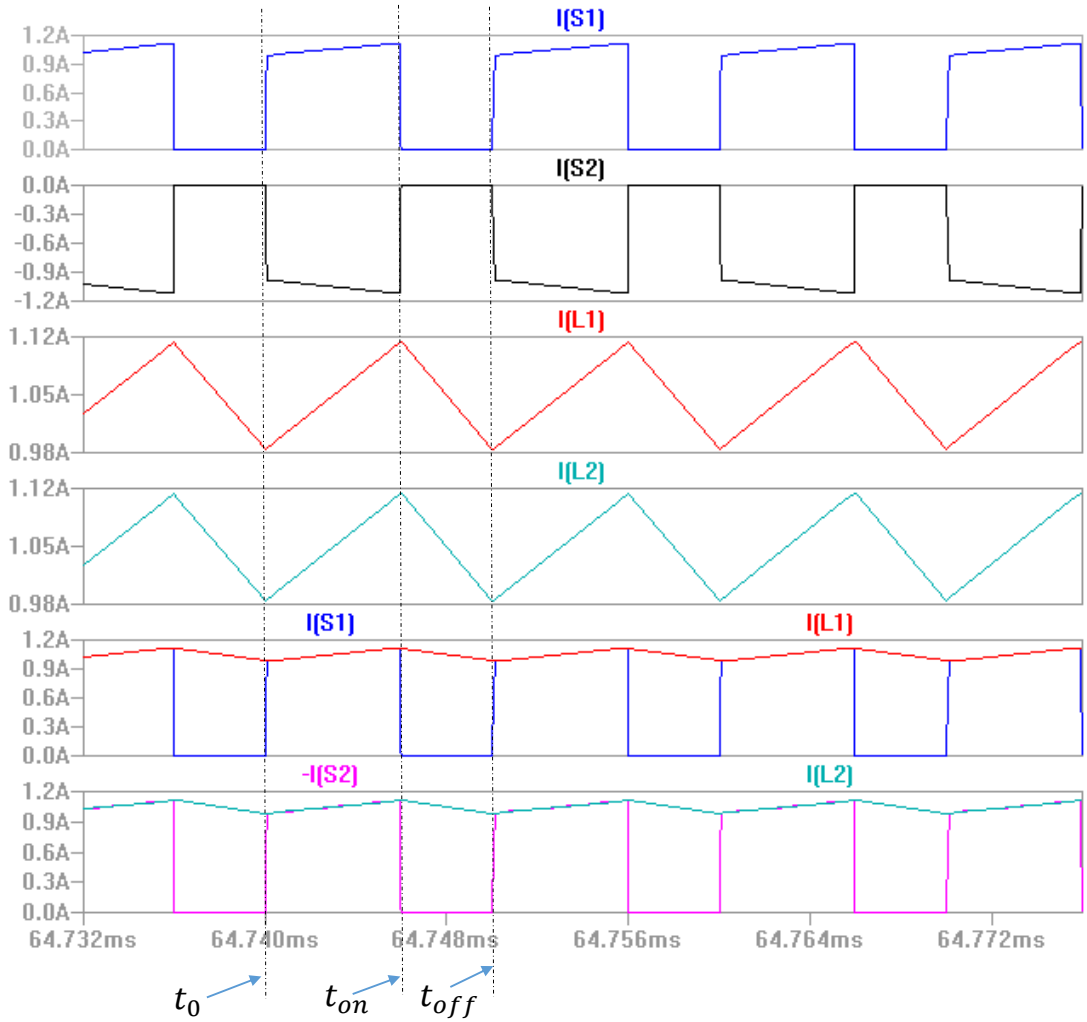

Figure 3.5: Four panes on top: Switch 1, Switch 2, Inductor 1 and Inductor 2 currents are shown independently. On the bottom: The Switch 1 with Inductor 1, and Switch 2 with Inductor 2 are shown. Notice the switch and inductor currents have the same value during t_{on} iy. During t_{off} the Switch currents are zero.

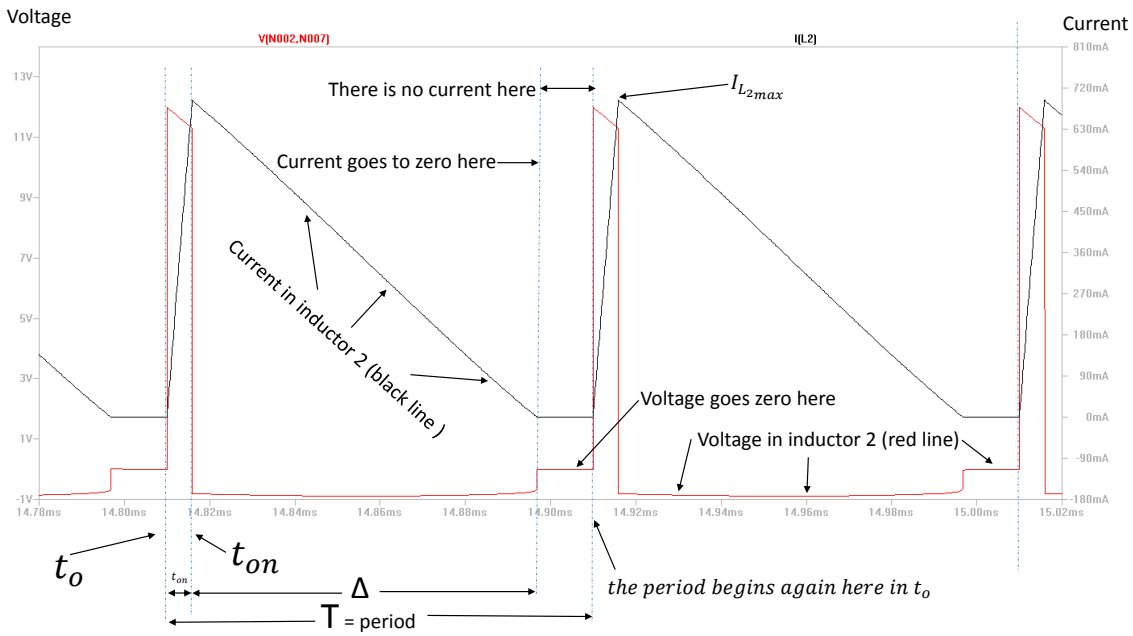

Figure 3.6: Current and voltage in inductor 2 in DCM. Delta is the time from the current's top $I_{L_{2max}}$ until this falls to zero.

$$V_{c_2} = \frac{D}{\Delta} V_{in} \tag{3.8}$$

Inserting (3.7) and (3.8) into (3.1)

$$-V_{in} - \frac{D}{\Delta} V_{in} - \frac{D}{\Delta} V_{in} = V_o \tag{3.9}$$

$$-V_{in} - 2\frac{D}{\Delta} V_{in} = V_o \tag{3.10}$$

Factorizing:

$$V_{in}(-1 - 2\frac{D}{\Delta}) = V_o \tag{3.11}$$

$$\frac{V_o}{V_{in}} = -1 - \frac{2D}{\Delta} \tag{3.12}$$

Figure 3.7 on page 40 shows the plot of voltage conversion ratios of the proposed dual buck-boost converter and basic buck-boost converter operating in DCM. It shows that the proposed converter has a higher gain than basic buck-boost converter and also higher than the proposed dual buck-boost converter in CCM as shown in Fig. 3.3 on page 36

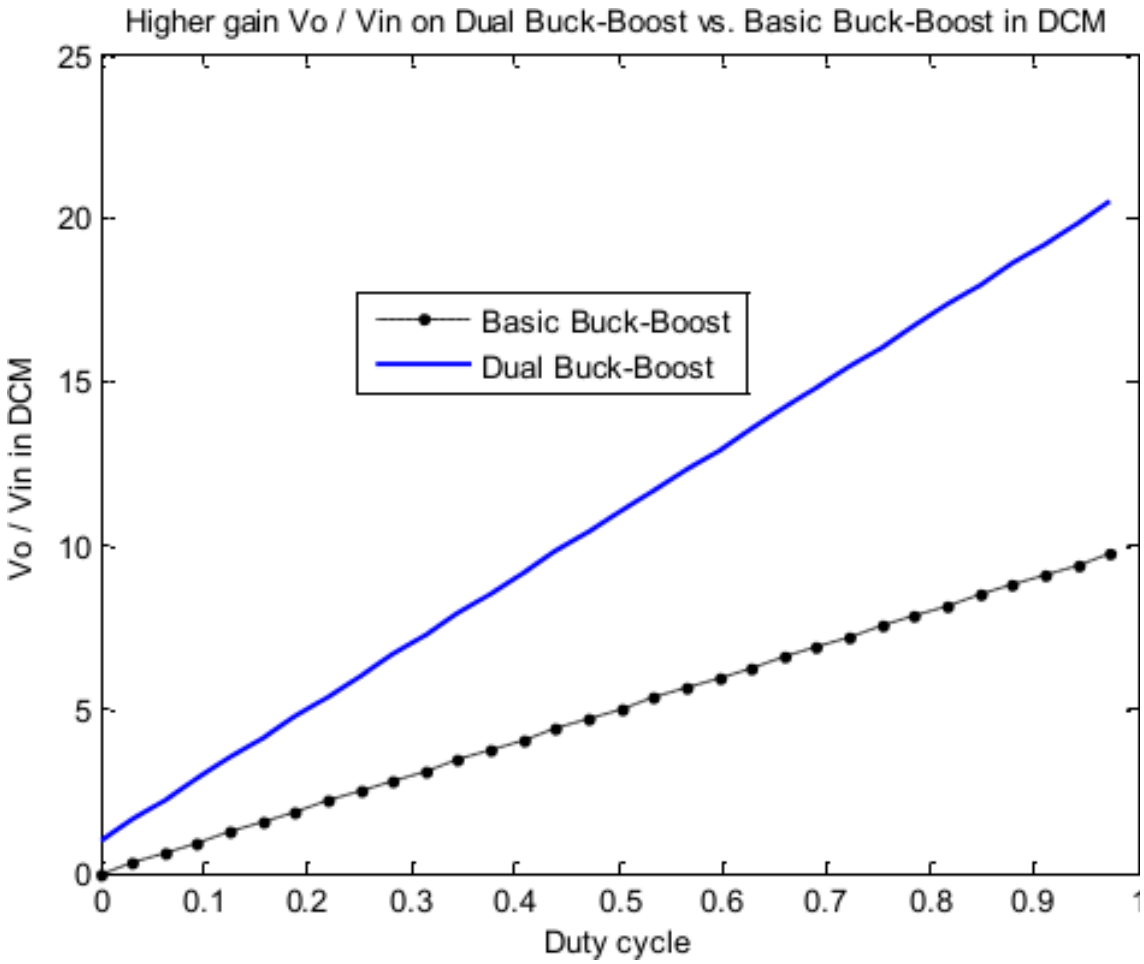

Figure 3.7: $\frac{V_o}{V_{in}}$ vs Duty cycle (DCM). The $\frac{V_o}{V_{in}}$ for the basic buck-boost converter is the dotted line and the $\frac{V_o}{V_{in}}$ for the proposed dual buck-boost is the black line corresponding to equation (3.12). This shows the improvement of stepping up the voltage better than conventional buck-boost converter.

3.3.4 Voltage Stresses on Devices

The maximum peak value of the voltage across each switch is

$$V_{S_{max}} = V_{in_{max}} + V_{c_1} \tag{3.13}$$

and the maximum peak value of the current through each switch is

$$I_{max_{Mosfet_1}} = I_{max_{L_1}} \tag{3.14}$$

$$I_{max_{Mosfet_2}} = I_{max_{L_2}} \tag{3.15}$$

3.4 Theoretical Waveforms Analysis

This section mainly considers the input and output current ripples of the proposed converter. Two scenarios are shown in Figs. 3.8 and 3.11 which display no phase-shift (Fig. 3.8) and 180 degrees phase-shift (Fig. 3.11) between the two duty cycles respectively.

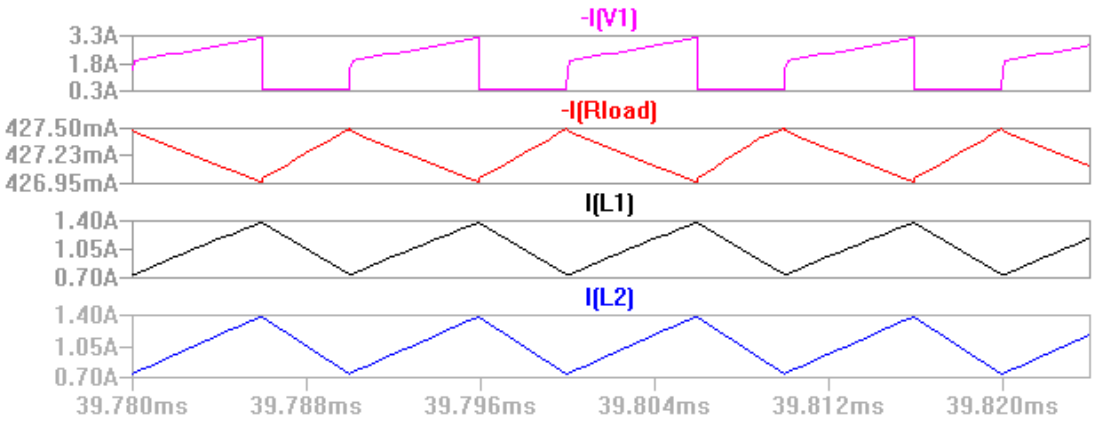

Figure 3.8: Case 1: No phase-shifting. The interleaved buck-boost with no phase-shifting is shown. When compared with Figure 3.11 the input and output currents have more ripple. The absolute value of peak-to-peak input current, $\mid I_{in_{p-p}} \mid$, = absolute value of peak-to-peak I(V1) = 3A. The absolute value of peak-to-peak output current , $\mid I_{o_{p-p}} \mid$ = absolute value of peak-to-peak I(Rload) = 50mA.

On Figure 3.9 on page 42 the dc/dc converter had a fault on the lower stage. Even though the inductor 2, diode 2 and MOSFET 2 are open-circuited and disconnected from rest of the converter circuit, the output voltage drops but doesn't arrive to zero. Note that this scenario is possible by having a fuse installed in series with each MOSFET. When a short-circuit fault occurs, the fuse will blow and isolate the converter from the input, i.e. no input current can flow into that converter part. The other converter continues operation to provide limited voltage conversion. Of course if both fuses are blown, the entire converter will stop operation. Nevertheless the proposed converter structure offers improved reliability over conventional basic or single-stage converter topology.

Figure 3.12 on page 44 shows the results of more variations of duty cycles and different degrees of phase-shift. The y-axis is the maximum input current over average input current and the x-axis is the delay between the two duty cycles. Three duty cycle values are considered, namely, 0.2, 0.5 and 0.8. It is interesting to observe that the ripple current reaches minimum when the phase-shift between the two duty cycles are close to 180 degrees.

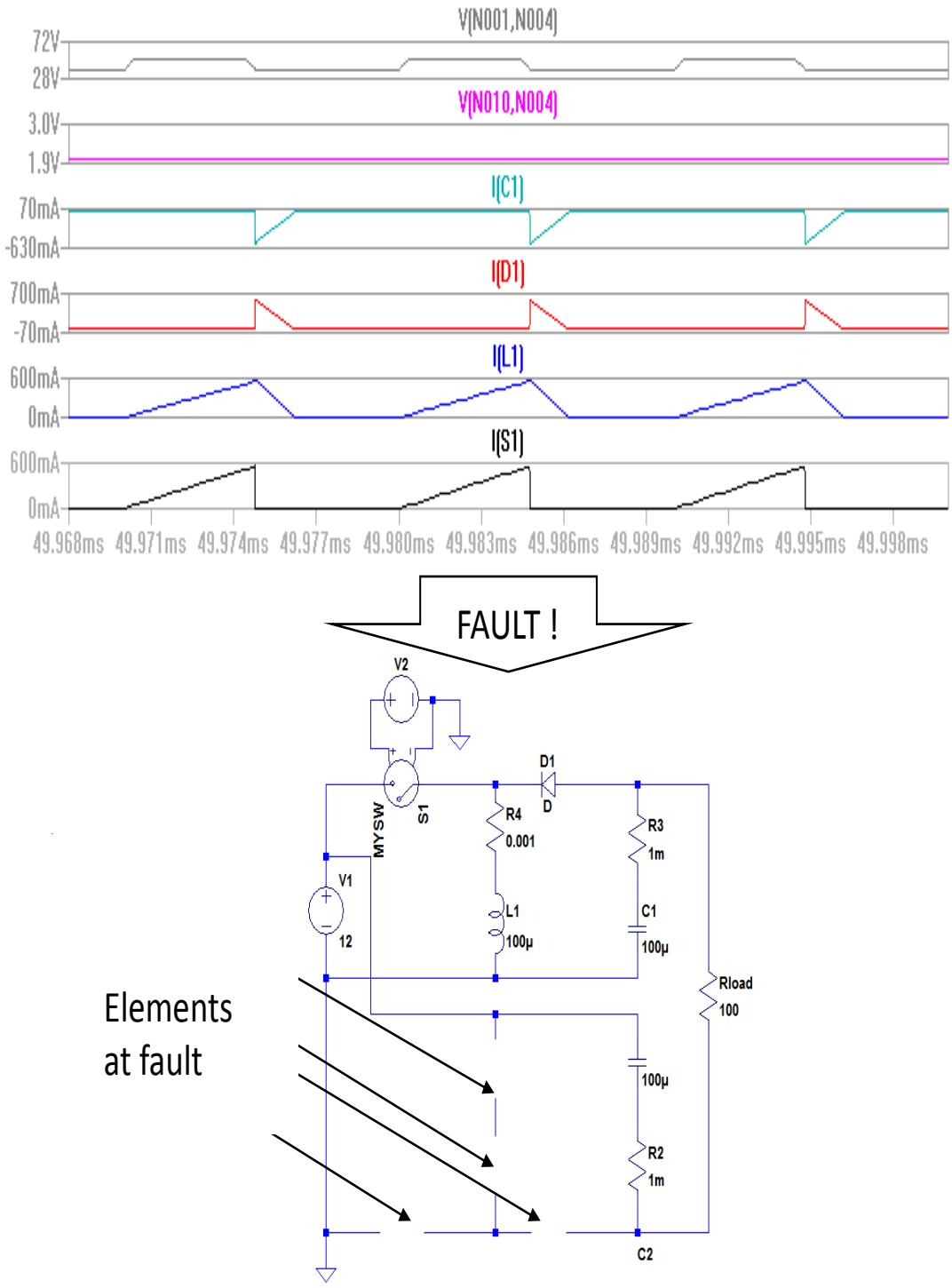

Figure 3.9: Fault case: When dc/dc converter 2 stops operation, dc/dc converter 1 is still on and the output voltage drops without achieving zero. Even though the lower stage is faulty the dual converter is working. This shows the proposed converter structure has good reliability.

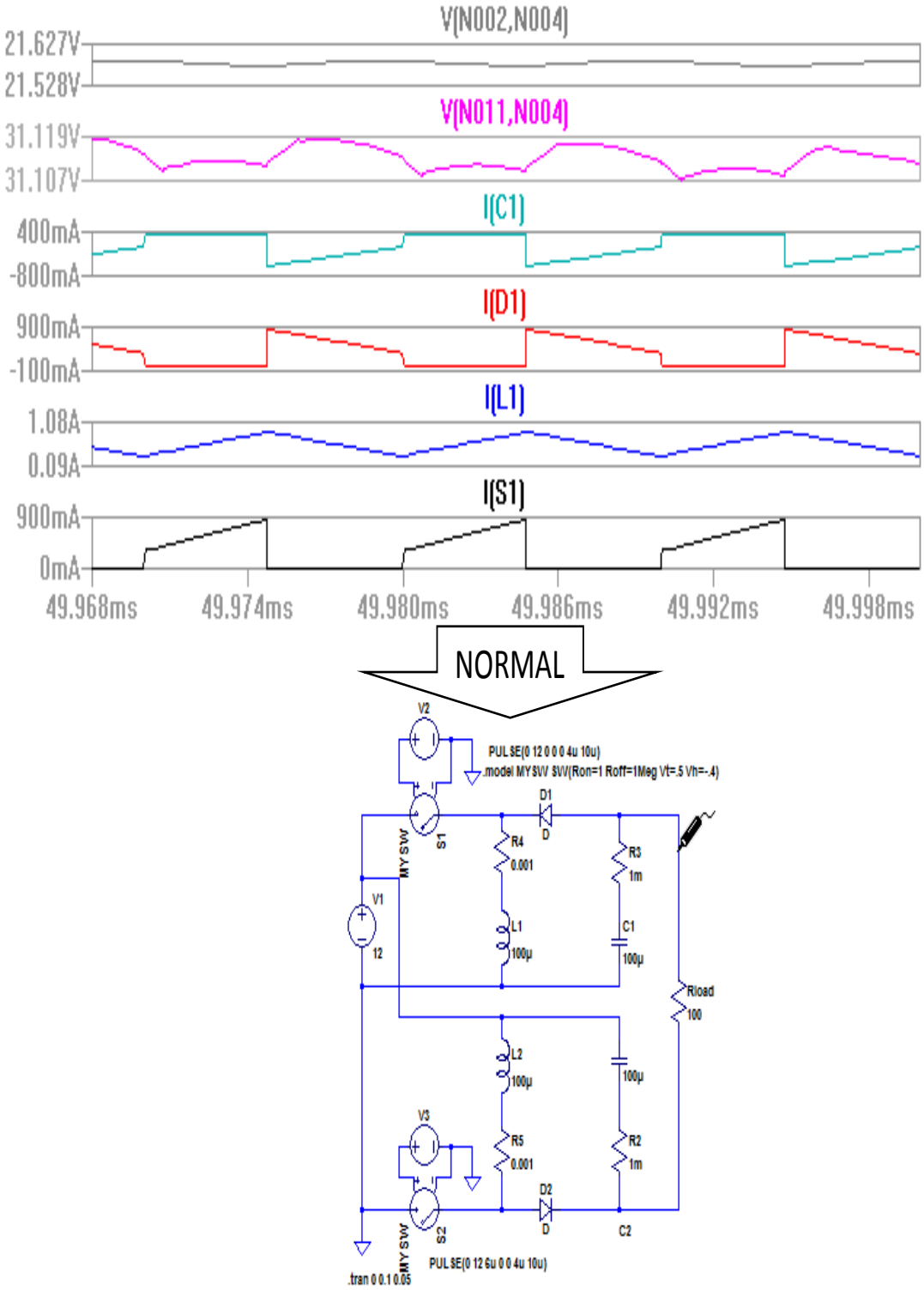

Figure 3.10: Normal operation of the proposed topology. If the output voltage,(V_o = V[N010,N004], floating) is compared with Figure 3.9 on page 42 the voltage drops in Figure 3.9 but doesn't drop to zero for this kind of fault. This shows the proposed converter structure has good reliability.

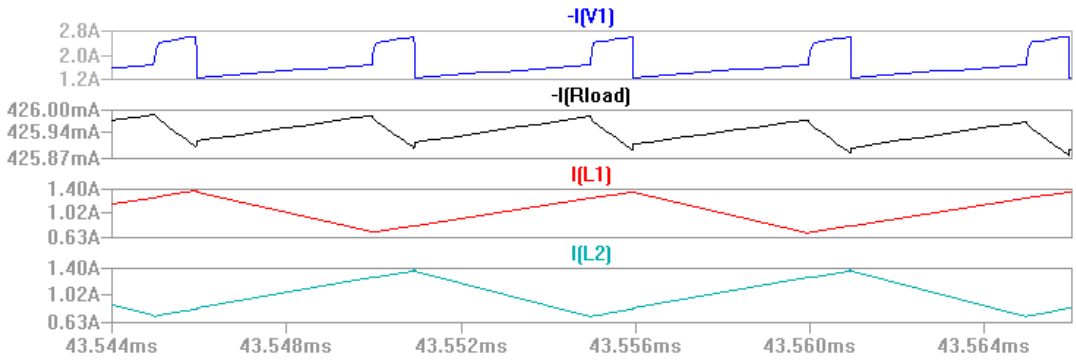

Figure 3.11: Case 2: Phase shifting. The Interleaved buck-boost has 180 degrees phase shifting and its effect on I_{in} and $I_{R_{load}}$ is stronger when compared with no-phase shifting as shown in Figure 3.8. The absolute value of peak-to-peak input current, $\mid I_{in_{p-p}} \mid =$ absolute value of peak-to-peak I(V1)= 1.5A. If compared to 3A of Figure 3.8 the ripple's reduction is two times: $\frac{3}{1.5} = 2$. The absolute value of peak-to-peak output current, $\mid I_{o_{p-p}} \mid$, = absolute value of peak-to-peak I(Rload) = 1.13mA, if compared to 50mA of Figure 3.8, the reduction is $\frac{50}{1.13} = 44.2$ times.

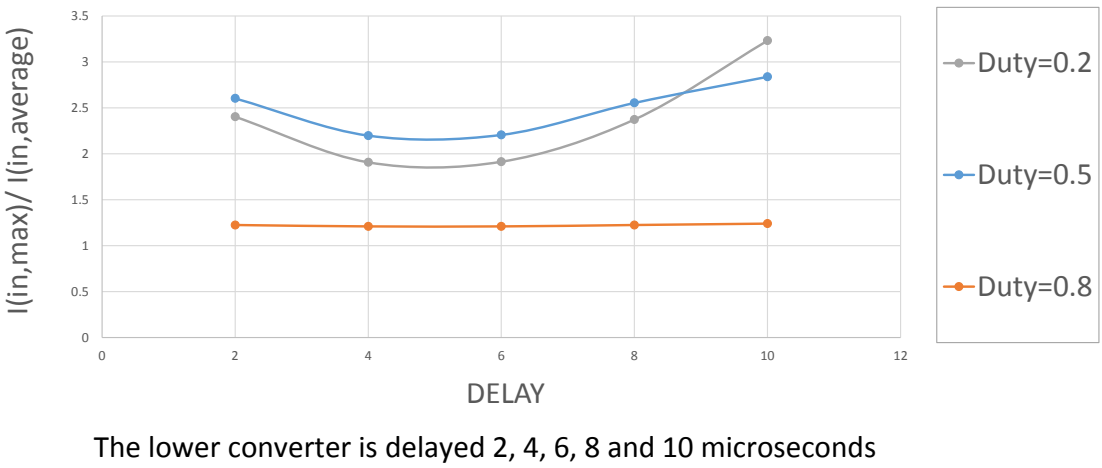

Figure 3.12: Maximum Input Current over Average Input Current vs. Delays in Lower Converter under different duty cycle values of both switches. Identical duty cycle for each converter is used.

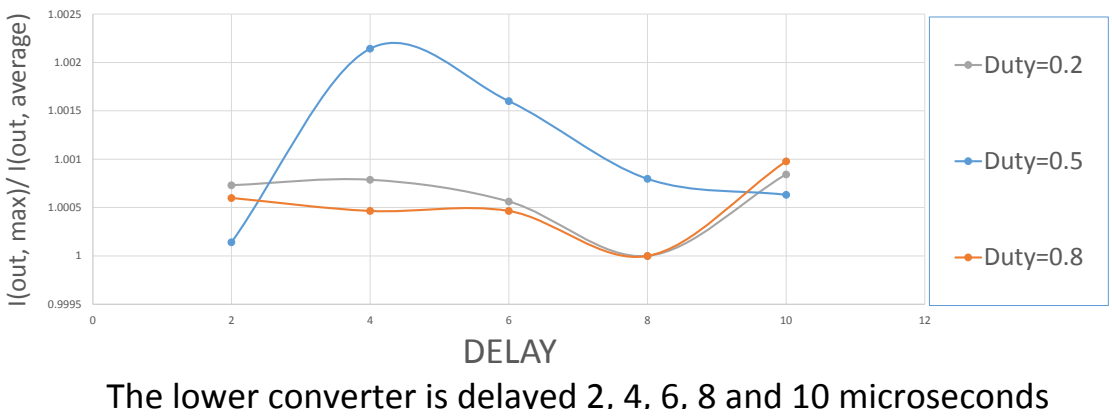

Figure 3.13: Maximum Output Current over Average-Output Current vs. Delays in Lower Converter under different duty cycle values of both switches. Identical duty cycle for each converter is used.

Figure 3.13 on page 45 shows the results of more variations of duty cycles and different degrees of phase-shift. The y-axis is the maximum output-current over average-output current and the x-axis is the delay between the two duty cycles. Three duty cycles are considered, namely, 0.2, 0.5 and 0.8. It can been observed that at higher duty ratio the output ripple is lower. From the these two figures, it can be concluded that the higher the duty ratio is, the lower the current ripple.

3.5 Other Converter Topologies of Proposed Interleaved Family

The proposed converter structure provides a generalized configuration for different types of converter topologies to be configured, designed and analyzed. A dual-boost converter is reported in [1]. Two topologies are discussed [1], one topology interleaves and cascades boost converters as shown in Figure 3.1 on page 35 and the other in Figure 3.14 on page 46 uses four interleaved boost converters. The benefits of interleaving like the reduction of input and output current ripples and increase in output voltage are presented in [1]. In contrast to Figure 3.14 [1] the use of inverting converter topologies for the converter structure has a higher voltage conversion ratio due to the fact that the output voltage is the addition of input voltage to the two output capacitors voltages, as shown in (3.1). If non-inverting topologies are used, the output voltage is a subtraction of input voltage from the two capacitors voltages, similar to the boost converter case in Figure 3.14. There are more converter topologies such as Ćuk, Flyback, Forward, SEPIC and Zeta which

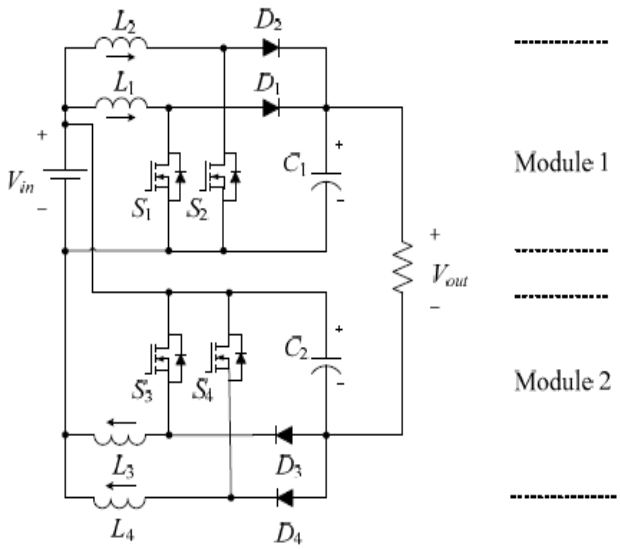

Figure 3.14: Four interleaved boost converters [1]

can also be applied to the parallel-input series-output structure as described in Fig.3.1 on page 35. Some of these new topologies are shown as follows:

- Dual-Ćuk in Figure 3.15 on page 47.
- Dual-Flyback in Figure 3.16 on page 47.
- Dual-Forward in Figure 3.17 on page 48.
- Dual-SEPIC in Figure 3.18 on page 49.
- Dual-Zeta in Figure 3.19 on page 49.

The previous list is not exhaustive and can be broaden by mixing the basic topologies and/or adding others, on converter 1 and converter 2. For example:

- By mixing the Ćuk on converter 1 and Zeta on converter 2 a new interleaved Ćuk-Zeta converter is found.

In general if n is the number of basic topologies, a number of $n + (n-1) + (n-2) + (n-n+1) = \frac{n(n+1)}{2}$ is the number of possibilities found.[1]

[1]Numbers of this form are called triangular numbers because they can be arranged in a triangle.

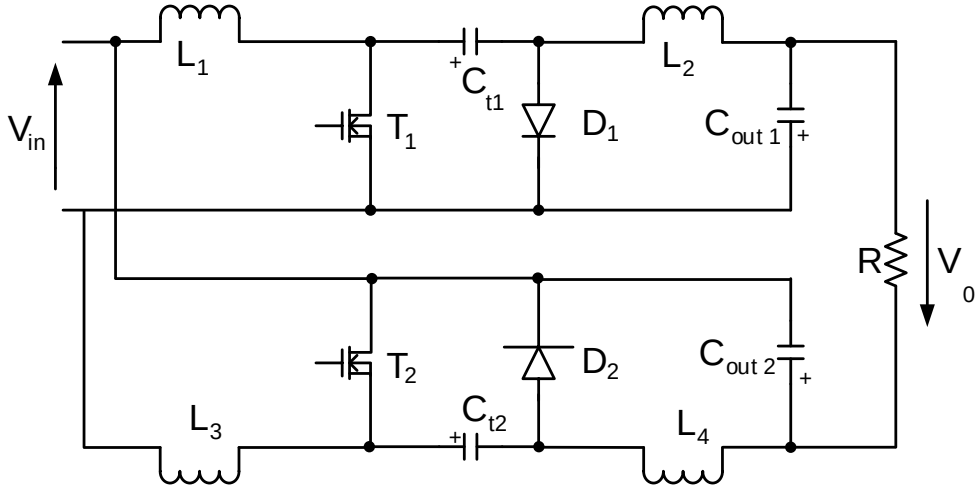

Figure 3.15: Dual Ćuk converter

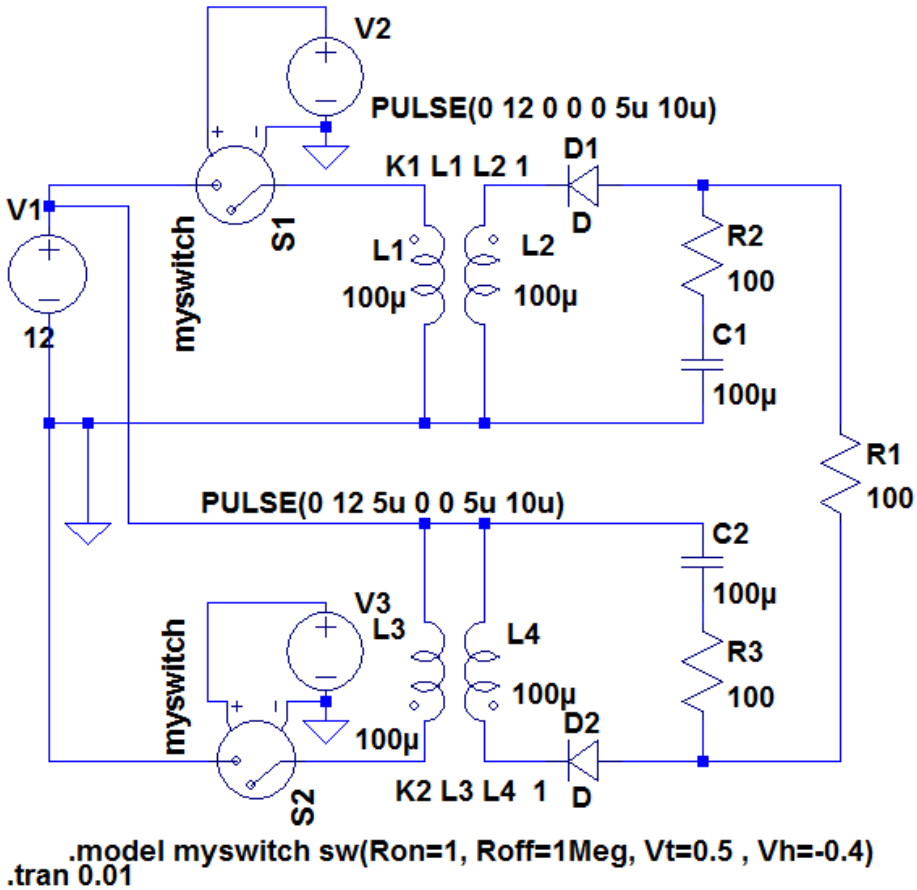

Figure 3.16: Dual Flyback converter

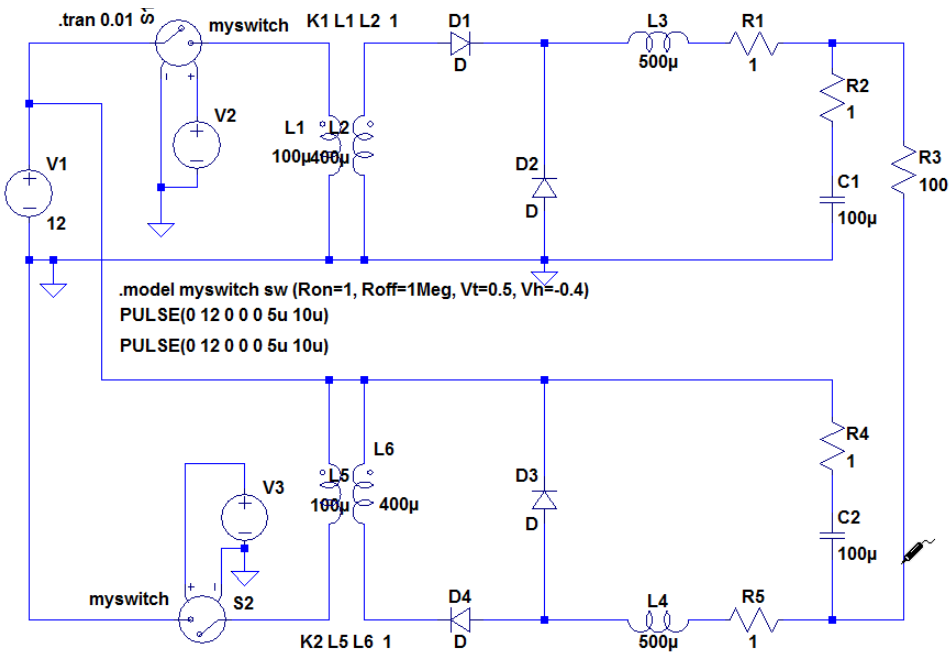

Figure 3.17: Dual Forward converter

Interleaved Topology	$\frac{V_o}{V_{in}}$ in CCM	$\frac{V_o}{V_{in}}$ in DCM	Output polarity
buck-boost	$\frac{1+D}{1-D}$	$\frac{1+2D+\Delta}{1-\Delta}$	opposite to V_{in}
Ćuk	$\frac{1+D}{1-D}$	$\frac{1+2D+\Delta}{1-\Delta}$	opposite to V_{in}
Sepic	$\frac{1+D}{1-D}$	$\frac{1+2D+\Delta}{1-\Delta}$	same as V_{in}
Zeta	$\frac{1+D}{1-D}$	$\frac{1+2D+\Delta}{1-\Delta}$	same as V_{in}

Table 3.1: Summary of line to output or $\frac{V_o}{V_{in}}$ in CCM and DCM for the New Interleaved Family

Bibliography

[1] D. Coutellier, V. G. Agelidis, and S. Choi, "Experimental verification of floating-output interleaved-input dc-dc high-gain transformer-less converter topologies," Rhodes, Greece, 2008, pp. 562 – 568. [Online]. Available: http://dx.doi.org/10.1109/PESC.2008.4591989

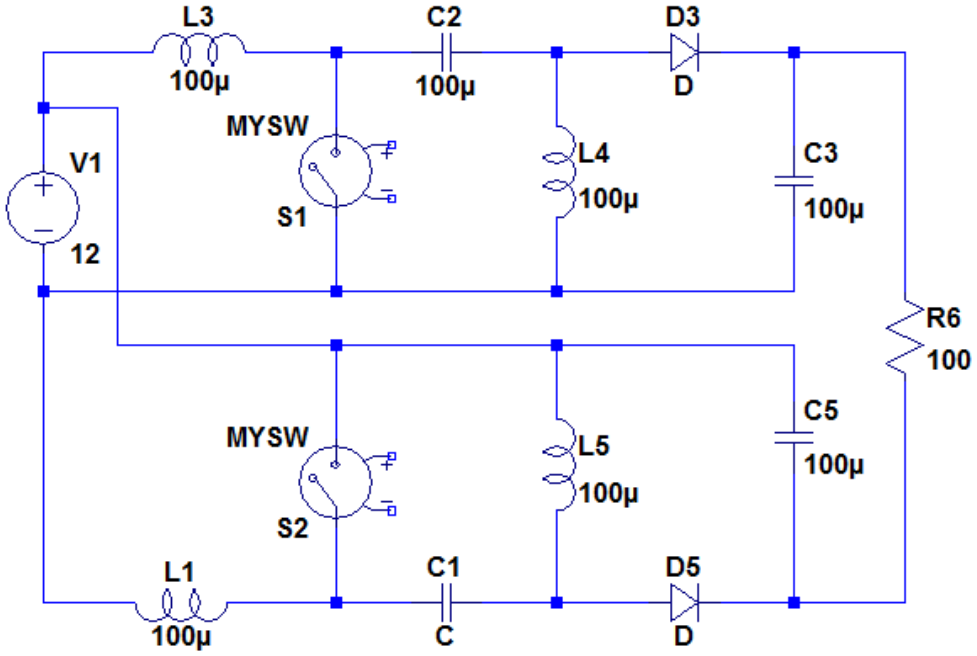

Figure 3.18: Dual SEPIC converter

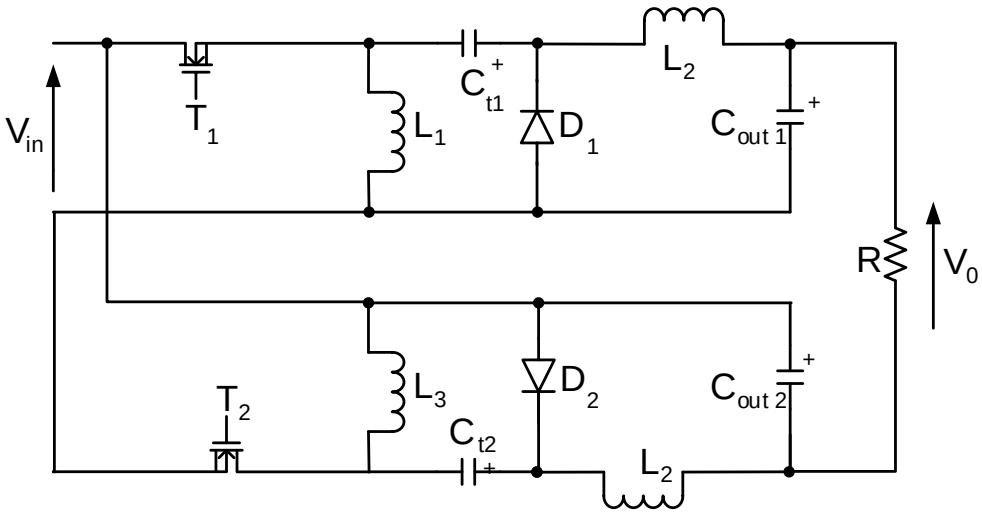

Figure 3.19: Dual Zeta converter

Chapter 4

Small-Signal Analysis of High Step-Up DC/DC Converters

These interleaved dc-dc converters are non linear because they contain at least two transistors and two diodes that are operated as switches and could require control circuits to regulate the output voltage against load and line variations [1]. Linear control theory is well developed and can describe the dynamic performance of these PWM converters. In order to apply this theory , they need to be averaged and linearised [1]. There are some average methods for PWM converters like the minimum separable switching configuration (MISSCO), the state-space averaging method, the circuit averaging method and the fast analytical method.

4.1 Example with Interleaved Buck-Boost

A dual buck-boost is analysed by using the circuit average method [1, page 441]. A similar procedure found in [2] is used to find the dc model and the small-signal model for the proposed topology. According to the notation used in references [1] and [2] it is easy to visualize the relation between the general small-signal model of the proposed dual buck-boost and the other models derived from this approach to determine the following figures, where the disturbances can be d, i_o and/or v_{in}:

- The input to output transfer function or $\frac{V_o}{V_{in}} = M_v$, here $d = 0$, $i_o = 0$. Figure 4.1 on page 51
- The control to output transfer function or $\frac{v_o}{d} = T_p$, here $i_o = 0, v_i = 0$. Figure 4.2 on page 52.

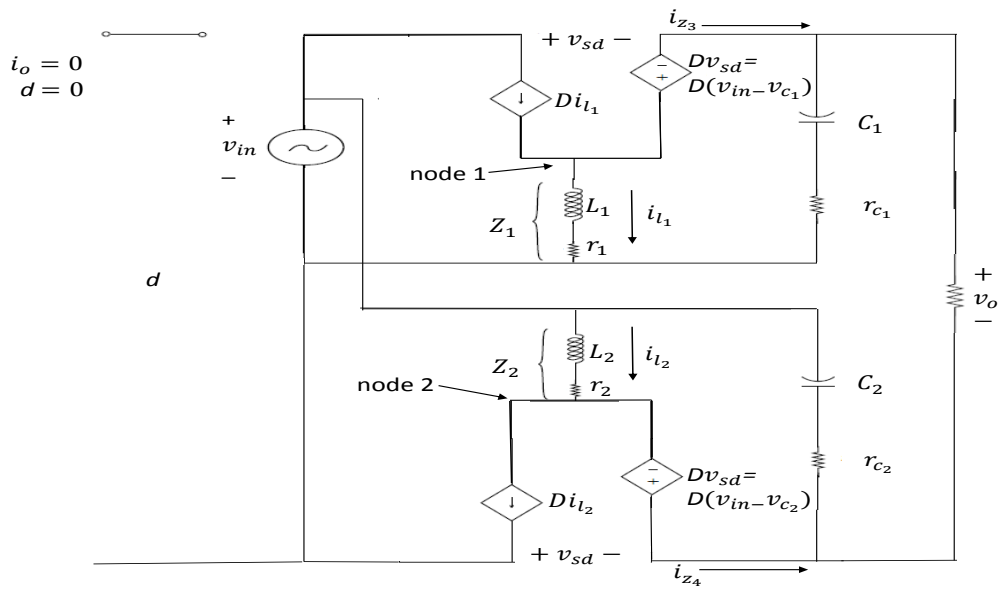

Figure 4.1: Small signal model of dual buck-boost to determine $\frac{V_o}{V_{in}} = M_v$. The circuit average method was used.

- The output impedance Z_o, here $d = 0$, $i_o = 0$, $v_{in} = 0$ Figure 4.3 on page 52.

A dc model is shown in Figure 4.7 on page 54 . This will be used in conjunction with the general small signal model on Figure 4.5 on page 53 to find the control to output transfer function. The corresponding simulated LTspice[1] small signal model is shown in Figure 4.6 on page 54.

The main result, $M_v = \frac{v_o}{v_{in}}$, is found in the equation A.63 and is rewritten here in equation 4.1 for clarity:

$$M_v = \frac{v_o}{v_{in}} = \frac{s^2CL + sCr - 1 - D - 4D^2}{-s^2CL - sCr + 1 - D} \tag{4.1}$$

4.1.1 Minimum Separable Switching Configuration Method

A second methodology to find the transfer functions is investigated. An interleaved buck-boost is analysed by using MInimum Separable Switching COnfiguration technique (MISSCO) [3]. This methodology models the low-frequency behavior of power switches in square-wave power converters. MISSCO is used to derive the low-frequency behavior model of the interleaved buck-boost and will be used to find the relationship between the duty cycle and the output voltage, $\frac{\delta V_o(s)}{\delta D(s)}$ and the relationship between the dc input voltage and the output voltage, $\frac{\delta V_o(s)}{\delta V_{in}(s)}$

[1]LTSpice is a simulation software from www.linear.com

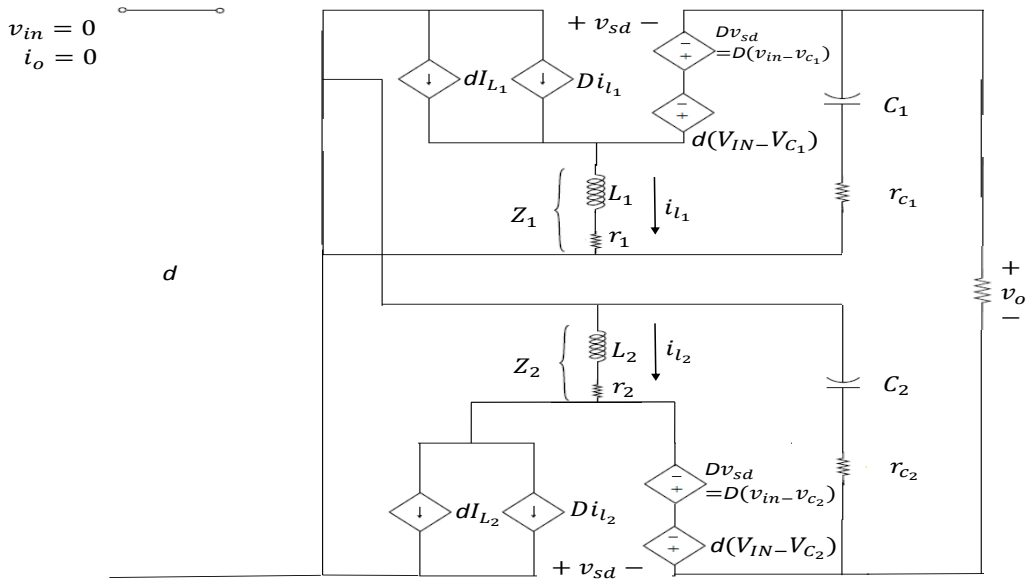

Figure 4.2: Small signal model of dual buck-boost to determine the control to output transfer function $T_p = \frac{V_o}{d}$. The circuit average method was used.

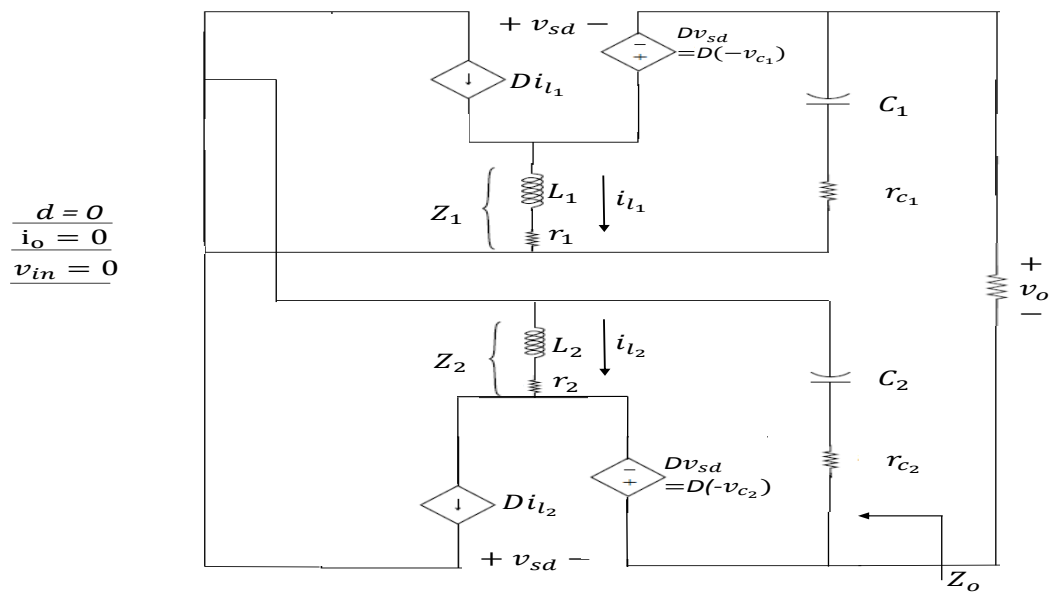

Figure 4.3: Small signal model of dual buck-boost to determine the output impedance Z_o. The circuit average method was used.

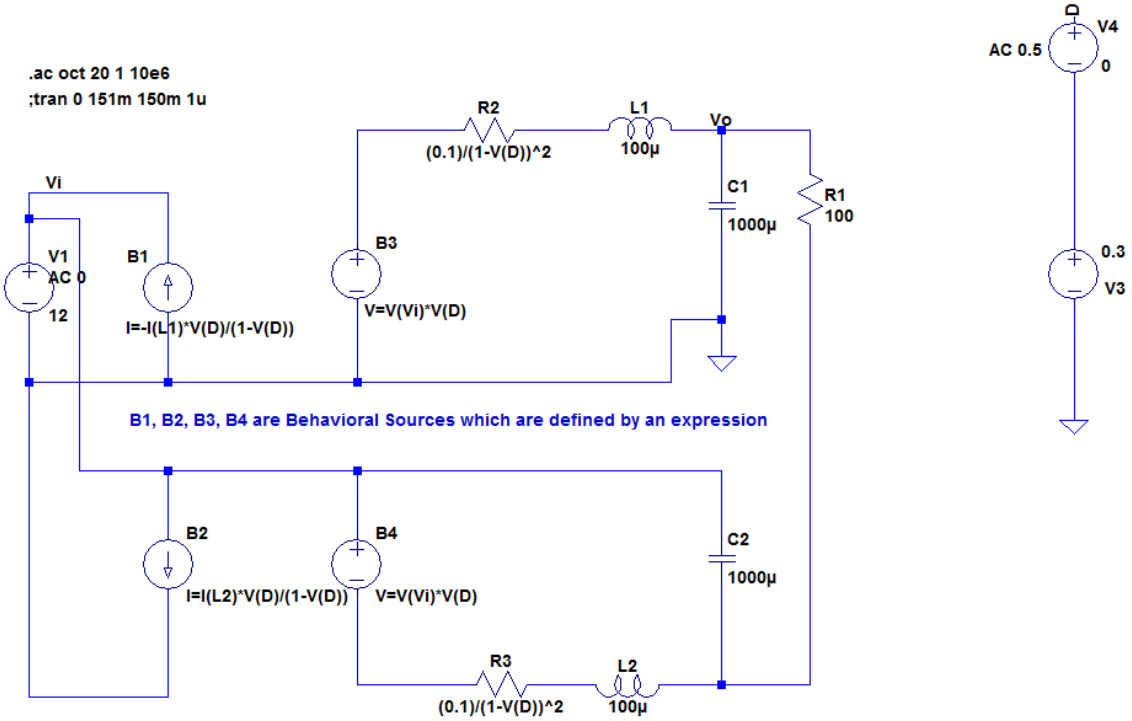

Figure 4.4: Small signal model of dual interleaved buck-boost. The MISSCO method was used. LTspice simulation software was used

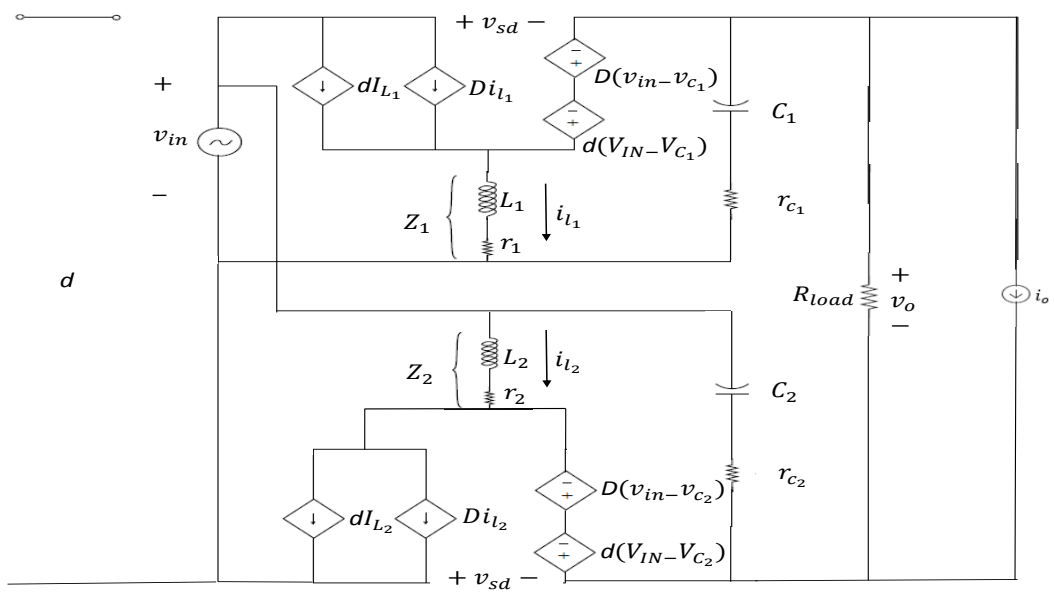

Figure 4.5: General small signal model of dual buck-boost. Figures 4.1, 4.2 and 4.3 are derived from this Figure. The circuit average method was used.

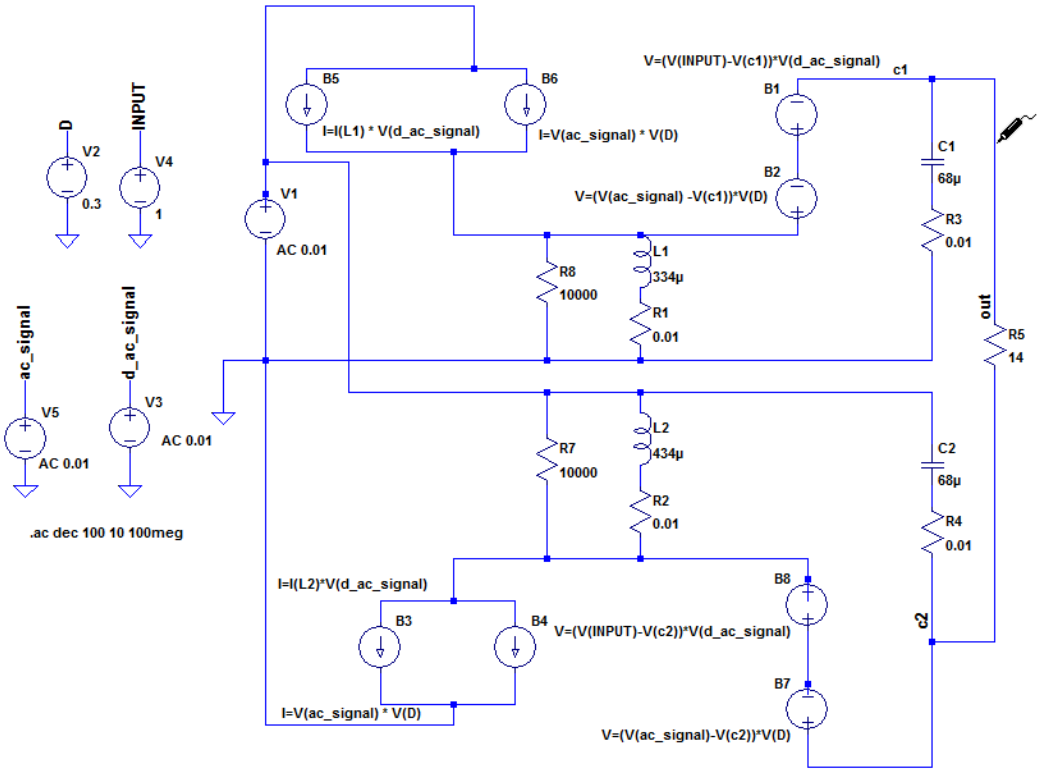

Figure 4.6: LTspiceIV model for dual buck-boost. The circuit average method was used.

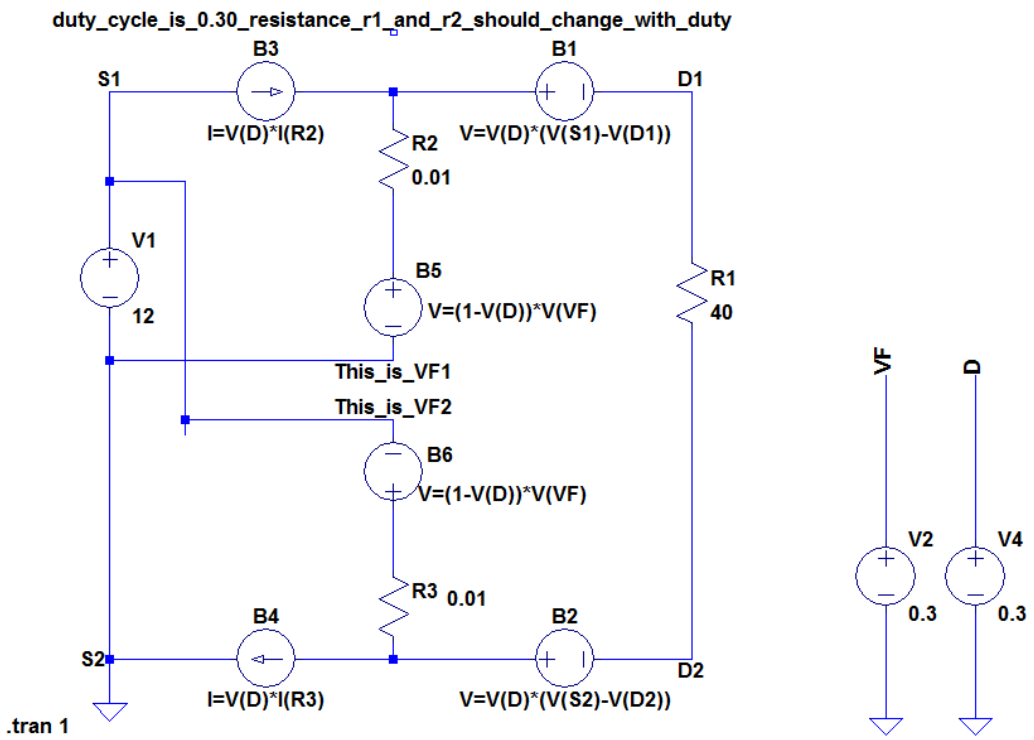

Figure 4.7: DC model of dual interleaved buck-boost. The MISSCO method was used.

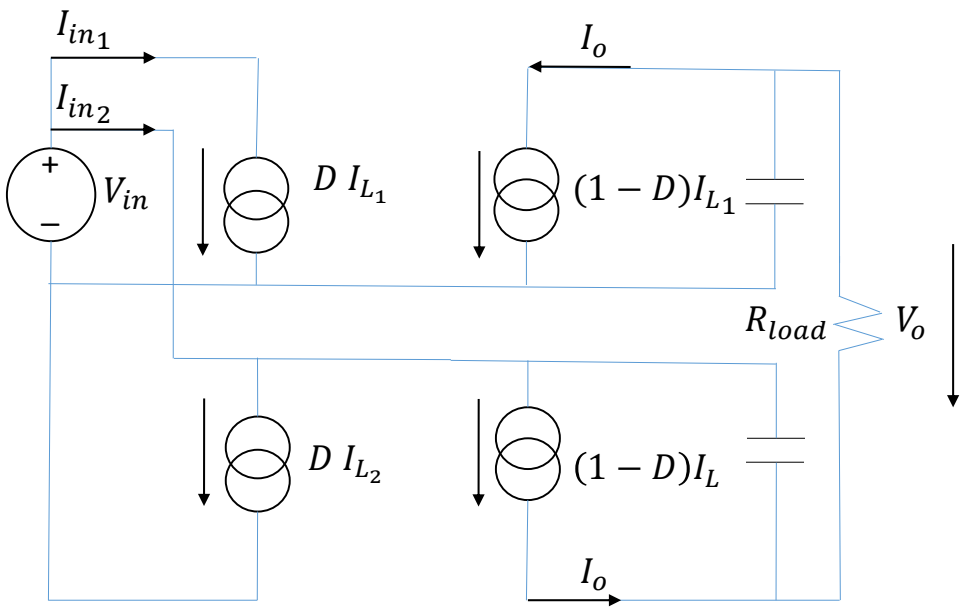

Figure 4.8: SPICE model for the proposed dual buck-boost converter in CCM. MISSCO methodology was applied for the analysis.

Following a similar procedure [4] a SPICE model is found for the proposed topology. The SPICE model of the dual buck-boost converter in CCM is presented in Figure 4.8 on page 55. The SPICE model of the dual buck-boost converter in DCM is presented in Figure 4.9 on page 56.

4.1.2 State Space Averaging Method

The circuit averaging technique was developed before the state-space averaging [5]. All the manipulations are performed on the circuit diagram, instead on its equations, and hence the circuit averaging technique gives a more physical interpretation to the model. Since the circuit averaging involves averaging and small-signal linearization, it is equivalent to state-space averaging. Both methodologies can be combined to give more insight when and involuted model is obtained and overcome this problem.

For the proposed topology 4 switching states are found, referred as modes of operation depending on the input signals, and they are described from Figure 5.1 on page 64 to Figure 5.4 on page 66. The matrices, corresponding to the four modes, are obtained for the proposed topology as follows[2]:

[2]Notation: In A0 (decimal notation) both switches are off, this can be rewritten as A00 (in binary notation). Therefore A0 is in decimal corresponding to A00 in binary. By using this notation the

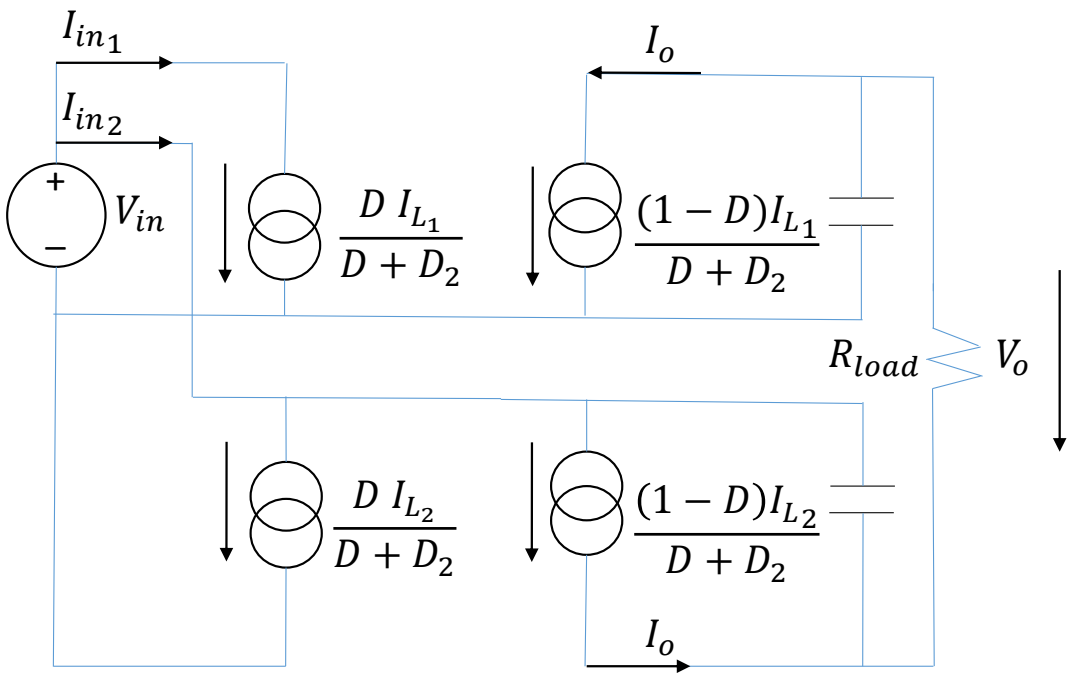

Figure 4.9: SPICE model for the proposed dual buck-boost converter in DCM. MISSCO methodology was applied for the analysis.

Decimal notation	Binary notation	MOSFET 1	MOSFET 2
A0	A00	OFF	OFF
A1	A01	OFF	ON
A2	A10	ON	OFF
A3	A11	ON	ON

Table 4.1: MOSFET's states for A0, A1, A2, A3 matrices

The state-space average systems is written as:

$$\begin{aligned} \dot{X} &= \boldsymbol{A}X(t) + \boldsymbol{B}(U) \\ Y(t) &= \boldsymbol{C}X(t) + \boldsymbol{E}U(t) \end{aligned} \tag{4.2}$$

The matrices for (4.2) are as follows:

MOSFET's states e.i. can be seen through the decimal notation.

A0 → MOSFET 1 OFF, MOSFET 2 OFF.

$$A0 = \begin{bmatrix} \frac{-1}{C_1 R_{load}} & \frac{-1}{C_1 R_{load}} & \frac{1}{C_1} & 0 \\ \frac{-1}{C_2 R_{load}} & \frac{-1}{C_2 R_{load}} & 0 & \frac{1}{C_2} \\ \frac{-1}{L_1} & 0 & 0 & 0 \\ 0 & \frac{-1}{L_2} & 0 & 0 \end{bmatrix}$$

A1 → MOSFET 1 OFF, MOSFET 2 ON.

$$A1 = \begin{bmatrix} \frac{-1}{C_1 R_{load}} & \frac{-1}{C_1 R_{load}} & \frac{1}{C_1} & 0 \\ \frac{-1}{C_2 R_{load}} & \frac{-1}{C_2 R_{load}} & 0 & 0 \\ \frac{-1}{L_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$$

A2 → MOSFET 1 ON, MOSFET 2 is OFF.

$$A2 = \begin{bmatrix} \frac{-1}{C_1 R_{load}} & \frac{-1}{C_1 R_{load}} & 0 & 0 \\ \frac{-1}{C_2 R_{load}} & \frac{-1}{C_2 R_{load}} & 0 & \frac{1}{C2} \\ 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{L_2} & 0 & 0 \end{bmatrix}$$

A3 → MOSFET 1 ON, MOSFET 2 is ON.

$$A3 = \begin{bmatrix} \frac{-1}{C_1 R_{load}} & \frac{-1}{C_1 R_{load}} & 0 & 0 \\ \frac{-1}{C_2 R_{load}} & \frac{-1}{C_2 R_{load}} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$$

B0 → MOSFET 1 OFF, MOSFET 2 OFF.

$$B0 = \begin{bmatrix} \frac{-1}{C_1 R_{load}} \\ \frac{-1}{C_2 R_{load}} \\ 0 \\ 0 \end{bmatrix}$$

B1 → MOSFET 1 OFF, MOSFET 2 ON.

$$B1 = \begin{bmatrix} \frac{-1}{C_1 R_{load}} \\ \frac{-1}{C_2 R_{load}} \\ 0 \\ \frac{-1}{L_2} \end{bmatrix}$$

B2 → MOSFET 1 ON, MOSFET 2 OFF.

$$B2 = \begin{bmatrix} \frac{-1}{C_1 R_{load}} \\ \frac{-1}{C_2 R_{load}} \\ \frac{-1}{L_1} \\ 0 \end{bmatrix}$$

B3 → MOSFET 1 ON, MOSFET 2 ON.

$$B3 = \begin{bmatrix} \frac{-1}{C_1 R_{load}} \\ \frac{-1}{C_2 R_{load}} \\ \frac{-1}{L_1} \\ \frac{-1}{L_2} \end{bmatrix}$$

C1, C2, C3, C4 matrices[3] are the same matrix because there is a direct transfer from the input to the output. Using this notation: C1 = C2 = C3 = C4 = C.

$$C = \begin{bmatrix} 1 \\ 1 \\ 0 \\ \frac{-1}{L_2} \end{bmatrix}$$

E1, E2, E3, E4 matrices are the same matrix because there is a direct transfer from the input to the output. Using this notation: E1 = E2 = E3 = E4 = E.

$$E = \begin{bmatrix} 1 \end{bmatrix}$$

The state-space average model that describes the converter in equilibrium is:

$$\begin{aligned} 0 &= \boldsymbol{A}X(t) + \boldsymbol{B}(U) \\ Y(t) &= \boldsymbol{C}X(t) + \boldsymbol{E}U(t) \end{aligned} \tag{4.3}$$

For the proposed converter with $V_{in} = 12V$, by using MATLAB, the equilibrium vector was found in Table 4.2 and in Figure 4.10.

The transfer function for the proposed converter found in MATLAB without any small ac variations about the equilibrium solution, or quiescent operating point is shown if Figure 4.11.

[3]In this context don't confuse C1 with C_1 = capacitor 1 or C2 with C_2 = capacitor 2

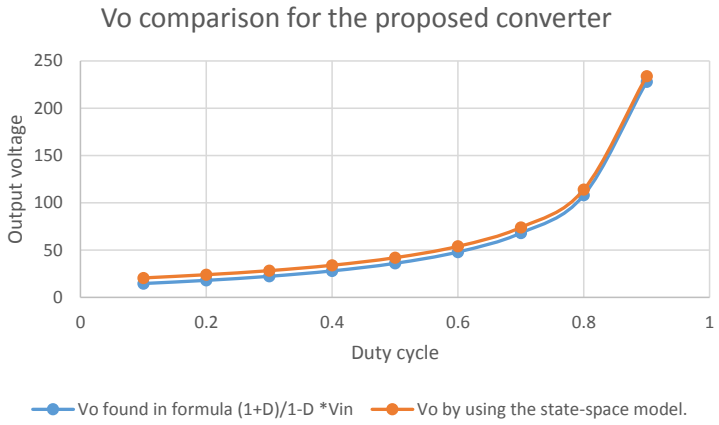

Figure 4.10: Output voltage of proposed converter. Lower line comes from theoretical result (3.6). Upper line comes from the small-signal model when the converter is in equilibrium. Therefore $\dot{X} = 0$.

```
D =

  0.4000


sys =

 s^4 + 1.149e-13 s^3 + 5.52e06 s^2 + 7.657e-07 s + 5.875e12
 ------------------------------------------------------------
    s^4 + 4 s^3 + 2.88e06 s^2 + 5.76e06 s + 2.074e12

Continuous-time transfer function.


X =

  14.0000
   8.0000
   0.5667
   0.5667


Y =

  34
```

Figure 4.11: Matlab screen: Transfer function, sys, for the proposed topology by using the state-space averaged model. Duty is D = 0.40. The equilibrium point where $\dot{X} = 0$ is the vector X (4rows 1 column) with four values: $V_{c_1} = 14V$, $V_{c_2} = 8V$, $I_{L_1} = 0.566A$ and $I_{L_2} = 0.566A$. Output voltage, Y is 34.

Vo from $12 * \frac{1+D}{1-D}$	Vo from state-space model by using MATLAB	Duty cycle
14.66	20.66	0.1
18	24	0.2
22.28	28.28	0.3
28	34	0.4
36	42	0.5
48	54	0.6
68	74	0.7
108	114	0.8
228	234	0.9

Table 4.2: Output voltage of proposed topology. First column is the theoretical value found in (3.6). Second column is found by using the state-space model in equilibrium. 4.10

To find a small-signal model by using the state-space representation one needs to perturb the system. After perturbing the system with small signal variations in the input vector,$\hat{u}(t)$, and the duty cycle, $\hat{d}(t)$. The vectors $\hat{x}(t)$ and $\hat{y}(t)$ are the resulting small ac variations in the state and output vectors. The ac variations are assumed to be much smaller than the quiescent values. After following a procedure, like the one found in [5, page 221], in order to find de small-signal model, the dc terms that satisfy (4.3) can be dropped from the analysis and the second order terms as well.

The transfer function for the small signal model is found in Matlab for the perturbation of the duty and output vectors:

4.1.3 Canonical Model

In the previous chapters 3 techniques have been discussed to find the ac equivalent circuit. In the literature review there are numerous references on average modeling. For example [5, pages 257-258] mentions twenty that are used for modeling switching converters. [5, page 247] proposes a Canonical Circuit Model with 3 characteristics for all PWM CCM dc/dc converters because they perform similar basic functions:

1. They transform the voltage and current levels, ideally with 100% of efficiency.

2. They contain low pass filtering of waveforms. While necessary to remove the high-frequency switching ripple, this filtering also influences low-frequency voltage and current variations.

```
d_perturbation =   0.0100
u_perturbation =   0.0100
D = 0.4000

sys =

  s^4 + 3.92 s^3 - 6.569e05 s^2 + 5.645e06 s - 3.02e12
  ----------------------------------------------------
  s^4 + 3.96 s^3 + 2.88e06 s^2 + 5.702e06 s + 2.074e12

Continuous-time transfer function.

X =
   0.1400
  -29.6085
   -0.4841
   -0.4841
Y =
  -17.4685
```

Figure 4.12: Matlab screen: Transfer function, sys, for the proposed topology by using the small-signal ac model. Duty is D = 0.40. The $\hat{x}$, $\hat{u}$, $\hat{y}$ and $\hat{d}$ are small ac variations about the equilibrium solution, or quiescent operating point.

3. The converter waveforms can be controlled by variation of duty cycle.

Therefore canonical model tries to include the the physical properties of converters that the analysis is after. [5, page 249] describes a figure of the complete canonical circuit, which can model <u>any</u> PWM CCM dc-dc converter. In [5, page 250] mentions a canonical transfer function for the small-signal control-to-output voltage.

4.2 Bode Plots of Open-Loop Transfer Function

In Figure 4.13 circuit average's bode plots from the dual buck-boost's small signal model are shown. The simulation software for this figure is LTspice IV.

In Figure 4.14 on page 62 MISSCO's bode plots from the dual buck-boost's small signal model are shown. The simulation software for this figure is LTspice IV.

4.3 Control Aspects of Dual DC/DC converter

The converter can be regulated via voltage mode control or current mode control. Since the output voltage is floating with respect to the input source, either opto-coupler amplifier or differential amplifier is used to feedback sensed output voltage to the PWM controller. As mentioned in Chapter 3, the two switches can be phase-shifted in order to reduce the input current ripple. The phase shift can be achieved via an RC delay circuit if analogue controller is used or software delay if digital control is used. The detailed

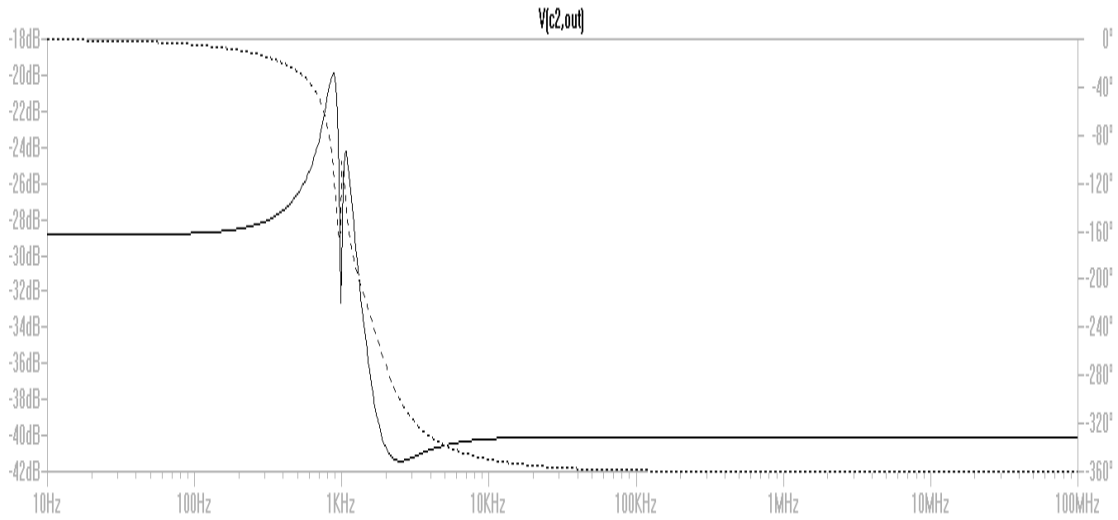

Figure 4.13: Bode plot of dual buck-boost's of general small signal model from LTspice IV on Figure 4.6. Magnitude is the continuous line. The circuit average method was used.

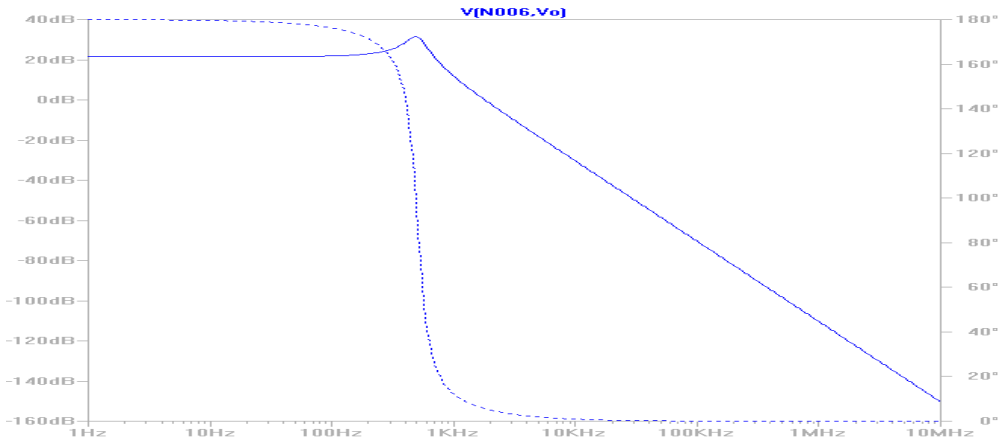

Figure 4.14: Bode plot of dual buck-boost's converter by using MISSCO technique. Simulation software was LTspice IV. The magnitude is the continuous line.

control scheme can be found in [6].

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[1] M. K. Kazimierczuk, *Pulse-width Modulated DC-DC Power Converters.* Wiley, 15.09.2008.

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[6] W. Wang and D.-C. Lu, "A bridgeless divm buck pfc rectifier with digital control and voltage doubler configuration," *International Journal of Power Electronics*, Vol. 5, No. 2, pp.125-144, 2013.

Chapter 5

Experimental Verification and Discussion

In this chapter, the dual buck-boost converter, which has been studied in Chapter 4, is built and tested.

5.1 Further Discussion on Circuit Operation

In CCM, the proposed converter can operate in 4 different conduction modes depending on the input signals.

- Mode 1, Figure 5.1
- Mode 2, Figure 5.2
- Mode 3, Figure 5.3

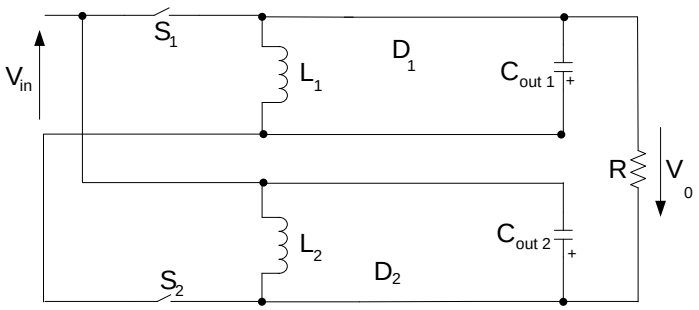

Figure 5.1: Mode 1: D1 and D2 are closed.

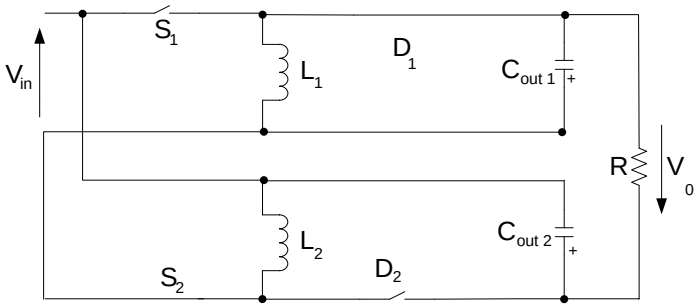

Figure 5.2: Mode 2: D1 and S2 are closed.

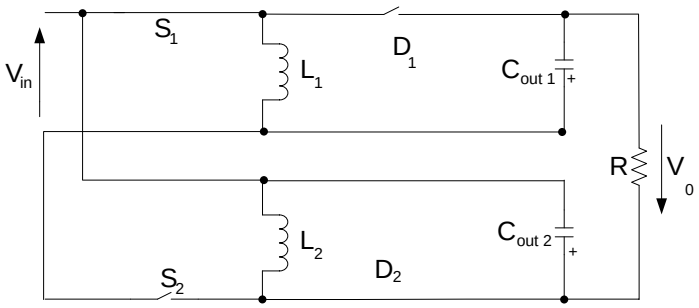

Figure 5.3: Mode 3: S1 and D2 are closed.

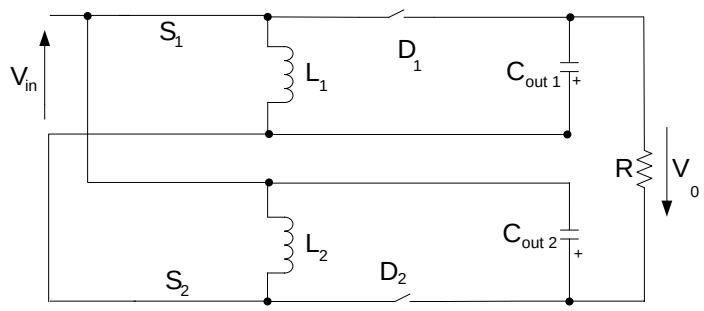

Figure 5.4: Mode 4: S1 and S2 are closed.

- Mode 4, Figure 5.4

5.2 Experimental Setup

A hardware prototype using the dual buck-boost topology as analyzed in Chapters 3 and 4 is constructed and tested. The schematic of the converter is shown in Figure 5.8 and Figure 5.6 shows a snapshot of the experimental setup. The following parameters are used for the prototype:

- Capacitor 1000μF 35V, 2 capacitors connected to the R_{load}
- Capacitor 22μF, 63V, 1 capacitor connected between V_{cc} and COM (IR2101)
- Capacitor 330μF, 25V 1 capacitor connected between V_{cc} and COM (IR2101)
- Capacitor 10μF, 2 capacitors connected between V_B and V_s (IR2101)
- Diode U820: Quantity 1: for V_{cc} and V_B (IR2101)
- Diode IN4148: Quantity 3: 2 for gate signals, 1 for V_{cc} and V_B (IR2101)
- IR2101: Quantity: 2 (for 2 MOSFETS)
- Inductor: 100uH
- MOSFET: MTW32N20E
- MOSFET: STP24NF10
- Isolated 1W Dual Output DC-DC Converters: NMA1212S: Quantity 2.

T1	T2	D1	D2	Stages of a switching cycle	CCM	DCM
0	0	0	0	0	-	0
0	0	0	1	1	-	1
0	0	1	0	2	-	2
0	0	1	1	3	3	3
0	1	0	0	4	-	4
0	1	0	1	5	-	-
0	1	1	0	6	6	6
0	1	1	1	7	-	-
1	0	0	0	8	-	8
1	0	0	1	9	9	9
1	0	1	0	10	-	-
1	0	1	1	11	-	-
1	1	0	0	12	12	12
1	1	0	1	13	-	-
1	1	1	0	14	-	-
1	1	1	1	15	-	-

Figure 5.5: It shows all possible states the converter can have. There are 4 in CCM and 9 in DCM. Some states are not possible unless the converter is malfunctioning or broken.

5.3 Key Switching Waveforms

Pulses for the Gate to Source Voltage applied to the MOSFET are shown in Figs. 5.9 and 5.10

The Figure 5.12shows inductor 1 compared with input pulses. Figure 5.13 shows inductor 2 compared with input pulses.

From Figure 5.14 , on page 72, to Figure 5.18, on page 73, the inductor 2 voltage, V_{L_2} in blue, can be seen going from DCM to CCM. In Figure 5.14 is clear the inductor is in DCM because the voltage drops to zero, sags and bounces before the period ends. In Figure 5.16 the inductor is about to leave DCM and enter CCM. In Figure 5.18 the inductor already is in CCM.

5.4 Plots of Voltage Conversion Ratio

The voltage conversion ratio of a single buck-boost is shown in Figure 5.19

The voltage conversion ratio of a dual buck-boost is shown of Figure 5.20

The formula L_{min} from [1, page 204] is used to find the maximum resistance that can

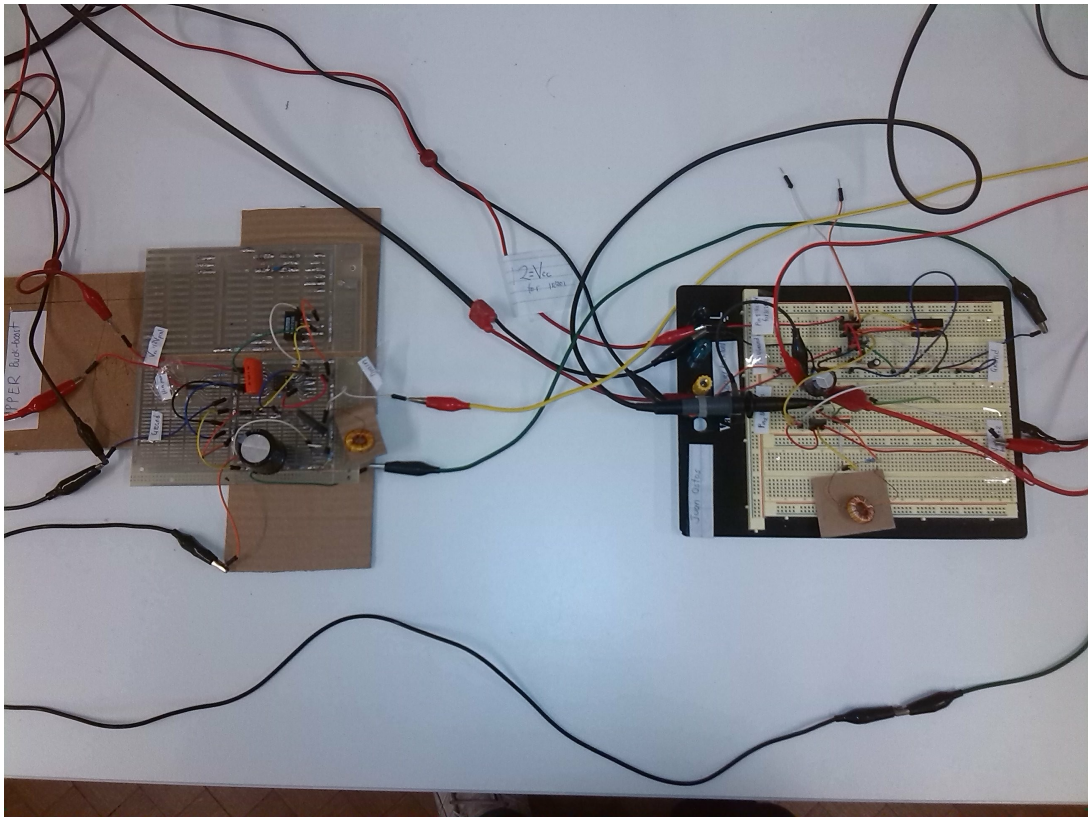

Figure 5.6: Photo of the actual lab prototype of dual buck-boost. To the left is the upper stage and to the right is the lower stage. A external signal generator was used to drive the MOSFETs.

be applied to the converter:

$$L_{min} = \frac{(1-D)^2 R}{2f} \tag{5.1}$$

The maximum resistance for a buck-boost converter for not to enter in DCM was used as shown in the Figure 5.7

Bibliography

[1] D. W. Hart, *Introduction to power electronics.* Prentice Hall, Upper Saddle River, 1997.

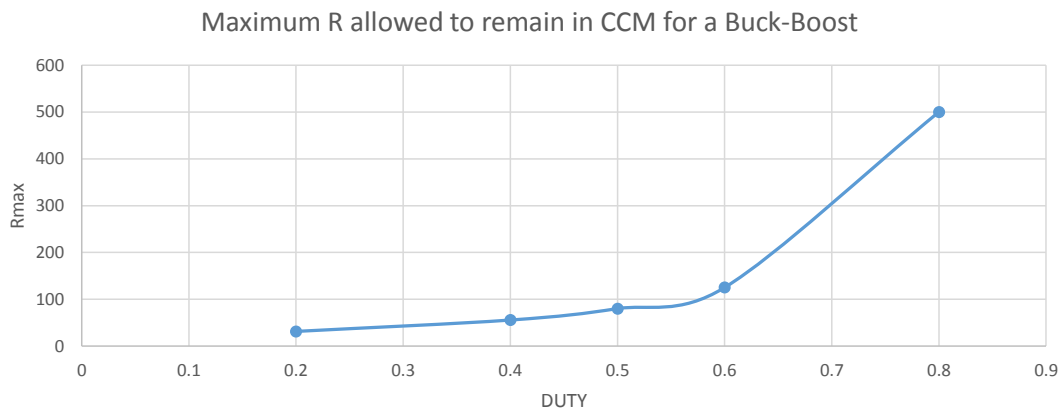

Figure 5.7: R_{max} for a buck-boost converter to remain in CCM

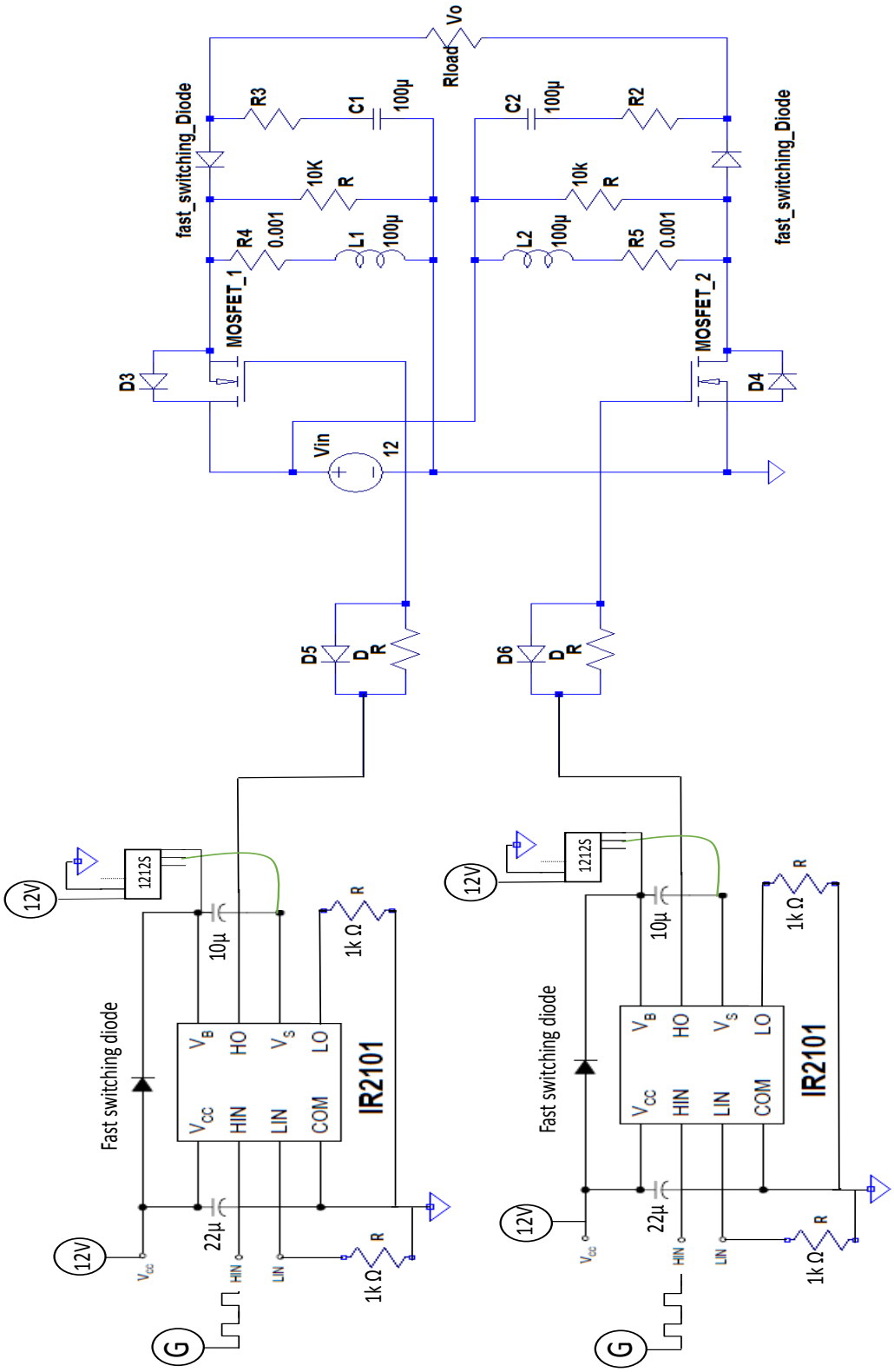

Figure 5.8: Schematic. Left side is the control system for the Mosfets and right side is the dual buck-boost.

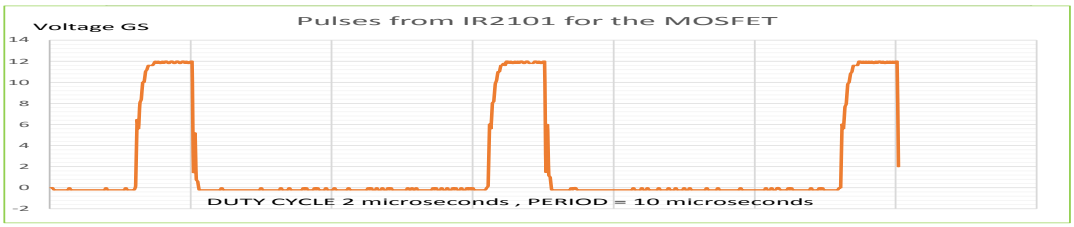

Figure 5.9: Pulses applied to the Mosfet 1, from IR2101 V_s's pin, to have the gate to source Voltage. Excel graph. Compare with Figure 5.10

Figure 5.10: Pulses applied to the Mosfet 2, from IR2101 V_s's pin, to have the gate to source Voltage.

Figure 5.11: Upper: Input pulses to IR2101 are shown. Pulses are generated externally by a Signal Generator 33120A Hewlett Packard to feed the IR2101 on pin HIN. Lower: Output pulses (number 2) come from IR2101's V_s pin on Figure 5.8 and are applied to the Mosfet's gate. Note that output signal is attenuated because needs more rising time.

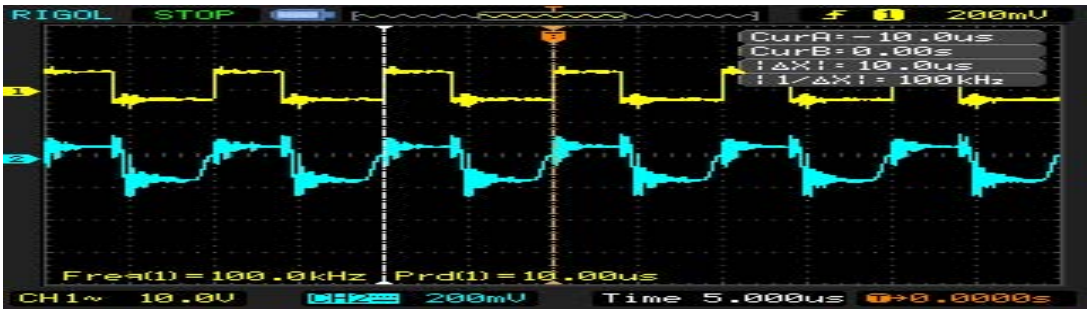

Figure 5.12: Upper: Input pulses to IR2101. Duty cycle is 0.40. Lower: Inductor 1 voltage signal in CCM.

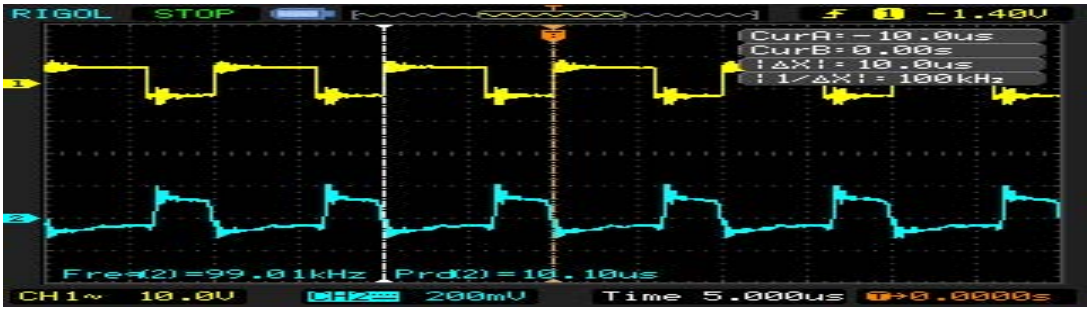

Figure 5.13: Upper: Input pulses to IR2101. Duty cycle is 0.60. Lower: Inductor 2 voltage signal in CCM.

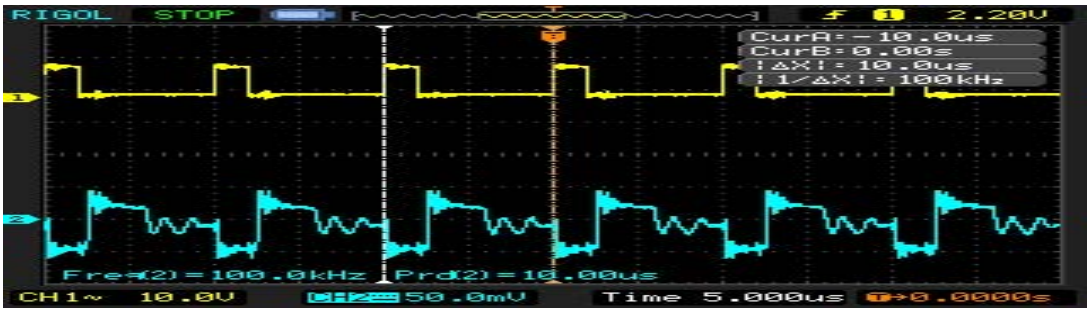

Figure 5.14: Upper: Input pulses to IR2101. Duty cycle is 0.20. Lower: Inductor 2 voltage signal in DCM.

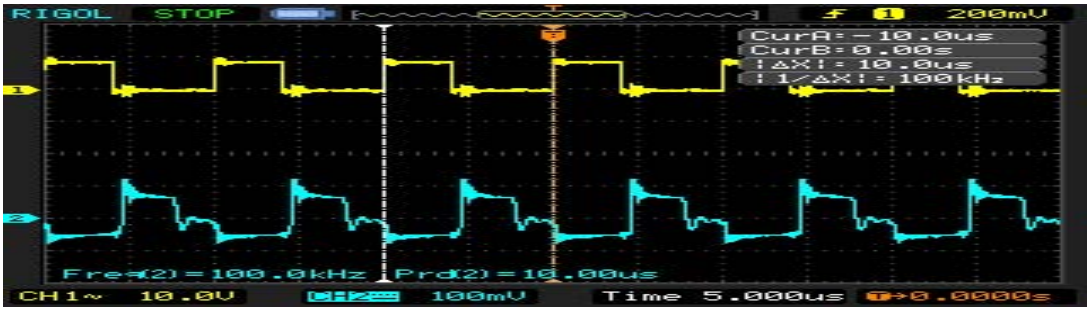

Figure 5.15: Upper: Input pulses to IR2101. Duty cycle is 0.40. Lower: Inductor 2 voltage signal in DCM.

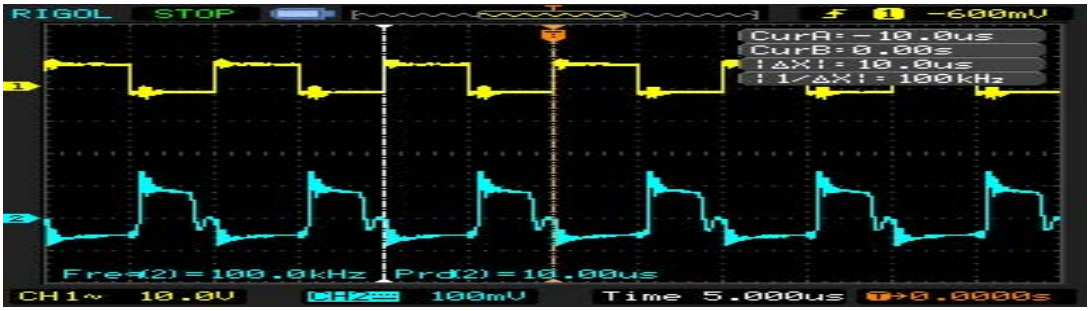

Figure 5.16: Upper: Input pulses to IR2101. Duty cycle is 0.50. Lower: Inductor 2 voltage signal in DCM.

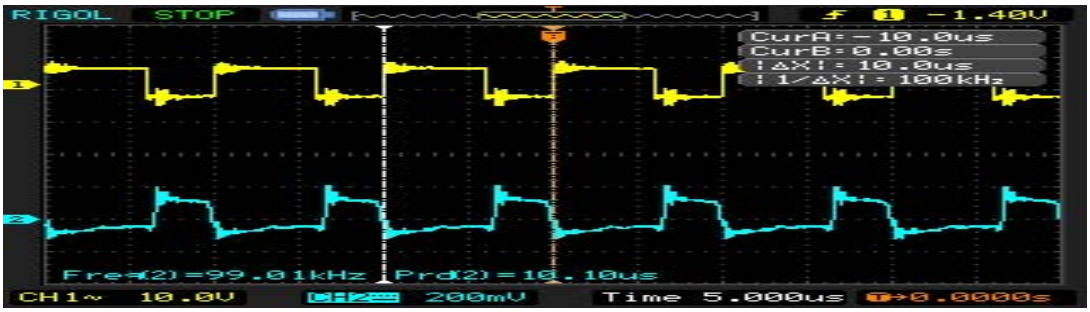

Figure 5.17: Upper: Input pulses to IR2101. Duty cycle is 0.60. Lower: Inductor 2 voltage signal in CCM.

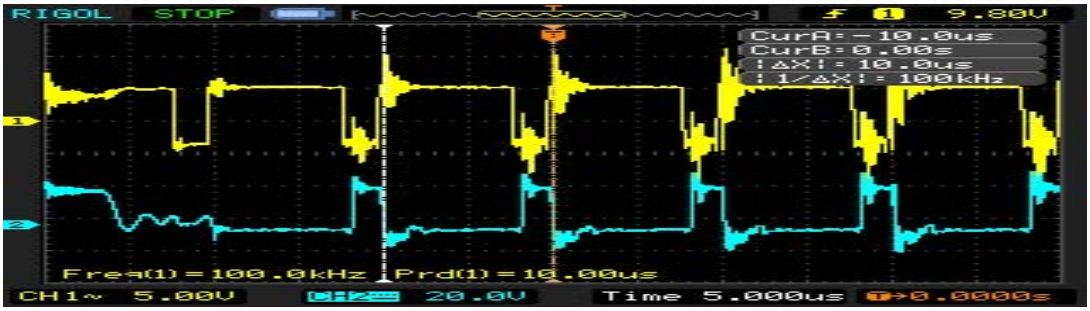

Figure 5.18: Upper: Input pulses to IR2101. Duty cycle is 0.80. Lower: Inductor 2 voltage signal in CCM.

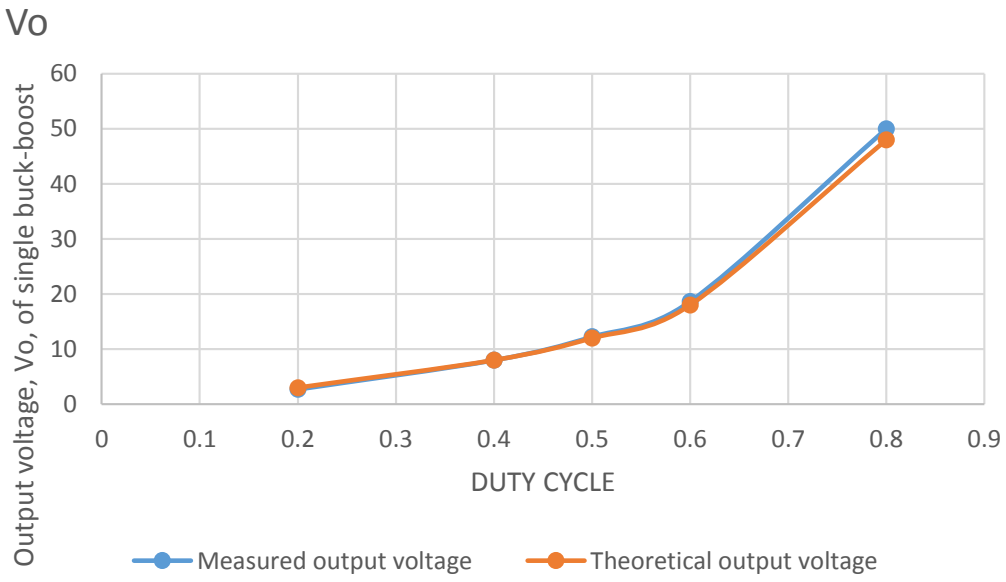

Figure 5.19: The measured output voltage vs. the theoretical one, for a single buck-boost is shown. Note that the lab results in the last point, 50 volts, exceeded the expectations that were 48 volts.

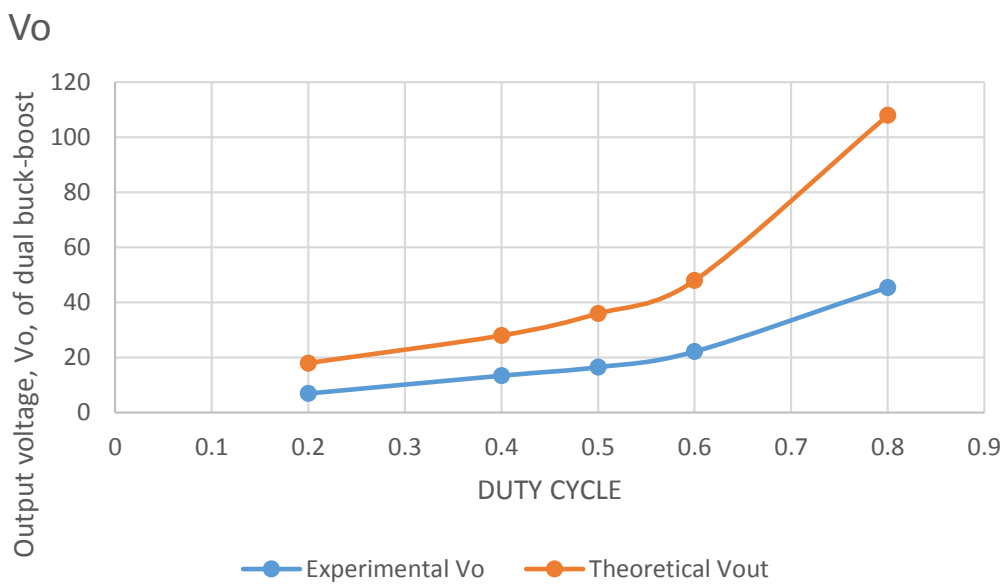

Figure 5.20: The measured output voltage for a single buck-boost vs a dual buck-boost is shown.

Chapter 6

Conclusion and future work

6.1 Conclusion

This thesis reviewed existing switching power converters for high voltage gain applications. The general criteria of developing high quality power conversion are collected through the literature review. This thesis proposed a new converter structure which is suitable for high voltage gain applications with some critical features such as high efficiency, low current ripple, and improved reliability. Vast majority of the converter topologies can be inserted in the proposed converter structure. Due to the converter structure, an inverting topology will yield higher conversion efficiency than a non-inverting topology. A dual buck-boost topology is used as a case study. Steady-state and dynamic analyses were performed. Some experimental are provided to confirm the analysis of the converter topology.

6.2 Future Work

This thesis focuses on the analysis of proposed converter structure and synthesis of the converter topologies. Future work can be conducted to apply this converter structure for specific applications such as PV and battery systems. Apart from hard-switching topologies, the proposed converter structure is also suitable for resonant-type converters to be inserted as they inherit soft-switching feature which reduces the switching losses. The open-loop was investigated in this thesis. It provides key equations for close-loop design according to different applications the converter to be designed.

Appendices

Appendix A

Equations to Find M_v

The procedure to find M_v, equation A.63, begins with equation A.1.

From the dc model, Figure 4.7 on page 54, is found:

$$DI_{L_1} = I_{L_1} + I_o \tag{A.1}$$

$$-(1-D)I_{L_1} = I_o \tag{A.2}$$

$$I_{L_1} = -\frac{I_o}{(1-D)} \tag{A.3}$$

On the other hand:

$$I_o = \frac{v_o}{R_{load}} \tag{A.4}$$

Therefore we can join A.3 with A.4 to have:

$$I_{L1} = -\frac{v_o}{(1-D)R_{load}} \tag{A.5}$$

Similarly with the lower stage:

$$I_{L2} + I_o = DI_{L2} \tag{A.6}$$

$$I_{L2}(1-D) = I_o \tag{A.7}$$

therefore

$$I_{L2} = \frac{I_o}{(1-D)} \tag{A.8}$$

The currents are the same but with different direction:

$$I_{L1} = -I_{L2} \tag{A.9}$$

For convenience this is assumed that reflected resistances from the diode and switch branches to the inductor 1 and inductor 2 respectively are equal.

$$r_1 = r_2 \tag{A.10}$$

r_{DS} is the switch resistance. When is averaged a D appears under this resistance: $\frac{r_{DS}}{D}$. This resistance is located in the switch branch [1, page 405]. Similarly R_F is the diode forward resistance. When is averaged a $(1-D)$ appears under this resistance: $\frac{R_F}{(1-D)}$ [1, page 405]. This resistance is located in the diode branch. Because is easier to reflect those resistances, r_{DS} and R_F, to the inductor branch, the reflection rules are used.

General reflection rules for averaged resistances on inductor, switch and diode branch respectively are as follows:

$$r_l = D^2 r_s = (1-D)^2 r_d \tag{A.11}$$

and for equivalent averaged voltage sources in the inductor, switch and diode branch respectively are:

$$V_l = DV_s = (1-D)V_d \tag{A.12}$$

Therefore the switch resistance reflected to the inductor branch found is:

$$Dr_{DS} \tag{A.13}$$

and the diode resistance reflected to the inductor branch found is:

$$(1-D)R_F \tag{A.14}$$

r_l as the average inductor resistance. Finally r is found:

$$r = Dr_{DS} + (1-D)R_F + r_l \tag{A.15}$$

In order to find the $T_p = \frac{V_o}{d}$. The following Kirchhoff Voltage Law (KVL) is used on the Figure 4.2 on page 52 , where v_{l_1} is the inductor 1 voltage, i_{l_1} is the current on inductor 1, v_{c_1} is the voltage on Capacitor 1 and D is the duty cycle:

$$v_{l_1} + i_{l_1} r + v_{c_1} - d(V_{IN} - V_{C_1}) - D(v_{in} - v_{c_1}) = 0 \tag{A.16}$$

For this analysis $v_{in} = 0$ and $i_o = 0$, it is known for a buck-boost the capacitor voltage and input voltage are related by $\frac{D}{(1-D)}$, therefore:

$$v_{c_1} = \frac{D}{(1-D)} v_{in} = 0 \tag{A.17}$$

The capacitor 1's low signal voltage is zero. For analogy the lower stage is analysed and it is found the lower capacitor 2's low signal voltage is zero as well. Therefore (A.16) becomes:

$$v_{l_1} + i_{l_1} r - d(V_{IN} - V_{C_1}) = 0 \tag{A.18}$$

$v_{l_1} + i_{l_1} r$ can be written as $Z_1 i_{l_1}$ because $Z_1 = r + sL$.

For now it is considered that the diode's forward voltages $V_{F_1} = V_{F_2} = 0$ are negligible for easiness without losing generality. i_{l_1} is the current on inductor 1 and i_{l_2} is the current on inductor 2. Because $D(v_{in} - v_{c_1}) = D(v_{in} - v_{c_1}) = 0$, we apply the KVL, in order to relate both stages and v_o, the following equation is found:

$$-v_o + d(V_{IN} - V_{C_1}) + d(V_{IN} - V_{C_2}) + Z_1 i_{l_1} + Z_2 i_{l_2} = 0 \tag{A.19}$$

For easiness $Z_1 = Z_2 = Z$ and $V_{C_1} = V_{C_2} = V_C$ (A.19) is reduced to:

$$-v_o + 2d(V_{IN} - V_C) + 2Z(i_{l_1} + i_{l_2}) = 0 \tag{A.20}$$

For convenience this is considered: $V_{C_1} = V_{C_2} = V_C$. $r_{c_1} = r_{c_2}$ can not be negligible because otherwise v_o would be zero. Therefore those resistances are considered in the analysis.

Applying KCL in central part of the Figure 4.2 on page 52 the following currents are found:

The following currents arrive to the node:

$$i_{l_1} + i_{r_{c_1}} + dI_{L_2} + Di_{l_2} \tag{A.21}$$

and the following currents exit the node:

$$i_{l_2} + i_{r_{c_2}} + dI_{L_1} + Di_{l_2} \tag{A.22}$$

Therefore (A.21)= (A.22), can be rewritten as :

$$i_{l_1} + i_{r_{c_1}} + dI_{L_2} + Di_{l_2} = i_{l_2} + i_{r_{c_2}} + dI_{L_1} + Di_{l_2} \tag{A.23}$$

for easiness we assume $i_{r_{c_1}} = i_{r_{c_2}} = i_{r_c}$, they cancel out and (A.23) becomes:

$$i_{l_1} + dI_{L_2} + Di_{l_2} = i_{l_2} + dI_{L_1} + Di_{l_2} \tag{A.24}$$

By using (A.9) into (A.24), and assuming $I_{L_1} = -I_{L_2} = I_L$ this becomes:

$$i_{l_1} - dI_L + Di_{l_2} = i_{l_2} + dI_L + Di_{l_2} \tag{A.25}$$

Passing the $-dI_L$ to the right side A.25 becomes:

$$i_{l_1} + Di_{l_2} = i_{l_2} + 2dI_L + Di_{l_1} \tag{A.26}$$

Organising the currents the following is found:

$$i_{l_1}(1-D) = 2dI_L + (1-D)i_{l_2} \tag{A.27}$$

and finally

$$i_{l_1} = i_{l_2} + \frac{2dI_L}{1-D} \tag{A.28}$$

Inserting (A.28) into (A.20) the following is found:

$$-v_o + 2d(V_{IN} - V_C) + 2Z(i_{l_1} + i_{l_1} - \frac{2dI_L}{1-D}) = 0 \tag{A.29}$$

From the small signal model in Figure 4.2 on page 52 it is know that:

$$dI_L + Di_{l_1} = i_{l_1} \tag{A.30}$$

From (A.56)

$$i_{l_1} = \frac{dI_L}{1-D} \tag{A.31}$$

(A.56) is inserted into (A.29) to overcome the unknown i_{l_1} .

$$-v_o + 2d(V_{IN} - V_C) + 2Z(\frac{2dI_L}{1-D} - \frac{2dI_L}{1-D}) = 0 \tag{A.32}$$

Therefore two terms are cancelled out and (A.33) becomes:

$$-v_o + 2d(V_{IN} - V_C) = 0 \tag{A.33}$$

Organizing elements

$$v_o = 2d(V_{IN} - V_C) \tag{A.34}$$

$$\frac{v_o}{d} = 2(V_{IN} - V_C) \tag{A.35}$$

If the diode's forward voltage is considered an additional term appears to the right:

$$\frac{v_o}{d} = 2(V_{IN} - V_C) - \frac{2V_F}{d} \tag{A.36}$$

From the basic buck-boost $V_C = \frac{D}{1-D}V_{in}$. Inserting this into (A.37) the following is found:

$$\frac{v_o}{d} = 2(V_{IN} - V_{IN}\frac{D}{1-D}) \tag{A.37}$$

Therefore T_p is constant dependent of duty cycle:

$$\frac{v_o}{d} = 2V_{IN}(1 - \frac{D}{1-D}) \tag{A.38}$$

Organising terms:

$$T_p = \frac{v_o}{d} = 2V_{IN}(\frac{1-2D}{1-D}) \tag{A.39}$$

In order to find the line to output transfer function, $M_v = \frac{v_o}{v_{in}}$, M_v model from Figure 4.1 is used. KVL is applied to relate v_o with v_{in} via voltage dependant sources. Considering $Z_1 = Z_2 = Z$ and $v_{c_1} = v_{c_2} = v_c$ then the following equation is found:

$$-v_o - v_{in} + (i_{l_1} + i_{l_2})Z - 2D(v_{in} - v_c) = 0 \tag{A.40}$$

v_c is related to v_{in} by $\frac{D}{1-D}$. Inserting this in A.42:

$$-v_o - v_{in} + (i_{l_1} + i_{l_2})Z - 2D(v_{in} - v_{in}\frac{D}{1-D}) = 0 \tag{A.41}$$

Organising the last term:

$$-v_o - v_{in} + (i_{l_1} + i_{l_2})Z - 2Dv_{in}(\frac{1-2D}{1-D}) = 0 \tag{A.42}$$

Joining v_{in}:

$$-v_o - v_{in}(1 + 2D(\frac{1-2D}{1-D})) + (i_{l_1} + i_{l_2})Z = 0 \tag{A.43}$$

Leaving v_o on the left side:

$$v_o = -v_{in}(\frac{1+2D-4D^2}{1-D}) + (i_{l_1} + i_{l_2})Z \tag{A.44}$$

To find i_{l_1} and i_{l_2} KCL is applied on node 1 and 2 respectively:

$$i_{l_1} = -\frac{i_{z_3}}{1-D} \tag{A.45}$$

$$i_{l_2} = \frac{i_{z_4}}{1-D} \tag{A.46}$$

KVL is applied to relate v_o with v_{in} by using the capacitors:

$$-v_{in} - v_{c_2} - v_{c_1} - v_o = 0 \tag{A.47}$$

The capacitor current, i_{c_1} is related with i_{z_3} by KCL.

$$i_{z_3} = i_{c_1} + i_o \tag{A.48}$$

$$i_{z_4} = -i_{c_2} + i_o \tag{A.49}$$

i_o is assumed to be zero from the very beginning of this analysis. Therefore:

$$i_{z_3} = i_{c_1} \tag{A.50}$$

$$i_{z_4} = i_{c_2} \tag{A.51}$$

C_1 and C_2 are the capacitors 1 and 2:

$$i_{c_1}\frac{1}{sC_1} = v_{c_1} \tag{A.52}$$

$$i_{c_2}\frac{1}{sC_2} = v_{c_2} \tag{A.53}$$

Leaving currents on one side :

$$i_{c_1} = sC_1 v_{c_1} \tag{A.54}$$

$$i_{c_2} = sC_2 v_{c_2} \tag{A.55}$$

By inserting (A.54) and (A.50) into (A.45):

$$i_{l_1} = -\frac{v_{c_1} sC_1}{1-D} \tag{A.56}$$

By inserting (A.55) and (A.51) into A.46:

$$i_{l_2} = -\frac{v_{c_2} sC_2}{1-D} \tag{A.57}$$

Finally the currents (A.56) and (A.57) are found to be inserted in (A.44):

$$v_o = -v_{in}(\frac{1+2D-4D^2}{1-D}) + (-\frac{v_{c_1} sC_1}{1-D} + -\frac{v_{c_2} sC_2}{1-D})Z \tag{A.58}$$

Organising (A.58) the term to the right: If $C_1 = C_2 = C$

$$v_o = -v_{in}(\frac{1+2D-4D^2}{1-D}) + (-\frac{sC}{1-D}(v_{c_1} + v_{c_2}))Z \tag{A.59}$$

Applying KVL through the capacitors:

$$-v_{in} - v_{c_2} - vc_1 - v_o = 0 \tag{A.60}$$

Organising A.60:

$$-v_{in} - v_{c_2} = vc_1 + v_o \tag{A.61}$$

Inserting (A.61) into (A.62):

$$v_o = -v_{in}(\frac{1+2D-4D^2}{1-D}) + (-\frac{sC}{1-D}(-v_{in} - v_o))Z \tag{A.62}$$

Finally is just organising (A.62) to find the line to output transfer function M_v.

$$M_v = \frac{v_o}{v_{in}} = \frac{s^2CL + sCr - 1 - D - 4D^2}{-s^2CL - sCr + 1 - D} \tag{A.63}$$

Bibliography

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VITA

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