

# Chapter 1

## Introduction

This thesis deals with the design, development and application of components for wide bandwidth signal processing in radio astronomy. In order to set the context for the work that follows, I will give a brief introduction to the field of radio astronomy. This will give sufficient information to appreciate the relevance of the work in this thesis, and in particular the need for wider bandwidth observing systems than are currently in use. As radio astronomy is an extensive science this is not a comprehensive discussion and references such as [1] should be consulted for full information.

### 1.1 A Short Introduction to Radio Astronomy

Radio astronomy is the study of the observable Universe by means of received radiation of radio wavelengths. This encompasses electromagnetic emissions with frequencies ranging from a few megahertz to over a terahertz. The mechanisms responsible for these emissions are many and varied and it is through the study of these emissions, and their interactions with other matter, that the physical processes occurring within astronomical bodies can be investigated.

Conventionally, radio astronomical observations can be classified into

three broad classes: Radiometry; Spectroscopy and Interferometry.

### 1.1.1 Radiometry

Radiometry is the observation mode where the total power emitted by a source within a given receiver bandwidth is measured. This is useful if one is attempting to detect the presence or absence of a source, but is not interested in its spectrum. In this mode the total power is measured, and by doing on and off source measurements, the increase in received power due to the source can be determined, and with suitable calibration the source flux. Typically the presence of a source will only raise the system temperature by a few milliKelvin in a background system temperature of several hundred Kelvin. This requires the power to be measured to an accuracy of better than 1 in 10000. It is the accuracy to which the power can be measured that sets the ultimate sensitivity of the radiometer. The power measurement from the radiometer fluctuates around the true value and has to be integrated until the variance of the measurement error is a few standard deviations smaller than the increase in power due to the source, to be able to make a reliable detection. In a Nyquist sampled measurement bandwidth of  $B$  and an averaging time of  $T$  there are  $2BT$  independent samples than can be taken. The standard deviation of an average of  $N$  normally distributed samples is  $\sqrt{\frac{2}{N}}$  so the standard deviation of the radiometer measurement is

$$\frac{\delta P}{P_0} = \frac{1}{\sqrt{BT}}, \quad (1.1)$$

where  $P_0$  is the mean power. This equation is known as the radiometer equation and describes the theoretical maximum sensitivity of a radiometer system of a given bandwidth with a given integration time. A rigorous derivation of this important result can be found in [1].

### 1.1.2 Spectroscopy

Spectroscopy is concerned with measuring the frequency spectrum of a source. This is useful for determining the presence or absence of elements and molecules, the rates by which objects are receding, approaching or rotating by means of Doppler shifts, conditions of temperature and pressure, and many other uses. In order to measure the spectrum we need a device that separates the received radio signal into its separate wavelength components. In optical astronomy this is done using gratings or prisms. In the radio regime special purpose instruments must be built for this task. The design of some of the key components of such radio spectrometers is what forms the main topic of this work. The sensitivity relation 1.1 also applies to a spectrometer but with the bandwidth being the per channel bandwidth.

### 1.1.3 Interferometry

Interferometry is a technique that allows an increase in resolution by observing a source with two or more telescopes separated by some distance, which can range from metres to many thousands of kilometres. Effectively, the resolution of the observation is equivalent to that of a telescope with diameter equal to the separation of the two telescopes. By repeating the observations using many pairs of telescopes with different spacings, possibly over periods of many months, and relying upon the rotation of the Earth, an image of the source in the spatial Fourier component domain can be obtained, which can then be inverted to give a true intensity image [2].

## 1.2 Importance of Wide Bandwidths

There are several reasons why using wider bandwidths for observations are very desirable. From the brief discussion above it is clear from 1.1 that the sensitivity of an observation is proportional to the square root of the bandwidth. Increasing the bandwidth by a factor of four allows sources twice

as faint to be detected in the same observation time, or alternatively, sources of the same brightness can be detected in a quarter of the time, massively reducing the time required for large surveys.

In the case of spectrometers increased bandwidth is equivalent to increased velocity coverage. That is, the shift in the rest frequency of atomic and molecular emissions due to Doppler shifts. For instance, the hydrogen emission in a rotating galaxy may manifest itself as two large peaks, centred around the mean velocity of recession, due to the line of sight concentration of mass of the two edges rotating towards and away from us, with a broad velocity spread in between. If the galaxy is rotating sufficiently fast, it may be impossible to fit the entire galaxy profile within the bandwidth available, making it impossible to establish a baseline for the emission. As observing frequencies move constantly higher the same fractional bandwidth implies a greater absolute bandwidth, so that objects of the same Doppler shift observed at higher frequencies require more absolute bandwidth for the same velocity coverage.

### 1.3 List of Contributions

In this thesis I will deal with the design, analysis, implementation and application of wide bandwidth signal processing components to all three of the areas of radio astronomy mentioned previously.

I will present the design and implementation of high speed three-level digitisers using an Indium Phosphide Heterojunction Bipolar Transistor (InP HBT) integrated circuit process. They are intended for use in autocorrelation spectrometers and crosscorrelation imaging systems. A detailed analysis of the performance limits of these designs is presented along with the solution to practical problems of packaging and system integration. These digitiser integrated circuits will be shown to operate at up to 10 giga-samples/s, significantly faster than other reported digitisers for radio astronomy, and one of these devices is integrated into a complete 4 giga-sample/s digitiser sys-

tem, along with required support hardware. This digitiser system has been installed at the Parkes radio observatory. A further novel photonic I/O digitiser is presented which contains an integrated photonic interface, which I believe is the first digitiser device reported with integrated photonic connectivity.

On the topic of wide bandwidth multipliers for analogue correlators, I will present the design and development of a 15 GHz bandwidth analogue multiplier IC in InP HBT technology and give a detailed noise analysis of multipliers in analogue correlators. This noise analysis will highlight the need for low noise back-end components in wide bandwidth systems, in contrast to the generally accepted wisdom at lower bandwidths. This will prompt the development of a further analogue multiplier IC in SiGe HBT technology which has the benefit of reduced low frequency noise, and which provides a better solution for analogue multipliers if problems of substrate loss can be overcome.

To push bandwidth capabilities further I will present a new photonic multiplier system and experimental results that confirm its operation. This photonic multiplier is capable of operating to greater bandwidths than semiconductor multipliers. A noise analysis of the photonic multiplier is provided. Finally, an application of photonic analogue-to-digital converters to radio astronomy digitisers is presented.



## Chapter 2

# High Speed Digitisers

A digitiser is the component in a radio astronomical receiving system that samples and quantises the down-converted radio frequency (RF) signal for subsequent digital processing. It is a type of analogue-to-digital converter (ADC) tailored to the requirements of astronomical signal processing. In this work I will use the term digitiser to refer to such devices in order to differentiate them from general purpose ADCs. Figure 2.1 shows a simplified diagram of the receiving chain in a typical radio telescope. The source of interest is observed using a collector of some kind, for example a large parabolic dish with a feedhorn. The collected signal is then amplified with a low noise amplifier (LNA), which is typically cooled to reduce electronic noise contributions. The received signal is then mixed down and amplified, through one or more stages, to somewhere near baseband to ease the operation frequency requirements of the following components. Many variations on the above simplified signal chain exist, for instance in the case of very high observing frequencies where adequate LNAs do not exist and the received signal is directly mixed down to a convenient IF using low noise, high frequency SIS mixers, but as this is not the central topic of this work I will not go into detail on the many types of receiver systems that exist. Once the bandwidth of interest has been mixed to near baseband then the signal is typically digitised, that is, converted to a digital representation that is then

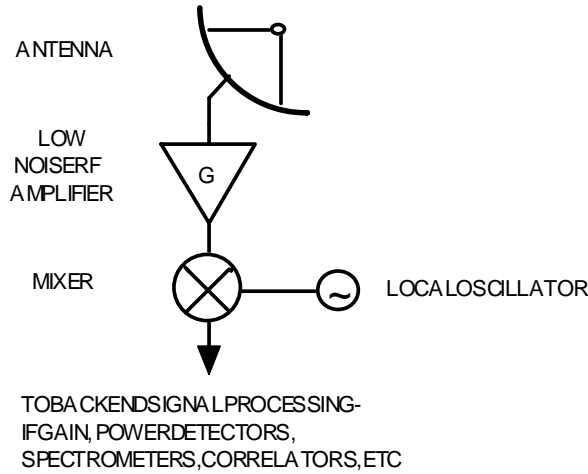


Figure 2.1: Simplified superheterodyne radio telescope receiver.

sent to a correlator or spectrometer of some type, depending on the exact instrument. The correlator is a special purpose instrument that measures the correlation function of two time varying signals supplied to its inputs. If the two signals are the same it forms the autocorrelation function, which can be inverted by virtue of the Wiener-Khinchine theorem, to give the spectrum of the input signal. The Wiener-Khinchine theorem states that the power spectral density and autocorrelation function of a stationary signal form a Fourier transform pair [3]. If the two signals are different the correlator measures the cross correlation function of the two inputs, which is the fundamental input data for interferometric synthesis imaging. This digital approach is used in almost all modern radio telescope spectrometers and correlators because of the advantages of stability, reproducibility and reliability of digital electronics, compared to analogue implementations, and the ease of varying the bandwidth by simple sample rate variation.

In the case of cross-correlators for interferometers, the order of the frequency transform and time multiplication can be reversed in the correlator with the two systems of different sequence of operations known as XF or FX



[4]. Either the XF or FX architecture will be more optimal in a particular situation depending on many parameters such as number of baselines to be processed, bandwidth and ability to remove interference. This work is presented from the point of view of XF systems as this is the scheme used in all existing Australia Telescope National Facility (ATNF) correlators. The digitisers developed can be used in either architecture.

Analogue spectrometers do exist and have been used extensively and successfully, for example, acousto-optic spectrometers [5], chirp transform spectrometers [6] and filterbank spectrometers. Analogue cross correlators also exist [7] and the core multiplying component for such an analogue cross correlator forms the subject of chapter 5 of this work.

The split between analogue and digital approaches is a function of the bandwidth. In accordance with the Nyquist criterion a digital correlator must sample at a rate of at least twice the bandwidth of the signal to not introduce aliasing and loss of information. As bandwidths become larger this implies the digitisers must work at very high sample rates. The correlator portion of the system can be implemented in parallel by slicing the input signals into contiguous time chunks, so that very high sample rates can be accommodated in the correlator by using many correlator elements in parallel. However, the digitiser must operate at the full sample rate and so is the limiting component in present correlator systems. It was for this reason that I decided to look at extending the current level of performance in radio astronomy digitisers.

It is also possible to deal with large bandwidths by splitting the input analogue signal into several contiguous frequency bands, by means of an analogue filterbank, and then processing each of these with a lower bandwidth correlator. Systems of this type are known as hybrid correlators and several such implementations exist and are in use. However, they are affected by calibration problems in attempting to reassemble the contiguous bands after correlation [8]. Hybrid correlators also result in more physical hardware for the same bandwidth so that correlators that can process as much integral bandwidth as possible are preferred.

## 2.1 The Use of Digitisers in Digital Correlators

The chief use of digitisers in radio astronomy is as the analogue-to-digital conversion element in auto and cross correlators for spectrometry and imaging [9, 10]. Their end use in this application defines the key parameters of the digitisers. Most notable, compared to the conventional communications applications of ADCs, is the small number of quantisation levels generally used. Radio astronomy signals are usually the result of broadband emission from an ensemble of many uncorrelated emitters and so the resulting radiation has the form of white noise. It can be shown that the true correlation function, and therefore the frequency spectrum, can be derived from the digital correlation function of coarsely quantised bandlimited gaussian signals, with the only penalty being a loss of S/N ratio [11]. For instance, using three-level quantisation delivers 0.81 of the S/N ratio of an unquantised measurement, while four-level (two bit) quantisation yields an efficiency of 0.88 [12]. The advantage is that the implementation of the following correlator elements, usually in the form of ASICs, is simpler with one or two bit samples. This in turn allows very fast correlator ASICs to be designed giving large bandwidth coverage in a single chip. For input sample streams  $x_i$  and  $y_i$ , which may be the same for an autocorrelation, the correlator ASIC performs the operation

$$R_n = \frac{1}{N} \sum_{i=1}^N x_i y_{n-i} \quad (2.1)$$

where  $N$  is the number of samples processed and the subscript  $n$  refers to the lag number.

The latest correlator ASICs achieve equivalent sample rates over 1 GHz with several hundred lags in the correlation function using 3-level [13] or 4-level [14] quantisation. Almost all correlator systems currently in use in radio astronomy facilities around the world are either two-, three- or four level systems. Figure 2.2 illustrates these quantisation schemes. All the

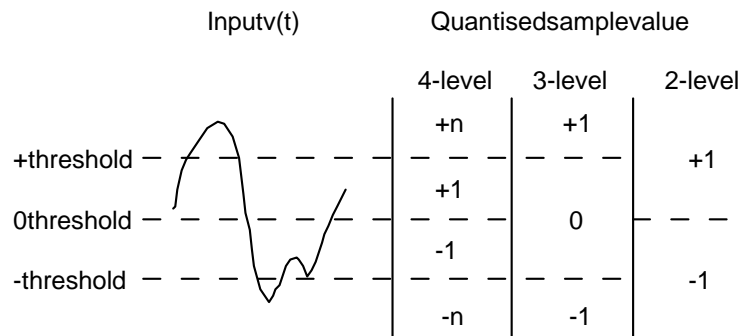


Figure 2.2: 2-,3- and 4-level quantisation schemes.

digitisers developed in this work are three-level to be compatible with the three-level correlator ICs available at the ATNF [15]. The digitiser ICs can be used with four-level correlators, if necessary, by replacing the zero state of the three-level representation with a zero mean pseudo-random sequence in the least significant bit (LSB) of the four-level representation. Of course this does not recover the extra S/N lost in doing three-level instead of four-level quantisation. The ICs can also be used with two-level correlators by simply driving the threshold levels to the centre of the common mode range and taking one or other of the output bits.

### 2.1.1 Coarse Digitisation Basics

The previous section mentioned that for band-limited white noise signals, the spectrum derived by a correlation approach using coarse quantisation leads to only a small loss in signal-to-noise ratio, compared to a non-quantised measurement. As this is a somewhat surprising result, which is unfamiliar to people working with non-stationary communications type signals, I will go into a little more detail to show how this is the case.

Consider quantising the received signal into three levels, as the digitisers in this thesis are designed to do. This can be achieved using two threshold levels placed symmetrically about the mean DC level of the signal. For the purposes of analysis, consider the signal mean is zero and the signal variance

is normalised to unity. Then, ignoring offset errors in the digitiser front-end, the threshold levels will be symmetrical about 0 of value  $+v$  and  $-v$ . The signal is quantised to value  $+1$  if the signal,  $S$ , is  $> +v$ ,  $0$  if the signal is between  $+v$  and  $-v$ , and  $-1$  if the signal is  $< -v$ , at the instant of strobing the digitiser. This quantisation rule is displayed in equation 2.2.

$$\text{Sample Value} = \begin{cases} 1 & S > v \\ 0 & -v \leq S \leq v \\ -1 & S < -v \end{cases} \quad (2.2)$$

Consider now two bandlimited white noise signals,  $x(t)$  and  $y(t)$ , which have a true correlation  $\rho$ . The joint distribution of the signal voltages can be modelled by the bivariate normal distribution function for stationary, white noise signals. The probability that at any instant  $\{x(t) \geq x, y(t) \geq y\}$  is given by the integral of the bivariate normal distribution function  $L(x, y, \rho)$  defined by

$$L(x, y, \rho) = \int_x^\infty \int_y^\infty \frac{1}{2\pi\sqrt{1-\rho^2}} e^{-\frac{1}{2} \frac{(x^2 - 2\rho\bar{x}\bar{y} + y^2)}{\sqrt{1-\rho^2}}} d\bar{x} d\bar{y}. \quad (2.3)$$

With three-level quantisation there are 9 possible states for the pair of sampled values of the two signals after quantisation. If we let the probability that the quantised samples are in state  $\{i, j\}$ , that is  $x(t)$  is quantised to  $i$  and  $y(t)$  is quantised to  $j$ , be given by  $P_{ij}$  where  $i, j \in \{-1, 0, 1\}$ , then the probabilities are defined by

$$\begin{aligned} P_{11} &= P_{-1-1} = L(v, v, \rho) \\ P_{01} &= P_{10} = L(-v, v, \rho) - L(v, v, \rho) \\ P_{-10} &= P_{0-1} = L(-v, -\infty, \rho) - L(v, -\infty, \rho) - L(-v, -v, \rho) + L(v, -v, \rho) \\ P_{-11} &= P_{1-1} = L(v, -\infty, \rho) - L(v, -v, \rho) \\ P_{00} &= L(-v, -v, \rho) - 2L(v, -v, \rho) + L(v, v, \rho). \end{aligned} \quad (2.4)$$

Using these, and some simplifications amongst the integral relations, the

expected mean value of the correlator output is

$$R(\rho) = \sum_i \sum_j ijP_{ij} = 2L(v, v, \rho) - 2L(v, v, -\rho). \quad (2.5)$$

The case of three-level quantisation leads to a fairly simple result since all of the products containing a multiplier of zero vanish. Nevertheless, in this case, as in general except for the simplest case of two-level quantisation, an analytic relationship between the correlation as measured  $R(\rho)$  and the true correlation  $\rho$  cannot be found. In order to correct the measured correlation to give the true correlation the previous expression can be inverted, usually in the form of a power series, and is applied to the measured correlation values prior to Fourier transforming to recover the spectrum. A detailed analysis of the previous result and inversion expressions over various ranges of validity can be found in [16].

To quantify the effect on signal-to-noise ratio of the quantising process we can note that the correlator usually operates with signals of low correlation. This allows several simplifications to be made. The variance of the correlator measurement given in equation 2.1 is

$$\sigma_R^2 = E\{R^2\} - E\{R\}^2, \quad (2.6)$$

where  $E\{ \}$  is the expectation. In the limit as the correlation approaches zero the second term approaches zero and the two processes,  $x(t)$  and  $y(t)$ , become independent. Under these conditions and with Nyquist sampling so that successive samples are uncorrelated the expression for the variance reduces to

$$\begin{aligned} \sigma_R^2 &= E \left\{ \frac{1}{N^2} \sum_{i=1}^N \sum_{j=1}^N x_i y_i x_j y_j \right\} \\ &= \frac{1}{N^2} \sum_{i=1}^N E \{ x_i^2 y_i^2 \} \\ &= \frac{1}{N} E \{ x_i^2 \} E \{ y_i^2 \} \end{aligned} \quad (2.7)$$

Hence the signal-to-noise ratio of the correlator measurement is

$$\left( \frac{S}{N} \right) = \frac{R\sqrt{N}}{\sqrt{E \{ x_i^2 \} E \{ y_i^2 \}}} \quad \rho \ll 1. \quad (2.8)$$

For the ideal case with no quantization this becomes

$$\left(\frac{S}{N}\right)_{ideal} = \rho\sqrt{N} \quad \rho \ll 1. \quad (2.9)$$

Thus, the efficiency of the correlator is

$$\eta = \frac{(S/N)_{quantized}}{(S/N)_{ideal}} = \frac{R(\rho)}{\rho\sqrt{E\{x_i^2\}E\{y_i^2\}}} \quad \rho \ll 1. \quad (2.10)$$

On using a first order in  $\rho$  approximation to the integral of the bivariate normal distribution function,

$$L(h, k, \rho) \approx \frac{1}{4} \operatorname{erfc}(h/\sqrt{2}) \operatorname{erfc}(k/\sqrt{2}) + \frac{\rho}{2\pi} e^{-\frac{1}{2}h^2} e^{-\frac{1}{2}k^2}, \quad (2.11)$$

in the expression for  $R(\rho)$  in equation 2.5, gives for the efficiency for three-level quantisation

$$\eta_{threelevel} = \frac{2e^{-v^2}}{\pi \operatorname{erfc}(\frac{v}{\sqrt{2}})}. \quad (2.12)$$

This expression is a maximum for  $v = 0.612$ , with a value of 0.81, at which point 27% of samples are in the +1 state, 27% of samples are in the -1 state, and 46% of samples are in the 0 state. This is the optimum point for three-level quantisation and is the usual operating point of the digitiser. Similar results can be derived for slightly different schemes such as two or four level quantisation [12, 17, 18] and for correlator schemes which incorporate digital mixers for VLBI processing [19].

## 2.2 Current Digitisers for Radio Astronomy

The current state of the art in wide bandwidth digitisers for radio astronomy lies at approximately two giga-samples/s sampling rate. The widest bandwidth digitisers currently in use are the 1.6 giga-samples/s system deployed on the Green Bank Telescope in West Virginia designed at the National Radio Astronomy Observatory (NRAO) in Charlottesville, USA; the 2.0 giga-sample/s system designed by the Max Plank Institute für Radio Astronomy (MPIFR) in Bonn, Germany [20]; the 2.048 giga-samples/s system deployed

on the Swedish-ESO Submillimetre Telescope (SEST) in Chile designed by the author at the Australia Telescope National Facility (ATNF) [21], and the 2.048 giga-samples/s system deployed on the Nobeyama Millimetre Array designed by NTT Electronics Technology Co. [22].

The first three of these systems are based on a hybrid design approach. That is, they use individually packaged silicon-based devices assembled onto various types of microwave laminate and conventional printed circuit board (PCB). This is about the practical limit for this type of technology. There are several problems with this approach such as the bandwidth-limiting parasitics inherent in packaged devices, the problems of very high speed interconnect, the matching limitations of individually packaged components and performance degradation due to poor temperature tracking. All of these problems can be effectively dealt with by the use of integrated circuit technology.

The first integrated circuit digitiser IC for radio astronomy was the 2 bit digitiser device developed for the Nobeyama Radio Observatory in Japan by NTT Electronics Technology Co. [22]. This is a GaAs device which was designed for a sampling rate of 2.048 GHz. There was a problem with this device in that there was on-chip crosstalk between the clock and data which corrupts the digitised data to some extent, but they manage to use the devices by control of the input level [23]. The new digitisers for the Japanese 1-GBPS VLBI system do not use these devices. Instead, they have contracted the manufacturer of the Sony-Tektronix TDS784 high speed oscilloscope to modify their oscilloscope front-end to allow it to be used as a 1.024 giga-samples/s two-bit digitiser [24]. Recent work by Japanese groups has focussed on developing a high speed digitiser using individually packaged high speed GaAs decision circuit ICs, as used in fibre optic data transmission receivers, and packaged GaAs demultiplexer ICs [25]. They currently have performed tests on a one-bit prototype board and produced a 1 GHz bandwidth spectrum. Their two-bit system is constructed by splitting the input signal and sending it to three of the one-bit boards in parallel, with appropriate threshold level settings for the decision circuits. In this system

achieving delay and bandpass matching would be very challenging. They mention that their next step is to move on to developing a dedicated digitiser integrated circuit.

Recently, the French team composed of groups from the Observatoire de Bordeaux, Université de Bordeaux and the Université de Grenoble have been pursuing an effort to design two and three bit digitiser ICs [26] as part of the technology effort for the Atacama Large Millimetre Array (ALMA), a large international project to build a millimetre wave array in the Atacama desert in Chile. They are using a SiGe BiCMOS process well suited for digitiser development. To date they have fabricated their first two generations of devices and presented results for their three-level device in a prototype setup which shows good performance to 5 giga-samples/s sampling rate [27]. Their digitisers have no on-chip demultiplexer and the full data rate from the flash converter is demultiplexed to a slower rate using a set of external commercial GaAs demultiplexer ICs.

## 2.3 Choice of InP-based Technology

There are several available semiconductor technologies that could be considered for implementing digitiser ICs. These include Si CMOS and BJT, GaAs HEMT and HBT, InP HEMT and HBT and SiGe HBT. Of all these semiconductor processes InP has the fastest intrinsic transistors in both HEMTs and HBTs. This is due principally to the much higher electron mobility in InP and InGaAs, of which transistors are composed in the InP material system. InGaAs has approximately 1.6 times the mobility of GaAs and 9 times the mobility of Si.

HEMT devices are unsuitable for implementing the digitiser because they lack the across wafer device matching needed for circuits with many hundreds of transistors. This is a result of the fact that the pinch-off voltage in HEMTs is a function of the device geometry, defined by lithography and etching, where as the equivalent turn-on voltage for bipolar devices is a function



purely of the semiconductor material used.

GaAs and InP based processes have a strong advantage for high frequency circuits because the substrates are insulating, in combination with a backside Au ground plane and low inductance vias to ground. This allows the design of low loss and highly stable microwave circuits with well defined impedances in microstrip or conductor-backed coplanar waveguide. In contrast conventional silicon processes use a conductive silicon substrate, which has to be negatively biased, and have no backside ground plane or vias. The dielectric losses in the silicon combined with the device-to-substrate capacitance of the biased substrate lead to much greater losses, especially at higher frequencies. There are techniques such as silicon on insulator and high resistivity substrates designed to ameliorate these problems but they still do not give performance as good as the insulating substrates of GaAs and InP. The conductive silicon substrate, and considerable device-to-substrate capacitance of silicon processes, also leads to much greater signal coupling from digital nodes to sensitive analogue nodes in mixed signal designs. The digitiser devices reported previously in [27] for example contain no demultiplexer on chip, possibly because of concerns of coupling from the digital demultiplexer to the analogue portion of the chip.

SiGe HBT is a promising technology for new applications. By incorporating germanium into the base, a heterojunction bipolar transistor is formed that uses most of the process steps and manufacturing infrastructure of standard silicon processes, but with much greater speed [28]. The latest SiGe processes rival InP in performance, albeit with much smaller transistor dimensions [29, 30]. The SiGe processes still suffer from the additional losses due to the conducting silicon substrate. Nevertheless, SiGe is attractive since it offers a high speed process combined with the low-cost high-volume manufacturing of the silicon semiconductor industry.

In all, the InP process offers the best combination of desirable properties for implementing the digitisers, and was the only available process at the time of beginning this project in 1998 that was sufficiently fast to meet the

speed goal of 8 giga-samples/s conversion rate. The InP HBT process used was provided by TRW Corporation, Redondo Beach, California (this division has now become Velocium) and is described in [31]. This is a single heterojunction bipolar transistor process based on an InGaAs/InGaAs/InAlAs transistor structure for the collector, base and emitter respectively, grown with molecular beam epitaxy (MBE) on 3-inch semi-insulating InP wafers. The process has peak  $f_T$ s of approximately 70 GHz, DC current gain ( $\beta$ ) of approximately 25 and breakdown voltages of  $BV_{ceo} \approx 8V$  and  $BV_{cbo} \approx 13V$ . InGaAs p-i-n photodiodes sensitive to 1.3-1.55  $\mu\text{m}$  light are also incorporated on wafer for opto-electronic applications. This was a non-commercial process with access enabled through a special collaborative agreement between the CSIRO and TRW. Radio astronomy provides a non-commercial, non-military application that benchmarks TRW's advanced process capabilities without commercial risk, and with the freedom to publicise results.

## 2.4 Digitisers and ADCs

The digitisers presented in this work and general analogue-to-digital converters clearly have much in common. The digitisers presented here are essentially low resolution ADCs optimised for speed and for the processing of the types of signals found in radio astronomy.

It is useful to look briefly at the characteristics of general ADCs and in particular some of their performance metrics. Whilst these are generally not directly applicable to the digitisers, they provide the standard means of comparison amongst ADCs in the literature, and will be used later in this work to place upper bounds on error mechanisms.

A fundamental property of an ADC is the number of bits,  $B$ , of the digital representation it produces, and correspondingly, the number of quantisation levels,  $N$ . These are related by  $N = 2^B$ . Given the number of bits the most important property of the ADC is its signal-to-noise ratio (SNR). This is conventionally derived based upon a sine wave input. This derivation can

be found in any standard text on ADCs or digital communications [3]. A simple derivation will be presented to highlight the assumptions that set ADCs apart from the digitisers in this work.

The input to the ADC is a full scale sine wave of amplitude  $V$ . Despite this, it is assumed that the input is uniformly distributed across all the quantisation levels. This is a reasonable approximation when the number of quantisation levels is large. Given this assumption, the quantisation error, that is the error between the true signal and the quantised signal, is uniformly distributed across each quantisation level. If the quantisation level is of width  $\delta$  and the sample value is considered to be the centre of the quantisation level then the quantisation error,  $e$ , is uniformly distributed between  $-\frac{\delta}{2}$  and  $\frac{\delta}{2}$  with a density of  $\frac{1}{\delta}$ . There is an implicit assumption that the quantisation error is uncorrelated with the input signal. Given these definitions the expected error power due to quantisation is

$$E(e^2) = \int_{-\frac{\delta}{2}}^{\frac{\delta}{2}} e^2 \frac{1}{\delta} de. \quad (2.13)$$

Performing the integration and noting that  $\delta$  and  $B$  are related by

$$\delta = \frac{2V}{2^B}, \quad (2.14)$$

and that the sine wave rms power is  $\frac{V^2}{2}$ , gives the well known relation for SNR in db

$$SNR_{adc} = 6.02B + 1.76 \text{ dB}. \quad (2.15)$$

This relation gives the theoretical maximum SNR that can be achieved. This relation is often inverted when evaluating ADCs in practice so that a SNR, or signal-to-noise-plus-distortion ratio (SNDR) including harmonics, is measured from digitised data and from this an effective number of bits derived.

In the case of low resolution digitisers the assumptions implicit in the result of equation 2.15 are not valid. The received signal is normally distributed and the quantisation error is strongly correlated with the signal. In the case of two-level quantisation the signal and quantisation error are

essentially the same. For three-level quantisers the signal and quantisation error are still strongly correlated. The methods of section 2.1.1 are then the appropriate formalism for analysing the performance of systems using such quantisers.

Likewise, SNDR measurements for low resolution digitisers are not meaningful. The conventional SFDR of a low resolution digitiser is poor. These systems, however, are not designed for processing discrete tones, but for processing signals with predominantly noise like character.

# Chapter 3

## InP Digitiser Designs

The goal of the digitiser research was to realise a range of two-bit three-level digitisers that were capable of full Nyquist sampling at up to 8 gigasamples/s.

The digitisers were designed using an all-parallel "flash" architecture because this provides the highest sample rate of all ADC architectures [32]. In this architecture the input signal is sent to a set of comparators in parallel,  $2^n - 1$  for an  $n$  bit digitiser, with appropriate threshold settings for each of the comparators. For the three-level digitisers developed two comparators are required.

The process of digitisation involves two steps, sampling and quantisation. Sampling is taking a snapshot of a signal at a particular instant. Quantisation classifies a signal into one of a discrete set of states. These operations may be performed in either order. It is common with moderate to high precision ADCs to employ a sample-and-hold circuit before the quantiser so as to provide non-slewing samples in time. This is mandatory for ADC architectures that use feedback, such as successive approximation and folding/interpolating architectures, but is also often used with flash converters to overcome problems with input capacitance from the parallel bank of comparators, and limitations in being able to equalise the wire lengths and delays to each of the comparators. The digitisers designed in this chapter contain

no sample-and-hold as they contain few comparators, and the process was not well suited for realising low distortion sample-and-holds on chip. Instead, clocked comparators with matched delays are used to perform both the sampling and quantisation. Implications of this decision are treated in section 3.3.3 on error mechanisms.

The digitiser ICs were designed using a combination of emitter coupled logic (ECL) and current mode logic (CML) transistor circuit topologies, as these are well known to provide the fastest operation in bipolar technologies, due to nonsaturating operation, along with good noise immunity and ability to operate fully differentially [33, 34, 35, 36]. ECL and CML are based upon stacked emitter-coupled pair differential amplifiers as their basic logic elements. See for example [37] for a thorough treatment of ECL and CML and their use in bipolar VLSI circuits.

### 3.1 Summary of Designs

Three digitiser integrated circuits were designed and implemented:

1) **A digitiser/demultiplexer.** This is a two-bit/three-level flash converter with dual post converter 1-4 serial/parallel converters to reduce the output data rate to  $\simeq 2$  Gbits/s. The demultiplexed data is then at a sample rate where commercially available ECL logic can be used for processing the signals. Without the integrated demultiplexers external demultiplexer chips would have to be designed. Although fast demultiplexers for the OC-192 optical data transmission standard (10Gb/s) are available [38], these are single bit demultiplexers where there is a synchronisation problem in getting the phase of the  $1/n$  dividers of multiple demultiplexers aligned. This can be overcome, but at higher complexity and cost than an integrated demultiplexer. See [39] for one particular solution.

2) **A digitiser without integrated demultiplexer.** This design was included chiefly as a back up option in case the yield of the process was low, in which case the previous design, with six times as many transistors as the

digitiser without demultiplexer, may not have yielded any working circuits.

3) **A photonic I/O digitiser.** This is a novel two-bit/three-level digitiser with the sampling clock delivered by fibre and received by an on-chip photodiode and transimpedance amplifier. The design also has current-switching output buffers which can be used to directly modulate an externally bonded LED, laser diode or optical intensity modulator. This allows a purely optically connected digitiser for remote antenna applications with low self-generated radio frequency interference (RFI).

## 3.2 Fundamental Design Parameters

I will now discuss some of the fundamental optimisations and design decisions that effect all of the circuits to follow, such as device sizing, device currents, choice of supply voltage, internal signal swings and limitations on the input signal voltage.

### 3.2.1 Device Sizing

Transistors are available in the InP HBT process in a variety of emitter widths and lengths. Fastest device operation is achieved with the narrowest base width, as this minimises the base transit time. The process used offers a minimum base width of 1.5  $\mu\text{m}$ , so devices of 1.5  $\mu\text{m}$  base width were used in all designs. A large selection of emitter lengths was available as well as devices with multiple emitters. The majority of transistors in the digitisers were minimum size single emitter transistors, with this decision made largely on the basis of power dissipation. The speed of the transistors is governed by the collector current density - A transistor of twice the emitter length requires twice the collector current to maintain the same emitter current density, and hence maintain the speed. This leads to twice the total power dissipation of the device. For integrated circuits with many hundreds to thousands of transistors it is imperative to reduce the device dissipation [40]. Larger

devices are used as appropriate, for example, in the clock driver circuits and output driver circuits which must drive high load currents at high bandwidth. The choice of device for each of these sub-circuits is dealt with in more detail in the relevant section.

### 3.2.2 Signal Swing

One important question is what internal voltage swings should be used in the circuits. The larger the voltage swing the longer the internal nodes take to reach valid logic levels, and the longer it takes internal nodes to slew from one full scale state to the other. The power dissipated in internal capacitive parasitics is also higher. It is clear that the internal voltage swings should be as low as possible consistent with reliable operation. An emitter-coupled pair differential amplifier has a differential output voltage as a function of differential input voltage given by [41]

$$V_{out} = I_{EE} R_C \tanh\left(\frac{V_{in}}{2V_T}\right) \quad (3.1)$$

where  $I_{EE}$  is the tail current,  $R_C$  the collector load resistance and  $V_T$  is the thermal voltage. The output will almost fully switch from  $I_{EE} R_C$  to  $-I_{EE} R_C$  with an input differential voltage swing of only 3 or 4  $V_T$ . At room temperature this implies a peak to peak input signal swing of 100 mV is required. Considering the circuit may have to operate at up to 150 C, and the thermal voltage increases accordingly, this becomes 140 mV. The parasitic emitter resistance of the minimum size HBTs leads to an additional loss of about 50 mV at the design current density. Thus, an input signal swing of 190 mV worst case over temperature is indicated. Allowing for process variations, offsets and imbalances by a 20% margin, a nominal signal swing of 230mV was chosen for the internal circuit nodes.



### 3.2.3 Bias Current

The speed of operation of InP single heterojunction bipolar transistors, in terms of  $f_t$  and  $f_{max}$ , increases with collector current until the device enters the region of unsafe power dissipation. This is in contrast with conventional BJTs, which reach a definite peak before they reach their maximum dissipation level, because of effective base widening as a result of the Kirk, or base push out, effect [41]. Thus, for maximum speed we must ideally bias the transistors at the highest current that is consistent with safe operation of the device and total power dissipation constraints of the chip. The minimum size transistors have a maximum emitter current of approximately 2.0 mA. A safe current which allows for process variations and increase of current source output with temperature is 1.6 mA. As will be mentioned in section 3.3.8, all the digitiser ICs have an external pad that allows the bias current for all transistors to be varied above or below this nominal value by application of an external voltage.

### 3.2.4 Supply Voltage

In order to reduce power dissipation in the circuit, it is clear that the supply voltage should be kept as low as possible. The minimum supply for a two stacked transistor configuration (the other sub-circuits on the chip are also at most two level stacked), which prevents the current source going into saturation, is

$$V_{ee}(min) = 3V_{be} + V_{ce} + V_{rcs}, \quad (3.2)$$

where  $V_{be}$  is the base emitter voltage,  $V_{ce}$  is the transistor saturation voltage and  $V_{rcs}$  is the voltage drop across the current source resistor. Taking typical values of  $V_{be} = 0.8V$ ,  $V_{ce} = 0.3V$  and  $V_{rcs} = 0.3V$ , this gives a minimum supply voltage of 3.0V. A reasonable choice for supply voltage which allows for process variations, and provides greater input common mode range, is 3.5V. This is referred to as VEE in the circuit schematics to follow. The upper rail voltage, referred to as VCC in the circuit schematics, was chosen

to be ground. This was done for a few reasons. Firstly, the process uses a backside ground plane with low inductance vias to provide solid ground connections. Using this for one of the voltage rails allows simple connection to the rail using backside vias, without having to route another power rail to all the devices on the chip. This is very useful considering the process offers two metal layers for all signal and power connections. Secondly, with the differential amplifier based logic used in the design, noise coupled through the negative rail is rejected by the differential amplifier, whilst noise coming through the upper rail adds directly to the output voltage. It is much easier to keep ground clean, so it is prudent to use this as the upper voltage rail. This is the reason that commercial ECL logic conventionally uses an upper rail voltage of ground [42]. Thirdly, this choice makes the outputs of the IC directly compatible with commercial ECL logic which is used for further processing of the digitised data.

### 3.2.5 Input Common Mode Range

The input common mode range, for the comparator cell to be presented in 3.3.1, is limited in the positive direction by ground, assuming the positive rail is at ground potential, and in the negative direction by preventing current source saturation, so that

$$V_{ee} + (2V_{be} + V_{ce} + V_{rcs}) \leq V_{in} \leq 0. \quad (3.3)$$

Using the transistor parameters in the previous section, and a supply voltage of -3.5 V, this gives a common mode range of 1.3 V extending from 0 to -1.3 V. For an input biased about -0.65 V this sets the maximum input level for a sine wave source as 1.3 V peak-to-peak or +6 dBm, or for a Gaussian distributed source, taking an effective crest factor of 5, of 0.13 V rms or -4 dBm.

### 3.3 Digitiser/Demultiplexer

Having presented the common fundamental design decisions in the previous section, I will now move on to the detailed design and analysis of each of the digitisers that were produced. For each of the designs I will present a top level functional description of the circuit, followed by in-depth design and analysis of the sub-circuits from which the designs are composed. Some of the sub-circuits are reused in multiple designs. For instance, the same optimised comparator block is used in all the circuits, so the analysis of these common blocks will be presented in the first circuit in which they were used.

The high-level block diagram of the digitiser/demultiplexer is presented in figure 3.1. The digitiser/demultiplexer is composed of comparators, de-

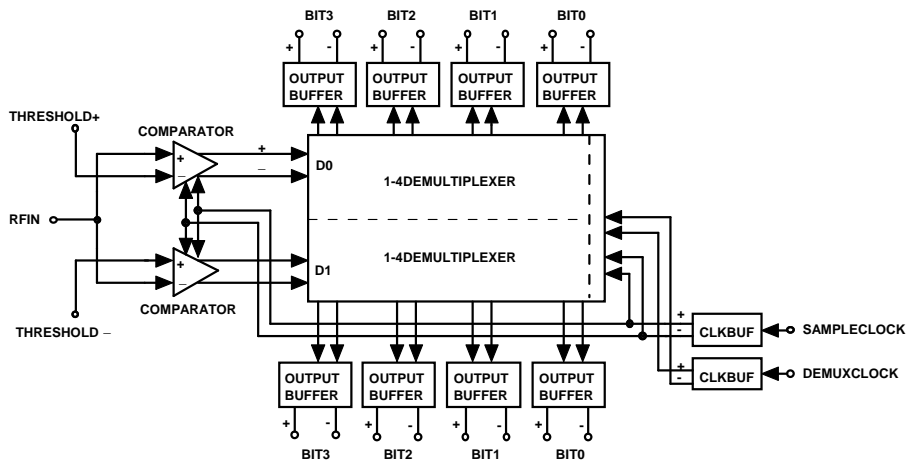


Figure 3.1: Digitiser/Demultiplexer block diagram.

multiplexers, a clock buffer, output buffers and a current control block. This design, as with all the designs, was designed and laid out using the Libra Series IV microwave design package from Agilent EESOF. All connections were hand routed. The design was hierarchical, reflecting that of the block diagram, so that common cells were laid out once only and repeated where necessary and the required interconnections put in place. The layout and simulation is an iterative process as the simulation requires knowledge of the layout for correct simulation of the interconnects and parasitics. The process

is then iterated, with the simulations refined in light of the current layout, until they converge.

### 3.3.1 Comparator

The basic element on which a flash converter is based is the voltage comparator. This is the device which performs the comparison between the input signal and a supplied threshold level, and outputs one of two digital states, "1" or "0", depending on whether the input signal is greater than threshold or otherwise. The performance of its constituent comparators is what ultimately sets the performance level of the overall digitiser, so this block is in many ways the most critical block in the digitisers, and the block which requires the most detailed analysis.

The circuit of the clocked comparator that was designed is illustrated in figure 3.2. This is based upon comparator designs presented in [43, 44, 45]. The input transistors Q1, Q2 serve to buffer the input signals and provide a relatively constant input bias current. They also prevent the following differential preamplifier Q3, Q4 from going into saturation, as the bases of Q3, Q4 are always at least a diode drop below the upper rail, ground in this case. The first preamplifier composed of Q3, Q4 serves to increase the front end gain, so enhancing the comparators response and recovery times and reducing metastability as the threshold region is traversed quicker. It also reduces clock kickback propagated to the inputs when the CLK switches. Q7-Q14 form a second preamplifier and regenerative latch. When CLKP is high and CLKN is low the preamplifier is enabled and the output tracks and amplifies the voltage difference at the input, acting as a high gain amplifier. Note that the amplifier does not have to be linear. The comparator is simply a polarity sampling device and the overriding concern is speed. This means that fast open loop configurations as in the schematic are called for.

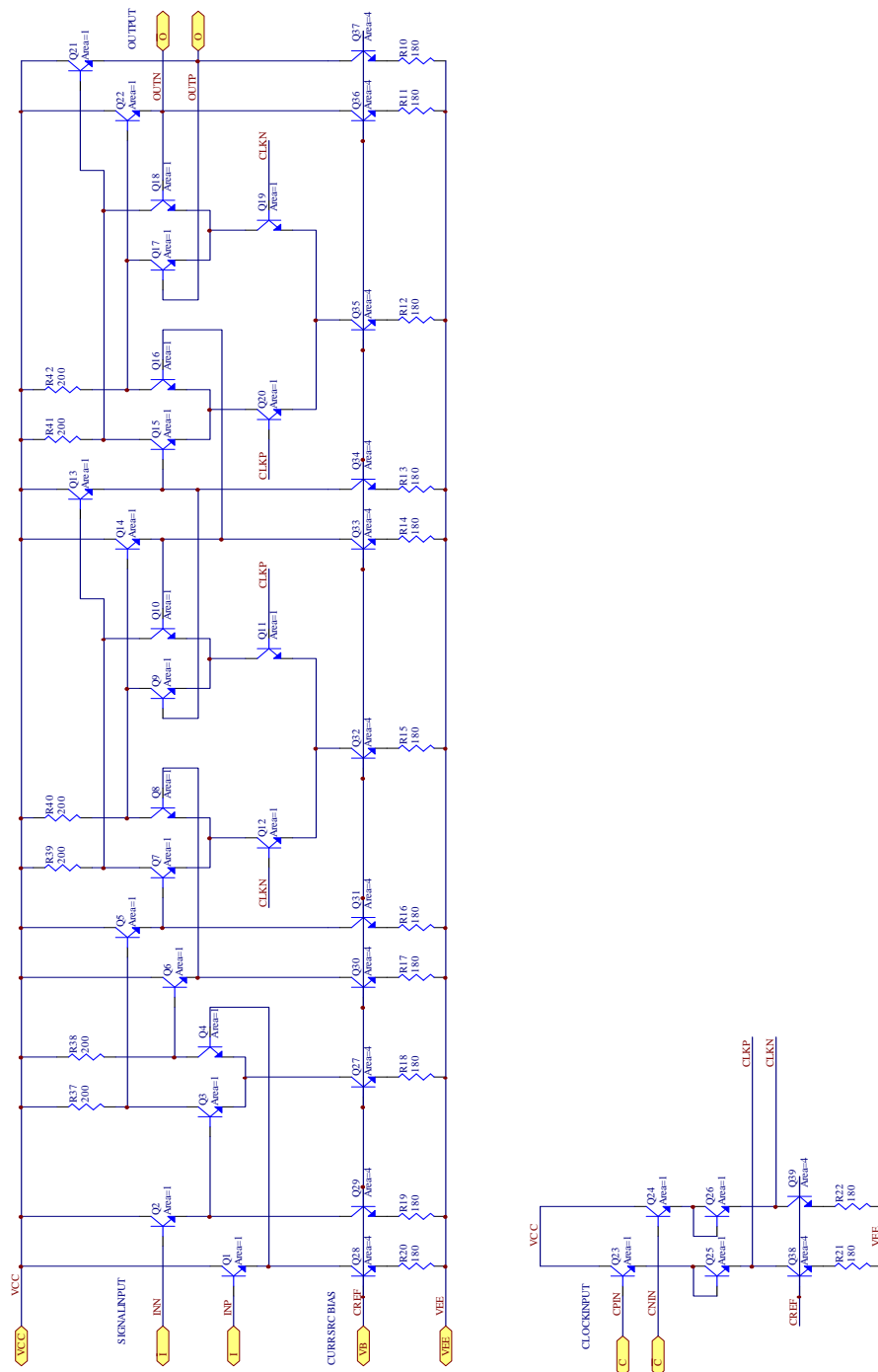


Figure 3.2: Schematic of comparator.

As the clock is switched the latch composed of Q9,Q10,Q13,Q14 is enabled and the positive feedback serves to amplify the voltage difference present at the collectors of Q7,Q8 at the moment of switching, and hold this level until the CLK is asserted again. The output emitter followers serve to enhance the regeneration rate of the latch slightly, provide a low impedance current drive for the following stages and level shift the signal to be compatible with the differential amplifier inputs of the following stage. Q15-Q22 form a second slave latch which operates in anti-phase to the first latch. This slave latch increases the regeneration time available, leading to less probability of metastable states, and also ensures the final output of the comparator is stable for a full clock cycle, instead of tracking for half the clock period. This is the usual master-slave flip-flop arrangement and gives the following logic twice the setup time for more reliable operation. Also included on the schematic is a local level shifting cell which shifts the level of the external clock inputs down two diode drops to put them at the correct DC level for the CLKP and CLKN inputs. The reason for including the level shifting cell in each comparator will be explained in section 3.3.6.

### 3.3.2 Comparator Dynamic Performance

The key performance parameter of a comparator is the ultimate comparison rate that can be achieved. This is the fastest rate at which the comparator can be clocked and correctly respond to the polarity of the signal at its input. There are several aspects that have to be considered:

The first is the recovery rate of the comparator. This is the rate at which the comparator's preamplifiers can slew from one state to a point in the other state where the logic level will be correctly interpreted. This is dependent on the gain of the preamplifiers, their bandwidth, the size of the full scale swing, the load resistance, and parasitic resistances and capacitances. The comparator cannot be strobed at a period less than it takes the comparator to slew unambiguously between states.

The second is the regeneration time constant of the latch. When the latch is strobed the differential voltage difference at its inputs is regenerated by positive feedback to full logic levels. The comparator cannot be strobed at a period smaller than required for valid logic levels to be attained. The regeneration time is dependent upon the same parameters as for the recovery rate, and also upon the differential voltage difference at the latch inputs at the time of strobing. An important implication of this is that for any given clocking rate, there will always be a minimum differential voltage that is needed to fully switch the output state of the clocked comparator.

### Recovery Rate

To examine the recovery rate of the comparator consider the differential pair preamplifier composed of Q1-Q4. If we were to do a small signal analysis of this circuit we would find that, using a single pole approximation, the frequency response would roll off with a 3dB point  $\omega_\tau$ , or alternatively the circuit has a characteristic time constant  $\tau_0 = 1/2\pi\omega_\tau$ . Then the small signal response can be approximated as

$$\frac{V_{out}}{V_{in}} = \frac{-g_m R_L}{1 + j\omega_\tau}. \quad (3.4)$$

Here  $-g_m R_L$  is the usual low frequency gain involving the transconductance  $g_m$ , and the load resistance  $R_L$ . The time constant of the circuit is dependent on the collector current  $I_C$ , intrinsic forward base transit time, various junction capacitances and resistances, the load resistance and the parasitic load capacitances. In general, it is therefore a very complicated expression, though in various regimes it can be simplified. For instance, if the load capacitance is high the circuit response is dependent only on the load. In the case at hand though, this is not true, and the best way to proceed is through simulation.

To estimate the performance of the comparator in a worst case situation, the comparator can be analysed in the condition where the input is at full scale in one direction,  $V_{fs}$ , and subsequently has to respond to a small in-

stantaneous differential input,  $V_d$ , in the other direction. This is known as an overdrive recovery test [46]. The circuit response using the small signal response of equation 3.4 will be an exponential slew to the opposite polarity. This is very approximate, as  $g_m$  and  $\tau_0$  depend on the collector current and bias voltages, which are constantly varying. The  $g_m$ , for instance, can vary anywhere between  $I_c/V_T$  and almost zero in each transistor, depending upon the input signal. In addition, the response to a pulse cannot be regarded as small signal. The full comparator circuit of figure 3.2 has two stages of pre-amplification, so that the overall DC gain is squared, and the time constant doubled, compared to a single preamplifier. Using the nominal SPICE models provided, and examining the response to the situation described above where the input differential slews from full scale positive to a small negative value, gives the typical response illustrated in figure 3.3. Defining the recovery time by the time from application of the small voltage difference (0 ps in figure 3.3) until the output responses cross, indicating a change of polarity, gives an indication of the performance of the comparator in this worst case condition. For a full-scale Gaussian-distributed input, full scale

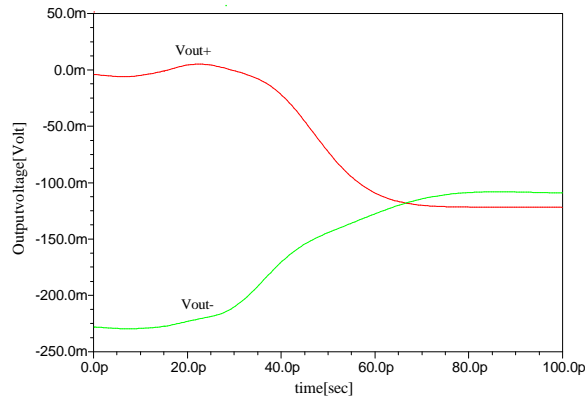


Figure 3.3: Typical comparator overdrive response.

is approximately four times the standard deviation. For a rms input level of 130 mV, determined earlier, this implies a full scale of 520mV. This is taken as full scale for the simulation. The voltage to which the comparator input is



subsequently driven is known as the overdrive. As the overdrive is increased, the recovery time decreases, since in the small differential input range the preamplifiers are simply acting as linear amplifiers, and so the slew rate is proportional to the input voltage difference. Figure 3.4 gives the results of simulating the comparator recovery time as a function of overdrive, given the initial condition that the comparator is currently in opposite polarity full scale. This is a very demanding test and can be regarded as a worst case operation of the device. It can be seen that even for a very small overdrive of only 1 mV, figure 3.4 implies an ability to operate at a rate greater than 16 giga-samples/s. For applications where the overdrive is large, for example re-timing optically transmitted data in a decision circuit, figure 3.4 implies an ability to operate at greater than 33 giga-samples/s.

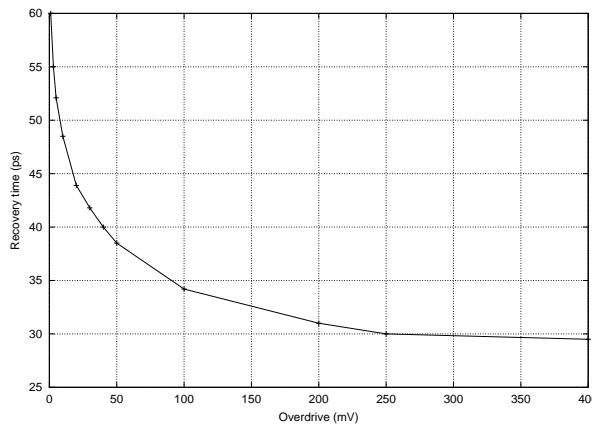


Figure 3.4: Comparator recovery time.

### Regeneration Time

The output differential voltage produced by the preamplifier circuit dealt with in the previous section has to be latched and regenerated to valid logic levels by the latch portion of the comparator. Quite often, the differential input to the latch will be very small at the moment of strobing, if the overdrive at that instant is small. The time required for a small input to be regenerated by positive feedback to valid logic levels is, thus, another constraint on

the maximum operation speed of the comparator.

The point to which the levels need to regenerate to be correctly determined is not clear. As mentioned previously, a differential amplifier will almost fully switch with a  $3V_t$  input voltage differential. So considering the amplification that will follow the latch when the signal enters the next latch or logic element, an output level of  $3V_t$  will almost certainly give correct operation. Taking this as the criterion, the regeneration time of the latch as a function of the input differential present at the instant of strobing can be derived from simulation. The results are presented in figure 3.5.

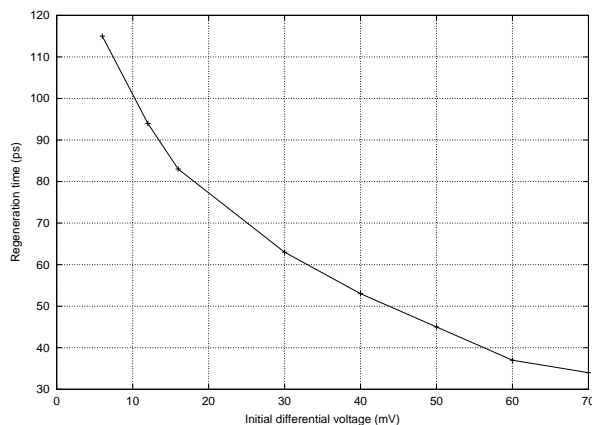


Figure 3.5: Comparator regeneration time.

This graph indicates that to operate at say 10 giga-samples/s (corresponding to 100 ps regeneration time), then at least 10 mV differential input voltage is required at the instant of switching. It is impossible to avoid falling in the uncertainty region some of the time, since there is always a finite probability of the input differential voltage lying in the uncertainty region. Hence the performance achievable is dependent upon the error rate that can be tolerated. Considering the case of a 10GHz clock rate again we can make an estimate of the error rate. If for the time being the slew rate limitation of the input preamplifiers is neglected, and they are considered to be working in their linear region when the difference between the threshold value and the input is small, then they have a gain of  $(g_m R_L)^2 = 80$ . Thus, to have an

input differential voltage of 10mV at the input to the latch requires an input differential voltage of  $10/80 = 0.125 \text{ mV}$  at the input to the comparator. The input signal is normally distributed with a variance,  $\sigma$ , of 130 mV at full scale input, as derived earlier. In normal operation, the threshold levels are held at  $0.612 \sigma$  (section 2.1), so that the probability density at this point is given by the normal distribution probability distribution function (PDF),

$$Z(x) = \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{x^2}{2\sigma^2}}, \quad (3.5)$$

evaluated at  $x = 0.612 \sigma$ . From this, the probability that the signal lies in the uncertainty region is approximately  $2.6 \times 10^{-4}$ . For a sample rate of 20 GS/s the probability of error increases to  $9.5 \times 10^{-4}$ .

The above figures are pessimistic. Even if the output voltage differential does not reach  $3V_T$ , the gain in the preamplifier and regeneration in the latch of the following logic stage will aid in achieving correct operation. This is the function of the slave latch in figure 3.2 - it amplifies the regenerated voltage in the master latch and effectively doubles, to a first approximation, the regeneration time available, thus greatly reducing the probability of metastable states. It also has the property that the output from the slave latch is in hold for almost a full clock cycle, instead of tracking for half the clock cycle, giving the following logic twice the setup time.

To get some estimate of the improvement in error rate provided by the slave latch, consider an ideal latch. An ideal latch composed of two amplifiers in positive feedback has output voltage, as a function of time, expressed by [46, 47]

$$V_{out} = V_{in} e^{\frac{A-1}{\tau}t}, \quad (3.6)$$

where  $A$  and  $\tau$  are the gain and characteristic time constant of the amplifier and  $V_{in}$  the applied input voltage. Fixing the output voltage at  $V_0$  and expressing  $t$  as a function of  $V_{in}$  gives

$$t = \frac{\tau}{A-1} \ln\left(\frac{V_0}{V_{in}}\right). \quad (3.7)$$

This is the ideal relationship for the simulation data displayed in figure 3.5. In reality, the gain and time constant are constantly changing as the collector current and junction voltages vary in the real latch. Fitting the data of figure 3.5 to this relationship, and extrapolating to  $2t$ , gives the  $V_{in}$  that is acceptable if twice the regeneration time is available. From this the probability of error can now be estimated at  $\approx 1 \times 10^{-7}$  at a 10 giga-samples/s rate, or  $\approx 1.9 \times 10^{-4}$  at a 20 giga-samples/s rate. Notice that the error rate for 20 giga-samples/s operation has decreased much less than the error rate for 10 giga-samples/s operation, as the slope of the curve in figure 3.5 is much less at this point. The error rate at 10 giga-samples/s operation is sufficiently low for the current application.

### 3.3.3 Comparator Error Sources

The previous section investigated the maximum performance level that can be achieved with the devices. In a sense, it represents the upper limit as determined by the speed of the transistors available and the associated device and interconnect parasitics. In practice, other error mechanisms are present which serve to degrade the performance of the comparators. These error mechanisms include: jitter; thermal noise; slew rate dependent sampling point; clock kickback; input signal dependent delay and capacitive junction feed-through. Thermal noise and jitter are fundamental properties of any sampling system. The remaining error mechanisms arise from the choice of comparators as both the sampling and quantising element. The following section will deal with these error mechanisms and their impact upon the digitisers.

#### Jitter

Jitter on the sampling clock is one of the most important error sources in digitisers [48, 49]. Jitter of the clock source leads to variation of the sampling point and hence error in the sampled voltage. To analyse this effect

consider an input sinusoidal source  $V(t) = A\sin(2\pi ft)$ . The voltage error  $\Delta V$ , introduced by a sampling time error  $\Delta t$ , is to first order

$$\Delta V = \frac{dV(t)}{dt} \Delta t. \quad (3.8)$$

If the probability distribution function (PDF) of the timing jitter, that is the variation about the true sampling point, is modelled as a Gaussian distribution of zero mean and variance  $\sigma^2$ , then the rms error voltage over the period of the sine wave input,  $T$ , is [48]

$$V_\sigma = \sqrt{\frac{1}{T} \int_0^T \left( \frac{dV(t)}{dt} \right)^2 dt} \sigma = \sqrt{2\pi} Af\sigma. \quad (3.9)$$

The signal power is given by  $A^2/2$  so that the signal-to-noise ratio, due to timing jitter, is

$$SNR_{jitter} = -20 \log(2\pi f\sigma) \text{ dB}. \quad (3.10)$$

If this result is equated with the general expression of equation 2.15 for the signal-to-noise ratio of a general  $B$  bit ADC, and the resulting equality solved for  $B$ , an effective number of bits limit due to timing jitter can be derived as

$$B_{jitter} = -3.3 \log(2\pi f\sigma) - 0.29 \text{ bits}. \quad (3.11)$$

In the ADC survey in [50] it is empirically found that all published ADCs lie above a minimum jitter value of approximately 0.5 ps. Assuming that a similar value of jitter can be achieved with the present designs, and at the highest analogue input frequency of 4 GHz, the effective number of bits is approximately 6 (i.e. 64 levels). As this is well above the three-level quantising used in the digitisers, jitter is not a limiting error source.

As well as random timing jitter in the sampling signal, constant offsets between the sampling instant at different comparators lead to distortion and loss of signal-to-noise ratio [51]. This timing skew must be reduced to a similar level as for random jitter and highlights the need to ensure that clock lines to each comparator are well balanced in length and loading.

### Thermal noise

Thermal noise generated at the input, and internal circuit impedances, provides background noise that is indistinguishable from real input signal. Clearly, as this approaches half of a LSB in value, significant degradation of the output signal-to-noise ratio will be experienced. If all thermal noise sources are referred back to the input, they can be represented by an equivalent input noise resistance at room temperature. In the ADC survey cited in the previous section [50], it has been empirically found that state of the art ADCs lie above a noise resistance value,  $R_{th}$ , of approximately 2000 ohm. This reference also derives an effective number of bits due to thermal noise limitations given by

$$B_{th} = \log_2 \sqrt{\left(\frac{V_{fs}^2}{6kTR_{th}f_s}\right)} - 1 \quad \text{bits}, \quad (3.12)$$

where  $k$  is Boltzmann's constant,  $T$  the absolute temperature,  $f_s$  the sampling rate and  $V_{fs}$  the full scale input voltage. At the maximum intended sampling rate of 8 giga-samples/s the effective number of bits is approximately 9.6. Thermal noise is not a significant error source for the digitisers.

### Input Slew Rate Dependent Sampling Point

This effect arises when high slew rate input signals are latched by finite rise time clock signals. As the latching signal is applied, and the latch passes from track to hold, then it is possible that a high slew rate signal, which is about to pass through the threshold level of the comparator, may pass through the threshold during the switching period and cause the latched value to be the opposite of what it was at the initial application of the latch signal. A slow slew rate signal on the other hand would be latched to give the same polarity as at the application of the latch signal. This is equivalent to a variation of the sampling point dependent upon the input slew rate. This effect has been treated in [43], where it is shown that this leads to third harmonic distortion. This effect can be minimised by insuring the rise time of the clock signals

on chip is significantly faster than the maximum input slew rate. In section 3.3.6 dealing with the clock buffers, it will be seen that the clock buffers were designed for high bandwidth to minimise the clock waveform rise time. The simulated rise time was approximately 25 ps. The large quantisation steps of the digitiser also help to make the design insensitive to this effect, as the amplitude error introduced by an effective sample time variation is small compared to the quantisation step.

### **Clock Kickback**

During the latch-to-track transition of the latch composed of Q7-Q14 in figure 3.2, transistors Q7 and Q8 are initially off. As Q12 turns on, and current begins to flow, the base emitter junction capacitances of Q7 and Q8 initially provide a low impedance to the fast clock transient. This allows the clock transient to propagate through the junction capacitances back to the input of the latch. This phenomenon is known as kickback noise. One of the benefits of the preamplifier before the latch is that it reduces the level of kickback noise propagated back to the input [52]. In addition, the fully differential architecture ensures that the impedance of both the positive and negative latch inputs is the same, so the differential error voltage induced by the current transient, which occurs in both inputs, is small. The low impedance of the internal collector nodes of 200 ohm, and the comparator input impedance of 50 ohm, ensures the magnitude of induced voltage is also small. The level of kickback noise was verified through simulation. The kickback noise spike induced at the emitters of Q5 and Q6 is equal to within 4 mV, and the transient completely decays within 150 ps, which shows kickback noise is not a problem at the target sampling rate, and with the large quantisation levels used.

### Input Signal Dependent Delay

As the input signal level changes the junction capacitances of the input emitter follower change. Of most importance is the base-collector capacitance, which varies non-linearly with base-collector voltage according to the usual relation for depletion capacitance of reversed biased p-n junctions, namely

$$C_{bc} = \frac{C_0}{\left(1 + \frac{V_{bc}}{\phi}\right)^{m_j}}, \quad (3.13)$$

where  $C_0$  is the zero bias capacitance,  $V_{bc}$  is the voltage across the junction,  $\phi$  is the base-collector built-in potential and  $m_j$  is the junction ideality factor, which is usually in the range 0.3-0.6. As this capacitance changes, the delay introduced by the emitter follower changes. This is equivalent to a variation of the effective sample point, leading to an amplitude error in the sampled signal proportional to the capacitance and the slew rate of the input signal. This mechanism is analysed in [53], where it is shown that this effect leads to harmonic distortion terms and becomes a problem when the amplitude errors approach half of a LSB. The relative amplitude of the second order distortion term is estimated as

$$HD_2 = \frac{V_0 \omega C_{j1} R}{2 \sqrt{1 + (2 \omega C_{j0} R)^2}}. \quad (3.14)$$

Here  $V_0$  is the magnitude of the fundamental,  $\omega$  the frequency,  $C_{j1}$  the linear term in a polynomial expansion of equation 3.13,  $C_{j0}$  the constant term in the same expansion and  $R$  the source resistance. For the InP process, exact data on the junction capacitances and junction properties is not available. However, the collector-base capacitance is very small, of the order of tens of femto-farads, for similar high speed transistors from other published sources [54]. Taking an upper limit of 50 fF for the capacitance, a typical built in potential of 0.5 V for InP devices, and an ideality factor of 0.5, then equation 3.14 indicates the second harmonic distortion is over 40 dB below the fundamental at the highest anticipated input frequency of 4 GHz for the current design. For high resolution flash A/D converters the many comparators



in parallel lead to a high total input junction capacitance and the size of the LSB is also small, so this effect can be then problematic. In the InP digitisers designed here, the small number of comparators and low junction capacitance, combined with the large quantisation levels, means this effect is insignificant.

### Capacitive Junction Feed-through

At high analogue input frequencies, a portion of the input signal at INP is able to couple through the base-emitter junction capacitances of Q24-Q27 and feed back to the inverting input, INN [45]. This causes distortion of the analogue input signal. It is possible to short out this feed-through by including a small capacitor of a few pF on the inverting input of each comparator, but in the present device it was preferred not to do this, as the digitiser was designed to be also usable as a dual 1-4 data demultiplexer. This is achieved by fixing what would normally be the analogue input at the centre of the input common mode range, and AC coupling the two data bits to the two inverting inputs. Placing an AC short on the inverting inputs would prevent the devices being reused in this way.

In order to verify that the level of feed-through was tolerable at the intended input frequencies, a simulation was performed to measure this effect. Up to the intended maximum input frequency of 4 GHz, the proportion of signal power coupled to the inverting input is less than -30 dB, which is acceptable for the present design.

### 3.3.4 Comparator Performance and Errors Summary

The previous performance and error analyses show that the digitisers should be able to achieve the target goal of Nyquist sampling to 8 giga-samples/s rate. The error analyses also show that the choice of using comparators for both the sampling and quantising elements in the digitiser designs, instead of incorporating an additional sample and hold, does not lead to any appreciable

loss of performance for these designs.

### 3.3.5 Output Demultiplexer

After the input analogue signal is digitised, the digital output data undergoes a 1-4 serial to parallel conversion, and the data is sent from the chip four samples at a time, at a quarter of the input sample rate. This was done to ease the burden on the following electronics that must further process the digitised data. If the data were output from the chip at the sample rate, up to 8 giga-samples/s, it would be very difficult to deal with the data at this speed. The fastest conventional commercial logic works to speeds of approximately 2 GHz [55]. Devices are available which can operate at the full data rate but are expensive and space consuming and would require very tight skew and timing control. It makes sense to include this first stage of demultiplexing on chip, where the timing and skew can be well controlled, and which will then allow cheap commercial ECL logic to be used from the chip outputs downstream.

The demultiplexer is based on a shift register with output data register as shown in figure 3.6. The four bit shift register fills with four successive bits and then the output register, which operates at one quarter of the sample rate, captures the four bits and presents them to the output buffers. The

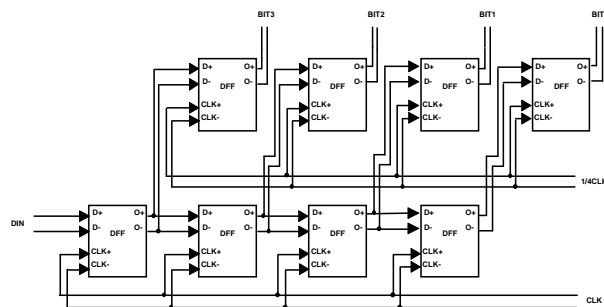


Figure 3.6: 1-4 demultiplexer block diagram.

demultiplexing clock is driven from a second clock input for maximum flexibility and ease of synchronising the demultiplexed data across several units. In general, it would be at one quarter of the input clock rate, and is phase

locked to the sample clock. It can optionally be driven at different integer fractions of the sample rate for testing or undersampling applications. Using the two separate clocks makes the task of synchronising the data from multiple units much easier. In general, multiple digitiser units will be separated by large indeterminate physical distances, in terms of the wavelength of the sampling clock. If the demultiplexing clock were derived internal to the chip with a  $1/n$  divider, there exists a phase ambiguity in the relative position of the demultiplexing clock in the multiple digitiser units. For example, with a  $1/4$  divider there are 4 separate phase slots in which the demultiplexing clock can reside. To synchronise multiple units a reset input to the divide-by- $n$  is needed. All the digitiser inputs must receive this reset within the same sampling clock period and with sufficient setup time to be recognised by the rising clock edge. With an 8 GHz sampling clock, this implies that the reset signal must reach all reset inputs within 125 ps of each other, a very difficult system challenge. Even then, the phase of the demultiplexed data must be measured to ensure that the reset operation has proceeded correctly, which adds to the system complexity. By using phase locked sample and demultiplexer clocks distributed to all the digitiser units in parallel all the units are guaranteed to be synchronised. The flip-flops are D-type master-slave flip-flops, composed of two cascaded latches in series which are driven in antiphase. This is similar to the master-slave latches of the comparator but does not include the front-end preamplifier. The schematic of the D-type flip-flop is shown in figure 3.7.

### 3.3.6 Clock Buffer

The sampling clock and the demultiplexing clock must be distributed to all of the clocked comparators and flip-flops on the chip. The large number of loads and interconnect transmission lines present a significant load, so a high current clock driver is needed to maintain high bandwidth and sufficient signal level. The schematic of the clock buffer circuit is shown in figure 3.8.

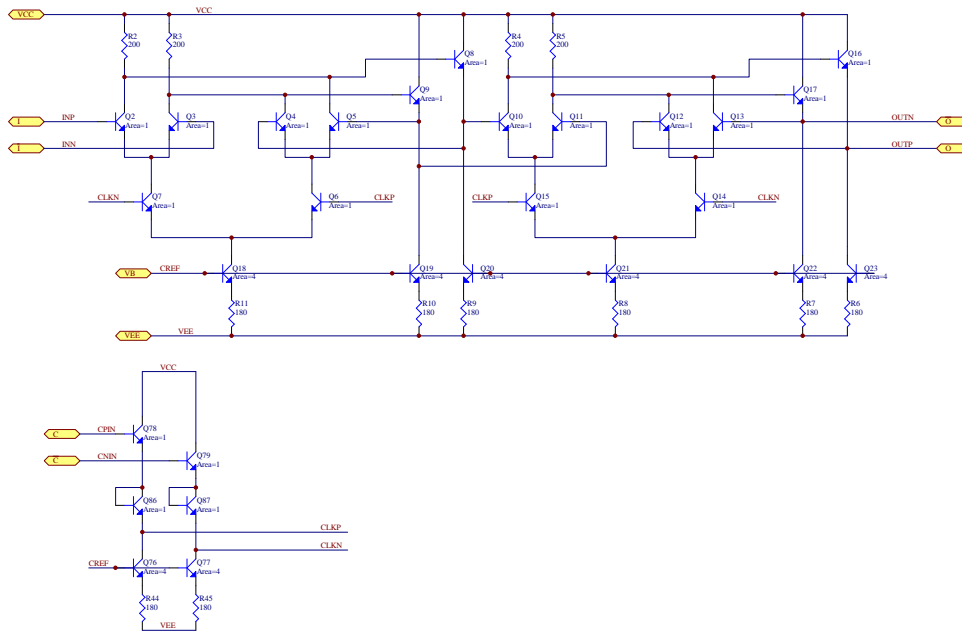


Figure 3.7: Schematic of D-type flip-flop.

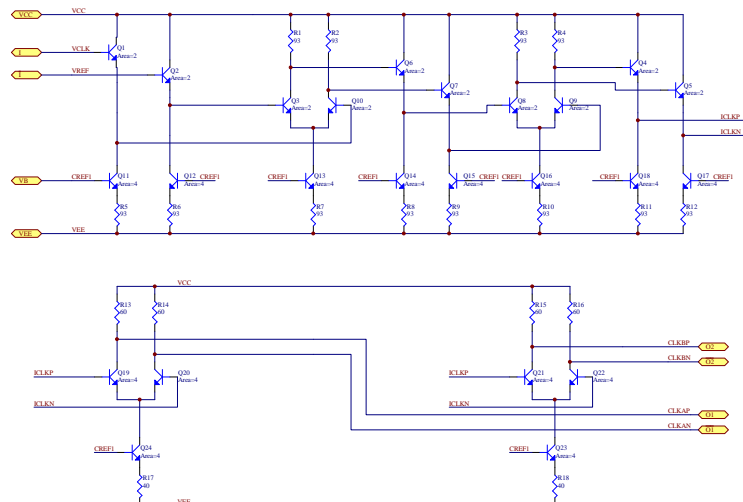


Figure 3.8: Schematic of the clock buffer.

The circuit is composed of a cascade of three high gain differential amplifiers. The input sinusoidal clock source is AC coupled to the positive input, with the inverting input held at the same DC reference voltage as the non-inverting input. The cascade of high gain amplifiers squares up the sinusoidal source and also performs a single ended to differential conversion. The clock is split in the last stage to drive two final amplifiers, so that half the loads are driven from one amplifier and half the loads from the other. All clocks are distributed differentially to provide maximum rejection of common mode noise. On the chip, the clock signals, which run over comparatively long distances of over a millimetre, are routed as differential controlled impedance transmission lines of approximately 100 ohm differential impedance. Careful

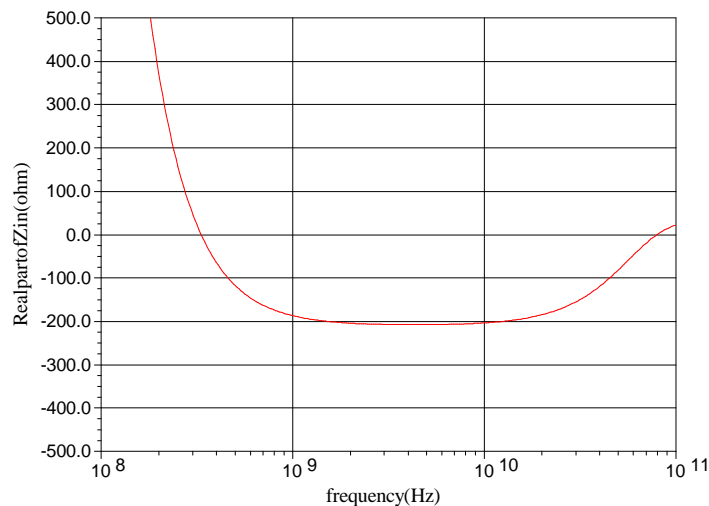


Figure 3.9: Emitter follower input impedance.

modelling of the clock transmission lines was very important, as the significant phase shift of long transmission lines provides the potential for on chip oscillation. Of particular concern are the use of emitter followers, as the combination of capacitive loading on the emitter combined with inductance in the base, for example as a result of a length of transmission line, can lead to oscillation of the emitter follower [32, 56]. Looking at the input impedance of a simple emitter follower using a minimum size InP transistor, without any loading, gives the results of figure 3.9.

It can be seen that the real part of the input impedance is negative over a large part of the frequency range, and hence if the  $Q$  of the resonant circuit formed by the combination of base inductance and emitter capacitance is sufficiently high, the circuit will oscillate. The clock drivers could have provided an emitter follower level shift in the buffer and driven the transmission lines from the emitter followers. This is the generally accepted approach as it provides a low impedance drive which should be good for driving capacitive loads and the clock signal is at the correct DC level for driving the clock inputs of the flip-flops and comparators directly. Figure 3.10 shows a simulation of the clock switching waveform for a clock buffer incorporating emitter followers driving 300  $\mu\text{m}$  of transmission line into a differential amplifier load. It is evident that there is significant ringing and the circuit is on the verge

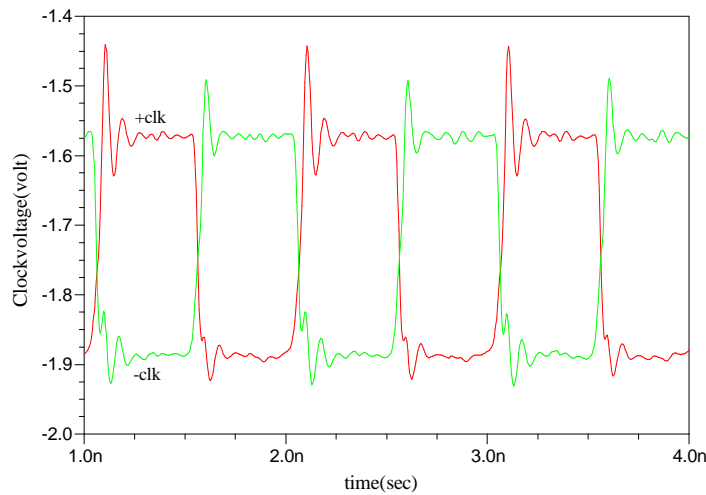


Figure 3.10: Clock driver with emitter followers.

of instability. By moving the emitter follower level shifting to the end of the transmission line, and using collector drive of the transmission line, the result of figure 3.11 was obtained. It is clear that this is a far more stable approach. The disadvantage is that a local level shifting block has to be included at the receiving end in every comparator and flip-flop. This incurs a penalty of six transistors per comparator or flip-flop, but was considered

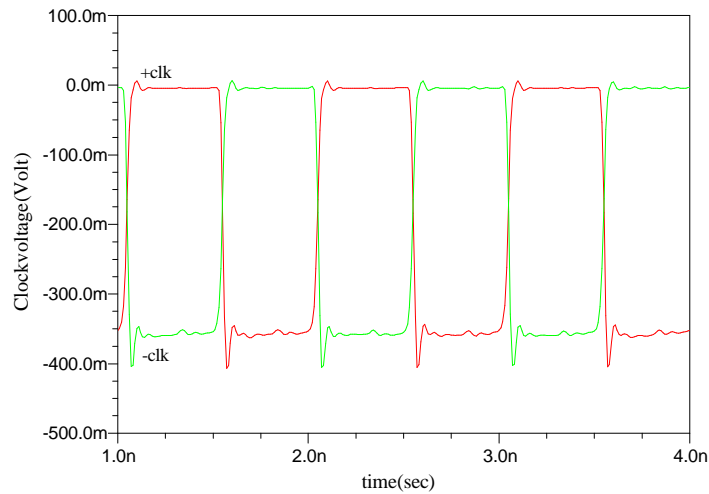


Figure 3.11: Clock driver with collector drive.

the superior approach in the interests of stability. The collector drive of the transmission line provides a further advantage in that the collector resistors provide a back termination for the transmission line, so that any reflected wave from the load is absorbed in the back termination resistors, if they are well matched. The current level and device size of the drive transistors Q19-Q22 were selected so that collector load resistors could be chosen that not only provide the required clock voltage swing, but also give a good match to the impedance of the transmission lines.

### 3.3.7 Output Buffer

The digitised data is sent off chip through specially designed output buffers. The function of the output buffers is to provide sufficient drive to overcome any capacitive and transmission line loading on the outputs and to translate the internal voltage levels to a standard voltage level that can be interpreted by commercial logic. The only readily available commercial logic family that operates at the required speed, of up to 2 GHz, is ECL [55]. Hence the output buffers were designed to drive ECL logic. The standard ECL logic levels are -0.8 V for logic high, and -1.6V for logic low, with a signal

swing of 800 mV into a 50 ohm transmission line. Providing 800 mV signal swing at high slew rate into a 50 ohm transmission line, with a possible capacitive load of a few pF, requires a very high current output driver. The output buffers alone would consume well over half the total current and power budget of the chip. To reduce the current drive requirement, and lower the power dissipation of the chip, it was decided to use a 400 mV signal swing extending from approximately -0.9V to -1.3V, which for the purposes of this work I will call pseudo ECL levels, and to design the outputs to drive 75 ohm transmission lines. Looking more closely at the ECL datasheets, one notes that the AC parameters are fully guaranteed for 150 mV signal swing about the switching threshold. By using differential outputs on the buffers, and differential input ECL receiver inputs, the switching threshold is defined by the point at which the in-phase and complement signals cross over, not by any arbitrary voltage level, so long as the respective in-phase and complement signals remain within the common mode range of the receiver (approximately -0.4V - -2.0V at standard supply voltages). Pseudo ECL levels combined with differential transmission satisfy these requirements and maintain full AC performance of the ECL receivers. With these approaches the current drive and power requirement of the output buffers were greatly reduced, but even then they still contribute approximately one quarter of the total device dissipation. The schematic of the output buffer is presented in figure 3.12. The output buffer is composed of a cascaded pair of differential amplifiers

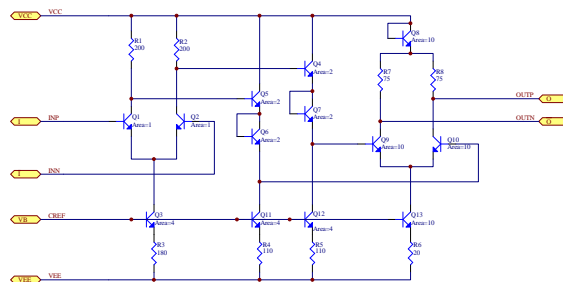


Figure 3.12: Output buffer schematic.



with increasing transistor size, scaled so that the preceding amplifier has sufficient current to drive the following amplifier. Of note is that the output is driven from the collector of the final differential amplifier, with a diode connected transistor providing a level shift down to within the common mode range of the ECL receivers. This is in contrast to almost all commercial chips with ECL compatible outputs, which instead use emitter follower outputs. As noted in the previous section on the clock buffer, emitter followers are inherently unstable in the current process due to the very high speed of the devices, combined with extremely low parasitic base resistance. Hence, it was decided to use the far more stable collector output drive, and also the collector load resistors provide matched back termination for the output transmission lines.

### 3.3.8 Current Sources

Biasing for all the active circuits on chip is provided through current sources. The current sources used are simple current mirrors with emitter resistors [41], as shown in figure 3.13. The emitter resistors in the current sources were used in the interests of thermal stability, as current sources using HBTs without emitter resistors are known to be prone to thermal runaway [57]. The emitter resistors provide the necessary negative feedback to ensure temperature stability. The reference voltage  $V_B$ , developed over the diode connected transistor Q1, is distributed to all the current mirrors on the chip, approximately 150 in total. The top of the resistor R1, which sets the reference current, is connected to a chip pad and controlled externally. This allows the current bias in all the devices on the chip to be controlled by means of this control voltage, allowing a trade off between device speed and power dissipation in the application circuit. This pin is nominally connected to ground to give the designed value of bias current. In the ideal case of infinite  $\beta$ , the programmed current is set by the ratio of R2 to R3 times the reference current through R1. Owing to the low  $\beta$  of the devices of around 30, significant

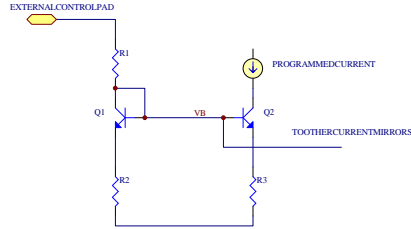


Figure 3.13: Current source with emitter resistors.

base current is drawn by the current sources, so simulation was used to adjust the parameters to give the correct bias current. Larger devices than the switching transistors were used in the current sources so that the transistors' parasitic emitter resistance would be smaller. In this way, the programmed current is set by R2 and R3, and is not dependent on Q2. Given that the supplied device models were only preliminary and subject to change it was imperative to make the design insensitive to model parameter variations.

### 3.3.9 Summary

The final mask layout of the digitiser/demultiplexer IC is shown in figure 3.14.

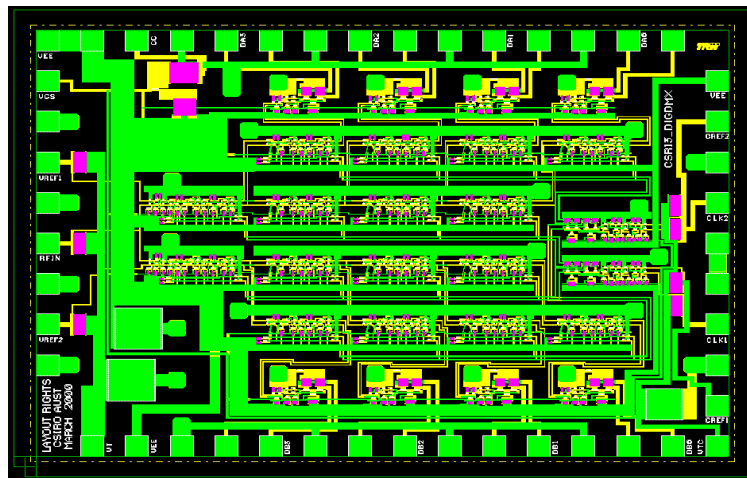


Figure 3.14: Digitiser/Demultiplexer layout.

In summary, key features of the design are:

- Designed for operation up to 8 giga-samples/s
- Fully differential ECL/CML topology
- On chip matching of RF and clock inputs
- Dual 1-4 demultiplexer on chip
- Outputs designed to drive 75 ohm terminated lines at pseudo ECL levels
- Input common mode range 0 - -1.3 V
- Input level -4 dBm
- Reusable as a dual 1-4 data demultiplexer
- Uses mostly minimum size transistors
- 740 transistors, 315 resistors, 3 capacitors
- 3.2 mm x 2.2 mm die
- Dissipates 1.6 W with a 3.5 V supply

### 3.4 Digitiser - No Demultiplexer

The digitiser without demultiplexer design was included chiefly as a backup in case of poor device yields, in which case the simpler design without on-chip demultiplexer would be more likely to yield working circuits. The block diagram of the the digitiser without demultiplexer is illustrated in figure 3.15. The digitiser without demultiplexer uses the same comparator blocks, output buffers and clock drivers as the digitiser with demultiplexer, so the dynamic performance of the two devices is the same.

Key features of this design which are distinct from the previous design are the following:

- Contains no demultiplexer on chip
- 119 transistors, 57 resistors, 3 capacitors
- 1.6 mm x 1.2 mm die
- Dissipates 350 mW with a 3.5 V supply

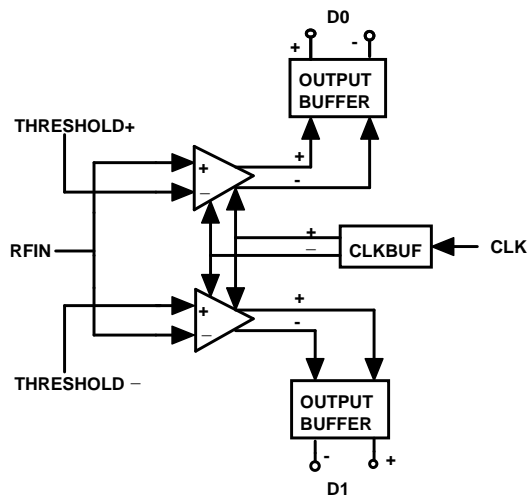


Figure 3.15: Digitiser without demultiplexer block diagram.

The corresponding chip layout is shown in figure 3.16.

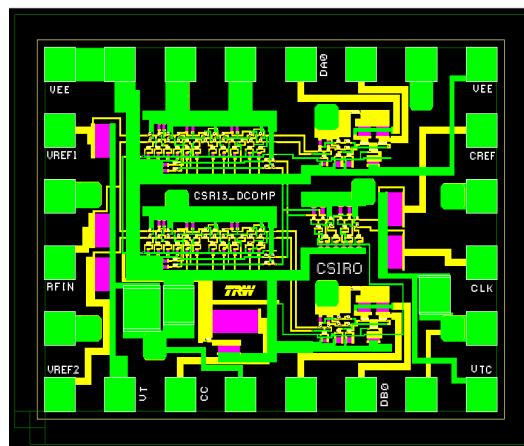


Figure 3.16: Digitiser without demultiplexer layout.

### 3.5 Photonic I/O Digitiser

The photonic I/O digitiser is a novel variation of the digitiser design in which the sampling clock is supplied photonically, via an optical fibre, and the digitised data can be returned photonically. The advantage of full optical connectivity is several fold: Having the sampling clock in optical form right until it is received on chip almost completely eliminates self generated interference from the sampling clock. In the radio telescope receiving chain there may be over 80 dB of RF gain between the receiver input and the processing backend, owing to the weakness of the signals being received. With electrical sampling clocks a small portion of the clock, or harmonics thereof, can radiate from the cables and connectors and enter back through the front end of the telescope. With the very high gain available this interference can easily cause significant interference spikes in the spectral data. A second advantage of photonic connectivity is the ability for remotely locating the digitiser from the rest of the signal processing machinery, like correlators. In-fibre losses are of the order of 0.1 dB/km so it makes little difference if the device is one metre or a kilometre away. The block diagram of the photonic I/O digitiser is presented in figure 3.17.

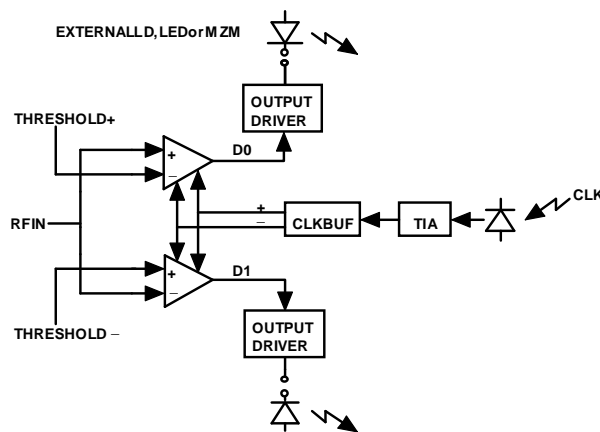


Figure 3.17: Photonic I/O digitiser block diagram

### 3.5.1 Transimpedance Amplifier

The sampling clock is received by a p-i-n photodiode on-chip, onto which the beam from the cleaved end of a fibre is positioned. A transimpedance amplifier amplifies the photodiode current and converts it to a voltage, before a single-ended to differential converter then generates the differential clock. The circuit diagram of the transimpedance amplifier is shown in figure 3.18. It is a common emitter amplifier with output emitter-follower buffer and

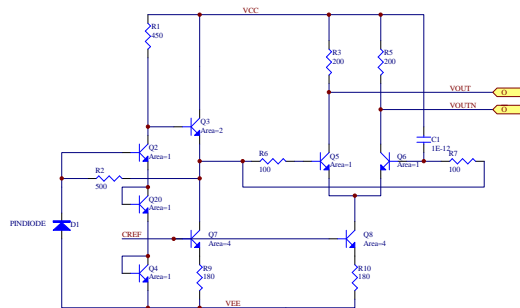


Figure 3.18: Transimpedance amplifier schematic

feedback resistor R2. It provides a transimpedance gain of approximately 400. The single-ended to differential converter is realised as a differential amplifier, with one input being the single-ended clock signal, and the other input being the single-ended clock signal passed through a low-pass filter. If the clock signal frequency is well above the cut-off frequency of the low pass filter then the output of the low pass filter is simply the mean DC level of the clock signal. The differential amplifier is thus self-biasing and places the inverting input at the same mean DC level as the non-inverting input, giving high sensitivity and a 50% duty cycle on the output clock waveform. This scheme functions only above a minimum frequency determined by the low pass filter. The combination is functional from approximately 100 MHz to 15 GHz in the present design. The low frequency cutoff is determined by the low-pass filter and the high frequency cutoff by gain roll-off in the transimpedance amplifier.

### 3.5.2 Output Buffer

The output buffers on the photonic I/O digitiser are designed as current switches [58, 59]. They are intended for bonding to an external LED, laser diode or optical intensity modulator. In the case of LEDs and laser diodes, the current is used to directly modulate the device. With the intensity modulator, the current is used to develop the necessary drive voltage across the typically 50 ohm input impedance of the modulator. The output buffers have a separate bias control pin to the switching transistors on the circuit. This allows the driving current of the output buffers to be adjusted from 0 to 65 mA. This is sufficient for modulating an LED or laser diode and gives a 3.2 V swing across 50 ohm for an intensity modulator, and is well within the breakdown voltage of  $\approx 8V$  of the transistors. The schematic of the output buffer is presented in figure 3.19.

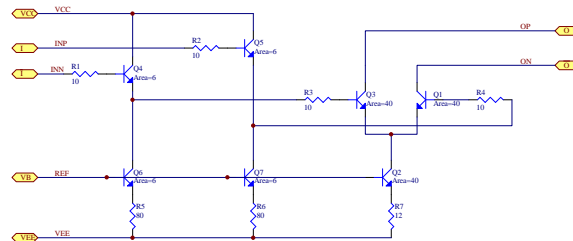


Figure 3.19: Output buffer schematic.

### 3.5.3 Summary

In summary, key features of the design are:

- Sampling clock supplied photonically
- Digital data returned photonically
- On chip photodiode and transimpedance amplifier

- Current switching output drivers for driving external laser diodes, LEDs or optical intensity modulators
- 116 transistors, 59 resistors and 3 capacitors
- 700 mW on a 1.6mm x 1.2mm die

The layout of the completed photonic I/O digitiser is shown in figure 3.20.

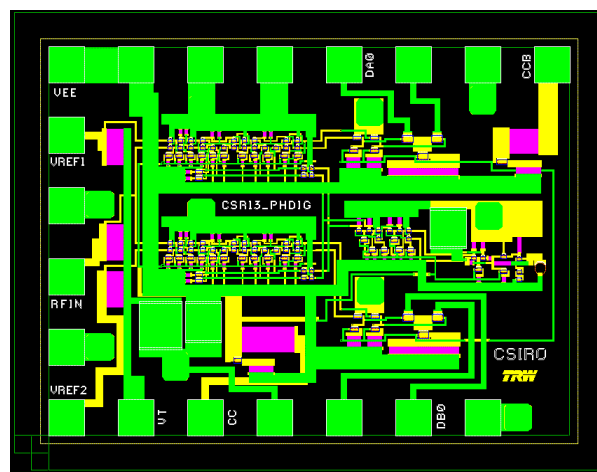


Figure 3.20: Photonic I/O digitiser layout.

To the best of my knowledge, this is the first digitiser or ADC device reported with integrated photonic input and output interfaces.



# Chapter 4

## Digitiser Testing and Packaging

### 4.1 Test Results

The digitiser ICs were fabricated at TRW Corporation, Los Angeles, USA. Testing of the devices was then divided into two parts. Initially, the InP wafers were returned as whole wafers mounted on a thick silicon carrier for mechanical stability (the 75  $\mu\text{m}$  thick InP wafers are extremely brittle). This was to allow simple on-wafer probing of all of the circuits on the wafers. Thus, on-wafer testing of the circuits was performed first. Following on-wafer verification and measurements the wafers were resent to TRW for dicing and the diced chips returned. The individually diced chips were then packaged and in-package and system tests were performed. The system test results are presented later in section 4.4.

#### 4.1.1 On-wafer Tests

The on-wafer tests were performed using a probe station supplied by the CSIRO, Division of Telecommunication and Industrial Physics (CTIP). The probe station comprised of a central mount with vacuum suction to hold the wafer under test in place. On all four sides of the central mount are positioned movable arms, to which either RF or DC wafer probes can be attached. The arms are equipped with micrometer adjustments on the x, y

and z axes to allow precise positioning of the wafer probes onto the IC pads. Test equipment is then connected to the wafer probes using coaxial cable.

### Digitiser/Demultiplexer

To test the functionality of the Digitiser/Demultiplexer IC a beat frequency test was used [45]. In this scheme the IC is clocked at a frequency  $f$  and an input sinusoid, phase locked to the clock signal, of frequency  $f + \delta f$  is applied to the RF input. The digitised output data will then only change at the beat frequency of  $\delta f$ , typically in the megahertz range, and can be observed on an oscilloscope. This tests the RF and clock portions of the IC at full speed whilst allowing the digital output data to be observed at low speeds. This was essential as the digital output data is differential ECL driven over twisted pair cables. Since the on-wafer probe setup is quite large long cables are needed. This limits their bandwidth to a few hundred MHz. The RF and clock inputs, by contrast, are delivered by on-wafer co-planar waveguide probes rated to 50 GHz, so these inputs could be exercised to full speed. Purchasing on-wafer RF probes for all of the sixteen digital outputs would have been prohibitively expensive. For the purposes of this test the threshold level inputs were left undriven, in which case they are both pulled on-chip to the same DC bias potential as the RF input, that is the DC value applied to the VT pin, nominally -0.65 V. In this case, the digitised data will be 50% of the time in the +1 state and 50% of the time in the -1 state i.e each output bit is a square wave of 50% duty cycle, assuming the input offset voltages are zero.

Figure 4.1 shows one of the output bits while exercising the chip at a clock rate of 10 GHz with an input sinusoidal excitation of 9.94 GHz. The output data rate is at 60 MHz. Input power levels for both the clock and data were -6 dBm. This figure shows correct large signal function of the device at 20% above the target speed. The function of the entire device was verified by examining each of the output bits in turn.

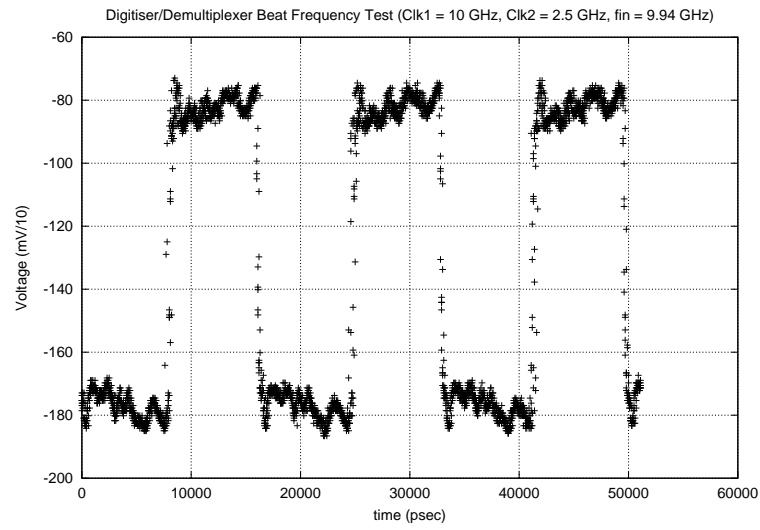


Figure 4.1: Digitiser/Demultiplexer beat frequency test.

### Digitiser

The digitiser without demultiplexer was wafer tested in the same fashion as the previous circuit. Figure 4.2 displays the result of a beat frequency test at 10 GHz clock rate with a 9.97 GHz sinusoidal data source and viewing one of the two output bits.

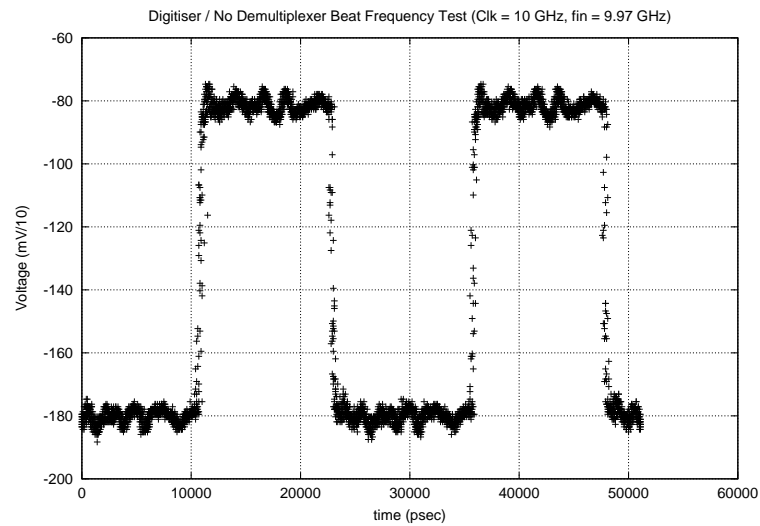


Figure 4.2: Digitiser beat frequency test.

### Photonic I/O Digitiser

The photonic I/O digitiser was wafer tested in a similar fashion to the previous devices. In this case though the clock has to be delivered optically and the outputs are current drivers. The optical clock was delivered over a single mode fibre with cleaved end. The fibre was fixed within a bare fibre adapter, with approximately 20 mm of fibre protruding, and the fibre adapter was fixed to one of the arms of the wafer probing station. The fibre end was then positioned over the photodiode on the chip.

To observe the output data the current switched output was driven through a 50 ohm resistor to ground and the voltage developed across the resistor observed on an oscilloscope.

The optical source was a directly modulated laser diode. The maximum modulation frequency of this diode was approximately 2.5 GHz, so the maximum operation frequency to which the chip could be tested was limited to this value. The fact that the current switched outputs are not transmission line drivers, and the cables must be long to the load resistor because of the limitations of the probe setup, meant that the measured data was quite noisy due to reflections and noise pickup on the output cable. Figure 4.3 shows

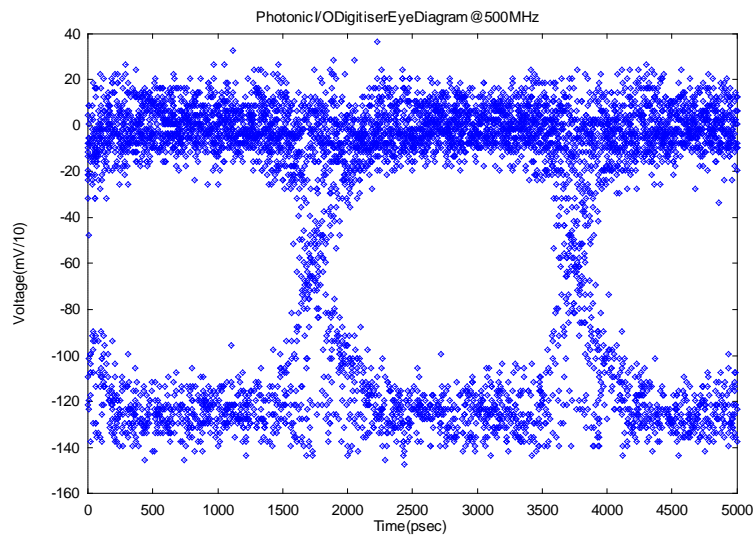


Figure 4.3: Photonic I/O digitiser eye diagram.

an eye diagram from operating the device at 500 MHz.

## Yields

Yields for the devices were high. All the circuits on two of the wafers were tested for functionality. From these measurements the average yield was 96% of circuits functional. This gives an indication of the excellent quality of the TRW manufacturing process. Given these high results the remaining three wafers were spot tested only and assumed to have similar yield to arrive at an estimate of the total number of circuits yielded, which were as follows:

- Digitiser/Demultiplexer 360 circuits
- Digitiser 258 circuits
- Photonic I/O Digitiser 180 circuits

## 4.2 Packaging of the Digitiser ICs

The digitiser ICs cannot be used directly as die, but must be packaged in some form that allows them to be connected to the surrounding circuits. Chief requirements for a packaging solution include: conveying the input, clock and output data signals with a minimum of degradation to and from the chip pads; providing adequate heat sinking so that the chip is operating with the device junctions at a safe temperature for reliable long-term use; providing mechanical and metallurgical conditions conducive to reliable wire bonding; and easy interconnection into the application circuit.

The package which was designed for this purpose is shown in figure 4.4. It consists of a brass package with a centre recess and lid. The package is plated with several microns of nickel as a diffusion barrier and finished with a gold flash. Onto the base of the inside of the package is fixed a small circuit board made of microwave laminate. The microwave laminate is patterned with a set of controlled impedance transmission lines that convey the input and output signals to and from the package pins and device pads. The transmission lines terminate a short distance from the IC at the edge of a cutout

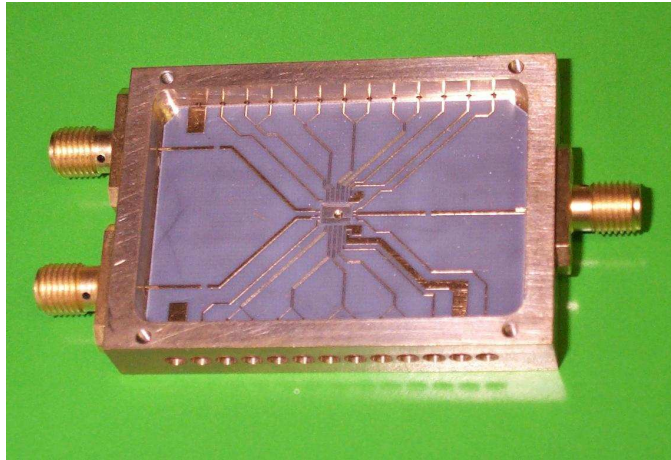


Figure 4.4: Digitiser/Demultiplexer package.

in the laminate, through which the IC is directly bonded to the base of the package with conductive epoxy. This provides a good thermal and electrical bond. The package itself forms the heatsink for the die and is cooled with forced air circulation in the application circuit. Small single-layer decoupling capacitors are also attached to the laminate and directly bonded to the IC power pads. The signal and power lines on the laminate are wire bonded to the IC using thermo-sonic wedge bonding with 17  $\mu\text{m}$  gold bond wire. To enable a reliable bond to be made the laminate is plated with 0.5  $\mu\text{m}$  of gold over a 4  $\mu\text{m}$  layer of nickel. The nickel prevents diffusion of the copper into the gold that naturally occurs, especially at the elevated temperatures used in thermo-sonic bonding [60]. Without the nickel layer the copper would diffuse into the gold and oxidise on the surface, preventing wire bonding. The relatively thick nickel layer of 4  $\mu\text{m}$  also provides mechanical stability of the bonding pads on the microwave laminate. Microwave laminates are made from relatively soft dielectric materials with low glass transition temperatures [61]. Under the pressure of thermo-sonic bonding it is common for the copper bond pad to simply deform as the dielectric beneath it is compressed [60, 62]. The energy of the thermo-sonic bonder is dissipated in deformation of the dielectric, instead of heating the bond interface, and a reliable bond does not form. The thick layer of hard nickel provides rigidity for the bond

pad helping prevent bond pad deformation. To aid with the bonding the microwave laminate Rogers Corporation RO4000 was used as this incorporates dielectric fillers designed to increase the compressive modulus of the material [63]. This is a far more rigid dielectric than the pure teflon dielectrics commonly used in microwave laminates. The laminate is attached to the package with conductive silver-filled epoxy. RF and clock inputs are through SMA connectors on the front and rear of the package. Digital output data, power, and level control are through a total of 26 feed-through pins on either side of the package. The next higher level of assembly is accomplished by inserting the package into a cutout in a carrier board. The feed-through pins rest on pads at the edge of the cutout and are soldered in place. Figure 4.4 shows a picture of the package with the lid removed. Figure A.1 shows the package installed in the carrier PCB.

### **4.3 Digitiser Subsystem and Support Hardware**

Various support electronics are required to implement a full digitiser system. The digitiser IC is the first, albeit most critical, element in the signal processing chain but a large amount of peripheral circuitry is required to realise the full digitiser system. There were four main circuit boards that had to be designed to fulfill these functions: The chip carrier PCB; The demultiplexer/statistics counter PCB; The DSP based controller PCB; and the synthesiser PCB. While there is a lot of work involved in the design and realisation of these subunits, I will not go into extensive details on each of the boards, as they are not the core topic of this work, but I will give a brief description of the functionality of the subunits. Full schematics of the subunit PCBs can be found in appendix A.

### 4.3.1 Chip Carrier

The chip carrier PCB provides the physical mounting for the chip via a cutout into which the chip package rests, supported by the lateral pins on the IC package. These pins are then soldered to the chip carrier PCB. The board also contains high speed differential ECL receivers that accept the pseudo-ECL differential data from the IC, buffer it, and send it to the following circuitry at standard ECL levels. Also present on this board is voltage regulation circuitry that converts the system -5.2 V supply to the -3.5 V supply required by the digitiser IC. Over-current and over-voltage sensing are included on the board to shutdown the power to the IC in case of a fault condition. Finally, bias control circuitry for setting the IC current bias, voltage bias for the termination voltages, and buffer amplifiers for the sampling threshold levels are also included. The output data signals are routed to the edge of the board as differential controlled impedance transmission lines of 100 ohm impedance and are connected to the following demultiplexer/statistics board with soldered links. The board was designed for a maximum operation speed of 2 GHz. As the input data has already undergone a 1-4 serial/parallel conversion by this stage within the digitiser IC, the board can support digitiser IC clock rates up to 8 GHz. An image of the complete chip carrier PCB with IC package installed is shown in figure A.1.

### 4.3.2 Demultiplexer/Statistics Counter

When the digitiser IC is operating at 4 giga-samples/s the output symbol rate from the previous chip carrier board is 1 giga-samples/s. This symbol rate is still too fast for the correlator system to process. The data must be further parallelised and presented to the correlator at a lower symbol rate. The demultiplexer/statistics counter board performs a further 1-4 serial to parallel conversion of the data, so that the final data is presented 16 samples wide, at 1/16 of the original sample rate. For example with a digitiser clock frequency of 4 GHz the output symbol rate is 250 MHz. The parallel data is



conveyed to the correlator with differential ECL line drivers over twisted pair cable of 100 ohm impedance. In addition, this board also counts the number of samples in each of the +1 and -1 states. Fast counters prescale this count by 256 and ripple into further 16 bit counters on the control board. A further counter accumulates the clock count and also ripples into a counter on the control board. The ratio of the +1 and -1 counts to the clock counts allows the proportion of samples in the +1, 0 and -1 states to be determined. This board was designed for a maximum operation frequency of 1.2 GHz and so limits the system to digitiser clock rates of 4.8 GHz. This was considered adequate as the following correlator has a maximum equivalent sample rate capability of 4 giga-samples/s. An image of the demultiplexer/statistics counter is shown in figure A.3.

### 4.3.3 Controller

The controller board, as suggested by its name, oversees the functions of the digitiser and provides communications with a host correlator control computer. The counts from the demultiplexer/statistics board are sent to the control board where they enter further counters. The ratio of the sample to clock counts gives the statistics of the signal. A digital control loop, implemented in the on-board DSP chip, uses this information to adjust the threshold levels of the digitiser, by way of 12 bit digital-to-analogue converters (DAC), so as to give 27% of the samples in both the +1 and -1 states. This is the required statistics for optimum signal to noise ratio. The DSP controller allows arbitrary setting of the loop constants as well as manual control of the thresholds if required. The default loop bandwidth is set at  $1/10$  Hz. The controller board also has an ATNF Block Control Computer (BCC) interface. This is a 16 bit parallel data bus that allows data transfer between the controller board and the BCC. The BCC is the computer which controls and coordinates the operation of the correlator system [64]. The control board has a universal asynchronous receiver/transmitter (UART) on

board with RS232 transceivers for serial communications if desired, and also drives a front panel alphanumeric display for visual status monitoring of the digitiser in normal operation. A picture of the complete controller board is shown in figure A.11.

#### 4.3.4 Synthesiser

The final functional unit within the digitiser is the synthesiser unit. This unit synthesises the nominally 4 GHz sample clock from the 5MHz reference frequency, and also generates a quarter sample rate clock, phase locked to the sample clock, for driving the demultiplexer clock and associated circuits. The synthesiser is programmable from 3.5 - 4.5 GHz and is based on a PLL architecture. An important function of the synthesiser board is that the sample and demultiplexer clocks must be synchronous across multiple units and also must have a fixed phase relationship to an external 1 Hz epoch signal. This is important for applications that require precise and repeatable absolute delays such as Very Long Baseline Interferometry (VLBI) imaging. This is achieved on board the synthesiser by using an external 1 Hz, or optionally another external SYNC signal, to perform a synchronous reset of the division counters in the synthesiser, combined with synchronous stop and start circuitry within the digitiser. A picture of the synthesiser unit is shown in figure A.16.

### 4.4 Complete Digitiser System Tests

Following dicing the digitiser/demultiplexer IC was assembled into its package and integrated into a full digitiser system unit with the support PCBs described earlier [65]. A photo of the complete digitiser unit is shown in figure 4.5. The unit contains the packaged device along with the support PCBs, power supplies, input/output connectors and cooling fans. The unit is assembled into a 2U standard sub-rack designed for mounting in a 19"



Figure 4.5: Complete 4 giga-sample/s digitiser unit.

RF screened industrial equipment rack. The assembled unit was then tested by connecting it to the ATNF's wide band correlator unit [66]. This system has a maximum bandwidth capability of 2 GHz, with up to 2048 frequency channels, but up until this time was limited to 1 GHz bandwidth, due to the lack of a fast enough digitiser. For this test the digitiser was fed with wide band noise through a 950-1800 MHz bandpass filter and the resulting correlation function and derived spectrum recorded as the output of the correlator. Figure 4.6 shows the result of the 2 GHz bandwidth, 2048 channel spectrum recorded. The ripple in the spectrum is due to the noise source and filter as verified by measuring the spectrum with a conventional spectrum analyser and comparing it with the spectrum from the correlator. The amplitude scale is linear in power which tends to exaggerate the ripple, which is approximately  $\pm 1.5$  dB over the pass-band.

The sensitivity of the digitiser was tested by reducing the power level of the input noise pass-band and noting the effect upon the spectrum from the correlator. The power level was reduced by over 20 db below the nominal input level before any observable change was seen. Even then the major effect

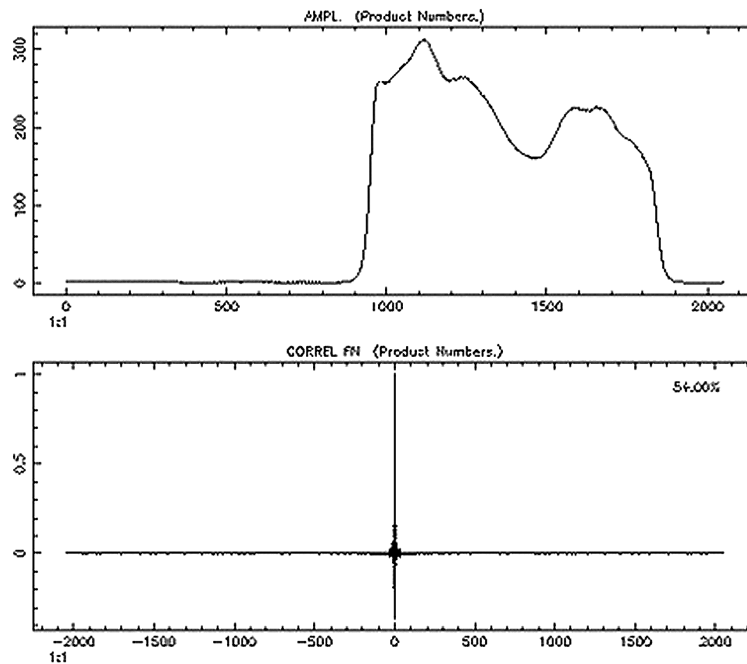


Figure 4.6: 2 GHz spectrum of 950 - 1800 MHz BPF with 2048 channels.

was a rise in the the DC offset of the correlation function as the noise power approached the quantising step of the 12-bit DACs which set the threshold levels. When the power level is of the order of the DAC quantising step the feedback loop is unable to accurately maintain the correct signal statistics and so a DC offset in the correlation function, and a corresponding zero frequency spike in the amplitude function, results. In normal operation, the dynamic range required of the digitiser is only of the order of 3 dB, as the input power level, dominated by noise from the receivers, changes very little when observing different parts of the sky.

An estimate of the usable input bandwidth of the digitiser was made using the following method. A CW signal from a synthesiser was summed with a wide bandwidth noise signal using a 1-20 GHz coupler and fed to the digitiser. The level of the CW was set so that the resulting tone in the correlator spectrum was approximately 6 dB above the noise pass-band. The narrow CW signal is only a small perturbation of the noise, as the total power in the CW spike is much less than the total power across the noise band, and

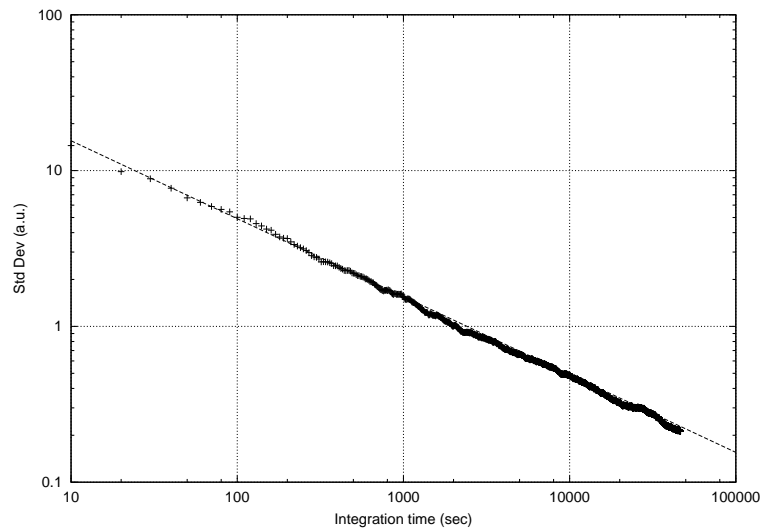


Figure 4.7: Standard deviation of correlator measurement.

so the digitiser is still operating with gaussian distributed input signal. The frequency of the CW signal was then stepped in frequency, being careful to choose frequencies that place the tone in the centre of an output frequency channel, so as to not smear the power over adjacent channels. As the CW frequency increases to 2 GHz the tone moves to the top of the spectrum, and as the frequency increases further aliases back in at the top of the band and moves down towards the zero frequency channel. Increasing the frequency further causes the tone to move back up through the spectrum and so forth. With this test the measured amplitude of the tone was found to be 3 dB down at approximately 9.5 GHz.

As a final test the standard deviation of the integrated spectrum from the correlator was measured as a function of the integration time. The standard deviation should reduce with the square root of integration time in accordance with the radiometer equation 1.1. This tests the entire digitiser and correlator system. Figure 4.7 shows the result of this measurement over a total integration time of 47000 seconds (13 hours). The slope of the regression line fitted to this data is -0.506, consistent with the radiometer equation.

## 4.5 Deployment

Two additional digitiser units were constructed and installed at the Australia Telescope National Facility's Parkes Observatory in central New South Wales in April 2002, where they provide the digitising for the ATNF Wide Band Pulsar Correlator [66]. This is a version of the correlator system mentioned in the previous section, optimised for pulsar observations.

It is planned to construct a further eight digitiser units to be used on the new Digital Filterbank Correlator [67] to be installed on the ATNF's Mopra telescope at Coonabarabran during 2003-04. This is an 8 GHz total bandwidth dual polarisation system made up of four 2 GHz chunks of spectrum, requiring a total of eight digitiser units.

# Chapter 5

## Wide Bandwidth Multipliers

At the very widest of bandwidths digital signal processing methods, such as those presented in the previous two chapters, can no longer be used. As the Nyquist sampling rate required to faithfully sample the signals moves into the tens of gigahertz range, it moves well beyond the capabilities of present day digitisers and digital signal processing machinery. Inevitably, digital processing will continue to advance with time and progressively move upward in bandwidth processing ability, but at the present time a break point exists at about the 2-4 GHz of integral bandwidth, beyond which analogue processing means must be used. Chief among the devices required are spectrometers, interferometers and bolometers.

Various forms of analogue spectrometers have been developed, the most important of which are acousto-optic spectrometers, which are in current use in many observatories around the world [5] and have been flown on-board satellites. These systems use a Bragg cell to diffract a laser beam passing obliquely through the cell. The RF band to be analysed drives an acoustic transducer attached to the Bragg cell. The angular diffraction of the laser beam and its relative intensity, when correctly aligned, can then be shown to be proportional to frequency and relative power of the applied RF and can be accumulated and read out from a linear CCD array positioned appropriately behind the Bragg cell.

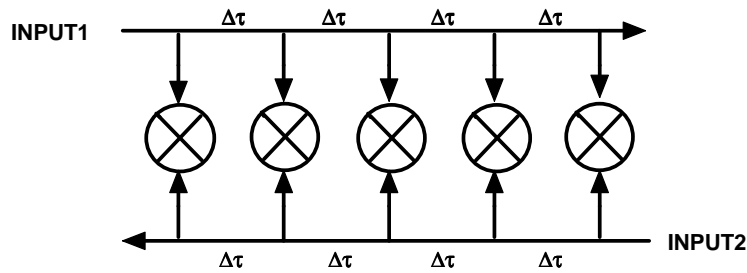


Figure 5.1: Generic lag correlator structure.

Chirp-z spectrometers have also been investigated and used in radio-astronomy [68, 6, 69]. These are known as compressive receivers in the radar community. This chirp-z spectrometer implements a chirp-z transform using mixers and dispersive delay lines. The incoming RF, whose frequency spectrum is to be analysed, is multiplied in a mixer with an LO drive that is a linear chirp. Typically, this would be generated by a wideband linear voltage controlled oscillator (VCO) fed from a ramp generator. This multiplied signal is then feed through a dispersive delay line, with chirp opposite to that of the VCO chirp, and with a total dispersive delay equal to the repetition rate of the VCO chirp waveform. This combination of processes results in each of the frequency components in the input signal combining at a specific time at the output. The spectrum of the input signal is then available as the amplitude versus time at the output. The spectrum repeats at the chirp waveform repetition rate and can thus be further accumulated if desired. This system can also be adapted to perform a cross-correlation of two input signals as required for an interferometer implementation [69].

A third class of spectrometers and correlators is based on an analogue implementation of a correlator. These use transmission line delays to generate the delayed versions of the input signal and use analogue multipliers to perform the multiplication operation that is inherent in the correlation process. Figure 5.1 shows one particular implementation of this approach, shown with 5 lags. The data at each lag is then accumulated by a combination of low pass filtering and post sampling digital accumulation. Owing to their



relative analogue complexity, with the concomitant matching and stability issues, these analogue correlators typically have far fewer lags than a digital correlator. Number of lags ranges from just a few to about 128. The wider the bandwidth processed then, usually, the less the number of lags generated. A good example of a modern high performance analogue correlator system is presented in [7]. The analogue lag correlator is very versatile and can be used in an auto- or cross-correlation mode as required by the particular experiment.

The bandwidth of an analogue correlator is limited by the bandwidth of the analogue multiplier elements it uses. This multiplication element has taken a few different forms in present correlator systems. These include microwave mixers with very low power drive to both inputs, of order -20 dBm [70], Gilbert cell type transistor multipliers [71], or via an add and square approach where the signals from the two antennas are summed and detected in a square law device and the product term extracted [1]. The system in [7] for instance uses commercial monolithic silicon Gilbert cell multipliers. These particular devices have a 3dB bandwidth of 3.5 GHz and represent the current commercial state of the art.

The analogue correlator approach looks to be the most versatile and most suitable for very wide bandwidth applications. In order to increase the bandwidth capability of analogue correlators, this chapter deals with the design of wide bandwidth multipliers suitable for use in analogue spectrometers and correlation receivers. I will present the design of a linear monolithic multiplier in InP HBT technology to produce a multiplier with much greater bandwidth than commercially available devices. I will also present a further multiplier design in an alternative SiGe semiconductor process, that may help solve some of the problems uncovered with the InP multiplier. A full noise analysis of each of these approaches is also presented, highlighting the importance of noise considerations in very wide bandwidth systems.

## 5.1 InP HBT Multiplier

Multipliers are popular circuits for implementing in high speed semiconductor processes. In general, these are designed for use as active mixers so that only linearity of the RF port is important. The LO port is designed to be fully switched. Active multipliers are almost universally based upon a Gilbert cell [71] architecture, realised in either field effect or bipolar device technologies. Amongst field effect devices, the widest bandwidth multipliers have been realised with GaAs and InP HEMTs. The device presented in [72] achieved a bandwidth of 38 GHz using a 150 GHz  $f_T$  InP HEMT process and distributed amplifier design techniques. Bipolar implementations have been reported with 15 GHz [73] and 20 GHz [74] bandwidth. The latter is implemented in a high speed InP HBT process.

As will be discussed in more detail later, whilst HEMT devices can achieve much greater speeds than HBTs, they suffer from very high low frequency noise [31], which makes them unsuitable for applications, like the present, where the output is taken at low frequencies and noise is of paramount importance. For this reason the multiplier was not designed with HEMTs, but instead using the same InP HBT process used to realise the digitisers in the previous chapters. Figure 5.2 shows the schematic of the InP HBT multiplier designed. The multiplier is based on a Gilbert cell core. The major difference between this circuit and the previously cited devices is that this circuit includes a pre-distortion circuit on what is conventionally known as the LO port in a mixer application, and the total amount of linearisation on both the inputs is greater than for a mixer application. This allows the device to operate linearly on both inputs over a 200 mV p-p input range.

The inputs X and Y are differential, though in normal usage the negative side of each input would be AC grounded, and only the positive side driven. Input X feeds a differential amplifier, consisting of Q7 and Q8, with diode connected transistors, Q1 and Q2, as loads. This forms a diode pre-distortion circuit that compensates the tanh characteristic of the Gilbert cell

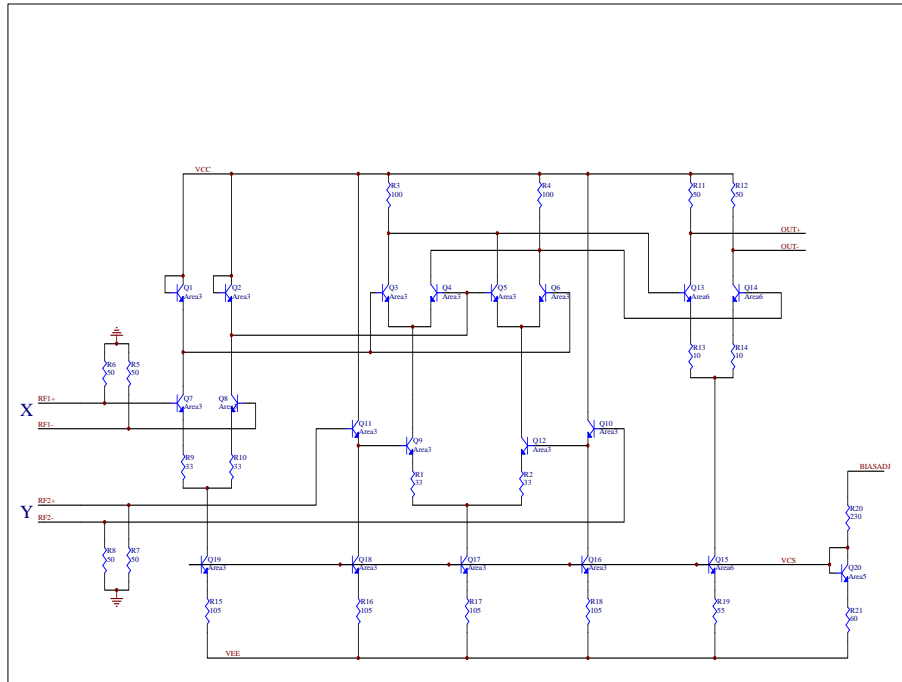


Figure 5.2: InP multiplier schematic.

core, composed of Q3-Q6, Q9 and Q12 [41]. The emitter degeneration resistors, R9 and R10, serve to linearise the differential amplifier and so increase the input amplitude range over which the multiplier can be used. Resistors R1 and R2 serve the same purpose on the Y input. Transistors Q13 and Q14 form a post amplifier to boost the output level and also buffer the multiplier core from the external load. Collector drive with 50 ohm back-termination impedance is used on the output for the same stability reasons mentioned in section 3.3.6, namely that the alternative emitter follower drivers that would commonly be used for this purpose are very unstable in the InP HBT system used to implement the multipliers. The output is differential and in normal operation is designed to be connected to a low-noise differential amplifier, which removes the common mode voltage present at the output of the device. The circuit was designed for a wide output bandwidth, despite the fact that in its use as an interferometer element its output bandwidth requirement is only of the order of a megahertz maximum, depending upon the phase switching frequency used. The circuit was designed in this way

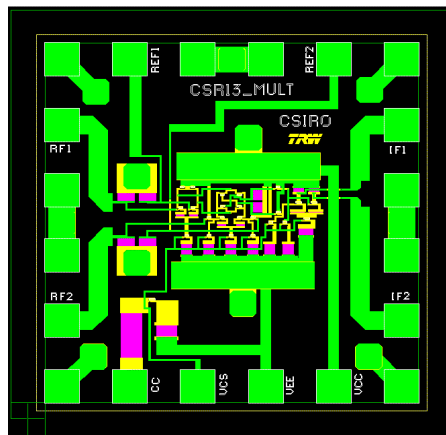


Figure 5.3: Multiplier layout.

to allow it to be also used as a wide bandwidth variable gain amplifier or in other general purpose applications. Collector current level in the transistors was designed for a nominal value of 85% of maximum, so as to maintain a high bandwidth, whilst not risking self-heating induced destruction of the devices. An external control input is provided to vary this bias current from zero to beyond the maximum current of the devices. When connected to ground this pin programs the device to the designed current level of 85% of maximum. The layout of the multiplier is shown in figure 5.3.

### 5.1.1 Noise Analysis

Apart from having sufficient bandwidth for the application, the most important criterion for a multiplier in a correlator application is that the device noise added by the multiplier does not seriously degrade the system sensitivity. A common specification is that the device should reduce the system sensitivity by less than one per cent. Put another way, this means the device noise should be more than 20 dB below the noise power, i.e. the variance, of the measurement itself. To analyse this noise situation consider a one element correlation receiver processing two signals  $x(t)$  and  $y(t)$  in the multiplier as shown in figure 5.4. This correlation receiver has been treated extensively in the radio astronomy literature. The standard approach is to analyse the sys-

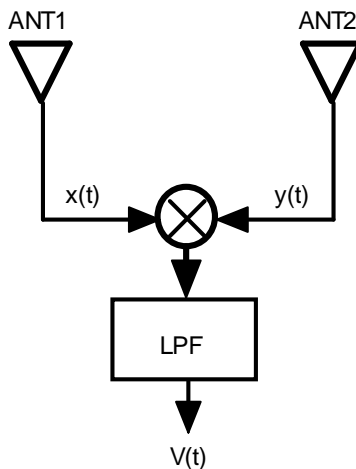


Figure 5.4: Generic correlation receiver.

tem in terms of equivalent noise temperatures. In terms of noise temperature  $T$  the noise power in a bandwidth  $B$  is given by

$$W = kTB \quad (5.1)$$

The noise power at the output of the receiver is the total system noise, or equivalently the system temperature,  $T_{sys}$ . This includes contributions from the antenna, the receiver and any other losses. The noise in each of the antennas is uncorrelated so the output of the correlation receiver is ideally zero with no input signal. When the antennas are pointed at a source and a signal is present in each of the antennas the sensitivity is the minimum signal temperature that can be detected. As derived in [1] this is given by

$$T_{min} = \frac{\sqrt{T_{sys1}T_{sys2}}}{\sqrt{2B\tau}}, \quad (5.2)$$

where  $B$  is the bandwidth of the input signals,  $\tau$  is the time over which the measurement is averaged and  $T_{sys1,2}$  are the system temperatures of each antenna. If the system temperatures of the two antennas are equal, and of value  $T_{sys}$ , this reduces to the familiar form

$$T_{min} = \frac{T_{sys}}{\sqrt{2B\tau}}. \quad (5.3)$$

The statistical interpretation of this result is that  $T_{min}$  is the standard deviation of the fluctuations at the output of the post multiplier averaging circuit.

Returning to the InP multiplier, the output voltage of the post multiplier averager is proportional to the input signal temperature. The output voltage corresponding to  $T_{sys}$  is found when the two inputs are 100% correlated and the circuit then measures the power of the input signal. If the output voltage corresponding to  $T_{sys}$  is  $V_0$ , then from 5.3 the standard deviation of the output voltage measurement,  $\delta V$ , is given by

$$\delta V = \frac{V_0}{\sqrt{2B\tau}}. \quad (5.4)$$

To express this in terms of per unit bandwidth noise at the output, consider that the output is averaged in an ideal low pass filter of bandwidth  $B_{LF}$  of 1 Hz, giving  $\tau = \frac{1}{2\pi B_{LF}}$ . This results in the following expression for the noise voltage per unit bandwidth, due to measurement variance, in the output voltage

$$\langle v_m(f) \rangle = V_0 \sqrt{\frac{\pi}{B}} \quad V/\sqrt{Hz}. \quad (5.5)$$

It is necessary that the device's noise voltage due to other sources be small compared to this value. If the multiplier has the transfer function  $V(t) = kx(t)y(t)$ , where  $k$  is the gain factor and  $x(t)$  and  $y(t)$  are the input voltages due to the two input signals, then the expected output voltage of the multiplier is

$$\langle V(t) \rangle = k \langle x(t)y(t) \rangle. \quad (5.6)$$

The InP HBT multiplier was designed for a maximum input level of -5 dBm CW (corresponding to a peak voltage excursion of 100 mV). Since the input is gaussian noise, we can assume an effective crest factor of about 4 or 5, so the maximum gaussian input power should be approximately -19 dBm. The gain factor for the multiplier is 9 so the maximum output voltage, which occurs for 100% correlated inputs, is 3.6 mV. The design bandwidth of the multiplier is 15 GHz so the standard deviation of the output voltage measurement noise, when processing the full bandwidth, is  $v_m = 52 \text{ nV}/\sqrt{Hz}$ .

The additional device noise consists of three principal components. Thermal noise generated in the circuit resistances and parasitic resistances of the transistors and other components, shot noise due to the current flow in the devices in the circuit and excess noise due to a number of physical processes occurring in chiefly the active components. The main forms of excess noise are generation-recombination noise and 1/f noise. Generation-recombination noise is a result of the number of free electrons in the semiconductor conduction band fluctuating as a result of generation and recombination processes between the band and traps. The exact origin of 1/f noise is still unclear [75]. The 1/f noise usually does not have a strictly 1/f spectrum and is a property of the semiconductor material, defects, impurities, and the exact physical structure of the transistors. The 1/f noise is currently impossible to predict.

The thermal and shot noise are correctly modelled by conventional circuit analysis packages based upon the circuit components and active device models. The 1/f noise has to be included explicitly from either manufacturer supplied data or measurements. For the InP HBT process used, no data for 1/f noise was available except to say that it is "low" compared to GaAs or InP HEMTs. HEMT devices typically have 1/f noise corner frequencies, the frequency where the extrapolated 1/f noise curve intersects the thermal plus shot noise horizontal asymptote, of the order of a few megahertz [31]. As a comparison typical Si bipolar transistors have 1/f noise corner frequencies of a few hundreds of hertz.

For the present design the output noise voltage density due to thermal and shot noise is approximately  $v_t = 3 \text{ nV}/\sqrt{\text{Hz}}$ , derived from simulation. Compared to the measurement variance of  $52 \text{ nV}/\sqrt{\text{Hz}}$  this reduces the system sensitivity by 0.3%, derived from  $\frac{v_t^2}{v_t^2 + v_m^2}$  as the noise powers add incoherently. The impact of the 1/f noise must be determined by measurement and will be presented in section 3.1.3 on measurements, where it will be shown that the 1/f noise has a much greater impact upon the system sensitivity.

It is well recognised that low frequency noise is a problem along with DC

offsets and slow DC drifts with temperature. To help reject these effects, along with other interference, it is usual with correlation interferometers like this to employ some form of phase switching combined with synchronous detection. In the wider engineering community this approach is known as lock-in detection or phase sensitive detection. It is a very popular technique in applications that require detection of small near DC signals in the presence of large amounts of background noise. In the application to radio astronomical interferometers the typical arrangement is to periodically invert the phase of one of the signals to the multiplier, either at baseband with a phase switch, or in the frequency conversion system by inverting the phase of the local oscillator, and then to multiply the output of the multiplier by  $\pm 1$  synchronously with the phase switching signal. The result is then passed through a low pass filter. The total effect of the operation is to centre the final detection bandwidth about the phase switching frequency, typically a few tens of hertz to kilohertz, so avoiding the worst of the low frequency noise and rejecting other low frequency drifts and DC offsets.

The sensitivity analysis so far has assumed ideal components, such as perfectly stable receivers with constant gain and noise figure, and an ideal multiplier. In reality the components contain imperfections. The effect of receiver gain variations on the system sensitivity of a correlation receiver is small as the output is only sensitive to the correlated component in each of the antennas. Gain variations only lead to a variation of output signal proportional to the correlated signal and this correlated signal component is invariably small compared to the  $T_{sys}$ . Specifically, if the gain variation is assumed to follow gaussian statistics, with mean gain  $G_n$  and standard deviation  $\sigma_{G_n}$ , where  $n = 1, 2$  refers to the antenna, then it has been shown [76] that the system sensitivity, for low signal-to-noise ratio inputs, is

$$T_{min} = \frac{T_{sys}}{\sqrt{2B\tau}} \left( 1 + \frac{1}{2} \frac{\sigma_{G1}^2}{G1^2} + \frac{1}{2} \frac{\sigma_{G2}^2}{G2^2} \right) \quad (5.7)$$

For small gain fluctuations this expression shows the sensitivity degradation is minimal and can generally be ignored.



The multiplier thus far has been assumed to be ideal. It gives an output equal to the product of the input signals only. In reality, the multiplier has non-linearities which become more pronounced as the input driving signals become larger. To second order, a general multiplier circuit will have an output given by

$$V_{out}(t) = k_0 + k_1x(t) + k_2y(t) + k_3x(t)y(t) + k_4x(t)^2 + k_5y(t)^2. \quad (5.8)$$

The constant  $k_0$  term contributes no noise just a constant offset that can be calibrated. The linear terms are completely filtered out in the post multiplier low pass filter, as this has a bandwidth in the kilohertz range whilst the input signals are microwave bandpass signals with low frequency cutoffs in the megahertz range. The squared terms produce a DC output that is proportional to the  $T_{sys}$  of each of the antennas. If the receiving system is stable this is not a problem as these DC terms are constant and their noise reduces with the averaging time so they produce a constant offset that can be calibrated. However, gain variations in the receiver lead to directly proportional changes in the apparent  $T_{sys}$ , and thus proportional changes in the expected values of the squared terms. These power changes due to gain variation are indistinguishable from power changes due to the presence of a source and so directly limit the sensitivity of the correlation receiver. The noise due to gain variations is independent of the noise in each of the antennas so the noise powers add incoherently. The system sensitivity is then

$$T_{min} = T_{sys} \sqrt{\frac{1}{2B\tau} + \left(\frac{k_4 \sigma_{G1}}{k_3 G1}\right)^2 + \left(\frac{k_5 \sigma_{G2}}{k_3 G2}\right)^2}. \quad (5.9)$$

For wide bandwidth systems with significant second order terms the gain fluctuations can clearly be problematic.

### 5.1.2 Multiplier Packaging

The InP HBT multipliers were wafer tested to establish functionality and were then integrated into a suitable package to allow more extensive tests in a

low noise shielded environment. The package consisted of a brass block with a centre recess. Inside the recess a small microwave laminate was attached with conductive epoxy to the base of the recess. On the laminate was patterned microwave transmission lines to convey the input and output signals from SMA connectors fixed to the sides of the package. As in the case of the digitiser package discussed previously, the copper surfaces of the laminate were plated with 0.5  $\mu\text{m}$  of Au over 4  $\mu\text{m}$  of Ni to provide mechanical bond pad stability and provide the correct metallurgical conditions for reliable bonding with Au bond wire. The multiplier is directly attached to the base of the package with conductive epoxy through a cut out in the microwave laminate. The input and output signals were connected to the bond pads on the laminate with thermo-sonic wedge bonded Au wire bonds. Figure 5.5 shows the interior of the package with the multiplier in place. Not visible

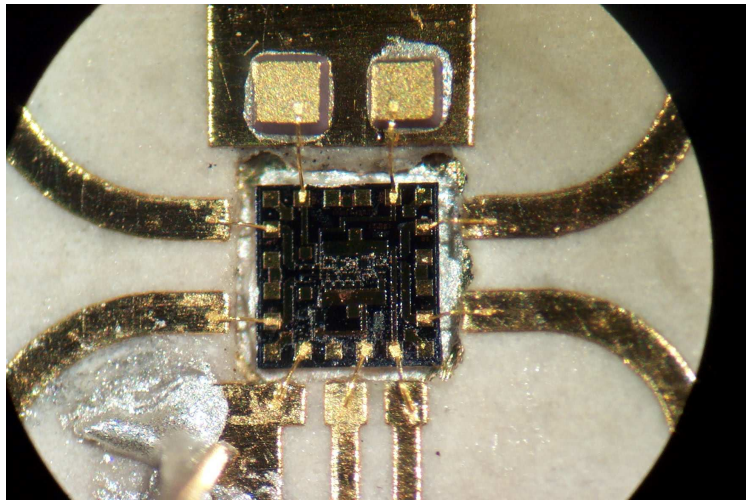


Figure 5.5: Bonded multiplier IC.

are DC blocking capacitors on the input of value 1 pF. The capacitors near the top of the IC are decoupling capacitors of value 0.3 pF on the inverting inputs to provide an AC ground and to short out any output signal coupled into the inverting inputs. Figure 5.6 displays the full test package with the input and output connectors visible.

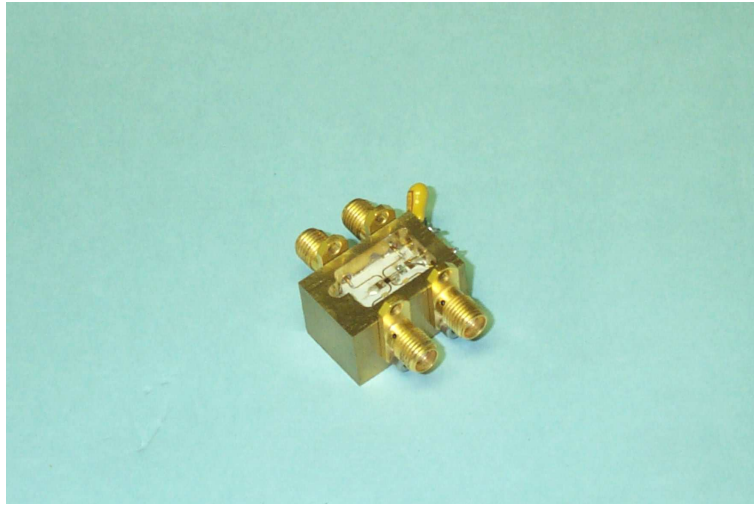


Figure 5.6: InP multiplier test package.

### 5.1.3 Test Results

The InP HBT multiplier was tested for bandwidth, linearity, dynamic range and low frequency noise.

#### Multiplication Bandwidth

The multiplication bandwidth was measured by applying two sinusoidal sources to the inputs that were phase locked, but differ in frequency by a constant offset of 10 kHz. The amplitude of the output 10 kHz beat signal was then measured as the two signal sources were stepped in frequency, keeping the constant 10 kHz offset between them. Input power level was set at -15 dBm on both inputs. The differential outputs of the multiplier were DC coupled to a low noise differential amplifier, Burr-Brown part number INA103 [77], configured for a gain 120. The output could then be easily observed on an oscilloscope or spectrum analyser. Figure 5.7 shows the measured multiplication bandwidth for the packaged multiplier. The -3dB bandwidth is approximately 15.5 GHz, which compares to the value of 15 GHz derived from simulation. The low frequency cutoff is due to the 1 pF DC blocking capacitors on the inputs but the response extends in principle down to

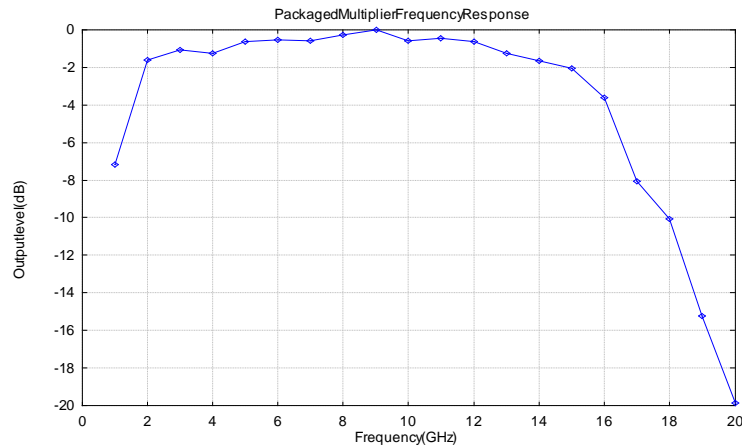


Figure 5.7: InP multiplier bandwidth.

DC. A rather small value of DC blocking capacitance was chosen so that the self-resonance frequency of the capacitor would be above the anticipated maximum operation frequency of the multiplier, allowing a true determination of the upper frequency limit of the device.

### Linearity

Linearity was measured at a frequency of 5 GHz by measuring output power as a function of input power as the input power on both inputs is swept from +1 dBm to -20 dBm. The measured results are displayed in Figure 5.8. As expected by design the circuit is linear below approximately -5 dBm.

### Dynamic Range

A multiplier can be used as a mixer and active multipliers such as the present circuit are often used in this capacity. They have the advantage that they can be designed for conversion gain where as diode based mixers always incur substantial conversion loss. Conversely, diode mixers have much lower noise than active mixers. The present multiplier does not exhibit conversion gain when used as a mixer because it was designed for linearity, sacrificing some of the gain. To characterise the device as a mixer the dynamic range of the multiplier when used in this capacity was measured. The maximum output

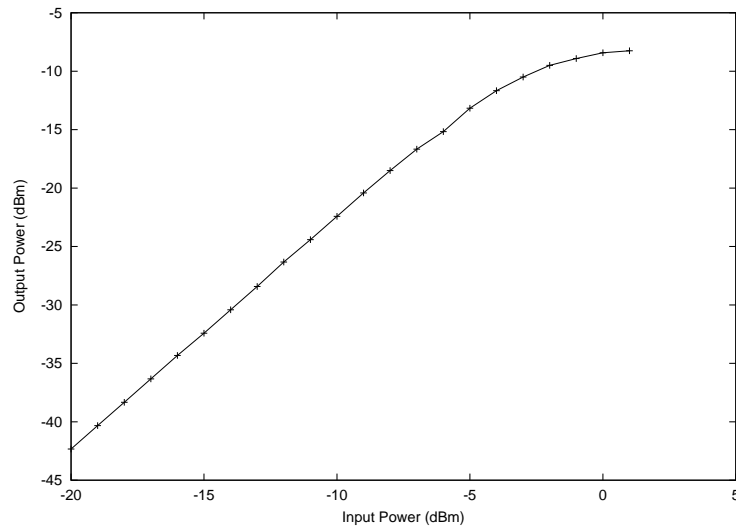


Figure 5.8: InP multiplier linearity.

signal level is set by the 1 dB compression point, that is the power level at which the output power is 1 dB below the extrapolation from lower power levels. The minimum output level is that where the output is just visible above the noise floor. The particular definition of dynamic range adopted is the difference between the 1 dB compression point and the minimum discernable signal. [78].

The local oscillator power level was set at 0 dBm, in order to fully switch the local oscillator transistors, and the measurements were performed at an RF frequency of 5 GHz, and an IF of 100 MHz. The measured 1 dB compression point was at -5 dBm input power. The input power which gave an output just visible above the noise floor was -106 dBm, at a resolution bandwidth of 100 Hz. This gives a dynamic range of 101 dB for the multiplier.

### Low Frequency Noise

The low frequency noise was measured using the arrangement described for measuring the multiplication bandwidth. That is a low noise DC coupled differential amplifier was connected to the differential outputs of the multiplier. The low noise of the differential amplifier, combined with its gain,

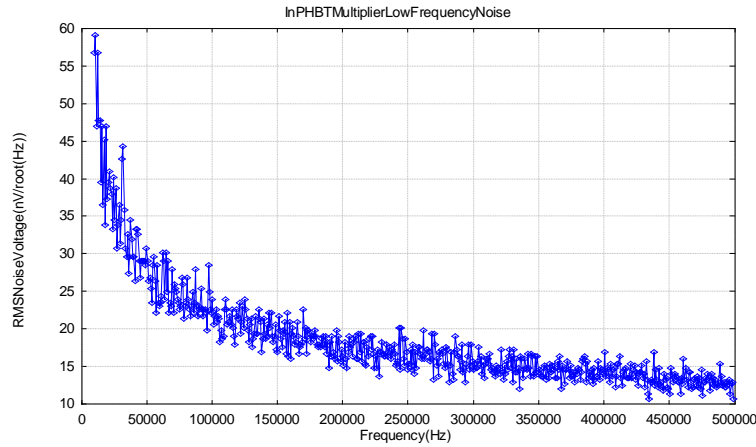


Figure 5.9: InP multiplier low frequency noise.

ensures that the post amplifier does not affect the noise measurement. This was verified by removing the device under test and noting that the noise power measured dropped by over 20 dB, verifying that the post amplifier contributes at most 1% of the measured noise. The noise measurement was performed by observing the amplified output, with the inputs undriven, on a spectrum analyser. The HP6163 spectrum analyser extends down to 30 Hz so is suitable for low frequency noise measurements. The resulting spectrum was then captured and corrected for the gain of the post amplifier. Figure 5.9 shows the measured low frequency noise spectrum at the multipliers' output. Immediately obvious from figure 5.9 is that the low frequency noise spectral density is high. It is much greater than the  $3 \text{ nV}/\sqrt{\text{Hz}}$  thermal and shot noise spectral density. The corner frequency is of the order of a few hundred kilohertz, which is much poorer than silicon, though superior to GaAs or InP HEMTs [80, 31]. It was previously derived that the measurement variance noise using this multiplier at full bandwidth is  $52 \text{ nV}/\sqrt{\text{Hz}}$ . To contribute less than 1% to this the noise spectral density due to device noise must be less than  $5 \text{ nV}/\sqrt{\text{Hz}}$ . This is barely above the noise contributed by thermal and shot sources and highlights the problems involved in very high bandwidth systems. The enormous bandwidth leads to very high sensitivity of the measurement and so puts very stringent noise requirements on back-end

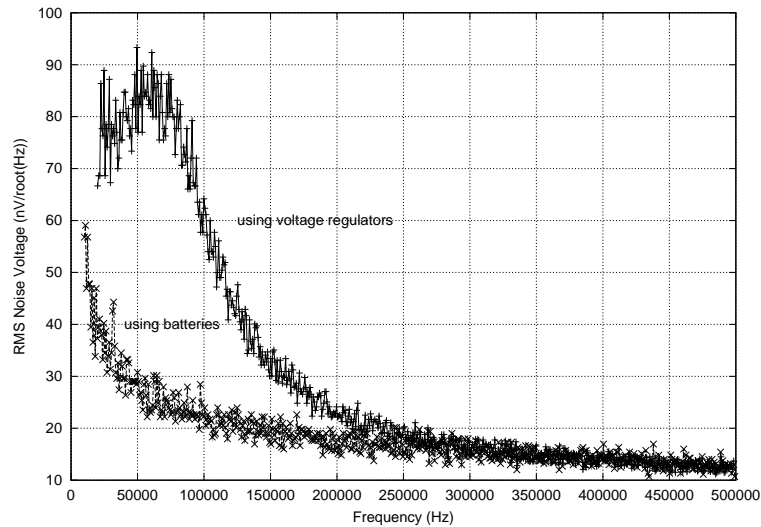


Figure 5.10: Comparison of low frequency noise with regulated and battery supplies.

components down the signal processing chain. It is usually taken for granted that after the low noise amplifiers in the receivers the noise performance of the following components is unimportant, within reason. The present example clearly shows that for very high bandwidth systems this assumption must be reevaluated.

From figure 5.9 it is seen that using this multiplier in practise requires high phase switching frequencies of the order of 500 kHz to avoid unacceptable signal to noise degradation. At this frequency the device noise is approximately  $12 \text{ nV}/\sqrt{\text{Hz}}$ . This leads to a sensitivity degradation of 5%, which while not ideal, is acceptable in most situations given the huge bandwidth advantage that the device provides.

Also of interest is that for the low frequency noise measurement it was necessary to drive the multiplier from battery voltage supplies, as the use of regulated supplies contributed a great deal of low frequency noise. Figure 5.10 shows the low frequency noise measurement using supplies derived via the ubiquitous LM317 and LM337 [79] voltage regulators in comparison with that using battery voltage supplies. It is clear that in practical use of this

device a lot of care needs to be taken in developing low noise voltage supplies.

### Yield

There were a total of 120 multiplier circuits on the 5 wafers returned from manufacturing. Each of these were individually tested and 115 of these were found to be functional, indicating a yield for this circuit of 96 %.

## 5.2 SiGe Multiplier

The previous section dealing with the InP multiplier highlighted the need for low 1/f noise devices in the design of multipliers for analogue correlators. To this end alternative technologies were investigated that could potentially offer much lower 1/f noise whilst achieving the wide bandwidth requirements. It is well known that silicon offers low 1/f noise but it cannot provide the wide bandwidths. A recent process technology that holds promise is that of SiGe HBT. This uses a modified silicon process which incorporates germanium into the base of the transistors to provide heterojunction bipolar transistors. SiGe HBTs share similar low 1/f noise properties to silicon [80, 81] but in addition provide much faster transistors. The latest research grade SiGe processes offer transistor  $f_{ts}$  and  $f_{max}$ s comparable to GaAs and InP, though requiring much smaller device geometries to achieve this [30]. The chief disadvantage of SiGe is that conventional silicon is a conductive substrate and so incurs high transmission line losses compared to the insulating substrates of GaAs and InP. This is compounded by the need to bias the conducting silicon substrate with the most negative supply in the circuit, enhancing the device to substrate capacitive parasitics.

In order to evaluate the performance of SiGe in multiplier applications a SiGe analogue multiplier was designed using the Austria Microsystems (AMS) 0.8 um SiGe BiCMOS process [82]. This process offers SiGe HBTs with  $f_{ts}$  of approximately 25 GHz. Whilst modest compared to the InP process and high speed SiGe processes, this is sufficient to get some idea



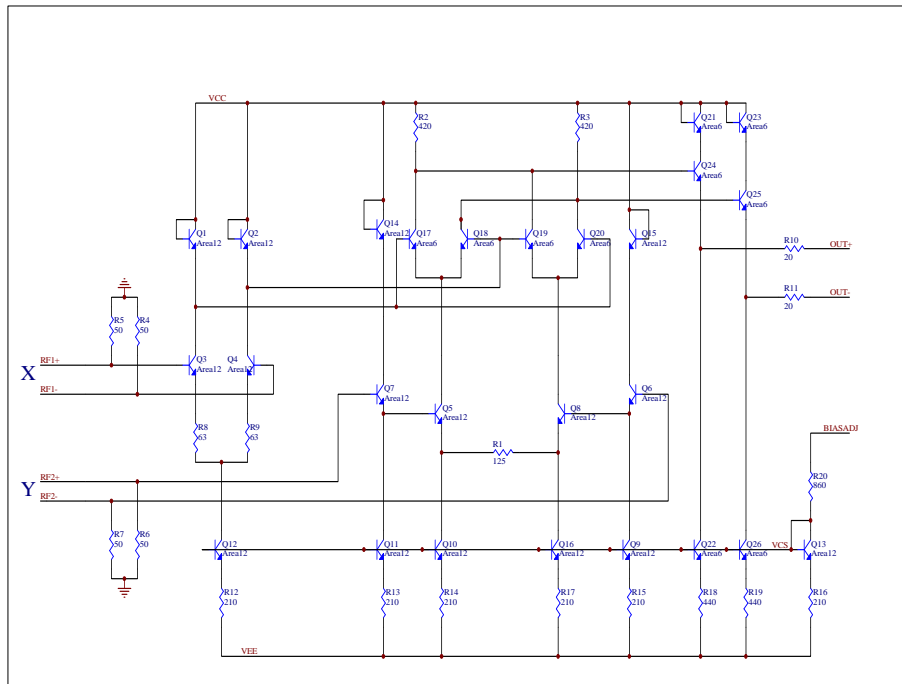


Figure 5.11: SiGe multiplier schematic.

of how SiGe performs, especially in the area of low frequency noise. This could then provide justification to pursue a full bandwidth multiplier design in a higher speed, high cost, SiGe process. Analogue multipliers have been designed using SiGe before such as the device presented in [83] which displays a bandwidth of 12 GHz using a process with  $f_T$  of 47 GHz. This circuit was designed for use as an active mixer. No information was presented concerning the low frequency noise of this multiplier.

The circuit schematic of the SiGe multiplier that was designed is presented in figure 5.11. The circuit is similar in concept to the InP multiplier. The simulations indicated a -3 dB multiplication bandwidth of 6 GHz and a gain factor of 22. Total DC current drawn was designed to be 13 mA with a total power dissipation of 52 mW with supplies of +1 V and -3 V. Similarly to the InP multiplier an external pad allows the current bias of the circuit to be raised or lowered by application of an external voltage. The nominal design value is programmed by connecting this pad to ground.

Figure 5.12 shows the layout of the SiGe multiplier chip. The chip was

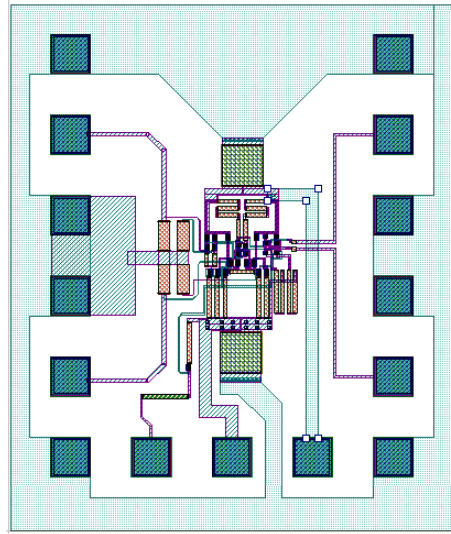


Figure 5.12: SiGe multiplier layout.

designed as a collaborative effort between the CSIRO, Australia Telescope National Facility and the National Taiwan University as part of a broad collaborative project between the two institutions dealing with radio astronomical instrumentation. The circuit design and core multiplier layout was performed by the author. Addition of extra ground metallisation and arranging fabrication was performed by National Taiwan University.

### 5.2.1 SiGe Multiplier Tests

Following fabrication the SiGe multipliers were tested in the same fashion as the InP multiplier chips. The circuit samples (5 chips in total) were returned from the AMS foundry individually diced so were remounted with wax on a glass slide for wafer probing with a probe station. DC current draw of the devices was 13 mA, consistent with the value expected from design. Of the 5 samples obtained all circuits were functional.

#### Multiplication Bandwidth

For the multiplier bandwidth measurements the circuits were driven from two phase locked synthesisers with a constant frequency offset of 100 kHz.

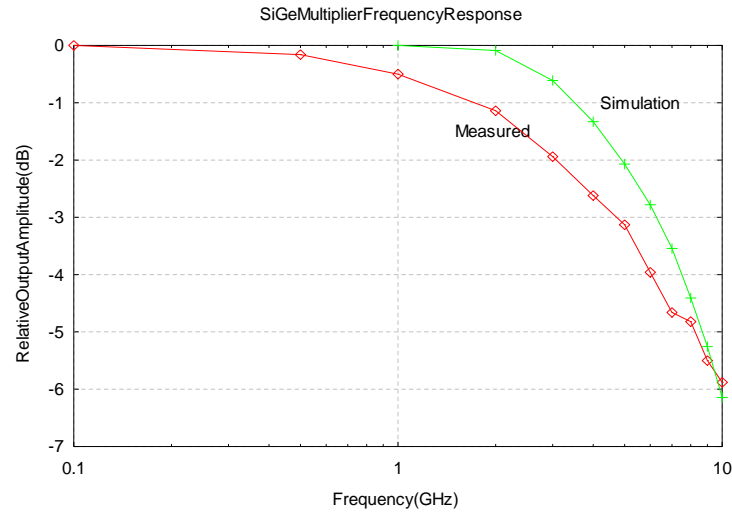


Figure 5.13: Bandwidth of SiGe multiplier.

The amplitude of the 100 kHz difference tone was observed on a spectrum analyser as the synthesisers were swept in frequency keeping the 100 kHz frequency offset. Figure 5.13 displays the result of the multiplier bandwidth measurements. Included for comparison is the result derived from simulation. The -3 dB bandwidth is approximately 5 GHz with a -6dB bandwidth of 10 GHz. It is clear from the results that the fabricated multiplier displays somewhat less bandwidth than predicted from the simulations. In trying to explain this discrepancy it appeared that possibly there was more loss in the input transmission lines than expected. From the layout in figure 5.12 it is seen that there is approximately 360  $\mu\text{m}$  of input transmission line from the input pads to the multiplier core. This line was not initially modelled in the simulation. This input transmission line is a form of coplanar waveguide on lossy silicon, as the SiGe process does not have a backside ground plane, unlike the InP process. The ground return for the SiGe transmission line is through the adjacent ground metallisation on the same layer forming a coplanar waveguide. To estimate the effect of the input transmission line it was analysed using the SonnetLite electromagnetic simulation package [84]. A 360  $\mu\text{m}$  long, 10  $\mu\text{m}$  wide transmission line with adjacent ground metalli-

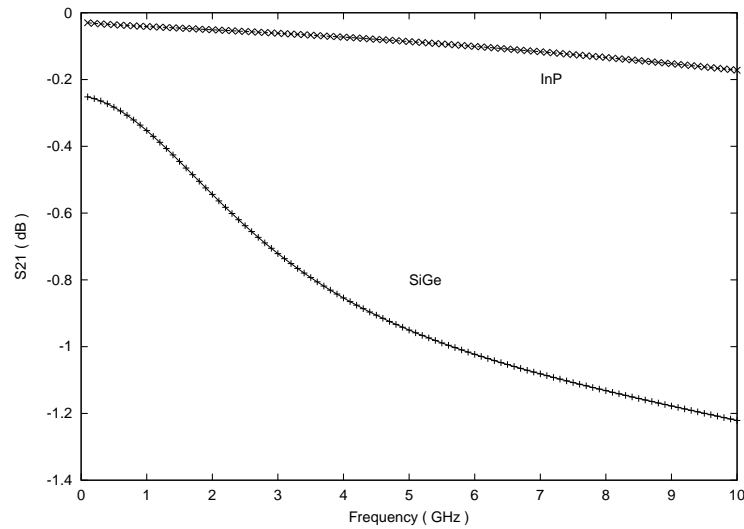


Figure 5.14: Comparison of transmission loss on Si and InP.

sation at 150  $\mu\text{m}$  spacing was constructed to approximate that on the chip. The substrate material was 500  $\mu\text{m}$  thick lossy silicon as specified in the AMS process parameters ( dielectric constant 11.9 with resistivity  $\approx 20\Omega\text{m}$ , by contrast InP is  $10^6 - 10^7\Omega\text{m}$ ). The transmission metal is separated from the substrate by 0.5  $\mu\text{m}$  of field oxide with dielectric constant 3.9. The metallisation for the SiGe process is predominantly aluminium of thickness 0.6  $\mu\text{m}$  giving a sheet resistance of 0.08 ohms per square. By contrast the InP process has thick gold metallisation of several microns giving a much lower sheet resistance. Figure 5.14 gives the result of simulating the input transmission line and displaying the  $S_{21}$  of the transmission line. Included for comparison are the results for the same structure using the InP process material parameters. The loss on the silicon substrate is surprisingly high. The loss of approximately 0.25 dB at DC is also real as the considerable sheet resistance leads to a DC resistance of about 2 ohms for the input transmission line. Including this loss in the simulation results gives a new predicted -3 dB bandwidth of 4.6 GHz, slightly less than the measured value of 5 GHz. This supports the hypothesis than input transmission line loss is the dominant cause of loss of bandwidth in this design. The loss has been overestimated

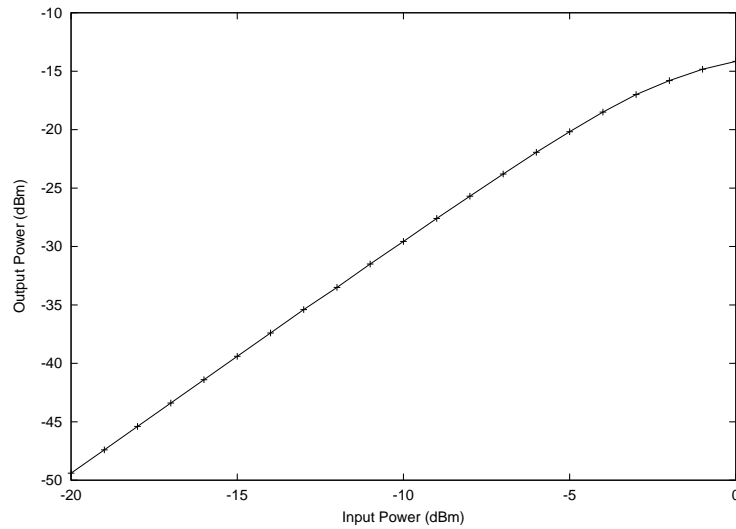


Figure 5.15: SiGe Multiplier linearity.

slightly, but is reasonable given the coarse approximation to the true structure on the chip used in the electromagnetic analysis, and the uncertainty in the conductivity of the silicon substrate.

### Linearity

Linearity was measured at a frequency of 5 GHz by driving the multiplier with equal amplitude sources offset in frequency by 100 kHz and observing the amplitude of the 100 kHz difference tone. The input amplitude was then swept from -20 dBm to 0 dBm noting the change in output tone amplitude. The measurement results are presented in figure 5.15 which indicate the circuit is linear below approximately -5 dBm consistent with design.

### Low Frequency Noise

In order to measure the low frequency noise the devices were removed from the glass mounting plate and a single device was remounted on a test printed circuit board with wire bond connections for input, output and power. This was required as the wafer probing setup is too noisy for a highly sensitive measurement such as this due to the need to have long connections from

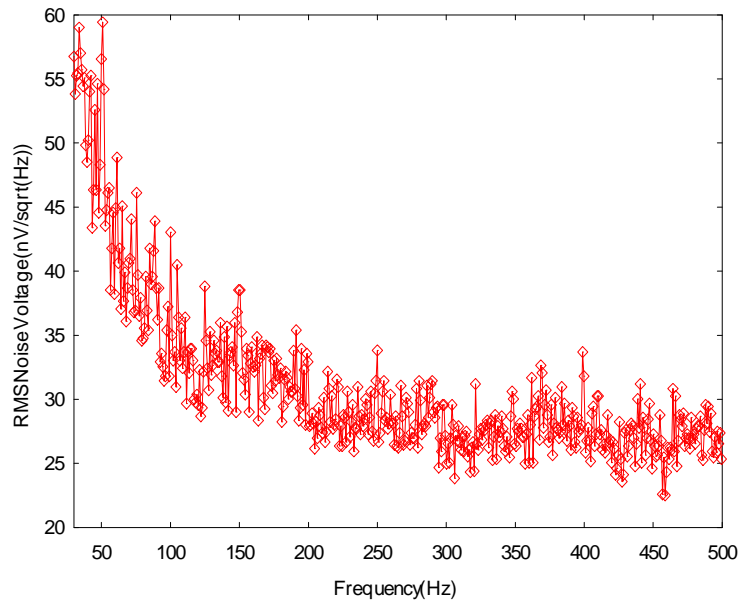


Figure 5.16: SiGe multiplier low frequency noise.

power, input and output to the device under test, which are then sensitive to pickup. The device was powered from a battery source and the same low noise differential post amplifier as previously connected to the outputs before observing the amplified noise on a HP6163 spectrum analyzer.

The result for output noise voltage spectral density, after correcting for the post amplifier gain, is shown in figure 5.16. The spectrum is essentially flat beyond a few hundred hertz so only the spectrum up to 500 hertz is shown. The limiting spectral density of about  $23nV/\sqrt{Hz}$  compares with the value of  $20nV/\sqrt{Hz}$  derived from simulation as a result of the thermal and shot noise sources alone. The contribution due to flicker noise is small and the spectrum indicates the flicker noise corner frequency is about 300 hertz.

### 5.2.2 Discussion

It is clear from the results in the previous section that loss in the silicon substrate is a serious problem. The losses encountered in this design make it very

hard to imagine designing multipliers with tens of gigahertz of bandwidth in this process.

To overcome this and other problems several semiconductor foundries around the world are investigating various forms of silicon on insulator technology. All the approaches have in common the idea of placing an insulating layer between the interconnect and active devices, and the lossy silicon. The insulator is generally thick silicon dioxide or sapphire. This reduces the dielectric loss in the silicon and the device parasitic capacitances, along with other benefits [85, 86]. Commercial processes based on these technologies are now available.

A simple alternative enhancement is the use of high resistivity silicon substrates. These are more expensive than conventional silicon substrates pushing the cost to similar levels as for a GaAs process which would probably be preferred in most instances. For special cases like the present where specific properties of silicon are required the extra cost could be justified. The improvements can be dramatic when using high resistivity silicon as shown in [87] where reductions in loss by over a hundred are demonstrated.

Another approach uses MEMS (micro electro-mechanical systems) technology. In this approach MEMS techniques are used to etch away most of the silicon from underneath the interconnects and leave them suspended in air with a small number of silicon posts [88]. By removing the lossy substrate in the region where the electric fields lines of the transmission line exist the transmission loss can be greatly reduced.

Even in the conventional silicon process used to design the SiGe multiplier there is probably much that can be done to reduce the transmission losses. Apart from ensuring all high frequency transmission lines are as short as possible one approach that is worth considering is using the two metals available in the process to form an on-chip microstrip structure [56]. A grounded wide strip of the bottom metal is placed as a ground plane and a thin strip of top metal above this to form a local microstrip transmission line. Between the two metals exists a layer of approximately 1.5  $\mu\text{m}$  of silicon dioxide in

the AMS process. One would expect with this structure that most of the field is contained between the two conductors and not in the lossy substrate. This approach has been used in [89] with a relatively thick  $12\ \mu\text{m}$  polyimide dielectric between the two metal layers, and a silicon dioxide insulator layer between the bottom metal and the substrate, to achieve transmission line losses of less than 0.15 dB/mm at 10 GHz in a SiGe HBT process.

The SiGe HBT has extremely good low frequency noise performance. The measured corner frequency of a few hundred hertz compares to several hundred kilohertz for InP and GaAs HBT and megahertz for HEMT devices. This provides a good case for the use of SiGe technology in analogue multipliers for interferometers if the loss problems can be overcome.



## Chapter 6

# Photonic Multipliers and Digitisers

The previous chapters have dealt with enhancing the speed and performance of digitisers and multipliers using semiconductor technology. Whilst semiconductor processes will continue to rapidly advance, allowing even wider bandwidth digitisers and multipliers to be designed, a large jump in performance of 5 to 10 times will most likely require a fundamental technology shift. To that end I decided to investigate if the very wide bandwidth signal processing capability of photonics could be harnessed to realise multipliers and digitisers with greater bandwidth than attainable through purely integrated circuit means. In this chapter I will first present a new design for a photonic multiplier that has the ability to process much greater bandwidths than the analogue multipliers presented earlier. I will examine this multiplier's application to radio astronomy interferometers and analyse its noise performance in this role. Following this, I will present some of the recent work that has been occurring in the field of photonic A/D conversion and how it may be of use in digitisers for radio astronomy.

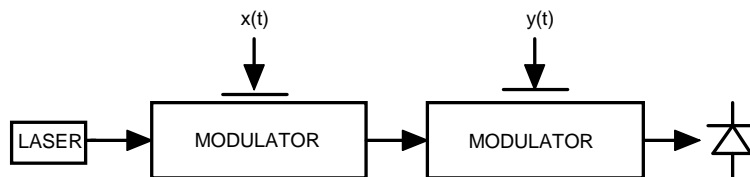


Figure 6.1: Photonic multiplier.

## 6.1 Photonic Multiplier

It would be very advantageous to be able to use multipliers with even greater bandwidth than the devices presented in the previous chapter due to the greater sensitivity that wider bandwidths can provide, as reflected in the radiometer equation, equation 1.1. In this section I will present a new system for wide bandwidth signal multiplication using in-fibre photonics.

Consider the arrangement depicted in figure 6.1 which shows two cascaded optical intensity modulators fed from a constant power laser source. One of the modulators is excited by a microwave signal  $x(t)$ , the second by a signal  $y(t)$ . This arrangement has been studied previously in the context of mixers for microwave frequency translation [90]. There seems to have been no work done on the possibility of using this arrangement for wide bandwidth signal multiplication. A single optical modulator has the transfer function, in the case of a conventional Mach-Zehnder type optical intensity modulator, of

$$I(t) = \frac{I_0}{2} \left( 1 + \sin\left(\frac{\pi x(t)}{V_\pi}\right) \right), \quad (6.1)$$

where  $I(t)$  is the output optical intensity,  $I_0$  is the constant incident optical intensity,  $x(t)$  is the modulating voltage and  $V_\pi$  is a device specific constant known as the half wave voltage, as it is the applied voltage required to change the intensity to half of its maximum value. For small intensity changes about the half intensity point of  $\frac{I_0}{2}$  this transfer function can be linearised to

$$I(t) = \frac{I_0}{2} \left( 1 + \frac{\pi x(t)}{V_\pi} \right). \quad (6.2)$$

If two intensity modulators are cascaded the final transfer function for small

signal inputs is

$$I(t) = \frac{I_0}{4} \left(1 + \frac{\pi x(t)}{V_\pi}\right) \left(1 + \frac{\pi y(t)}{V_\pi}\right) \quad (6.3)$$

When this optical signal is detected in a photodiode of responsivity  $\eta$  and time averaged in a low pass filter the resulting output voltage  $V$  is

$$V = \langle \eta I(t) \rangle = \frac{\eta I_0}{4} + \frac{\eta I_0 \pi}{4V_\pi} \langle x(t) \rangle + \frac{\eta I_0 \pi}{4V_\pi} \langle y(t) \rangle + \frac{\eta I_0 \pi^2}{4V_\pi^2} \langle x(t)y(t) \rangle, \quad (6.4)$$

where  $\langle \rangle$  is the expectation operator. Since the input signals are zero mean this reduces to

$$V = \langle \eta I(t) \rangle = \frac{\eta I_0}{4} + \frac{\eta I_0 \pi^2}{4V_\pi^2} \langle x(t)y(t) \rangle, \quad (6.5)$$

The output voltage thus comprises of a constant term equal to one quarter of the detected incident optical intensity plus a term proportional to the time averaged product of the input signals. This time averaged product of the input signals is precisely the quantity that we require when using a multiplier in an interferometer. The problem then remains how to separate the small required term from the much larger background constant term. This can be accomplished using phase switching and synchronous detection. One of the inputs is inverted periodically, with a 50% duty cycle switching signal, and the output of the multiplier synchronously switched between +1 and -1 before being passed to a low pass filter. The constant term is removed, as it does not change sign with inversion of the signal, and the wanted signal is recovered as the output of the low pass filter. As with the integrated circuit multiplier, the switching frequency should be chosen so as to put the final detection bandwidth far enough out in frequency so that low frequency noise is minimised.

In order to test the operation of the photonic multiplier the experimental setup of figure 6.2 was constructed. This setup tests the operation of the multiplier by using it as a phase detector [91]. If two locked sinusoidal signals are applied to the two inputs of an ideal multiplier it is well known from simple trigonometry that the DC output is proportional to the cosine of the

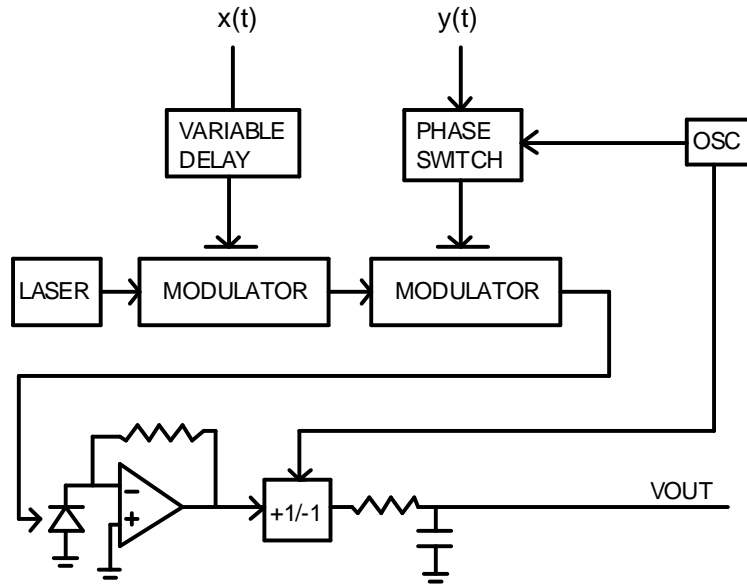


Figure 6.2: Photonic multiplier experiment setup.

phase difference between the two input signals. Explicitly,

$$\sin(\omega t)\sin(\omega t + \phi) = \frac{1}{2}\cos(\phi) + \frac{1}{2}\cos(2\omega t + \phi). \quad (6.6)$$

Thus, by varying the phase difference between the two input signals the output should describe a sinusoid if the photonic multiplier is truly acting as a linear multiplier. The intensity modulators that were available for this experiment had a 2.5 GHz -3db electrical bandwidth. The experiment was performed at an RF frequency of 1 GHz as this was limited by the signal generator available and the length of the delay line. Figure 6.3 shows the result of the experiment which clearly shows the sinusoidal output voltage as a function of phase difference. The total phase range is about 180 degrees, limited by the length of the variable delay line available. Phase switching was performed at a frequency of 100 Hz, phase locked to the mains 50 Hz so as to reject mains pickup. The schematics of the transimpedance amplifier and synchronous detector constructed for this experiment are presented in appendix A.

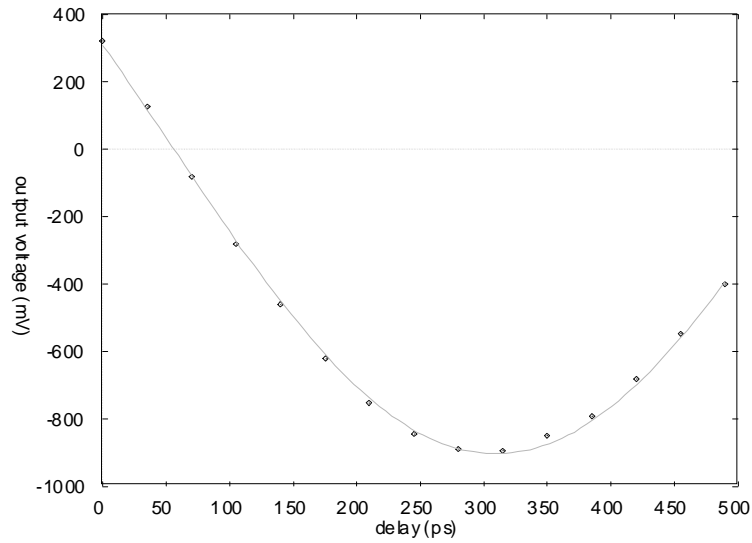


Figure 6.3: Result of phase detection experiment.

### 6.1.1 Discussion

The foregoing gives a proof of principle demonstration that the proposed photonic multiplier is capable of acting as a multiplier in a wide band interferometer application. Whilst this demonstration was performed at a frequency of only 1 GHz, as limited by available components, the principle is valid up to the bandwidth capability of the modulators used. Currently, optical intensity and electro-absorption modulators with bandwidths of about 40 GHz are available commercially [92] and research devices with two to three times this bandwidth are regularly reported [93]. Thus, the scheme has the potential for providing extremely wide bandwidth multiplication. In addition, the proposed multiplier uses only in-fibre components and requires no free space optics, which would help greatly in realising a robust and stable system that does not require regular calibration and alignment.

### 6.1.2 Noise Analysis

The extremely noise-critical interferometer application means that the noise performance of the proposed photonic multiplier is just as critical as its ability

to achieve wide bandwidths. There are three main noise sources that generate additional noise in the photonic multiplier output. These are 1) Shot noise generated by the photodetector current. 2) Thermal noise generated in the photodiode load impedance and 3) Relative intensity noise ( RIN ) generated in the laser.

Looking at the expression of equation 6.4 for the output of the photonic multiplier the wanted signal term is the last term in the expression. The measurement noise of this term is governed by the usual radiometer equation 5.3 and we require other external noise sources to be much smaller than this measurement variance noise to not degrade the system sensitivity. The two terms involving the average values of the input signals  $x(t)$  and  $y(t)$  have average values of zero over an infinite measurement period, since they are AC coupled signals, but their variance over any finite time period is not necessarily zero, and so they have the ability to add noise. However, if the input signals are bandpass signals with a spectrum starting from some lower frequency value well above the band of the detection low pass filter then they will be completely filtered and will add no additional noise. This would certainly be the case in practice as the final detection bandwidth would be centred about a frequency in the kilohertz range whereas the signal bandpass would begin somewhere in the vicinity of a gigahertz for wide bandwidth systems ( a typical signal band could be 1 - 20 GHz for instance).

Looking at the physical noise sources in turn we have

1) Shot Noise

The current in the photodetector is dominated by the large DC term in equation 6.4. Hence the shot noise current spectral density introduced in the photodetector is

$$\langle i_s^2(f) \rangle = \frac{e\eta I_0}{2}, \quad A^2/Hz \quad (6.7)$$

where  $e$  is the electronic charge.

2) Thermal noise

Thermal noise spectral density in the detector's load resistance is given by

the Johnson relation

$$\langle v_t^2(f) \rangle = 4kTR, \quad V^2/Hz \quad (6.8)$$

where  $k$  is Boltzman's constant,  $T$  is the absolute temperature and  $R$  is the load resistance.

### 3) Relative Intensity Noise

Relative intensity noise (RIN) describes the fluctuations of the lasers output power about the mean power level. RIN is defined as a spectral density [94] where the definition is

$$RIN(f) = \frac{\langle I_{RIN}^2 \rangle}{I^2} \quad Hz^{-1}, \quad (6.9)$$

where  $I$  is the mean power level. Though RIN is usually quoted as a single spectral density figure for a laser its spectrum is not white. A typical value of RIN is -140 dB / Hz. Low RIN lasers can improve on this by over 20 dB.

In the present case, the received optical power is dominated by the large constant term equal to one quarter of the incident optical power emitted from the laser. Hence, the noise current power spectral density resulting from the laser RIN is given by

$$\langle i_{RIN}^2(f) \rangle = \frac{\eta^2 I_0^2}{16} RIN(f) \quad A^2/Hz. \quad (6.10)$$

Using these three expressions the total noise power spectral density developed across the detector load resistance is

$$\langle v_N^2(f) \rangle = \frac{\eta^2 I_0^2 R^2}{16} RIN(f) + 4kTR + \frac{e\eta I_0}{2} R^2 \quad V^2/Hz. \quad (6.11)$$

The measurement variance noise power spectral density in the signal across the detector load resistance is given from equation 5.5 as

$$\langle v_n^2(f) \rangle = \frac{\pi}{B} \left( \frac{\eta I_0 \pi^2 R}{4V_{pi}^2} \langle x(t)y(t) \rangle \right)^2 \quad V^2/Hz, \quad (6.12)$$

evaluated at the 100% correlated input condition of  $x(t) = y(t)$ , and at the maximum input power level.

Ideally, we would like the additive noise power due to shot, thermal and RIN noise to be 20 dB or more below the measurement variance. To get an idea of the magnitude of the terms for a typical device in a typical system consider the following representative system - A cw laser of power 4 mW with a RIN of -150 dB/Hz combined with two conventional Mach-Zehnder intensity modulators with  $V_\pi$  of 4 V. The bandwidth of the measurement is 10 GHz. A photodiode of responsivity of 0.8 is used with a load resistance of 1000  $\Omega$ .

The shot noise as given by equation 6.7 is dominated by the 1 mW of average optical power that reaches the photodetector leading to a constant 0.8 mA through the photodiode. The magnitude of the noise voltage spectral density developed across the load resistance by the shot noise current is  $2.56 \times 10^{-16} \text{ V}^2/\text{Hz}$ .

The RIN noise contribution across the load resistance is again dominated by the large average optical power that reaches the detector. It has a magnitude of  $6.4 \times 10^{-16} \text{ V}^2/\text{Hz}$ .

The thermal noise in the load resistance has a magnitude of  $1.6 \times 10^{-17} \text{ V}^2/\text{Hz}$ .

Thus the total noise across the load is  $9.0 \times 10^{-16} \text{ V}^2/\text{Hz}$ , dominated by RIN noise.

The measurement variance noise is given by equation 6.12. This is dependent upon the power levels of the input signals. The input power level is limited by the linearity of the modulator transfer function. For a conventional Mach-Zehnder modulator with raised cosine transfer function and biased about quadrature, the signal excursion is limited to about 0.08 of  $V_\pi$ , for a maximum deviation of 1% from linearity. Taking this as the peak deviation, and assuming an effective crest factor of 4 for a white noise gaussian distributed signal, then the rms input voltage level of each input is  $0.02V_\pi$ . With these parameters and a 10 GHz bandwidth the measurement variance noise power spectral density is  $3.1 \times 10^{-15} \text{ V}^2/\text{Hz}$ .

The noise from external sources is about one third of the measurement



variance. The problem is that the noise sources are dominated by the large average current that exists in the photo-detector, combined with the small value of the wanted signal term. The signal term current is about  $10^{-4}$  of the bias DC term. The chief noise source is the considerable RIN of the laser. Looking at the expression for device and measurement noise in equations 6.11 and 6.12, a few things can be noticed. While the RIN, shot noise and measurement noise are proportional to  $R^2$  the thermal noise is proportional to  $R$ . Thus, thermal noise can be made relatively unimportant by making the load resistance high enough. Likewise, signal and RIN noise are proportional to  $I_0^2$  whilst the shot noise is proportional to  $I_0$  thus the shot noise can be made relatively small by a large enough value of  $I_0$ . The choice of a high power laser and large load resistance gives a situation where the noise is totally RIN dominated.

What can be done to improve the signal to noise ratio? A few things are possible. First of all using a lower RIN laser. A good laser optimised for low RIN can have a RIN of less than -160 dB. This would reduce the RIN noise contribution to a tenth of its value in the calculation above. The resulting noise level would still degrade the sensitivity by about 10% which is generally unacceptable.

Another obvious way is to increase the signal level. This is limited by the non-linear transfer function of the optical intensity modulator. If the modulators' transfer function could be linearised this would aid enormously. A wide field of research is devoted to exactly this problem of designing linearised modulators for dynamic range enhancement in analogue optical links [95, 96]. If the modulator could be driven just twice as far from the bias point in the previous example, combined with a low RIN laser, the signal-to-noise improvement would be over 20 dB and the sensitivity degradation would be less than 1%.

A third possibility is that since the dominant noise source is RIN, and this is a property of the optical source, it could be measured and removed from the detected signal with a balanced receiver architecture. This could be

quite feasible in the present situation since the output bandwidth required is only of the order of kilohertz, so measuring and removing to some degree the RIN noise over this bandwidth would be practical in a number of ways. This method of RIN reduction through balanced receiver architectures has been pursued previously for wide dynamic range direct detection links [97, 98]. A typical architecture used in these references, and which is applicable in the present case, is shown in figure 6.4. The optical source is split before one

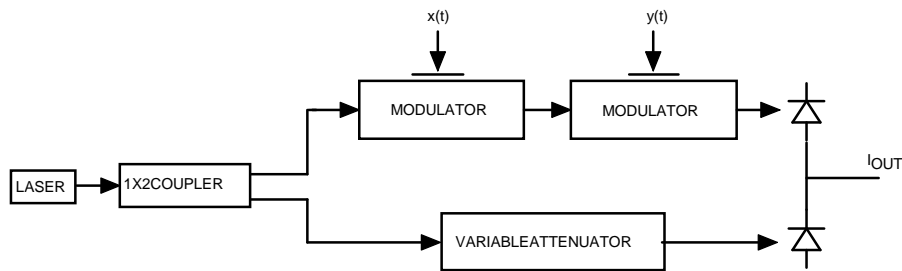


Figure 6.4: Balanced receiver for RIN reduction.

half passes through the modulators, the other half through an attenuator to match the optical loss in the parallel path. The two signals are then photo-detected in a receiver with a differential architecture, in this case simply two photodiodes in a differencing arrangement, but considering the low frequency output bandwidth of the current application a system comprising of active electronics may well give better performance. In [98] a typical improvement of 10 dB in RIN noise was observed at an RF frequency of 900 MHz. At the much lower frequencies in the current application better performance would be expected. Practical investigation of the various schemes has not been performed but is a topic for further research in this area.

## 6.2 Photonic Digitisers

In the last few years there has been much interest in the topic of photonically assisted A/D conversion [99, 100, 101]. As this is an important and fast growing area which could well have impact upon digitisers for radio astron-

omy in the future, I will briefly describe the key properties of this method, and how it might be used in a future radio astronomy application.

The central idea behind photonically assisted A/D conversion is that very short optical pulses can be used to perform almost ideal sampling of electrical signals since the optical pulses are so short in time [102]. These pulses are typically of the order of a picosecond in width. The sampling transducer is usually an optical intensity modulator or phase modulator. Quantisation then usually takes place in the electrical domain after the amplitude modulated sample pulses have been detected and pulse stretched. The key features which make this approach so promising are:

- 1) Optical pulse sources can be made with over 100 times less jitter than electronic sampling circuits. The best electronic sampling circuits have measured jitter greater than about 0.5 ps whereas optical pulse sources with less than 50 fs of jitter have been measured [103]. Given the effect of timing jitter on SNR of the sampled data, expressed in equation 3.11, a limit of 0.5 ps of jitter places severe limits on the upper frequency of sampling. For instance, at a sampling rate of 4 giga-samples/s, 0.5 ps of jitter limits the SNR to less than 7 bits for Nyquist rate sampling. Whilst currently high resolution ADCs are not commonly used in radio astronomy this is likely to change in the future due to the need to handle ever increasing amounts of radio frequency interference in the observing bands.

- 2) The high bandwidth sampling ability of short pulses with low jitter allows direct digital down-conversion of high frequency signals eliminating the need for separate mixers and local oscillators.

- 3) Demultiplexing of the sample pulses can be performed in the optical domain allowing successive samples to be sent in parallel to an array of cheaper, low speed ADCs for the quantising step, giving an effective increase in sample rate [104]. One method uses wavelength-interleaved pulses which are then separated by passive filters to perform the demultiplexing. Other methods use fast optical switches to perform time domain demultiplexing [105]. The latest experiments are approaching sample rates of 100 giga-samples/s with resolutions of 4 bits [106].

In the radio astronomy specific application there are a few more properties of optical sampling by short pulses that are potentially very useful: Firstly, short optical pulses can be propagated large distances without distortion using managed soliton transmission schemes [107]. In a large, dispersed phase array of radio telescopes, for example the proposed Square Kilometre Array, sampling pulses could be sent from and returned to a central base station so that the bulk of the signal processing machinery can be housed in a central location, and only the sampling transducers and a minimal amount of hardware located at the antenna elements. Such a system would require active temperature stabilisation and control to compensate for delay changes with temperature and wavelength; Secondly, having the sampling clock and sampled data in optical form reduces the potential for self-generated radio frequency interference enormously.

An example of how the features discussed in the previous paragraphs could be used in a phased array for radio astronomy is shown in figure 6.5 [108].

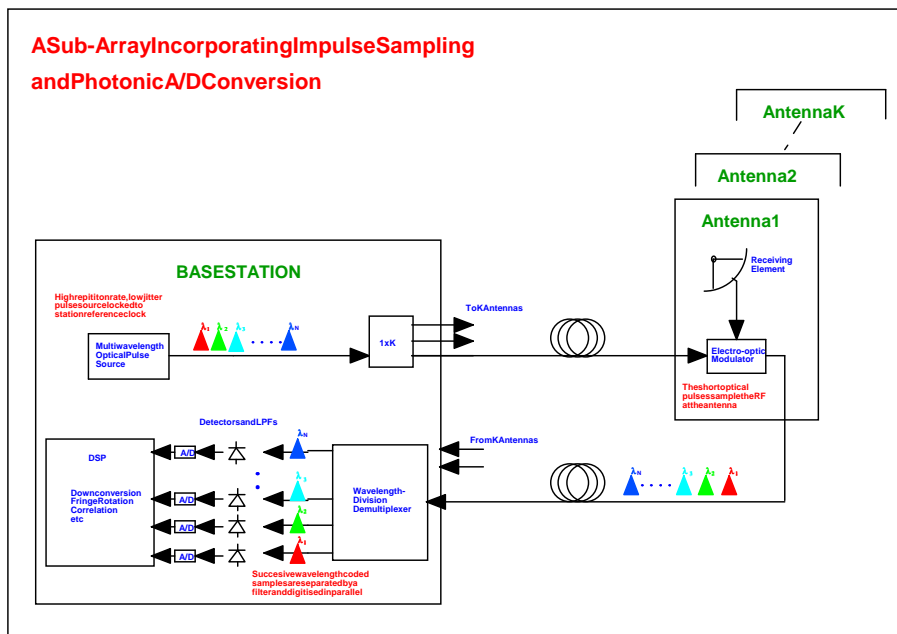


Figure 6.5: Phased array incorporating photonic A/D.

# Chapter 7

## Conclusion

### 7.1 Thesis Summary

This thesis has dealt with the design, development and application of specialised components for wide bandwidth signal processing in the field of radio astronomy. It was shown that wide bandwidths were desirable for the reasons of improved sensitivity and velocity coverage.

Demonstrated in this thesis were a range of high sample rate three-level digitisers ICs including an analysis of their performance limitations and critical design considerations. Specifically, a three-level digitiser with integrated demultiplexer was designed which operated to greater than 10 giga-samples/s and is the fastest digitiser device for radio astronomy reported. This device was packaged and integrated into a complete 4 giga-sample/s digitiser system. Two of these were installed at the Parkes radio observatory and construction of more of these units is planned for deployment in future facilities. Also presented was a photonic I/O digitiser integrated circuit. This device is the first reported digitiser device designed to accept its sampling clock photonically and deliver the digitised data photonically.

A 15 GHz bandwidth analogue multiplier designed for use in analogue correlators was presented. A noise analysis of multipliers in interferometers was given and the noise of back-end components found to be of great impor-

tance in very wide bandwidth systems. The noise performance of the InP HBT multiplier was investigated and contrasted with a SiGe HBT analogue multiplier of 5 GHz bandwidth. The SiGe HBT technology was found to be a good choice for implementing multipliers if substrate loss can be overcome.

In the final chapter a new photonic multiplier architecture was proposed and demonstrated. This multiplier has the ability to perform signal multiplication over much greater bandwidths than purely electronic means. A noise analysis of this multiplier was performed, and several methods proposed to make it more practical in the particularly noise-critical application to radio astronomy interferometers. Lastly, a brief survey of photonic analogue-to-digital conversion was presented and an application of this technology to radio astronomy phased arrays suggested.

## 7.2 Further Work

With the speed of technology development in the semiconductor industry much has happened since the devices in this thesis were designed. InP HBT processes are now available with over twice the speed of the process used to implement these digitisers and so it would be possible to design similar devices with much greater speeds in these newer processes.

There will continue to be a position in radio astronomy for high-speed coarse-quantisation devices like the ones in this work especially in the area of millimetre wavelength astronomy where the widest of bandwidths are needed, and there is currently little man-made interference. At the lower observing frequencies there is a trend towards using higher number of bit digitisers. This is largely in response to the realisation that man-made interference is impossible to avoid at the lower frequencies, so it must be measured and removed using digital signal processing means. This requires faithfully digitising the astronomy signal plus the interfering noise and so requires high precision digitisers. These digitisers are then the same as general ADCs as required for oscilloscopes, military communications and software radio ap-

plications and radio astronomy will hopefully be able to benefit from ADC developments in these areas.

Between these two extremes lies the regime of using a moderate number of bits, for example three or four. The high speed of newer semiconductor technologies could be used to realise digitisers with similar sample rates to those in this thesis, but using the extra transistor speed to allow higher number of bits operation. This has the advantage of having higher sensitivity. A 3-bit system has an efficiency of about 0.96 compared to 0.81 for the three-level devices in this work. Such a system is also more interference tolerant. The group in [26] are developing just such a device for the digitisers for the ALMA project.

In the area of multipliers, SiGe appears to have decisive advantages over III-V semiconductors in the area of low frequency noise. Being aware of the need to minimise substrate losses, and with the newer high-speed SiGe processes available, low noise multipliers of the order of 10-15 GHz of bandwidth should be practical and is the logical next step for pursuing wider bandwidths in analogue correlators.

The compelling advantages of photonic A/D conversion also make this technology well worth investigating. What needs to be done is a system demonstration in a setting typical to radio astronomy to see if system aspects limit the usefulness of this technique in practice. Experiments in this direction are planned for the near future.

End





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# Appendix A

## Hardware Reference

This appendix contains schematics for the circuit boards designed as part of this work and referenced in the thesis. Only the hardware schematics are included. Schematics for the FPGA programmable logic devices and assembly language code for the DSP controller are not included as they are too voluminous. They can be obtained from the author if required.

## A.1 Chip carrier

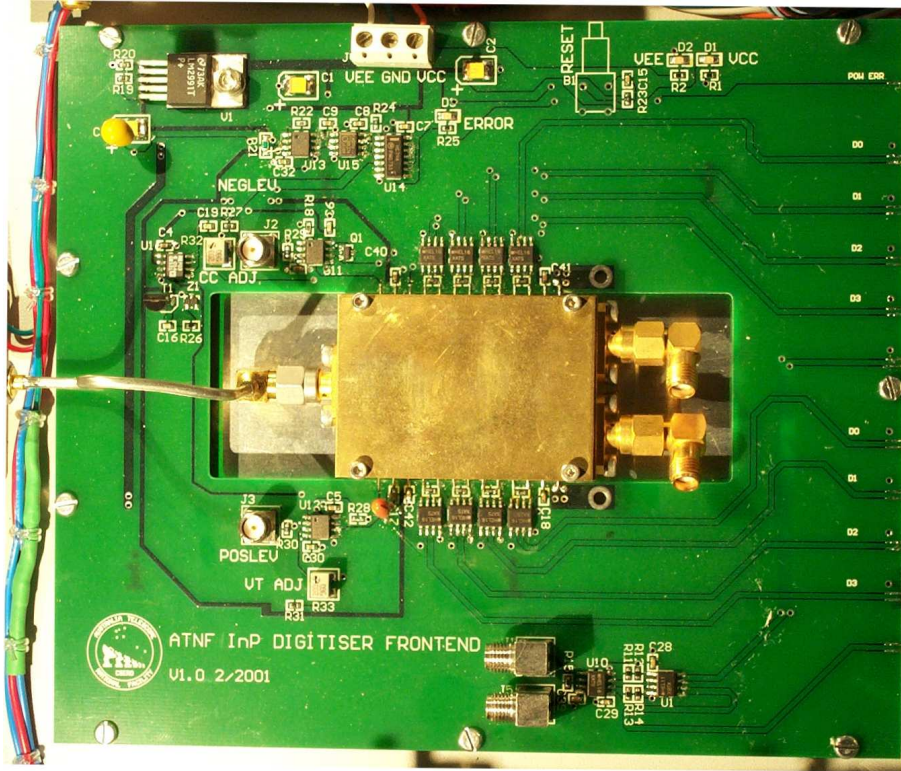


Figure A.1: Chip carrier with IC installed.

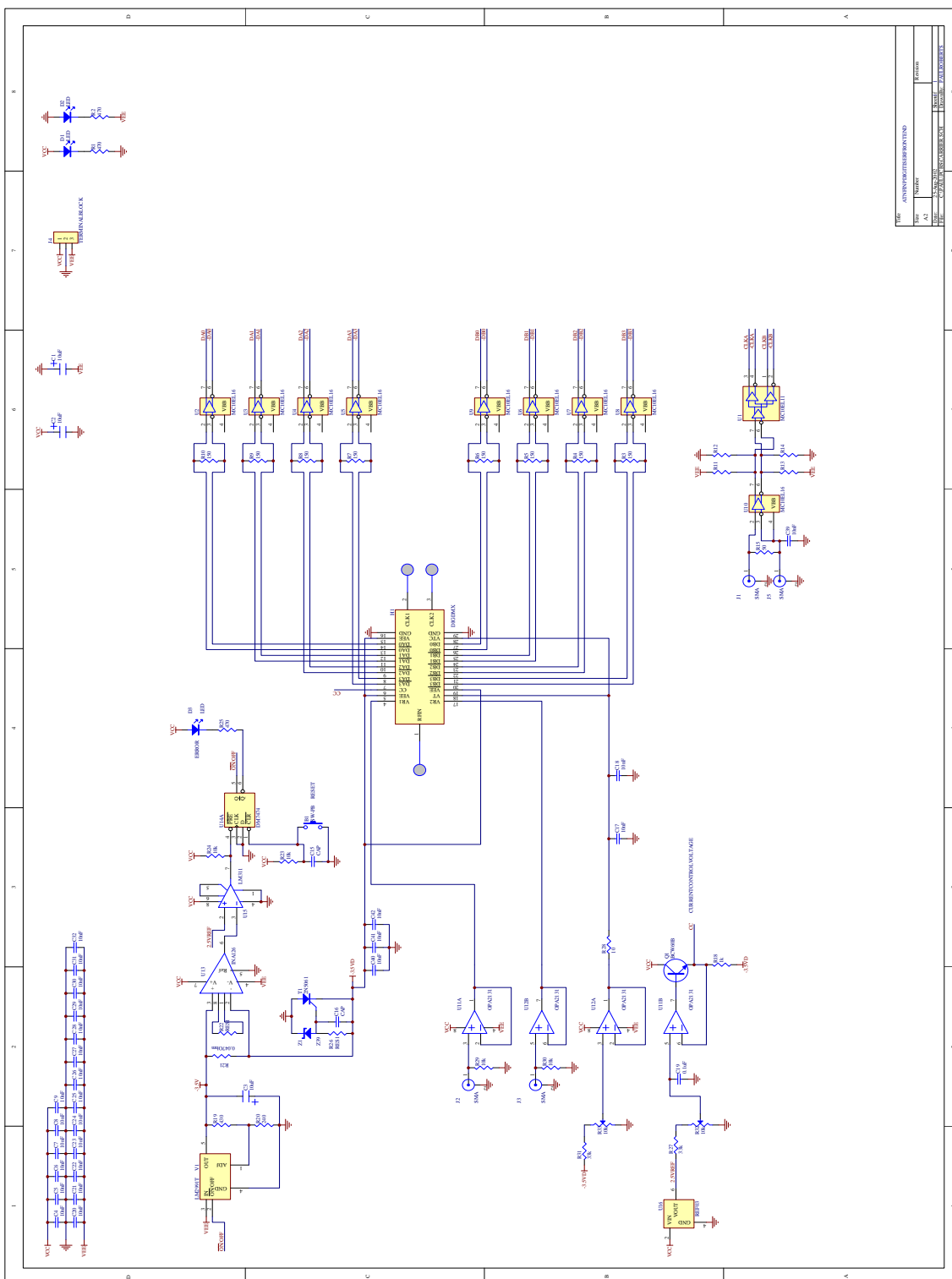


Figure A.2: Chip carrier schematic.

## A.2 Demultiplexer/Statistics Counter

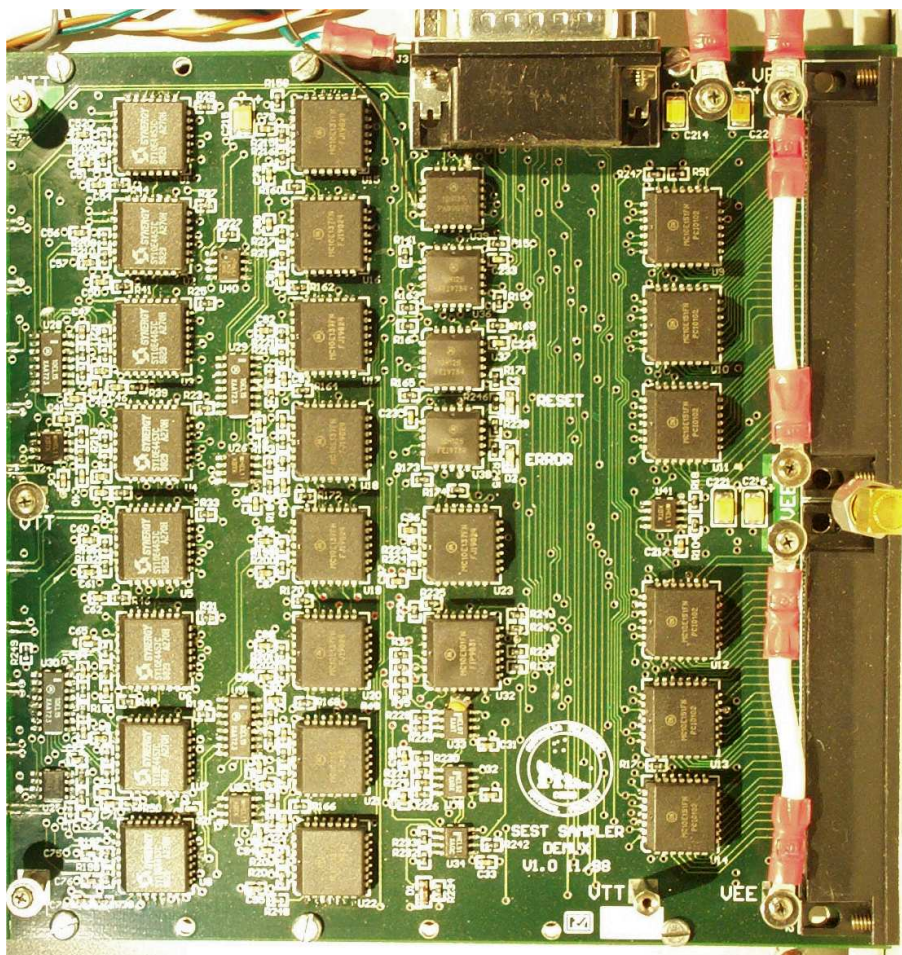


Figure A.3: Demultiplexer/Statistics counter.



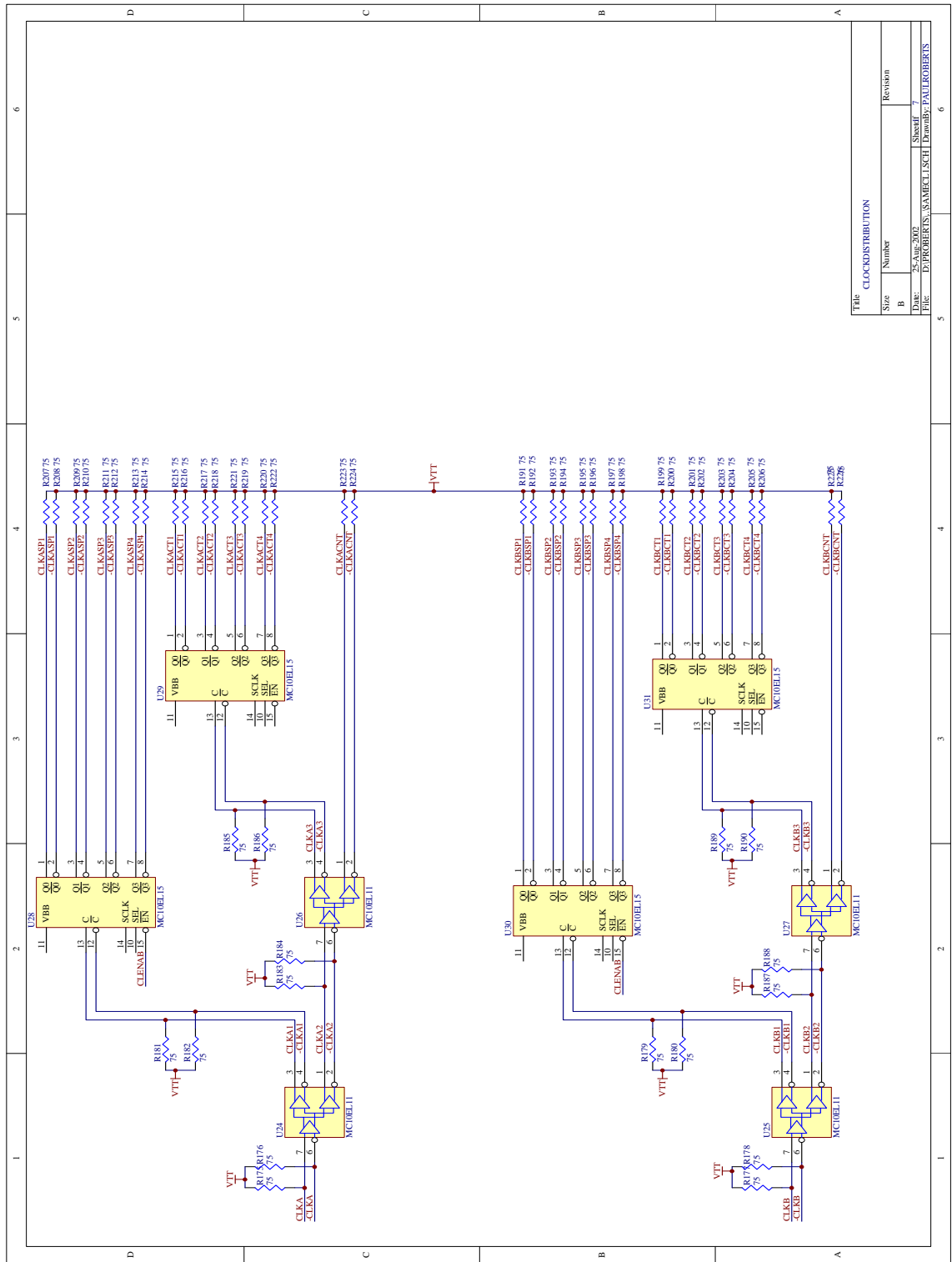


Figure A.4: Demultiplexer/Statistics counter schematic - page 1.

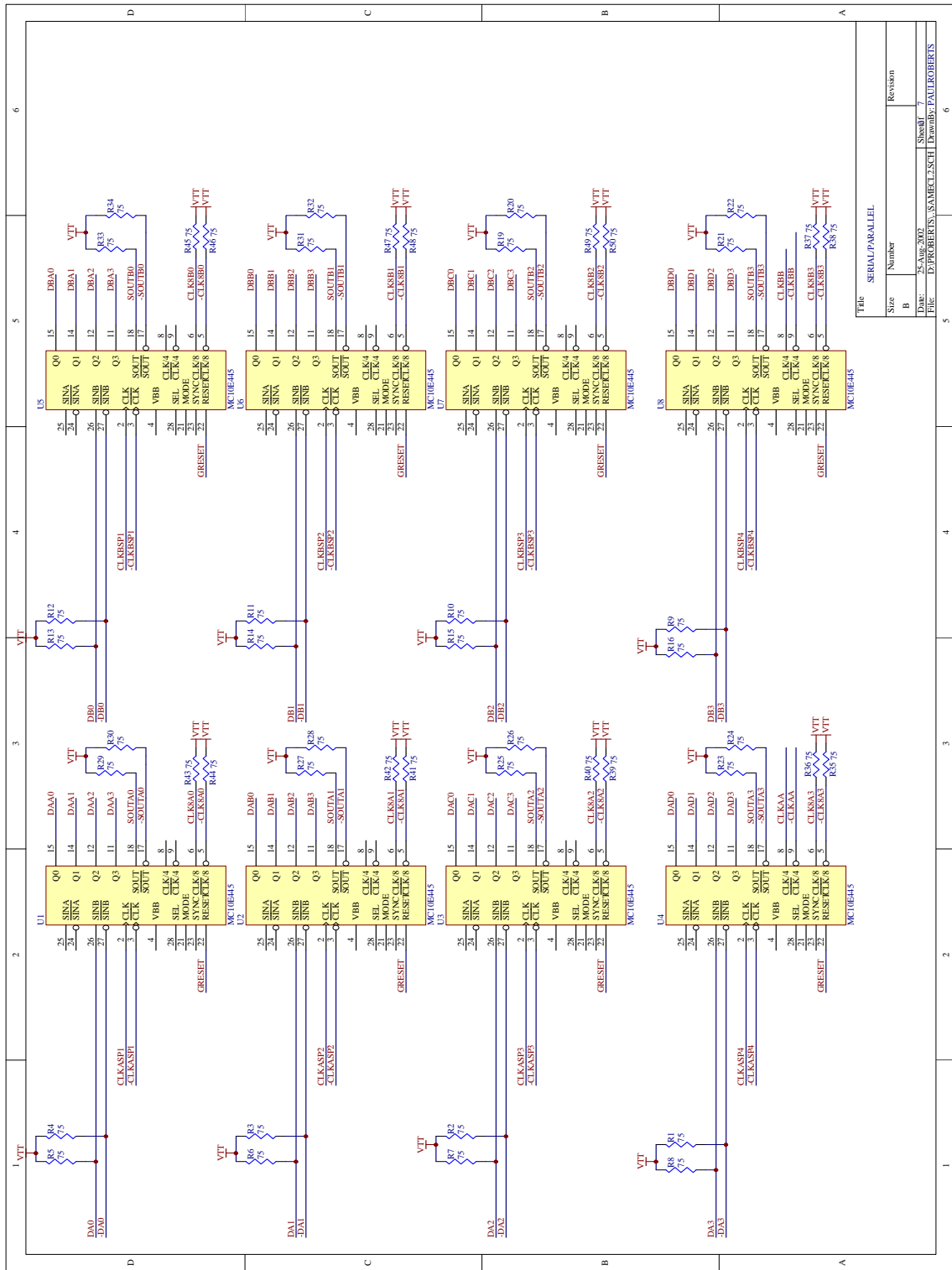


Figure A.5: Demultiplexer/Statistics counter schematic - page 2.

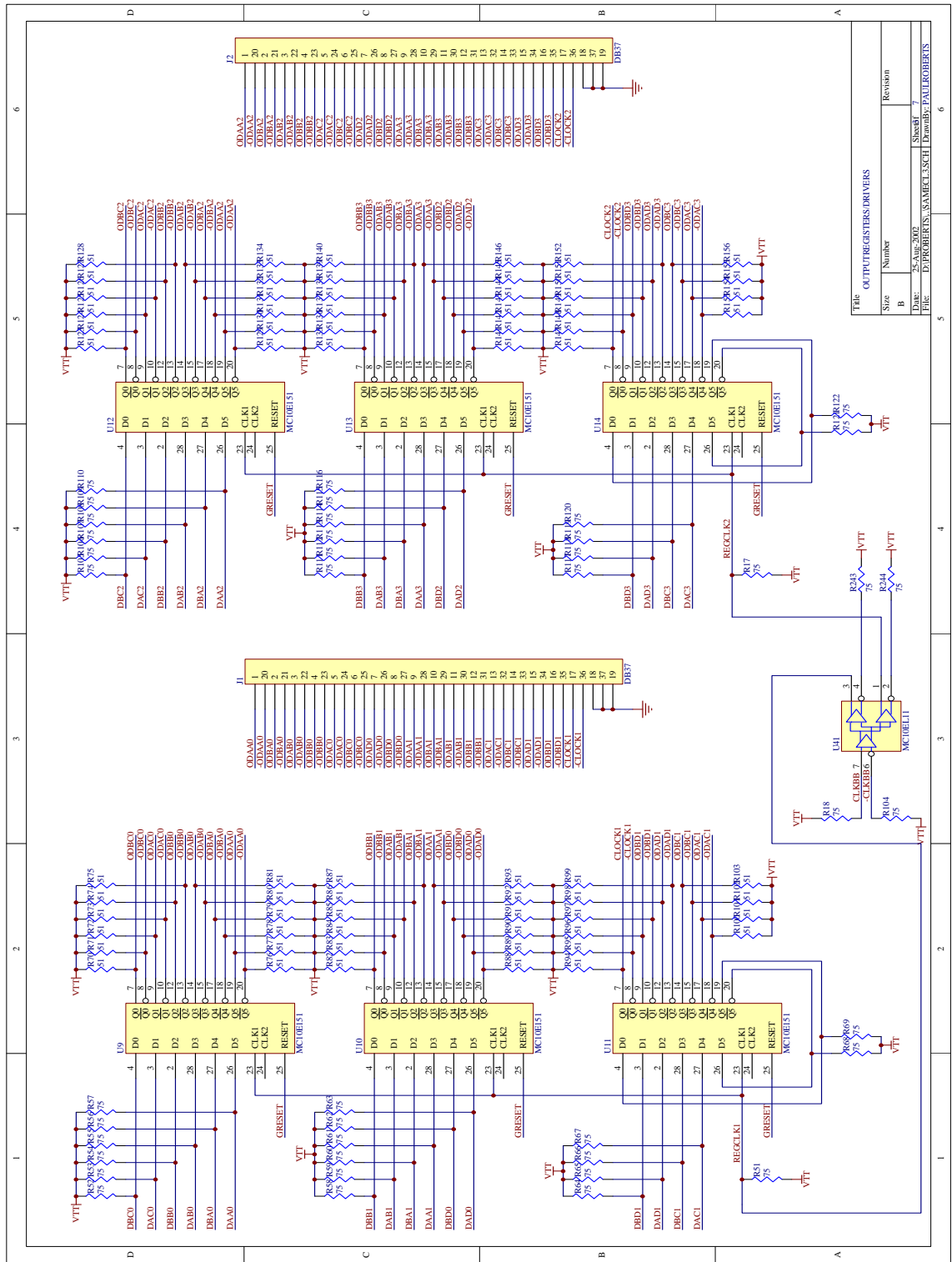
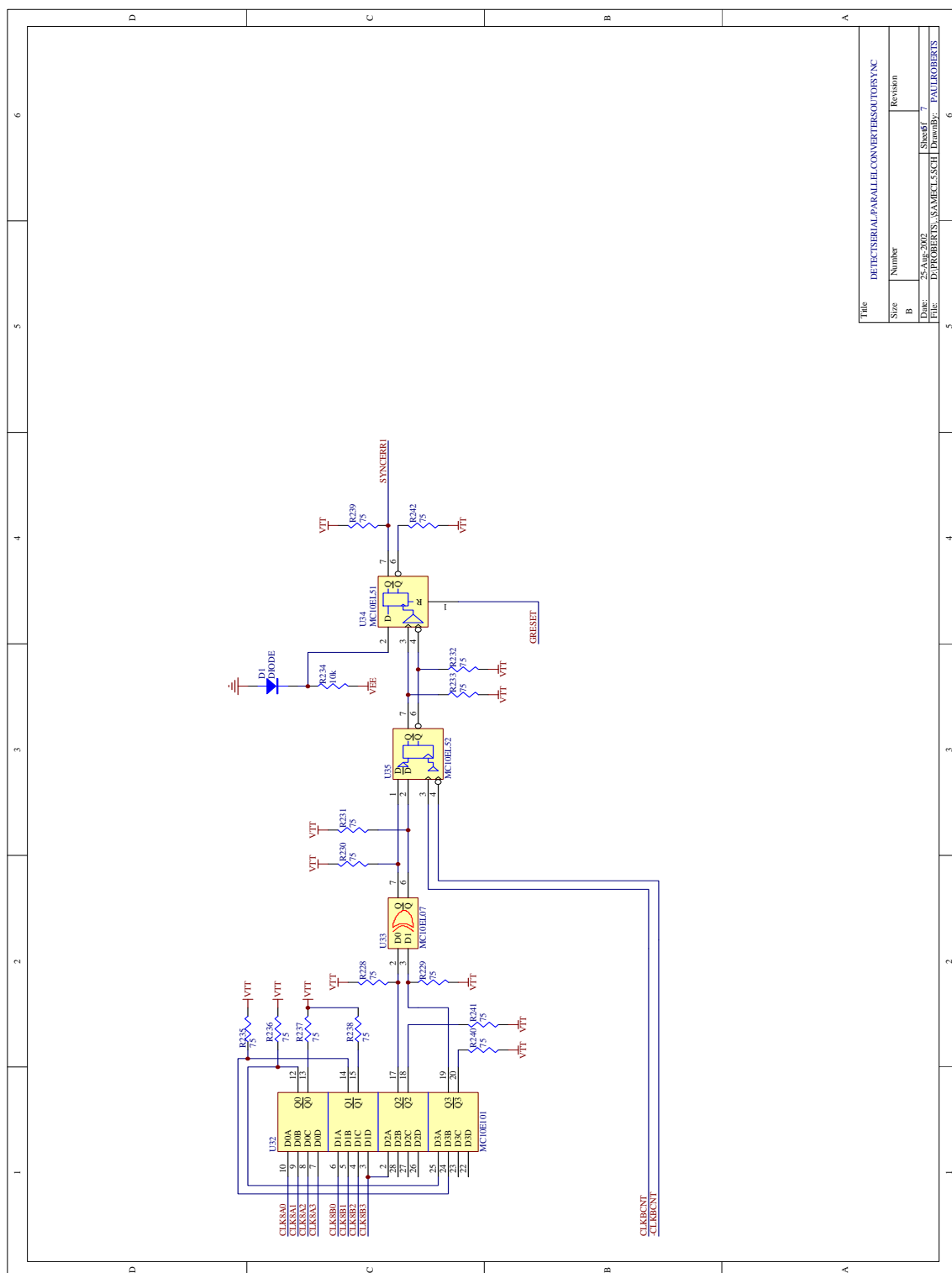


Figure A.6: Demultiplexer/Statistics counter schematic - page 3.



Figure A.7: Demultiplexer/Statistics counter schematic - page 4.



Title		DETECTSERIAL/PARALLEL CONVERTERS/OUT8SYN	
Size	Number	Revision	
B			
Date:	25-Aug-2002	Sheet#	7
File:	D:\PROJETS\SAMKLE\SCH	DrawnBy:	PAULLROBERTS

Figure A.8: Demultiplexer/Statistics counter schematic - page 5.

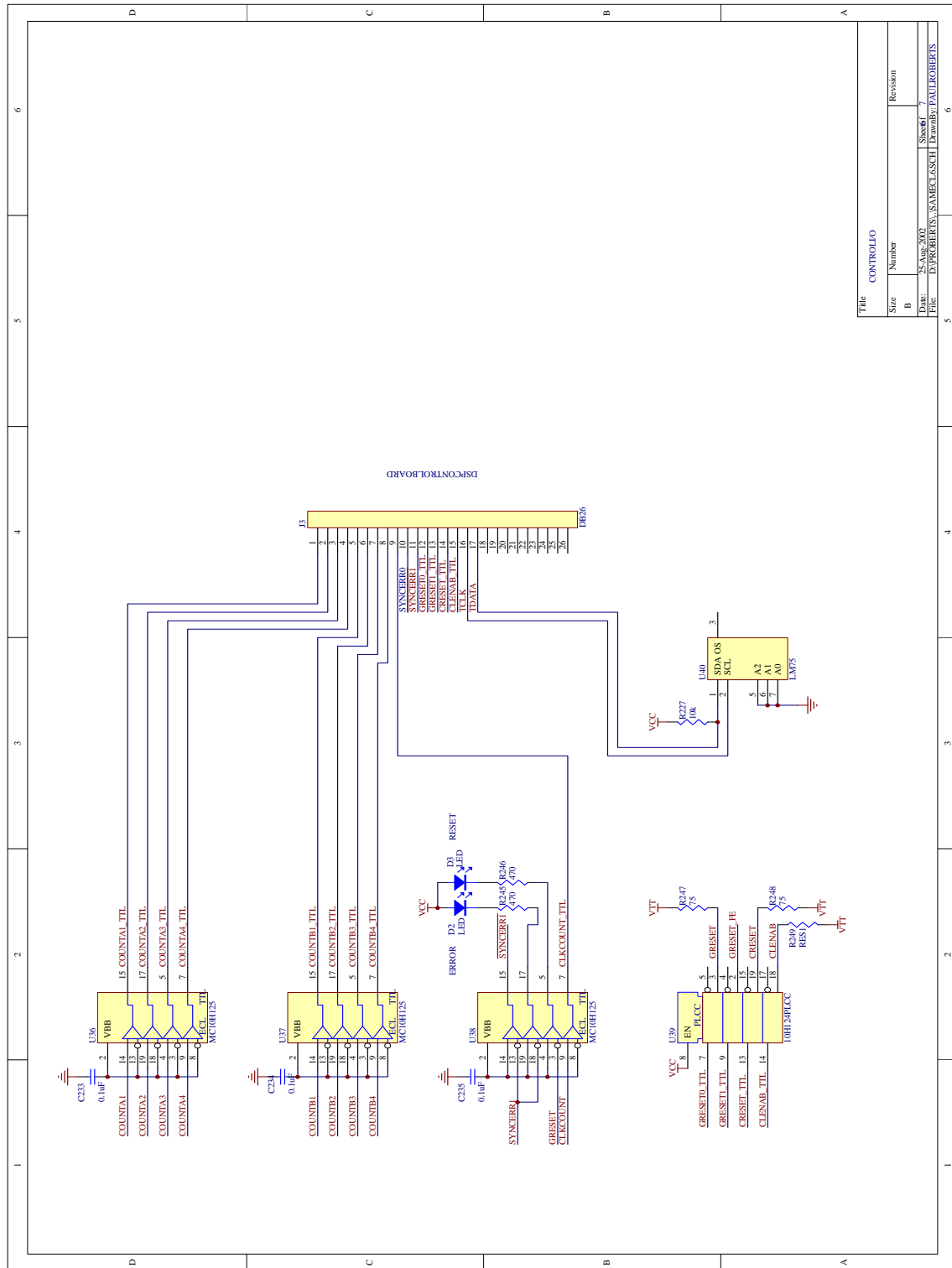


Figure A.9: Demultiplexer/Statistics counter schematic - page 6.

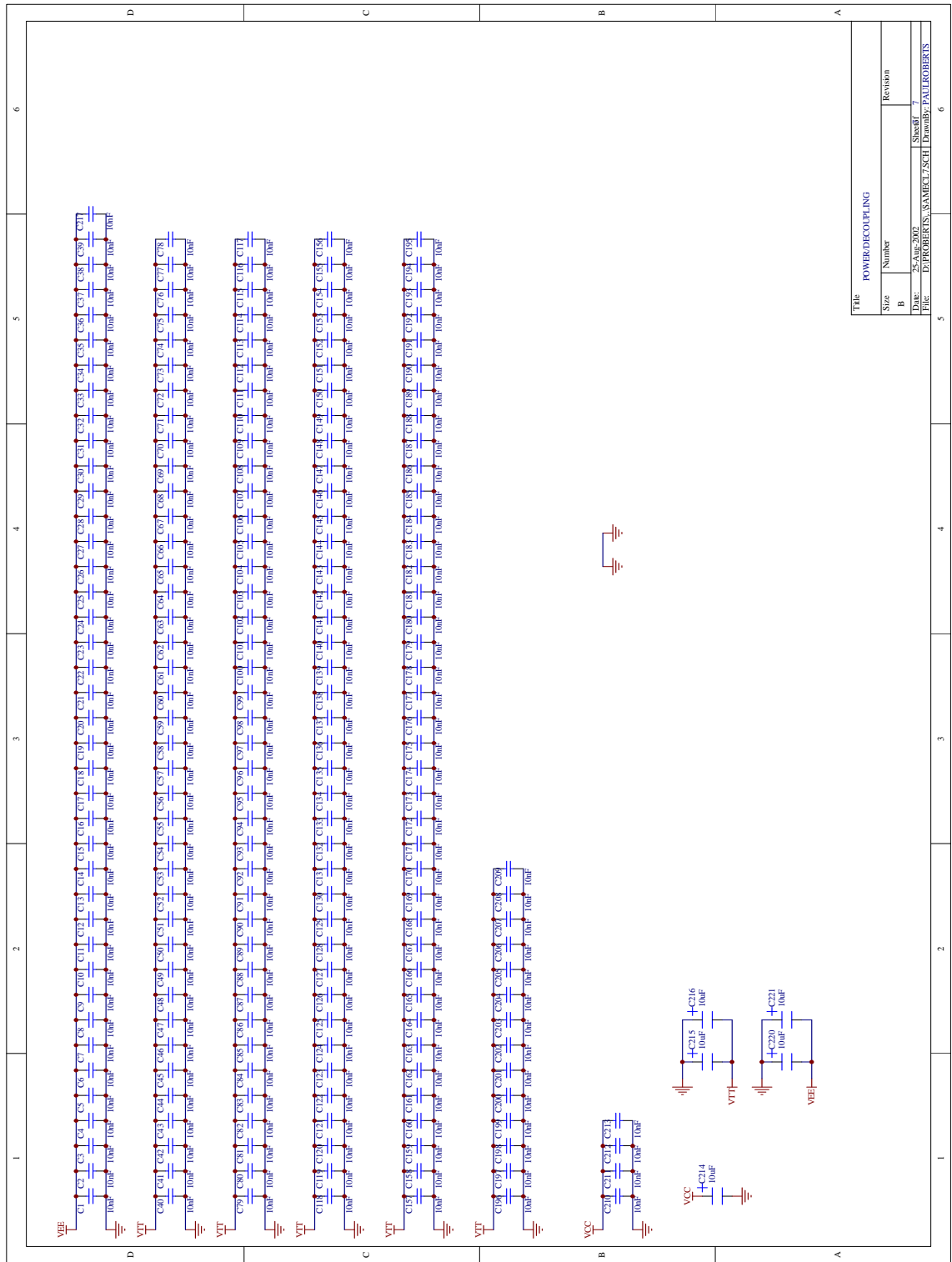


Figure A.10: Demultiplexer/Statistics counter schematic - page 7.

## A.3 Controller

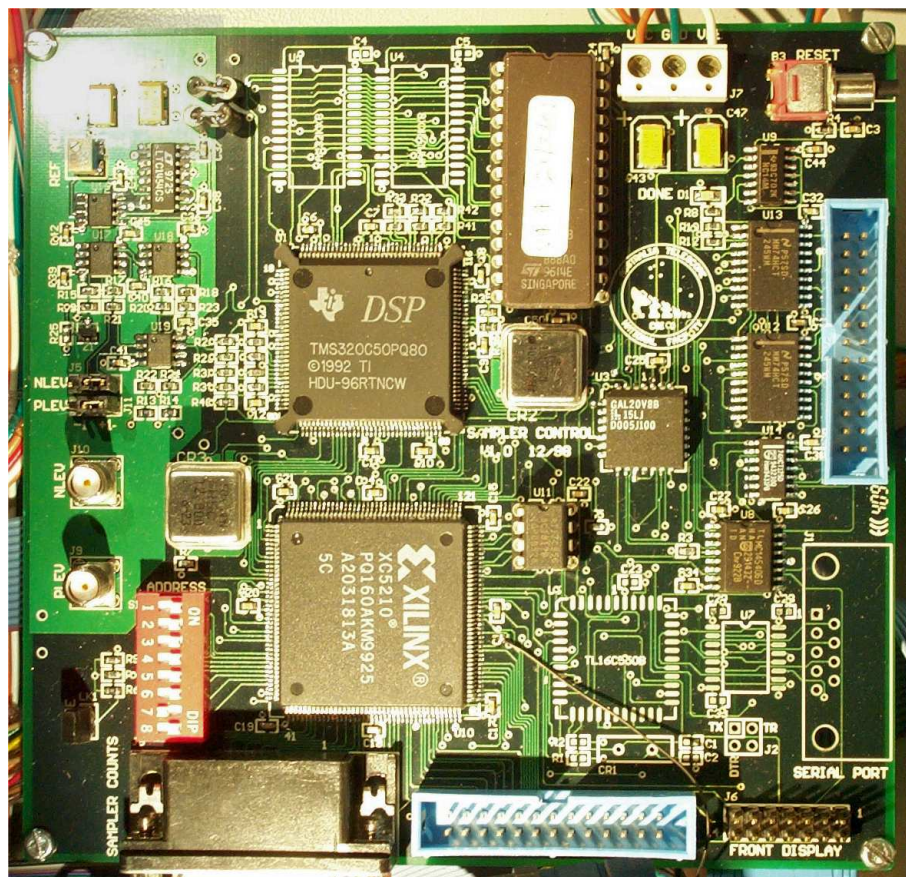


Figure A.11: DSP based controller.



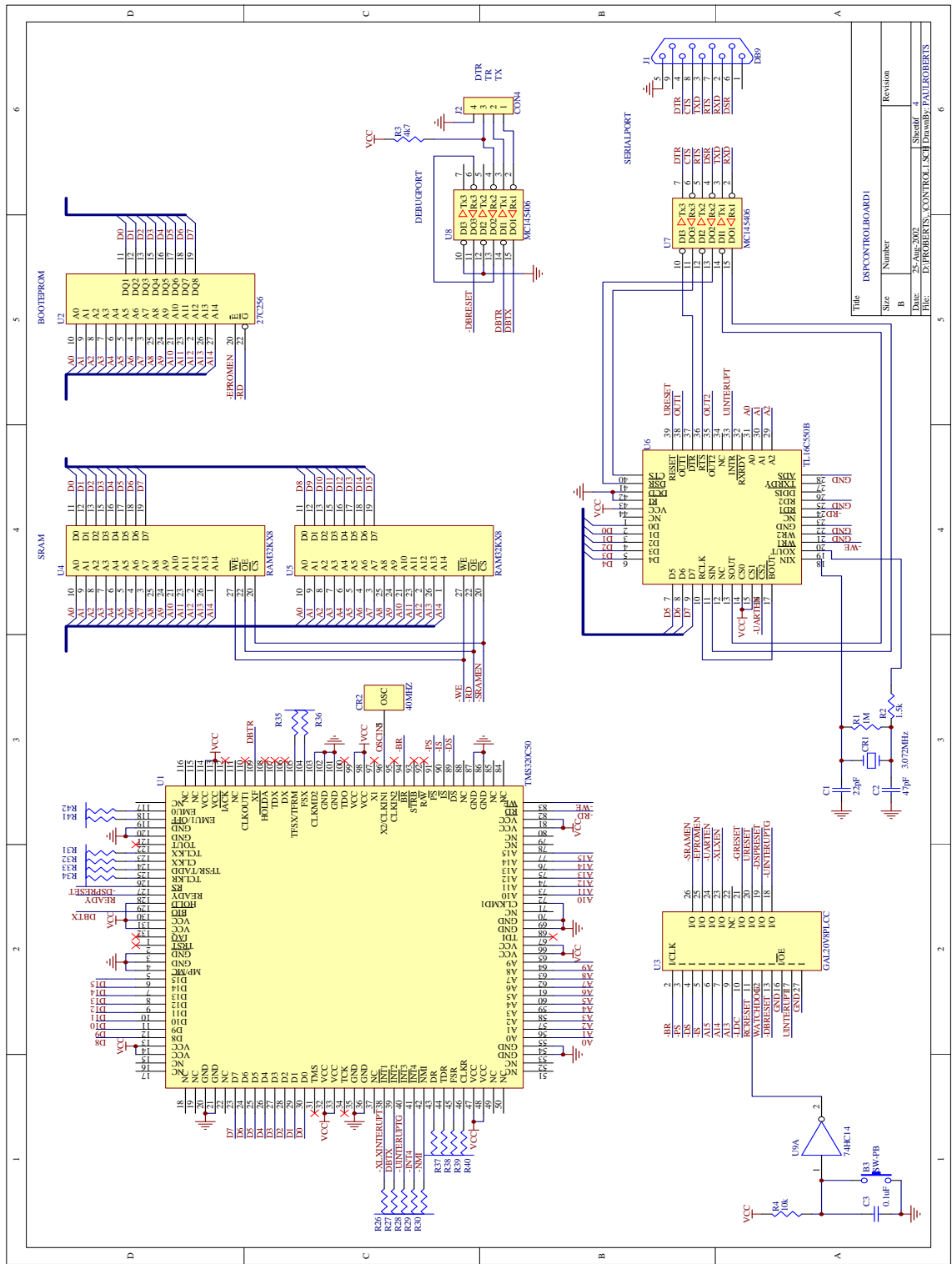


Figure A.12: Controller schematic - page 1.

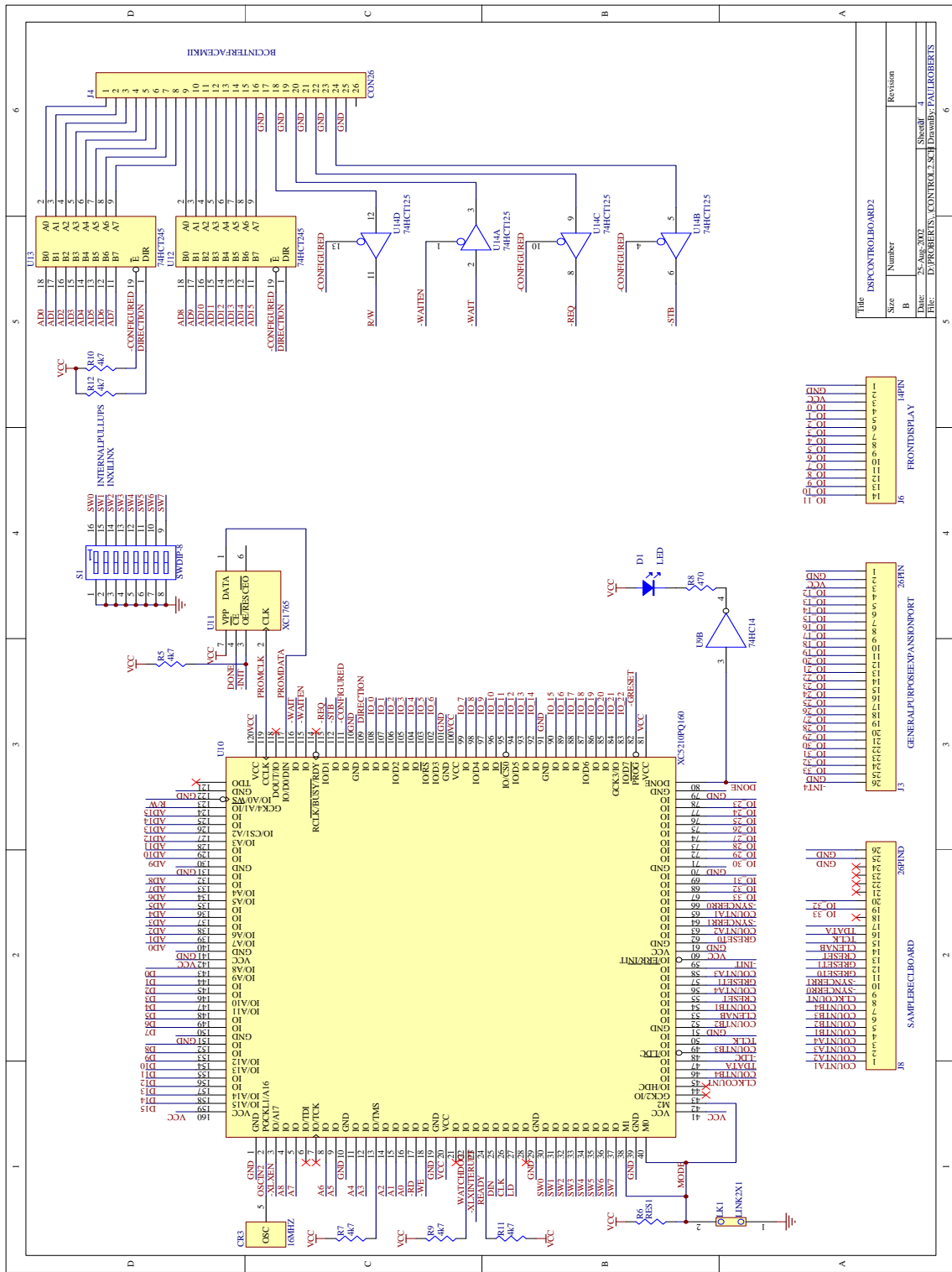
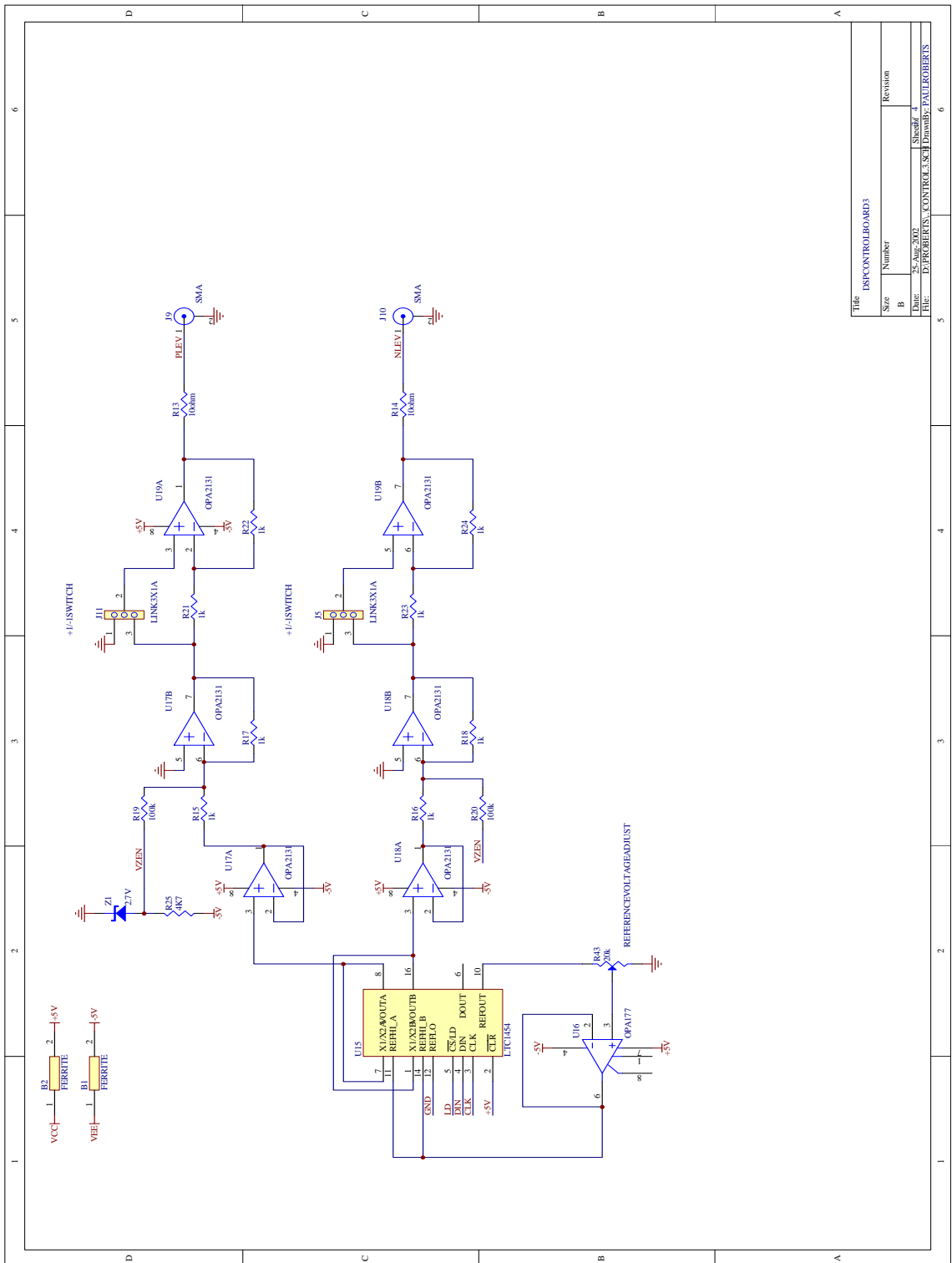


Figure A.13: Controller schematic - page 2.



Title		ESP CONTROL BOARD3	
Size	Number	Revision	
B			
Date	25-Aug-2002	Sheet of	4
File	D:\PROJETS\CONTROL3.SCH	Drawn by	PAUL ROBERTS

Figure A.14: Controller schematic - page 3.

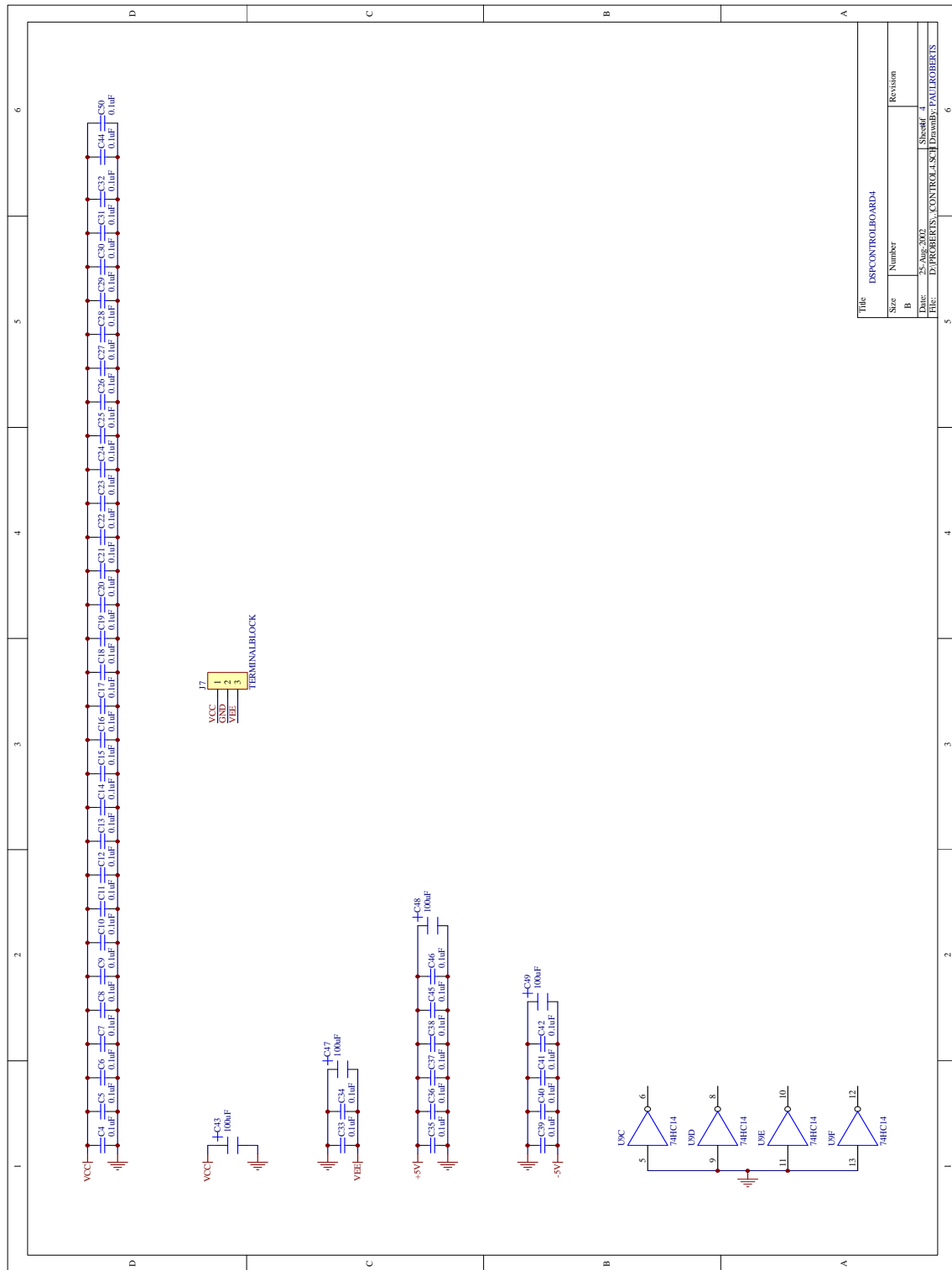


Figure A.15: Controller schematic - page 4.

## A.4 Synthesiser

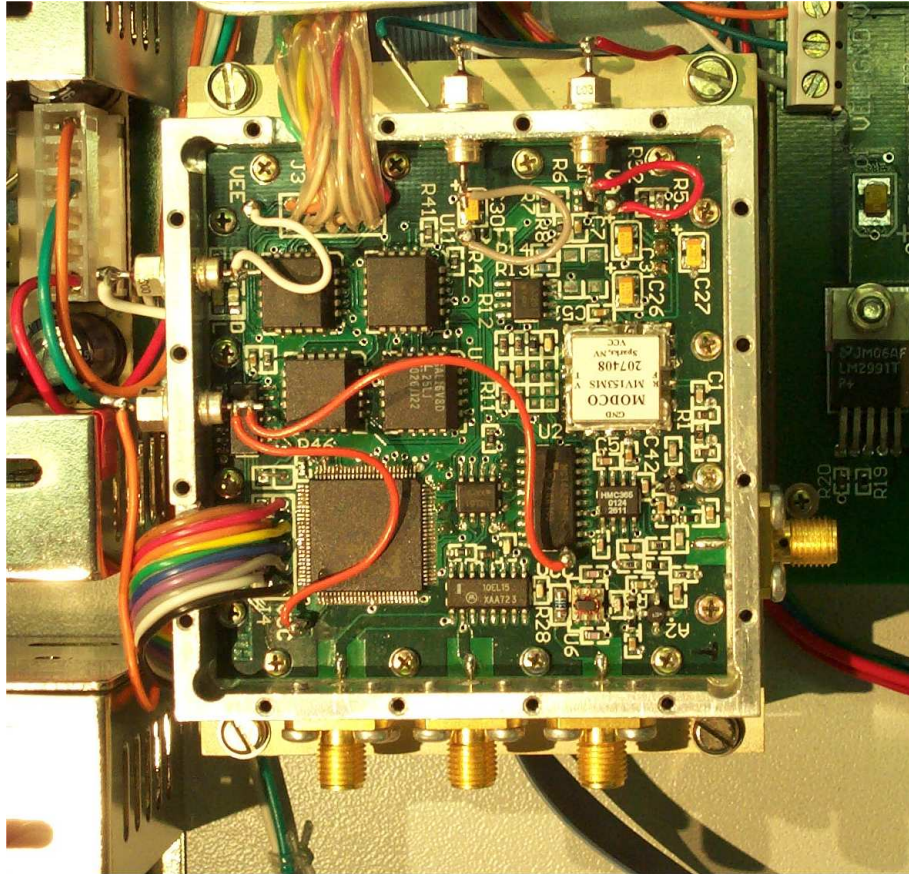


Figure A.16: Synthesiser.

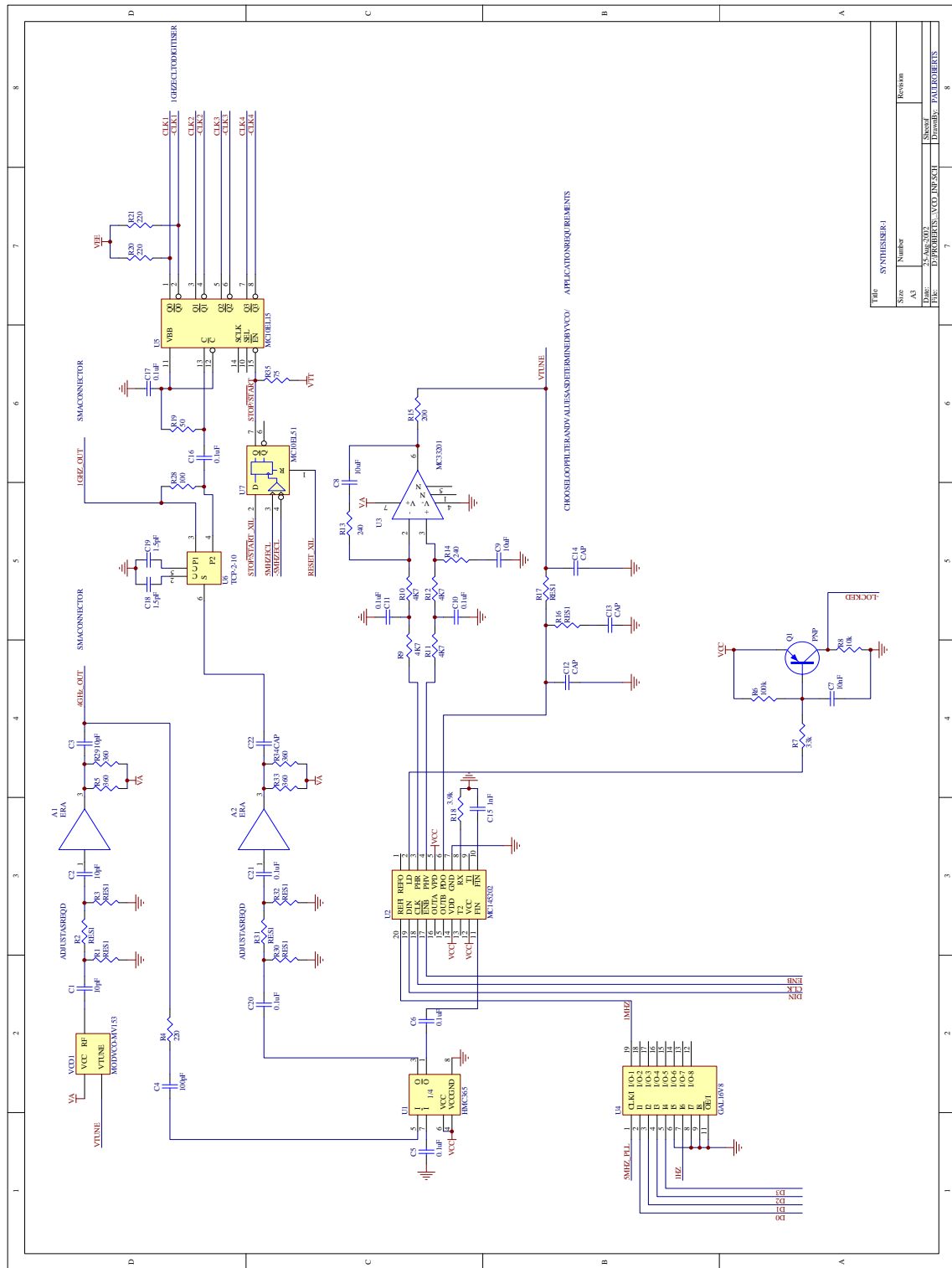


Figure A.17: Synthesiser schematic - page 1.

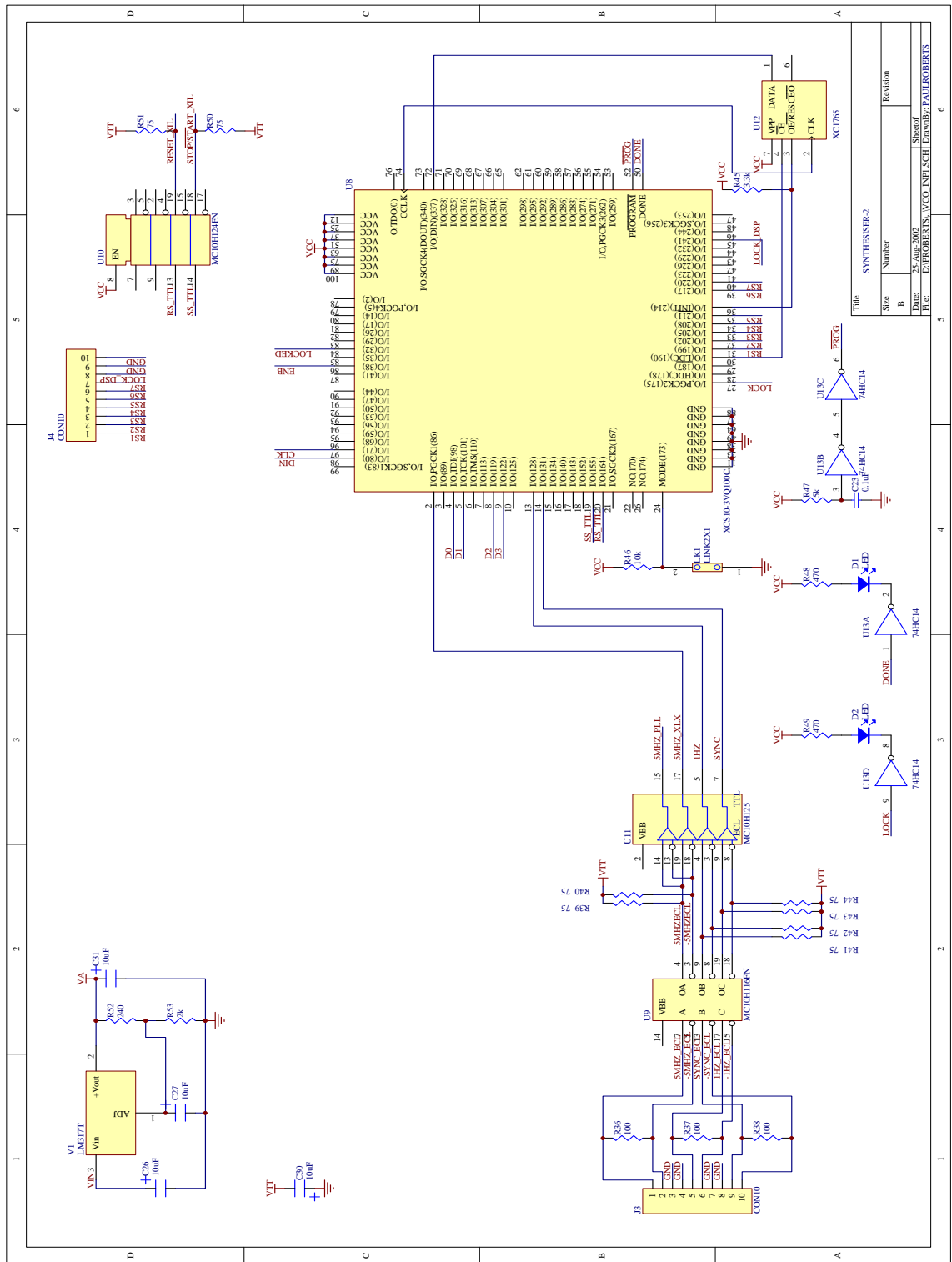


Figure A.18: Synthesiser schematic - page 2.

## A.5 Photonic multiplier

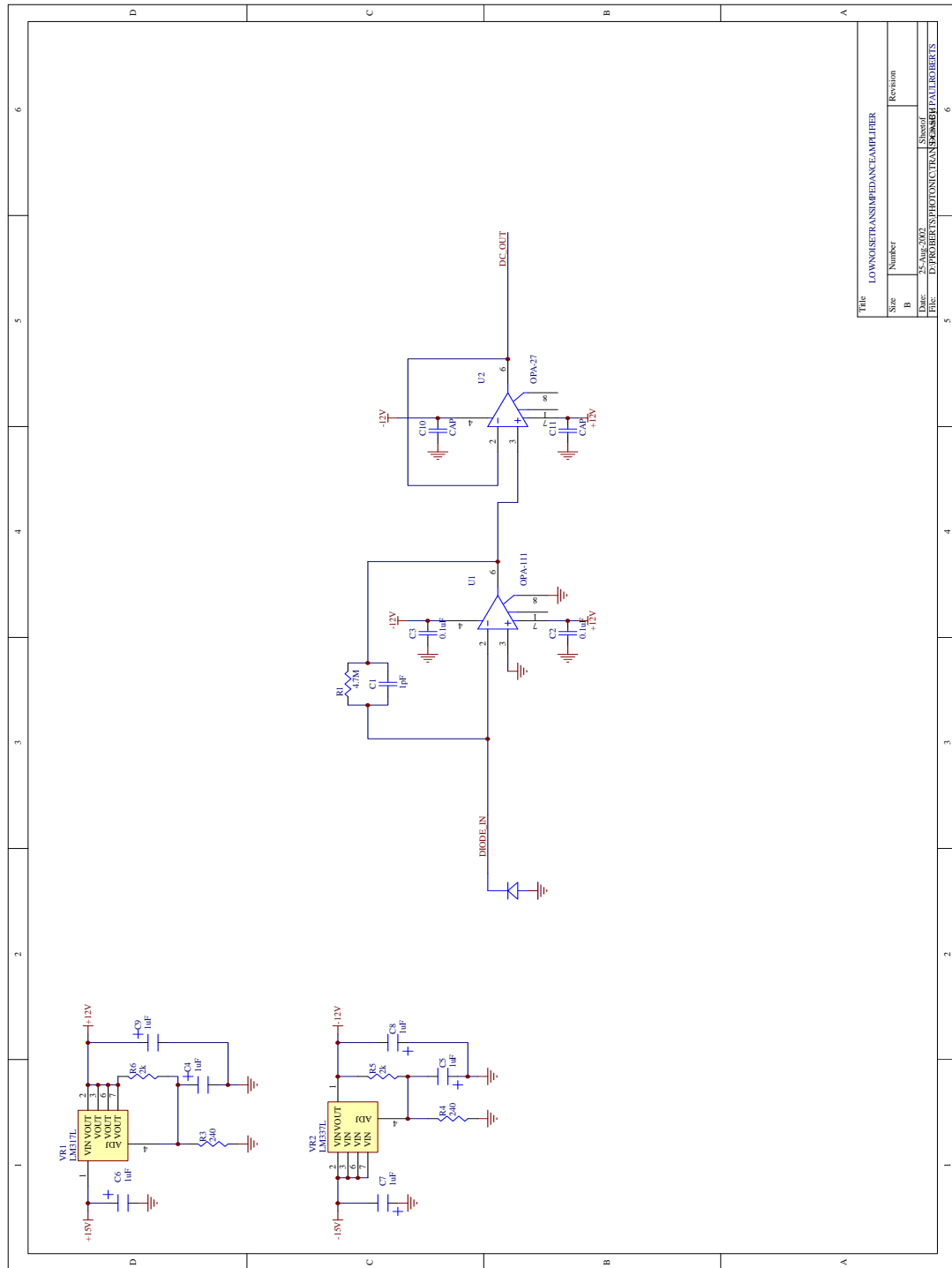


Figure A.19: Transimpedance amplifier



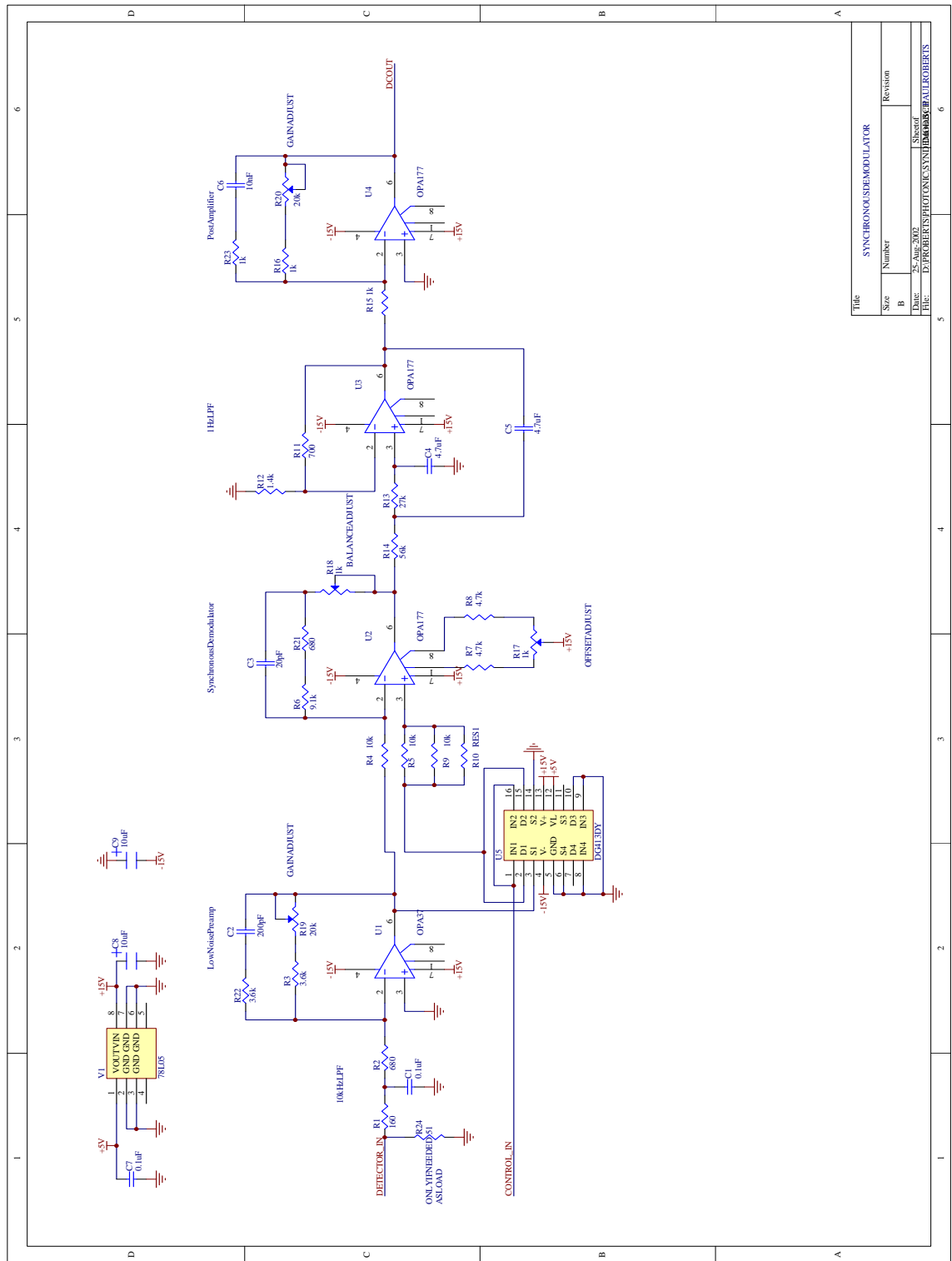


Figure A.20: Synchronous demodulator