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Performance Analysis of Junctionless Transistors Based on Monte Carlo Simulation

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Abstract—A junctionless (JL) transistor has no pn junctions and has a number of advantages to fabricate ultrashort-channel metal-oxide-semiconductor field-effect transistors. In this paper, we study the electron transport in JL transistors based on a Monte Carlo simulation. We demonstrate that high channel doping will not degrade the drive current seriously, because ionized impurities scatter electrons mostly forward, and thus there is less chance for scattered electrons to return back to the source. We also find that smaller parasitic resistance in the source of a JL transistor also contributes to achieve high drive current.

Recently, a junctionless (JL) transistor with no pn junctions has been proposed [1,2]. In this device, doping type and concentration in the channel are identical to those in the source and drain, and hence, there are no junctions and no doping concentration gradients between source and channel or drain and channel, which requires no costly ultrafast annealing techniques and thus allows us to fabricate ultrashort-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) [1]. Furthermore, JL transistors have a number of advantages, such as less sensitivity to the channel-gate oxide interface, carrier transport with bulk mobility, which is typically higher than the inversion layer mobility [3], and better speed performance. On the other hand, impurity scattering in the channel may decrease the carrier mobility [4] and degrade the device performance.

The key technique to obtaining a properly working JL transistor is the formation of an ultrathin or ultranarrow channel with a proper gate work function so that the channel region can be fully depleted when the device is turned off. Meanwhile, the channel needs to be heavily doped to obtain a sufficiently large drive current at ON-state. Therefore, the use of an ultrathin body or nanowire channels combined with multigate electrodes and high channel doping concentration is indispensable [1,2]. In this paper, to understand the roles of the miniaturization of the channel cross section and impurity scattering in the channel, we performed electron transport simulation of JL transistors with different channel dimensions, based on a Monte Carlo (MC) approach.

Since a multigate structure is indispensable to JL transistors, we employed here an ultrathin-body double-gate (DG) MOSFET shown in Fig. 1. Although a three-dimensional (3D) tri-gate or gate-all-around configuration is preferable, the present DG configuration with an ultimately scaled gate oxide as $T_{ox} = 0.5$ nm has a good electrostatic controllability over the channel, and also can avoid a huge computational time and numerical instability both inherent to 3D MC simulation. To compare with the performances of conventional DG devices, the doping concentration in the source and drain is taken to be highly sufficient, $N_D = 1 \times 10^{20}$ cm^{-3}. For simulations of JL transistors, the doping concentration in the channel N_{ch} is set at the same value as the above N_D, while it is assumed to be zero, that is, the channel is intrinsic, for the conventional devices. A p$^+$ (n$^+$) polysilicon gate is used for JL (conventional) transistors [1], where we considered n-channel MOSFETs. The channel thicknesses T_{Si}'s are given as 10 and 5 nm, and the channel length L_{ch} is provided by following an empirical rule of $L_{ch} = 4 \times T_{Si}$, which is often used as a guideline to suppress short-channel effects [5]. The electrical characteristics were computed by using a MC device simulation [6,7,8]. Any quantum effects were disregarded here, since rather large channel dimensions are used in this study. We considered

phonon and impurity scatterings [7,8], while roughness scattering was ignored to directly examine the effects of the gate electrostatic controllability in JL transistors.

First, we present the drain current versus gate voltage (I_D - V_G) characteristics computed for both the JL and conventional MOS transistors in Fig. 2, where (a) and (b) correspond to T_{Si} = 10 and 5 nm, respectively. The drain voltage V_D is set at 0.5 V. The right panels indicate the logarithmic plot of the drain current. Here, the drain current properties below ~ 10^{-2} mA/μm are unreliable in the present MC technique because of the small number of particles travelling across the channel, and we did not include those data in Fig. 2. First of all, the conventional DG devices are confirmed to work well for both T_{Si}'s. On the other hand, the JL transistor with T_{Si} = 10 nm indicates a lack of switching behavior, which means that it is a simple n^+ - n^+ - n^+ resistor. However, as the channel thickness decreases to 5 nm, it exhibits a well-behaved transistor operation owing to the enhanced gate electrostatics as shown in Fig. 2(b). The successful switching operation by using the ultrathin-body DG structure has been also demonstrated based on a simple analytical current model and a device simulation [9]. Incidentally, from Fig. 2(b), current slopes at the minimum gate voltage are evaluated to be about 75 and 114 mV/dec for the conventional and JL transistors, respectively. These results reconfirm that the channel thickness is required to be smaller than the depletion layer width (about 4 nm × 2 in the present DG device) to make JL transistors work properly [1,2].

Next, we compare the drain current versus gate overdrive (V_G - V_{th}) characteristics between the two devices as shown in Fig. 3, where T_{Si} = 5 nm and the threshold voltage V_{th} was defined as a gate voltage corresponding to I_D = 0.03 mA/μm. The right panel again indicates the logarithmic plot of the drain current. It is found that the JL transistor exhibits a large ON-current and good turn-on characteristics, quite comparable to those of the conventional MOS transistor. The result is consistent with the experimental measurement reported in ref. 1. This is a good news for JL transistors, because it suggests that high channel doping does not degrade the drive current seriously. We have checked the number of scattering events that actually happened in the devices by making use of the MC algorithm, and found that the impurity scattering events have happened approximately twice as many as the phonon scattering within the channel. Nevertheless, the JL transistor still retains almost the same ON-current as the conventional transistor, as shown in Fig. 3. One of the reasons is that the Coulomb interaction with ionized atoms scatters electrons mostly forward [7,8,10,11], and thus, electrons are less likely to be returned to the source even if they are scattered by impurities within the channel. To demonstrate the impact of this forward scattering, we intentionally programmed the impurity scattering that happened in the channel to scatter electrons equally

forward and backward (i.e., isotropically), and the results are indicated by the dashed-dotted line in Fig. 3. As expected, the drain current obviously decreases by assuming the isotropic impurity scattering. This means that the actual anisotropic scattering mechanism due to ionized donors, which induces mostly forward scattering, prevents scattered electrons from returning back to the source, and hence, the doping in the channel is not detrimental to the ON-current property. Here, we should point out that as for the impurity scattering, high-energy electrons accelerated by a large drain bias such as $V_D = 0.5$ V are more likely to be scattered forward than low-energy electrons. Therefore, the impurity scattering has a smaller negative influence on the drain current as compared to the mobility degradation observed in a low electric field regime.

Another reason is that source parasitic resistance is smaller in the JL MOS transistor as shown in Fig. 4(a), where the result for the isotropic impurity scattering model is also plotted. As a result, the channel electric field becomes larger in the JL MOS transistor and electrons are more effectively accelerated. Both the anisotropic nature of the impurity scattering and the larger channel electric field contribute to the realization of the averaged electron velocity comparable to that of the conventional MOS transistor as shown in Fig. 4(b). Note that the pronounced source parasitic resistance observed in the conventional MOS transistor is due to the extremely thin gate oxide as $T_{ox} = 0.5$ nm. Finally, we can confirm that the magnitude relation of the drain currents is primarily determined by the electron velocity, because the channel electron densities are nearly identical among the three results as shown in Fig. 4(c).

In conclusion, we have demonstrated that the high channel doping does not degrade the drive current of a JL transistor seriously, because ionized impurities scatter electrons mostly forward, and the source electrode of a JL transistor has a smaller parasitic resistance. A roughness scattering at the channel interfaces and a spatially dependent deformation potential for acoustic phonon scattering [12] will be needed for further accurate performance projection of JL transistors.

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Fig. 1. Ultrathin-body double-gate MOSFET used in the simulation. The doping concentration in the source and drain is taken to be $N_D = 1 \times 10^{20}\,\text{cm}^{-3}$. For simulations of JL transistors, the doping concentration in the channel N_{ch} is set at the same value as the above N_D, while it is assumed to be zero, that is, the channel is intrinsic, for the conventional devices. A p^+ (n^+) polysilicon gate is used for JL (conventional) transistors. The channel thicknesses T_{Si}'s are given as 10 and 5 nm, and the channel length L_{ch} is provided by following an empirical rule of $L_{ch} = 4 \times T_{Si}$, which is often used as a guideline to suppress short-channel effects.

Fig. 2. I_D - V_G characteristics computed for both JL and conventional MOS transistors, where (a) and (b) correspond to $T_{Si} = 10$ and 5 nm, respectively. The drain voltage is set at 0.5 V. The right panels indicate the logarithmic plot of the drain current.

Fig. 3. Drain current versus gate overdrive (V_G - V_{th}) characteristics between JL and conventional transistors, where $T_{Si} = 5$ nm and the threshold voltage V_{th} was defined as a gate voltage corresponding to $I_D = 0.03$ mA/μm. The dashed-dotted line represents the result calculated by assuming isotropic impurity scattering where electrons are scattered equally forward and backward due to ionized donors.

Fig. 4. (a) Potential energy, (b) averaged electron velocity and (c) sheet electron density profiles computed at V_G - $V_{th} = 0.4$ V and $V_D = 0.5$ V. The channel region extends from y = 30 to 50 nm. $T_{Si} = 5$ nm.
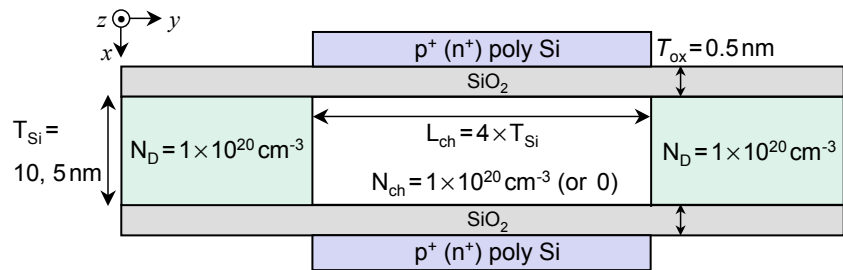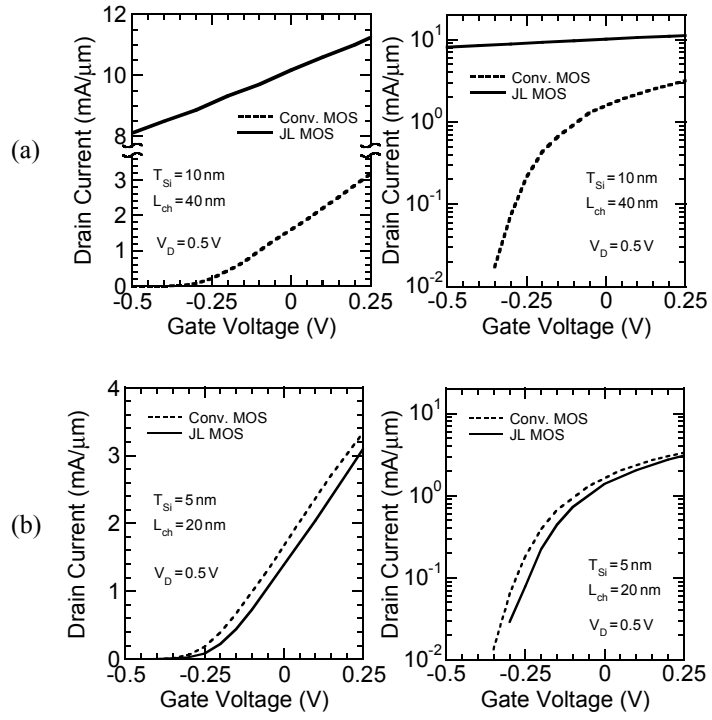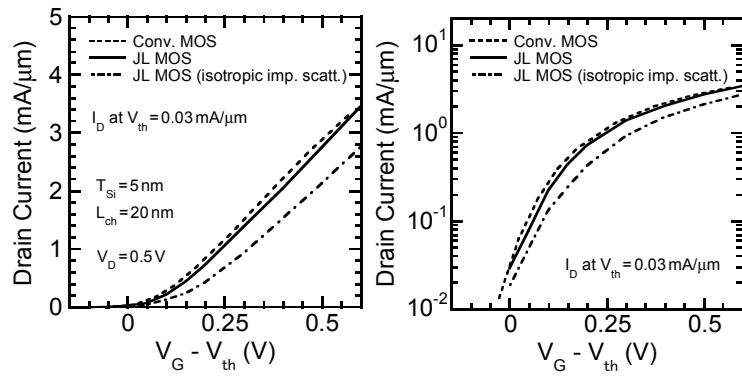
FIGURE 1

FIGURE 2

FIGURE 3

FIGURE 4