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5GHz CMOS All-Pass Filter-Based True Time Delay Cell

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Abstract: Analog CMOS time-delay cells realized by passive components, e.g., lumped LC delay lines, are inefficient in terms of area for multi-GHz frequencies. All-pass filters considered as active circuits can, therefore, be the best candidates to approximate time delays. This paper proposes a broadband first-order voltage-mode all-pass filter as a true-time-delay cell. The proposed true-time-delay cell is capable of tuning delay, demonstrating its potential capability to be used in different systems, e.g., RF beam-formers. The proposed filter achieves a flat group delay of over 60 ps with a pole/zero pair located at 5 GHz. This proposed circuit consumes only 10 mW power from a 1.8-V supply. To demonstrate the performance of the proposed all-pass filter, simulation results are conducted by using Virtuoso Cadence in a standard TSMC 180-nm CMOS process.

Keywords: all-pass filter; CMOS; time delay; broadband; true-time-delay

1. Introduction

All-pass filters as delay cells have a variety of applications in signal processing and communication systems, like equalizers and analog/RF beam-formers [1–6]. In these circuits, the amplitude of the input signal is constant over the desired frequency band, while creating a frequency-dependent delay. There are several reported approaches to approximately realize delay, such as transmission lines and lumped LC delay lines [7,8], which are passive components and, thus, are area inefficient, and also phase shifters for narrow-band frequencies [9–14]. Apart from these circuits, an active RF all-pass filter can be the best option to approximate delay due to its size and delay to area ratio [15,16].

There are many voltage-mode all-pass filters reported over the last one decade, which operate in broadband frequencies and have different applications [15–21]. In some applications, e.g., RF beam-forming, delay stages as delay cells are normally realized by cascading first-order all-pass filters in order to achieve a desired delay [15–17]. However, there are just a few first-order voltage-mode all-pass filters for wide frequency ranges in the literature [15–17,22]. This is because these analog circuits should possess important specifications like wide bandwidth, efficient area, low cost, and power consumption, and high delay amount to be considered as practical and efficient systems. Furthermore, recent circuits have been taking advantage of tunability, since it is one of the key features of signal processing and communication systems [15,16,18,23].

A broadband first-order voltage-mode all-pass filter as a true-time-delay cell is introduced in this paper. The proposed all-pass filter is comprised of two transistors, two resistors, and one grounded inductor. This circuit demonstrates a large amount of delay in a single delay cell through a wide frequency band. The amount of delay can be controlled within the frequency range of interest. Moreover, circuit optimization is carried out to increase the operating frequency and improve the performance of the filter, in particular, in high frequencies.

The structure of this paper is as follows: Section 2 describes the structure of proposed all-pass filter and provides theoretical analyses. In Section 3, circuit optimization technique and tunability are presented, and also the parasitic effects of the proposed filter are evaluated. Section 4 provides results and ultimately a discussion is provided in Section 5.

2. Proposed First-Order All-Pass Filter

Figure 1 shows the block level of the first-order voltage-mode all-pass filter. As shown, a first-order all-pass filter can be approximated by the combination of two sections: a low-pass section with a DC gain of 2 and a unity gain section [24]. Therefore, its ideal transfer function is given as:

$$H(s) = e^{-s\tau} \approx \frac{-2}{1+s(\tau/2)} + 1 = -\frac{1-s(\tau/2)}{1+s(\tau/2)}, \quad (1)$$

where τ is the time delay. Ideally, the gain of the transfer function is 1 and its phase is linear versus the frequency.

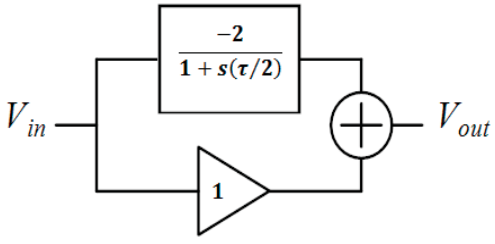

Figure 1. Block diagram of the first-order all-pass filter.

Figure 2 illustrates the block diagram and schematic of the proposed broadband first-order voltage-mode all-pass filter. In this filter, transistor M_1, inductor L, and resistor R_L form the low-pass part, while transistor M_2 and resistor R_L comprise the unity-gain part. In other words, M_1 and M_2 are, respectively, common-source (CS) and common-gate (CG) configurations to convert the input voltage signal into current. At the output node, the drain currents of M_1 and M_2 are subtracted to realize an all-pass function. Then, the output signal will be converted back to voltage by the load resistor R_L.

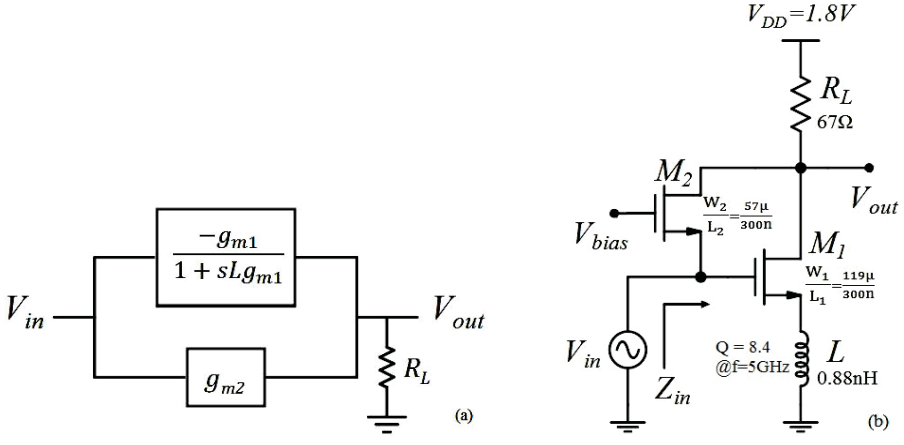

Figure 2. (**a**) Block diagram and (**b**) schematic of the proposed first-order all-pass filter.

Ignoring the parasitics of the transistors (the parasitic effects will be assessed in Section 3) for simplicity, the transfer function of the proposed first-order all-pass filter can be determined by:

$$\frac{V_{out}}{V_{in}}(s) = -\frac{g_{m1}R_L}{1+sLg_{m1}} + g_{m2}R_L = -R_L(g_{m1}-g_{m2})\cdot\frac{1-sL\frac{g_{m1}g_{m2}}{g_{m1}-g_{m2}}}{1+sLg_{m1}}, \quad (2)$$

where g_{m1} and g_{m2} are the transconductances of M_1 and M_2, respectively. If $g_{m1} = 2g_{m2}$ and $g_{m2}R_L = 1$, an all-pass structure will be realized with the same frequency of the left-plane pole and right-plane zero, resulting in twice the phase and group delay responses of an all-pass circuit. As a consequence, the transfer function in (2) can be simplified as:

$$\frac{V_{out}}{V_{in}}(s) = -\frac{1-sLg_{m1}}{1+sLg_{m1}}. \quad (3)$$

The pole/zero frequency and phase response of the first-order all-pass filter can be given as:

$$|\omega_{p,z}| = \frac{1}{Lg_{m1}}, \quad (4)$$

$$\phi(\omega) = -2tan^{-1}(\omega Lg_{m1}), \quad (5)$$

respectively, and, thus, group delay response is expressed by:

$$D(\omega) = -\frac{\partial\phi(\omega)}{\partial\omega} = 2Lg_{m1}\cdot\frac{1}{1+(\omega Lg_{m1})^2}, \quad (6)$$

where ω is the angular frequency related to the frequency f through $\omega = 2\pi f$. The group delay is approximately equal to $2Lg_{m1}$ at low frequencies. However, this group delay is practically affected by parasitic inductances stemmed from, e.g., bonding wire and PCB and, thus, its value will be increased. The input impedance of the proposed all-pass filter can be simply approximated by considering the Miller effect on the parasitic capacitances of the transistor M_1 plus C_{gs2} given as:

$$C_{in} \approx \frac{\left(C_{gs1}+C_{gd1}\right)(3+sLg_{m1})}{1+sLg_{m1}} + C_{gs2}, \quad (7)$$

which its value affects the next delay stage for cascading purposes.

3. Circuit Optimization and Tunability

In order to contribute to the linearity and increase the operating frequency of the proposed all-pass filter, a variable resistor (R_d) is added to the unity-gain path as shown in Figure 3. In this case, a discrete tuning of delay can be carried out by changing the value of R_d and the bias voltage of M_2 as well, which adjusts g_{m2}. The R_d can be implemented by a switched resistors bank which can be implemented by CMOS transistors, with great ease.

The transfer function of the CG transistor of M_2 (the part inside the dotted box) is, therefore, given as:

$$H_{CG}(s) = \frac{g_{m2}R_L}{1+sC_{gd2}(R_L+R_d)}. \quad (8)$$

Its value for low and high frequencies is $H_{CG,LF} \approx g_{m2}R_L$ and $H_{CG,HF} \approx g_{m2}R_L/C_{gd2}(R_L+R_d)$, respectively. Hence, the R_d will affect the frequency response of the proposed filter at higher frequencies. Note that $g_{m2}R_L$ (i.e., the unity gain section) is no longer equal to 1 at high frequencies, but via varying the bias voltage of M_2, g_{m2} changes and, therefore, the two conditions $g_{m1} = 2g_{m2}$ and $g_{m2}R_L = 1$ will be satisfied.

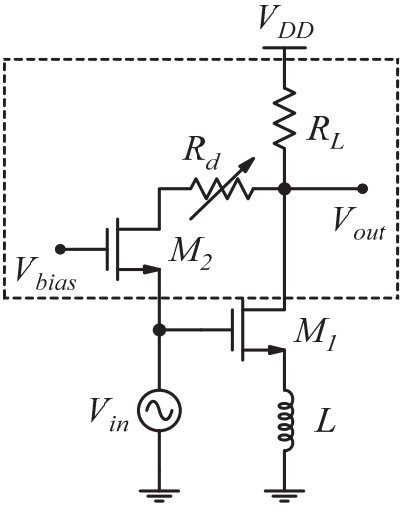

Figure 3. The optimization and tunability technique.

Non-Ideality Analysis

To analyze accurately the performance of the proposed all-pass filter in Figure 3 at high frequencies, the finite output impedances (g_{ds}) and parasitic capacitances (C_{gs} and C_{gd}) of the transistors M_1 and M_2 should be considered. Therefore, the transfer function in (2) can be rewritten as:

$$\begin{aligned}&\frac{V_{out}}{V_{in}}(s)\\&\approx -\frac{R_L(g_{m1}-g_{ds1})-s\left(Lg_{m1}g_{ds1}R_L+C_{gd1}R_L\right)}{sL(g_{m1}+g_{ds1})\left[1+g_{ds1}R_L+R_L\left(g_{ds1}+sC_{gd1}\right)\right]+1+R_L\left(g_{ds1}+sC_{gd1}\right)}\\&+\frac{R_L(g_{m2}+g_{ds2})}{sC_{gd2}(R_L+R_d)+1+g_{ds2}(R_L+R_d)}.\end{aligned} \tag{9}$$

If $g_{m1,2} \gg g_{ds1,2}$, $g_{ds1,2}R_L \ll 1$, and $g_{ds2}R_d \ll 1$, the transfer function in Equation (9) can be simplified as:

$$\frac{V_{out}}{V_{in}}(s) = -\frac{g_{m1}R_L\left(1-s\frac{Lg_{m1}g_{ds1}+C_{gd1}}{g_{m1}}\right)}{\left(1+sC_{gd1}R_L\right)(1+sLg_{m1})}+\frac{g_{m2}R_L}{1+sC_{gd2}(R_L+R_d)}, \tag{10}$$

which includes additional parasitic poles and zero. These parasitic high-frequency poles stemmed from C_{gd1} and C_{gd2}, which are located at $1/C_{gd1}R_L$ and $1/C_{gd2}(R_L+R_d)$ respectively, are far beyond the dominant pole in Equation (4) since the values of R_L and R_d are small. Moreover, the additional right-plane zero $(g_{m1}/Lg_{m1}g_{ds1}+C_{gd1})$ is located at considerably higher frequencies, as well.

Additionally, small-signal analysis conducted on the proposed all-pass circuit indicates that the third parasitic pole stemmed from C_{gs1} will be located at:

$$\omega_{p3} = -\frac{\left[g_{m1}\left(1+\sqrt{1-\frac{4C_{gs1}}{Lg_{m1}^2}}\right)\right]}{2C_{gs1}} \approx -\frac{g_{m1}}{C_{gs1}}, \tag{11}$$

which is far beyond the dominant pole in Equation (4). It can be noted that the order of the proposed circuit will increase and convert to the second one if the absolute value of C_{gs1}, which is

process-dependent, is large enough. Consequently, choosing an appropriate CMOS process can reduce the effect of the C_{gs1} on the frequency response of the circuit.

4. Results

The proposed first-order all-pass filter is designed in a standard 180-nm TSMC CMOS process and results are obtained using Virtuoso Cadence. The proposed all-pass filter is simulated without and with the R_d. The power consumption of the proposed broadband true-time-delay cell is only 10 mW from a 1.8-V supply voltage.

Figure 4 shows the gain and phase responses of the proposed filter under different values of the R_d. As it can be observed, the gain of the proposed filter without the R_d (i.e., $R_d = 0\ \Omega$) is almost -0.5 dB due to the existence of the parasitic capacitors and finite output impedances of the transistors. Furthermore, the proposed filter does not achieve desired (flat) gain responses at higher frequencies, whereas by varying the value of the R_d, better gain responses are proved at these frequencies. As seen, the pole/zero frequency of the proposed circuit with $R_d = 120\ \Omega$ is 5 GHz (i.e., the point where phase is 90°), indicating a 14% bandwidth improvement compared to once $R_d = 0\ \Omega$ (i.e., 4.4 GHz).

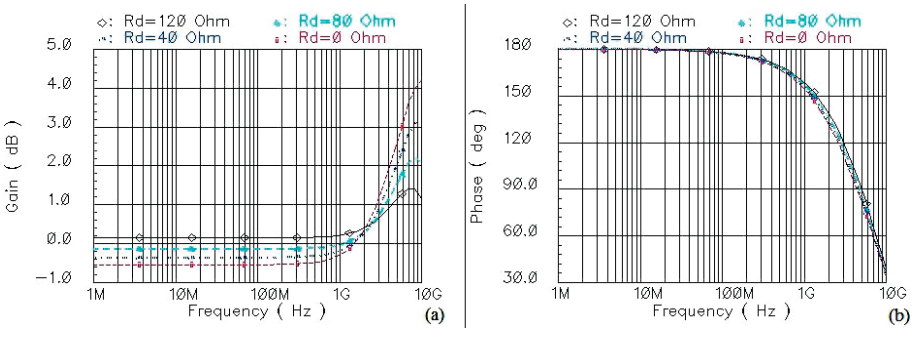

Figure 4. Simulated results for (**a**) gain response and (**b**) phase response of the proposed first-order all-pass filter under different values of the R_d.

The group delay responses of the proposed all-pass filter for different values of the R_d are shown in Figure 5. As it can be seen, the delay can be controlled by varying the R_d. The group delay is equal to about 59 ps, when $R_d = 120\ \Omega$. This group delay value is very close to the theoretical one in Equation (6), with an error of around 11%.

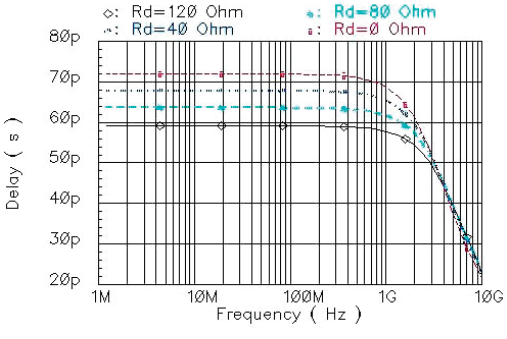

Figure 5. Simulated group delay responses of the proposed first-order all-pass filter under different values of the R_d.

In Figure 6, the input-referred noise response of the all-pass filter is shown when $R_d = 120\ \Omega$. The input-referred noise value is approximately 2.36 nV/sqrt (Hz) by the frequency of 1 GHz. Figure 7 shows the noise figure of the proposed all-pass filter with $R_d = 120\ \Omega$, which is <15 dB over the frequency band. The input-referred 1-dB compression point (P_{1dB}) and input-referred third-order intercept point (IIP3) responses of the first-order all-pass filter with $R_d = 120\ \Omega$ are shown in Figure 8. The input-referred P_{1dB} and IIP3 are -1.9 dBm and 16.6 dBm at 2.5 GHz, respectively.

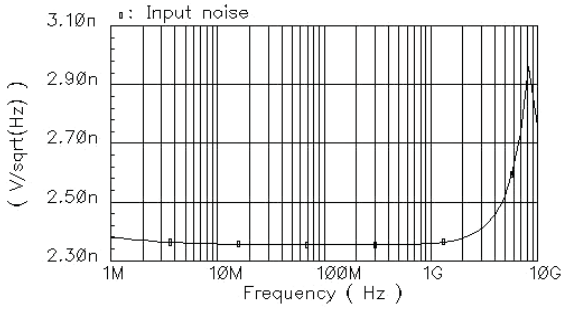

Figure 6. Simulated input-referred noise response of the proposed first-order all-pass filter.

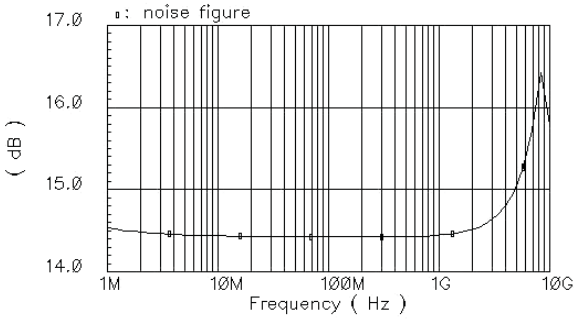

Figure 7. Simulated noise figure response of the proposed first-order all-pass filter.

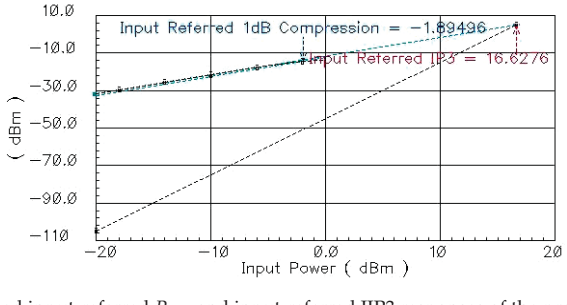

Figure 8. Simulated input-referred P_{1dB} and input-referred IIP3 responses of the proposed first-order all-pass filter.

Since the amount of group delay is affected by the mismatch and is basically process, voltage, and temperature (PVT) dependent, we should therefore consider the effect of these variations on the proposed true-time-delay cell. Figure 9 illustrates Monte Carlo simulation results, which are performed with a Gaussian distribution and 100 iterations, when $R_d = 120\ \Omega$. As it can be seen, the difference between group delay responses due to the mismatch is very small. Although the gain, P_{1dB}, and IIP3 will be affected by the mismatch, these variations can be minimized by changing the

bias voltage of M_2. The group delay responses of the proposed filter with $R_d = 120\ \Omega$ for different supply voltages and temperatures are shown in Figure 10. The delay degrades by 15% because of the temperature variations.

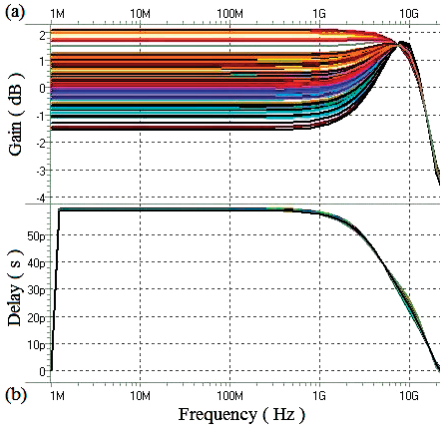

Figure 9. Monte Carlo simulation results for (**a**) gain response and (**b**) group delay response of the proposed first-order all-pass filter.

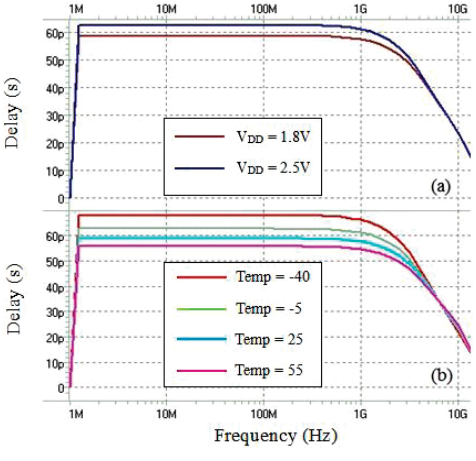

Figure 10. Simulated group delay responses of the proposed first-order all-pass filter for (**a**) different supply voltages and (**b**) different temperatures.

A comparison between recently reported voltage/current all-pass filters and the proposed true-time-delay cell is presented in Table 1. Comparing the results of the first-order voltage-mode all-pass filters, the proposed filter has improved the frequency range compared to the filter in [15]. Moreover, the power consumption and delay tuning can be highlighted and compared with the filter in [22], in which the delay could not be tuned.

Table 1. Performance summary and comparison between broadband all-pass filters.

Reference	Technology	Mode	Order	Frequency (GHz)	Max. Delay (ps)	P_{1dB} (dBm)	IIP3 (dBm)	Power (mW/V)
[15]	140-nm CMOS	Voltage	1st	1–2.5	61 [1]	N/A	N/A	10 [2]/1.5
[19]	SiGe2RF HBT	Voltage	2nd	3–10	75	−1	N/A	38.8/2.5
[20]	130-nm CMOS	Voltage	2nd	6	55	−5.5	2	18.5/1.5
[22]	130-nm CMOS	Voltage	1st	9	49 [3]	−2	8.5	20.4/1.5
[25]	130-nm CMOS	Current	1st	0.3–5.1	82	N/A	N/A	6.15/1.5
[26]	180-nm CMOS	Voltage	2nd	3–12	8.5	14.6	22.6	12/1.8
This work	180-nm CMOS	Voltage	1st	5	59 [4]	−1.9	16.6	10/1.8

[1] A maximum delay of 550 ps was achieved by three fine and six coarse delays. [2] A maximum power of 90 mW was consumed by three fine and six coarse delays. [3] Pre-layout group delay of 33 ps expected for the filter. [4] Simulated group delay value can be increased by varying the value of variable resistor in the proposed filter.

5. Discussion

Compared to the bulky LC delay lines, active filters can be good alternatives to approximate delays as these filters occupy smaller area. This paper presents a broadband first-order voltage-mode all-pass filter as an active circuit. Via an optimization technique, 14% bandwidth extension is achieved. The proposed first-order all-pass filter demonstrates a flat group delay of approximately 60ps through a bandwidth of 5 GHz, while consuming merely 10 mW power. Unlike the active all-pass filter in [22], the proposed filter has a DC-gain of 1 in its voltage transfer function and consequently there is no need for the gain adjustment via additional circuits or components. Furthermore, the proposed circuit proves a frequency range wider than that of the reported active filter in [15] (pre-layout pole frequency of 2.63 GHz), however at a larger area. The proposed all-pass filter is almost linear and achieves the input-referred P_{1dB} of −1.9 dBm and the input-referred IIP3 of 16.6 dBm. We will employ the proposed all-pass filter-based true-time-delay cell in analog RF beam-forming antennas for communication applications in our future work (see Figure 11). In timed-array receivers, tunable true-time-delay cells are exploited to align broadband signals received from a particular direction (θ).

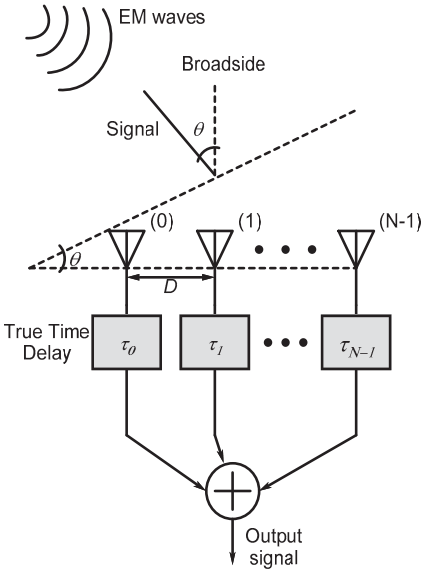

Figure 11. Block diagram of an N-element timed-array receiver.

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Conflicts of Interest: The authors declare no conflict of interest.

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