Electrochemical noise limits of femtoampere-sensing, CMOS-integrated transimpedance amplifiers

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Abstract

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Low-noise operational amplifiers are an important tool in the life sciences. Biosensor measurements typically rely on low-noise transimpedance amplifiers to record biological signals. Two different techniques were used to leverage the advantages of low-noise circuitry for bioelectronics.

A CMOS-integrated system for measuring redox-active substrates using electrochemical read-out at very low noise levels is presented. The system incorporates 112 amplifier channels capable of current sensing with noise levels below 1 fA_{rms} in a 3.5-Hz bandwidth. The amplifier is externally connected to a gold microelectrode with a radius of 15 µm. The amplifier enables measurement of redox-couples such as potassium ferrocyanide/ferricyanide with concentrations down to 10 nM at current levels of only 300 fA. The electrochemical noise that sets the limits of detection is also measured and analyzed based on redox mass transfer equation and electrochemical impedance spectroscopy.

Secondly, CMOS-integrated low noise junction field-effect transistors (JFETs) were developed in a standard 0.18-µm CMOS process. These JFETs reduce input referred flicker noise power by more than a factor of 10 when compared with equally sized n-channel MOS devices by eliminating oxide interfaces in contact with the channel. We show that this improvement in device performance translates into a factor-of-10 reduction in the input-referred noise of integrated CMOS operational amplifiers when JFET devices are used at the input.

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Chapter 1: Introduction

Molecular biology has emerged as an extremely important field due to the impact that it has on healthcare, disease treatment, and medical diagnosis. Fully leveraging the expanding knowledge of human biology requires improved healthcare tools for biological assays and rapid analysis. Advanced electronic systems are used to improve our understanding of DNA, proteins, bacteria, viruses, toxins, and other biomolecules in the context of the human body and human health. These systems often combine specialized biosensors with electrical amplifiers and control circuitry to record information from the target molecules.

Following the advent of the transistor, the advancement of electronics and semiconductor devices accelerated based on the exponential scaling principle of integrated electronics known as Moore's Law. The miniaturization and increased operating speed of microelectronics has quickly allowed electrical devices to become more portable and powerful. The combination of scaling electronics technology with biosensors has enabled vast improvements in terms of speed, portability, and reliability for medical and bioassay technology. The integration of biosensors into electronic systems permits measurement of biomolecules in a more direct and fundamental way than is possible with other sensing modalities such as optical or chemical measurements.

Communication within and between cells uses chemical and electrical signals which transfer minute quantities of energy. Often in bioelectronic measurements, the signals of interest are small and capturing every single electron is paramount. However, random signals and processes are common in biological, chemical and electrical systems. These random signals cause noise and interference which can contaminate or completely drown out the signal of interest. Analysis, simulation and measurement of noise can improve understanding of noise and its sources. This can in turn produce techniques to reduce, circumvent or eliminate

the noise. In this thesis, I will present two integrated amplifiers designed and fabricated using different approaches for noise reduction to improve their performance for biochemical measurements. The first project involves creating new CMOS-integrated Junction Field Effect Transistors (JFETs) specifically to reduce the electronic noise of measurement front-end amplifiers for small signal inputs. The second project involves the creation of a low-noise CMOS amplifier with femtoampere noise resolution which is used to measure electrochemical signals.

1.1 Thesis Outline

Chapter 2 provides an overview of electronic noise in the context of biological recordings and the particular benefits of JFET devices. This chapter also introduces electrochemistry using cyclic voltammetry, applications of electrochemical sensors for detecting and analyzing chemical compounds, and the origins of electrochemical noise.

Chapter 3 relates the design of low-noise JFETs created in a commercial 0.18 µm CMOS process, which are used to reduce circuit noise. These JFETs are used to construct a custom CMOS-integrated low-noise amplifier for biosensing measurements.

Chapter 4 describes the design and testing of a low-noise CMOS amplifier array for electrochemical voltammetry of femtoampere-level currents. The chip is fabricated in a commercial 0.13 µm process and contains 112 independent channels.

Chapter 5 investigates the use of the electrochemical amplifier presented in Chapter 4 to measure potassium ferrocyanide and potassium ferricyanide at submicromolar concentrations. Chapter 5 also demonstrates the connection between the properties of the electrode-electrolyte interface and the electronic and electrochemical noise processes that establish the limits of detection.

Chapter 6 concludes with a summary of the contributions of this author to the fields of electrical and electrochemical noise reduction and discussion of future work to be done in these areas.

Chapter 2: Background

2.1 Introduction

Biosensors have often been integrated with electronics through the use of current-based transimpedance amplifiers (TIAs). Current amplification is a simple and powerful method to interrogate biomolecules, since many biological process and bioassays can produce electrical current directly. Current amplifiers have enabled studies using ion channels [1], solid-state nanopores [2], nanopipettes [3], carbon nanotube transistors [4], nanowires [5], and many other biosensors. In these applications and others, electrical current can be transduced from biomolecules, allowing for connection of biosystems to computer systems for recording and analysis. Particularly, the use of integrated Complementary Metal Oxide Semiconductor (CMOS) technology enables the design of small size, high speed, and high sensitivity TIAs for these applications [6]–[15].

CMOS-integrated amplifiers confer many advantages for biosensing measurements when compared to discrete electronics including small design areas, faster transistor opration, and lower power consumption. These advantages lead to more compact and powerful amplifiers circuits scalable for high-speed multi-channel measurement which can approach parity with the physical size of biological systems. In addition, CMOS processes have powerful electronic simulation capabilities through sophisticated device modeling, which allows circuit designs to be extensively tested before production.

The design of microscale amplifiers becomes much more complicated when biological systems are introduced. Often biosystems are not easily characterized by an electronic model and need to be studied and characterized separately in order to ensure the integration with the silicon technology is possible. In addition, biosensors often produce signals of

nanoamperes or lower, thus making electronic design to accommodate these restrictions even more difficult. One of the greatest concerns in the design of an electronic system for biosensing is the amount of electrical and bioelectrical noise that will exist in the system. If the quantity of system noise is too high, the biosignal of interest becomes difficult to isolate from the background.

Careful design of electronic systems for measuring biochemical signals requires thorough understanding of noise from both circuit and sensor. First, the basics of noise in electronic circuits will be explained with considerations for biological measurements. Junction field-effect transistor (JFET) devices will be presented as a tactic to reduce the electronic noise contribution from the measurement system. Electrochemistry will be introduced as a sensing modality to detect, measure, and interact with biomolecules. Finally, the noise of the electrochemical interface will be addressed to understand the limitations and considerations when measuring electrochemical systems.

2.2 Signal-to-noise ratio of amplifiers

The vast improvements of CMOS fabrication for electronics has enabled the design of many different integrated circuits (ICs) for a variety of scientific fields, including biosensing. ICs are especially well suited to biosensing applications as miniaturization can reduce input parasitic capacitance, resistance and inductance while increasing circuit density.

However, short-channel CMOS circuits introduce parasitic effects that can cause problems in biosensor applications, particularly random electronic noise. Since biosensors typically produce only small electrical signals, random noise of the measurement electronics can obscure the signal. Noise has been studied in depth for electronic systems, enabling the creation of accurate noise models for simulation and circuit design.

2.2.1 Noise analysis

When considering circuit noise, it is simplest to think of any noise source as a perturbation $n(t)$ that is added on top of the signal current $y_i(t)$ to create the total signal:

$$y(t) = y_i(t) + n(t) \tag{2.1}$$

Because of the random nature of noise, it is not possible to perform most noise analysis in the time domain. If some assumptions are made about the nature of the noise signal, analysis can instead be performed in the frequency domain through the use of the Fourier transform. Assuming that the noise process has a mean μ and autocovariance $K_{XX}(\tau)$ that are constant with time and the standard deviation σ is finite, then the power spectral density (PSD) is also unchanging with time. With these assumptions, the PSDs of the noise and signal can be summed for an overall spectrum of

$$S_y(t) = S_{y_i}(t) + S_n(t) \tag{2.2}$$

The standard deviation of the noise can be determined by integrating the PSD over all frequencies, given by

$$\sigma = \sqrt{\int_0^\infty S_n(f)df} \tag{2.3}$$

The above equation can typically be constrained by the length of the measurement for the lower limit, and to the measurement bandwidth B for the upper limit. Given that the measurement can be extended arbitrarily to set the lower bandwidth, the standard deviation becomes

$$\sigma = \sqrt{\int_0^B S_n(f)df} \tag{2.4}$$

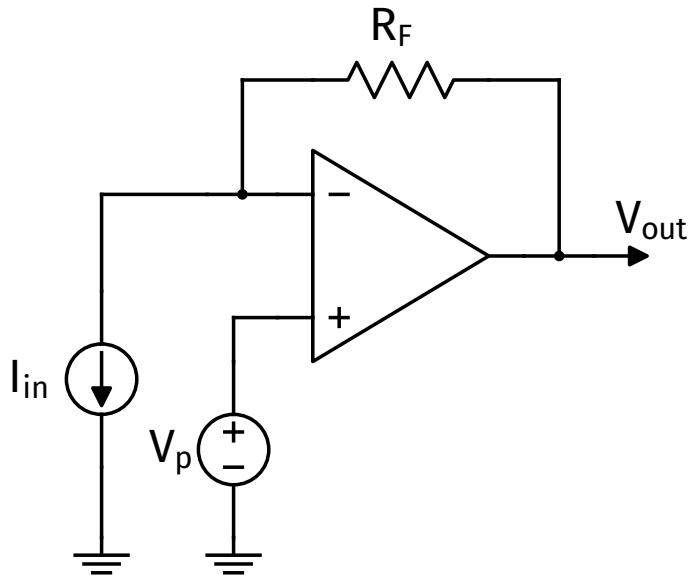


Figure 2.1: Basic transimpedance amplifier topology

The standard deviation of the noise, σ, can be used to establish a figure of merit for low-noise amplifiers. The signal-to-noise ratio (SNR) divides the magnitude of the signal of interest by the root-mean-square noise and is given by

$$\text{SNR} = \frac{I_{\text{signal}}}{i_{\text{rms}}} = \frac{I_{\text{signal}}}{\sqrt{\int_0^B S_n(f)df}} \tag{2.5}$$

Improving SNR by increasing signal current and decreasing circuit noise will improve the system's capability to measure very small signals.

2.2.2 Noise spectra

Because many biosensors transduce inputs into small currents, amplifiers are often used to increase the signal. A transimpedance amplifier (TIA), such as the simple topology shown in Figure 2.1, can be used to convert input current into output voltage. Amplifiers for measurement circuitry, including TIAs, are typically designed to have linear transfer functions. The linear transfer function of a TIA means that the input current $I(t)$ can be

compared with the output voltage $V(t)$ in the frequency domain as

$$V(f) = H(f)I(f) \tag{2.6}$$

where $H(f)$ is the frequency domain transfer function. This simplifies comparison of different amplifiers, as signals can be referred to the input and made independent of gain ($|H(f)|$). This is particularly useful when comparing TIA noise, since the magnitude of the signal current can be compared to the average noise power at the input. Given a voltage noise at the output of $v_n(t)$, the voltage noise spectrum can be converted to an input current noise using

$$S_{n,in}(f) = \frac{S_{n,out}(f)}{|H(f)|^2} \tag{2.7}$$

Different components of the circuit will contribute different amounts and types of noise. Assuming that the individual noise components all produce noise that is independent of each other (i.e. that the cross-correlation between the noise signals is zero), then the total output noise will be the sum of each component ($X_i(f)$) times the transfer function from that node to the output ($H_i(f)$). This allows for the individual noise sources for a TIA to be broken down to see how each contributes to the final noise and how best to mitigate the contributions to the final noise output. The total noise from N noise sources can then be input-referred using

$$S_{n,in}(f) = \frac{1}{|H(f)|^2} \sum_{i=0}^{N} X_i(f)|H_i(f)|^2 \tag{2.8}$$

In an amplifier circuit, the gain from a noise source to the output $H_i(f)$ should decrease as the source is located further from the input. This implies that the noise sources closest to the input contribute the most to the overall noise, as noise sources further away will be divided by more gain. Reducing the noise of devices close to the input while simultaneously increasing

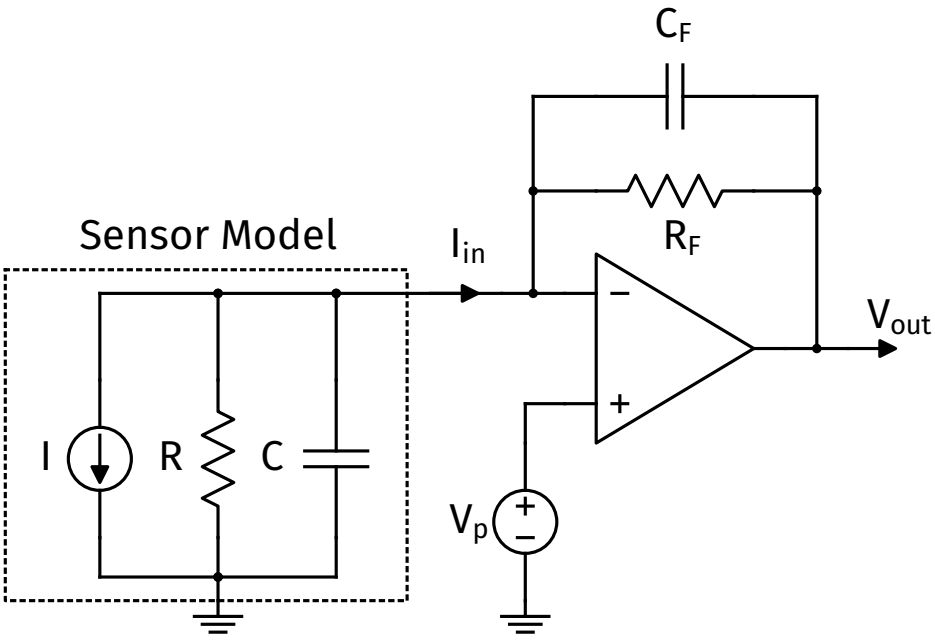


Figure 2.2: Basic transimpedance amplifier connected to simplified biosensor model

the gain of the input stages as much as possible will result in the lowest input-referred noise and increased SNR.

The next sections discuss the various types and sources for noise found in a TIA as used in a typical biosensing application. A typical TIA topology is shown in Figure 2.2 with the sensor represented by a simplified model using a resistor, capacitor, and current source in parallel.

Flicker noise

Flicker noise is noise which varies inversely with frequency. A variety of devices and sensors exhibit flicker noise, although the physical origin of the noise may differ. In semiconductors, there are two widely explored models that address the presence of flicker noise. The Hooge model attributes flicker noise to fluctuations in carrier mobility in semiconductor materials [16]. The McWhorter model instead explains flicker noise through the variations in the number of charge carriers in semiconducting materials [17]. Several efforts have modeled flicker noise using a combination of the two models [18]–[20].

Flicker noise in semiconductors is typically attributed to charge traps occurring at interfaces between materials, semiconductor dopants, and crystal defects. The presence of a small, countable number of defects in very small metal-oxide-semiconductor field-effect transistor (MOSFET) devices has been found to exhibit random telegraph signals (RTS) as single charge carriers are trapped and released by defects [21], [22]. RTS noise results in a Lorentzian power spectrum.In larger devices, there are many more defects each of which results in a Lorentzian spectrum. When the Lorentzian spectra for many defects are summed, the result is a current noise spectrum which varies directly with $1/f$. Flicker noise is thus referred to as $1/f$ noise, however the exact variation with frequency may differ from f^{-1} depending on the source.

Flicker noise in biosensor applications can originate both from within the measurement amplifier and from the actual biosensor. Flicker noise in semiconductor devices can be roughly considered to have the following PSD:

$$S_n(f) = SI^{\alpha}/f^{\beta} \tag{2.9}$$

where S represents the flicker noise magnitude, α represents the noise dependence on the current in the device I, and β represents the noise slope of the spectra.

White noise

White noise is a generic term for any noise source that contributes equal noise power at all frequencies. Thermal, or Johnson-Nyquist, noise is one type of white noise which is caused by the thermal fluctuation of charge carriers in resistive materials. The noise spectrum for thermal noise is

$$S_n(f) = 4k_BTR \tag{2.10}$$

where k_B is Boltzmann's constant ($k_B = 1.381 \times 10^{-23}$ J/K), T is the temperature in Kelvin, and R is the resistance of the material. Thermal noise occurs in all kinds of resistive materials, including the conductive channels of MOSFETs, bipolar junction transistors (BJTs) and JFETs. The TIA from Figure 2.2 would have thermal noise that originates from the transistors making up the amplifier, the feedback resistor R_F and the sensor resistance R.

Shot noise is also white noise caused by fluctuations in the kinetic energy of charge carriers. The kinetic energy fluctuation results in arrival times governed by Poisson statistics and this uncertainty results in shot noise, which has a PSD given by

$$S_n(f) = 2zqI \tag{2.11}$$

where z represents the electrical charge count for each particle, q represents the electron charge ($q = 1.609 \times 10^{-19}$ C), and I is the current.

f noise

Noise that increases in proportion with frequency can occur in TIA circuits. One origin for noise that scales directly with frequency is from dielectric relaxation of the insulating materials. This can include the capacitance of the sensor, amplifier, feedback capacitor, and any board parasitics. The noise associated with this dielectric relaxation for all sources can be summed and results in a noise spectrum of

$$S_n(f) = 8\pi k_B T \tan\delta C f \tag{2.12}$$

where $\tan\delta$ is the loss coefficient of the dielectric material, and C is the total capacitance.

Noise with a proportional dependence on frequency can also originate when voltage noise from the amplifier interacts with capacitance at the input. This noise is discussed in the following section.

f^2 noise

The amplification of the op-amp voltage noise spectrum by the capacitive elements of the circuit results in a current that varies with f^2. This noise results when the voltage noise spectrum of the op-amp is amplified from the positive terminal to the circuit output. The transfer function from the input voltage to the input current is derived by

$$\begin{aligned} v_o(f) = Z_f i_n(f) &= \frac{v_n Z_F}{Z_F + Z_{in}} \\ i_n(f) &= \frac{v_n(f)}{Z_f + Z_{in}} \\ i_n^2(f) &= \frac{v_n^2(f)}{(Z_f + Z_{in})^2} \end{aligned} \tag{2.13}$$

Then assuming that the input impedance is much greater than the feedback impedance ($Z_f << Z_{in}$), and that the capacitive elements dominate at higher frequencies ($Z_{in} \approx 1/(j\omega C_{in})$), the input referred current noise power can be derived as

$$S_n(f) = |i_n^2(f)| = (2\pi \Sigma C_{in} v_n(f))^2 f^2 \tag{2.14}$$

where ΣC_{in} is the sum of all capacitive contributions at the input of the TIA including the feedback capacitor C_F, input capacitance of the op-amp C_I, wiring capacitance C_W, and sensor capacitance C.

Because the voltage noise of the op-amp $v_n(f)$ typically has both $1/f$ and thermal noise components, (2.14) has both f and f^2 components. This term is particularly important in low-noise, high gain amplifiers, as the low thermal noise of the amplifier reveals the capacitive noise even at low frequencies (100 Hz and below). These noise implications will be further discussed in Section 2.5 and 5.4.1.

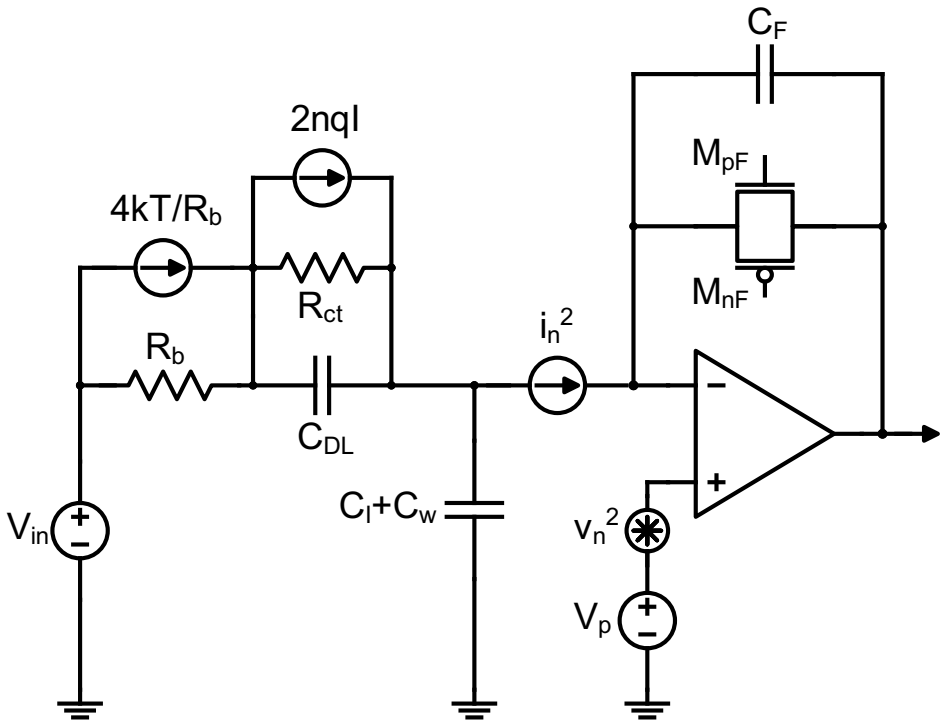


Figure 2.3: TIA topology with typical noise sources and redox sensor

2.3 JFETs

A direct method to reduce the circuit noise of TIAs is to improve the semiconductor devices used to construct them. CMOS technology has had a revolutionary impact on creating tiny, fast, and cheap circuits, but MOSFETs are not the best choice for experiments where low noise is a priority. For low noise discrete amplifiers, JFETs are typically used instead of MOSFETs for their high gain and low noise [23].

2.3.1 History of low noise amplifiers

Devices for computation have changed dramatically over the years from mechanical computers to vacuum tubes and finally to MOSFET devices and integrated circuits. Each type of device has intrinsic noise that determines the fundamental limits of detection.

The discovery of the MOSFET and the explosion of miniaturized semiconductor technology has improved circuit performance dramatically, but the fundamental limitations of

circuit noise still control signal sensitivity. Careful circuit design can help minimize the effects of noise, however combining this with optimized semiconductor devices is key to pushing down the noise of circuits.

Before the widespread use of CMOS technology to create integrated circuits, JFETs were used to create the best performing amplifiers for biological research [24]. In 1972, Holmer, et al. [24] compared three different circuit elements chosen for constructing a biological amplifier: Electrometer tube, JFET and IGFET, or insulated gate field-effect transistor, which corresponds to what are now called MOSFET devices. JFET input devices were used based on their superior noise performance for the application of biological sensing [24].

Fifty years later, the widespread use and improvement of MOSFET devices has changed the landscape of semiconductor devices. However, modern MOSFET devices have inferior low frequency noise performance when compared to JFETs. Discrete JFET devices are still used for the construction of biological and high sensitivity amplifiers due to their lower noise [23].

Additionally, JFET devices have been designed for co-fabrication in CMOS processes to take advantage of the benefits of both JFET devices and CMOS fabrication processes.

More recent efforts have used both discrete and integrated JFETs for a variety of applications, including radio frequency circuits [25], bio-potential amplifiers [26], [27], device testing circuits [28], photonics [29], and numerous physics and space applications [30]–[33].

2.3.2 JFET structure

JFETs are a basic type of silicon-based electronic device that can be used to create circuits. JFETs have one of the simplest transistor structures, typically consisting of n-type conducting channel that is bordered by one or two p-type gate regions, as shown in Figure 2.4. P-channel JFETs can also be constructed by reversing the doping of the diffusion regions. The source and drain are connected on either side of the channel, separated by the gate constriction. Transistor operation involves applying a negative bias between the n-

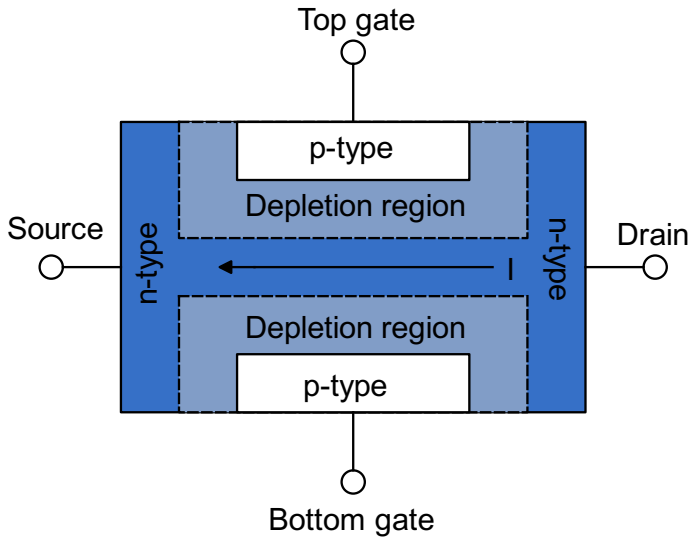


Figure 2.4: Basic JFET device structure

type channel (source and drain) and the p-type gates, thus depleting the conductive channel of dominant carriers as the interfaces operate as reverse-biased diodes. Increased negative voltages move the device from saturation (fully open), to linear (partially depleted), and then to cutoff (fully depleted). JFETs are therefore characterized as depletion mode (normally on) devices, as the application of voltage shuts off conduction in the channel. This is in contrast with BJTs and MOSFETs, which are generally enhancement mode (normally off) and require the application of voltage to enable current flow from source to drain.

Typical CMOS processes do not support JFET structures since JFET fabrication requires the use of additional masks and implants. However, some processes can support JFET structures with alternative use of triple-well implants [25], ESD implants [34], and other techniques, as will be discussed in Section 2.3.5.

2.3.3 Benefits and downsides of JFET versus MOSFET, BJT

Differences in the behavior of JFET devices when compared to other semiconductor devices make JFETs better for a variety of measurement applications. JFETs have lower noise, especially in the 1/f spectra than MOSFET or BJT devices, due to the reduced quantity of charge traps. The low noise properties of JFETs will be discussed in more detail in

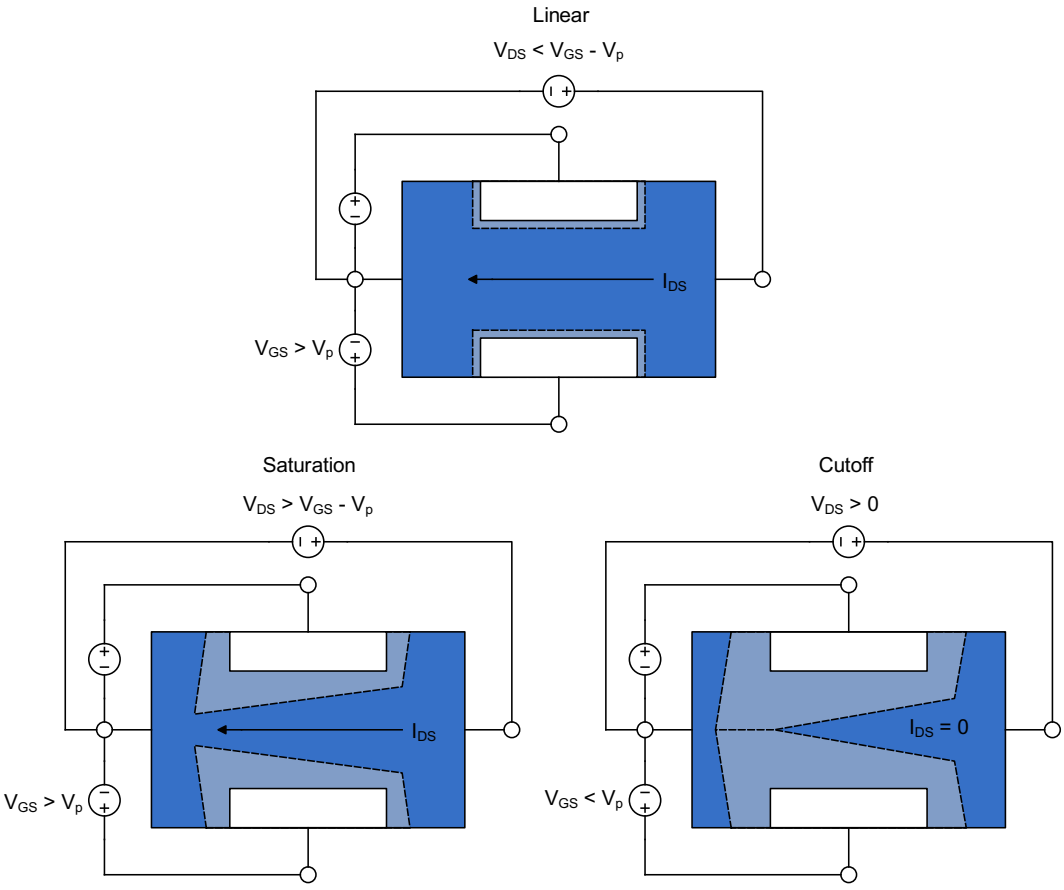


Figure 2.5: JFET operating regions based on V_{GS} and V_{DS}

Section 2.3.4. JFETs have less gate leakage than BJTs, thus giving them increased input impedance. This increased input impedance is essential for measuring small currents and creating front-end amplifiers that will work with high impedance sensors like nanopores, photodiodes, or electrochemical cells. MOSFETs require a thin silicon dioxide layer to function properly. Because JFETs are constructed without thin oxide, they are less likely to be damaged by electrostatic discharge (ESD) and ionizing radiation than MOSFETs. The simple construction of JFETs also results in less process variation and more consistent behavior across changing temperature. Finally, the relatively simple structure makes it possible to create different variants in many CMOS processes without the addition of too many additional masks or implants.

However, the diode structure and depletion mode operation of JFETs result in higher voltage requirements than BJTs or MOSFETs. The gate leakage of JFETs, while small, is not as low as MOSFET devices. This gate leakage can cause offset current that may interfere with very low current detection. JFETs also typically have lowered performance at high frequency due to the higher internal parasitic capacitances (C_{GS} and C_{GD}) resulting from larger overlap areas. Finally, JFET construction in modern technologies is not always supported or simple to implement given geometrical and process constraints.

Overall, JFETs provide advantages that are specifically helpful when designing amplifiers for detecting bioelectronic signals due to their low noise, low gate leakage, and high resistance to ESD damage. The low noise and leakage make it easier to maintain high SNR in biological measurements. Resistance to ESD damage is valuable, as the input stage for biological measurements can often be subject to static charge that results from fluid exchange and mechanical adjustment of the high impedance nodes before, during, and after the measurement.

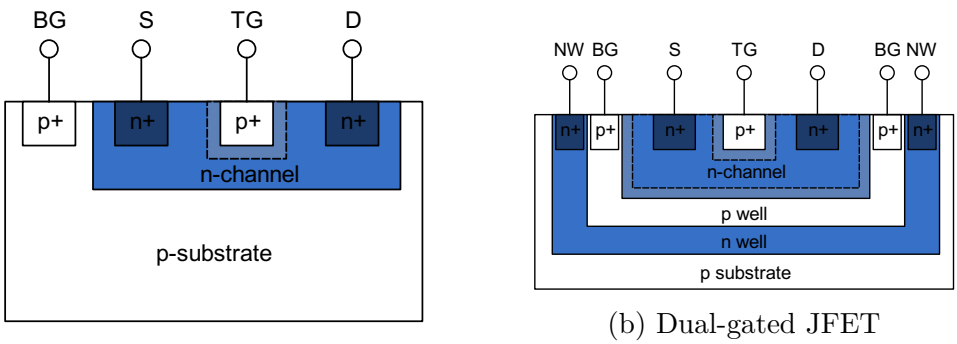
2.3.4 JFET noise

One of the primary reasons to choose JFETs over MOSFET or BJT devices is the lower noise offered by JFET circuits. JFETs have lower noise than other transistors because the JFET structure is free of silicon dioxide insulator. As discussed in Section 2.2.2, charge traps and crystal defects are responsible for $1/f$ noise in semiconductor device structures. The interface between silicon dioxide and the semiconductor channel is likely the cause of the increased flicker noise of MOSFETs. Electrons traveling in the semiconductor channel are trapped and released from defects between the oxide and silicon, resulting in variations of the device current. JFET and BJT devices have reduced flicker noise due to structures that do not require silicon dioxide. However despite the low flicker noise of BJTs, the high input current of BJTs makes them ill-suited for high gain, low offset amplifiers. JFETs thus offer the low flicker noise of a silicon dioxide free transistor along with low input current, resulting in ideal performance for as input devices for low noise TIAs.

2.3.5 JFET-CMOS devices

Once CMOS technology became the industrial focus for microelectronics, many sought to bring the advantages of JFET devices into the same process flow as MOSFETs. Combining both JFET and CMOS technologies allows for users to make low noise JFET front-end amplifiers while still being able to use the many other useful CMOS devices for later stages, digital logic, data conversion, and other circuits. The use of JFETs allows for lower noise for biological research, as well as radiation and temperature hardness for physics and space applications.

The various forms of CMOS-integrated JFET vary from dedicated hybrid-CMOS processes to creative adaptations of existing CMOS to construct radiation-hard JFETs, cryogenic JFETs, vertical JFETs, and other designs. The simplest design to construct a JFET involves creating a deep n-type implant in a p-type substrate, and then implanting a shallow p-type diffusion to form the top gate. The source and drain contacts connect to the n-type channel



(a) Top-gated JFET

(b) Dual-gated JFET

Figure 2.6: Generic n-channel JFET-CMOS devices

on either side of the top gate. The substrate itself forms the back gate for the device and in many cases must be left connected to ground for the rest of the circuit to function properly. This structure is shown in Figure 2.6a and is implemented in a CMOS process with limited additional processing steps. Many CMOS-integrated JFETs have been created using this technique [35]–[37].

A more sophisticated construction forms JFETs using the implants typically used for triple-well MOSFET devices [25], [38]. These devices are isolated from the substrate, as the bottom and top gates are constructed separately. The isolation from the substrate allows for reduced noise, and dual gate operation allows for increased gain due to channel depletion occurring from both sides of the device. A generic version of this kind of structure is shown in Figure 2.6b. Creative use of implants intended for other CMOS devices, such as ESD diodes, can also be used to construct JFETs in CMOS [34].

Adjustments to device construction and doping can also allow the use of JFETs in challenging environments including high radiation [35], [36], [39] and cyrogenic temperature [40]. MOSFET devices are non-ideal devices for use in high energy radiation environments, mostly due to the sensitivity and fragility of the thin oxide. Radiation-exposed MOSFETs can be permanently damaged and exhibit increased gate leakage from radiation induced leakage current or radiation soft breakdown as a result of oxide traps formed within the gate oxide [41]. Decreased current drive capability can also result from radiation wear out also

caused by damage to the thin oxide [41]. JFETs are resistant to radiation damage since the device structure is free of silicon oxide.

JFETs can be used at cryogenic temperatures for satellite and space applications [30] or for low temperature physics experiments [31]. Cryogenic JFETs may require increased carrier doping, since at low temperatures the carriers in the semiconductor will freeze out and be unable to jump to the conduction band [40]. Doping steps for JFET manufacture may also need to be altered to account for the creation of defects that result in increased noise at low temperature [30].

2.3.6 JFET applications

The increased availability of JFETs in CMOS processes has allowed for the creation of circuits incorporating JFETs for a variety of applications. JFET applications as preamplifiers are extremely numerous due to the low noise performance that this confers [24], [26]–[28], [31]–[33], [35], [42], [43]. JFETs are particularly well suited for physics detection applications based on the increased hardness against both ESD and radiation exposure. Cryogenic CMOS-integrated JFETs were designed to form photodiode readout circuits for the Gravity Probe B orbital telescope [30]. JFETs have been used to create preamplifiers for High-Purity Germanium detectors for the Germanium Detector Array [31], Silicon Drift Detectors (SDDs) [32], and acoustical sensing to detect Weakly-Interacting-Massive-Particles (WIMPs) in dark matter bubble detectors [33]. Several instrumentation amplifiers for low-noise sensor recording have been designed using JFET inputs [24], [26], [27], [44] Monolithically integrated phototransistors were also created using JFETs constructed from doped silicon nanowires [29]. The JFET structure can be used to construct useful electronic amplifiers and devices for a variety of scientific measurement applications.

2.4 Electrochemistry

Electrochemistry is a powerful branch of chemistry involving the measurement of electrical signals from chemical compounds. Since the discovery of the electroanalytical method in 1922 [45], this technique has been used in thousands of different experiemental measurements. Reduction/oxidation (redox) reactions occur when a chemical compound accepts electrons (reduction) or donates electrons (oxidation). Two redox half reactions between metal electrodes and corresponding ions in solution can be used to create a circuit called an electrochemical cell which exchanges electrical energy and chemical energy. If one half reaction is replaced by a well known reference reaction, the other half reaction can be studied by applying potential between the two electrodes. Applied potential is able to force the reaction towards reduction or oxidation by encouraging transfer of electrons in that direction.

$$\mathrm{O} + \mathrm{e}^{-} \underset{\mathrm{k_b}}{\overset{\mathrm{k_f}}{\rightleftharpoons}} \mathrm{R} \tag{2.15}$$

When the forward (k_f) and reverse (k_b) reaction rates are equal, the reaction has reached the standard redox potential $E^{0'}$, which is specific to the redox reaction.

In the most basic electrochemistry experiment, three electrodes are used in concert to apply voltage and measure current from the fluid substrate of interest. A working electrode consists of an inert metal, typically gold or platinum, and this is used to collect or deposit the electrons involved in the redox reaction. To apply the potential to the solution and thus to the substrate, a reference electrode with a known half cell reaction is used, typically consisting of a platimum wire or mesh. Finally, an auxiliary or counter electrode is used to flow the current necessary for the reaction, which consists of a silver wire with silver cloride coating that maintains a low resistance connection to the solution.

2.4.1 Step voltammetry

To measure the current from a redox substrate, a variable waveform is applied between the reference electrode and the working electrode. The simplest stimulation is to simply jump the voltage from an extreme reducing potential across the redox potential $E^{0'}$ to an extreme oxidizing potential. In this way, all of the substrate should be converted to the oxidized state, and thereby gives up all of the electrons in the redox reaction as current.

$$\mathrm{O} + \mathrm{ne}^- \rightleftharpoons \mathrm{R} \tag{2.16}$$

The application of a step potential can be characterized through the use of the diffusion equation, while applying some basic assumptions about the conditions of the reaction vessel [46]:

- that there is an infinite supply of the oxidized state of the substrate and that the concentration of the bulk solution is not affected by the reaction taking place [46].
- that the application of the step potential instantly converts the substrate near the electrode to the reduced state, making the surface concentration of oxidized species go to zero [46].
- that the redox reaction is an n-electron reaction that is fully reversible [46].
- that the solution remains unstirred during the reaction [46].

With these conditions, the current at time t after the step can be derived from the Diffusion equation using the Laplace transform and with the above as boundary conditions, resulting in the Cottrell equation

$$i_d(t) = \frac{nFAD_O^{1/2}C_O^*}{\pi^{1/2}t^{1/2}} \tag{2.17}$$

where n is the number of electrons in the reaction, F is Faraday's constant, A is the electrode area, D_O is the diffusion coefficient of the oxidized species, and C_O^* is the initial concentration of the oxidized species [46]. The Cottrell equation shows that the current measured will be initially very high, but will then rapidly decay with time. The initial high current occurs as the substrate near the electrode is reduced, but decreases as more solution becomes depleted of oxidizable substrate. The current is therefore limited by the diffusion of substrate within the concentration gradient. The region of solution impacted by the concentration gradient is called the diffusion layer. The thickness of the diffusion layer is typically given by

$$\delta = 2\sqrt{D_O t} \tag{2.18}$$

which encompasses a region near the electrode where 84 % of the diffusion process is contained [46]. In the bulk region outside of the diffusion layer, the diffusion process has little impact on the substrate concentration.

However, the diffusion process is altered when the depth of the diffusion layer δ becomes large when compared to the size of the electrode. When using electrodes of small dimension, often referred to as ultramicroelectrodes (UMEs), the linear diffusion expected at a planar electrode is modified due to the small electrode geometry [46]. The solution to the diffusion equation for semi-infinite spherical diffusion is [46]

$$\begin{aligned} i_d(t) &= nFAD_O^{1/2}C_O^* \left[\frac{1}{\pi^{1/2} D_O t^{1/2}} + \frac{D_O^{1/2}}{r_0} \right] \\ i_d(t) &= \underbrace{\frac{nFAD_O^{1/2}C_O^*}{\pi^{1/2} t^{1/2}}}_{\text{planar}} + \underbrace{\frac{nFAD_O C_O^*}{r_0}}_{\text{geom. correction}} \end{aligned} \tag{2.19}$$

This equation consists of a term representing the Cottrell current and a term caused by the geometrical edge effects. When measuring redox current with a UME, the Cottrell term dominates at very short time scales, but the diffusion layer quickly grows larger than the electrode. The geometrical edge effects dominate under these conditions and result in a

steady-state current that is constant with time. This steady-state current depends on the geometry of the UME and has the form:

$$i_{ss} = nFAm_O C_O^* \tag{2.20}$$

where m_O is the geometry-dependent mass transfer coefficient [46]. The mass transfer coefficient m_O is D_O/r_0 for a sphere or hemisphere and $4D_O/(\pi r_0)$ for a disk [46]. Therefore the steady-state current for a disk microelectrode is [46]

$$i_{ss} = 4nFD_O C_O^* r_0 \tag{2.21}$$

At short t when the diffusion layer remains very small, the current at a UME is identical to the Cottrell current at a macroelectrode, but at long t, the current for a UME will converge to the steady-state value for as long as sufficient oxidizable substrate remains [46]. The all-region equation for step voltammetry at a disk UME has been derived by Shoup and Szabo as

$$i(\tau) = i_{ss}\left(\frac{\pi}{4} + \sqrt{\frac{\pi}{4}}\tau^{-1/2} + \left(1 - \frac{\pi}{4}\right)e^{-0.7823\tau^{-1/2}}\right) \tag{2.22}$$

where $\tau = 4D_O t/r_0^2$ is normalized time such that $\tau = 1$ when the diffusion layer and electrode radius are the same [47].

2.4.2 Sampled voltammograms

While step voltammetry can be used as one of the simplest methods of extracting redox current from a substrate, more sophisticated measurements allow for more control of the system and easier identification of the redox parameters. Additionally, while step voltammetry provides some information about the redox current I_p, it does not reveal the value of the redox potential $E^{0'}$. In order to receive more information about the transistion voltage,

an alteration to the step voltammetry procedure can be used. Rather than stepping the potential all the way above the redox potential to a much higher voltage, the potential can be stepped to an intermediate value. In doing so, the voltage can be repeatedly pulsed from a low voltage to different final values, producing a sampled-current voltammogram. This produces a modified version of the Cottrell equation:

$$i(t) = \frac{i_d(t)}{1 + \xi\theta} \tag{2.23}$$

where $\xi = \sqrt{D_O/D_R}$ and $\theta = C_O(0,t)/C_R(0,t) = \exp\left[nF(E - E^{0'})/(RT)\right]$ [46]. The result is a waveform that varies between 0 and $i_d(t)$ depending on the concentration of oxidized versus reduced species that remains and the ratio of their diffusion coefficients.

These equations are again modified when using a UME, though the main difference in this case is that the waveform depends on the ratio of the diffusion coefficients, rather than the square-root of that ratio, with current given by [46]

$$i = \frac{i_d}{1 + \xi^2\theta} \tag{2.24}$$

2.4.3 Cyclic Voltammetry

Sampled voltammograms provide valuable information, but remain cumbersome, requiring multiple measurements for each voltammogram. In linear sweep voltammetry, a simple ramp potential is applied while measuring the current. Replacing the voltage step by a voltage ramp with a waveform of

$$E(t) = E_i - vt \tag{2.25}$$

when applied to the diffusion equation results in a redox current

$$\int_0^t i(\tau)(t-\tau)^{-1/2}d\tau = \frac{nFA\pi^{1/2}D_O^{1/2}C_O^*}{[\theta S(t)\xi + 1]} \tag{2.26}$$

which unfortunately is not easily invertable [46]. When the geometrical constraints of UMEs are also included, the equation can be evalulated computationally and given as

$$i = \underbrace{nFAC_O^*(\pi D_O\sigma)^{1/2}\chi(\sigma t)}_{\text{planar}} + \underbrace{nFAm_OC_O^*\phi(\sigma t)}_{\text{geom. correction}} \tag{2.27}$$

where the normalized sweep rate σ is given by $nFv/(RT)$, and $\chi(\sigma t)$ and $\phi(\sigma t)$ are tabulated functions [46]. This equation has two components, one consisting of the planar response for a macroelectrode and one containing the geometrical correction factor, similar to (2.19) [46]. It can be shown from the above equation that the boundary between the two behaviors is roughly governed by

$$\pi D_O\sigma = m_O^2 \tag{2.28}$$

For a typical sweep rate of 100 mV/s for linear sweep voltammetry at a hemispherical electrode, the boundary between macroelectrode and UME is $r_0 = 48\,\mu\text{m}$ [46]. For a disk electrode, the boundary is slightly higher at $r_0 = 61\,\mu\text{m}$ due to the larger value of $m_O = 4D_O/(\pi r_0)$ [46]. Figure 2.7 shows the linear sweep voltammogram that results from (2.27) for a macroelectrode of radius 0.8 mm, using parameters for potassium ferrocyanide/ferricyanide from Konopka, et al. [48]. This figure shows that the current increases to a peak level and then decays after surpassing the redox potential, due to the depletion of oxidizable molecules near the surface of the electrode and flux being limited by the mass transfer of the same molecules to the vicinity of the electrode. Figure 2.8 shows the waveforms that result for a microelectrode of radius 15 µm. Here, the geometrical correction current ($i_d\phi(\sigma t)$) dominates and the current remains relatively steady after passing $E^{0'}$ due

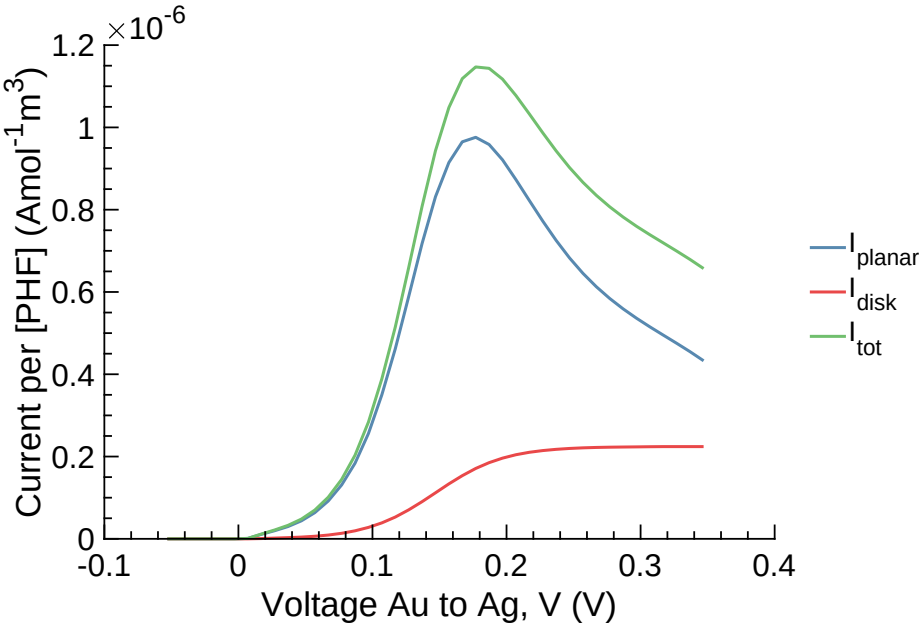


Figure 2.7: Linear sweep voltammetry of a theoretical 0.8 mm radius macroelectrode

to the small dimensions of the electrode relative to the thickness of the diffusion layer [46].

Cyclic voltammetry (CV) involves the repeated upwards and downwards sweeps of a ramp or staircase waveform, resulting in a complete voltammogram covering reducing and oxidizing potentials. The overall shape of the voltammogram for a macroelectrode thus becomes a double peaked shape where one peak indicates the oxidation process and one indicates the reduction. The peak locations E_p are shifted slightly to either side of the redox potential $E^{0'}$.

For CV at a UME, the voltammogram retraces with close to the original current when travelling between oxidized and reduced states, making the overall voltammogram a sigmoid shape. The peak current I_p can be seen from the maximal difference between the reduced and oxidized plateaus, and the half-wave potential $E_{1/2}$ indicates the location of the redox potential. This information can thus be used to identify the electroactive species by its redox potential, and the redox current can be used to determine the concentration of the reacting substrate.

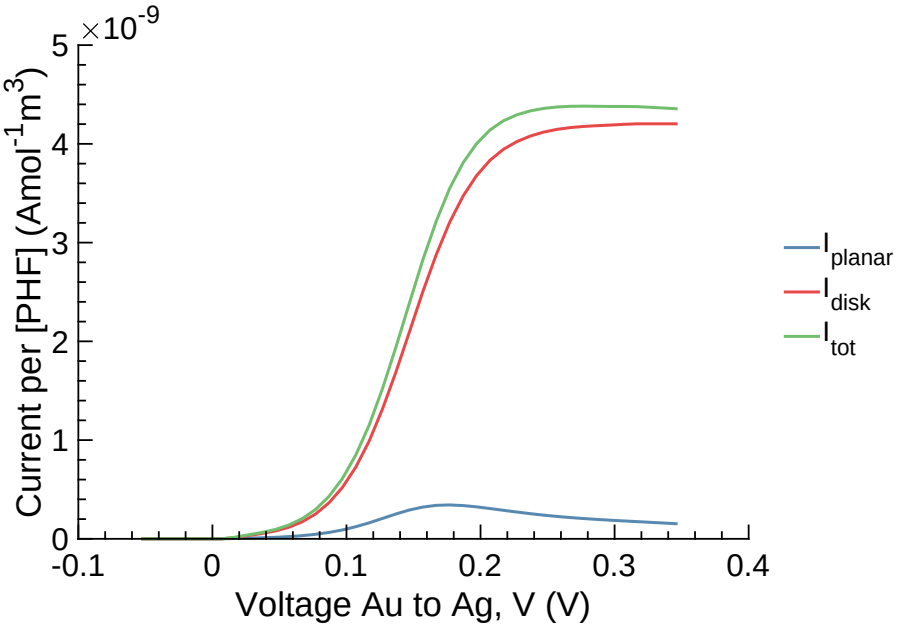


Figure 2.8: Linear sweep voltammetry of a theoretical 15 µm radius UME

2.4.4 Square-wave voltammetry

Square-wave voltammetry (SWV) is a more sophisticated electrochemistry method that helps to improve on one of the more challenging problems with cyclic voltammetry, charging current. SWV helps to separate the signal current created by the redox substrate from the capacitive charging current which is caused by the changing applied voltage across the electrode capacitance [49]. As potential steps are applied to the electrochemical cell, capacitive parasitics result in large spikes of current passing through at the same time as the signal current. These currents can be settled by the potentiostat, but charging current becomes worse at higher sweep rates and can obscure small signals. Instead when using SWV, the voltage alternates between stepping up and down, and the two current values are sampled and subtracted at the end of each alternating set of steps [49]. This results in the charging current from the transitions cancelling out, while the signal current of the redox molecules is unaffected [49]. A diagram showing the different voltage waveforms for CV, SWV, and step voltammetry is pictured in Figure 2.9.

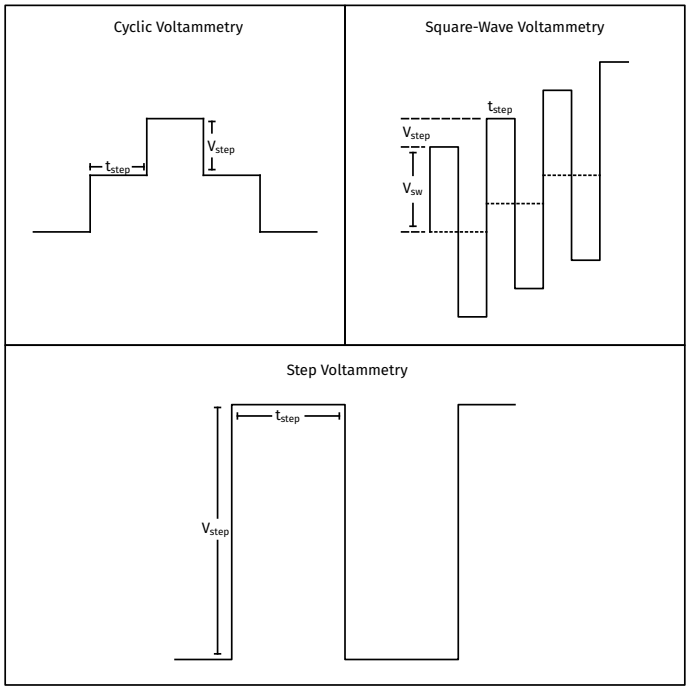


Figure 2.9: Voltammetry waveforms for CV, SWV and step voltammetry

2.4.5 Electrochemical equivalent circuits

To better understand the behavior of redox reactions, it is helpful to have a physical model for the chemical and molecular interactions that occur. The physical model can then be expressed as an equivalent electronic circuit, which will make it possible to simulate the electrical effects of reactions occurring on the working electrode. This section will provide a brief overview of the physical processes occurring at electrode-electrolyte interfaces and how this relates to electrical measurements of redox reactions.

Electrical double layer

The first models of electrode-electrolyte interfaces were constructed by studying the case of a non-conductive metal electrode in ionic solution exposed to an electrical field. Helmholtz first considered the charge separation occurring at this kind of interface [46]. Since the lack of electric fields inside a metal indicates that all excess charge must reside at the surface, Helmholtz proposed that a counter charge in solution would form a similar thin layer [46].

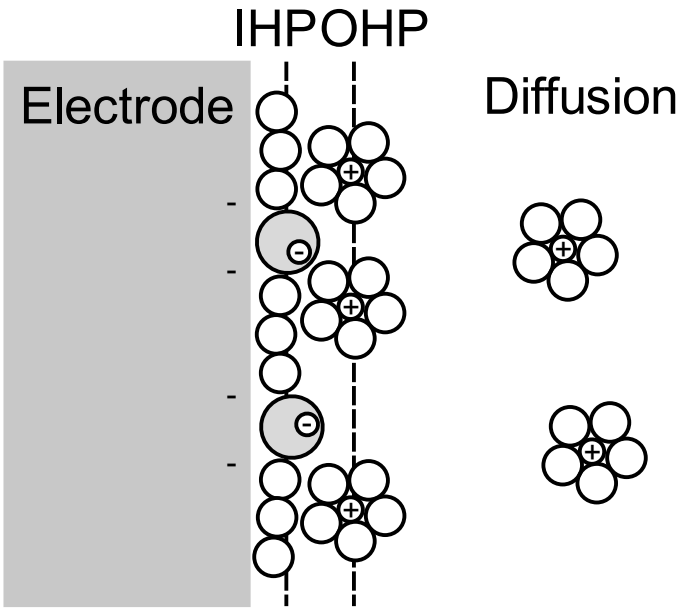


Figure 2.10: Guay-Chapman-Sterm model of electrical double layer, adapted from Bard and Faulkner [46, Figure 1.2.3]

This model of two layers of charge separated by a molecular distance resulted in the term double layer, which is now used generically to refer to the charge separation at electrode-electrolyte interfaces [46].

This basic model provides some insight into the separation of charge at the interface, but more accurate description of the electrode-electrolyte interface requires a more involved model. In the Gouy-Chapman-Stern (GCS) model, the ionic solution near the electrode surface forms into two distinct regions: the compact layer and the diffuse layer [46]. A schematic diagram of the GCS model adapted from [46] is shown in Figure 2.10. The compact, or fixed, layer is formed from ions and water specifically absorbed to the surface and solvated ions that are strongly attracted to the metal surface and approach as close as possible [46]. The absorbed ions sit at a distance called the inner Helmholtz plane and the solvated ions are positioned at the outer Helmholtz plane [46]. Changing potential and electrolyte concentration have little effect on the ion of the compact layer due to the tight attraction of the ions to the metal surface [46]. The diffuse layer is formed of charges which are electrostatically attracted to the interface, while simultaneously being pushed away by

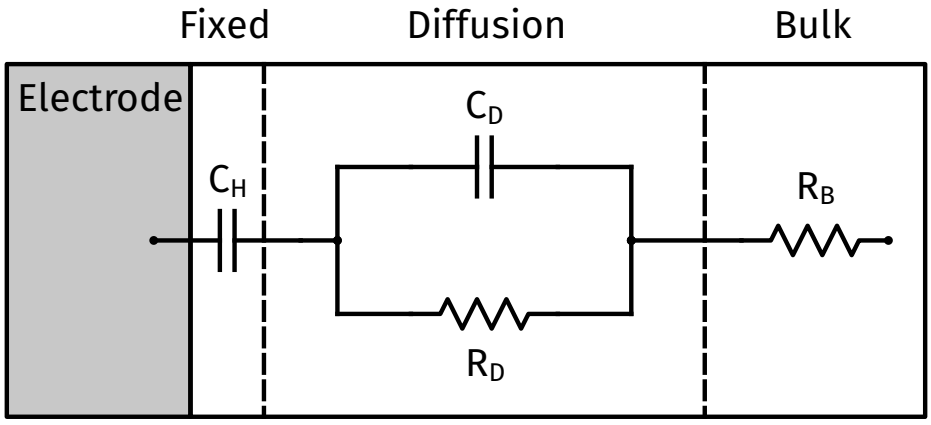


Figure 2.11: Ideal polarized electrode (IPE) equivalent circuit model

the thermal processes of diffusion [46]. Therefore, potential and electrolyte concentration have a large effect on the molecules of the diffuse layer [46]. This model of the double layer behavior can be used to construct equivalent circuit models for both non-Faradaic electrodes, also called ideal polarized electrodes (IPEs), and Faradaic electrodes exposed to redox molecules.

Ideal polarized electrode

The IPE represents static conditions at the electrode-electrolyte interface in the absence of any redox exchange and is therefore representative of the GCS model. A schematic of the IPE model is shown in Figure 2.11. The IPE model has capacitances C_H, which originates from the charge separation of the compact layer, and C_D, which represents the charge separation of the diffuse layer. In addition, the IPE model has R_b (sometimes called R_Ω), which represents the resistance of the bulk solution, and R_D, a resistance in parallel with C_D, which represents the resistance of the mobile charges of the diffuse layer [50].

Randles equivalent circuit

With the inclusion of redox substrates in the solution, the equivalent circuit model changes to the Randles model, shown in Figure 2.12. The Randles model represents the redox current through two impedances: the charge transfer resistance R_{ct} and the Warburg

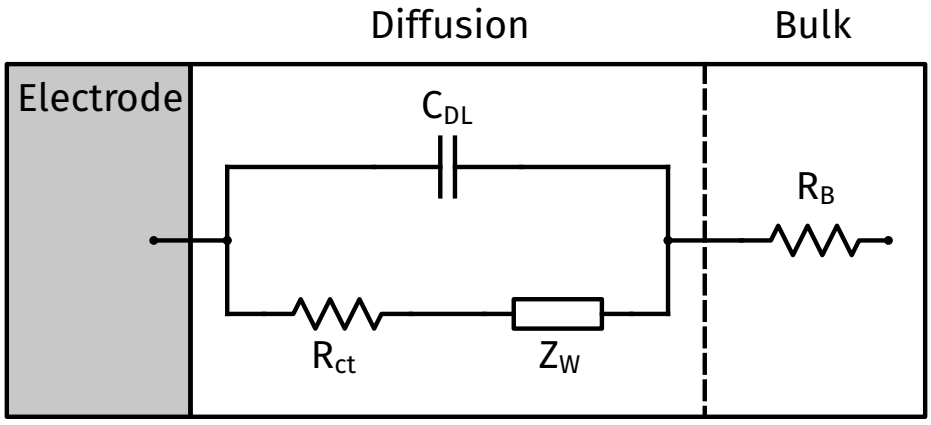


Figure 2.12: Randles equivalent circuit model

impedance Z_W. The charge transfer resistance represents the real portion of the redox current, while the Warburg impedance represents how the current changes with frequency. C_{DL} represents the capacitance of the diffuse layer and the resistance of the bulk R_b remains the same.

Electrochemical impedance spectroscopy

The component values for the electrochemical models shown in Figures 2.11 and 2.12 can be determined through direct measurement of the desired electrochemical system. Electrochemical impedance spectroscopy (EIS) is a technique to measure the impedance response of electrochemical cells over frequency. A potentiostat generates a small AC voltage signal which is applied to the electrochemical cell, and the AC current is simultaneously measured and used to determine the magnitude and phase of the cell impedance. The frequency of the stimulus voltage is then varied, so that the impedance can be measured across a broad range of frequency values. The resulting impedance data can be mathematically fit to a desired circuit model to determine the appropriate values of the model components. These models can then be used for circuit simulation that includes the impact of the electrochemical cell.

2.4.6 Electrochemical measurements

Modern voltammetry originated with the discovery of the electroanalytical method and polarography using a dropping mercury electrode by Jaroslav Heyrovský in 1922 [45]. In 1941, Archie Hickling created the first potentiostat and used it to perform automatic electrochemical characterization of chemical analytes [51]. The voltammetry field continued to develop through the 1970s and 1980s, due to improved analog and digital measurement electronics, and electrode microfabrication techniques. Since these early times, many new technologies take advantage of the sensing capabilities of electrochemistry. Miniaturized arrays of electrochemical amplifiers have been created using CMOS processes, and modern amplifiers can be designed for very low current detection. Electrochemical sensing capabilities have been improved through advances in electrode fabrication, miniaturization, and functionalization. Unique voltage scanning and data processing techniques have increased the sensitivity and variety of electrochemical data. Alternative measurement techniques have also emerged which provide unique sensing capabilities including scanning electrochemical microscopy (SECM), scanning ion-conductance microscopy (SICM), ion sensitive field-effect transistor (ISFET) sensing, electrochemical impedance spectroscopy (EIS), and redox cycling. Electrochemical measurement propels exploration of many chemical and biological systems.

Electrochemical arrays

Scaling down electrochemical measurement systems through the use of photolithography and CMOS fabrication provides benefits and challenges. The smaller size of CMOS circuits can result in smaller parasitic capacitances and resistances when connecting sensors to electronics, while increasing the number of simultaneous measurement channels. The CMOS electronics can also improve the speed of circuit operation and reduce the power consumption. The size restrictions required for creating multichannel circuits also provide challenges when trying to match or exceed the performance of large discrete electronics. Integrated cir-

cuits designed for electrochemical and other measurement assays with hundreds or thousands of channels are identified as Lab-on-a-chip (LOC) circuits.

The ideal LOC design incorporates several types of sensors and amplifiers in a self-contained design capable of fluidic measurements, while being cheap enough to be disposable or reusable for rapid, high throughput measurements of biological samples. Existing LOC systems can perform several measurements, including EIS, voltammetry, amperometry, and ion-sensing [52]. Some LOC circuits construct the electrodes and microfluidics monolithically with the electronics [53], while other connect the electrodes externally [54]. Co-fabrication results in more compact product, but electrodes can become fouled or contaminated, resulting in wasted chips. A first design incorporating potentiostats, UMEs, data conversion, heating coils, temperature sensors, and a fluidic chamber has been fabricated [53], illustrating the possibilities for fast, portable electrochemical analysis.

Femtoampere electrochemistry

Pushing the limits of electrochemical detection involves exploring very low concentrations of target molecules and therefore very small signal currents. EIS experiments on nanoelectrodes with 1 µm and 100 nm diameters were performed using an amplifier providing 1×10^{11} V/A gain [9]. Lebegue, et al. detected collisions of ferrocyanide-containing vesicles Pt electrodes that resulted in current spikes of 600 fA to 1000 fA [55]. Advancements of electrode performance involves new techniques of microelectrode and nanoelectrode fabrication. Many experiments to detect nanomolar concentrations of electrochemical substrates utilize electrodes functionalized by various chemicals and compounds to increase sensitivity. Nanomolar detection has been performed on electrodes functionalized by enzymatic biosensors [56], silver nanoparticles [57], carbon nanotubes [58], or large arrays of nanoelectrodes [59]. Glasscott, et al. detected very low numbers of silver nanoparticles in solution by measuring tiny droplets with radius 700 nm to increase the concentration [60]. Elkhawaga, et al. used gold nanoparticle and polyaniline modified electrodes to measure pyocyanin [61].

Electrochemical sensors

Electrochemical measurements are used to detect and discriminate a wide variety of chemical compounds. Various experiments have measured drugs, DNA, toxins, neurotransmitters, proteins, metals, and other biological and chemical compounds. Electrochemical measurements often target specific chemical or biological substrates, such as phenazines [61]–[69], DNA/nucleic acids [70], [71], dopamine [72]–[75], hydrogen peroxide [76], nitrates [57], methamphetamine [77], ferri/ferrocyanide [78], [79], clindamycin [80], ferrocene [81], proteins [82], vesicles [55], and platinum nanoparticles [60].

New electrochemistry techniques have also enabled novel measurements, including SECM [59], [83], [84], EIS [9], [85]–[87], and redox cycling [88]–[90]. Scanning electrochemical microscopy, or SECM, is a technique used to detect electrochemical activity across a large area. A quasi-reference microelectrode acting as both reference and counter electrode is suspended above the sample of interest and connected to a computer controlled stage to enable scanning across the sample while recording redox current from the tip. This allows for electrochemical mapping of a liquid-liquid, liquid-solid, or liquid-gas interface with high resolutions.

Electrochemical impedance spectroscopy (EIS) was addressed previously in Section 2.4.5. EIS is frequently performed using potentiostat circuits in order to characterize electrochemical impedances for analysis of electrochemical reactions. This often is combined with electrochemistry to improve understanding of the circuit at high frequency. EIS will be used in Chapter 5 for analysis of electrochemical noise.

Redox cycling is a technique of employing two metal electrodes constructed within a confined volume, one held at an oxidizing voltage and one at a reducing voltage for a particular redox substrate. If the substrate has a fast reversible redox reaction, the molecules can be repeatedly oxidized and reduced in a short span of time, greatly amplifying the amount of current that can be generated from a single molecule [88]. Microfabricated nanogaps, nanocavities, or nanopores can employ redox cycling to measure single molecules for high sensitivity chemical detection [90].

Related fields have also benefit from new knowledge about liquid-solid interfaces, such as ion-sensitive field-effect transistors (ISFETs) [91]–[95]. ISFETs are MOSFET devices constructed without gate metalization. Rather than use a metal gate for electronic control, the gate oxide is connected directly to ionic solution. ISFETs thus act as capacitive electrochemical sensors capable of sensitive detection of electrical charges. One typical use of ISFETs for pH measurement by sensing the charge of H^+ ions in solution. ISFETs were famously used as pH sensors for base calling in a massively-multiplexed CMOS DNA pyrosequencing system [96]. The electrochemistry sensing has enabled substantial scientific progress across numerous fields, and has made particular waves in biological fields by providing interfaces for electrically connecting to living systems.

2.5 Electrochemical noise

The similarity between the motion of charged ions in solution and the motion of electrons in electronic circuits has enabled modeling of the electrochemical circuit using standard electronic components. However, the Randles and IPE equivalent circuit models (Figures 2.11 and 2.12) do not include the noise of the electrode-electrolyte interface. As electrochemical interface noise strongly impacts the limits of detection for electroanalytical systems, it has been the target of several analytical efforts [50], [97]–[99]. Analysis of the electrode-electrolyte interface noise relies on fundamental electrochemistry equations with the addition of Poisson and Langevin noise sources [50], [99]. This analysis results in a model describing the electrochemical noise of the interface which can be aligned with the Randles and IPE equivalent circuits presented previously [50], [99].

The IPE model enhanced with the addition of electrochemical noise contributions is shown in Figure 2.13 [50]. The basic IPE model has current noise contributions from both the diffusion resistor R_D and the bulk resistor R_b, which introduce noise similar to a typical resistor as a result of the thermal motions of ions in the solution [50], [99]. These resistors

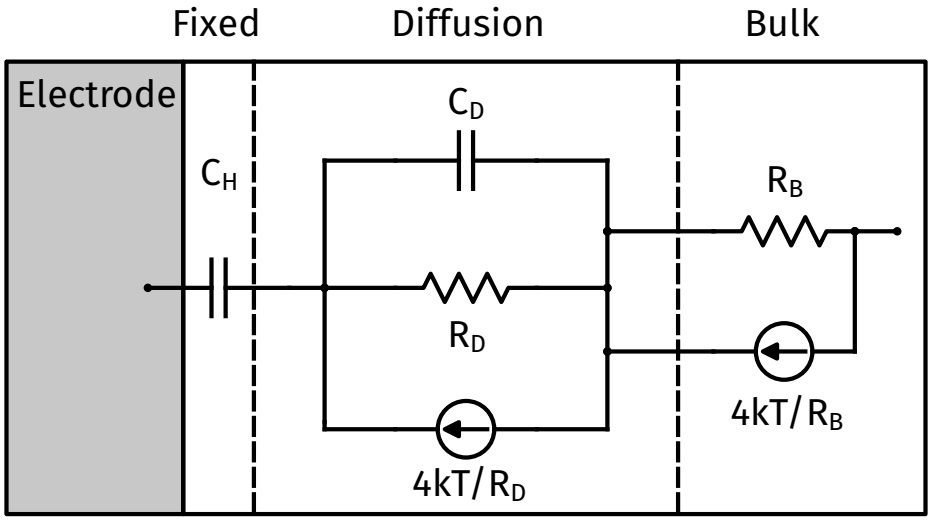


Figure 2.13: IPE electrochemical equivalent circuit with noise contributions, figure adapted from Hassibi, et al. [50]

each contribute a current noise with noise PSD of

$$S_n(f) = 4k_BT/R \tag{2.29}$$

as a result of thermal motion [50].

The Randles model including electrochemical noise is shown in Figure 2.14 [50]. The electrochemical noise for the redox conductive electrode is not simply the result of thermal motions of the ions. At low frequencies, a potential barrier exists between the metal electrode and the ionic solution, which results in shot noise with spectrum

$$S_n(f) = 2nqi_T \tag{2.30}$$

where n is the electrical charge of each carrier and i_T represents the total redox current [50]. The high frequency noise at a Faradaic electrode is given by

$$S_n(f) = 2nqi_T \cdot K(\omega) \tag{2.31}$$

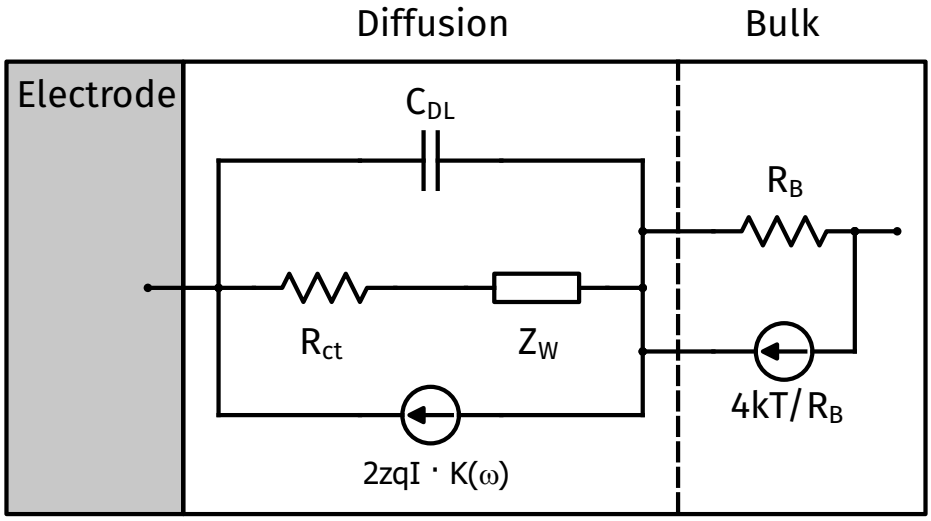


Figure 2.14: Randles electrochemical model with noise contributions, figure adapted from Hassibi, et al. [50]

where the function $K(\omega)$ depends on the dominant transport phenomenon [50]. Therefore, the overall noise spectrum has a shot noise plateau at low frequency that falls off at high frequency with a slope which is determined by the transport phenomenon [50]. Drift dominated electrodes experience noise that scales with f^{-2} at high frequency, while diffusion dominated electrodes have $K(\omega)$ that scales with f^{-1} [50].

Electrochemical interface noise analysis has been used in studies of corrosion, voltammetry, single-molecule kinetics, ISFETs, and biomedical interfaces. Many have studied the electrochemical noise of corrosion, and the impact of crystal structures, surface coatings, and oxides on corrosion noise [100]–[107]. Corrosion is a galvanic electrochemical reaction, where metals exposed to electrolyte undergo oxidation reactions spontaneously. Corrosion studies often use a device called a zero resistance ammeter (ZRA) to record electrochemical signals of corrosion [105], [108]. The physical phenomena of corrosion, such as pitting, inhibition or uniform corrosion, can be observed in electrochemical noise measurements [102], [109], [110]. In redox reactions, the working electrode is a noble metal which typically will not exhibit any corrosion current.

The implications of electrochemical noise for voltammetry or amperometry have only

attracted limited interest. A few measurements to validate the theoretical derivations of electrochemical noise have been performed [79], [99], [111]–[114]. Other have pursued applications of electrochemical noise to perform or enhance chemical assays [79], [85], [86], [115]–[118]. Very few have attempted to reduce electrochemical noise, although a recent work presents a technique for reducing the impact of the capacitance of the electrical double layer C_{DL} for chronoamperometry measurements [119].

2.6 Summary

The electroanalytical method is a powerful technique for interrogating a wide variety of chemical compounds. The combination of electrochemical techniques with the powers of modern CMOS circuit design has expanded measurement capabilities, while opening up broad new fields of study. The improvements provided by CMOS circuitry come at a cost of added complexity, however, with more considerations needed for integration with chemical and biological sensors, such as noise levels. In particular, the low-noise design of CMOS amplifiers for sensor interfaces extends the detection capabilities to smaller current regimes. The capabilities of low-noise electronic amplifiers have enabled electrochemical sensing of proteins, DNA, bacteria, nanoparticles, drugs, and many other small molecules. These incredible measurements relied upon the development of improved sensors, transistors, and amplifiers, and designs capable of low-noise performance.

Although electrochemical processes are involved in countless bioelectronic measurements, few studies have attempted to examine in detail the electrochemical noise involved in these processes. This work attempts to stretch the limits of low-noise detection by improving the CMOS measurement electronics through improved JFET transistors and carefully designed, compact circuits, while also striving to understand the fundamental behavior and limitations of electrochemical noise through extremely low-noise redox measurements.

Chapter 3: Design of Low-noise CMOS-Integrated JFETs

3.1 Introduction

Biosensors produce small magnitude signals which require amplification to elevate the signal above electronic and systemic random noise. Most low-noise front-ends are constructed from operational transconductance amplifiers (OTAs) configured for voltage or current sensing. For many measurement systems, these amplifiers are large rack mounted instruments with discrete electronics to achieve maximal performance. These commercial amplifiers often use discrete junction field effect transistors (JFETs) in their front-end amplifiers to reduce noise, as these devices have superior flicker noise performance when compared to MOSFETs. However, many applications demand increased channel count and decreased electronic size to more closely fit the size of the measured system, be it neurons, cells, proteins, or other biomolecules.

The push towards compact sensing electronics has required circuit designers to take advantage of CMOS technology to the utmost. MOSFET scaling is limited for these applications by noise, as the smaller a MOSFET becomes, the worse the noise performance gets. As the electrical current is averaged over a smaller area, the deviation of the current will increase. Scaling up the MOSFET size will decrease noise, but consumes more power, takes up more area, and presents greater input capacitance, which can impact the high frequency circuit performance and noise. Large input capacitance will also result in more voltage division for voltage sensing amplifiers.

Many efforts have been made to include JFET devices in CMOS to take advantage of the improved noise performance including both CMOS only and BiCMOS processes. Heavily scaled CMOS typically has few implants or additional masks to spare for constructing JFET

devices. For many other CMOS-compatible JFET (CMOS-JFET) devices, shallow trench isolation (STI) or LOCOS (Local Oxidation of Silicon) are used to construct the device and isolate the contacts for better breakdown performance or structural purposes. However, the use of this silicon dioxide in the device structure compromises noise performance due to the introduction of surface interfaces that create charge traps. Many of these devices thus do not provide the increased noise performance hoped for from CMOS-JFET devices.

The limitations of both MOSFET and prior CMOS-JFET devices were targeted through the design of low noise and compact CMOS-JFETs to enable microscale CMOS-integrated amplifiers for biosensing applications. An IBM 0.18 µm CMOS process supporting an n-channel JFET using STI for isolation was used to create a CMOS-JFET device free of STI with no changes to existing masks or implants. These devices were characterized for circuit behavior and noise performance, then used to construct a JFET-input CMOS-integrated transimpedance amplifier for low-noise measurements.

3.2 IBM JFETJC

The custom oxide-free JFET design was based on a CMOS-JFET with STI-isolation called JFETJC [25]. JFETJC is constructed using additional JFET-specific implants and implants typically used to create triple-well NFETs. The JFETJC structure pictured in Figure 3.1a allows for the device to be constructed with bottom gate separated from the silicon substrate. The device uses two additional mask levels to define the JFET structure: PI, which defines the bottom n-well isolation, and JC, which defines the n-type channel and p-type bottom gate. Unfortunately due to the particular construction of the device in this CMOS technology, the bottom and top gates are intrinsically shorted, so only one gate contact controls both top and bottom gate.

The JFETJC was designed to target RF and high-voltage operation with diode breakdown above 8 V. However, JFETJC has STI in direct contact with the conducting channel of the device [25]. This results in the JFETJC having noise performance more than ten

times worse than comparable MOSFET devices.

3.3 Custom JFET designs

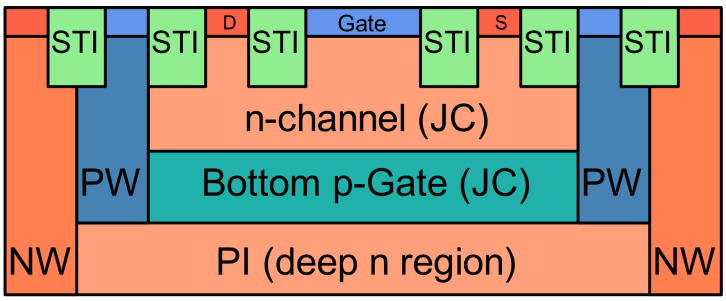
Variants on the JFETJC structure were developed in order to improve the low-noise properties. The principal objective was to remove as much STI from the vicinity of the conductive channel of the JFET, since the oxide-channel interface contains many charge traps known to cause flicker noise. Several different isolation tactics were used to create devices without STI that still operated at high frequency with high breakdown voltage like JFETJC.

The JFETPC was created by replacing the STI region with polysilicon (PC) to separate source, drain and gate. JFETOP was created by using resistor material (OP) to isolate the device regions. JFETBP2 was created by combining OP material with the OPBP2 layer, a mask typically used for Schottky diodes, which was used to block the n+ and p+ implants to reduce substrate doping. For comparison, stock JFETJC, NFET and PFET devices were also created. The stock JFETJC was created with minimum channel length $L = 400\,\text{nm}$, while a long channel version (JFETOM) was created with channel length $L = 1\,\mu\text{m}$.

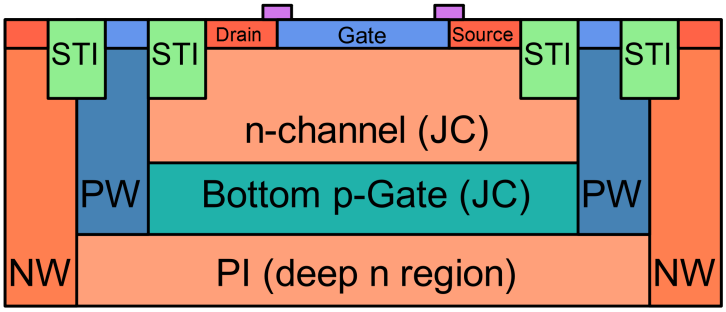
Two additional JFET variants were created in efforts to separate the back and top gates to create a four-terminal JFET. During testing, it was found that the polysilicon (PC) isolation preserved the original function of the JFETJC, while having reduced flicker noise when compared to both the original JFETJC and the NFET devices, the results of this measurement will be shown in Section 3.4.3. This device (JFETLN) worked as an upgraded version of the original JFETJC with similar circuit performance and improved noise performance.

JFETLN uses polysilicon (PC) as a blocking layer to replace the STI, which also breaks the silicide between the n-channel and top gate, as shown in Figure 3.1b. The polysilicon is electrically unused and is left floating, acting only to increase lateral isolation between top gate and channel diffusion regions.

Several geometric variants were created including a waffle-style JFETLN, as shown in



(a) Device structure of JFETJC n-channel JFET in CMOS

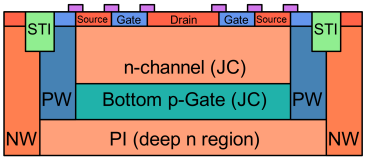


(b) Device structure of JFETLN transistor with polysilicon (PC, purple) blocking layer

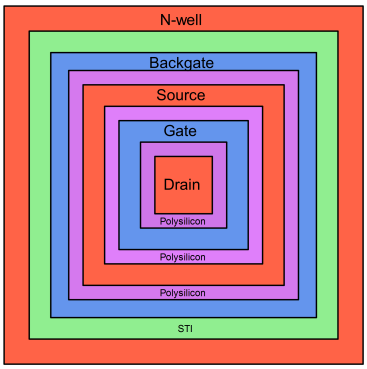
Figure 3.1: Device structures for JFETJC and JFETLN transistors © 2018 IEEE

Figures 3.2a and 3.2b. This JFET has a small drain, surrounded by gate and source. The smaller sized drain increases device switching speed through reduction of the drain capacitance. The waffle structure also allows for the design of well-matched layouts of multiple transistors with a shared source and individual drains. Additionally, the waffle structure has separate back and top gates, while also totally eliminating STI from all parts of the design.

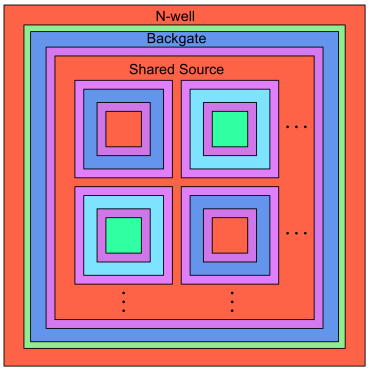
Figure 3.2c shows interdigitated waffle JFETLN devices used as a differential pair. This structure improves resistance to process variation through natural common centroid layout and simple patterning of dummy devices. This compact layout is useful for large balanced circuits including fully differential [26] or double differential designs [120], and for offset sensitive applications which rely on small signal detection.



(a) Front view of waffle JFETLN



(b) Top view of waffle JFETLN



(c) Top view of waffle JFETLN differential pair

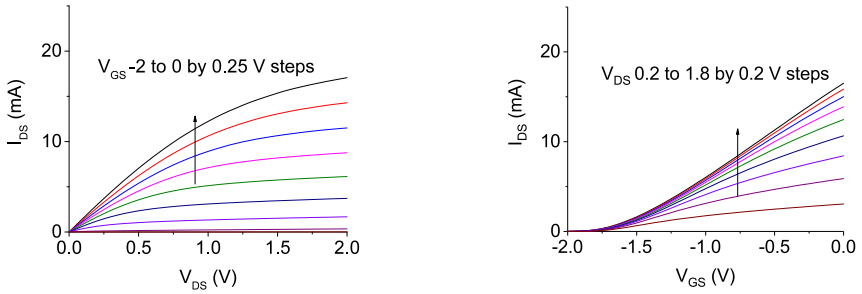
Figure 3.2: Device structures for JFETLN waffle variants © 2018 IEEE

3.4 Device results

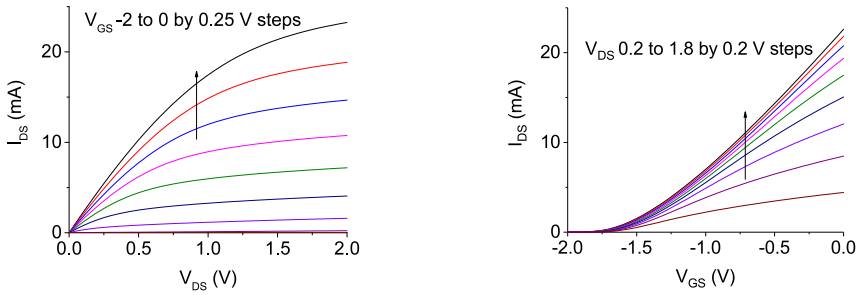
3.4.1 DC performance

The JFET chip was fabricated using IBM 0.18 µm CMOS process and die cut into individual 2 mm × 0.6 mm chips. The transistors were first characterized via DC measurement using large glass cut electrodes connected to the device terminals. The chip was mounted on a glass slide and connected to an Agilent B1500 semiconductor device parameter analyzer through use of a Summit 11000 probe station. The system was controlled with a PC running the Agilent EasyExpert software, which was used to program DC Current/Voltage (IV) sweeps.

IV sweeps were performed for each of the devices and used to independently change the gate to source and drain to source voltages, while measuring the gate and drain current. Measured IV sweeps for the JFETJC and JFETLN are shown in Figure 3.3. Device performance is shown to be relatively similar for the two JFET devices and shows a typical JFET



(a) JFETJC I_{DS} versus V_{DS} (b) JFETJC I_{DS} versus V_{GS}



(c) JFETLN I_{DS} versus V_{DS} (d) JFETLN I_{DS} versus V_{GS}

Figure 3.3: JFETJC and JFETLN Current-Voltage characterization © 2018 IEEE

device behavior with a linear region and saturation region in I_D versus V_{DS} plots and a pinch off and saturation region in I_D versus V_{GS} plots.

Further distinction between the JFETJC, JFETLN, and MOSFET can be made by looking at the device transconductance. This value was extracted from the slope of the I_D versus V_{GS} plots. Device transconductance per unit width for the shortest achievable channel length of 500 nm is typically 20.1 mS/mm (16.8 mS/mm) for the JFETLN (JFETJC). This compares with 23.7 mS/mm for a 0.5 µm long PFET and 44.2 mS/mm for a 0.5 µm long NFET in this technology.

3.4.2 Capacitance measurement

The B1500 semiconductor device parameter analyzer was used to characterize the input capacitance of the transistors using a capacitance measurement unit (CMU), in combination with the Summit 11000 probe station.

The measured JFETJC and JFETLN input capacitance as a function of V_{GS} are shown

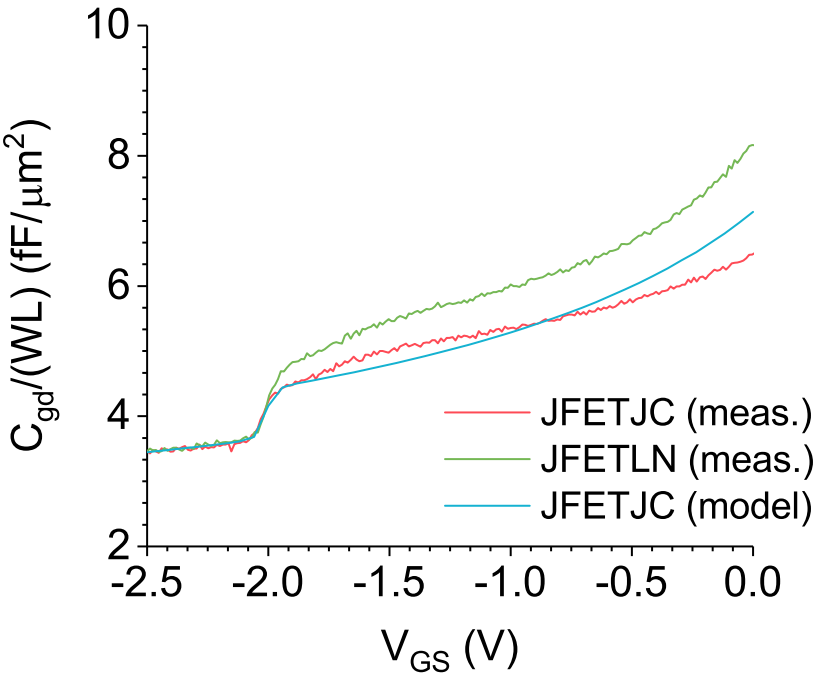


Figure 3.4: Measured JFETLN, JFETJC and JFET model input capacitance per gate width

in Figure 3.4. The 0.5 µm long JFETLN has an input capacitance between 4.4 fF/µm^2 and 5.9 fF/µm^2 of gate area in the typical region of operation (V_{GS} between −2.0 V and −1.0 V), while the JFETJC has between 4.4 fF/µm^2 and 5.4 fF/µm^2. In contrast, the measured NFET input capacitance for a 0.5 µm long device, shown in Figure 3.5, ranges from 5.8 fF/µm^2 and 8.6 fF/µm^2 in the typical region of operation (V_{GS} between 0.5 V and 1.0 V). The decrease in capacitance observed for the JFETLN and JFETJC for V_{GS} less than −2 V is caused by the body becoming fully depleted, resulting in a reduction in the gate-to-channel capacitance [121]. The JFETLN has slightly higher input capacitance than the JFETJC for V_{GS} above −2 V due to an increase in the gate-to-source junction area caused by the removal of the STI, as seen in Figures 3.1a and 3.1b.

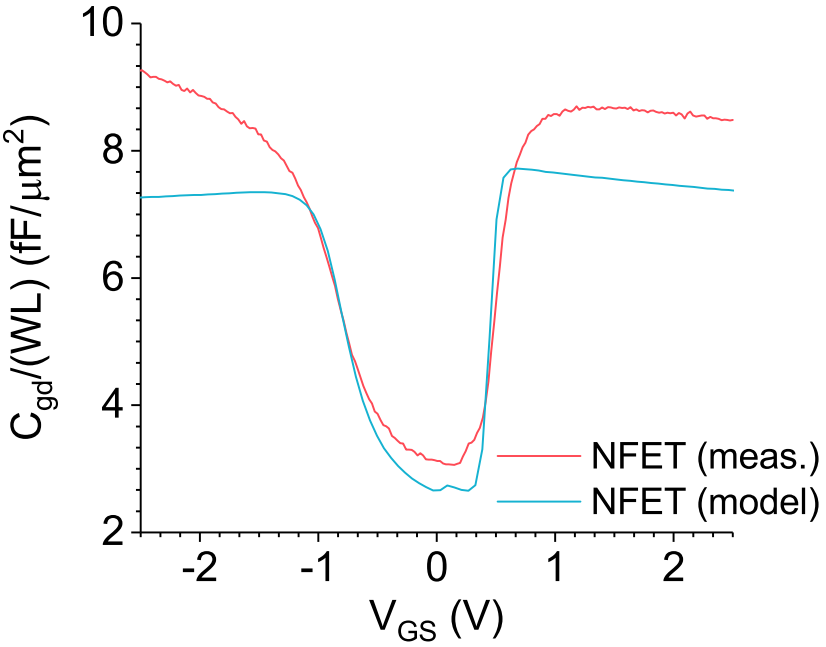


Figure 3.5: Measured NFET input capacitance per gate width compared with the NFET model © 2018 IEEE

3.4.3 Noise spectra measurement

Measurement of the transistor noise spectra were performed using the Summit 11000 probe station, a Stanford Research Systems SR570 transimpedance amplifier, and an Agilent Dynamic Signal Analyzer. The measurement was operated using MATLAB scripts to control all instruments via general purpose intrumentation bus (GPIB). The voltage noise was input referred using the transconductance of the SR570 and the transconductance value of the device under test (DUT) for the operating condition.

The input flicker noise power of the JFETJC, NFET, and JFETLN are shown in Figure 3.6 for devices with the same layout width (320 µm, as sixteen 20 µm fingers), length (500 nm), and current density (3.125 mA/mm). The input flicker noise power of the JFETLN is a factor of 100 lower than the JFETJC. In comparison with the NFET noise spectrum, the JFETLN has more than ten times lower input-referred flicker noise power. NFETs were used in these comparisons because the JFETJC, JFETLN, and NFET all support similar circuit topologies. An equally sized PFET in this technology still has more than four

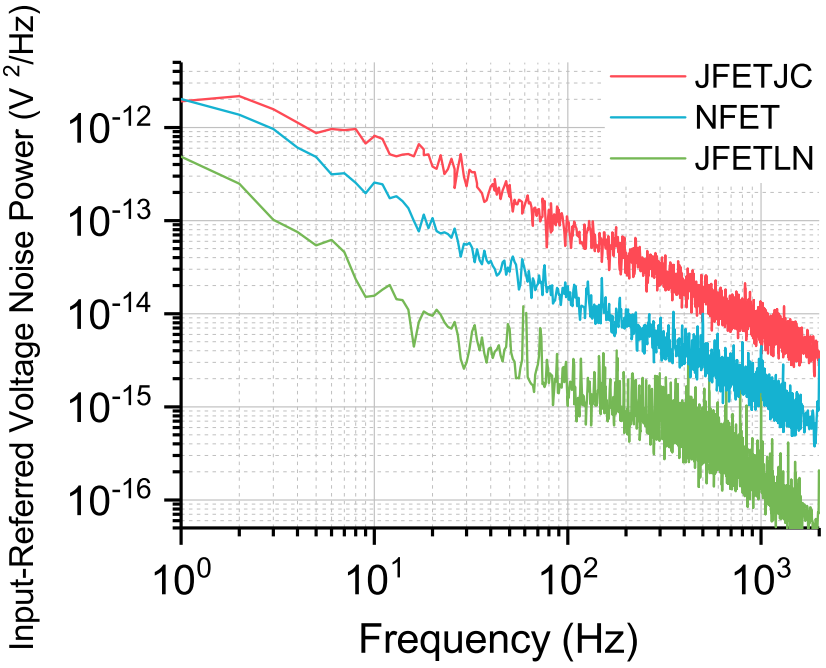


Figure 3.6: JFETJC, JFETLN, and NFET input-referred noise spectral density © 2018 IEEE

times the input-referred flicker noise as the JFETLN. The thermal noise performance is well predicted by the device transconductance. In this technology, the JFET devices have lower transconductance than NFET devices and comparable transconductance to the PFET devices. Therefore, the thermal noise performance of the JFET and PFET are comparable and higher than that of the NFET. The corner frequency for the JFETLN devices is approximately 4 MHz.

The $1/f$ noise was fit using an empirical model of the form: $S_n(f) = SI_D{}^{\alpha} f^{\beta}$, where I_D is the drain current, S is the total flicker noise coefficient, α is the current exponent, and β is the frequency exponent. The fit is then applied to noise curves at multiple current levels using a multilinear least-squares regression, as shown in Figure 3.7, for a waffle-style JFETLN (W = 10 µm, L = 500 nm). This fit results in noise coefficients of $S = 4 \times 10^{-16}$, $\alpha = 1.01$, and $\beta = -0.95$. These values are used in a Verilog-A compact model based on the JFETJC model, which is employed for circuit simulations.

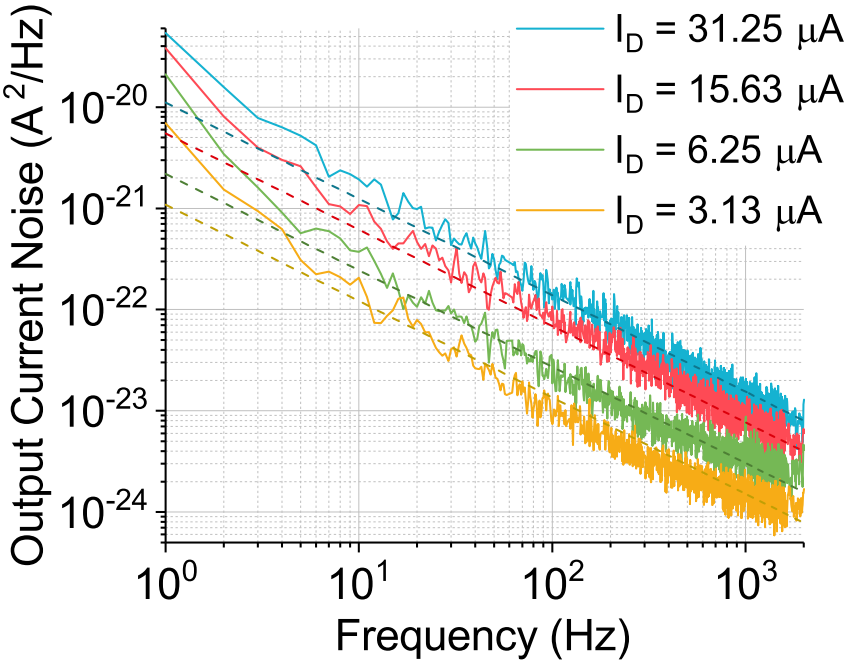
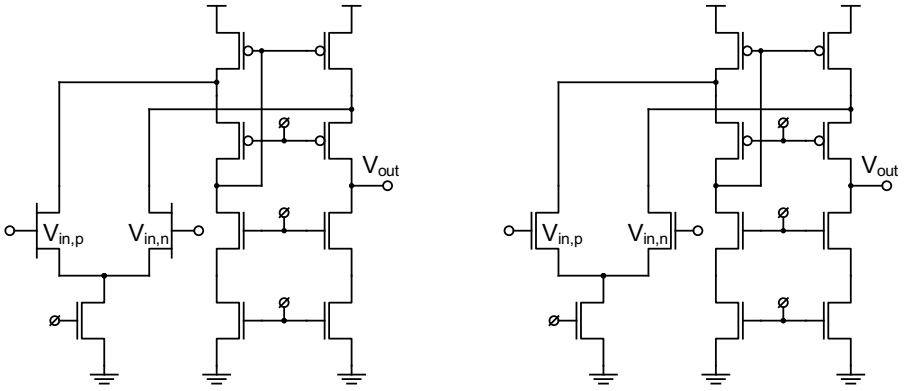


Figure 3.7: JFETLN output-referred current noise and multi-linear model fit © 2018 IEEE

3.5 Custom JFET-input low-noise amplifier

Using this JFETLN Verilog-A compact model, a low-noise JFETLN-input OTA was designed, built, and tested as seen in Figure 3.8a. This design uses two waffle-style JFETLN devices as the input differential pair. For comparison, an NFET-input OTA design (Figure 3.8b) was also simulated based on the same circuit design with the input transistors changed to NFETs. The geometry and bias currents were kept constant across the two designs and the DC bias configuration was set to keep both input pairs in saturation.

To verify the accuracy of the JFETLN model, the OTA was implemented in a trans-impedance configuration. The JFETLN-input amplifier has superior input-referred noise performance for bandwidths up to 1 MHz when compared to the simulated NFET-input design, as shown in Figure 3.9. The noise is reduced by up to 10 times versus the simulated NFET design. Using a feedback resistor of 1 MΩ, the measured DC gain was 986.7 kΩ. The input current was supplied via a 100 kΩ resistor to ground, to limit added noise. The



(a) JFETLN-input OTA schematic (b) NFET-input OTA schematic

Figure 3.8: JFETLN-input and NFET-input OTA schematics for amplifier noise comparison

measured noise for the JFETLN TIA agrees well with the simulation.

Near 1 MHz, the current noise from the feedback resistor begins to dominate for both OTAs. Also, the thermal noise caused by the lower transconductance of the JFETLN begins to overwhelm the gains from the lowered flicker noise. The JFETLN can be used for constructing low-noise integrated preamplifier stages in the 1 Hz to 1 MHz range, facilitating a variety of low-noise sensor applications.

3.6 Summary

New low-noise CMOS-integrated JFET structures were developed in a standard 0.18 µm CMOS process. These devices are ideal for low-noise amplifiers for bioelectronics applications due to flicker noise power that is a factor of 10 smaller than NFET transistors of the same size. Consequently, the input-referred current noise can be reduced by 90 % when these CMOS-integrated JFETs are used in place of NFET input transistors. In addition to reduced flicker noise, these low-noise JFETs are also well-suited for improving the performance of CMOS integrated amplifiers for bioelectronics applications due to their reduced input capacitance and CMOS compatibility.

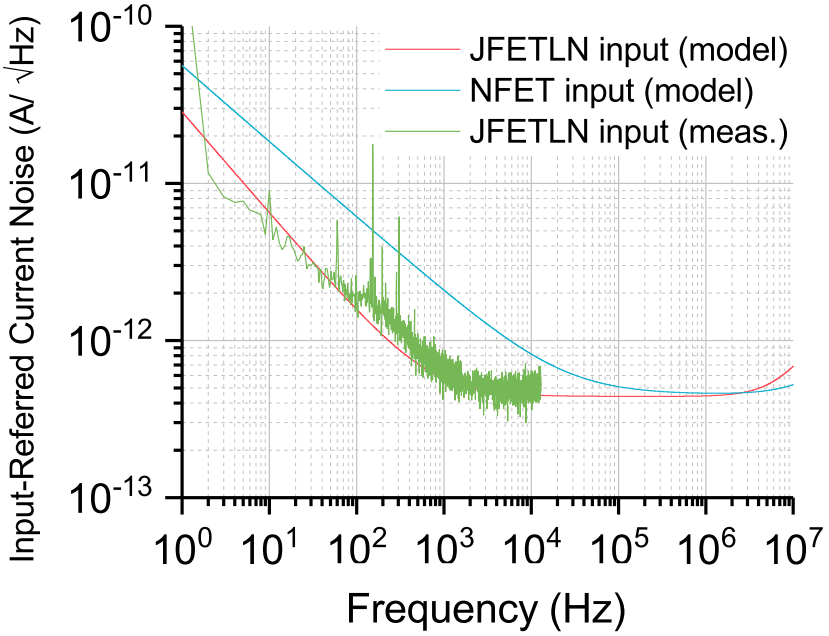


Figure 3.9: Input-referred current noise of JFETLN-input TIA compared with the simulation of JFETLN-input and NFET-input TIAs © 2018 IEEE

Chapter 4: Electrochemical Amplifier Design

4.1 Introduction

An electrochemical amplifier was designed to measure pA and fA level currents that are produced by redox substrates at extremely low concentrations. The system was designed with high gain and low noise in order to transduce electrochemical signals from these redox substrates. Effective low-current operation of the amplifier requires careful attention to circuit design, as parasitic elements that are ignored in typical designs can be influential. Additionally, the amplifier was created with a small form factor, to enable parallelized measurement. Although compact CMOS-integrated amplifiers benefit from decreased power consumption and reduced parasitic elements, limited layout area introduces significant challenges for low-noise detection. This amplifier design embodies the compromise between a small-form-factor CMOS-integrated amplifier and a high-gain, low-noise amplifier for electrochemical detection.

4.2 Design considerations

The overall specifications for the electrochemical amplifier were chosen to detect the lowest concentration of redox substrates with reasonable SNR, while maintaining acceptable bandwidth and dynamic range. The current produced by a small number of redox molecules can be extremely low and scales linearly with concentration. In steady state voltammetry, nM concentrations produce fA currents, so 20 fA was targeted as the smallest detectable signal. In order to achieve reasonable SNR, the input-referred noise in the target bandwidth needs to be at least three times lower than the smallest signal, so the noise specification was targeted for $5\,\mathrm{fA_{rms}}$. The complete target amplifier specifications are shown in Table 4.1.

	Target Spec.
Bandwidth	10 Hz
Noise	5 fA_{rms}
Gain	100 GΩ
Dynamic Range	67 dB
Channels	128

Table 4.1: Target specification for electrochemical amplifier

4.2.1 DC gain

An ideal amplifier has infinite gain as well as infinite speed allowing it to function at all frequencies. The gain of a real op-amp determines the accuracy and amplification of the output. The open loop gain of an op-amp is designed to be as large as possible, but the exact value cannot be known precisely due to small variations in the material properties of the semiconductor. To ensure an accurate and adjustable gain, op-amps are typically designed to operate in negative feedback to ensure a specified gain can be established accurately. When an op-amp is connected in negative feedback, the closed loop gain is determined by the impedance of the feedback network, resulting in

$$A_{CL} = R_F \tag{4.1}$$

for an ideal TIA. This gain determines the ultimate amplification of the input current signal.

The open loop gain of the op-amp is also important, as it determines the accuracy with which the input voltage is held to the reference potential V_p. The input voltage will have an error which is proportional to the inverse of the open loop gain A_v.

$$\Delta V = \frac{A_v}{1 + A_v} V_p \tag{4.2}$$

Therefore, an A_v of 1000 will result in the input voltage of $0.999V_p$.

4.2.2 Unity gain bandwidth

The ideal amplifier's infinite speed of operation is constrained by resistance, capacitance, and active device performance in real amplifiers. The bandwidth at which the loop gain of the amplifier becomes one is known as the Unity Gain Bandwidth (UGB). The UGB is the maximum bandwidth of operation for the amplifier, but the amplifier stability is also influenced by the UGB. Multistage amplifiers with multiple poles and high loop gain are necessary to achieve high loop gain, which enables low offset and high frequency performance. However, the presence of multiple poles in a negative feedback loop can cause the phase of the loop gain to drop below $-180°$ at a frequency below the UGB where the loop gain is greater than one. The result is positive feedback in the loop, causing the amplifier output to increase exponentially with time or oscillate. Therefore, frequency compensation is necessary to ensure amplifier stability at the UGB, while also retaining high loop gain.

4.2.3 Input and feedback capacitance

Input capacitance (C_I) is important when using op-amps for voltage sensing, charge sensing, or when considering the high frequency noise implications of TIAs. Input capacitance is not included to improve the circuit, but rather a necessary downside of semiconductor devices. Increasing the size of the input devices helps to reduce noise, but has the side effect of increasing C_I and potentially interfering also with the high frequency noise performance as seen previously in Section 2.2.2.

The feedback capacitance (C_F) is necessary to stabilize the amplifier feedback loop to prevent oscillations. C_F must be sufficiently large to stabilize the loop gain, but not too large as to impede the high frequency operation of the circuit through the $1/(R_F C_F)$ pole.

4.2.4 Voltage noise

Ideal op-amps do not generate or contribute any uncertainty or noise variation to the output voltage. Unfortunately, real circuit components introduce noise, which results in

random variation of the output voltage over time. The voltage noise of the op-amp directly impacts the noise performance of the overall circuit. Voltage noise in a TIA results in high frequency noise when amplified from the non-inverting input, as seen in Section 2.2.2.

The input differential pair is a primary concern, since the noise appears directly at the input. Careful sizing and biasing of these devices are required to maintain low-noise performance. For this application, the flicker noise has a large impact due to the low frequency of operation. Decreasing flicker noise of the input transistors is typically achieved by choosing large width and length to maximize device area. The larger device area helps to average out the individual trapping currents and thus reduces the flicker noise. Additionally, the biasing of transistors in weak inversion serves to reduce the white voltage noise, threshold voltage, V_{DSAT}, and DC mismatch, while increasing DC gain [122]. Weak inversion with large devices has the downside of reduced switching speed, worst g_m linearity, increased layout area, and increased input capacitance, which could negatively impact the noise as discussed in Section 2.2.2.

4.2.5 ESD

In ultra-low current amplifiers, electrostatic discharge (ESD) protection circuitry can impact the circuit performance. MOSFETs have thin oxide between the gate and channel, which allows for good control of the channel current as well as resulting in high g_m. However, thin oxide can be a liability if high voltages are involved. Static discharge can result in short-lived voltages of thousands to hundreds of thousands of volts, which can easily destroy thin oxide of MOSFET devices. To protect the oxide from static discharge, ESD diodes are added to the input and output pads to protect against unwanted high voltages appearing across MOSFET oxides. These diodes are reverse biased between the power rail and the signal line, and between the signal line and ground. If a high voltage or low voltage appears on the signal line, the corresponding diode will turn on and dissipate the voltage as a low resistance path.

However in ultra-low current measurements, ESD diodes are a potential concern, as even strongly reverse biased diodes can conduct a small current, which may contaminate the input current signal. The amount of current conducted by a p-n diode in reverse bias is given by

$$I_{R-G} = -\frac{qAn_iW}{2\tau_0} \qquad (4.3)$$
$$\tau_0 = \frac{1}{2}\left(\tau_p\frac{n_1}{n_i} + \tau_n\frac{p_1}{n_i}\right)$$

For typical applications, this current is insignificant, but for low-current measurements, any possible source of noise or error must be acknowledged.

4.2.6 Layout area

While not often discussed, layout area is an essential design consideration when implementing multichannel amplifier arrays. Device sizing for multichannel amplifiers is influenced by overall area limitations and geometrical constraints. The use of very small, short-channel devices increases the number of transistors that will fit on the chip and thereby increases the number of channels, while decreasing the power consumed. However, the smaller devices will suffer from increased noise due to more uneven charge trapping resulting in more $1/f$ noise and increased inversion level, resulting in increased white noise. Multichannel designs are forced to compromise between the device size, power consumption, noise performance, and many other factors impacted by device sizing.

4.2.7 Other considerations

Offsets

Offsets of both current and voltage in the amplifier circuit can have deleterious effects on performance. Voltage offset at the amplifier input is commonly caused by device mismatch as a result of process, voltage, and temperature (PVT) variations. The result is that despite the feedback operation of the amplifier and high loop gain (A_{OL}), a small difference in input

voltage will still exist. This voltage offset impacts the resulting output and has increased effect when the total closed loop gain is very high, as in this case.

Current offsets can also occur in the op-amp, most often due to current leakage through the input devices. BJT-input amplifiers operate through input current and are more likely to suffer from input current offest. In MOSFET devices, gate leakage is minimal due to the gate oxide presenting a nearly capacitive input. Gate leakage that does occur results from tunneling current through the gate oxide which results in leakage of fA current. While this current offset is often insignificant, thick-oxide MOSFET devices can be used to decrease the leakage further. However, the use of thick-oxide exacerbates short channel effects, while reducing g_m and switching speed.

Power supply noise

The power supply for an IC connects to almost all active devices directly. Therefore, any noise in the power supply voltage can impact noise performance throughout. Specifically, in op-amp circuits, the power supply noise is directly coupled to reference voltage noise, which presents as noise that is indistinguishable from the op-amp's input-referred noise. Careful design of the chip and PCBs can limit the effects of power supply noise. Power supply noise can be mitigated through the use of well behaved low-dropout (LDO) regulators combined with decoupling capacitance on both board and chip.

Shielding and guarding

When working with very small currents and voltages, parasitic resistance and capacitance can be extremely detrimental, since small conductances at any frequency are more likely to interfere than in more typical designs. Careful design of the circuitry involved is clearly important, but protecting the sensitive nodes from outside interference is essential to maintain the performance of the amplifier.

Shielding is used to prevent capacitive coupling between nearby circuits by providing

return path to ground or to an appropriate reference voltage [123]. Shielding is often used to protect a sensitive analog circuit from switching noise of a digital circuit. On CMOS chips, guard rings are shields which surround sensitive circuits and provide return path to prevent crosstalk and latchup between neighboring circuits [124]. Guard rings also protect against some ESD events by providing a discharge path for rogue currents [124].

Guarding, also known as active or driven shielding, is also used to protect sensitive circuitry. Guarding reduces common-mode capacitance, increases common-mode rejection, and eliminates leakage currents in high-impedance measurements [123]. The elimination of leakage currents is essential for detection of fA currents. To protect sensitive traces from these parasitics, a guard metal is used to surround the trace and drive the trace voltage close to the common-mode voltage. This reduces the voltage across the parasitic resistance and capacitance to zero, thereby eliminating the associated leakage current [123].

4.3 Chip design

The electrochemical amplifier was designed as a TIA with specific goals of both extremely low noise operation and compactness to enable the maximum number of channels. Each amplifier is constructed from three current amplifier stages and one TIA stage. The current amplifiers use either a compact matched CMOS pseudo-resistor design or matched diode-connected PMOS for the feedback network. The TIA stage uses resistive feedback with two programmable gain settings. To limit complexity and protect against digital charge injection, digital circuitry on the chip was limited to the bare minimum required for control of the amplifier operation. A schematic of the chip design including external gold and silver/silver chloride electrodes is shown in Figure 4.1.

The amplifier was fabricated in a commercial 0.13 µm CMOS process and contains 112 TIAs on each die. Each channel has input current noise density of $470\,\mathrm{aA}/\sqrt{\mathrm{Hz}}$ resulting in an integrated noise of $0.980\,\mathrm{fA_{rms}}$ within a 3.5 Hz bandwidth, while consuming 1.47 mW from a 1.2 V supply.

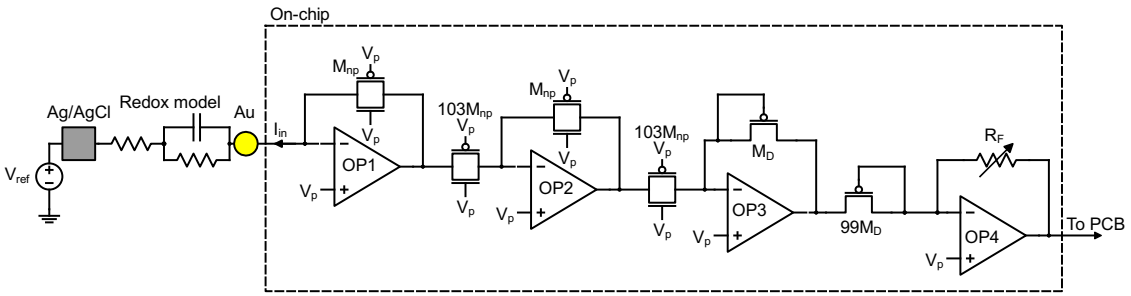


Figure 4.1: Schematic diagram of the chip design

4.3.1 Operational transconductance amplifier

Achieving the target specifications requires some careful design of the operational transconductance amplifier (OTA) that forms the main circuits for the amplifier. To achieve the noise target, the voltage noise of the amplifier should be minimized, while the gain should be maximized to reduce the contribution of noise from each op-amp stage. The dynamic range is another important metric to maximize, as it sets the sensing range of the amplifier.

However, to achieve the desired number of channels requires significant multiplexing by shrinking the area for each amplifier, which is in direct competition with the best noise performance and gain, which demand more circuit area. The target layout was designed to align with a 4 mil ball on 8 mil pitch for potential face-to-face chip bonding with a sensor array. This spacing limits each channel to an area of approximately 400 µm × 200 µm, as this will allow for one contact for signal input and one for signal output. This limits the available area for each stage to around 200 µm × 100 µm, with about half of the space being dedicated to the feedback network. This means that each op-amp circuit has to fit in 100 µm × 100 µm. The size restriction for each channel helps to determine the lower bound for the circuit noise. Increasing the size of the input transistors is the best way to reduce the $1/f$ noise that is the main culprit for op-amp voltage noise at these low frequencies. Therefore, the input transistors are made as large as possible to balance the size limits against the noise limits, while leaving enough space for the feedback network and stability compensation. A transistor

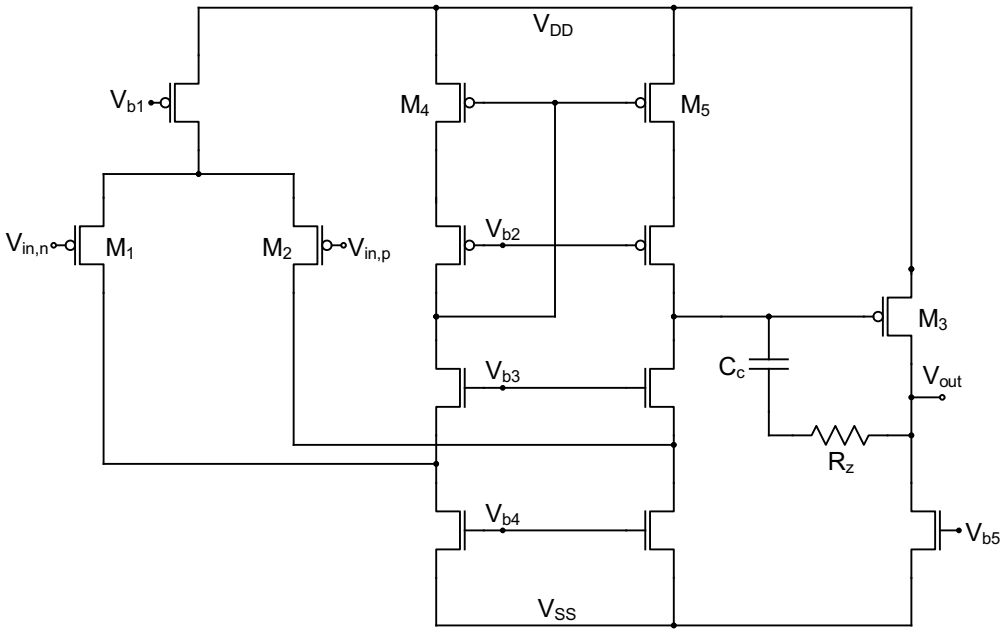


Figure 4.2: Two-stage folded cascode OTA with Miller compensation

level schematic of the OTA design is shown in Figure 4.2.

The amplifier was designed as a two-stage amplifier, with stage one being a folded cascode with p-type input transistors and stage two being a common source PFET stage. PFET devices were used for the differential pair because of their lower input-referred flicker noise in this CMOS process. Thick-oxide PFETs were used for the input transistors (M_1 and M_2) to ensure that any input leakage was kept to below fA levels. The input transistors are sized with $W/L = 200\,\mu m/500\,nm$ and are divided into $20\,\mu m$-wide fingers to construct a common centroid layout for improved matching. The input transistors are biased in weak to moderate inversion to increase the g_m/I_d and decrease the input noise while keeping the overall layout size down. The folded topology allows for maximal signal swing at the input for high dynamic range, while the cascode devices improve the gain of the first stage by increasing the load resistance. The second stage is a PFET common source amplifier (M_3) which further increases the gain and ensures high output swing that would be constrained by a cascode stage. The two-stage OTA design results in high open loop gain which requires capactitive compensation to maintain feedback stability. The second stage is compensated

with a 2.02 pF Miller capacitance C_c in series with a 1.5 kΩ resistance R_Z for pole-zero cancellation.

4.3.2 Current amplifier

Commercial instrumentation amplifiers are able to achieve high-gain and low-noise performance through the use of large discrete components Instrumentation amplifiers typically use large discrete JFET input transistors to achieve noise and gain performance required for physiological measurements [23]. Additionally, they use banks of large precise discrete resistors and capacitors to achieve high closed loop gain and wide dynamic range. Replicating the performance of instrumentation amplifiers in CMOS requires unique design adaptations.

Realizing large resistors in CMOS is difficult because the resistance per square is low for most CMOS materials. In this 0.13 µm technology, the CMOS resistor layer has a resistivity of 1.7 kΩ/□. Therefore, a CMOS resistor with 1 GΩ resistance would require an area of around 3×10^5 µm^2, which is almost four times the available 8×10^4 µm^2 area for each channel.

Several circuit methods can be used to achieve high transimpedance gain in a small layout area without using a large CMOS resistor. The most straightforward method is to construct an active device with high impedance to form the feedback network [11]. For this amplifier, pseudo-resistors were formed using large matched MOS transistor arrays to create the feedback resistance [125]. The pseudo-resistors consist of NFET and PFET transistors connected together by source and drain, with the gate biased using a reference voltage to keep them in the linear subthreshold region with very low V_{GS} and low V_{DS} [125]. The low current that flows and the mostly linear response to current in this region combine to create much higher resistances than are possible with CMOS resistors. Current amplifiers are created by using paired pseudo-resistors in a defined ratio [125] as shown in Figure 4.3. The width ratio between the two pseudo-resistors ensures that the feedback impedance is a specified fraction of the output impedance. Additionally, the matching of the feedback and

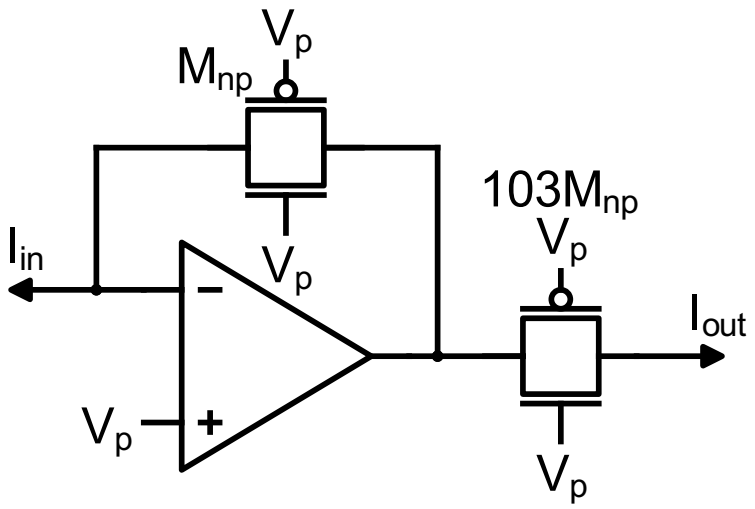


Figure 4.3: Current amplifier with pseudo-resistor feedback

output pseudo-resistors helps to cancel nonlinear behavior and maintains a linear overall response for current as the voltage across each pseudo-resistor varies. For this design, the feedback pseudo-resistors were composed of 2 parallel NFET and PFET devices each with $W = 20\,\mu\text{m}$ and $L = 500\,\text{nm}$. The output pseudo-resistors consisted of 206 NFET and PFET transistors of the same W and L. The transistors were arrayed in a symmetrical grid including 116 dummy transistors to improve PVT uniformity and matching. The resulting current amplifiers increase current by 103 A/A from input to output.

In order to maintain high resistance and linear current gain, the pseudo-resistors must stay in the linear subthreshold regime. In normal operation, this is ensured as the transistor gates are held at V_{mid} and the negative feedback of each stage maintains $V_{GS} = V_{mid}$. However, as current through the pseudo-resistor is increased, V_{DS} will necessarily increase. Momentary voltage transients at the negative terminal of the OTA due to amplifier settling can cause V_{GS} to increase above zero. When combined with the elevated V_{DS}, the pseudo-resistor will exit the subthreshold regime and no longer exhibit high resistance. To ensure that proper feedback resistance is maintained during transient behavior, the third stage was designed with diode-connected PFETs as feedback resistance, as shown in Figure 4.4. Diode-connected PFETs present a large bidirectional impedance much more compact than CMOS

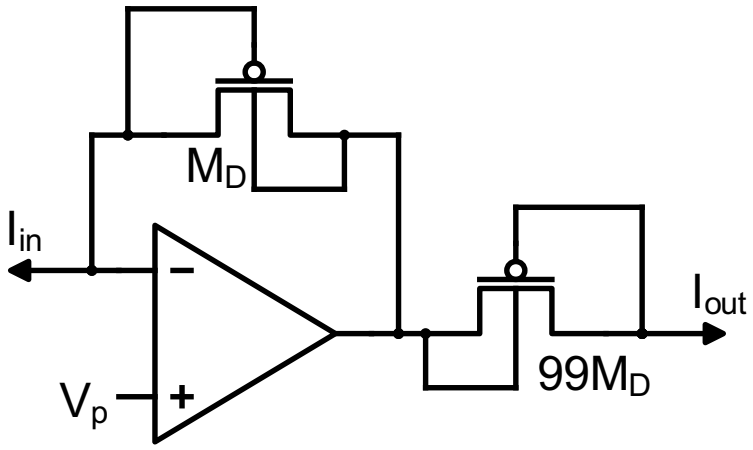


Figure 4.4: Current amplifier with diode-connected PFET feedback

resistors, but produce more current noise than the matched MOS pseudo-resistors. The alternate feedback increases the overall circuit noise, although the input-referred noise was increased only slightly due to the large current gain of the first two stages. The three current amplifier stages form a current gain of around 1 MA/A, which allows an input current of 1 fA to become 1 nA.

4.3.3 Transimpedance amplifier

The final stage is a TIA stage using a CMOS resistor for the feedback network. This TIA stage serves to convert the current signal to an output voltage. By this stage, the level of amplification ensures that the additional current noise from the feedback resistor (101.3 kΩ) will have minimal effect on the input-referred current noise. The feedback resistor is actually composed of twelve 8.44 kΩ resistors each with an area of 40 µm × 18 µm. The resistors were sized to achieve the desired gain, while also making use of the available space to ensure that the value is as accurate as possible given PVT varitions. In addition, the feedback resistor is flanked by four dummy devices for more protection against PVT variation and for improved matching between the elements. The feedback resistor is also controllable by an NFET switch to enable an alternate gain value of 67.5 kΩ, by shorting across four of the twelve resistors. The TIA and the three current amplifiers create an overall gain of 100 GΩ

on high gain and 66.7 GΩ on low gain. The TIA converts the fA–pA input current into an output voltage of mV–V, which is then passed on to the circuit boards for data conversion.

4.3.4 Bias circuitry

The bias circuitry on the IC supplies the voltages to the various OTA transistors to ensure the correct inversion level. This circuitry is shared between 32 amplifiers in order to save layout area. Current mirrors are used to set the needed current for each amplifier stage and are driven by off chip current sources (LM334). Channel selection circuits control the bias operation

4.3.5 Channel selection

The large number of input and output connections needed for the 112 amplifiers on the chip result in a very large number of pins needed for the pad ring. Due to the size restrictions of the chip and pads, the number of pads was limited to 232. This limitation requires that the inputs or outputs be multiplexed for simultaneous operation, but doing so with low current leakage restrictions is very challenging. Rather than introducting leakage from many transistor switches or digital switching noise from a multiplexer that can corrupt the input signal, the output voltage pins were shared between sets of four amplifiers, with operation of 32 TIA channels simultaneously. Amplifier selection is controlled through the use of fixed digital voltages to control which amplifiers are connected to the bias voltages at any time. The unused amplifiers are disconnected from the bias voltages, with the gates of the PFET bias devices connected to V_{DD} and the gates of the NFET bias devices connected to V_{SS} to ensure that the associated amplifiers are turned off. This methodology allows for the external one-hot channel selection signal to change which amplifiers are selected, without the complication of a multiplexer with potential leakage and high frequency charge injection.

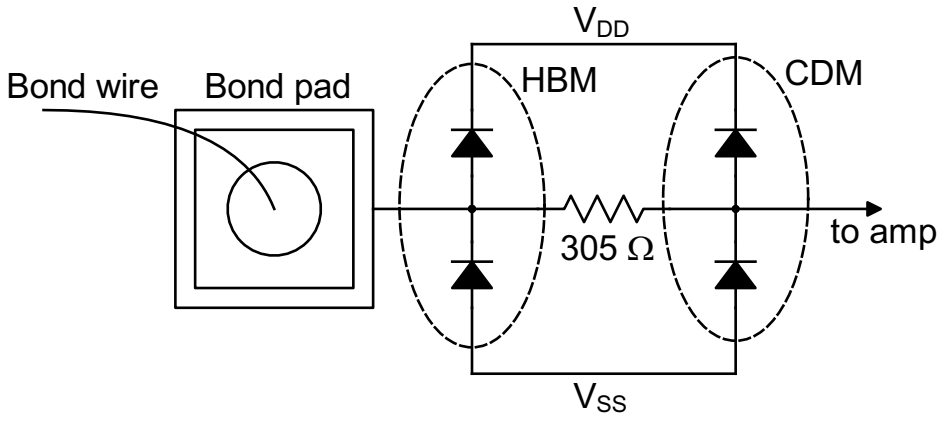


Figure 4.5: ESD protection circuit containing both HBM and CDM diodes

4.3.6 ESD

ESD is a particular concern for circuits sensitive to low current, both from the potential damage ESD can cause and the parasitic impacts of ESD protection circuitry. ESD from mechanical stress on the board or from ionic solution exchange in the fluid well were potential concerns. Mechanical stress and friction can cause electrical transients from piezoelectric or triboelectric effects. The exchange of solution by pipetting can cause static charge in the dispensed liquid due to frictional forces inside the pipette tip [126]. These concerns require the inclusion of ESD protection circuitry.

However, the typical ESD protection circuitry may cause unwanted leakage current that could compromise the measurement. ESD protection is provided by reverse biased p-n diodes connected between the chip pins and power rails. The full structure of the ESD protection circuit is shown in Figure 4.5. The full structure includes two sets of double diodes and a resistor to protect against human body model (HBM), machine model (MM) and charged device model (CDM) static events. HBM events occur when a human conducts charge between two chip pins. MM events are similar and occur when a charged metal tool discharges between two chip pins. CDM events occur when the chip is charged by the triboelectric effect or an external field and the voltage difference discharges through an external ground.

Even though the diodes do not conduct significant current in reverse bias, the current could be in the femtoampere regime, which would introduce unwanted noise and offset. Additionally, ESD diodes contribute unwanted capacitance at the input pins. Because of these potential problems, the amplifiers on the chip were constructed with three variations of the ESD protection circuit. Variants were created with full ESD protection, no ESD protection, and HBM-only ESD protection. This allows the ESD protection circuitry to be selected based on circuit performance.

4.3.7 Test resistance

A test resistor R_{cor} replicating the feedback resistor for the transimpedance amplifier was included to better calibrate and verify the overall system gain. PVT variation will result in different circuit behavior depending on the exact manufacturing details of the particular IC. The value of the R_{cor} will indicate the resistive process corner for each amplifier chip, and this information increases accuracy of circuit simulations.

4.3.8 Layout and packaging

Each amplifier channel occupies an area of $400\,\mu m \times 200\,\mu m$ and contains three current amplifiers and one transimpedance amplifier. The layout of the amplifiers including the locations of the different circuit elements is shown in Figure 4.6. The full chip area, shown in Figure 4.7, contains the 112 copies of the amplifier, test channel, and decoupling capacitors, as well as all previously discussed circuitry. The pad ring has 196 pads, which are connected via wirebond to corresponding bond fingers on a 272-pin ball-grid array (BGA) package. The BGA/chip assembly is then epoxy encapsulated using dam (Hysol FP4451) and fill (FP4450) epoxy to protect and cover the wirebonds and integrated circuit. The final chip is fully covered with epoxy and the input current is connected using the BGA socket.

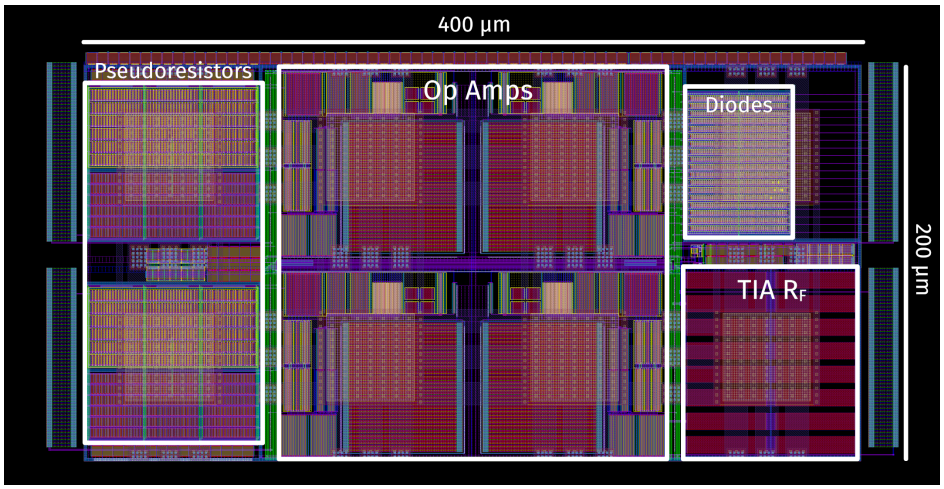


Figure 4.6: Single amplifier channel layout with 100 GΩ gain

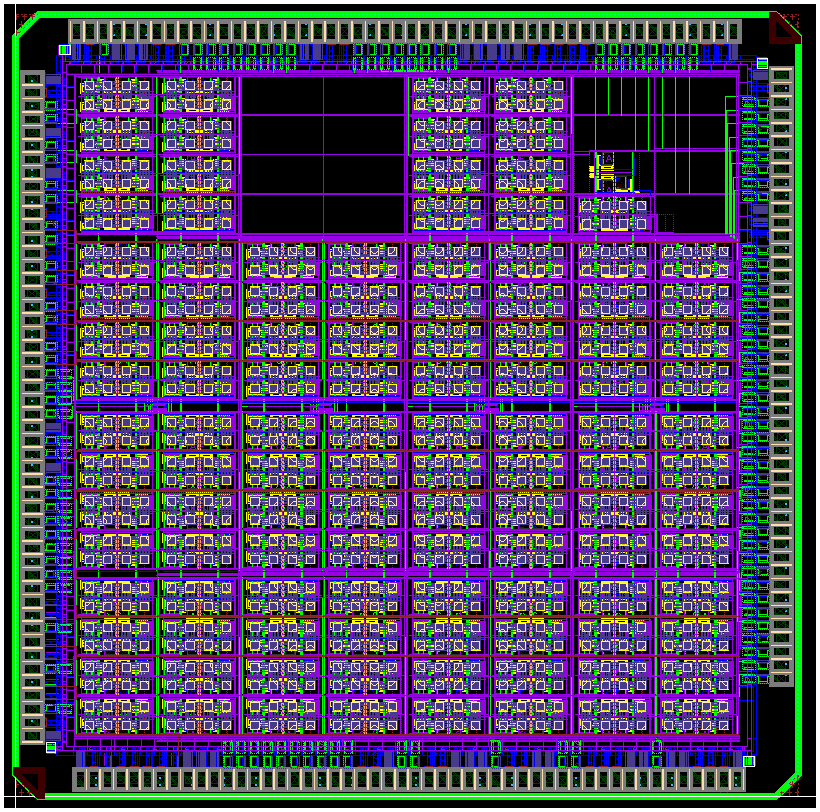


Figure 4.7: Full amplifier chip layout with 112 amplifier channels

4.4 Board design

4.4.1 System overview

Printed Circuit Boards (PCBs) were created to interface the circuit with the sensing electrodes and computer. To avoid the contamination of the sensitive analog input signal with digital noise from the control circuitry and electro-magnetic interference (EMI), the amplifier, electrodes, and associated circuits were isolated on the daughterboard, which was was contained within a grounded metal box used as a Faraday cage. The digital interface circuitry was assembled separately on the motherboard, with control signals for the amplifier passing through digital isolators to protect the analog front-end from switching noise. The boards are interfaced to the computer using an FPGA interface board (Opal Kelly XEM3010). The complete system block diagram showing both boards with the connections between the various components is shown in Figure 4.8.

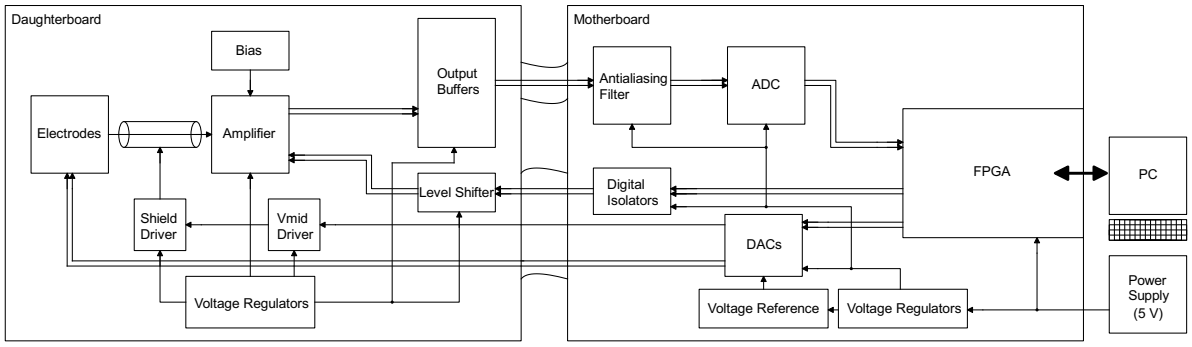


Figure 4.8: System block diagram showing PCBs

4.4.2 Power domains

Power for the PCBs is provided from a DC wall power supply at a voltage of 5 V. This power supply connects to low drop-out power regulators on both boards and to the FPGA interface board. On the daughterboard, the power regulators are connected to two different power planes. The output buffers, V_{mid} buffer, and shield buffer operate on a 3.3 V supply, while the amplifier and bias circuitry are powered by 1.2 V On the daughterboard, the power

regulators are connected to two different power planes. The output buffers, V_{mid} buffer, and shield buffer operate on a 3.3 V supply, while the amplifier and bias circuitry are powered by 1.2 V. The level shifter converts the 3.3 V logic of the FPGA to 1.2 V logic levels for the IC. The daughterboard makes special use of the internal power planes for shielding, which will be discussed in Section 4.4.4.

4.4.3 Voltage references

Several voltage references are required for the amplifier to function. The reference voltages are generated by the digital-to-analog converters (DACs) on the motherboard. The DACs also require a voltage reference to set the full scale value, which is generated using voltage reference IC (LM4041) utilizing a Zener diode. The LM4041 is configured for an output voltage of 1.2 V.

Voltage references are also used on the daughterboard for the amplifier and for applying the electrochemical potential to the pseudo-reference electrode. The V_{mid} reference provides the voltage for the positive terminal of each op-amp stage and applies the gate bias to the pseudo-resistors. The V_{mid} voltage is buffered and low-pass filtered on the daughterboard before connection to the corresponding amplifier pins. The electrode reference voltages are also generated by the DACs and are low-pass filtered to reduce high-frequency noise before connecting to the electrode socket and to pins for connection to external electrodes or test leads.

4.4.4 Input shielding

The performance of the amplifier is dependent upon the measurement of fA- and pA-level currents passing through the PCB. To decrease the possibility of current leakage through the PCB, the board material was altered and shielding circuitry was constructed on the daughterboard. PCBs are usually constructed from etched copper layers separated by a glass epoxy dielectric termed flame retardant 4 (FR4). However, typical FR4 material has

	FR4 glass epoxy [127]	Rogers 4003C [128]
ϵ_r	4.6	3.55
ρ ($\mathrm{M\Omega \cdot cm}$)	5.2×10^8	4.2×10^9
R_S ($\mathrm{M\Omega/\square}$)	5.4×10^7	1.7×10^{10}
$\tan\delta$	0.015 at 1 MHz	0.0021 at 2.5 GHz
Water Absorption	0.15 %	0.06 %

Table 4.2: Dielectric parameters of PCB insulator materials

dielectric properties that are not well suited for this application. The relevant dielectric properties of FR4 are compared against Rogers 4003 (RO4003C), a competing laminate typically used for RF design, in Table 4.2.

This PCB was constructed from RO4003C laminate rather than using FR4 material. The lower dielectric constant (ϵ_r) of RO4003C results in lower capacitance of traces on the PCB. The RO4003C material also has higher volume (ρ) and surface (R_S) resistivity, which protects against resistive leakage through the board. The Rogers material also has lower water absorption than FR4 material. Absorption of moisture from the air and assembly residues by the PCB causes the surface and volume resistivity to drop, increasing current conduction through the board. The dielectric loss ($\tan\delta$) of RO4003C is also lower than that of FR4 material. Voltage transients across the dielectric create long lived fA currents due to this dielectric loss. The lower $\tan\delta$ of the RO4003C causes these currents to drop below fA levels more than 100 times faster than on boards constructed of FR4. This change in PCB material helps to ensure that board-related losses are not causing fA leakage, which would otherwise significantly impact the sensing performance of the amplifier.

Additionally, the connection between the electrode socket and the amplifier socket that conducts the current signal was shielded with active electronics. Actively-driven shielding around sensitive current lines can help ensure that parasitic capacitance and resistance cause less leakage current, thus protecting the analog input [123]. For this board, the signal lines for the electrode connections were routed through the interior of the board. The layers above and below the signal lines were power planes used to create a pseudo-coaxial shielding

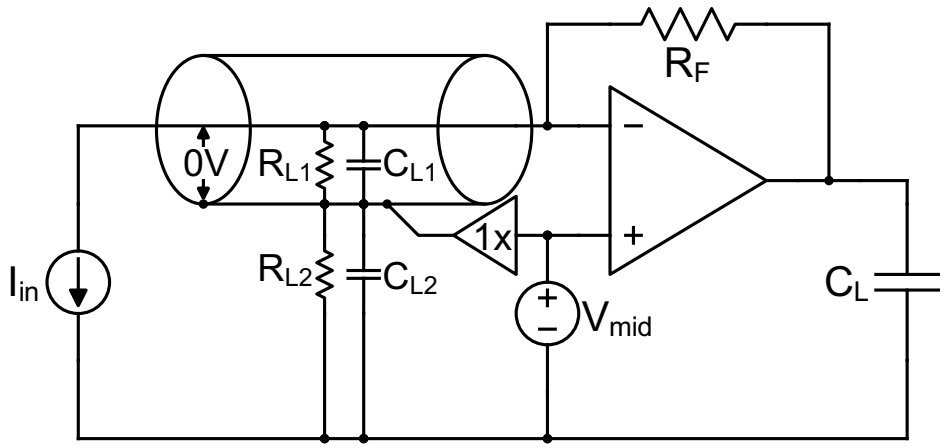


Figure 4.9: Schematic representation of shielding topology

surrounding each of the input lines. The shielding was connected to a buffered version of the V_{mid} voltage in order to minimize the voltage difference between the shield and the input line, for which the voltage should be held to V_{mid}. The shielding helps to limit the effect of PCB resistance and capacitance that might interfere with the ability to measure fA-level currents by forcing the voltage across these to zero. A schematic of the shielding circuit is shown in Figure 4.9.

4.4.5 Data transfer

The output of the amplifier is connected to a bank of output buffers to drive the capacitance of the cable and wiring between the two boards. The motherboard contains the circuitry for the data conversion and transfer to the computer. To avoid noise aliasing from the ADC, the analog data is low-pass filtered using a 4-pole Bessel filter implemented using cascaded Sallen-Key filters. Bessel filters are often used for anti-aliasing filters, since Bessel filters have maximally flat group delay which best maintains the shape of input signals. The overall filter transfer function is designed to have a gain of one and a cutoff frequency of 10 Hz. The filter prevents aliasing by minimizing any input to the ADC above 1/2 of the ADC sample rate of 60 samples per second. The Sallen-Key filter topology used to implement the Bessel filter is shown in Figure 4.10. The component values are shown in Table 4.3

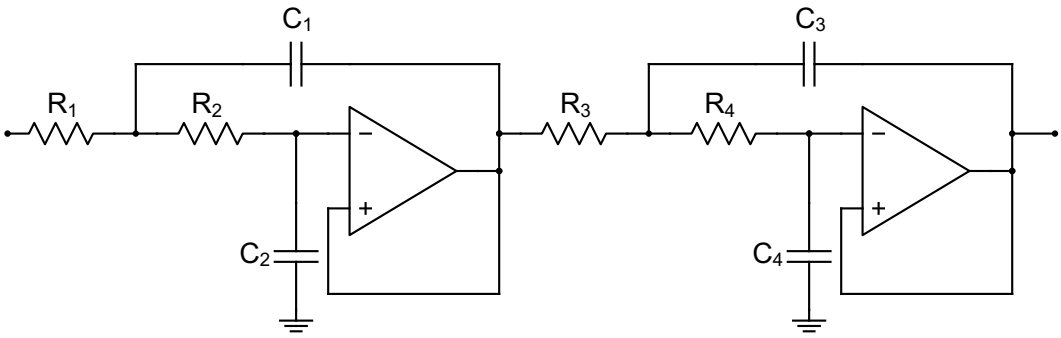


Figure 4.10: Sallen-Key filter topology

	Component values				Filter paramters	
Stage	R_1	R_2	C_1	C_2	Q	GBW
1	5.6 kΩ	16.3 kΩ	1 µF	1.5 µF	0.53	13.6 Hz
2	7.5 kΩ	16.3 kΩ	470 nF	1.5 µF	0.83	17.1 Hz

Table 4.3: Anti-aliasing filter component values and Q/GBW

and are chosen to ensure the 10 Hz cutoff.

A 24-bit Sigma-Delta ADC is then used to digitize the output of the anti-aliasing filter at an output data rate of 60 samples per second with four independent measurement channels. The ADC causes quantization noise as a result of sampling the analog signal, which depends on the resolution and full scale voltage. Given that $V_{fs} = 3.3\,\mathrm{V}$ and $\mathrm{N} = 24\,\mathrm{bit}$, the least significant bit $V_{lsb} = V_{fs}/2^N = 1.966 \times 10^{-7}\,\mathrm{V}$. This results in a quantization noise power of $V_{lsb}^2/12 = 3.22 \times 10^{-15}\,\mathrm{V^2/Hz}$. When input-referred this becomes $7.247 \times 10^{-37}\,\mathrm{A^2/Hz}$, which is equivalent to the noise of a 22.7 TΩ resistor and is therefore insignificant when compared to the other noise sources. The ADC digital outputs are connected directly to the Opal Kelly FPGA.

4.4.6 Grounding and EMI

To protect the sensitive input electronics from EMI, the daughterboard is enclosed in a Faraday cage connected to the board ground. The daughterboard and motherboard are both connected to ground at the negative terminal of the DC power supply in a star ground configuration, in order to prevent ground loops. High conductivity cabling is used to con-

nect the mother and daughterboard grounds together to ensure that the same potential is maintained and that no inductive currents flow in the ground connection.

4.5 Software

The amplifier and PCBs are controlled using 3.3 V logic from the Opal Kelly module. The Opal Kelly XEM3010 FPGA module controls the digital transfer of data from the ADC and to the boards, including programming the ADC, DAC, level shifter, and digital isolators. The FPGA is programmed using custom Verilog code to manage the data transfer and digital communications. Incoming data from the ADC is read serially into a 32×128 FIFO buffer to avoid any loss of data due to speed changes on the USB bus. The incoming data also records the ADC status and channel information.

The FPGA Verilog code also controls the programming of the DACs, isolators, and level shifter via serial interface. The DAC programming module also stores voltage waveform paramters and outputs the voltage-time curve for voltammetry experiments. To control the entire system, a software interface was written using Python backed by the PyQt5 user interface library. The computer program handles powering, resetting, programming, and reading back from the FPGA and various ICs on the boards, enabling the PC side data transfer, voltammetry waveform settings, and channel selection for the chip. The program stores the data in binary format, while processing and presenting the data as $i(t)$, $v(t)$, power spectral density, and voltammogram plots using the pyqtgraph module.

4.6 Measurement results

Once the amplifier was assembled onto the PCBs and connected to the computer, the electronic system could be characterized. The resulting specifications are compared to the target (and simulated) specifications in Table 4.4.

	Target Spec.	Postfab. Spec.
Bandwidth	10 Hz	3.5 Hz
Noise	5 fA_{rms}	1 fA_{rms}
Gain	100 GΩ	100 GΩ
Dynamic Range	>60 dB	65 dB
Channels	128	112

Table 4.4: Target and postfabrication specifications for electrochemical amplifier

4.6.1 Gain

To verify the performance specifications for the chip, a 10 GΩ test resistor (R_{test}, Ohmite HVF Series) was connected from the DAC-supplied reference voltage to the amplifier input, as shown in Figure 4.11. The exact value of R_{test} was verified using a Keithley 2450 source meter to be 10.86 GΩ. This resistor circuit allows for the characterization of the amplification gain, bandwidth, and offset current. For the measurement of the amplifier gain, the input current was varied using the DAC voltage and R_{test}. The current-voltage plot of the gain measurement is shown in Figure 4.12. The gain stays constant across a wide range of input currents for a maximum signal of 14.72 pA on the low gain setting. The current sensing capabilities of the amplifier are shown in Figure 4.13. This plot shows the response of the amplifier to voltage steps of 300 µA through R_{test}, resulting in 30 fA current steps. The individual steps are easily distinguishable from the baseline noise with high SNR.

4.6.2 Test resistance

The test resistor R_{cor} was included to characterize the effects of PVT on the amplifier feedback resistor R_F. Measurement of the test resistor can be done for each chip to see the unique impacts of PVT for that particular die. The nominal value for R_{cor} is 101.3 kΩ. Values of R_{cor} for several different amplifier chips were measured with a digital multimeter and are shown in Table 4.5. These measured values indicate a high R corner for the four measured amplifiers. This indicates that the overall PVT corner is towards a slow corner.

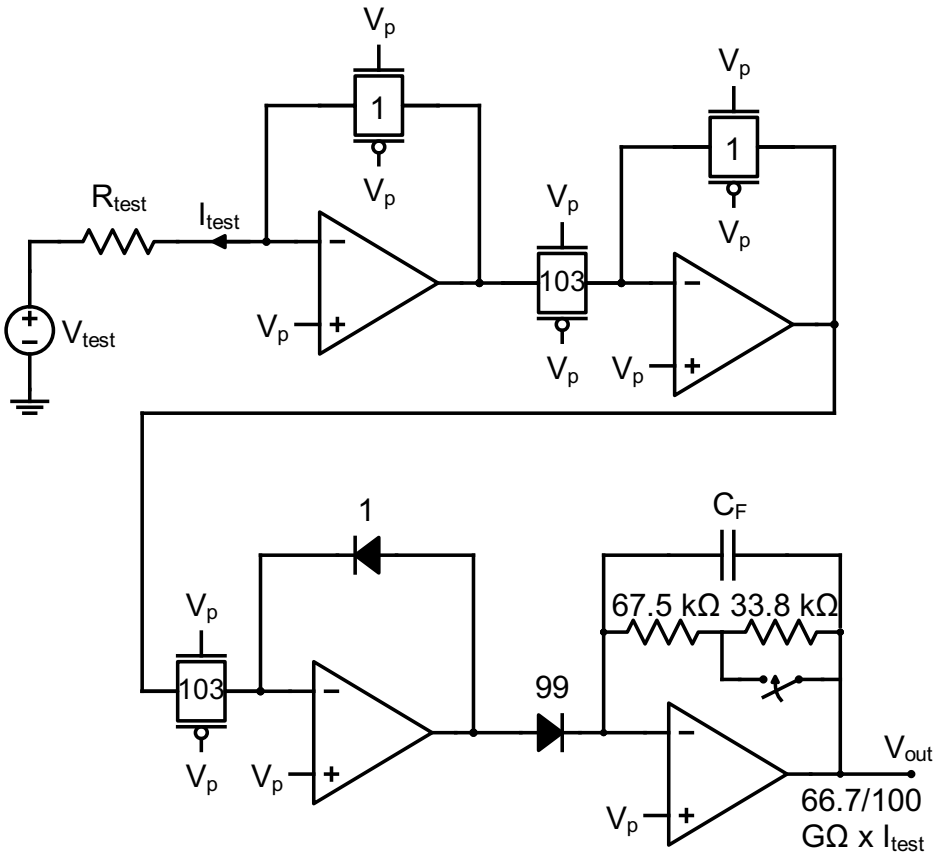


Figure 4.11: Test resistor setup used to verify gain, bandwidth, and offset

Amplifier	R_{cor} (kΩ)
1	106.3
2	107.6
3	105.5
4	106.9

Table 4.5: Values of R_{cor} for several amplifier chips

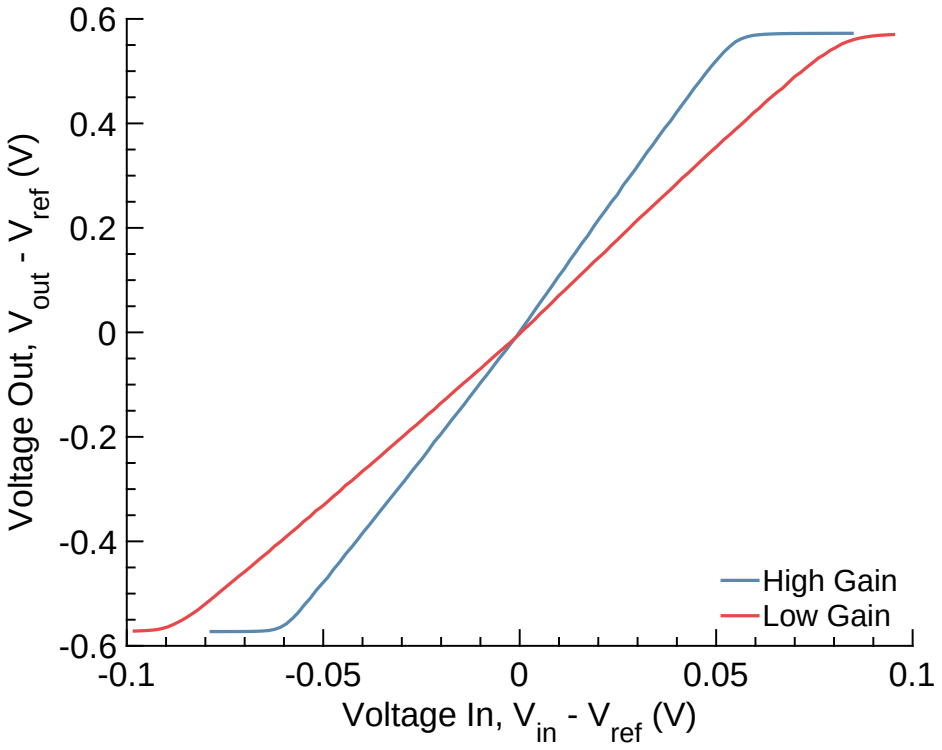


Figure 4.12: Amplifier current-voltage characteristic with $R_{test} = 10\,\mathrm{G\Omega}$

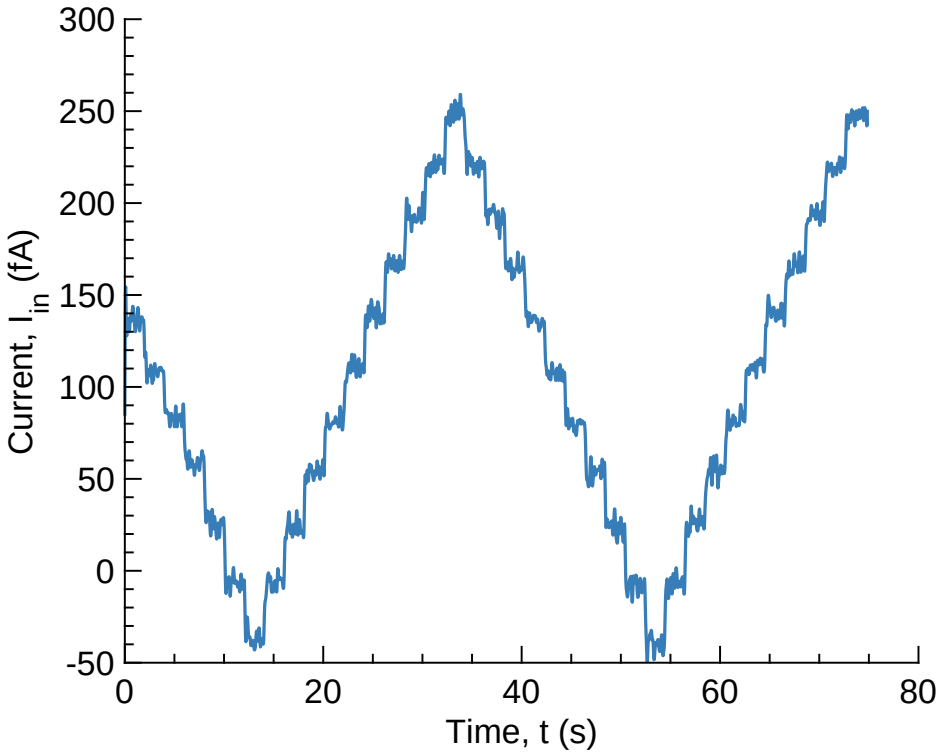


Figure 4.13: Amplifier current-time with 30 fA steps and $R_{test} = 10\,\mathrm{G\Omega}$

4.6.3 Bandwidth

The bandwidth of the system sets the minimum temporal resolution for the measurement. This system was designed with a target specification of 10 Hz bandwidth. However, the final system bandwidth is dependent on the input current. When the input current is high, the effective resistance of the R_f pseudo-resistor is lowered and therefore the primary pole between R_f and C_f moves to a higher frequency. When instead the input current is low or zero, the effective resistance of the pseudo-resistor becomes higher and then feedback pole moves in, shrinking the effective bandwidth.

The resulting bandwidth including the amplifier and the anti-aliasing filter was measured by injecting a sinusoidal input through R_{test} and recording the output with the PCB. The transfer function of input magnitude to output magnitude can then by sampled at different frequencies to find the bandwidth. The circuit was also simulated in the same configuration with an AC sweep. The resulting bandwidth measurements match in showing that the amplifier reaches 10 Hz bandwidth outside of the area around zero input current, but the bandwidth drops down to 3.5 Hz in the vicinity of zero current, as shown in Figure 4.14.

This issue can be solved with the inclusion of an additional capacitor between the output of the op-amp and the next stage that has a size ratio similar to that of the pseudo-resistor. This ensures that the specified gain will be maintained at higher frequencies due to the zero that this creates in the overall transfer function to cancel the primary pole. The current amplifier output capacitor could not be used in this design due to the additional layout area required, as $C_{out} = 103 \times C_F = 46.7\,\text{pF}$. Even if this capacitor was implemented as a high value metal-insulator-metal capacitor, the area of this capacitor would be prohibitively large, taking roughly $107\,\mu\text{m} \times 107\,\mu\text{m}$ for each amplifier stage. Additionally, a capacitor of this size could not be effectively matched to ensure alignment of the high frequency gain with the pseudo-resistor gain at low frequencies.

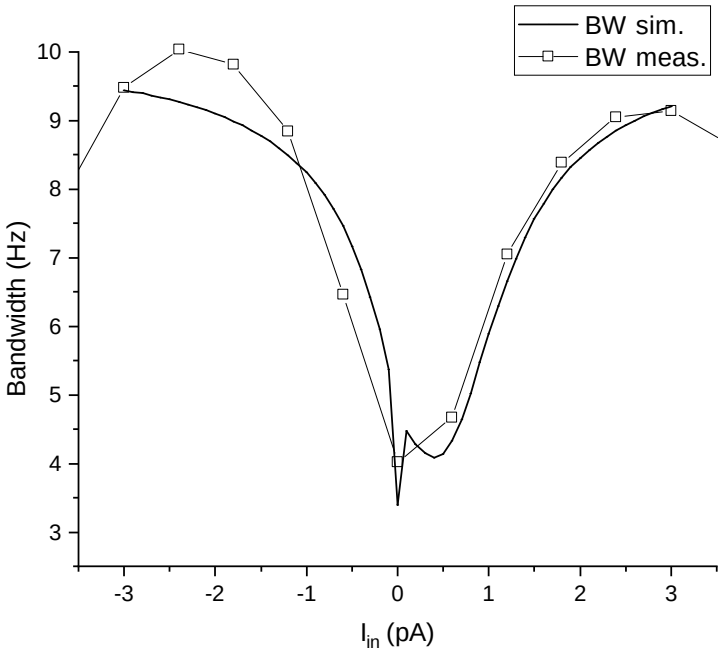


Figure 4.14: Amplifier bandwidth compared with simulation including anti-aliasing filter

4.6.4 Open head stage noise

The noise performance of the electrochemical amplifier is key for the measurement of low redox concentrations. Open head stage noise was measured using the 66.7-GΩ setting with no electrodes connect to the amplifier input, allowing only the board parasitics and amplifier circuitry to impact the noise. The chip was also simulated in the open head stage configuration across all PVT corners. The measured data fell in between the nominal (tt) and slow-fast (sf) PVT corners and is shown compared with these corner simulations in Figure 4.15. The tt corner simulation shows an integrated noise of $1.247\,\mathrm{fA_{rms}}$ in a bandwidth of 1 mHz to 3.5 Hz. The sf corner simulation has an integrated noise of $0.885\,\mathrm{fA_{rms}}$ in the same bandwidth. The measured data similarly has an integrated noise of $0.980\,\mathrm{fA_{rms}}$ in the same bandwidth, indicating circuit operation between the tt and sf process corners.

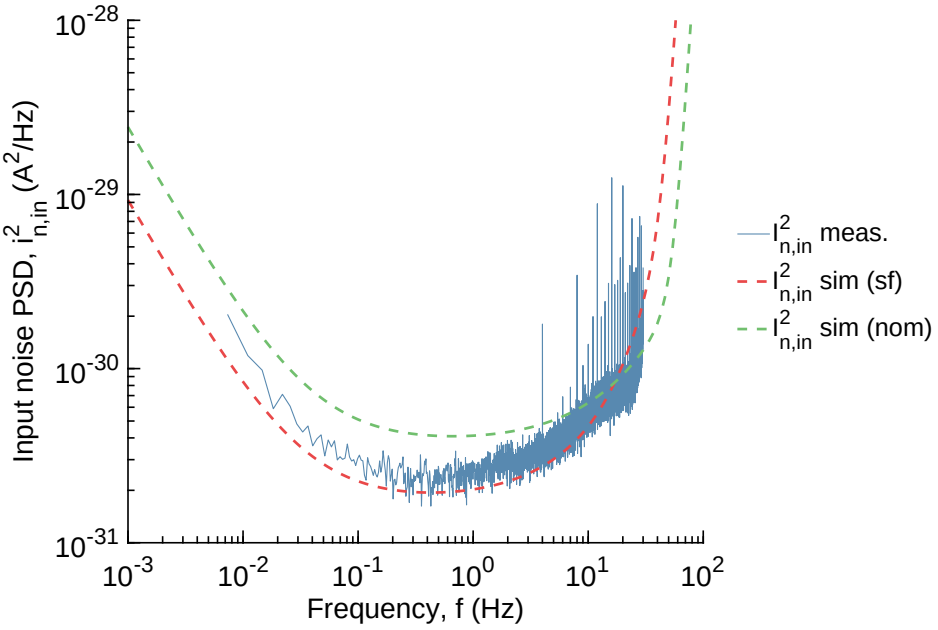


Figure 4.15: Open head stage noise power spectral density from measurement and simulation

4.6.5 Dynamic range

The open head stage noise (Section 4.6.4) can be combined with the maximum signal capabilities from the gain measurement (Section 4.6.1) to express the dynamic range of the TIA. The dynamic range provides a metric for the breadth of signal levels that can be measured, by dividing the maximum and minimum signal levels. Using the measured open headstage noise, the dynamic range is given by $DR = 14.72\,\text{pA}/0.980\,\text{fA} = 83.5\,\text{dB}$ for the $66.7\,\text{G}\Omega$ gain setting. When using the $100\,\text{G}\Omega$ gain setting, the input current range drops to $10.08\,\text{pA}$, resulting in a dynamic range of $80.2\,\text{dB}$.

4.7 Summary

A low-noise, high-gain amplifier was designed and created for the purpose of electrochemical measurements of low concentration redox analytes. The amplifier was assembled onto PCBs and connected to a computer using an Opal Kelly FPGA module to coordinate and transfer data to and from the PCBs. The entire current sensitive circuit was enclosed with a Faraday cage to protect against EMI. The system was tested to verify the circuit

performance compared to both target and simulated specifications. The electrochemical system is capable of measuring currents of single digit fA at a bandwidth of 3.5 Hz. Chapter 5 will show the application of this amplifier circuit to the measurement of low concentration potassium ferrocyanide and potassium ferricyanide solutions.

Chapter 5: Submicromolar Electrochemistry

5.1 Introduction

Electrochemical analysis is extremely useful for the detection and discrimination of chemical compounds. Techniques for electrochemistry have improved dramatically since the beginning days of polarography. Detection of biologically relevant chemicals has become one of the most important applications of electrochemistry. Point-of-care analysis using electrochemical detection requires exceedingly compact and sensitive multifunctional integrated circuits. As circuits become smaller, the high sensitivity capabilities become more important and more difficult to maintain. This chapter presents the low-noise detection of submicromolar redox analytes using a compact, multichannel CMOS-integrated circuit for current amplification. Highly sensitive redox measurement performed with an integrated amplifier paves the way for the development of portable multifunction analytical devices for medical diagnosis and treatment.

5.2 Experimental setup

The electrochemical amplifier was designed to measure redox-active molecules using voltammetry measurement techniques. The electronic specifications as detailed in Chapter 4 were designed to accomplish the task of voltammetry with very dilute solutions of redox molecules. The amplifier is capable of current measurement down to single-digit fA levels. The chip can perform voltammetry in order to determine the redox potential and current as shown in Section 2.4. Measurement of ferrocyanide/ferricyanide redox couple will be shown with a detection limit of 100 nM at a current level of 300 fA.

A working electrode was fabricated in the form of a gold ultramicroelectrode (UME)

with radius $r_0 = 15\,\mu m$. This disk-shaped UME was fabricated using a conventional photolithography process combined with metal deposition via electron-beam evaporation. After patterning a silicon dioxide-covered silicon wafer with positive photoresist, a 5 nm chrome adhesion layer and a 250 nm gold layer were deposited on top. The metal liftoff process leaves behind a layer of gold patterned into $50\,\mu m \times 50\,\mu m$ square pads with gold leads to larger pads for wirebonding. The gold pads were then masked with a circular microwell with $15\,\mu m$ radius using a negative p The SU-8 layer is $5\,\mu m$ to $10\,\mu m$ thick, forming a microwell with an volume of 3.5 pL to 7 pL.

The gold UME chips were then diced and mounted onto ball grid array (BGA) packages using silver epoxy. The individual electrode leads were electrically connected to the BGA via wirebonding, enabling electrical connection to the amplifier through the PCB. A separate BGA package was used to connect the electrodes to allow easy replacement in the event that the electrodes are fouled or contaminated by redox molecules. The extreme sensitivity of the amplifier to conductivity changes of the electrodes makes fouling and contamination likely. This configuration also allows for the amplifier to be exchanged without impacting the electrochemical cell.

A fluid well was constructed on the chip by attaching a cylindrical plastic tube with a diameter of 16 mm. The fluid well is attached to the chip using two-part silicone elastomer (WPI Kwik-Cast Sealant) to provide a water tight seal between the well and the chip, forming a liquid reservoir with total volume of $\approx$1 mL. A silver/silver chloride (Ag/AgCl) pellet electrode was connected to the V_{ref} voltage on the daughterboard. The electrode acts as a quasi-reference (both counter and reference) electrode for the redox measurement. Because the voltage of the gold working electrode is held to V_{mid} by the input amplifier feedback, the V_{ref} applied by the Ag/AgCl electrode controls the applied potential to the solution. This allows voltammetry waveforms to be applied by changing the DAC output voltage dynamically. A schematic representation of the experimental setup is shown in Figure 5.1.

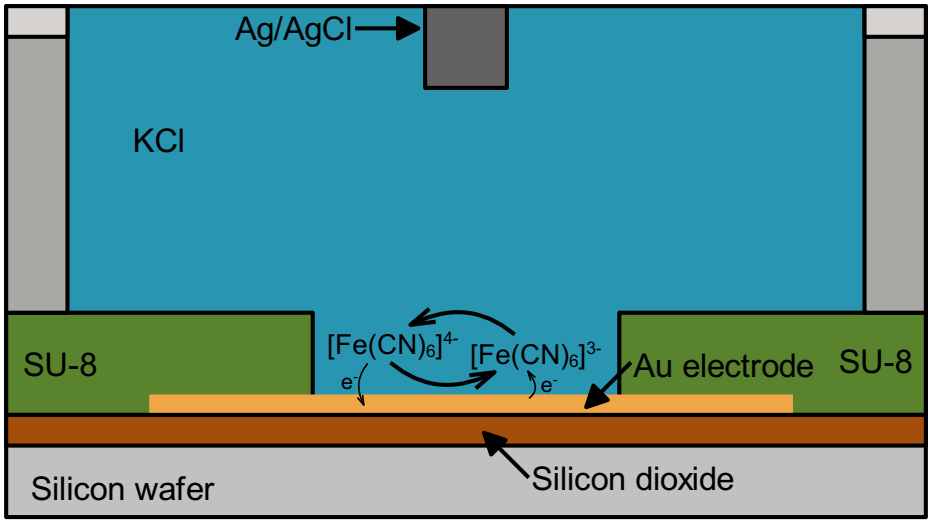


Figure 5.1: Schematic diagram with SU-8 microwell with gold UME for redox voltammetry

The supporting electrolyte for the measurements was created from 100 mM potassium chloride (KCl, Fisher Scientific) dissolved in distilled (DI) water, which was buffered to a pH 7.2 using 10 mM 3-(N-morpholino)propanesulfonic acid (MOPS, Fisher Scientific). Redox solutions were created from the KCl solution by addition of equal concentrations of potassium hexacyanoferrate (III) ($K_3[Fe(CN)_6]$, Fisher Scientific) and potassium hexacyanoferrate (II) ($K_4[Fe(CN)_6] \cdot 3\,H_2O$, Fisher Scientific).

Filling the electrode microwell with aqueous solution can be difficult due to the naturally hydrophobic nature of SU-8 photoresist and the small volume of the microwell. To avoid this issue, 100 µL of ethanol was first applied to the dry electrode chip. The low surface tension and hydrophobic groups of ethanol encourage wetting. The ethanol can then be replaced through repeated dilution with the experimental solution to guarantee proper wetting. Finally, the Ag/AgCl electrode was connected to the PCB for application of voltage stimuli, and the Faraday cage was closed around the electrochemical cell. The experiment was performed on a pneumatic anti-vibration table to protect against mechanical vibration which can cause triboelectric and piezoelectric noise. The FPGA and software interface are used for the real time observation of the current and voltage versus time, the power spectral density, and the voltammogram of sampled current versus voltage during the measurement.

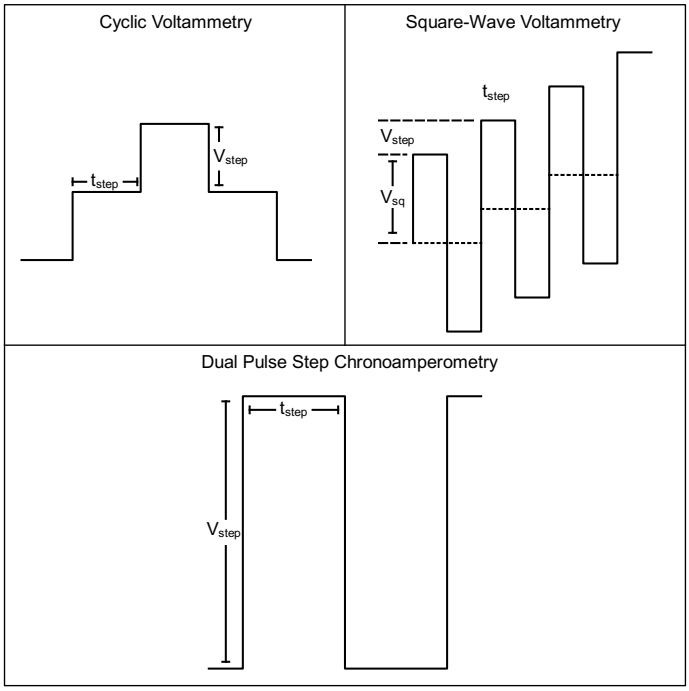


Figure 5.2: Voltammetry waveforms for CV, SWV and DPSCA measurements

5.3 Redox voltammetry

Voltammetry experiments were conducted to demonstrate the capabilities of the electrochemical amplifier for detection of low-concentration redox couples. Redox current was measured using step voltammetry, cyclic voltammetry (CV), and square-wave voltammetry (SWV). The waveforms used for the measurements are shown in Figure 5.2, and the operating parameters will be described for each method. Each voltammetry technique has specific benefits and hazards when used for ultra-low current measurements.

The expected redox potential for the measurements differs from the standard redox potential for hexacyanoferrate couple (HCF, $[Fe(CN)_6]^{3-/4-}$) due to different conditions. The $E^{0'}$ of HCF at the standard hydrogen electrode (SHE) is +0.3704 V [129]. The Ag/AgCl reaction occurs at a potential of +0.2223 V versus the SHE [130] which provides an offset when using the pellet electrode. The difference of these $E^{0'}$ values gives the expected redox potential of for HCF versus Ag/AgCl of +148.1 mV. Additionally, the half-wave potential ($E_{1/2}$) for a UME sampled voltammogram is slightly shifted from $E^{0'}$ [46]. The half-wave

potential can be determined from

$$E_{1/2} = E^{0'} + \frac{RT}{nF} \ln \frac{D_R}{D_O} \tag{5.1}$$

which results in an $E_{1/2}$ of $+145.9\,\text{mV}$.

5.3.1 Step voltammetry

The simplified waveform of step voltammetry provides several advantages for studying the redox current for very low concentrations. The single step conversion of the redox molecules is simpler to model through solution of the diffusion equation. The model can then be used to analyze measured step voltammetry of the redox couple. Additionally, the longer step times allow for the collection of higher resolution noise spectra compared to other voltammetry methods. Step voltammetry does suffer from the amount of charging current generated, as a result of the large step size. Additionally, the amplifier may experience nonlinear behavior or slewing as a result of the rapid changes of current at the input.

Step voltammetry measurements were performed for several different concentrations of HCF. The voltage waveform used was a double potential step chronoamperometry (DPSCA) waveform as seen in Figure 2.9 with a starting voltage of $0\,\text{V}$, a step size of $0.3\,\text{V}$, and a step time of $30\,\text{s}$. The use of a double pulse allows for the initial transient value to be subtracted for more consistent baseline. The $i(t)$ curves resulting from DPSCA measurements with several concentrations of HCF were recorded as shown in Figure 5.3. Based on the theoretical equations from Section 2.4, the current from a chronoamperometry step at a disk UME is

$$i(\tau) = i_d \underbrace{\left(\frac{\pi}{4} + \sqrt{\frac{\pi}{4}} \tau^{-1/2} + \left(1 - \frac{\pi}{4} \right) e^{-0.7823\tau^{-1/2}} \right)}_{f(\tau)} \tag{5.2}$$

where i_d is the steady-state current and $\tau = 4D_O t / r_0^2$ represents normalized time [47]. This equation shows that for single-step chronoamperometry, the redox current measured is in-

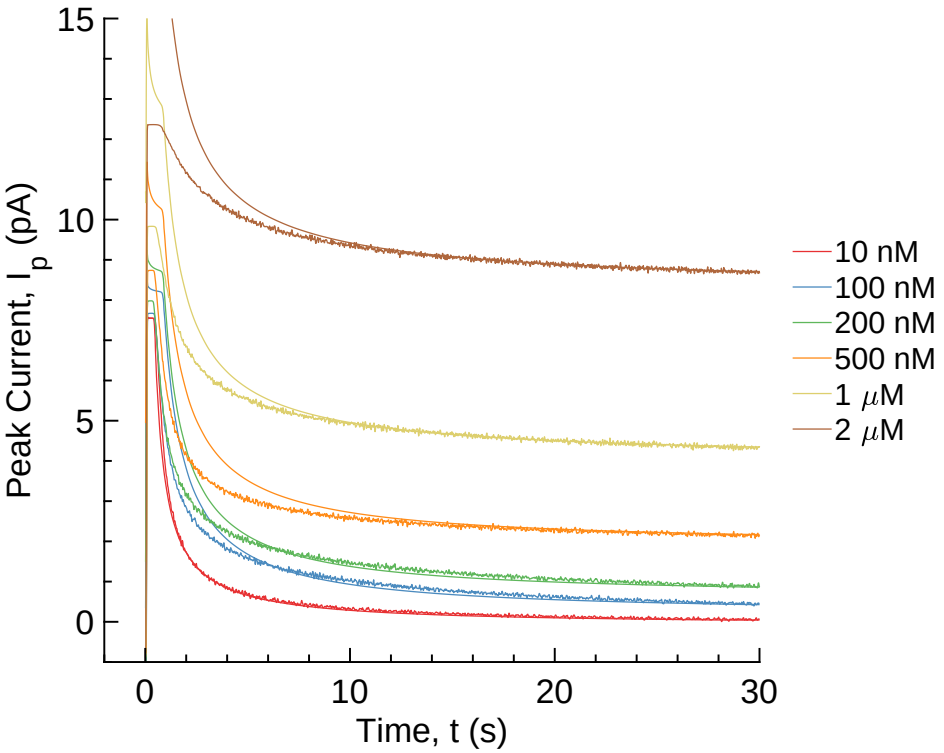


Figure 5.3: Step voltammetry $i(t)$ measurement and simulated response

dependent of applied potential and varies linearly with the bulk redox concentration C_O^*. Additionally, the redox current has an initial spike which converges to the steady state current i_d after τ becomes large. This equation can be used to analyze the change in redox current i with concentration C_O^*. The $i(t)$ data was sampled at $t_s = 30\,\text{s}$, and the resulting currents were plotted versus concentration of HCF in Figure 5.4. The current sampling allows (5.2) to be simplified to

$$\begin{aligned} i(t_s) &= i_d \times f(4D_O t_s/r_0^2)\Big|_{t_s=30\,\text{s}} \\ i(t_s) &= 4.3570\,\text{pA/µM} \times C_O^* \end{aligned} \tag{5.3}$$

This demonstrates that the current sampled from the $i(t)$ measurements has a linear relationship with the bulk concentration of the redox substrates. The sampled chronoamperometry data in Figure 5.4 was fit with a linear regression with a slope of $4.3331\,\text{pA/µM}$, which closely matches the theoretical value of $4.350\,\text{pA/µM}$. The selected data in this plot were

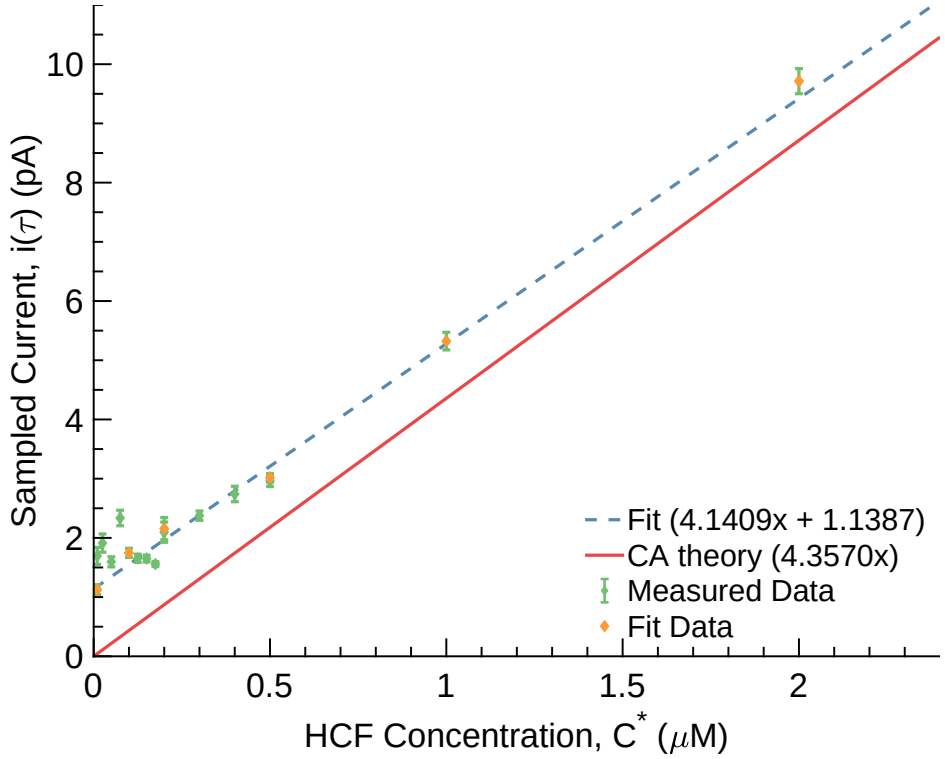


Figure 5.4: Step voltammetry sampled redox currents versus concentration

measured in an experiment performed with serial addition of HCF and are used for the linear regression shown in Figure 5.4.

5.3.2 Cyclic voltammetry

Cyclic voltammetry (CV) has several advantages when compared to DPSCA. The CV sweep results in a continuous sampled waveform which is not possible with step voltammetry alone. The CV waveform also creates charging current, but the use of smaller voltage steps than step voltammetry methods results in less charging current contribution per step. Since there is no cancellation of the charging current, the CV sweep rate must be slow enough to ensure that the Faradaic redox current dominates over the charging current. In this measurement, the voltage from working to reference electrode was varied continuously between $-0.1\,\mathrm{V}$ and $+0.4\,\mathrm{V}$ to capture the redox potential of HCF. The sweep rate v was set to $4.5\,\mathrm{mV/s}$ with a $1.5\,\mathrm{mV}$ step size, resulting in a step frequency of $3\,\mathrm{Hz}$. The low sweep rate and small radius of the UME result in decreased charging current when compared to

typical measurements.

The CV waveform, electrode radius, and electrochemical theory from Section 2.4 can be used to predict the redox current i_d. Steady-state behavior will dominate the CV current as long as the sweep rate satisfies

$$v \ll RTm_O/(nFr_0) \tag{5.4}$$

For this measurement, $RTm_O/(nFr_0)$ evaluates to 105.5 mV/s which is more than twenty times the CV sweep rate of 4.5 mV/s. Since the sweep rate is far below the limiting rate needed for transient behavior, the CV measurement will exhibit steady-state behavior, and the redox current for the voltammogram can be predicted with

$$\begin{aligned} i_d &= 4nFD_O C_O^* r_0 \\ i_d &= 4.2029\,\text{pA/µM} \times C_O^* \end{aligned} \tag{5.5}$$

This provides the theoretical sensitivity of the CV current to HCF concentration.

CV sweeps were performed with HCF concentrations ranging from 10 nM to 2 µM. The resulting cyclic voltammograms are shown for each concentration in Figure 5.5. These voltammograms show the expected sigmoidal shape that results from steady-state voltammetry at UMEs. The anodic sweep shows a predictable peak for at very low concentrations of HCF couple which prevents the typical blank experiment and originates from the Ag/AgCl reference electrode.

The cyclic voltammograms were fit through the use of linear regression on the plateau regions to extract redox current (i_d) and half-wave potential ($E_{1/2}$). The extracted half-wave potentials are shown in Table 5.1. The half-wave potentials vary, but are mostly centered near the predicted value of +145 mV for HCF couple at an Ag/AgCl electrode. The extracted i_d values are plotted versus concentration in Figure 5.6. The linear regression of the current values is shown and has a slope of 4.064 pA/µM, which closely matches the theoretical steady-

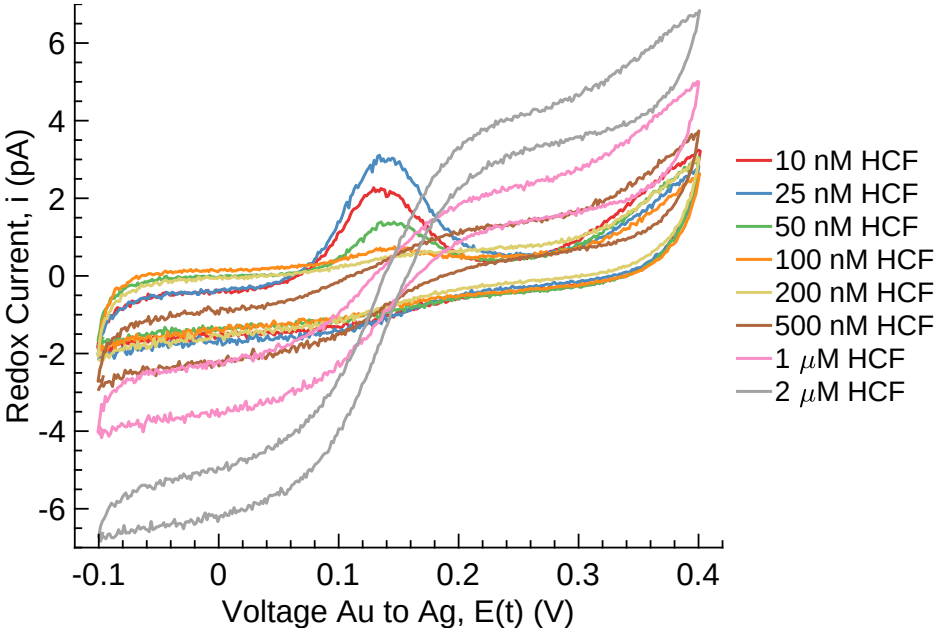


Figure 5.5: Selected cyclic voltammograms showing HCF redox couple from 10 nM to 2 µM concentration

Table 5.1: Half-wave potentials for each HCF concentration extracted from CV data

HCF Conc. (µM)	$E_{1/2}$ (V)	HCF Conc. (µM)	$E_{1/2}$ (V)
0.01	0.1594	0.2	0.139
0.01	0.1423	0.2	0.1522
0.025	0.1582	0.3	0.1453
0.05	0.1643	0.4	0.1432
0.075	0.161	0.5	0.1387
0.1	0.1413	0.5	0.14
0.125	0.1588	1	0.1385
0.15	0.1543	2	0.1393
0.175	0.155		

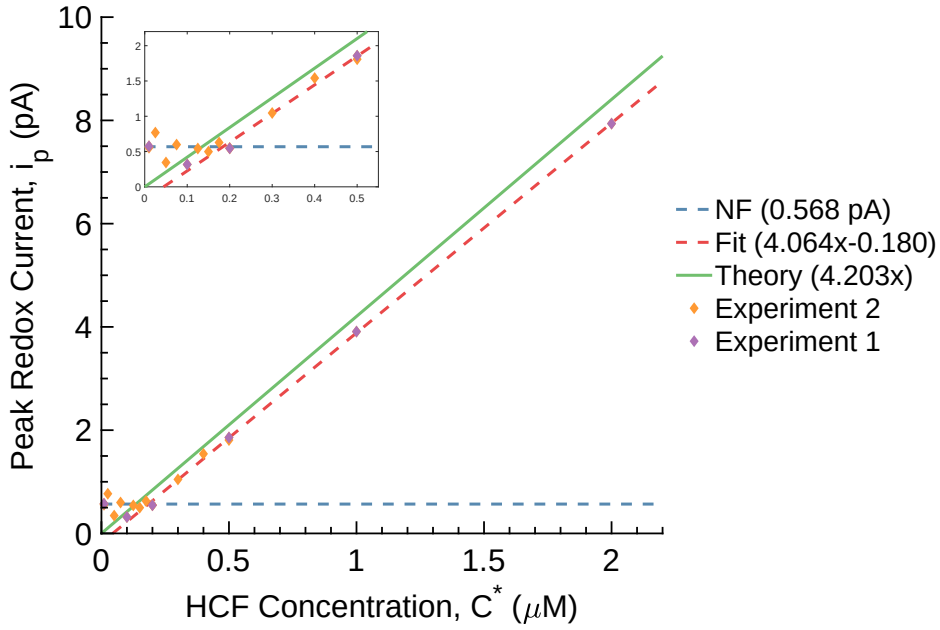


Figure 5.6: Cyclic voltammetry redox currents plotted versus concentration

state sensitivity 4.2029 pA/µM as predicted by (5.5). This sensitivity is used to predict the ferrocyanide diffusion coefficient by:

$$D_O = \frac{s}{4nFr_0} \tag{5.6}$$

$$= \frac{4.064\,\text{pA/µM}}{4F(1.5\times10^{-4}\,\text{cm})} \tag{5.7}$$

$$= 7.02\times10^{-6}\,\text{cm}^2/\text{s} \tag{5.8}$$

which matches well with the published value of $0.726\times10^{-5}\,\text{cm}^2/\text{s}$ [48].

Figure 5.6 shows the results of two different experiments. Experiment 1 began at low concentrations and increased, while experiment 2 started at high concentration and diluted sequentially. The average value of the low concentration data was used to set the measurement noise floor (NF), and measurements below the noise floor were not included in the linear fit.

To confirm the performance of the electrochemical amplifier, the same CV experiment was conducted with identical electrodes using the CH Instruments 760D potentiostat (CHI760D).

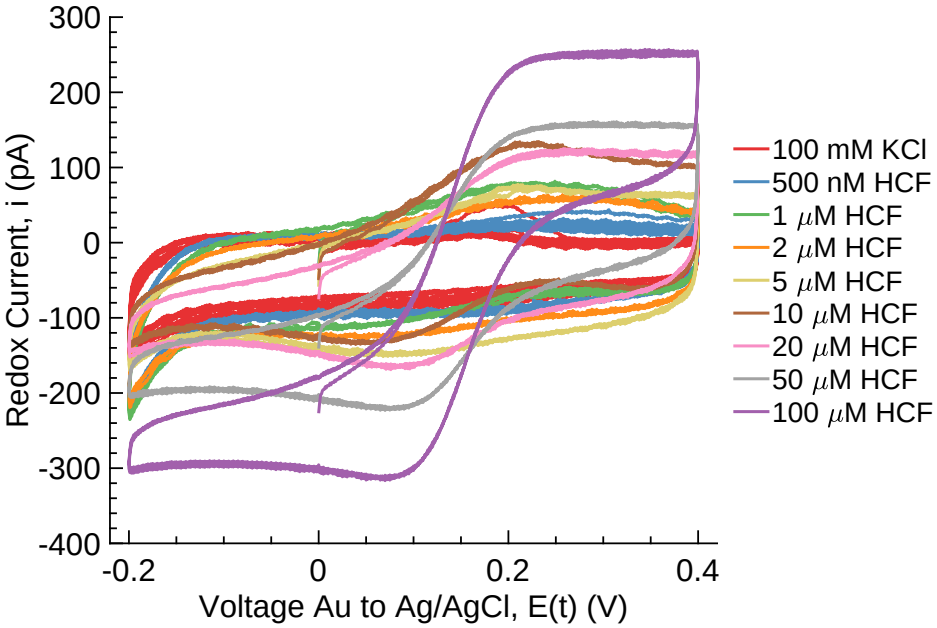


Figure 5.7: Cyclic voltammetry measurements conducted with the CHI760D

The cyclic voltammograms measured using the CHI760D and gold UME are shown in Figure 5.7. Redox currents were also extracted from these measurements using the CHI software and are plotted along with the theoretical steady-state current and the CV measurements from the CMOS electrochemical amplifier in Figure 5.8. The extracted currents from the CHI760D show a linear trend similar to the measured results, with a slope of 4.07 pA/µM. However, the CHI760D reaches a detection limit of 10 µM at current values of around 100 pA. The CMOS-integrated system reaches a detection limit of 100 nM at current values of around 300 fA. The detection limit seen in these voltammograms is constrained by various additional signals and noise that lead to the final performance.

The CV and SWV measurements revealed an anomalous current when measuring very low concentrations of HCF redox couple. When the redox concentration was lowered below 100 nM, a systematic peak would appear at a voltage just slightly below the typical peak redox potential of HCF. This peak appeared to increase as the concentration of the redox solution decreased and reached a maximum value of around 6 pA when tested using 100 mM KCl solution without HCF couple. This suggests that another redox reaction was occurring

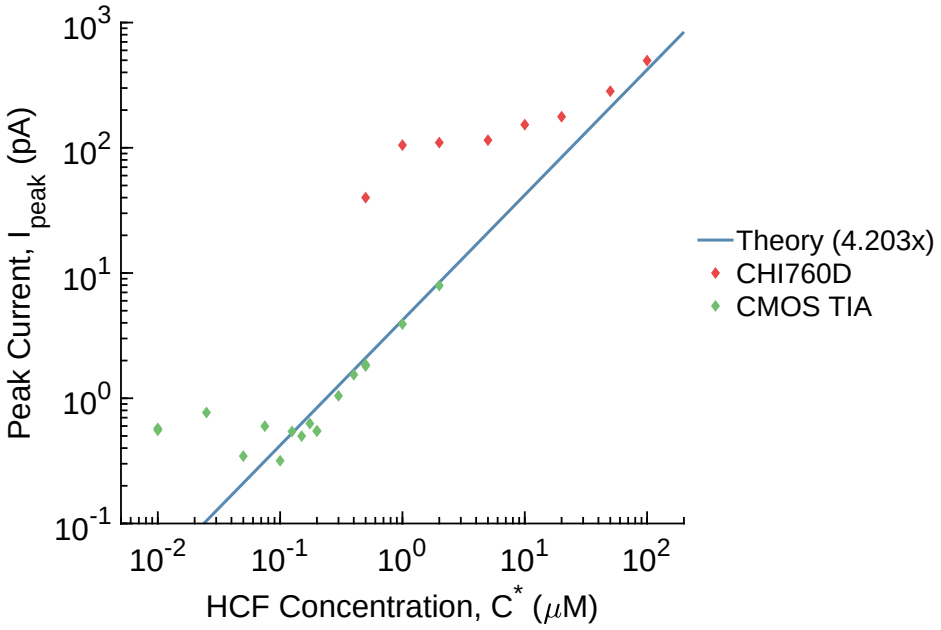


Figure 5.8: Cyclic voltammetry redox current compared with commercial potentiostat

alongside the HCF reaction, and this unknown reaction was unfavorable in the presence of high concentrations of HCF couple. The systematic peak appeared primarily in the anodic sweep when the voltage between the working and reference electrodes was increasing (See Figure 5.5). This systematic signal is likely due to the use of an Ag/AgCl reference electrode.

Many researchers work with very low concentration solutions measured using low noise electrochemical systems. In particular, nanopore array [131]–[133], nanogap [90], [134] and SECM [59], [84], [135] measurements require the use of a quasi-reference Ag/AgCl electrode to maintain a compact geometry and simplify the control electronics for the system. In such low concentrations and confined geometries, silver ions from the reference electrode can dissolve in the electrolyte solution. This results in a smaller redox current from silver as the ions are reduced to silver nanoparticles and then re-oxidized back into dissolved Ag^+ ion.

In an effort to avoid this complication, which likely accounts for the background signal seen in Figure 5.5, we employed an agar-filled agar bridge to separate the silver reference from the working electrode. This should prevent the contamination of the working electrode by silver nanoparticles or dissolved ions. The agar bridge was used to reduce in this back-

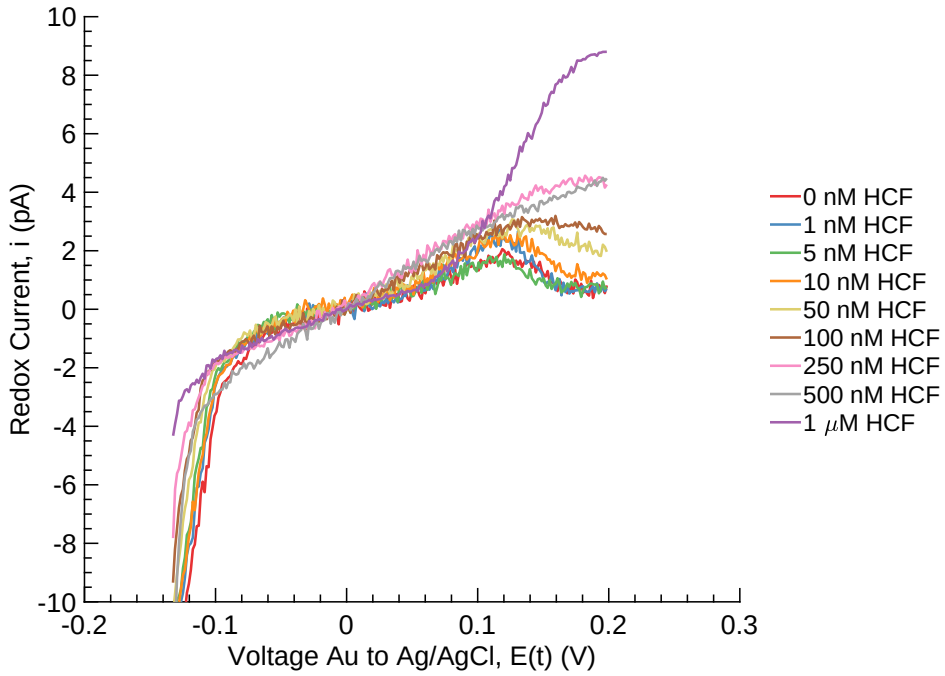


Figure 5.9: Cyclic voltammograms using agar bridge with HCF redox couple from 0 nM to 1000 nM concentration

ground signal in a further set of HCF concentration CVs. The resulting curves are shown in Figure 5.9. These results were able to show a much more predictable behavior without the additional current from the silver contamination. This enables the measurement of a blank experiment with only KCl in both agar bridge and fluid cells. However, these results also show interesting behavior at very low redox concentrations. In addition to eliminating the silver current, the agar bridge measurements reveal a change in behavior from the typical UME sigmoidal CV to a more Cottrellian, peaked response. This change in response complicates the results and requires use of further modeling to understand the redox chemistry involved, but these results were able to reduce noise and improve the detection limits further compared to the measurements without the bridge. More in depth discussion of these results with consideration for multiple sources of electrochemical interference will be presented in Section 5.4.2.

5.3.3 Square-wave voltammetry

Additional experiments were performed using SWV in a further effort to reduce detection limits. SWV is often a large improvement over the previous two voltammetry methods, due to the built-in cancellation of charging current. This cancellation should improve detection limits and produce a more idealized final curve without the charging current. However, these improvements are balanced by the reduced maximum current predicted by theory which is 0.75 times the CV steady-state current [136], [137]. This results in a steady-state maximum current of

$$i_d = 3nFD_O C_O^* r_0 \tag{5.9}$$

for SWV at a microdisc electrode. The SWV measurement should produce a flatter baseline curve as a result of the charging current cancellation. The square-wave waveform enables measurement of two simultaneous CV curves offset by $2V_{sq}$. At a UME, the sampled difference curve is a Gaussian which results from the difference of two offset sigmoids. This subtraction provides a reduction in the charging current contributed to the measurement, but this also results in increased noise from the summation of independent current noise from the two measured curves. Additionally, the large alternating waveform will use more of the output range of the amplifier, which limits the upper signal that can be measured and thus shrinks the dynamic range.

Equations for the peak current and the ratio of peak current to peak width have been derived to determine the optimal SWV parameters for experimental measurements at UMEs [136], [137]. The optimal parameters as calculated for a one-electron redox reaction are $V_{step} = 10\,\text{mV}$ and $V_{sq} = 50\,\text{mV}$ [136]. For this experiment, an SWV waveform with $v = 1.8\,\text{mV/s}$, $V_{step} = 4.5\,\text{mV}$, and $V_{sq} = 25\,\text{mV}$ was used, resulting in a $t_{step} = 800\,\text{ms}$. The decrease of V_{sq} from more optimal values was necessary to prevent overloading of the amplifier input from the increased charging current that is caused by the 50 mV square-wave steps, which

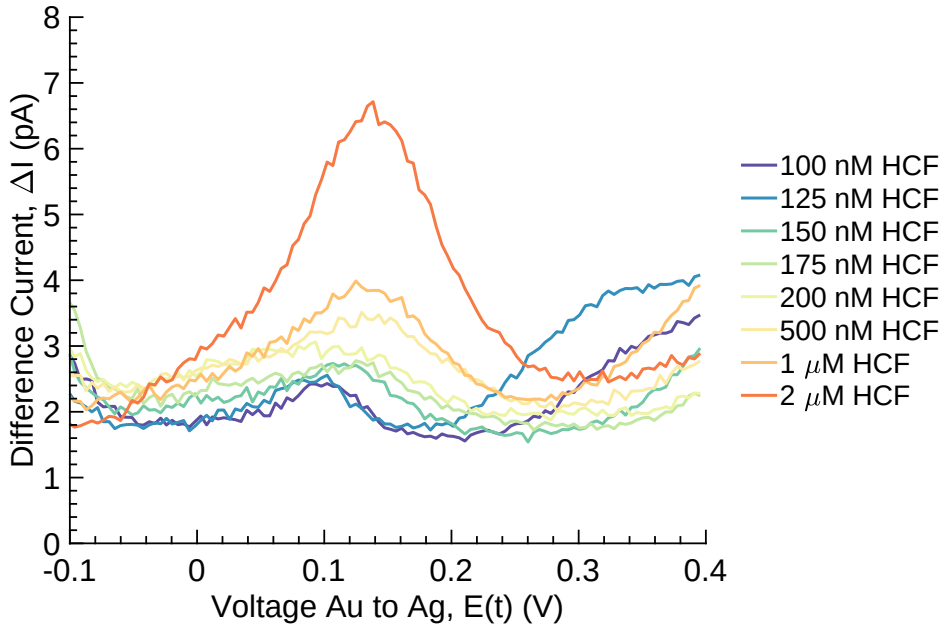


Figure 5.10: Voltammogram showing HCF redox couple from 100 nM to 2 µM concentration

are much larger than the CV V_{step} and more frequent than the steps for DPSCA. The SWV parameters are used to calculate the theoretical maximum current [136], [137], resulting in an expected peak current of $i_d = (2.324\,\text{pA/µM}) \times C_O^*$.

The resulting voltammograms with concentration of HCF of 100 nM to 2 µM are shown in Figure 5.10. The voltammograms were then fit using background subtraction based on third-order polynomial fitting. The peak current and peak voltage were extracted from the baseline subtracted data using a non-linear least squares Gaussian fit. Each data point was averaged from at least four independent measurements. The average peak potential and standard deviation are shown in Table 5.2 The extracted peak heights from multiple experimental trials were averaged and plotted together versus concentration in Figure 5.11. The noisy low concentration measurements were used as a guideline to choose data (Data sel.) for determining the measurement sensitivity. This SWV data was fit using a linear regression which shows a measured slope of 1.581 pA/µM. The peak current for SWV with these operating conditions was calculated [136] and resulted in a theoretical slope versus concentration of 2.324 pA/µM. The SWV measurement showed a current noise floor (NF)

Table 5.2: Average peak potential and standard deviation versus concentration for SWV measurements

HCF Conc. (µM)	E_p (V)	std(E_p)
0.01	0.162411	0.088854
0.02	0.102456	0.033621
0.05	0.108093	0.01539
0.1	0.1078	0.011451
0.2	0.125597	0.033085
0.5	0.128429	0.029918
1	0.138548	0.021974
2	0.128147	0.010413

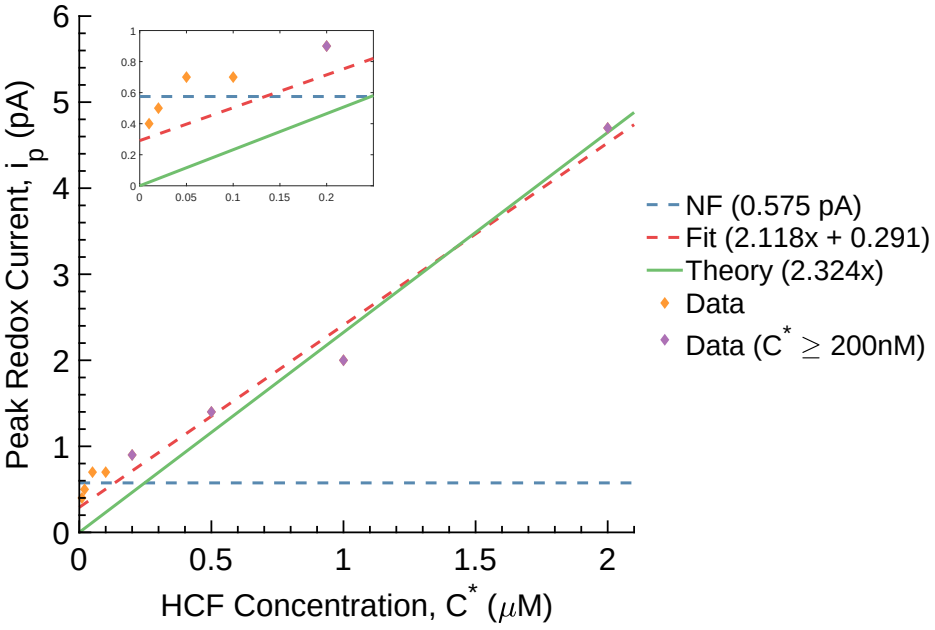


Figure 5.11: SWV peak currents extracted via Gaussian fitting and plotted versus concentration

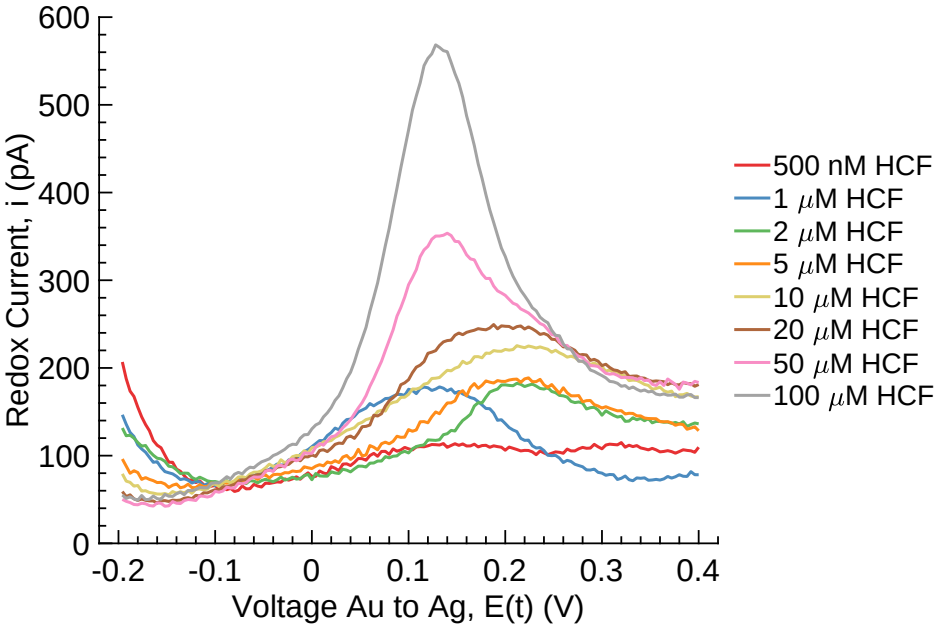


Figure 5.12: Square-wave voltammetry measurements conducted with the CHI760D

of 610 fA, which allowed detection of the redox solution at concentrations down to 500 nM.

The CHI760D was again used to validate the SWV measurements using the same electrodes and solutions. The CHI760D was used with $V_{step} = 4\,\text{mV}$, $V_{sq} = 25\,\text{mV}$, and $f = 15\,\text{Hz}$. This translates to an overall sweep rate of 60 mV/s and a theoretical current sensitivity of 4.76 pA/µM. The resulting SWV measurements are shown in Figure 5.12 and peak voltages and currents were extracted using the CHI software. The peak currents measured with the CHI amplifier are compared against the measurements using the CMOS TIA in Figure 5.13. The resulting SWV data has a slope of about 3.1 pA/µM for redox concentrations of 20 µM and above, which is significantly below the expected SWV current per concentration of 4.76 pA/µM However, the CHI760D data shows a measurement limit of around 30 pA for SWV measurements, which limits detection to concentrations of roughly 5 µM and higher. The CHI760D measurement shows that some limitations for the SWV measurement also stem from the electrodes themselves.

The current measurement limit is similar to the CV measurement, but the decreased current output per concentration and increased noise of SWV provide limitations on the

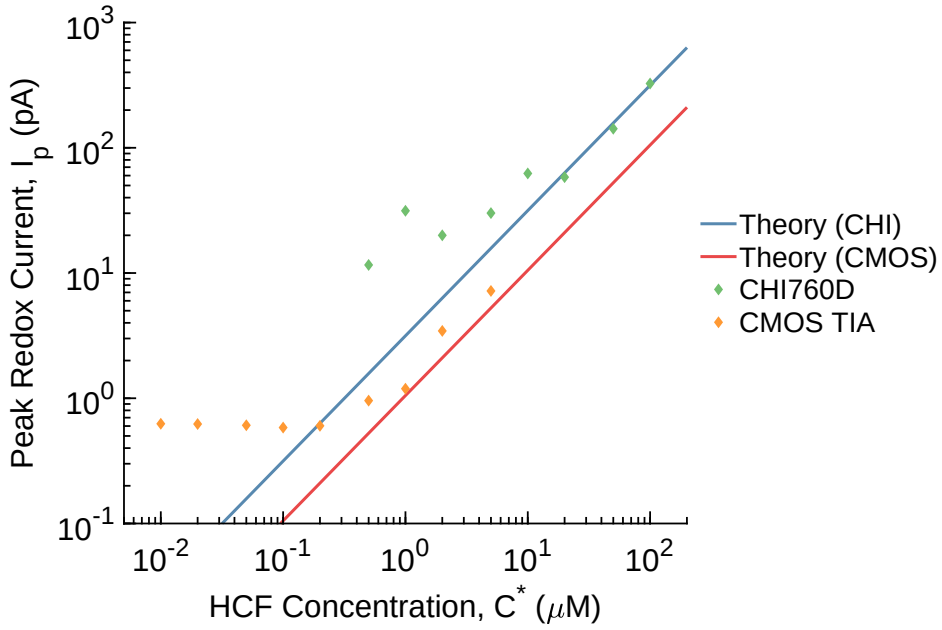


Figure 5.13: SWV measurements compared between CMOS TIA and CHI760D

detectable concentration. Several influences result in the discrepancies between the measured and theoretical slopes for both the CMOS TIA and the CHI760D. The large pulses from SWV resulted in some saturation of the amplifier at high and low input voltages. This saturation reduced the working range of the amplifier, causing the higher micromolar measurements to show reduced currents or non-linear response, since the amplifier is limited to 18 pA total. The SWV fitting algorithms underestimate the peak current for the TIA measurements, which decreases the observed slope. This fitting is less accurate, since the blank cannot be used as a baseline due to the silver background signal addressed previously. Additionally, the silver current persists at low concentrations of HCF, which makes resolving different values more difficult.

The SWV measurement did not provide much benefit over the CV voltammetry, due to the stringent requirements needed to achieve high SNR. The next section will explore the noise and measurement limitations that result in the limits of detection demonstrated in voltammetry measurements by the electrochemical system.

5.4 Redox Detection Limitations

The overall electrochemical system is limited in the redox concentration that can be detected. This can be seen in Figure 5.8 and Figure 5.13, where the current measured reaches a static limit after reaching the lower limit. This limitation is due to several different sources that result in current that does not come directly from the redox reaction of hexacyanoferrate. This section will address the most prominent signals which result in the limit of detection. In particular, electrical and electrochemical noise, diffusion and surface effects, and secondary reactions will be highlighted to explain how these create the total limit of detection seen in the voltammetry results.

5.4.1 Electrochemical noise

The electrode-electrolyte interface has associated noise that can impact the measurement of very low concentrations of redox substrates. The CMOS amplifier system was used to measure electrochemical signals with low electronic noise, which allowed for observation of electrochemical noise. However, the dynamic voltage waveforms of voltammetry complicate analysis of this noise, since noise analysis is typically performed in the frequency domain. The periodic voltage changes used for voltammetry limit the frequency resolution for noise spectra while also causing a constantly changing baseline and high-frequency noise that is difficult to separate from the signal. Since the voltammetry measurements presented here are dominated by steady-state behavior starting very shortly after each voltage change, the redox current noise can be analyzed using static noise measurements. Detailed static noise was recorded at fixed applied voltages for both dry electronic conditions and wet conditions with redox and KCl solutions. These static noise measurements can then be used to model the dynamic behavior through frequency domain analysis.

Solution		V_{bias}	R_b	R_{ct}	C_{DL}
100 mM KCl	1 µM HCF	0.1 V	8396 Ω	30.2 GΩ	300 pF

Solution	C_H	V_{bias}	R_b	R_D	C_D
100 mM KCl	241 pF	0 V	5853 Ω	43.8 kΩ	52.4 pF

Table 5.3: EIS parameters extracted from electrode impedance measurements

Electrochemical impedance spectroscopy

Electrochemical impedance spectroscopy (EIS) was used to understand and model the behavior of the electrode-electrolyte interface. EIS measurements enable the use of circuit components to model the electronic behaviors at the electrode and is also necessary to simulate the expected noise current of both electronic and electrochemical systems.

To perform EIS, a potentiostat is used to apply a small sinusoidal voltage with variable frequency to the electrochemical cell while measuring the current to determine the AC impedance. The electrodes and electrolyte were connected to the CHI760D in the same configuration as in the voltammetry experiments. EIS measurements were performed with a frequency range of 0.01 Hz to 10 MHz for both Faradaic and non-Faradaic conditions using solution with and without redox molecules. The Randles and IPE models as shown in Section 2.4.5 were fit to the electrode impedance data, and the resulting extracted parameters are shown in Table 5.3. The Warburg impedance Z_W of the Randles model was neglected for these measurements, since for UMEs at low frequency Z_W will be relatively small when compared to the charge transfer resistance R_{ct}.

One limitation of the EIS modeling is that the models only are appropriate to use as long as the voltage and electrochemical conditions used to extract the values are maintained. Therefore while the model can have a different large voltage applied to it, the model parameters will no longer remain valid under alternative conditions. This limitations makes it difficult to utilize the model when applying large step voltages as in step voltammetry or

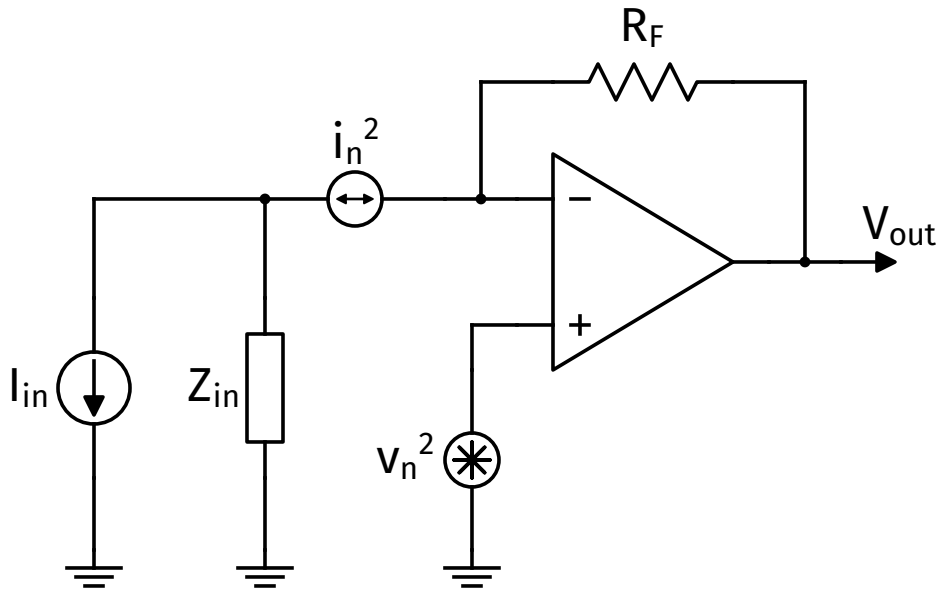


Figure 5.14: TIA schematic noise contributors with unknown input impedance

square-wave voltammetry and even the changing voltage of CV should result in a model that is only valid for a small area around the initial bias. A more complete empirical or theoretical model needs to be derived in order to use more extreme voltage variations, such as the SWV model derived by Dauphin-Ducharme, et al. [81]. However, the Randles and IPE EIS models can be used to evaluate the near steady-state behavior of the electrode-electrolyte system.

The measured static noise spectra were analyzed using a combination of these EIS models and noise simulations. The extracted EIS data was used with an analytical noise model derived from both electrochemical mass transfer equations and the contributions of Poisson and Langevin noise sources [50], [99]. The model and impedance data can then be used to predict the theoretical noise spectra at the electrode interface. Additionally, the electrochemical noise model was connected to the CMOS amplifier in Cadence Spectre circuit simulations to generate noise spectra for the complete system. The measured, modeled, and analytical noise spectra are presented and examined for different measurement conditions.

The noise of the electrochemical measurement can be predicted using circuit noise models and the extracted EIS values. A generalized noise model for TIA measurement of an unknown impedance is shown in Figure 5.14. The noise current for this configuration is given by

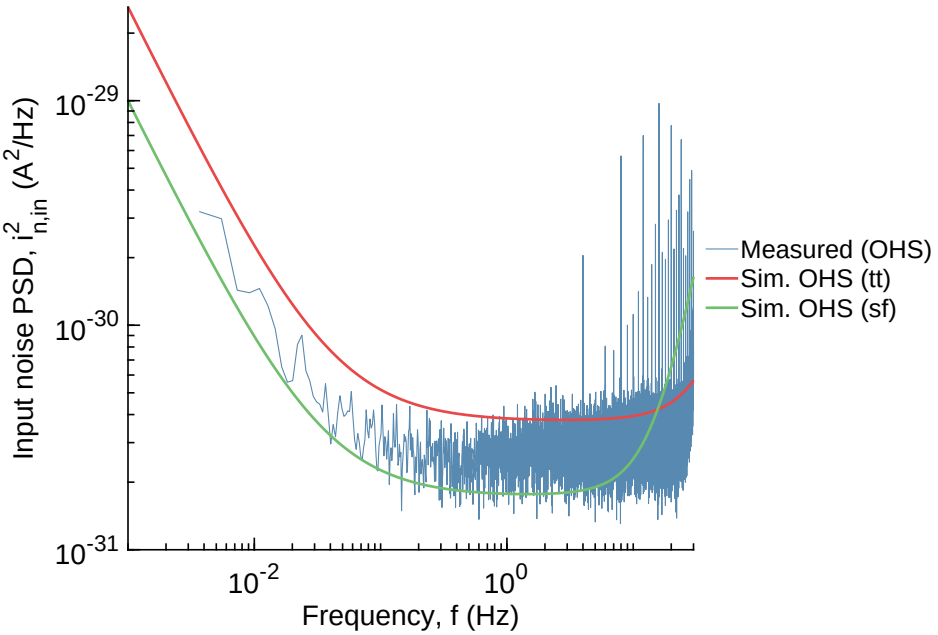


Figure 5.15: Noise power spectral density for open-headstage versus simulation

$$S_n(f) = S_i(f) + S_v(f)/|Z_{in}(f)|^2 + 4k_BT\,\mathrm{Re}\{1/Z_{in}(f)\} + 4k_BT/R_F \tag{5.10}$$

which includes the OTA current $S_i(f)$ and voltage noise power $S_v(f)$ along with the thermal noise of the input impedance Z_{in} and feedback resistance R_F. This basic model serves as a starting point for analyzing the noise of the electrochemical measurement.

Open-headstage noise

The input-referred, open-headstage noise was measured for the amplifier without electrodes or solution connected. In this configuration, the input load includes only parasitic components of the circuit board. The noise power spectral density of the open-headstage noise is shown in Figure 5.15. The open-headstage configuration was simulated without any input load for the amplifier schematic, as most board resistance and capacitance should be mitigated by the input shielding. The circuit simulator will add a required minimum conductance $g_{\min}$ which was set to 10 fS. Noise simulations were performed across all PVT corners to determine the closest match for the amplifier process corner. The noise spectra

for the nominal (tt) and slow-fast (sf) process corners most closely matched the measured open-circuit noise. The tt corner spectrum has integrated noise from 1 mHz to 3.5 Hz of $1.247\,\mathrm{fA_{rms}}$, while the sf corner spectrum has an integrated noise of $0.885\,\mathrm{fA_{rms}}$. The measured integrated current noise over the same bandwidth is $0.980\,\mathrm{fA_{rms}}$, which shows that the PVT region for the chip is between the tt and sf corners.

To analyze the noise spectrum, the noise contributions are broken down as shown in (5.10). Since no input load is used for the open-headstage configuration, the thermal noise is dominated by the noise of the feedback resistor R_F which has PSD of

$$S_n(f) = 4kT/R_F = 2.27 \times 10^{-31}\,\mathrm{A^2/Hz} \tag{5.11}$$

for R_F of 72.4 GΩ. The measured noise power spectral density has a floor between 0.5 Hz and 2 Hz with PSD of $2.21 \times 10^{-31}\,\mathrm{A^2/Hz}$, which matches up with the expected thermal noise of R_F. The OTA noise contributions of $S_i(f)$ and $S_v(f)$ can be determined from the circuit schematic or simulation. The current noise of an OTA should be fairly low since there is almost zero input current, but some current noise from the output will be referred to the input. The OTA current noise power was simulated using an ideal feedback network and the resulting spectrum is shown in Figure 5.16. This spectrum is dominated by $1/f$ noise, but some f noise appears above 8 Hz due to the feedback pole caused by $R_F \approx 43.1\,\mathrm{G\Omega}$ and $C_F = 453\,\mathrm{fF}$. The simulated OTA voltage noise power is shown in Figure 5.17. The voltage noise has both flicker and thermal components, however the flicker noise corner is around 10 kHz resulting in a relevant spectrum of entirely flicker noise. The OTA voltage noise power can be approximated by

$$S_v(f) = (1.2247 \times 10^{-11}\,\mathrm{V^2/Hz}) \times f^{-1.0656} \tag{5.12}$$

Since there is no input impedance, the current noise resulting from $v_n(f)$ will appear across

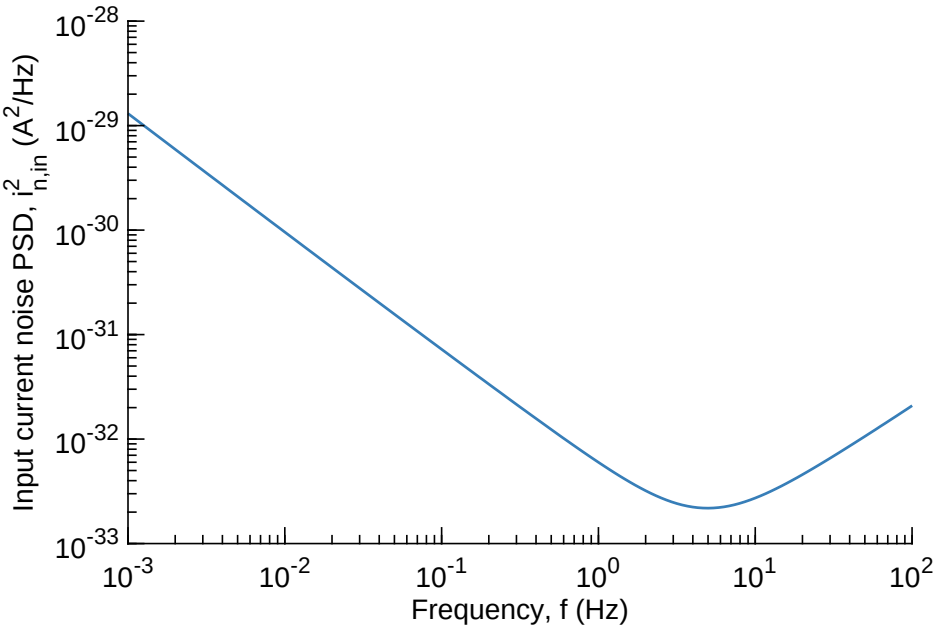


Figure 5.16: Simulated input current noise power spectral density of CMOS OTA

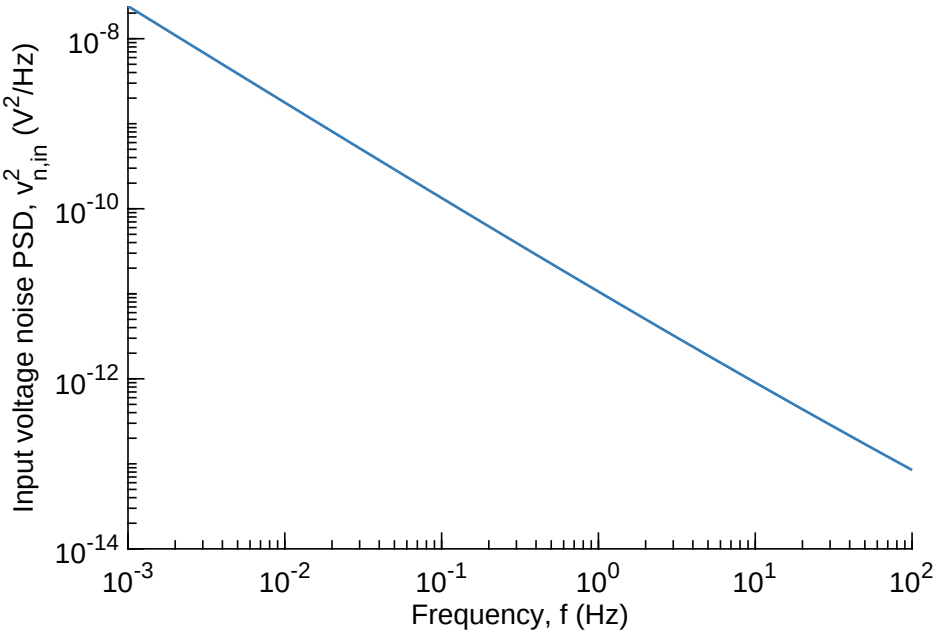


Figure 5.17: Simulated input voltage noise power spectral density of CMOS OTA

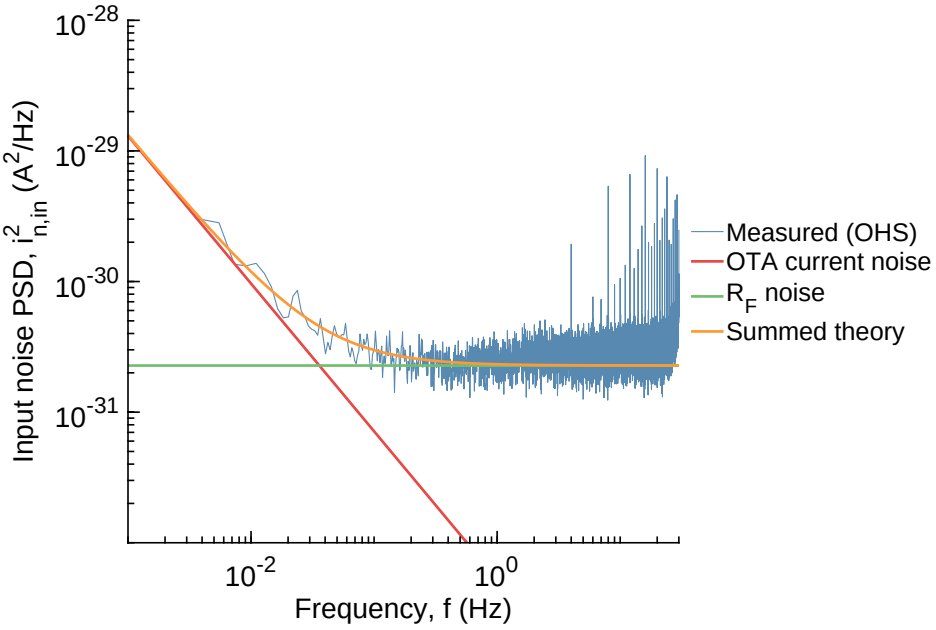


Figure 5.18: Measured open-headstage noise power spectral density with theoretical spectrum

$g_{\min}$ as

$$\begin{aligned} S_n(f) &= S_v(f)/|Z_{in}|^2 \\ &= g_{\min} S_v(f) \\ &= (1.2247 \times 10^{-39}\,\mathrm{A}^2/\mathrm{Hz}) \times f^{-1.0656} \end{aligned} \tag{5.13}$$

which is much smaller than the noise of $S_i(f)$ and can be neglected. Each of these noise contributions are shown along with the sum of all contributions and the measured open-headstage noise in Figure 5.18.

Test resistor noise

The dry circuit noise was also measured for the amplifier connected through the test resistor R_{test} to the DAC reference voltage V_{ref}. The input-referred noise PSD for the R_{test} configuration is shown in Figure 5.19. For the corresponding noise simulation, the amplifier input was connected to a 10 GΩ resistor connected to a voltage source as well as 15 pF

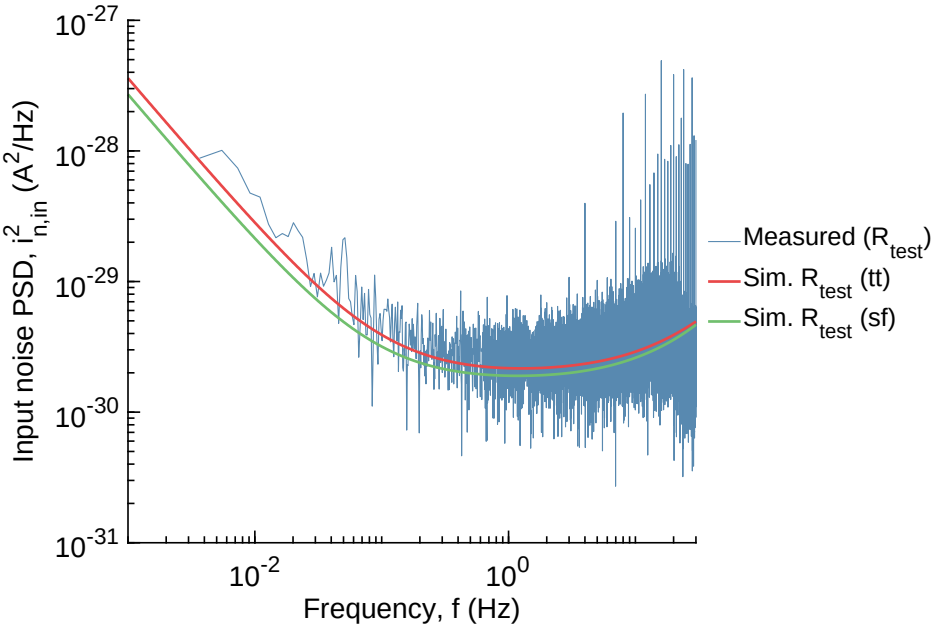


Figure 5.19: Noise power spectral density for R_{test} configuration compared to simulation

capacitor. The capacitor accounts for the mount used to attach the test resistor to the TIA input as well as any stray capacitance that the resistor presents. The simulated noise for the tt and sf corners matches up reasonably with the measured noise spectrum of the R_{test} setup.

The noise analysis for the R_{test} configuration is similar to the open-headstage case with the R_{test} appearing in parallel with R_F. The real part of the input impedance in this configuration should be

$$\begin{aligned} R_{in} &= R_{test} \parallel R_F \\ &= 9.44\,\mathrm{G\Omega} \end{aligned} \tag{5.14}$$

This results in a noise PSD of $1.74 \times 10^{-30}\,\mathrm{A^2/Hz}$, which corresponds with the measured noise PSD of $1.74 \times 10^{-30}\,\mathrm{A^2/Hz}$. The OTA voltage noise does have noise contribution with

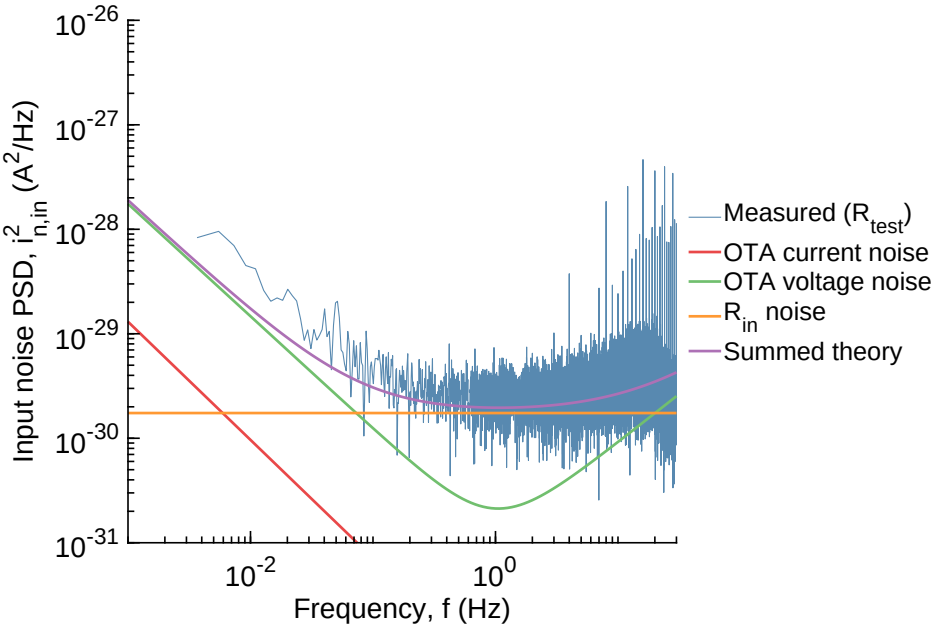


Figure 5.20: Measured R_{test} noise power spectral density with theoretical spectrum

R_{test} and C_{in} appearing as load impedance and can be calculated using

$$\begin{aligned} S_n(f) &= S_v(f)/|Z_{in}^2| \\ &= S_v(f)\left|\frac{1+2\pi f C_{in} R_{test}}{R_{test}}\right|^2 \\ &= S_v(f)\frac{R_{test}^2(1-4\pi f^2 C_{in}^2 R_{test}^2)}{(1+4\pi f^2 C_{in}^2 R_{test}^2)^2} \end{aligned} \tag{5.15}$$

The OTA current noise $S_i(f)$ is also included and the complete spectra are shown with the measured data in Figure 5.20.

Electrolyte noise

The noise measurement was replicated using working and quasi-reference electrodes connected to solution of 100 mM KCl and 10 mM MOPS to replicate the conditions for redox-free voltammetry. The resulting noise plot is shown in Figure 5.21. The IPE noise model shown previously in Figure 2.13 was used to perform the noise simulation, along with the EIS parameters for the IPE model from Table 5.3. This simulation shows reasonable alignment

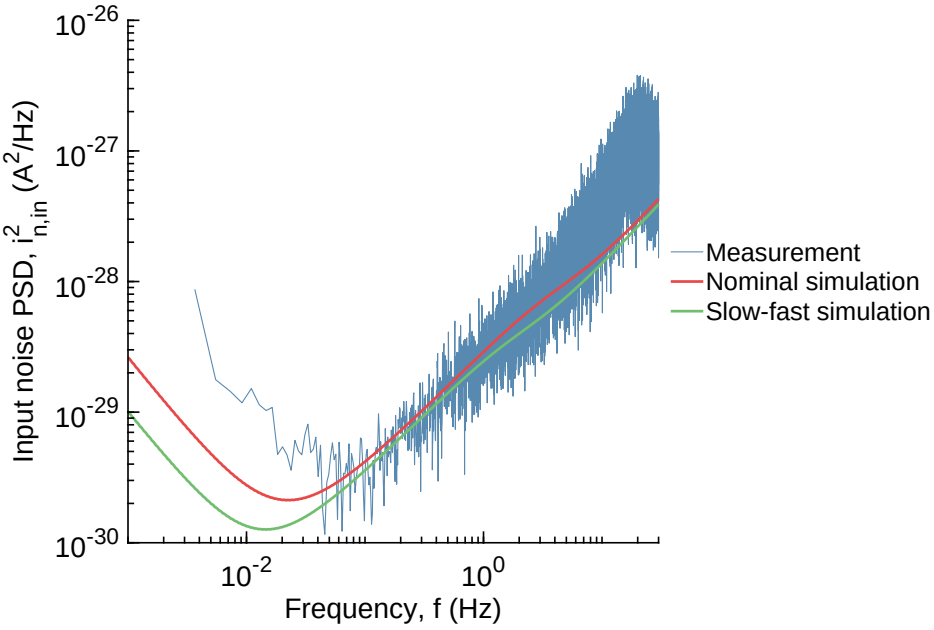


Figure 5.21: Noise power spectral density for KCl solution compared to simulation

with the measured noise data, with increased noise at low frequencies. This extra low frequency noise is likely a result of the Ag contamination which could cause some noise due to the redox reaction even without applied voltage.

The KCl electrochemical noise measurement is heavily dominated by f noise at frequencies of 0.3 Hz and higher. This noise is a result of current noise from the input voltage noise power of the OTA $S_v(f)$ being integrated by the input capacitance C_{in}. Above 0.3 Hz, Z_{in} is dominated by C_{in} of the IPE noise model, so the PSD resulting from the voltage noise can be estimated by

$$\begin{aligned} S_n(f) &= (2\pi C_{in})^2 S_v(f) f^2 \\ &= (1.22 \times 10^{-11}\,\mathrm{A}^2/\mathrm{Hz})(2\pi C_{in})^2 f^{0.9344} \end{aligned} \tag{5.16}$$

The f-noise spectrum can be used with C_{in} given by the EIS parameters to fit the measured noise spectra. The complete noise spectrum can be estimated from theory using (5.10) with

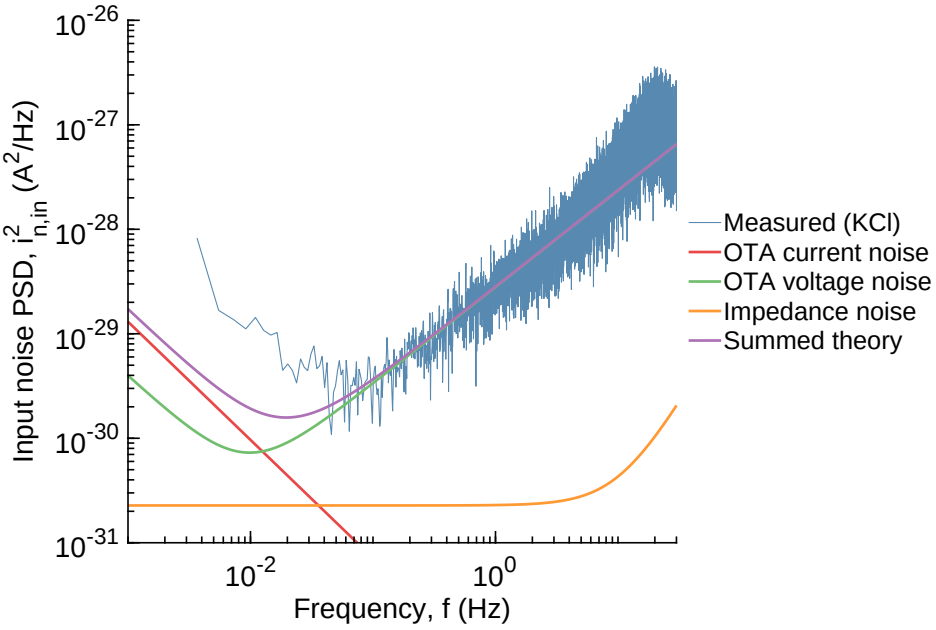


Figure 5.22: Measured KCl noise power spectral density with theoretical spectrum

the EIS parameters.

$$S_n(f) = S_i(f) + S_v(f)/|Z_{ipe}(f)|^2 + 4k_BT\,\mathrm{Re}\{1/Z_{ipe}(f)\} + 4k_BT/R_F \tag{5.17}$$

This noise spectrum is shown together with the measured data in Figure 5.22.

Redox noise

The noise measurement was then performed using solution of 100 mM KCl and 10 mM MOPS, with 1 µM HCF. The resulting noise plot is shown in Figure 5.23. The Randles model and representative noise sources for the simulation were included according to the noise model presented in Figure 2.14 and the redox EIS values from Table 5.3. The redox noise simulation has good alignment with the simulated results.

The theory noise contributions can be derived as in the above KCl analysis by starting with (5.10). However, the noise theory from Section 2.5 does influence this analysis. The presence of redox substrates in the solution results in an alteration of the noise sources. The

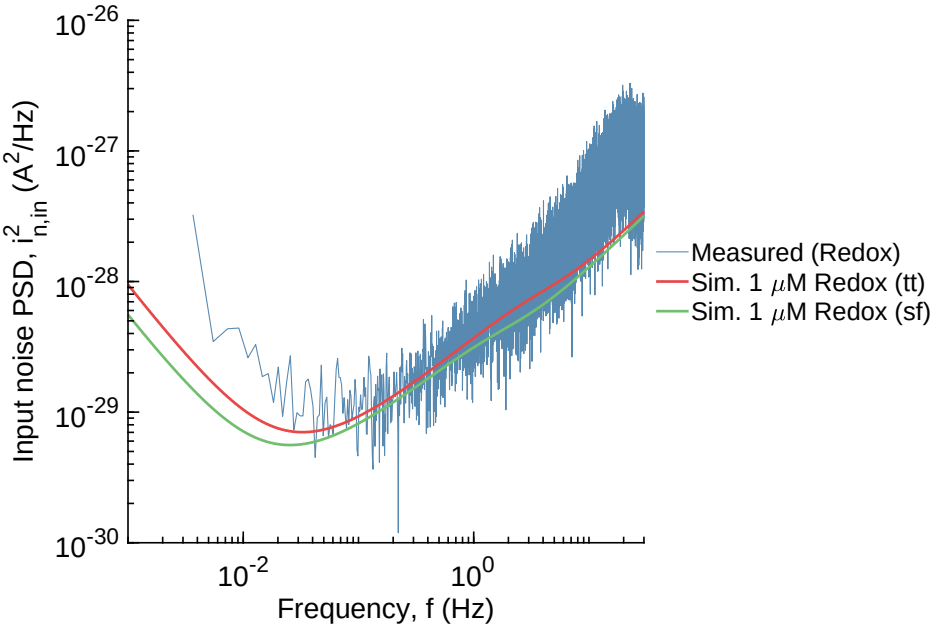


Figure 5.23: Noise power spectral density for redox solution compared with simulation

complete spectrum referred to the input of the OTA is instead given by

$$S_n(f) = S_i(f) + S_v(f)/|Z_{rand}(f)|^2 + 4k_BTR_b/|Z_{rand}(f)|^2 + 4k_BT/R_F + 2qI_p\frac{Z_{rand} - R_b}{Z_{rand}} \tag{5.18}$$

The noise created by the Faradaic impedance of $R_{ct} \parallel C_{DL}$ is given by the shot noise of the redox current [50], [99], while the current noise contribution of R_b is included separately. This theoretical redox noise spectrum is shown together with the measured data in Figure 5.24.

Noise aliasing

Noise from the CV sampling can result from aliasing of the higher frequencies back into the bandwidth of interest. The CV is classically constructed from a ramp voltage that alternates and a current measurement that records the response of the system. However, in modern applications, the ramp is typically constructed using a DAC to apply the voltage and therefore results in a staircase pattern. This is not an issue generally, since the input steps can be made very small and the sampling frequency can be set much higher than any signal

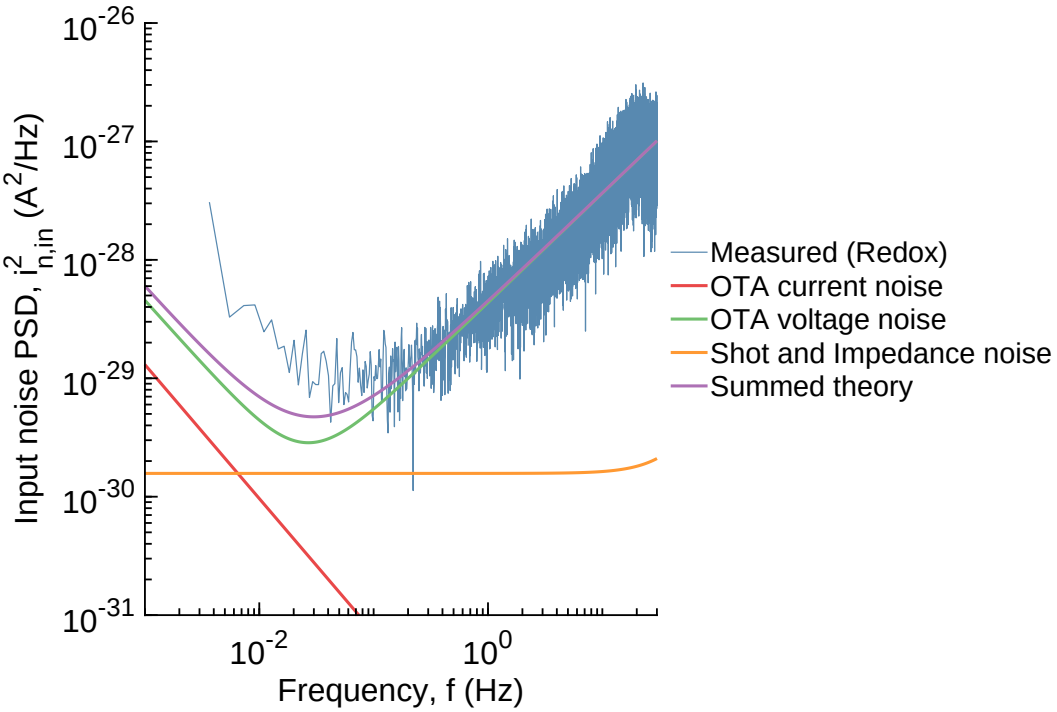


Figure 5.24: Measured redox noise power spectral density with theoretical spectrum

of interest. Therefore the noise of the charging current will end up averaged into the data, but this current should be a small fraction of the output signal. However, in this system, the sampling frequency is quite low due to the limitations of the amplifier bandwidth. In order to get enough samples to describe the output current, the DAC staircase has to be run at very low frequencies. In these measurements, the 3 Hz staircase voltage input falls within band, and therefore, must be handled separately to avoid aliasing significant noise back into the desired signal. We can compare the performance of the system with simple 3 Hz decimation to digital low-pass filtering of the data. The results show that while low-pass filtering may prevent the aliasing noise, it also folds the spikes from the charging current back in, creating a periodic signal in the filtered data.

Instead a selective sampling and filtering process was used to get better noise performance without low pass filtering below the DAC step rate. In this process, several points are sampled from the current trace before each voltage step. The sampled points are then smoothed using the multiscale local polynomial transform, which removes more of the noise caused by the

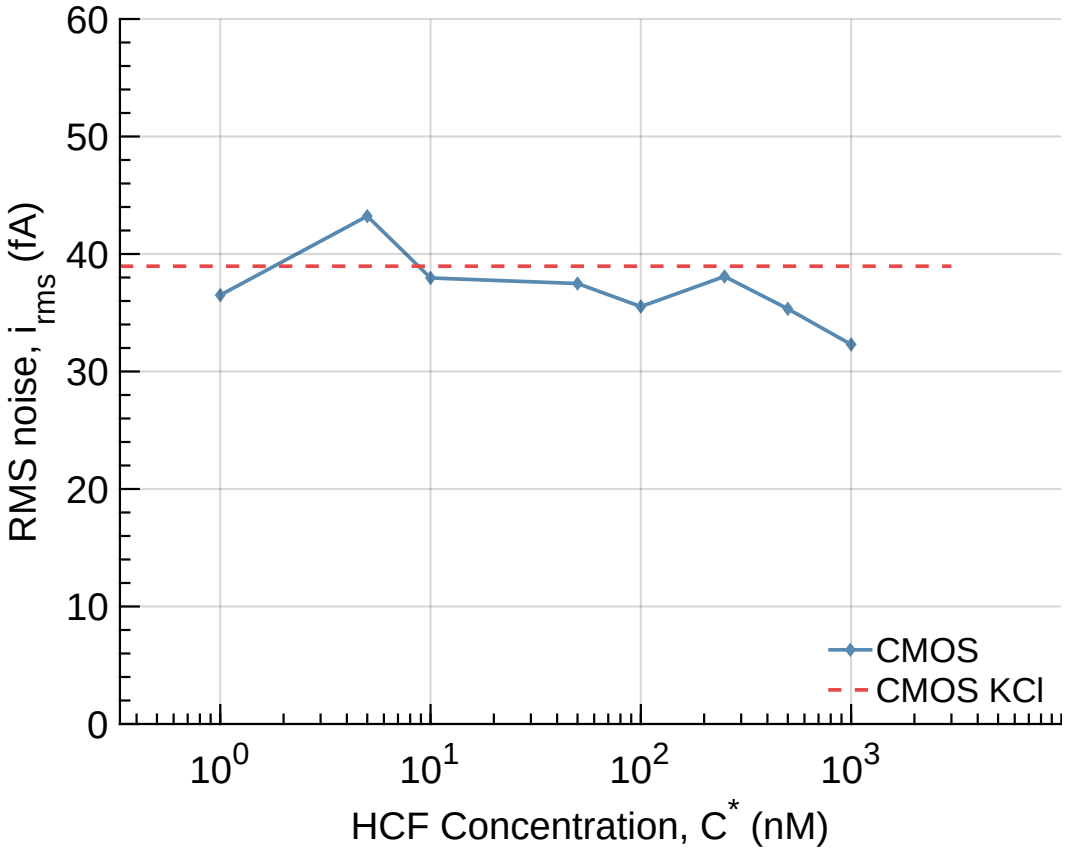


Figure 5.25: Measured steady-state and CV noise versus concentration, integrated over the CMOS TIA bandwidth

staircase voltage and operates across the non-uniformly sampled data. The resulting CV curves have reduced aliasing noise as well as decreased noise from the staircase voltage stimulus.

To understand the noise impact of this process, the CV curve data and steady-state noise were processed using the same techniques. The data was also bandpass filtered using a digital infinite impulse response (IIR) filter to remove the low frequency baseline from the CV curves. The noise was then integrated up to the 3.5 Hz bandwidth of the amplifier system. The resulting noise is shown in Figure 5.25 compared with HCF concentration. The steady-state noise measured in KCl-only solution is shown as a dashed line, which occupies a similar noise level to the noise from the CV curves. This shows that the steady-state noise represents the noise observed in the CV as long as the effects of the staircase voltage and

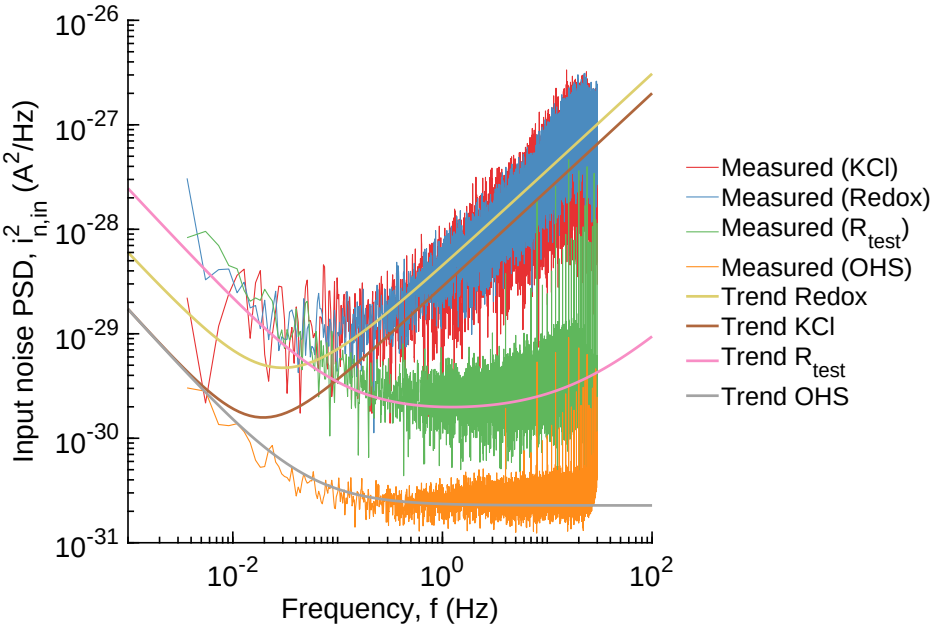


Figure 5.26: Measured noise spectra of all electrochemical measurements with analytical noise models

noise aliasing are dealt with properly.

Noise summary

The measured noise spectra are summarized with the analytical spectra in Figure 5.26 and the integrated root-mean-square noise is shown for the measured spectra in Figure 5.27. The dry measurements of the open-headstage and R_{test} noise provide a framework for understanding the wet electrochemical noise. The open-headstage noise provides a baseline for the dry noise measurement, as the only noise sources included are those internal to the chip and any unshielded PCB parasitic resistance. This noise is effectively described by the combination of the intrinsic OTA current noise combined with the feedback resistor thermal noise. The R_{test} noise measurement also remains close to expected electrical noise theory. The largest noise contributor is the thermal noise of the test resistor, which contributes noise PSD of $1.516 \times 10^{-30}\,\mathrm{A}^2/\mathrm{Hz}$. The voltage noise of the OTA can clearly seen to contributes significantly to the $1/f$ noise for this spectrum. The increased $1/f$ noise compared to the theory is likely the result of input offset voltage which creates a small current in R_{test} even

Table 5.4: Integrated input-referred root-mean-square noise for measured noise spectra

	0.1 Hz	1 Hz	3.5 Hz
OHS	0.228	0.529	0.980
R_{test}	1.20	2.01	3.30
KCl	1.26	4.91	15.1
Redox	1.28	5.07	15.2

at an applied bias of 0 V. Overall, the noise spectra of the dry components matches up reasonably with the simulation and theory.

The solid behavior of the dry electrical noise helps to characterize the electrochemical noise measurements. The behavior of the KCl and redox measured noise spectra appear similar, which would not be expected given the different solutions and different electrochemical models used. The redox measurement does exhibit slightly more noise than the KCl spectrum in the $1/f$ regime, which may indicate a higher input current to the TIA which could increase the flicker current noise. This supports the probability of a low-level redox current in the KCl solution resulting in increased noise, but less overall current compared to the solution of 1 µM HCF. The similarity of the two electrochemical measurements is clarified by the analytical noise model, which shows that the high capacitance of the electrode-electrolyte interface and the voltage noise of the OTA together cause the f noise that dominates the spectra. The impact of C_{DL} on the electrochemical noise is also apparent from the rapid growth of the integrated root-mean-square noise above 1 Hz, as shown in Figure 5.27. The noise of the electrochemical interface is dominated by f noise which results directly from the high input capacitance.

While this noise decreases the sensitivity of the amplifier and occludes observation of fundamental electrochemical noise, the integrated noise power remains low. The integrated input-referred root-mean-square noise is shown for each measured noise spectrum in Table 5.4. The steady-state noise current is significantly lower than the observed measurement limitations of the voltammetry measurements, which appeared at current levels around 500 fA. This discrepancy is explained by the redox current seen at very low HCF concen-

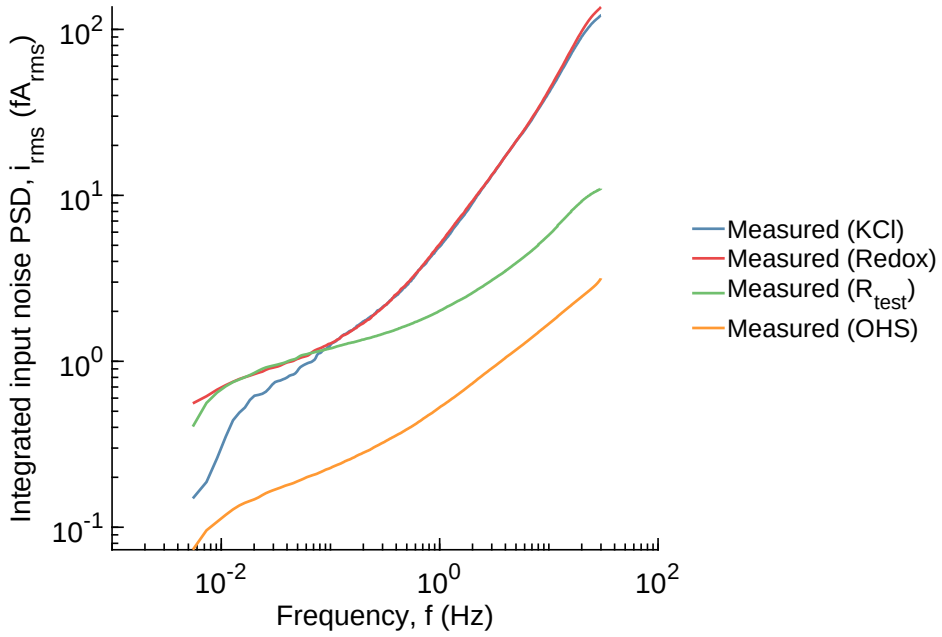


Figure 5.27: Integrated input-referred root-mean-square noise from measured spectra

trations, which could be caused by contamination. Despite the difficulties caused by this unknown contamination, detection of HCF was demonstrated at a concentration of 100 nM at 300 fA. Noise levels in redox and KCl solution were measured at 15 fA_{rms}, indicating that HCF detection of 5 nM could be achieved with the current system. The CMOS TIA is capable of extremely low-noise current measurements that approach fundamental limitations of both electronics and electrochemistry.

5.4.2 Secondary reactions

Anoxic voltammetry

Atmospheric gas such at oxygen or carbon dioxide are known to react with some solutions, resulting in interfering redox signals. This can present as an irreversible or quasireversible redox reaction, which will limit the limit of detection. To investigate reactions with atmospheric gas, cyclic voltammetry measurements were performed inside a nitrogen box to maintain an atmosphere of inert gas.

For these measurements, solutions containing only 100 mM KCl and 10 mM MOPS were

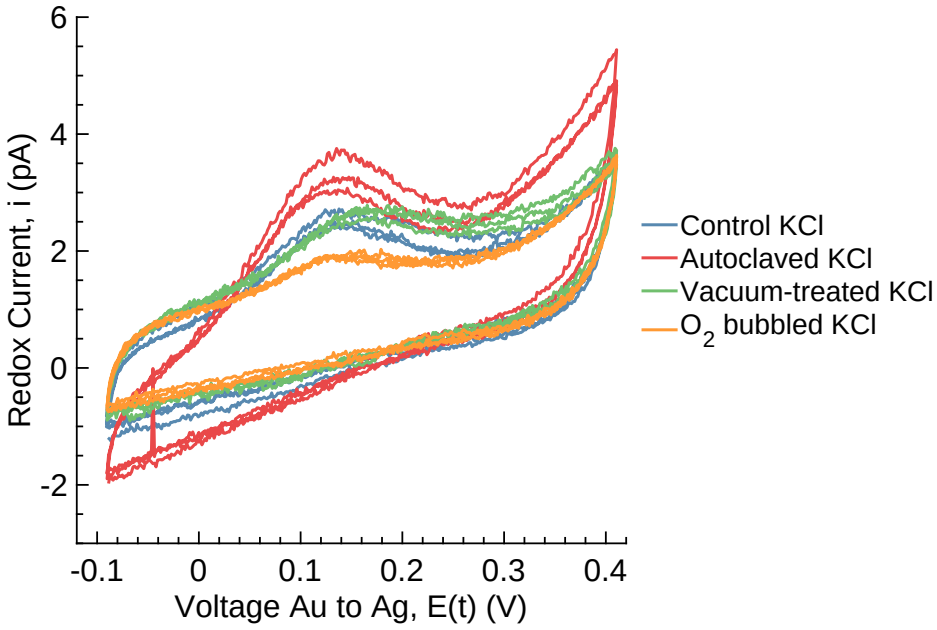


Figure 5.28: CV for different KCl solutions measured in nitrogen glove box

prepared and subjected to several different degassing procedures. Two solutions were bubbled with either pure nitrogen or pure oxygen for two hours. One test solution was sonicated and heated while under vacuum and another was treated in an autoclave to high temperature and pressure. A final solution was left untreated to serve as a control, and all five samples were transferred into a nitrogen glove box for testing. The contents of the nitrogen box were repeatedly cycled with house N_2 gas in order to ensure an atmosphere free of other contaminants. These different solutions were then used to perform the same CV measurements as the prior redox solutions, while within a nitrogen-only environment. The resulting voltammograms in Figure 5.28 show some differences between the four solutions.

The autoclave-treated solution showed a far worse peak in the measurement than either the vacuum-treated or control solutions, which showed similar peak behavior when tested with CV. The oxygen bubbled solution exhibited the lowest peak during the CV measurement when compared to the other solutions. This indicates the presence of an oxidative reaction, which can be driven entirely to the oxidated state by the bubbling of oxygen. This implies that the systematic peak can be reduced by bubbling solutions with oxygen

before testing. This could indicate that a systematic contaminant exists that is causing an independent redox reaction, which is driven highly to completion under oxidizing conditions.

Silver nanoparticle reaction

Another source for additional current which can be affected by oxidizing conditions is the Ag/AgCl quasi-reference electrode. Exposed Ag/AgCl electrodes are often used for electrochemical measurements, especially in confined volumes such as nanopore array and SECM measurements [59], [83], [133]. However, the Ag/AgCl electrode can cause silver ion dissolution and silver nanoparticle deposition that can produce redox current. Several investigations have found that exposed Ag/AgCl reference electrodes can cause small electrical currents as a result of silver dissolution [138]–[143]. The dissolved Ag^+ ions can be reduced after diffusing to the working electrode forming Ag^0 nanoparticles [140]–[142]. This dissolution is enhanced when the electrode is immersed in Cl^- solution, prompting use of chloride-free electrolyte, such as $HClO_4$ for sensitive measurements [141], [142], [144], [145], though this is not a usable solution for biological measurements. Other sensitive measurements have employed agar bridges to avoid the possible contamination of the silver reference electrode [84], [142]. This contamination could result in currents of several pA as observed in the CV measurements without the agar bridge.

The measurements of redox-free electrolyte using this system in the presence of an Ag/AgCl electrode as shown in Sections 5.4.1 and 5.4.2 provide evidence for the leakage of silver nanoparticles from the reference electrode. Silver redox current would appear at a lower redox potential near 0 V versus the silver reference, as shown in the original CV measurements.

Also, the bubbling of O_2 gas through this solution should fully oxidize the Ag^+ ions. This results in reduction of the anomalous current, as a majority of the free ions would be oxidized at the start of the measurement. Additionally, irreversible redox reactions of the nanoparticles at higher potential would further reduce the current, such as to Ag_2O, AgO or

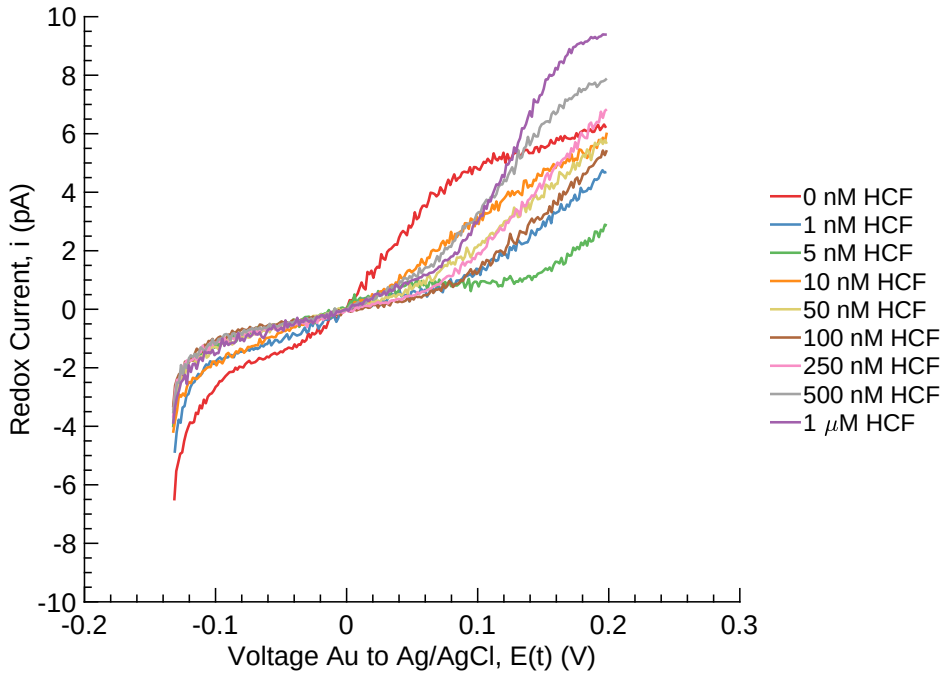


Figure 5.29: Anodic CV sweeps with HCF redox couple from 0 nM to 1000 nM concentration without agar bridge

Ag_2O_3. The presence of Cl^- ions may also be responsible for converting some of the ions into insoluble AgCl [142]. The detection of this tiny nanoparticle current proves the sensitivity of the measurement, but also presents a difficulty for observing the HCF reaction at very low concentrations.

Revisiting the CV measurements presented in Section 5.3 can provide clarity about the reference contamination. When an agar bridge is not used for the measurement, as in Figure 5.29, the low concentration measurements have a significant increase in current as the potential is swept from low to high. This current is extremely prominent in the solutions with no ferricyanide, as the ferricyanide competes with the silver to reach the surface of the gold electrode.

When the agar bridge is introduced, these currents no longer overwhelm the rest of the redox signal at low HCF concentrations. The removal of the silver current does reveal other electrochemical behavior which will be discussed in the following section. Use of the agar bridge serves to remove one variable and noise source from the measurement and allows for

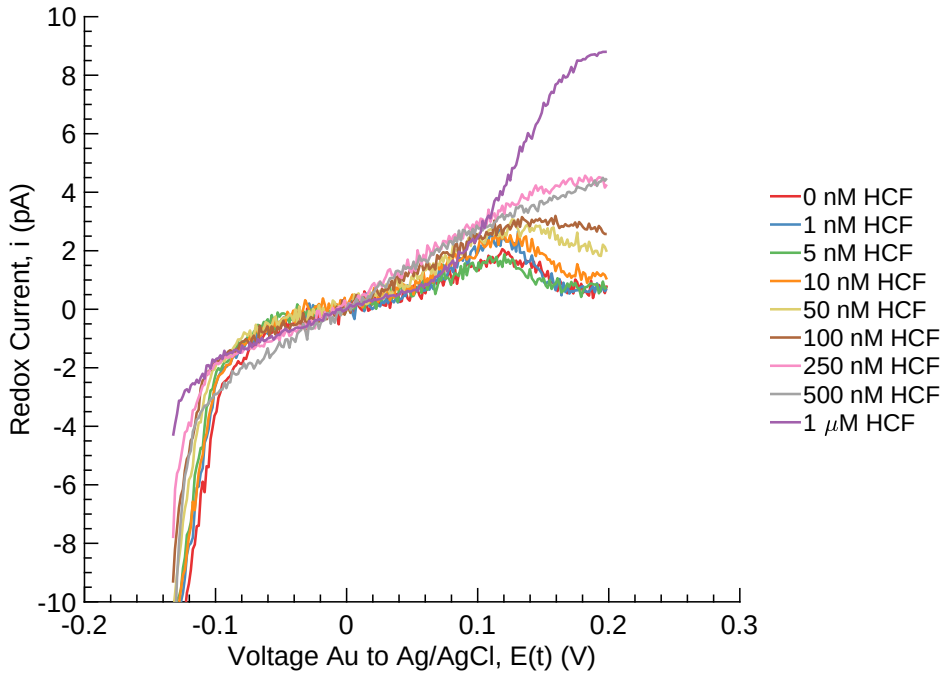


Figure 5.30: Anodic CV sweeps with HCF redox couple from 0 nM to 1000 nM concentration with agar bridge

further examination of the electrode-electrolyte interface phenomena.

Other redox reactions

Additional reactions are possible at a gold electrode in KCl buffer. Depending on conditions such as pH [146] and applied voltage [147], gold surfaces can dissolve into chloride media. Specifically, compounds such as $Au(OH)_2$ [146], [148]–[151] and $AuCl_2^-$ [146] can form on gold electrodes and are able to cause redox current. In most cases, this requires voltages outside of the working range of these measurements [146], [147], or particularly strong acidic [147] or basic [146], [148], [150] conditions. The contributions of these other chemical pathways is likely much smaller than that of the Ag/AgCl reference in these experiments.

5.4.3 Diffusion and surface effects

Reducing the contamination from the Ag/AgCl electrode allows the exposure of an additional source for system background current. At these low currents, diffusion patterns and

surface reactions at the gold working electrode are revealed to have significant impact on the voltammetry measurement. In UME measurements, the redox current should result primarily from steady-state radial diffusion due to the small area of the electrode compared to the diffusion length. However, our electrode geometry is a shallow recessed disk, which results in a modified diffusion pattern. Also, besides the possible surface reactions discussed in the previous section, surface adsorption of the substrates can also cause an alteration to the voltammetry profile. Together these phenomena help to explain the remaining background current seen in the CVs using an agar bridge.

Recessed disk electrode

The exact geometry of the electrode is created from the deposition of a layer of SU-8 photoresist onto gold microelectrodes. This layer forms the protective barrier that defines the edge of the working electrode. However, this layer also forms a shallow recess, which results in an alteration of the theoretical redox current [152]. The recessed geometry of the electrode reduces the steady state current at a UME due to an alteration of the diffusion profile, since the recess must first fill with substrates after a current step [153]. Recessed disc UMEs have a reduced steady state current of:

$$\frac{i_r}{i_d} = \frac{\pi r_0}{\pi r_0 + 4L} \tag{5.19}$$

as a fraction of the inlaid disk (flat) electrode current i_d derived previously, where L is the depth of the recession [153]. The UME used for the CV measurements is recessed by 5 µm to 10 µm, which causes a steady-state current reduction of 30 % to 45 %. This current reduction may explain some of the decrease of the measured current for CV and SWV from the theoretical values.

The recess also causes a more rapid and abrupt change between Cottrell and steady state behavior, which accounts for some differences in the CV waveform shape at low concentra-

tion [152]–[154]. The recess enforces a Cottrellian behavior at the beginning of the current step for longer, since the recess must linearly fill with substrate before a steady-state behavior can be reached. Together, these deviations can explain some of the smaller deviations from steady-state behavior seen in Figure 5.30 after the silver current was blocked by the agar bridge.

Surface adsorption

The CV waveform is also modified due to surface effects occurring at the electrode-electrolyte surface of the gold working electrode. Though several effects are known to cause reactions at the typically inert gold electrode surface [155], surface adsorption will occur in the absence of other reaction [134], [145]. In the case of anions like $[Fe(CN)_6]^{3-}$, this can occur due to electrostatic attraction and non-specific adsorption. Surface adsorption of redox substrates results in the disruption of the typical steady-state behavior at micro-electrodes. In typical measurements, the surface adsorption is insignificant at high redox concentration since the large number of available substrates will vastly overpower the current caused by adsorbed substrates [156]. However, as bulk concentration is decreased, the current that originates from adsorbed substrates will increase even as the diffusion related current decreases [156].

In a strong adsorption scenario, the free energy of adsorption will preference either forward or reverse reaction depending on the surface interaction of the substrate. This results in a pre-peak or post-peak in the voltammogram nearby the redox E_p [156]. Under weak adsorption, this peak will partially merge with the diffusion peak and cause either the anodic or cathodic peak to increase, while having little effect on the opposite direction [156].

This behavior is provides insight into the CV measurements both with and without the agar bridge. In absence of the agar bridge, silver ions in solution compete with HCF ions to adsorb to the surface. Competitive adsorption can be characterized using Langmuir isotherms which describe the surface kinetics [46]. At higher concentrations of ferrocyanide,

the silver was able to access only a small portion of the gold surface to react, resulting in current much lower than the HCF, resulting in little disturbance to the overall redox current. However, at nanomolar HCF concentrations, the silver was able to adsorb to the gold surface easily, resulting in redox currents up to pA levels.

With the agar bridge separating the silver from the gold electrodes, the silver current was mitigated, but the CV curves (Figure 5.30) still shows an increased anodic current due to the adsorption of HCF ions. This adsorption is described by the Langmuir isotherm:

$$\Gamma = \Gamma_s \frac{C}{C + K} \tag{5.20}$$

where K represents the adsorption coefficient, Γ represents the adsorbed substrate density, and Γ_s is the saturated substrate density. Additionally, surface adsorption is enhanced for HCF at positive electrode potentials because of the negative charge of the anions [157]. The attraction of the anions to the electrode as the applied voltage increases will encourage adsorption in the anodic sweep, while the decreasing voltage in the cathodic sweep will discourage adsorption, thus matching the CV waveforms seen in Figure 5.30.

These adsorbed ions form a small fraction of the current at micromolar HCF concentrations, but adsorbed ion current becomes more significant as the bulk concentration is decreased [156]. The limited supply of adsorbed ions results in a diffusion controlled current, in contrast to the steady-state UME behavior of the general diffusion current. Therefore, steady-state behavior is transformed into Cottrell currents at low concentrations. The combination of the diffusion and surface behaviors resulted in a peak shaped waveform that is revealed only when the bulk redox concentration decreases down to the nanomolar level. This behavior is very similar to the diffusion changes seen in nanopore nanogap arrays as concentration is decreased [133], [154].

To better understand the adsorption phenomena, peak heights for the diffusion controlled and steady-state currents were extracted and compared. The peak current for the

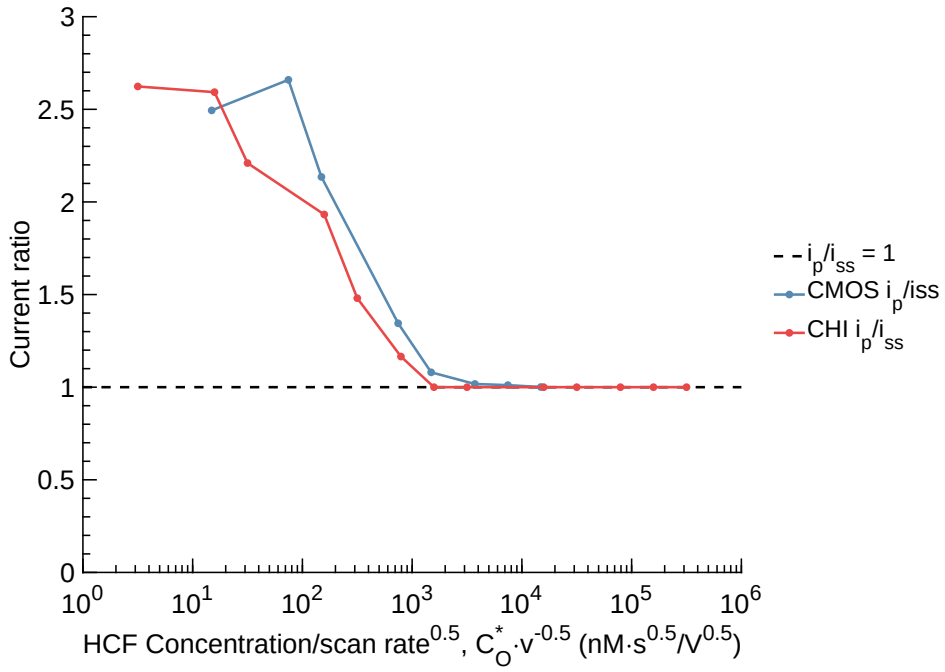


Figure 5.31: Current ratio versus normalized HCF concentration compared between the CHI760D and the CMOS TIA CV measurements

diffusion-controlled adsorption current increases compared to the steady-state current as the bulk concentration is decreased. The peak current to steady-state current ratios for the CMOS TIA and CHI760D measurements are plotted versus normalized HCF concentration in Figure 5.31. The plotted trends correspond with the theoretical model, as the current ratio increases from the pure steady state behavior at high redox concentration to a diffusion controlled current at low concentrations for both the CHI and CMOS TIA measurements, with the concentration normalized by the CV scan rate. The current ratio saturates at low concentration, as the adsorption reaches the Henry's law regime and no longer scales with changing concentration.

Additionally, the charge transferred due to adsorption can be calculated by integrating the current-time trace. This surface charge can be modeled using the thermodynamic isotherm to correlate the peak integrated charge with the bulk solution concentration [156]. The surface charge Q is plotted versus HCF concentration in Figure 5.32. The relation between surface charge and concentration from these measurements were more closely fit by the Freundlich

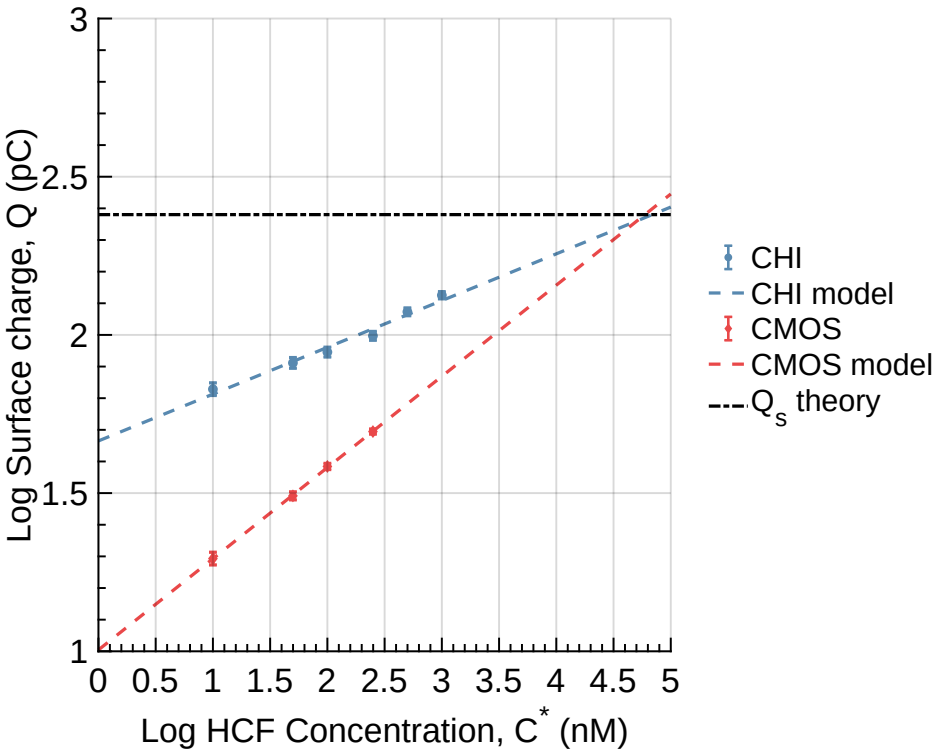


Figure 5.32: Surface charge integrated from current trace compared to bulk solution concentration

Table 5.5: Freundlich isotherm parameters extracted from integrated adsorption peaks

	K	1/n
CHI760D	46.23	0.148
CMOS	10.10	0.2882

isotherm:

$$Q = K \cdot C^{1/n} \tag{5.21}$$

This relation differs from the Langmuir isotherm by accounting for the effects of surface heterogeneity of the electrode, which impacts the adsorbed charge via a concentration dependence factor n [158]. The charge-concentration curves for the CHI and CMOS data converge towards a mutual saturation charge level, as predicted by the Langmuir isotherm, due to surface charge saturation from occupancy by a monolayer of adsorbed substrates [46]. The Freundlich model parameters for these fits are shown in Table 5.5. The expected saturated charge Q_s is shown as a horizontal line at 250 pC. This value was calculated using HCF

surface packing density measured using Auger spectroscopy by Baltruschat, et al. [159]. The Freundlich isotherm shows good agreement with the CMOS data down to the 10 nM level. Error bars are included based on the integrated RMS noise from the filtered CV curves as discussed in Section 5.4.1. These results show that the kinetics of electrochemical adsorption and diffusion are revealed in the CV measurements. The concentration data remains within 2σ of the model for each concentration down to 10 nM. Below 10 nM, low frequency noise limits the resolution of surface charge values, so these results were omitted from the model due to their larger than 2σ deviation.

Theoretical steady-state current from HCF couple for this electrode is 4.2 fA/nM, which combined with the 40 fA noise level would result in a limit of detection (SNR = 3) of about 30 nM. The surface adsorption results in increased current over the UME steady-state theory, thus enabling improved limit of detection down to 10 nM when modeled using the Freundlich isotherm. This low-noise electrochemical measurement system can therefore be applied to study many different microscale chemical and biological experiments.

5.5 Comparison to the state-of-the-art

The use of electrochemical detection for probing chemical and biological systems is invaluable for discrimination and quantification of analytes. The demonstrated measurement platform uses a CMOS TIA array to perform cyclic voltammetry detection and enables detection of HCF redox couple down to concentrations of 10 nM, through modeling of the adsorbed surface charge down to pC levels. The compact CMOS design also enables direct integration of the electronics with arrays of electrodes.

Additionally, this measurement system does not utilize current enhancement strategies, and instead sensitive detection is achieved through low-noise amplifier design. In order to perform high sensitivity electrochemical detection, most competing designs use various forms of signal enhancement. Nanogaps [134], [160], nanopore arrays [133], [154], and SECM [59], [83], [135] systems enable increased signal through redox cycling and compact reaction vol-

umes. Surface functionalization by nanoparticles [57], graphene [161], [162], nanotubes [77], [163], [164], self-assembled monolayers [165], [166], or biomolecule sensors [56], [167] also help to increase the electrical signal. Electronic methods such as stripping voltammetry [137], [168] and fast-scan CV (FSCV) [75], [80], [169] can provide some benefits, but increase further the complexity of the electronics and make minaturization more difficult. Unassisted microelectrode electrochemistry is often difficult to achieve due to the presence of many noise sources, as presented.

However, careful consideration of the noise sources can result in a circuit to provide high sensitivity without compromising the chemical signal. Additionally, this electrochemical measurement system can be significantly enhanced by combining innovations of current enhancement, such as nanogap redox cycling sensors [170], to achieve even better low-noise electrochemical sensitivity in a compact and efficient electronic system.

5.6 Summary

This chapter discussed the design and use of a CMOS array of low-noise transimpedance amplifiers for low-concentration measurement of redox-active substrates. Step voltammetry, cyclic voltammetry, and square-wave voltammetry were used to perform the measurement of HCF couple. The measured voltammograms were used to discriminate substrate concentrations down to 10 nM. The electrochemical noise of the measurement was modeled using analytical theory, electrochemical impedance spectroscopy, and circuit simulation to determine the noise contributors and the impact of the noise on the limits of detection. With the reduction of many of the outside sources of noise, surface adsorption phenomena were revealed, which can help further our understanding of the surface interactions at the electrode-electrolyte interface. The adsorption phenomena enabled measurement of lower redox concentrations than would be possible with steady-state current alone.

Chapter 6: Conclusion

6.1 Contributions

This dissertation presents the design of integrated amplifiers for current sensing of biological and chemical substrates. The work is focused on techniques to reduce circuit noise while maintaining compact measurement channels needed for high throughput CMOS arrays. First, JFETs were constructed in a commercial CMOS process with improved structures designed to reduce electrical noise for sensing applications. These JFET devices reduce noise significantly when compared to NFET devices of the same size. These devices are used to construct JFET-input amplifiers with lower input-referred noise than the equivalent NFET amplifier.

The second work presents a multi-channel CMOS TIA designed with femtoampere noise for electrochemical detection using low-noise design techniques. The amplifier array is used to measure femtoampere electrochemical currents from redox substrates via gold microelectrodes. The noise of the measurement is analyzed to separate electronic and electrochemical contributions using EIS, analytical theory, and circuit simulation. Ferrocyanide adsorption currents resulting in pC surface charge were observed down to the electrical noise floor.

These works have resulted in the following contributions to the field of low-noise CMOS integrated circuits:

- CMOS-integrated JFET devices with 10 times lower noise than equivalent NFETs
- A CMOS-JFET-input TIA designed with 10 times lower noise than the same amplifier with NFET input transistors
- CMOS TIA array of 112 amplifiers with $1\,\mathrm{fA_{rms}}$ current noise in a $3.5\,\mathrm{Hz}$ bandwidth

- Electrochemical detection of 10 nM redox substrates at gold microelectrodes using a 400 µm × 200 µm CMOS TIA

These contributions have resulted in the following peer-reviewed publications:

[1] D. A. Fleischer, S. Shekar, S. Dai, R. M. Field, J. Lary, J. K. Rosenstein, and K. L. Shepard, "CMOS-Integrated low-noise junction field-effect transistors for bioelectronic applications," *IEEE Electron Device Lett.*, vol. 39, no. 7, pp. 931–934, 2018.

[2] D. A. Fleischer, A. J. W. Hartel, S. Shekar, and K. L. Shepard, "Electrochemical noise limits of femtoampere-sensing, CMOS-integrated transimpedance amplifiers," *In preparation*, 2021.

[3] S. Shekar, D. J. Niedzwiecki, C. C. Chien, P. Ong, D. A. Fleischer, J. Lin, J. K. Rosenstein, M. Drndić, and K. L. Shepard, "Measurement of DNA translocation dynamics in a solid-state nanopore at 100 ns temporal resolution," *Nano Lett.*, vol. 16, no. 7, pp. 4483–4489, 2016.

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6.2 Future work

Low-noise JFET amplifier for biosensing

The CMOS-JFET amplifier was designed, fabricated, and measured, but was not applied to biosensing applications. The noise reduction provided by the CMOS-JFET devices would be ideal for low-noise biosensing in the low-frequency regime. This is potentially useful for many applications including patch clamp, electrochemistry, nanopipette, nanopore, and ion channel measurements.

JFET-electrochemical amplifier

The JFET devices could be especially useful for a CMOS potentiostat. The reduced flicker noise would result in decreased input-referred voltage noise that specifically benefits low frequencies. The voltage noise has large impact on current noise both at very low frequency through R_{ct} and at frequencies up to the flicker noise corner through C_{DL}.

Double layer compensation

Capacitance compensation is a method for reducing the impact of input capacitance on circuit frequency response through controllable feedback. This method is used frequently for patch clamp and nanopipette amplifiers, as these have large parasitic resistance from the solution and parasitic capacitance from the pipette. Current injection can be used to remove the impact of a parasitic capacitance on the TIA, but this does not extend to reduction of the noise that such a capacitance may cause. Reduction of the double layer capacitance may allow for higher bandwidth measurements, but circuit requirements to cancel the large value of C_{DL} completely are very high.

Some techniques have been used to reduce the noise impact of C_{DL} [119], but these have not been fully explored. Alternatively, the low-noise measurement capabilities of this system makes nanoelectrodes a viable method for reducing the double layer capacitance [9], [77], [142]. As electrode radius is scaled down, steady-state current decreases linearly, but C_{DL} decreases with the square of the radius. Reduction of C_{DL} through the use of nanoelectrodes could enable extremely low-noise electrochemical meausrements.

On-chip electrodes

The electrochemical amplifier was connected to external electrodes for the redox measurements presented here. This was a conscious decision to avoid the complications involved with on-chip electrodes, such as the difficulties involved with electrodes that become fouled or contaminated, thus destroying the entire chip. The use of on-chip electrodes would allow

for multi-channel operation with microfluidics and increases the miniaturization of the platform. The current chip design is also amenable for chip-to-chip bonding, which is possible with foundry fabricated BGA interconnects on the IC. With this technique, the IC can be attached to a custom electrode array while using the outer chip connections for power and digital communication.

Biosensing

Since the CV measurements with the amplifier were successful, the use of this low-noise system to measure biosystems is a natural next step. Several measurements of neurotransmitters [73], DNA melting [53], and DNA aptamers [119] have been performed using electrochemical transduction. Others have measured biological molecules through functionalization or by direct measurements of electrical activity [85]. The ultra-low noise performance of the presented amplifier could enable measurements of small biological currents.

Multi-channel measurements

While the electrochemical amplifier is capable of multi-channel operations with up to 32 channels, measurements were only attempted for a single channel. The current electronic system can measure four electrochemical cells with the use of microfluidics to enable separate addressing of four gold electrodes. Extending the measurement for more simultaneous measurements is achievable with upgraded PCBs, electrodes, and microfluidics.

Three-electrode potentiostat

Similarly, a three-electrode potentiostat is a potential improvement to the electrochemical system which has been demonstrated with multi-channel operation in CMOS [53]. The addition of a true reference and counter electrode would provide performance benefits when either the electrochemical current or the solution resistance is very high. The high current limitation would not typically apply for microelectrodes, although this is a typical concern

for FSCV. High solution resistance is observed during measurements of microelectrodes in acetonitrile and other non-conductive media. In this application, a three-electrode setup will ensure that the counter electrode is maintained at the proper voltage despite any solution resistance.

6.3 Final remarks

The innovations launched by the discovery of the transistor continue to make waves throughout all fields of science. Microelectronics can improve human life in myriad ways from hardware to healthcare. I hope that my work demonstrates the benefits of low-noise electronics for investigating the microscopic worlds of chemistry and biology. All we can hope for is that our efforts today will give the world a better tomorrow.

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