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Beam-steering MOEMS system based on a resonant piezoMEMS mirror and a phase-locked loop controller

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ABSTRACT

This work aimed to create a beam steering system based on a resonant micromirror with a control drive and sense modules implemented with low-voltage electronics and piezoelectric actuation and sensing. Solution's optimization goal was to create scalable architecture with minimal power consumption and reduce an overall MOEMS system size.

We applied a direct digital control methodology for resonant piezoelectric elements by designing a level-translating electronics to directly interface actuator and sense elements with MAX1000 FPGA development board. This implementation merged control and measurement loops into VLSI design operating in the FPGA. The system behavior studied with 2D-scanning mirrors featuring an in-house piezoelectric MEMS-platform with AIN patterned actuation and sensing elements by measuring the generated laser reflection and pattern cross-correlating it with electrical signals.

The developed MOEMS system provides the means for 2D optical scanning with a 1.8V logic level drive. Characterization results presented, study a mirror reflection pattern correlation with optical signals, and implemented control methods enabled frequency control with feedback in all operating conditions. The mirror feedback loop in the time domain provides reliable phase delay and oscillation period information. The calibrated look-up table post-processing module leverages this information and calculates the mirror's angular position at a given moment in time.

The direct digital interface with a resonant piezoelectric mirror can deliver controllable beam steering in a single-supply, low-voltage, and high integration environment. The digital control loop allows for measurement and adjustment on a cycle-to-cycle basis, enabling further algorithm development for advanced functions like cross-sensor compensation, safety, and sensor fusion.

Keywords: PLL, Digital Contol, Micromirror, Piezoelectric, LiDAR, MEMS, scanning mirror

1. INTRODUCTION

Resonant piezoelectric mirrors as micro-opto-electro-mechanical systems (MOEMS) offer options for laser beam steering or optical multiplexing. While piezoelectric resonant devices are more complex than typical electrostatics devices, they have a distinct advantage as they operate on minimal current and voltage levels that interface directly with standard CMOS.

Multiple topologies exist to drive resonant structures, and patents like [1] and [2] have been granted for both of these examples; there is a method of capturing the signal, manipulating that signal, and feeding the signal back as a sine wave. In [3] driver side applies Delta-sigma-modulator and low-pass filter to form a sine wave for a resonating structure. In [4], the piezo element's internal properties are entrusted to separate the signal's primary frequency from the closest harmonics. Multiple options for resonance monitoring exist in the literature, like analog to digital converters[2], peak detectors[4], voltage controller oscillators[3], or phase-locked loops [5]: each of these methods have a different response time, accuracy and complexity impact to system-level design.

The most minimalistic phase-locked loop approach was selected to allow the design to be applied to various resonator structures. Applying loop control via FPGA will allow a digital system design methodology and reduction of most external components. The first step of this reduction is the full digital mirror control topology that evolved from the earlier work on VTT [4]. Based on initial findings, one may conclude that the spectrum width of excitation signal or waveform shape has minimal effect on resonating modes of high-Q Piezo-MEMS structures. Digitalization of design allows the coupling of different structures further away from the resonance loop while reducing components that interact with the resonance loop.

2. METHODOLOGY

MicroMirrors

The presented control method is designed to be used with test devices created by VTT AIN-based piezoelectric process. Samples from various production runs were tested, with a major difference originating from geometry-induced resonance shifts and sensitivities. The devices were patterned on bonded SOI-wafers with an active layer in [111] orientation to reduce the effect of crystal orientation on spring elements. The cap wafer with a deep cavity, silicon filled through-silicon via routing and flip-chip soldering pads, was bonded with device wafer and glass carrier wafer for an optical window by Murata Electronics using glass-Si anodic bonding process. The finished device. that is soldered to ceramic carrier board for easy handling is shown in figure 1.

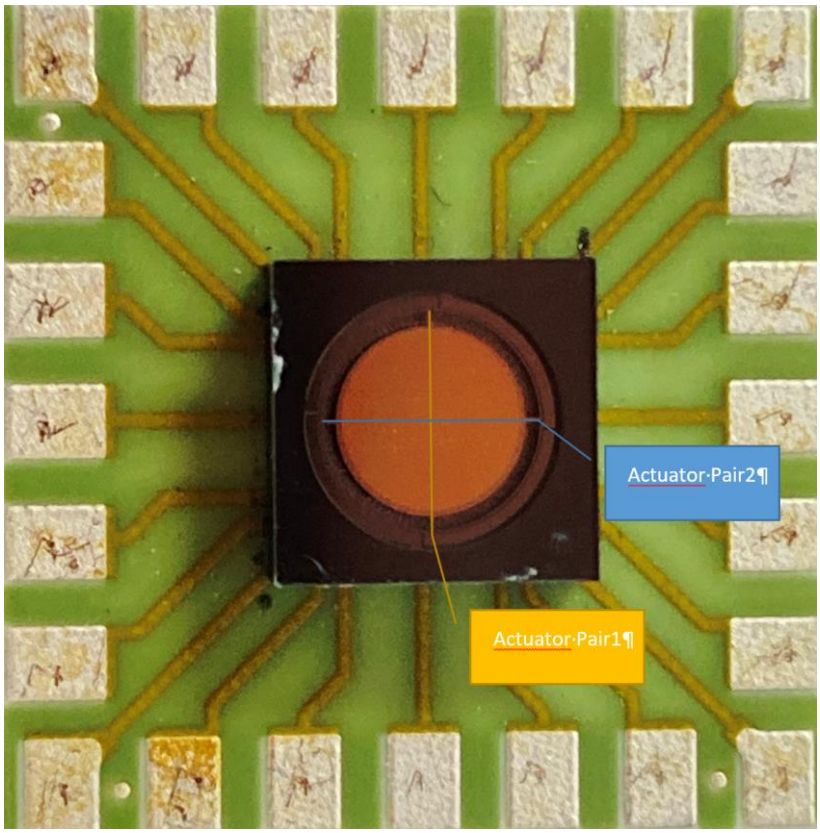

Figure 1 Orthogonally actuated piezoelectric mirror on a ceramic carrier.

Figure 1 illustrates resonance axes formed between actuator pairs, where perpendicular actuator pair s. The micromirror in figure 1 has a reflective surface diameter of 4 mm and a chip area of 7x7 mm^2.

Electronics

Based on earlier [4] findings, the control platform was created to enable algorithm development with real-time mirror sensory signals. The mirror's simplified drive side consists of only a half-bridge buffer to separate analog and digital domains and enable drive voltage selection. This drive buffer could be scaled to match the higher voltage requirements of electrostatic mirrors, as in [5]. The comparator stage translates voltage levels to the IO standard used by the FPGA. Mirror driver digital design implemented with Verilog resides on MAX1000 FPGA development board integrated into mechanical design. The summing amplifier captures high impedance sense signals with opposite polarity; this amplifier stage eases the sensing signals without disturbing the operation. The differential sensing of the mechanically paired element increases a signal-to-noise ratio of the signal as electrical interference or mechanical shocks manifest as a common-mode error, non-detectable by the amplifier. The comparator phase after the amplifier translates analog signal to digital signal suitable for MAX1000 digital input. The supply voltage for the mirrors was selected to be 1.8V IO voltage standard. The complete analog front-end illustrated in figure 2 operates from a common 3.3V supply rail.

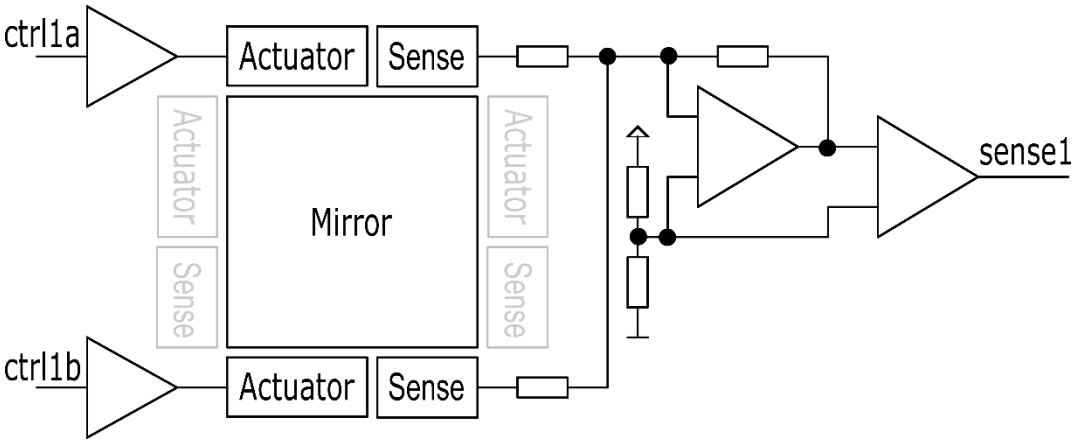

Figure 2. Analog front-end for each resonator pair.

As seen from Figure 2, this drive architecture allows fast adaptation to different element configurations as drive, and sense pairs can separate or be combined to interface multi-axis elements. The proposed electronics interface with minimal conversion provides a good solution size. Programmable logic integrates most space-consuming tuning elements like filters and delays and does not require precision current or voltage sources for operation. This change allows the transfer of information and synergy between different resonator structures and directs development efforts to the digital domain. The frequency range of the current Piezo-MEMS resonating mirrors is 500 to 2000Hz, enabling a real-time digital manipulation as typical FPGA operates at 125MHz. Further, the time delay to be inserted between the sense and drive signals is in the range of 100 to 200µs. Figure 3 presents a 3D-printed mechanical support structure that includes the mirror carrier, Analog front-end board, and MAX1000 development board, which is mountable to generally available standard holders for the 2-inch optical components.

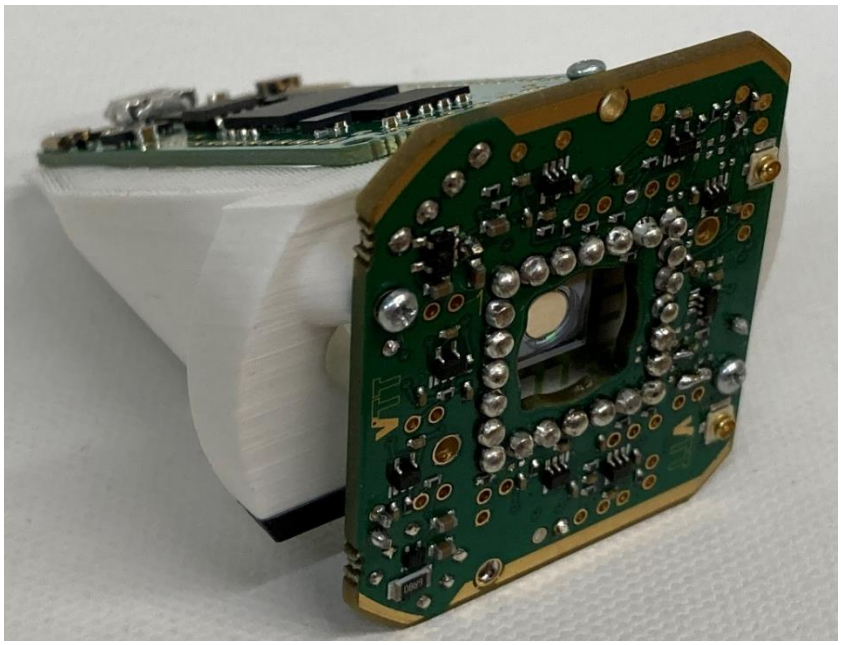

Figure 3. 2" optical scanner module.

As seen from figure 3, the board contains more components than described and illustrated by figure 2. Additional components on the board drive amplifier stages to measure and monitor different parts and do not affect the circuit's operation.

Digital control loop

MAX10 field-programmable gate array (FPGA) hosts the digital system design realized in Verilog Hardware Description Language (HDL). Implementation of the control loop as programmable logic allows multiple feedback routes and control methods without compromising the main adjustable delay block's low-latency operation at the mirror loop controller's core. Other digital design subsystems include calculators, switches, start-up circuitry, time digitizer, and communications circuitry. Digital system design utilizing only 651 logic cells and 249 registers is presented in figure 4 with interfaces to analog front-end and PC-host.

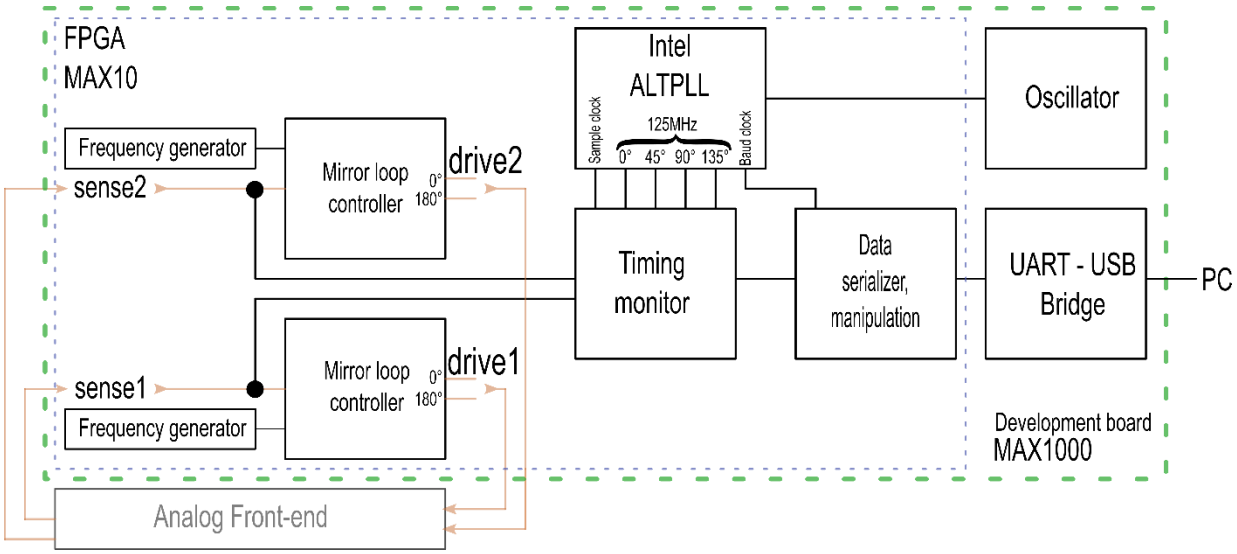

Figure 4 Block diagram of a two-axis drive with phase and period detection.

The digital design consists of four discrete design modules. The frequency generator includes start-up circuitry, reset, and frequency sweep functionalities. Static frequency generation and sweep modes operate with an 8-ns time resolution derived from a 125MHz-system clock. The Mirror loop controller monitors sense and frequency generator signals. Statemachine triggered delay adjustments are used to align these signals and determine the proper operations mode for the resonator. The first mode is an open-loop, where an internal frequency signal is supplied as-is to the analog front-end. The sense signal does not affect the operation during the open-loop mode, but loop control monitors phase-shift between drive and sense signals to ensure stability. The second operation mode is a Phase-locked loop operation, where the sense signal generates the drive signal from the sense channel. Free-running phase-locked loop finds peak resonance for a given element and operational parameters: drive voltage, phase delay, duty cycle. Mirror loop controller may adjust digital domain duty cycle and delay so therefore indirect a frequency. This control method allows a combination of a closed-loop system's ruggedness, which can recover resonance after a shock, and open-loop frequency stability. Frequency stability provided by this control method is proportional to the purity of the sense signal, as additional frequency components transform to jitter when digitized. Mirror loop controller archives seamless transfer from open-

loop mode to the phase-lock loop operation by matching delay from frequency generator to the drive signal to be equal than sense signal to drive signals delay and then changing signal source after toggle event.

Resonance timing monitor uses PLL generated phase-shifted primary clocks at 0°, 45°, 90°, and 135° and a dual-edge pulse generator to increase period and phase counter resolution to 1ns, equal to implementation in [3]. Implementation of the Tapped-Delay Line (TDL) was omitted, as 1-ns timer resolution was deemed adequate when used to clock 2-kHz mirror movement: with 2 kHz movement $\frac{360°}{2000kHz} * 1ns = 0.00072°$ theoretical resolution is achieved. The running timers monitor coupled resonators and provide accurate relative position at the external trigger or sample clock events, as illustrated in figure 5.

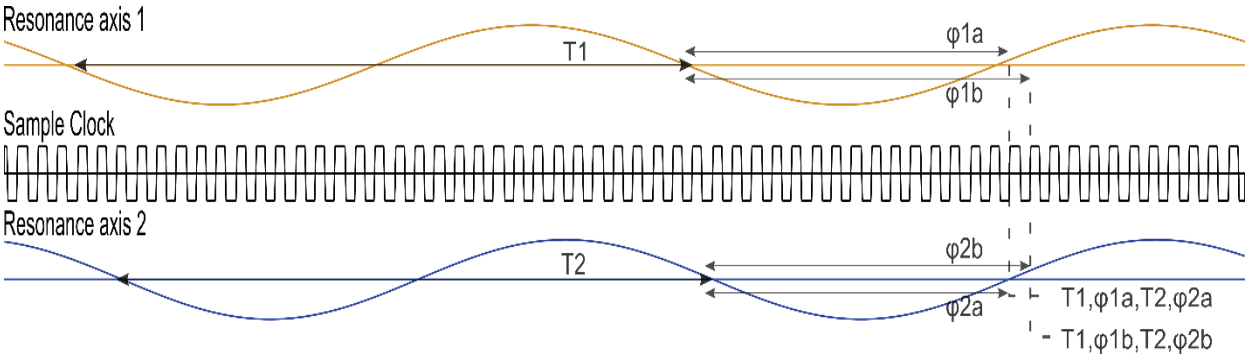

Figure 5 Resonance axes synchronization and measurements

In figure 5, T1 and T2 are measured on a cycle-to-cycle basis, and with each sampling event, a current counter value is logged as phase information. The presented design can transmit native period and phase information via the Data post-processing module 100k times per second from the FPGA to the PC host.

Information compression at the post-processing module would allow improvement of possible data rate. A simple way to compress data would be to implement formula $Angle_1 = k_0 * Sin\left(2\pi * \frac{\varphi_{1n}}{T_1}\right)$, where k_0 is angle calibration value, φ_{1n} Phase information from figure 5 and T_1 is the previous period. Inserting a maximum deflection angle to k_0 does not solve the angle in all cases, as a simple equation is accurate only for a rectangular scanning pattern. The optical system as a whole involves multiple sources of variables that should be studied and quantified separately. In figure 6, lens distortion phenomena like a barrel, pincushion, and keystone are visible in the field of view. Those can result from non-idealities in different optical surfaces or effects that frequency and phase of resonator pairs have on each other.

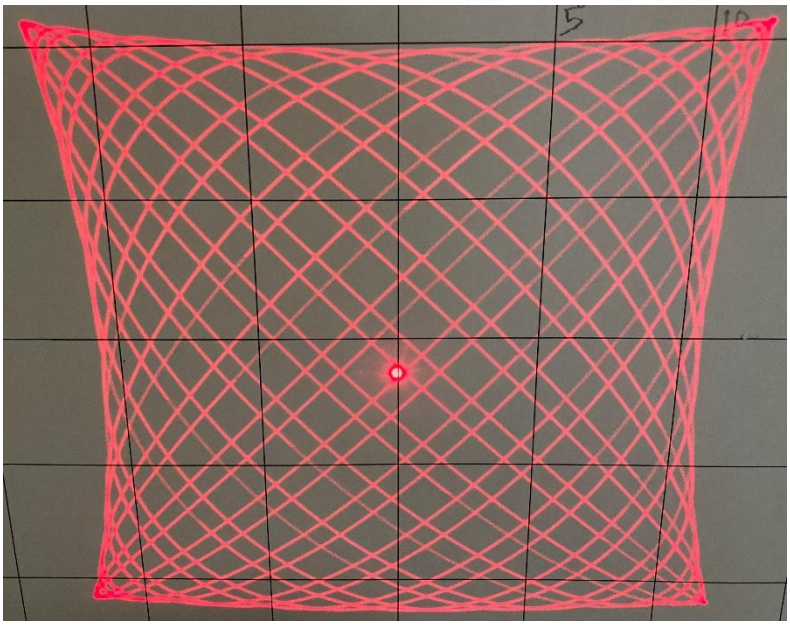

Figure 6 Lissajous laser beam scanning pattern

A complete optical characterization would be needed to trace distortion sources in figure 6 to root causes like mirror deformations, non-linearity, and packaging of the mirror, and to separate the mechanical factors from the electrical factors caused by piezoelectric properties and cross-talk. An example of cross-talk artifacts cause by the close routing of the drive, and sense signals can be seen in figure 7, where the yellow pair has long parallel routing and blue has not.

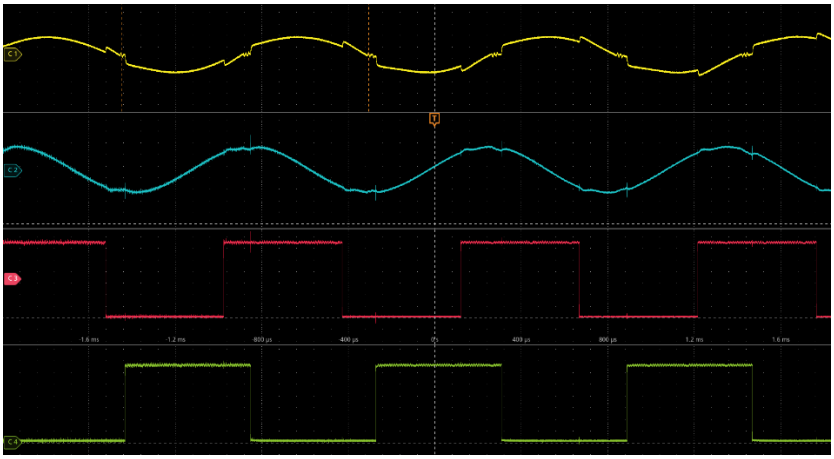

Figure 7 Cross-talk artifacts cause by the close routing of the drive and sense signals.

In the figure 7, the drive signals cause a level shift to the yellow signal, which may in some cases trigger a false edge that can lead to a collapse of resonance or wrong reading at the resonance monitoring circuit.

3. RESULTS

Dataset presented in figure 8 was collected by measuring an orthogonal corner-to-corner distance, and concave or convex distortion at the middle of the pattern is ignored. Measurements from patterns like figure 6 are taken with calipers from the middle of the laser's path. These measurements have an error tolerance of approximately ±1mm, which translates to an angle error of ±0.05°. Distance measurement to Angle conversion is made using two distances to measure the same pattern and then calculate the angle. An additional error factor is caused by the laser beam angle compared to the deflection angle, as the Laser source is located at an angle of 15° from the mirror centerline. The wall is symmetrically 15° from the mirror centerline. This asymmetry causes distortion as the glass wafer's planar surface refracts light as a function of the incident angle described by Snell's law [6]. Cumulative errors measured from rotated patterns were in the range of ±5 mm or ±0,25°. As measurements are performed in the same manner for each point, the error between similar points is not significant. However, as absolute values are less accurate, the comparison between different measurements can lead to false conclusions.

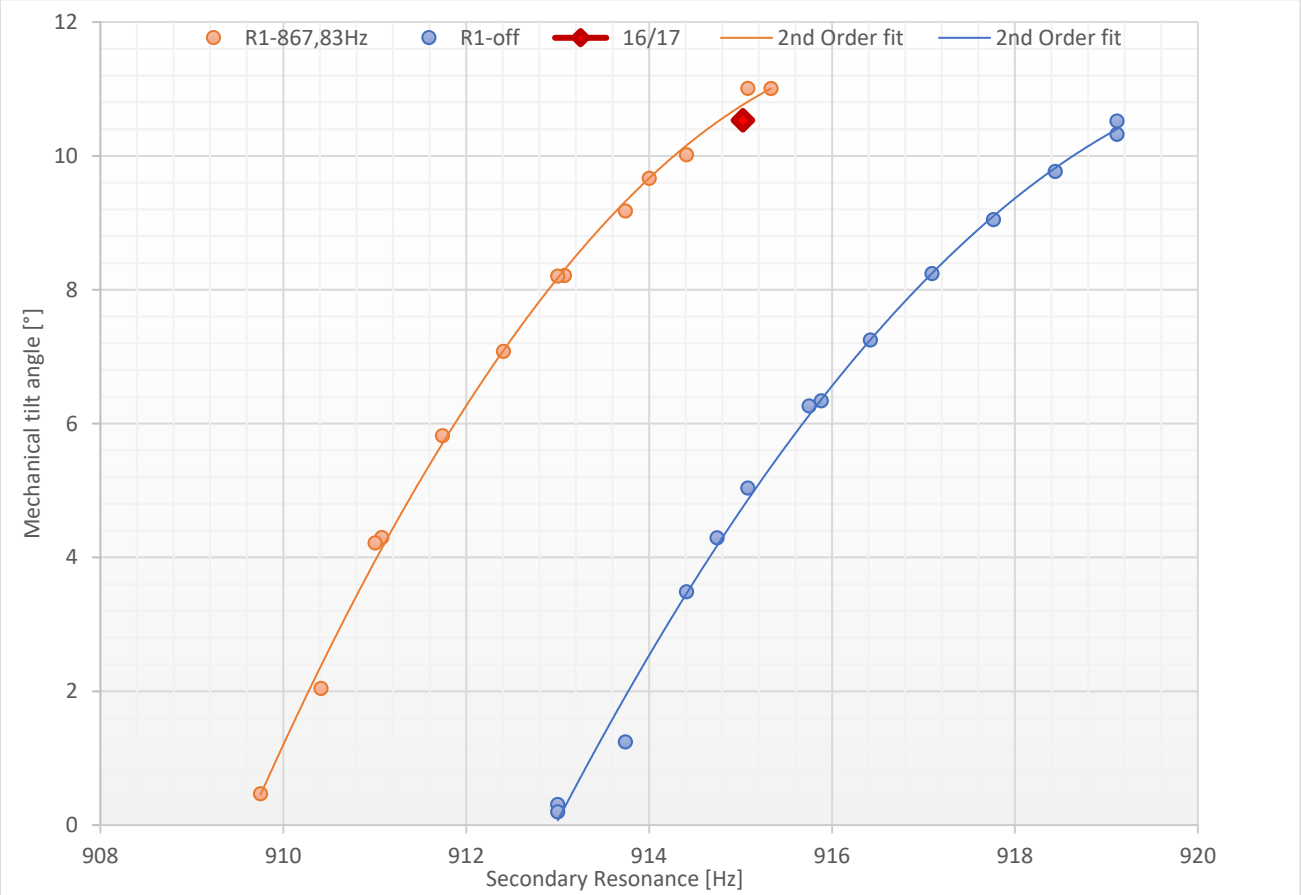

Figure 8. Resonance amplitude in the function of primary and secondary resonances

Figure 8 shows that the orange and Blue curves present hardening of the actuator spring, while resonator R1 induced stress remains static. This non-linear effect on the single silicon springs is modeled in depth in [7]. The secondary 4-Hz frequency shift of the resonance peak complicates calibration, as the simple angle equation presented earlier gains an additional term that is the proportional frequency of the orthogonal axis. A shift of the resonance peak also changes the

2nd degree polynomial of the amplitude/frequency curve. However, even if the center frequency shift complicates the system's precise simulation, it also eases the creation of scanning patterns for a specific purpose, as both frequencies can be tuned without drastic amplitude reduction. When looking at the literature behind the parametrization of imaging systems [8], we see that the presented architecture is exceptionally suitable as it allows mechanics limited control of resonance frequencies. Selected multiplier values of the system clock can meet application and system requirements. The red dot in figure 8 presents a fractional point created by setting an open-loop counter for resonator R1 at 145146 clock cycles(861,2Hz) and 136608 clock cycles(915Hz) for resonator R2; this results in a static pattern with a ratio of 16/17. The pattern repeats every 18.6 ms or 54 Hz, so with a matching sample rate in the sampling system, the same pixels can be measured. For LIDAR-application, this may not be desirable as the static pattern also translates to a low fill factor of the field of view. A prime number based scanning may be more suitable for maximizing the scanner sample rate, fill factor, and deflection angles. The presented method allows easy insertion of prime numbers as counter values for a period or half-period to decrease the repeat rate. An example would be to use 136621 instead of 136608 and 145177 instead of 145146, this would not change the pattern's amplitude as frequencies are 0.1Hz and 0.2Hz from the original, but it would increase the pattern repetition rate to 149.8 seconds from the earlier 18.6milliseconds.

In addition to optical and resonance measurements, performed current measurements verify the piezoelectric resonator's energy demand and the drive solution's comparable energy demand. Figure 9 shows the current drawn signals from the 5-V main supply line provided with USB.

	mA	d_mA	d_mW	Figure
System Reset	91,60			
Logic Init	93,66	2,06	10,61	
Logic 1 resonator	94,76	1,10	5,69	
Logic 2 resonator	95,15	0,39	1,99	
AFE idle	3,19			
AFE 1 resonator	3,19	0,0019	0,0099	
AFE 2 resonator	3,19	0,0007	0,0034	

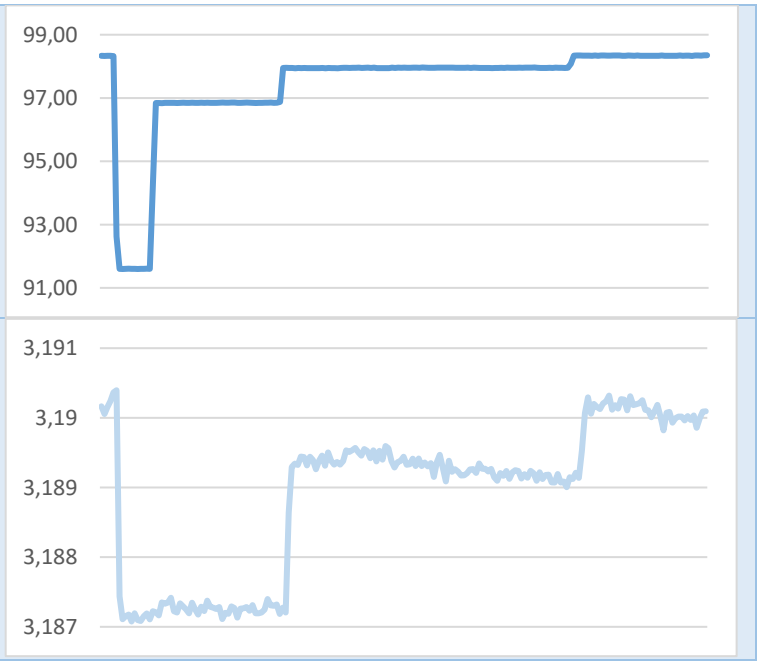

Figure 9 Current draw at different phases.

Figure 9 illustrates four different power consumption phases; the first is the regular operation where both resonators and digital design is active. 2nd phase is on-set of a hard reset, where logic consumption drops to its minimum value, and the analog front-end goes to the idle stage. 3rd phase is when the software is loaded but remains idle until a 32-second

timer triggers a start of resonator R1. In the 4th phase, resonator R1 is started, and the energy demand to accelerate the mirror mass can be seen in the current consumption curve. The start of the 5th event brings the device back to the first phase, where resonator R2 is activated and draws a bit more current during an acceleration phase.

As seen in the measurements, a static current into MAX1000 and analog front-end is substantial compared to dynamic measurements. MAX1000 supplies LEDs, SDRAM, accelerometer, other peripherals available onboard, and analog front-end supplies static current to amplifiers. Therefore, looking at the delta values reveals that the energy consumption due to the second resonating piezo element rises only about 3.4 µW and logic side by 2 mW. Wake-up of the first resonator consumes a bit more at 10 µW, but the digital logic consumption rises at the beginning of the active operation by 5.7 mW; this also includes activation of the measurement circuitry and communication interfaces.

4. CONCLUSIONS

The developed MOEMS system provides 2D optical scanning with a 1.8V logic level drive and low power consumption. As design mainly exists as intellectual property, it is ideally adaptable to different resonating topologies by rearranging, coupling, and parametrizing the digital systems design modules. The design solution is limited to work with practical resolution steps on resonant elements up to 20-kHz center frequency. However, sigma-delta techniques [9] would allow improvements of frequency resolution on the drive side. Furthermore, much-studied programmable logic-based time digitizer methods like[10-12] would mitigate low receiver resolution derived from the system clock. Calibration methods or application innovation are needed so that ±0.125° systematic errors in the field of view can be eliminated or correlated. As presented, the FPGA in the loop method for the piezoelectric mirror offers flexibility and minimization of resonator dependent hardware. Thus enabling a focus shift from drive optimization to the development of analysis algorithms, calibration methods, and integration.

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