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A Full Ka-Band GaN-on-Si Low-Noise Amplifier

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***Abstract*— In this paper we present the design of a full Ka-band low-noise amplifier implemented in a 100-nm GaN HEMT on a high-resistivity silicon substrate technology. The amplifier achieves a noise figure of an average of 1.9 dB and a gain better than 23 dB for the whole Ka-band. Measured 1-dB output compression point was 22 dBm at 38.5 GHz.**

***Keywords*— gallium nitride, HEMTs, linearity, low-noise amplifiers, MMICs.**

I. Introduction

In addition of having low-noise and adequate gain high linearity and overdrive survivability are desirable features for low-noise amplifiers utilized in transceiver front-ends for telecommunication payloads, radars and mobile base stations. Gallium nitride (GaN) based technologies have shown their potential for implementing low-noise amplifiers with high linearity and robustness [1]. Although GaN on SiC substrates have better thermal conductivity making it more suitable for high power applications it remains more expensive compared to GaN on Si substrates [2]. In this paper we study the feasibility of using a 100-nm GaN HEMT on silicon substrate from OMMIC, France, to design a full Ka-band low-noise amplifier (LNA) with high linearity.

II. Low-Noise Amplifier Design

A three-stage common source (CS) configured transistors are used to design the full Ka-band LNA. The design of the first stage of an LNA is critical because it mainly defines the noise figure and the input return loss of the amplifier. Therefore, while choosing the biasing voltage, the number of fingers, finger width, and the size of the source feedback inductance for the first-stage transistor, we have kept tracking on the minimum noise measure (M_{min}) [3]. When a multistage amplifier is to be designed and the available transistors have fairly low-gain at the design frequency, M_{min} is a useful figure of merit for obtaining optimum noise performance [4].

Usually, the transistor size is set by first choosing the unit gate width for a single finger for optimum noise performance and then changing the number of gate fingers to achieve required input and output impedance for matching [5]. Adding more fingers can be also used to improve the linearity of the device. However, in our design we have chosen a four-finger device since adding more fingers add parasitics because of the connecting wiring and more airbridges needed to connect the sources together. This could make the device also more prone for instability [5].

Therefore, our design task started by varying total gate width of a four-finger device while keeping track of the $\Gamma_{M_{min}}$

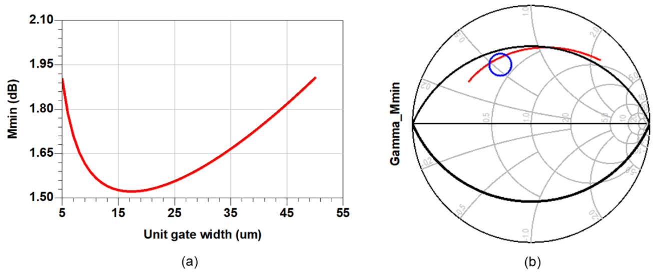

Fig. 1. (a) Minimum noise measure (M_{min}) in a function of total unit gate width for a four finger GaN HEMT at 35 GHz. (b) Optimum noise match ($\Gamma_{M_{min}}$) trajectory over the gate width from 5 to 50 μm. The gate width increases towards short. The $Q = 2.35$ enclosure is shown on the smith chart with the black line. The blue circle shows the location of optimum noise measure match for the chosen 35-μm wide transistor.

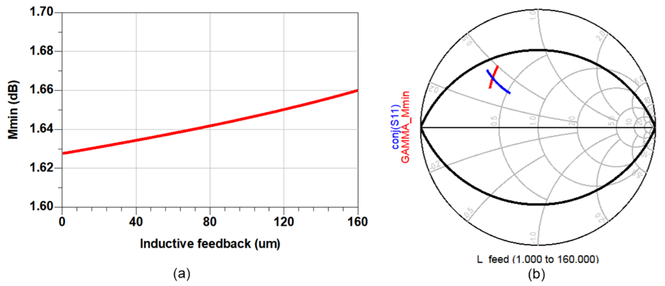

Fig. 2. (a) Minimum noise measure (M_{min}) over the source feedback line at 35 GHz. (b) Optimum noise match ($\Gamma_{M_{min}}$) and the conjugate of the S_{11} trajectories over the source feedback line. The $Q = 2.35$ enclose is shown on the smith chart with the black dashed line.

(input impedance required for optimum noise match) on the Smith chart, in order to see how the optimum noise impedance varies. It is seen from Fig. 1(b) that as the transistor's gate width increases, the trajectory of the $\Gamma_{M_{min}}$ move towards left and falls inside a constant Q-curve. The Q of a circuit can be defined as the ratio of the frequency (f_c) to the bandwidth (Δf) [6]:

$$Q = \frac{f_c}{\Delta f} \tag{1}$$

A low Q translates into a broad band circuit. In this work, we took advantage of Q-curve to design a full Ka-band LNA. The Ka-band refers a bandwidth of 14 GHz (26 GHz-40 GHz) with a center frequency at 33 GHz. Therefore, according to Eq. 1, to cover the full Ka-band, the optimum noise impedance must lie inside the $Q = 2.35$ enclosure. Hence, although the Fig. 1(a) shows that the lowest M_{min} is obtained with a total gate width of 17μm, a 32μm of total gate width was chosen

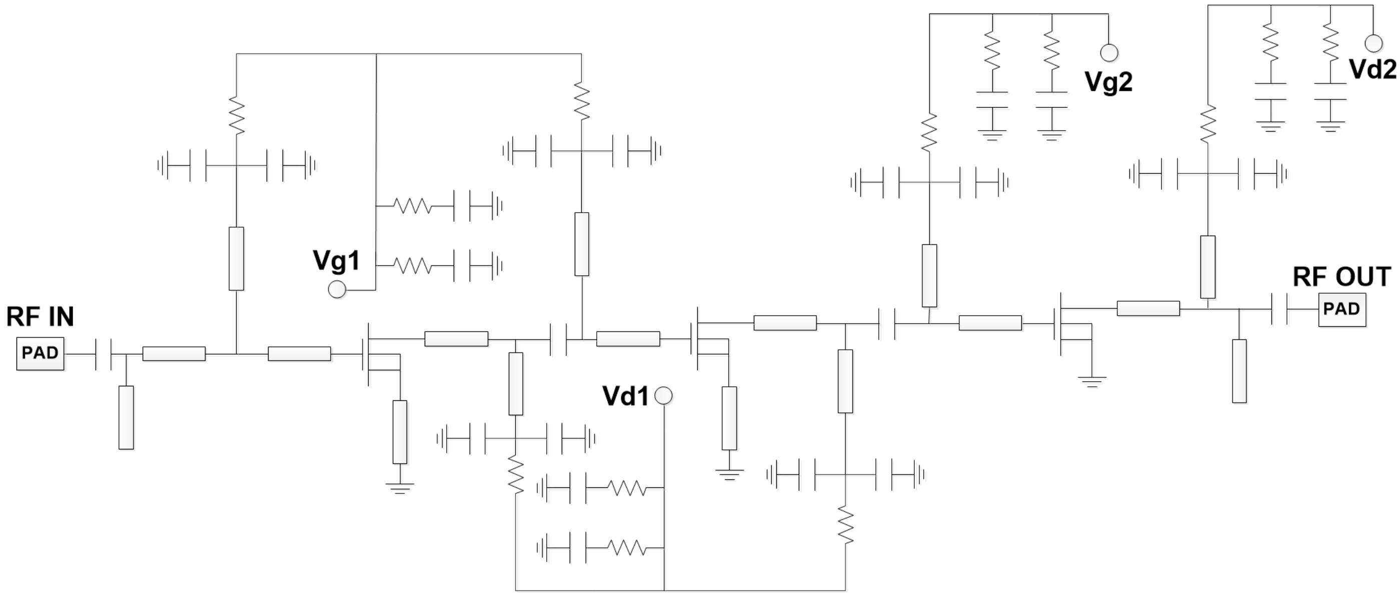

Fig. 3. A simplified schematic of the designed full Ka-band LNA.

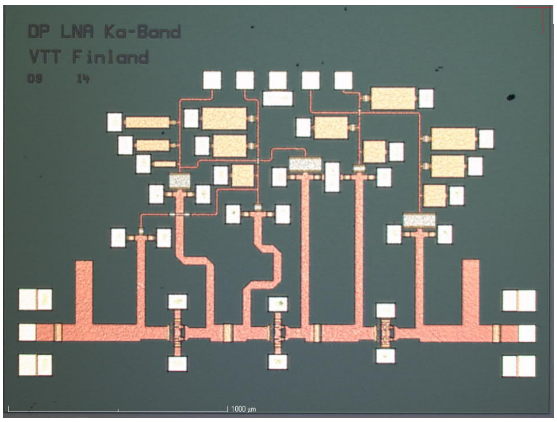

Fig. 4. Layout of the designed full Ka-band LNA.

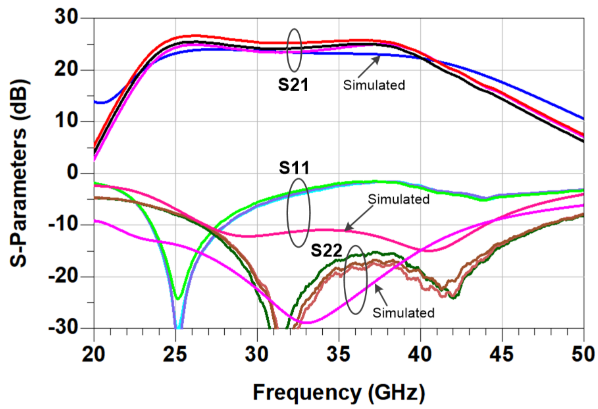

Fig. 5. Simulated and measured (three-samples) S-parameters of the designed full Ka-band LNA.

because that falls inside the $Q = 2.35$ enclosure and also eases the input matching.

To improve the input matching and stability, inductive source feedback is realized by a section of transmission line connected to the source of the input transistor. Fig. 2(a) shows that the change in M_{min} is minimal on the source feedback, however, Fig. 2(b) shows that by varying the length of the feedback transmission line, we can obtain an optimum impedance which satisfy both an improved input matching and the optimum noise measure. In this work, we have chosen the length of the feedback transmission line from the intersection of the conjugate of the S_{11} and the $\Gamma_{M_{min}}$.

The same gate width of the transistor and the source feedback transmission line are used for the second stage whereas a wider gate width (42μm) is set to the third stage for improved linearity. This way an optimized power consumption and better noise performance are achieved.

The simplified schematic of the designed three-stage common-source (CS) LNA is illustrated in Fig. 3. The inter-stage matching networks consist of series transmission lines and a short-circuited shunt stub. The input and output matching networks include additional open-circuited shunt stubs to obtain a wideband input and output matching. The bias networks are connected through the short-circuited shunt stubs, where the low-frequency stability is ensured by adding the resistor-capacitor networks.

III. Measurement Results Of The LNA

The layout of the MMIC is shown in Fig. 4. The total DC power consumption of the circuit is 433 mW. On-wafer measurements were carried out to characterize the manufactured LNA. The measured and simulated S-parameters are shown in Fig. 5. The measured small-signal gain is better

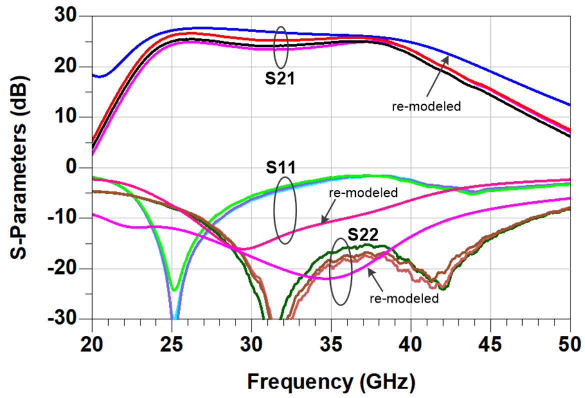

Fig. 6. Re-modeled S-parameters of the LNA with the small signal model presented in [7]) and the measured S-parameters.

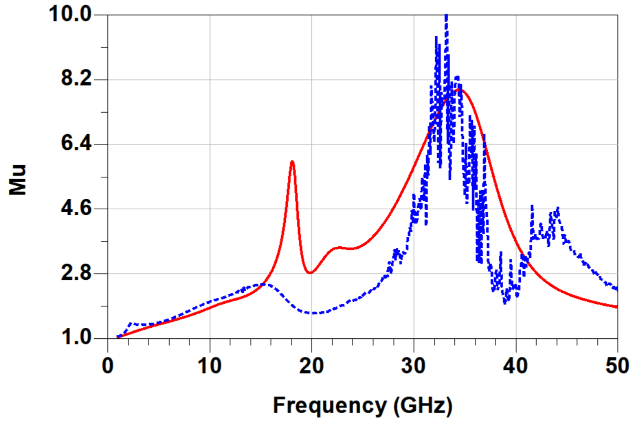

Fig. 7. Simulated (solid) and measured (dotted) μ-factor of the LNA

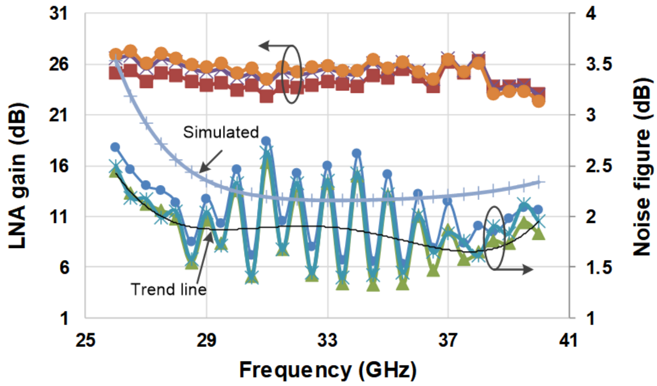

Fig. 8. Simulated and measured (three-samples) noise figures and insertion gain of the designed LNA.

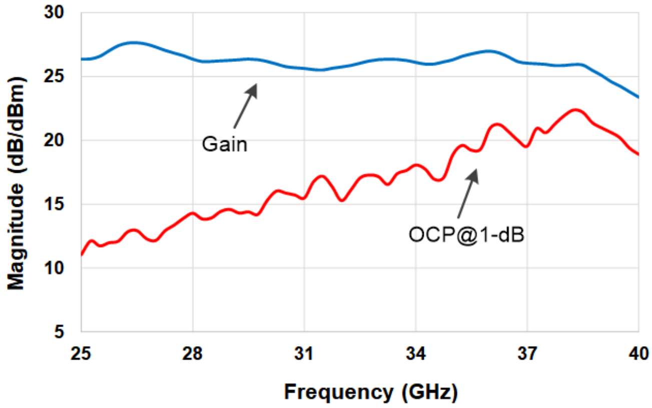

Fig. 9. Measured 1-dB output compression point (OCP) and the associated gain of the designed LNA over the Ka-band.

than 23 dB over the whole Ka-band band. It can be seen that the measured input matching is worse than originally designed. To study this we used an updated small-signal model presented in [7]. As can be seen from Fig. 6 similar tendency for worse input matching and also closer match for the measured S_{21} suggests that an improved input matching could be obtained by retuning the amplifier based on the updated small-signal model. The circuit is unconditionally stable over the whole frequency range ($\mu > 1$) [9]. The measured and the simulated μ-factors are illustrated in Fig. 7.

Noise figure measurement was carried out by Y-factor method with a diode noise source and a down-converter. The measured noise and insertion gain are shown in Fig. 8. Undulation in the measured noise figure can typically be observed when the output reflection coefficient of the noise source changes between hot and cold state. Also, this can be partly due to uncertainties in the ENR calibration [8]. An average of 1.9$-$dB noise figure was obtained across the Ka-band which is better than the simulated noise figure. The discrepancy might come from a higher transconductance ((g_m)) value and different pinch-off characteristics of the fabricated transistor. This enabled us to use a lower bias current for the amplifier while still having the same gain as in simulations. This lower bias current produces a lower noise performance for the LNA. The total simulated DC power was 620 mW whereas in the measurement we have used 433 mW of power.

Fig. 9 shows the large signal measurements over the operating frequency. The 1$-$dB output compression point (OCP) is 22 dBm at 38.5 GHz. We have also measured the third order intercept poit (IP3) with a tone separation of 1 MHz over the full Ka-band and plotted in Fig. 10.

IV. Conclusion

A full Ka-band GaN low-noise amplifier was presented for the first time. Measured results are compared to other published Ka-band GaN MMIC low-noise amplifiers in Table 1. The LNA presented in this work shows a wideband gain and noise characteristics while having a comparable figure-of-merit with previously published GaN LNAs which demonstrates the potential of utilizing a 100-nm GaN HEMT on silicon substrate technology for highly linear and wideband LNA design at mm-Wave frequencies.

Table 1. Comparison of Ka-band GaN MMIC low-noise amplifiers.

Technology	Frequency [GHz]	Noise Figure [dB]	Gain [dB]	1-dB OCP [dBm]	P_{DC} [mW]	FOM*	Reference
100-nm GaN/Si	26-40	1.9	> 23	12-22	433	11710	This work
100-nm GaN/Si	34-37.5	2.4	31	23-24	1300	11408	[7]
40-nm GaN/SiC	30-39.3	< 1.6	> 24	11	150	1860	[10]
100-nm GaN/Si	23-31	0.93-1.4	22-27.5	22-25	1080	12658	[11]
150-nm GaN/SiC	26-31	4	18-24	>12.5	800	26.5	[12]
150-nm GaN/SiC	28-31	3.7-3.9	14.4-19.6	n/a	560	n/a	[1]
100-nm GaN/Si	27-34	1.7	>20	n/a	1050	n/a	[2]
120-nm GaN/SiC	33-41	3	15	13	280	86	[13]

FOM = *Gain (lin)*frequency (GHz)*1dBOCP(mW)/((NF(lin)-1)*P_{DC}(mW))*
*FOM calculated at the highest 1-dB output compression point.

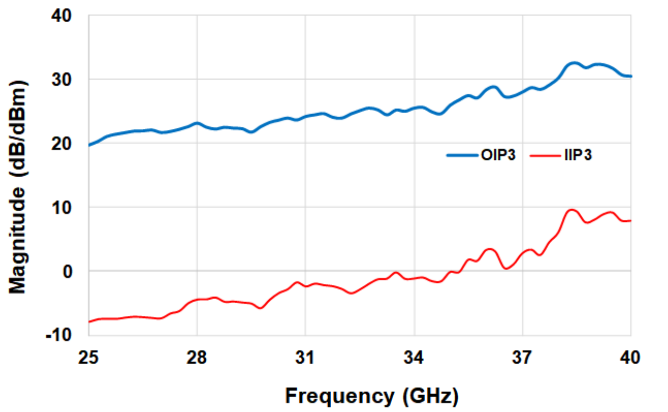

Fig. 10. Measured OIP3 and IIP3 with a tone separation of 1 MHz over the Ka-band.

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