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To the Graduate Council:

I am submitting herewith a dissertation written by Jung Won Park entitled "Characterization of materials and fabrication of active matrix thin film transistor arrays for electrical interfacing of biological materials." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Materials Science and Engineering.

Philip D. Rack, Major Professor

We have read this dissertation and recommend its acceptance:

Accepted for the Council:

Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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We have read this dissertation
and recommend its acceptance:

Michael L. Simpson

Thomas T. Meek

David C. Joy

Accepted for the Council:

Carolyn R. Hodges
Vice Provost and Dean of Graduate School

(Original signatures are on file with official student records.)

Characterization of Materials and Fabrication of Active Matrix Thin Film Transistor Arrays for Electrical Interfacing of Biological Materials

A Dissertation
Presented for the
Doctor of Philosophy
Degree
The University of Tennessee, Knoxville

Jung won Park
May 2009

Dedicated to my parents and wife

Abstract

Electrical interfacing between semiconductor devices and biological materials has been studied for live cell probing which will make it possible to perform direct electrical sensing of cells. To extend the applicability of extracellular and planar microelectrode arrays, recently vertically aligned carbon nanofibers (VACNFs) have been integrated with micro electrode arrays (MEA) for applications such as cell membrane mimics, gene delivery arrays, neuroelectrochemical interfacing arrays, superhydrophobic switches, and intracellular probes. The main drawback of VACNF-MEA devices are the low density of electrodes and passive addressing approach. In order to increase the number of elements of an MEA and enable both stimulation and recording on the same platform, an actively addressed thin film transistor (TFT) array platform was developed. Active matrix-TFTs are highly functional devices which have been used widely as backplanes in display electronics field over the past few decades. VACNFs were integrated onto the TFT array (TFT-VACNF) as they enhance the electrical sensitivity to the cell relative to standard planar arrays; furthermore, the vertical electrodes provide the potential for intracellular sensing within individual cells. This device platform provides great potential as an advanced microelectrode array for direct cell sensing, probing, and recording with a high electrode density and active addressability.

In this study, VACNFs were successfully integrated onto TFT devices to demonstrate a new microelectrode array platform. The materials and processes of the TFT structure were designed to be compatible with the requisite high-temperature (~700°C) and direct current Plasma Enhanced Chemical Vapor Deposition (dc-PECVD) VACNF growth process. To extend

the applicability of utilizing these vertical electrodes, this dissertation describes: the characterization and optimization of each layer for the TFT; the fabrication process and issues for active matrix TFT array; the critical device integration issues of VACNFs onto active matrix TFT arrays are elaborated; and the initial and final device characteristics are reported.

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I would like to thank my advisor Dr. Philip D. Rack for his support, his idea for this project, and continuous stimulating discussions. Most of all I would like to thank Dr. Seung-Ik Jun for mentoring and training me in all aspects of characterization, fabrication, and testing. I would also like to thank Seyeoul Kwon for working closely with and giving me valuable advice for this dissertation. I would like to thank the people at Center for Nanophase Materials and Science, Oak Ridge National Laboratory, Oak Ridge, TN for their support. Lastly I would like to thank my family. Most of all I would like to thank my wife Soyeon Kim for her understanding, love, and support.

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1. Introduction

1.1. Motivation of this work

1.1.1 Extra/intracellular cell probing

Electrical interfacing between semiconductor based devices and biological materials have been studied for live cell probing which could enable direct electrical sensing of live cells. Over the past ten years there has been a growing interest in the development of experimental techniques for cell probing from direct optical microscopy image detection to electrical silicon based device measurements [1-15]. These technologies are especially useful to research cell manipulation, cell detection, and gene delivery. First of all, cell manipulation has long been of considerable interest to biomedical researchers. Transgenic cells or manipulated cells by injecting proteins, dyes, or drug compounds have been studied. Second, cell detection is useful for medical diagnostics. The ability to detect small amounts of materials is important for monitoring specific cells. Finally, gene delivery techniques are essential for gene therapy which treats disease by adding new genes. The transfer of defined genetic material to specific target cells of a patient for the ultimate purpose of preventing or altering a particular disease state helps the new genes to target the right place in the body [1].

1.1.2 Microelectrode Array (MEA) device

Microelectrode arrays (MEAs) have been studied to investigate electrogenic cells and tissues by intra/extracellular stimulating and recording. A microelectrode array (MEA) is an arrangement of typically more than a few tens of electrodes with 100 ~ 500µm pitch allowing the probing of several sites for cell stimulation and extracellular recording at once [16-18]. Currently,

these devices are fabricated by conventional semiconductor fabrication processes (thin film deposition, lithography, and wet / dry chemical etching) with a high density of electrodes. However, the main drawback of the MEA is that only cells lying on the electrodes can be measured due to the relatively low electrode density relative to the size of the cells. In addition, cells may not adhere well on the electrodes and the cell-electrode contact may thus be compromised. As a consequence, the signal to noise ratio is not optimal and often the signal is not detected properly. Previously, to enhance the density of electrodes for cell sensing, an electrode array was addressed by laser irradiation, where the current was directly induced to the electrode just below stimulating cells [8-10]. However, this technique still has some disadvantages used in the driving electronics. Due to the passive driving operation, there were no switching devices, and each unit cell is addressed for more than one frame time, the effective voltage applied to the device must average the signal voltage pulses over several frame times, which results in a slow response time. The addressing of a passive matrix also produces a kind of crosstalk that influences electrical signals because non-selected electrodes are driven through a secondary signal path.

1.2. Thin film transistor (TFT)

1.2.1 History

The thin film transistor (TFT) has been used as a capacitor and electronic computer in the past 60 years. Indeed, its basic operation concept is very similar those of the metal oxide semiconductor field-effect transistor (MOSFET). The earliest type of transistor was suggested by Lilienfeld [19], Brody [20], and Heil [21]. Their concepts for operating transistor using field driven by a capacitor were extensively developed by Shockley [22]. He introduced the MOSFET

and established the concept of 3 terminal operation; gate, source, and drain. After that, many reports were published for thin film transistors using CdS film as the active semiconducting layer, and SiO_x used as the gate dielectric layer. When CdS film is used as an active layer, applications are limited due to its high leakage current. Additionally, instability problems also prevented its wide use. During 20 years, however, thin film transistor physics have been very well established. Even though most concepts were adopted from the P-N junction diode, or MOSFET which is based on generating an inversion region at the channel, TFT's operation concept is based on an accumulation regime. Dramatic evolution in the field of TFT occurred in the 1970s with the introduction of crystalline silicon TFTs [23] and hydrogenated amorphous silicon (a-Si:H) active layer TFTs [24].

After the first hydrogenated amorphous silicon thin film transistor (a-Si:H TFT) was initially proposed by LeComber as an electronic switching device in 1979 [24-25], a-Si:H TFTs have attracted increased attention over the past few decades due to their promising potential for applications involving large-area integration such as matrix addressing of liquid crystal display (LCD) [26-35], optical sensors [36-40], chemical/biological sensors [41-43], and medical imaging sensors [44-45]. Using amorphous silicon, lower leakage current can be achieved below the pico-ampere range, while CdS TFT could only realize nano-ampere ranges. Low leakage current means that a-Si based TFT can be used as low current applications such as liquid crystal flat panel displays, and solar cell panels. In 1979, with the advent of hydrogenated amorphous silicon could be doped with donors or acceptors to induce conductivity, and hydrogenation could passivate the large density of dangling bonds in the silicon amorphous network. Defect states in the gap in the pure amorphous silicon caused by band tails of localized state extended into the band gap and induce a charge trapping and release from these localized

states consequently. However, hydrogen passivated dangling bonds removed these localized states.

Since LeComber suggested hydrogenated amorphous silicon based TFTs, the fundamental a-Si:H TFT operation sequence is established very well. When a positive voltage is applied to the gate electrode, the band bending at or near the gate dielectric/amorphous silicon interface is increased and electrons accumulate near the interface to form the conduction channel. When a negative bias is applied to the gate electrode, the channel region is operated in the depletion regime. When in accumulation, a positive drain voltage applied to the drain electrode induces a drain-source current to flow from the drain to the source electrodes through a n^+ a-Si:H contact layer, and the intrinsic a-Si:H conduction channel.

1.2.2 TFT structures and fabrication step

There are a number of thin-film transistor structures according to the position of the active layer, gate dielectric, and gate electrodes. Among them, staggered and inverted staggered structures have been used widely [46]. Figure 1-1 illustrates the fabrication process of staggered TFT. A staggered TFT has a top side gate electrode. Fabrication of a typical top-gate staggered TFT starts with the formation of the source/drain electrodes on the substrate with buffer layer. In order to make an ohmic contact, a n^+ a-Si is deposited directly on the metal layer. In this case, the n^+ a-Si:H and the source and drain electrode must be patterned to separate the source and drain region with one photolithography step. During this process, the n^+ a-Si layer is exposed to air, thus, any oxide formed at the top surface should be removed. Following this step, intrinsic a-Si:H and silicon nitride (SiN_x) gate dielectric film are deposited sequentially in a plasma enhanced chemical vapor deposition (PECVD) chamber, and the gate metal layer is formed

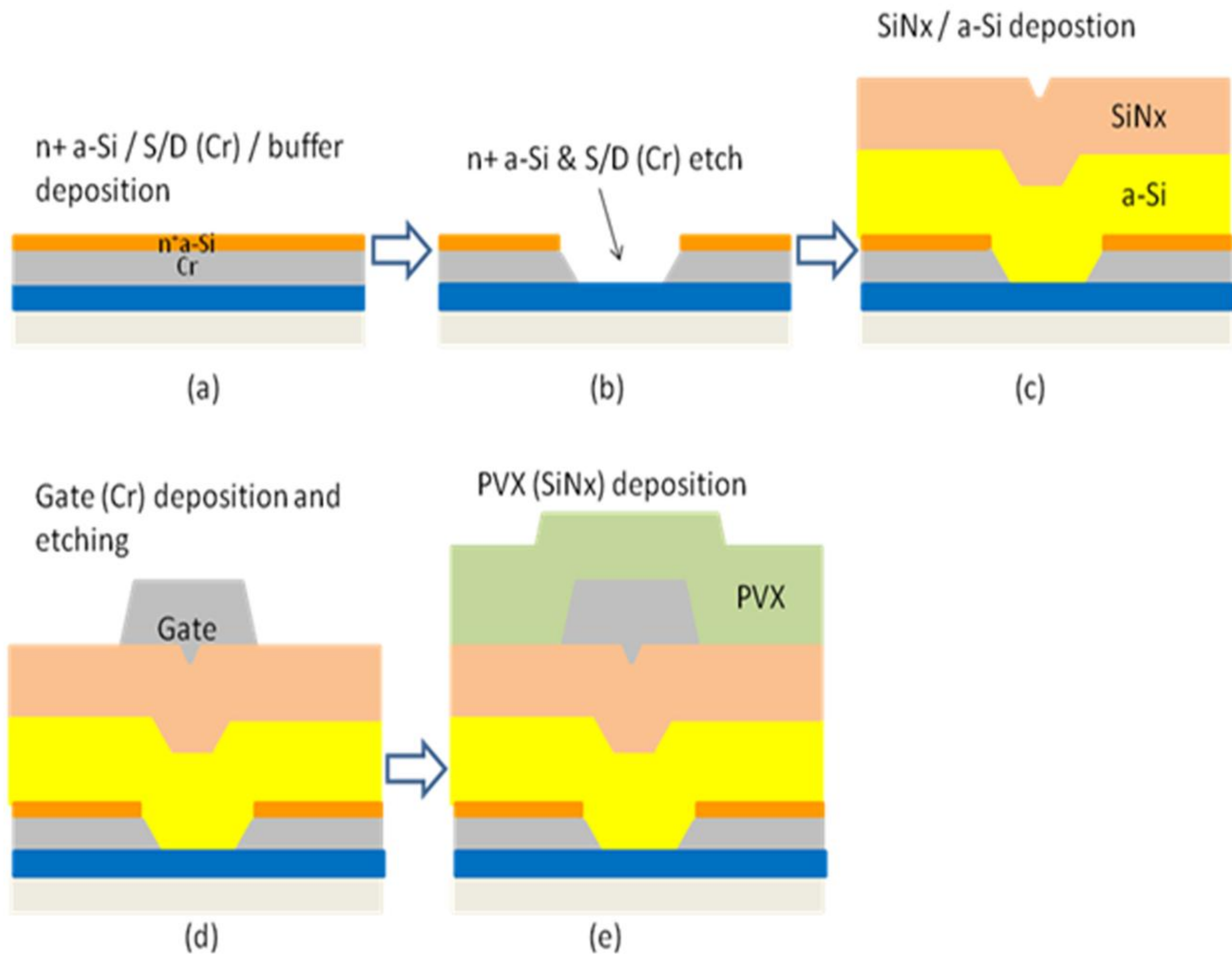


Figure 1-1.The fabrication process flow and cross sectional view of staggered thin film transistor (staggered TFT)

on the SiN_x. After patterning gate electrodes, a passivation (PVX) layer is deposited in a PECVD to protect the device from moisture in the air.

For an inverted-staggered a-Si:H TFT, the gate is first formed on the substrate. Thus it is referred as bottom gate structure. The inverted-staggered TFT, widely used in the manufacturing of active-matrix LCD panels, is commonly fabricated as the back channel etched (BCE) structure or the channel passivation (CHP) structure using etch stop layer pattern. Figure 1-2 and 1-3 show the structure and fabrication steps for BCE-TFT, and CHP-TFT. Many companies are currently using these two structures depending on their specific purpose of the device. For both structures, the gate electrode patterning is considered a critical step to determine device stability since the step coverage of the gate electrode determines the other layer's continuity. Next, the gate dielectric SiN_x layer is deposited for a-Si:H based TFTs on the patterned gate electrodes. Even though SiN_x has a higher interface density than SiO_2, SiN_x is usually used as gate dielectric for a-Si:H TFT because the dielectric constant value of SiN_x is two times greater than SiO_2. The BCE a-Si:H TFT saves at least one photo-mask step for fabrication compared to the CHP a-Si:H TFT; however, it needs a rather thick (~200nm) intrinsic layer to have enough process margin for n^+ a-Si etching. The n^+ a-Si layer and metal source and drain electrodes are deposited on the a-Si active layer, respectively. After patterning the source and drain electrodes, the n^+ a-Si layer between the source and drain electrode must be over-etched to remove the n^+ a-Si over the channel region. If n^+ a-Si residues remain on the channel, the electrical characteristics will have diode characteristics because of the conduction in the n^+ layer. In a CHP structure, however, the back channel is protected by another etch-stop SiN_x layer, so the n^+ a-Si etch process has more process latitude and the intrinsic a-Si:H can be thin as 50nm. Actually, as the thickness of active

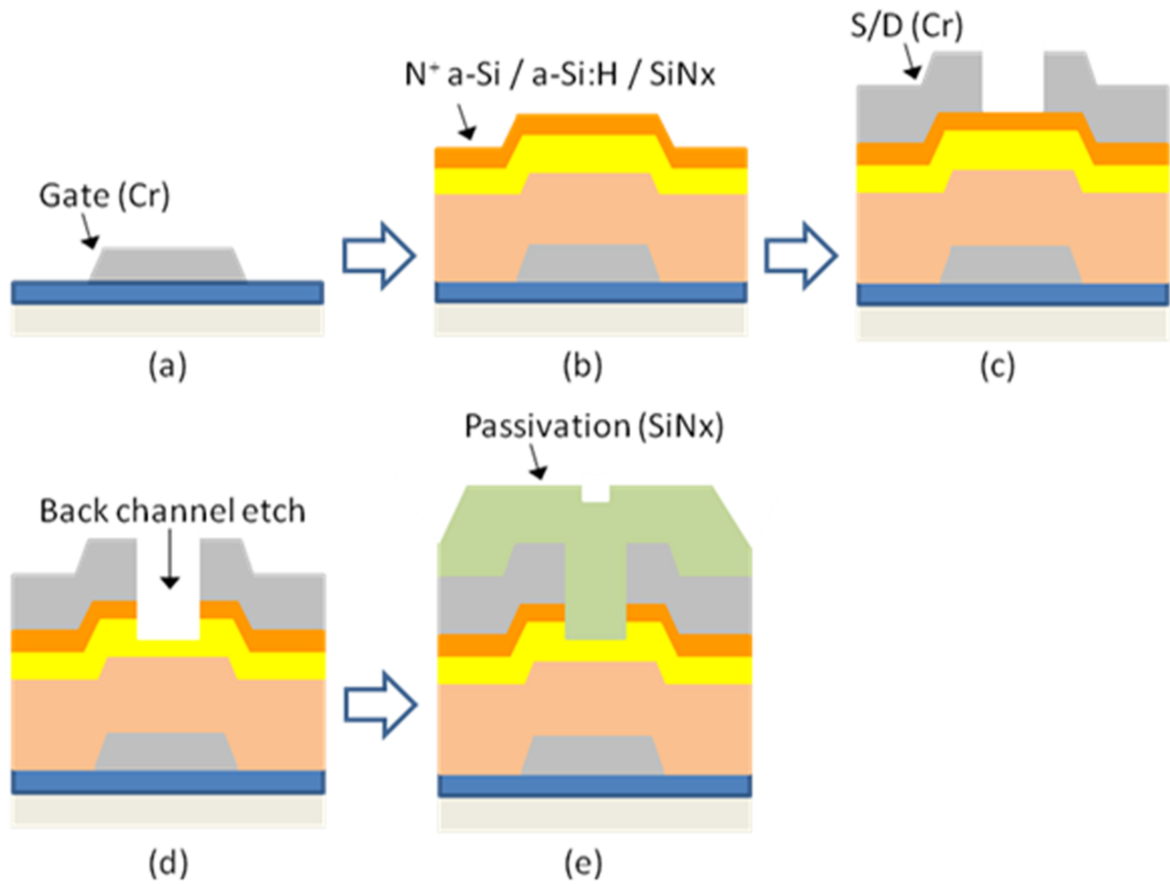


Figure 1-2.The fabrication step and cross sectional view of Back channel etched TFT (BCE-TFT)

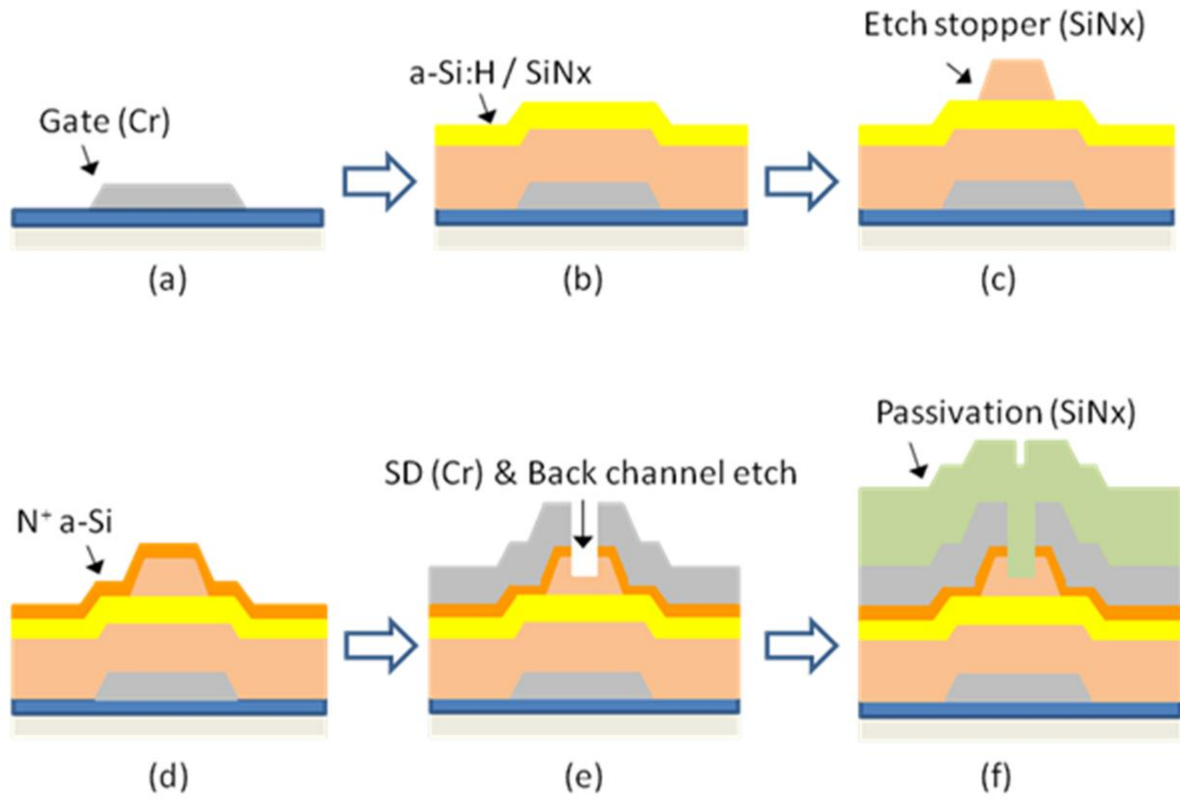


Figure 1-3.The fabrication step and cross sectional view of channel passivation TFT (CHP-TFT)

layer is reduced, the field-effect mobility of electrons in the active layer increase until the active layer fully accumulates. However, the processing is a little more complicated than that of the BCE a-Si TFT, since there is an additional photo mask step. After SiN_x/a-Si:H/SiN_x trilayer deposition, the etch-stopper island must be patterned, after which the n^+ a-Si layer is deposited while the BCE structures, gate dielectric SiN_x, intrinsic a-Si:H, and n^+ a-Si layers can be deposited sequentially in a single pump-down in a PECVD chamber. While the CHP structure requires more process step to produce, the CHP structure has much less photo-induced leakage current, and its extrinsic field effect mobility can be a little higher because the a-Si:H layer. Note that the field effect mobility degrades when increasing the a-Si:H layer thickness because of the series contact resistance between the n^+ a-Si and channel. Similarly, the photo-induced leakage current of an a-Si:H TFT is reduced by decreasing the a-Si:H thickness, optical absorption of light is minimized. To achieve a lower photo-induced leakage current in the "off" state, active islands are also patterned to decrease the area of a-Si:H film. Finally, passivation layer SiN_x is deposited to protect the device and channel region; particularly in the channel region of BCE structures as it is directly exposed to the ambient.

1.3. Vertically Aligned Carbon Nanofiber (VACNF)

To extend the applicability of extracellular and planar microelectrode arrays, vertically aligned carbon nanofibers (VACNFs) [12] have been integrated with microfabricated structures for applications such as cell membrane mimics [47], gene delivery arrays [48], neuroelectrochemical interfacing arrays [49], superhydrophobic switches [50], and intracellular probes [13]. Carbon nanofibers (CNF) are cylindrical or conical structures with diameters from a few to hundreds of nanometers and lengths ranging from less than a micron to hundreds of

microns [12]. Melechko et al. reported that vertically aligned carbon nanofibers (VACNF) were used as nano-scaled devices including nano-manipulators, field-emitters, fluidic pipes, cellular-scale material delivery vectors, and electrochemical sensors [13-14]. In particular, VACNFs have been used to impale the cell on the microelectrodes to manipulate and sense individual cells on the nanoscale [15]. A scanning electron image of a VACNF growth by direct current (dc)-PECVD is shown in Figure 1-4. The VACNF was grown at 700°C and a 10nm thick Ni catalyst was used for the growth. In order to increase the number of elements of an MEA and enable both stimulation and recording on the same platform, an actively addressed TFT array was developed. VACNFs were integrated onto the TFT array as they enhance the electrical sensitivity to the cell relative to standard planar arrays; furthermore, the vertical electrodes provide the potential for intracellular sensing within individual cells. To extend the applicability of utilizing these vertical electrodes, this dissertation describes the characterization and optimization of each layer for TFT, fabrication process and issues for the active matrix TFT array, and integration of VACNFs onto active matrix TFT array.

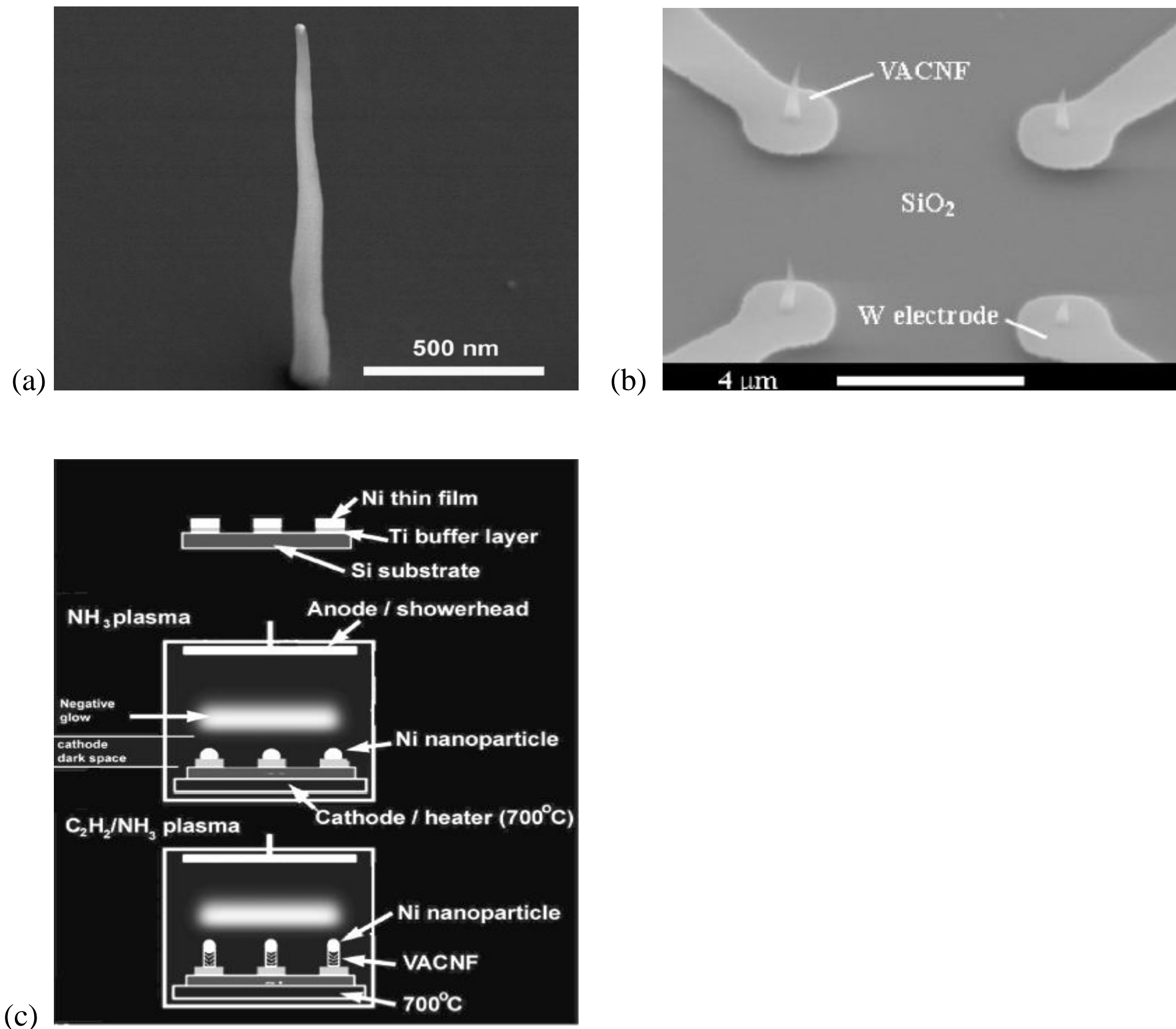


Figure 1-4. (a) SEM image of a VACNF grown by dc-PECVD, (b) SEM images of four VACNF probes on individual tungsten electrodes, and (c) Schematic diagram of dc-PECVD process for growing VACNFs (images adopted from M. Gulliorn, T. McKnight, A. Melechko, V. Merkulov, P. Britt, D. Austin, D. Lowndes, and M. Simpson, “Individually addressable vertically aligned carbon nanofibers-based electrochemical probes”, J. Appl. Phys., Vol. 91(6), p3824-3828, (2002))

2. Fabrication and characterization of thin films for TFT array and integration of TFT-VACNF

2.1. Metal electrode; chromium (Cr)

2.1.1. Background

In choosing a metal electrode material, several factors should be considered. First of all, a low resistivity gate and/or source-drain metal electrode is essential for high speed operation and low-power consumption. Low resistivity gate electrodes reduce the charging time to gate dielectric material. The total turn-on resistance (R) of thin film transistor (TFT) is expressed as

$$R = R_S + R_{CH} + R_D$$

Where, R_S is the resistance associated with the source contact, R_D is the resistance associated with the drain contact, and R_{CH} is the channel resistance. For good TFT operation, R_{CH} should be the limiting factor to decide the transfer characteristics of current-voltage relationship, therefore R_S and/or R_D must have a low resistivity. The resistance in the contact region (R_S and/or R_D) can be written as

$$R_S = \rho \frac{L}{A} = \rho \frac{L}{Wd} = \frac{\rho}{d} \frac{L}{W} = R_s \frac{L}{W}$$

Where ρ is resistivity of metal electrode, L and W is the length and the width of contact region, and the source-drain electrode overlaps the underlying ohmic contact layer, d is the metal electrode thickness, and R_s is the sheet resistance.

Good thermal stability is also required to achieve a stable device operation. If the thermal stability of the metal is low, inter-diffusion can occur during the fabrication, because the film deposition temperature is up to 600°C when Low Pressure Chemical Vapor Deposition (LPCVD) is used. This may result for instance in the formation of metal silicides. Therefore, for material selection for metal electrode, resistivity and thermal stability should be considered simultaneously. Even though Al and Cu have a very low resistivity (ρ_{Al}= 4~5 x10^{-6} and ρ_{Cu}=3~4 x 10^{-6} ohm-cm) and optimized for using it in high-speed electronic device, their poor thermal stability prevent them from being used in the VACNF integration. Another drawback is that inter-diffusion between many metals and silicon occurs above 500°C. As mentioned, high temperature processing may form a silicide or cause metal residues in the silicon film, which results to increase resistivity. Metal residues in gate dielectric films are particularly problematic as they can inhibit charge transport in the active layer when the metal residues elecromigrate under the gate bias.

Previously, Jun [51] studied molybdenum tungsten (MoW) as the metal electrode to achieve a low resistivity and good thermal stability by changing composition of atomic fraction of Mo and W. Even though low resistivity is achieved by following Nordheim's equation, lower etching selectivity prevents it to be used as metal electrode. Since the gate dielectric and active layers are based on silicon, fluorine based reactive ion etch recipes are used to etch these layers, which also attacks the MoW layer during etching procedures. Thus, poor etching profile can occur and etching damages occurs on the MoW electrodes during the final via etch [51].

To realize a better etching selectivity with a low resistivity and good thermal stability, chromium (Cr) metal is used as gate and source-drain electrode since Cr has a high etch selectivity during fluorine based plasma etching. Cr is known as stable material under high

temperature process environment [52]. However, some reports indicated that Cr silicide can be formed at 500 ~ 700^oC when very thin Cr film is directly contacted with silicon based compounds or silicon materials [53-55]. During fabrication of TFTs, Cr is rarely exposed to high temperature with silicon based materials, it can be ignored because inverted staggered structure TFT does not require this procedure and staggered structured poly-crystalline silicon TFT need a higher temperature and doped silicon deposition.

2.1.2. Experimental

Cr film is prepared by Radio Frequency (RF) magnetron sputtering. The variable deposition conditions were gas composition (pure Ar and 5% hydrogen-Ar), working pressure, substrate power, while Cr target RF power was fixed at 200 watt, and substrate temperature was 200^oC. A Cr target was 99.95% pure, 2.00 inch diameter and 0.25 inch thickness (Kurt J. Lesker, PA, US). The initial deposition is that 200 W RF power, 200^oC temperature, 25 sccm flow rate of 5% hydrogen-Ar gas, 3mTorr pressure, and no substrate power. The resulting baseline deposition rate was 5.0nm/min and the resistivity of thin film was 2.45 x 10^{-5} ohm-cm for a 250 nm thickness. To characterize a lower resistivity of the film, working gas, pressure, and substrate power conditions were varied.

2.1.3. Results and discussion

Figure 2-1 represents the film resistivity and deposition rate of the Cr layer when pure Ar and 5% hydrogen-Ar are used as working gas with 5mTorr pressure at 200^oC temperature without substrate power. Depending on working gas, pure Ar gas flow results a lower resistivity and higher deposition rate than 5% hydrogen-Ar gas. To compare it to previous result of 3 mTorr

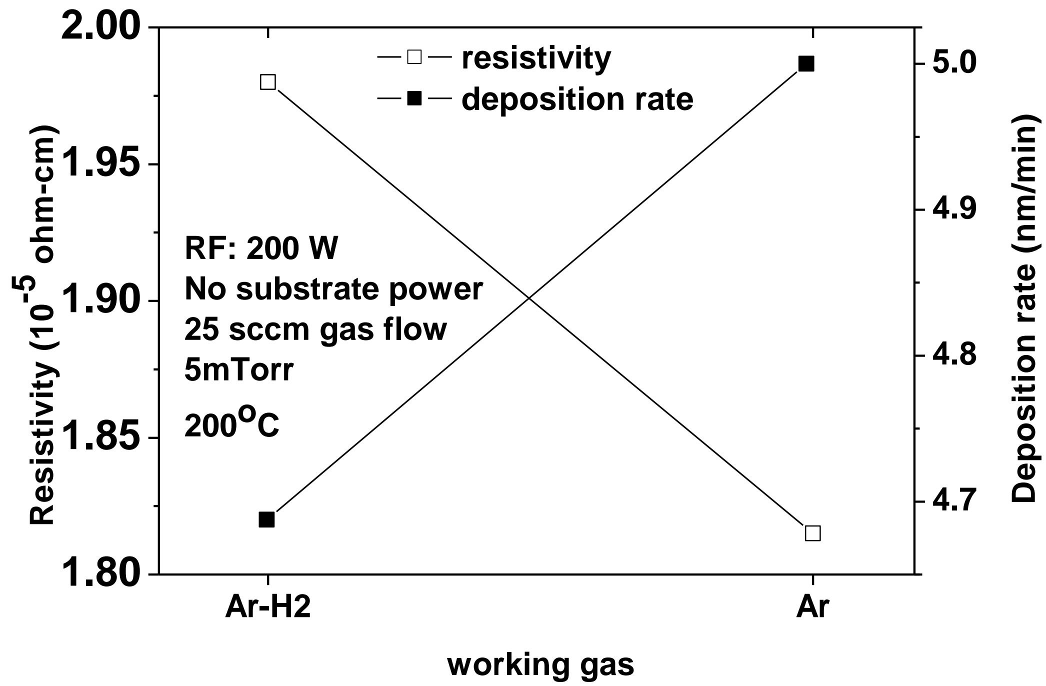
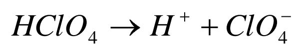


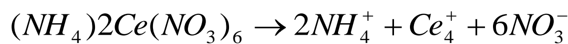
Figure 2-1. Target voltage and refractive index as a function of processing gas; Ar and 5% hydrogen-Ar

conditions, 5mTorr conditions resulted in a 1.98 x 10^{-5} ohm-cm Cr film resistivity. To investigate the substrate power effect, substrate power is varied with 0, 5, 10, and 25 watt. The results are shown in Figure 2-2. As increasing substrate power, the resistivity of Cr film decreased modestly for the 5W power and did not a significant change at higher powers. The deposition rate decreased modestly at 5W and then more severely at higher substrate power. The initial decrease in the sputter rate and decrease in resistivity at 5W is attributed to densification possibly a decrease in the oxygen incorporation due to the energetic ion bombardment. Subsequent decreases in the deposition rate could be due to re-sputtering and damage effects which likely cause the decreased sputtering rate and increased resistivity. While a slight improvement in resistivity was realized for the 5W substrate bias, for simplification, 0W substrate bias was originally set as the initial electrode sputtering condition.

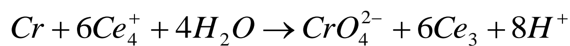
The etching of Cr film is essential to make the gate and source-drain pads and active addressing lines. The method of Cr etching is usually wet etch process. A CR-14S etchant (Cyantek) wet etchant was used for etching the Cr layers. The solution contains 9%$(NH_4)_2Ce(NO_3)_6$+6%$(HClO_4)$+H_2O, and the etch mechanism for Cr by this wet etchant is



$$HClO_4 \rightarrow H^+ + ClO_4^-$$



$$(NH_4)2Ce(NO_3)_6 \rightarrow 2NH_4^+ + Ce_4^+ + 6NO_3^-$$



$$Cr + 6Ce_4^+ + 4H_2O \rightarrow CrO_4^{2-} + 6Ce_3 + 8H^+$$

The conventional etch rate is ~ 66.7nm/min at a room temperature with agitation and the CR-10S wet etchant had a 150 nm/min etch rate at 45°C with agitation. Almost all Cr wet etching described in this dissertation was done using CR-14S. As will be elaborated in more detail later,

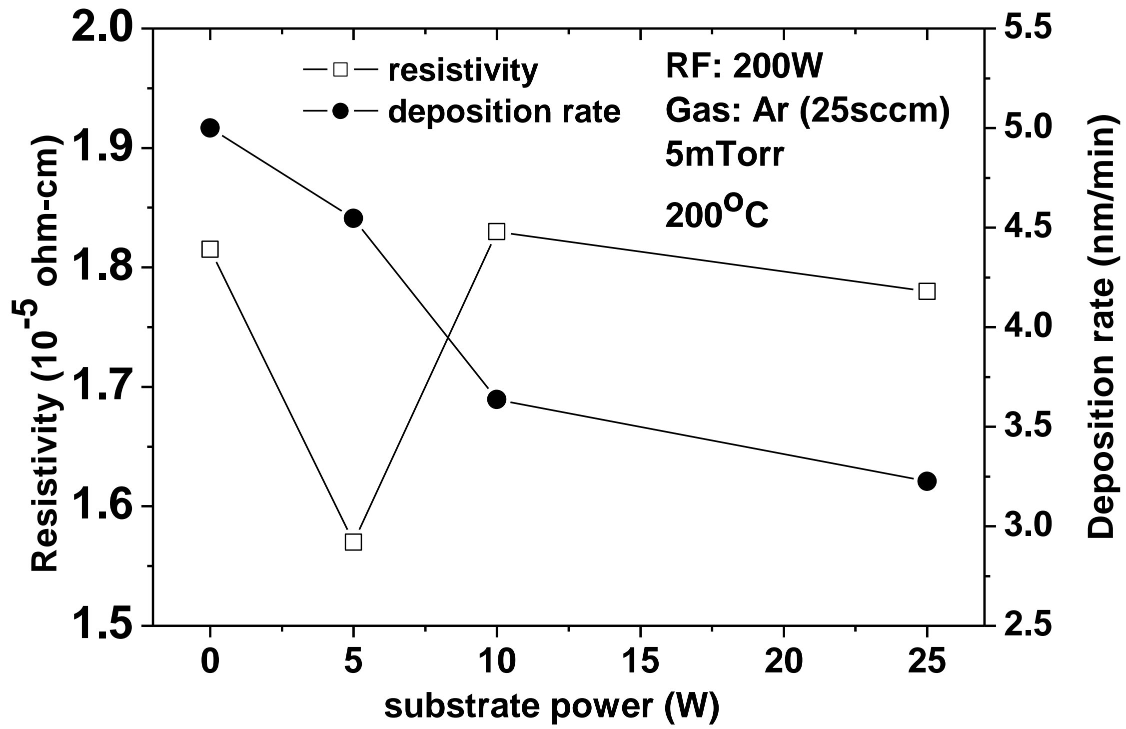


Figure 2-2. Resistivity and deposition rate of Cr film as a function of substrate power during deposition

the etch profile of the Cr etching is critical to achieve a good step coverage, so a shallow angle isotropic etch rate was desirable.

2.2. Gate dielectric materials; SiO_2 and SiN_x

2.2.1. Sputtered silicon dioxide (SiO_2) film

2.2.1.1. Background

Silicon dioxide (SiO_2) has been widely used as a gate dielectric and passivation layer of thin film transistor device. Sputter deposition is an attractive process since it requires a lower temperature relative to conventional thermal growth, LPCVD, and PECVD processes. A room temperature deposition of silicon dioxide using sputter deposition is possible, however, the lower breakdown strength of the film prevents it as application as a gate dielectric layer. For conventional sputtering technique, single SiO_2 solid target has a low deposition rate since SiO_2 has an extremely low sputtering yield (S_{si}=0.6 and S_{SiO2}=0.13 atoms/ion for 1 KeV Argon). Therefore, to achieve fast deposition rate, reactive sputtering can be used to deposit SiO_2 films. In reactive sputtering, SiO_2 film is deposited on a substrate by sputtering from solid silicon targets in the presence of a reactive oxygen gas, which is mixed with an inert working gas (typically Ar). In the case of the reactive sputtered SiO_2 film, room temperature deposited material also has low breakdown strength and typically has high trap densities. In this work, we optimized the silicon dioxide reactive sputtering process with high capacitance value, stoichiometric composition, and high breakdown strength.

2.2.1.2. Experimental

RF magnetron sputtering system (AJA, ATC2000) was used to deposit SiO_2 film. The base pressure was maintained below 5.0 x 10^{-7} Torr to reduce the contamination of the film. RF power, substrate bias voltage, temperature, and flow rate of 5% hydrogen-Ar gas was fixed at 200 watt, 150 volt, 300°C, and 25 sccm. A pure undoped silicon target (99.999%) of 2 inch diameter and 0.25 inch thick was used. The film thickness and refractive index value was measured using a reflectometer with Deuterium Lamp (Filmetrics F20/40 Advanced Thin Film Measurement System). The reported thickness and refractive index value is an average of at least three measurements over each sample. Furthermore, in order to measure the current-voltage relationship to get breakdown strength and capacitance-voltage relationships, metal-insulator-silicon (MIS) structures were fabricated. Silicon dioxide films were deposited on single crystalline silicon wafer (n-type: phosphor doped). After depositing the SiO_2 film, 130nm Cr film was deposited onto the sample and patterned to leave a metal contact pad. The Cr deposition process was described previously. After Cr layer formed, SPR^{TM}220-2.1 photoresist was spun onto the whole wafer with 3000rpm for 60 seconds. A soft baking procedure was also done at 90°C for 90 seconds. Photolithography work was done using GCA auto-stepper. Next a post expose bake (PEB) was done for 90 seconds with 90°C. The photoresist was developed using a CD-26 developer for 60 seconds. After developing, hard baking was done at 90°C for 90 seconds. Cr is etched by CR-10S at 45°C with agitation for 120 seconds. Finally, photoresist is removed by micro-remover (Cyantek) for 20 minutes. The capacitance was evaluated with a Keithely 590 C-V analyzer and the dielectric breakdown strength was evaluated with a Keithely 2400 source-meter on a Signatone Checkmate probe station system.

2.2.1. 2. Results and Discussion

In order to evaluate reactive sputtering hysteresis curve, the oxygen flow rate was varied from 0 to 10 sccm while 5% hydrogen-Ar gas flow rate was fixed at 25 sccm. Other conditions were also fixed; RF power was 200 watt, substrate bias was 150 volt (10 watt), 300°C temperature, and 3mTorr pressure. Figure 2-3 shows the target voltage and refractive index (n) results as a function of oxygen flow rate.

As oxygen flow rate increased, target voltage decreased since the silicon target was covered by oxygen molecules, which when fully covered and oxidized results the similar deposition condition to that of a SiO_2 target (oxide mode). The abrupt decrease in target voltage is a result of the secondary electron yield change from Si to SiO_2 and the plasma impedance change when oxygen flows. Additionally, since the silicon target can be oxidized easily with a low oxygen flow rate at high pressure regime, the working pressure was fixed at 3mTorr. To determine the metal mode and oxide mode, refractive index values were compared to ideal stoichiometric composition (n_{SiO2}= ~1.46).

Based on the hysteresis curve, films were sputter deposited with oxygen flow rates of 4.4 and 7.5 sccm to represent the metal mode condition and the oxide mode, respectively. Figure 2-4 show the deposition rate change as a function of oxygen flow. Since the deposition rate is proportional to the sputtering yield, as the mode is changed from metal to oxide mode, the sputtering rate was decreased significantly. To measure the current-voltage and capacitance-voltage relationship, MIS structures were fabricated following the lithography process using GCA-auto stepper previously described. Figure 2-5 shows the schematic MIS structures, which were used to measure these characteristics. Two samples were prepared; metal mode SiO_2, 50nm

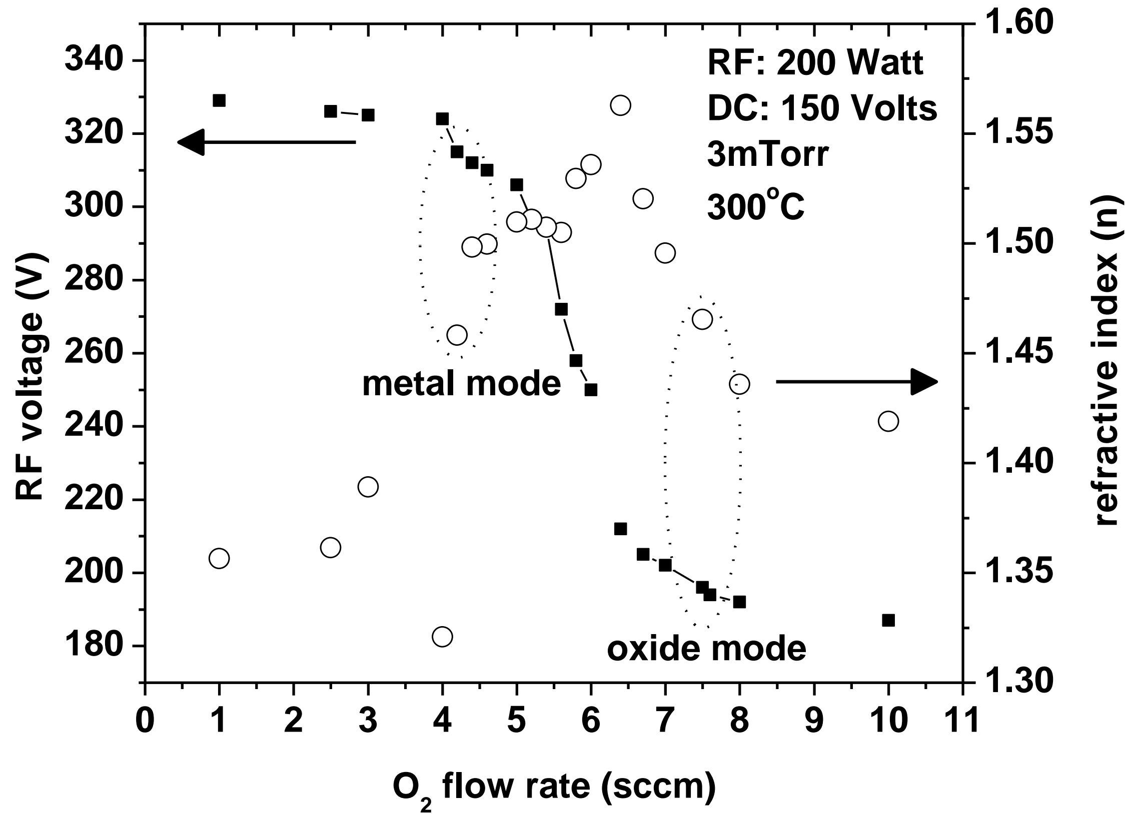


Figure 2-3. RF voltage and refractive index change as a function of increasing oxygen flow rate

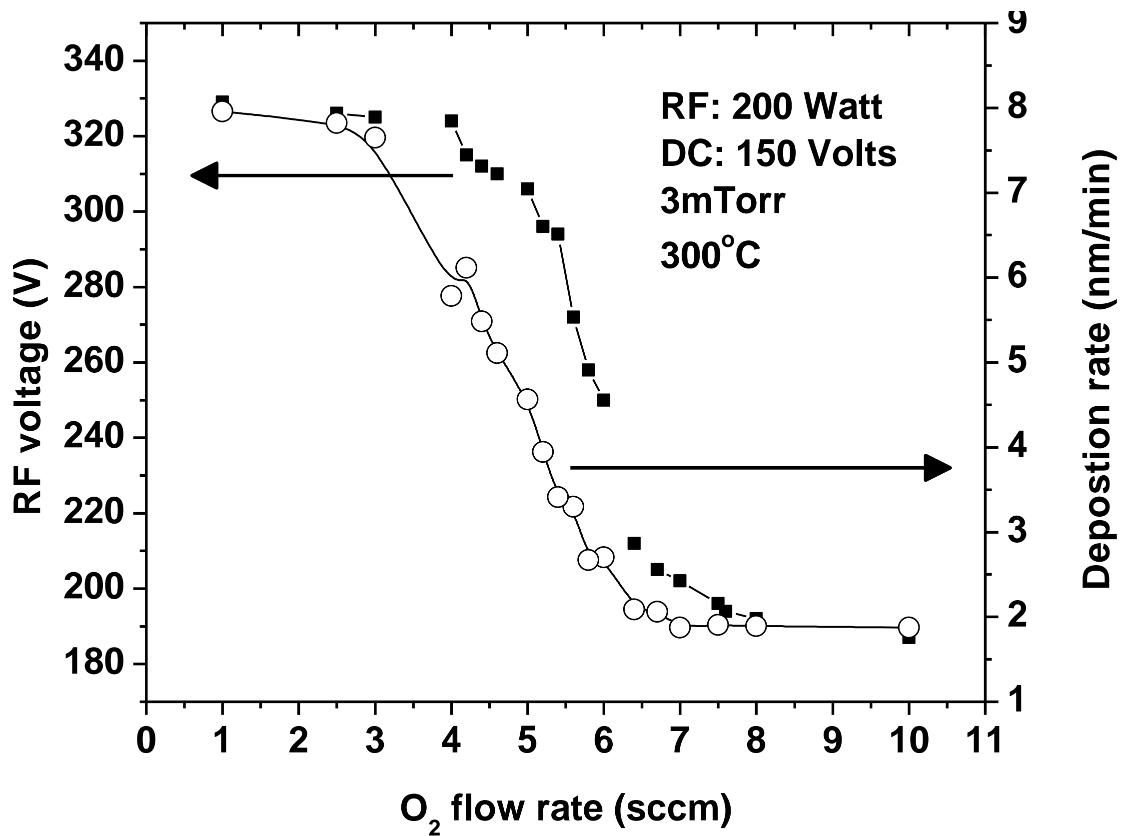


Figure 2-4. Deposition rate of SiO_2 film as a function of reactive oxygen flow rate

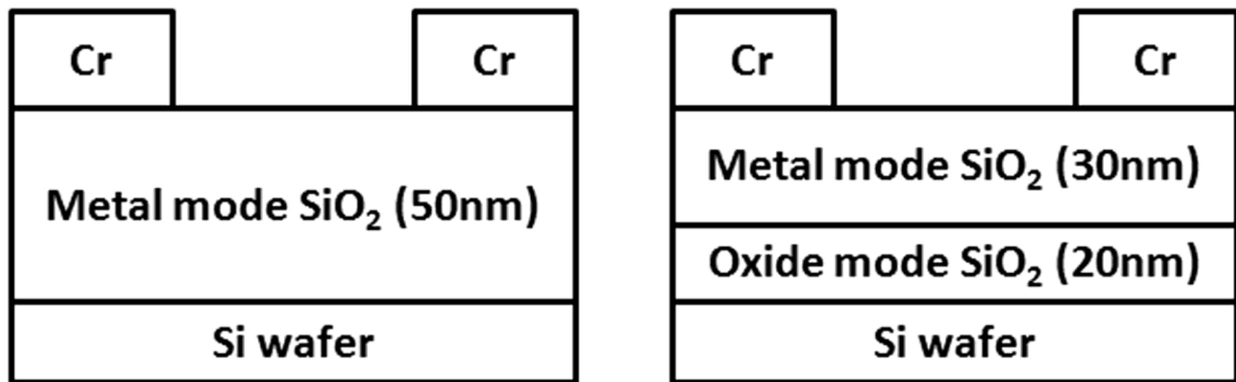
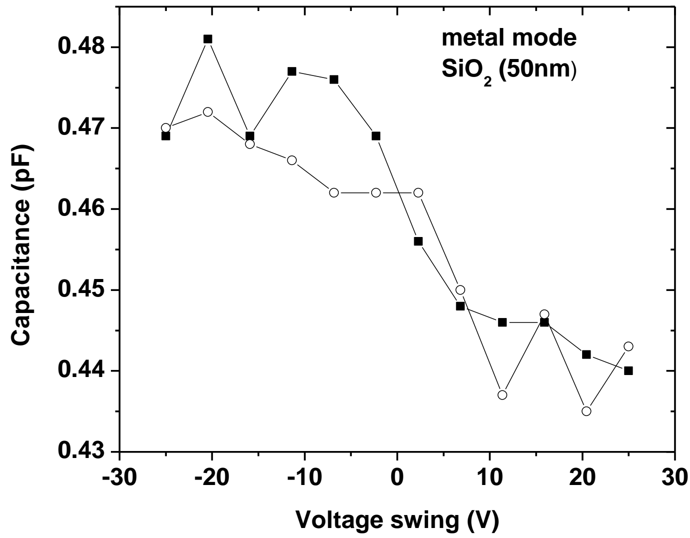


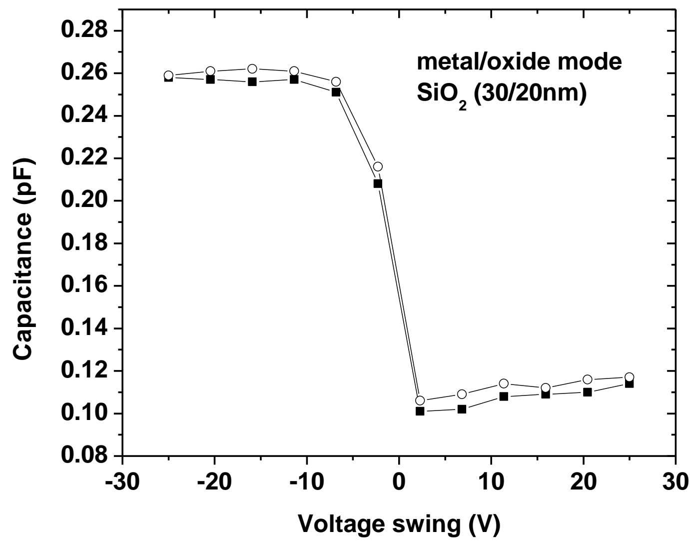
Figure 2-5. MIS structure for measuring electrical characteristics of dielectric layer.

thick, and double layer (metal/oxide mode, 30/20nm thick). Figure 2-6 shows the capacitance-voltage characteristics of MIS switching device fabricated by sputtered chromium, silicon dioxide on single crystalline silicon wafer as a function of gate voltage swing.

As shown in Figure 2-6, the double layer structure shows the better capacitance characteristics for charge build up, which is proportional to the ratio of C and Co. Additionally, double layer structure has a lower flat band voltage shift characteristics indicating that there are less defects which is consistent with the expectation that oxide mode films have higher quality and are more dense than metal mode films which can be slightly sub-stoichiometric. The I-V curve measured from double layered silicon dioxide is shown in figure 2-7 which demonstrates 3.47 MV/cm breakdown strength; this relatively poor value is not sufficient to be used as a gate dielectric for the TFT-VACNF application.



(a)



(b)

Figure 2-6. Capacitance of sputtered SiO_2 film (a) metal mode deposition (50nm thick) and (b) dual mode deposition (metal mode/oxide mode; 20/30 nm thick)

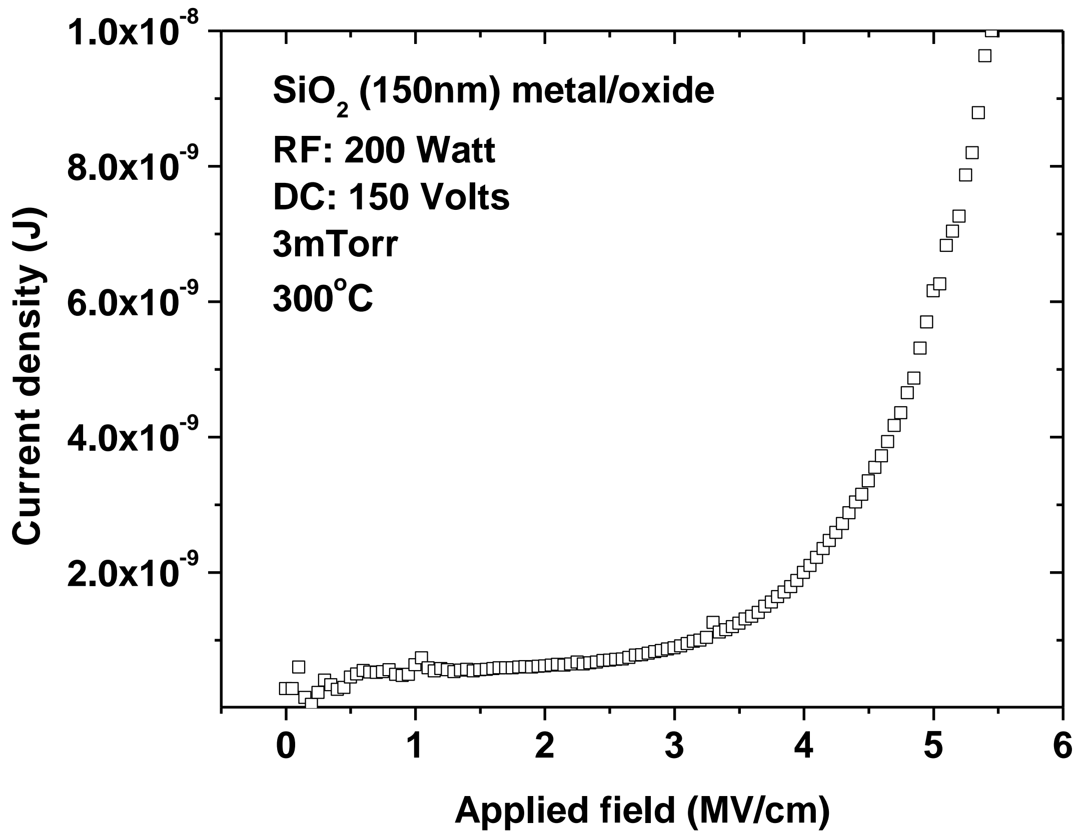
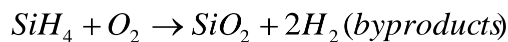


Figure 2-7. Breakdown strength of sputter SiO_2 film (metal/oxide mode)

2.2.2. Plasma Enhanced Chemical Vapor Deposition (PECVD) silicon dioxide (SiO_2) film

2.2.2.1. Background

PECVD silicon dioxide films play a critical role in several different areas of TFT technology. Briefly, SiO_2 can be used as a buffer layer on bare silicon wafer, gate dielectric layer, and passivation layer. For amorphous silicon based TFT, silicon oxide is rarely used as gate dielectric because its low dielectric constant (k), while poly crystalline silicon based TFT, and fast driving circuit device are usually using SiO_2 film as gate dielectric since the field effect mobility of silicon is fast enough to switching the channel region and it has a negligible interface density with silicon layer. In other words, it can be used as a good insulating layer for TFT structure due to high breakdown strength. Most oxide films are deposited at relatively low temperatures, from 200°C to 500°C using CVD techniques since it has a better step coverage. Silane and oxygen are commonly source gases for PECVD silicon dioxide deposition (along with Ar and nitrogen carrier and dilutant gases). The general reactions for SiO_2 from these gases are;



$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2(byproducts)$$

Or using SiH_4 and N_2O gas plasma, the brief sequence of deposition process is;

$$SiH_4 + N_2O \rightarrow SiO_2 + byproducts$$

2.2.2.2. Experimental

An Oxford PECVD system was used to deposit SiO_2 films. The deposition condition for PECVD SiO_2 film was 20 Watts RF power, 1000mTorr pressure, 5%SiH_4-Ar/N_2O (85/157 sccm) gas flow rate, and 350°C temperature. The deposition rate of SiO_2 film was nominally 69nm/min.

It has an ideal stoichiometric composition and a refractive index ~ 1.46. Another process was explored for SiO_2 deposition which used 140 Watts RF power, 1600mTorr Pressure, 5%SiH_4-Ar/N_2O/N_2 (600/1500/400 sccm) gas flow rate, and 350^oC temperature. The deposition rate of SiO_2 film was 217nm/min. It has a higher deposition rate rather than the former process. However, it had a higher refractive index (~ 1.49) suggesting it is non-stoichiometric. To measure the breakdown strength, the same MIS (Cr/SiO_2/Si wafer) structures were fabricated. SPR^{TM} 220-2.1 photoresist was used with a 3000 rpm spin speed for 60 seconds which resulted in a thickness of 1.75 µm. A resist pre-bake resist (soft bake) was done at 90^oC for 60 sec to enhance the adhesion of photo resist on the substrate, and to relieve the stress in the photoresist through thermal relaxation. Photo lithography was done using a Quintel contact aligner. Using the vacuum mode, an exposure time of nominally 4.6 seconds was used. After resist exposure, a post exposure bake (PEB) was done at 115^oC for 90sec. A PEB is used to minimize standing waves in resist. Resist development was then done using CD-26 developer for 60 seconds. Next a resist post-bake (hard bake) was done at 115^oC for 90sec. A descum process based on an oxygen plasma was performed to remove any photoresist residues which could compromise the etching. The descum employed a Technics reactive ion etching (RIE) system with a condition of 400 watts RF power, 10 sccm flow rate of O_2, 150mTorr pressure, and a descum time of 30 seconds. For Cr etching, CR14S wet etchant was used at room temperature following SiO_2 film was etched using RIE. The etching condition was that 30 watts RF power, 2000 watts ICP power, SF_6/Ar(45/1 sccm) gas, 10 mTorr, 15^oC temperature. After the etching, the photoresist was stripped in the wet bath with Microposit^{TM} remover 1165 for 30 minutes. After that, a 60 second descum procedure was applied to remove the photoresist residues. This photolithography process

is the standard photolithography process used in this work and will be the process lithography process implied unless stated otherwise.

2.2.2.3. Result and discussions

The main drawbacks of sputtered silicon dioxide (low breakdown strength and poor step coverage) can be overcome using PECVD silicon oxide. The measured breakdown strength is shown in Figure 2-8 for a ~50nm thick oxide, which results in an 11 MV/cm breakdown strength. Therefore, PECVD SiO_2 film used as a buffer layer as a starting layer of TFT structure.

2.2.3. Sputtered silicon nitride (SiN_x) film

2.2.3.1. Background

Silicon nitride, SiN_x films are used primarily for two purposes. It is used for dielectric layers to electrically separate conducting gate metal and the semiconducting active layer and induce a field effect accumulation layer. The other main use of silicon nitride is as a final passivation layer on the device. Silicon nitride is a very good barrier against water and sodium diffusion, and it can be deposited uniformly, making it an excellent passivation layer for thin film transistors. Usually Plasma enhanced Chemical Vapor Deposition (PECVD) or Radio Frequency (RF) sputtering is used to deposit amorphous phase silicon nitride (a-SiN_x) for micro or nano fabrication. The general requirements for gate dielectric a-SiN_x are high breakdown strength, and high capacitance value. For inducing more in the active layer, high dielectric constant is favorable to the dielectric must have adequate breakdown strength to withstand the applied gate voltage. The dielectric constant of SiN_x film is known to be ~7.5 for stoichiometric

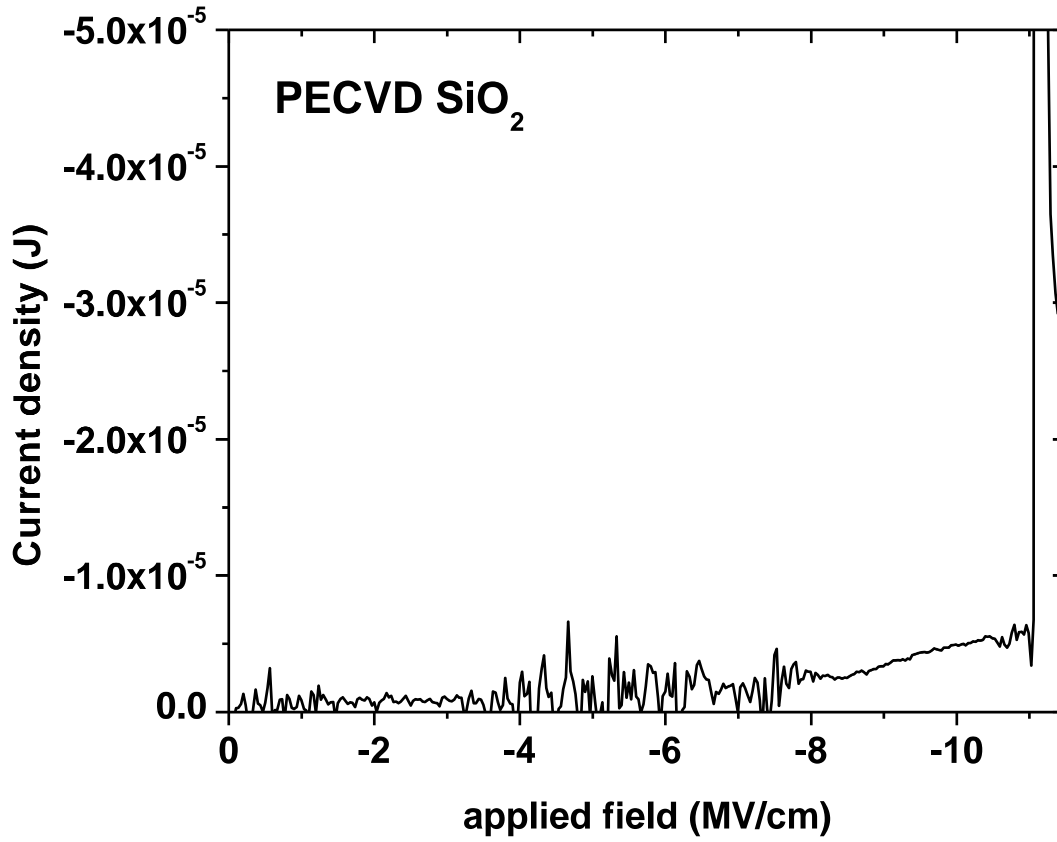


Figure 2-8. Breakdown strength of PECVD silicon dioxide film

composition (Si_3N_4) while SiO_2 film has dielectric constant of 3.7. Using sputter deposition, silicon nitride can be formed at low temperature to deposit on glass or polymer substrates.

The gate dielectric layer of a-Si TFT structures are typically hydrogenated a-SiNx (a-SiN_x:H) films since the excess hydrogen passivates dangling bonds at the interface between a-SiN_x and active a-Si layers [46]. Moreover, through diffusion, hydrogen contents migrate into the silicon layer and can passivate dangling bonds in a-Si active layer, which shows the better transfer characteristics by reducing channel resistivity [46]. However, excessive hydrogen content can act as a leakage current source, therefore, the properties of SiN_x:H have to be controlled for the specific purpose of the layer. Notably, sputtered SiN_x film has a relatively small amount of hydrogen content since only 5% H_2-Ar gas was used as one of the sputtering gases.

2.2.3.2. Experimental

An AJA, ATC 2000 sputter system was used to deposit silicon nitride films. Similar to the SiO_2 deposition, a reactive sputtering technique was used employing mixtures of N_2 and 5% hydrogen-Ar gases. To achieve stable silicon nitride film properties, covered mode was used to deposit SiN_x. The condition was that 200 watt RF power, 5mTorr pressure, and variable substrate power and temperature. Below 5.0 x 10^{-7} Torr base pressure was maintained prior to deposition. The flow rate of 5% hydrogen-Ar gas was fixed at 25 sccm and N_2 flow rate was fixed at 25 sccm and 50 sccm to discharge plasma at cover mode regime with a pure undoped silicon target (99.999%) of 2 inch diameter and 0.25 inch thick was used. The film thickness and refractive index value was measured using a reflectometer with a Deuterium Lamp (Filmetrics F20/40 Advanced Thin Film Measurement System). In order to measure the current-voltage relationship

to get breakdown strength and capacitance-voltage relationship, metal-insulator-silicon (MIS) structures were fabricated. Silicon nitride films were deposited on single crystalline silicon wafer (n-type: phosphor doped). After depositing SiN_x film, 130nm Cr film was deposited onto the sample and patterned to leave a metal contact pad using the standard photolithography process. The Cr deposition and etching process was previously described. The capacitance was evaluated with a Keithely 590 C-V analyzer and the dielectric breakdown strength was evaluated with a Keithely 2400 source-meter on Signatone Checkmate probe station system.

2.2.3.3. Results and discussion

Refractive index (n) property of SiN_x films is a good indicator of the atomic composition of silicon, silicon nitride (or nitrogen content), and hydrogen content in the deposited film. Thus the index of refraction was monitored as a function of the sputter deposition parameters. Because the hydrogen content in the gas was relatively small (<2.5%), the refractive index value mainly revealed the ratio of Si and SiN_x content in the films. Kuo reported that the nitrogen rich silicon nitride (N-rich SiN_x) film shows the better transfer characteristics when it is used as gate dielectric layer of TFT [46]. Additionally, the compressive stress in the nitrogen rich SiN_x film also enhances the transfer characteristic [46] by reducing the interface defect density, the leakage current at the interface.

Figure 2-9 shows the refractive index value of sputtered silicon nitride film as a function of substrate power and deposition temperature. At room temperature, as the substrate power increase, the refractive index tends to decrease since the nitrogen is sputtered densely and the plasma at the substrate helps incorporate more nitrogen and hydrogen into the SiN_x film. As will be demonstrated layer, but briefly noted here, the reduced refractive at room temperature is

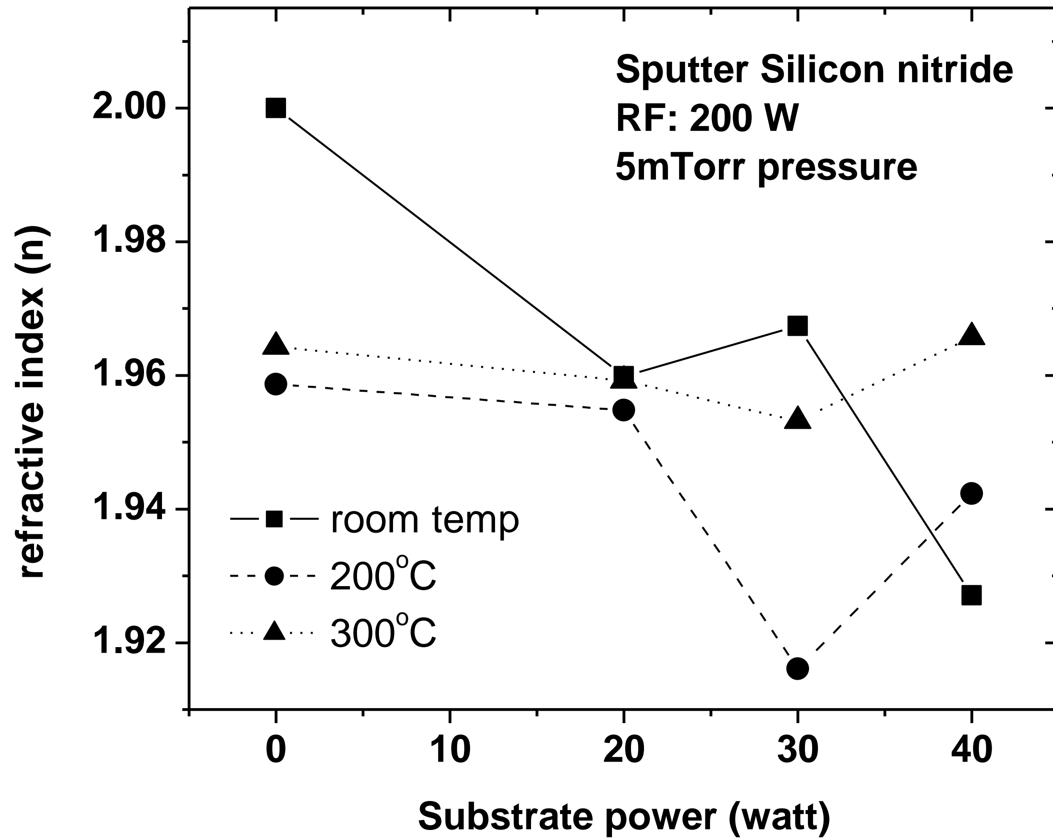


Figure 2-9. The refractive index changes of sputtered deposited silicon nitride film as a function of substrate power during deposition

mainly due to increased hydrogen content, not increasing nitrogen content. At high temperature such as 200 and 300°C, the refractive index value was initially decreased and then increased again. As the substrate bias increased, the index of refraction decrease indicating more nitrogen incorporation, however, above ~30 W, the index value increases again. This is likely due to preferential re-sputtering of nitrogen atoms which has the effect of increasing the silicon content in the films. Based on figure 2-9, the optimized film properties were obtained from 30 watt substrate bias and 200°C temperature with the deposition rate of 1.15nm/min. Additionally,150nm thickness SiN_x film has a - 1.81GPa stress (- indicated a negative or compressive stress).

Figure 2-10 shows breakdown strength of sputter SiN_x, SiO_2, and dual layer (SiN_x/SiO_2 stack) as a function of applied field. Since they are deposited in sputter system, lower breakdown strength was shown than PECVD films, which are discussed later.

2.2.4. PECVD silicon nitride (SiN_x) film

2.2.4.1. Background

Stoichiometric of SiN_x film can be controlled easily in PECVD growth. PECVD deposited silicon nitride has an amorphous structure, and its properties depend on the atomic concentration of silicon, nitrogen, and hydrogen. The atomic concentrations can be controlled by changing deposition conditions such as RF power, pressure, gas flows, and gas ratio. As mentioned previously, good TFT characteristics for a-Si active layers are achieved with SiN_x gate dielectric films containing a large amount of hydrogen (up to 20% H_2). To characterize PECVD SiN_x films properties the Si/N ratio, the refractive index, the N-H/Si-H ratio, the stress,

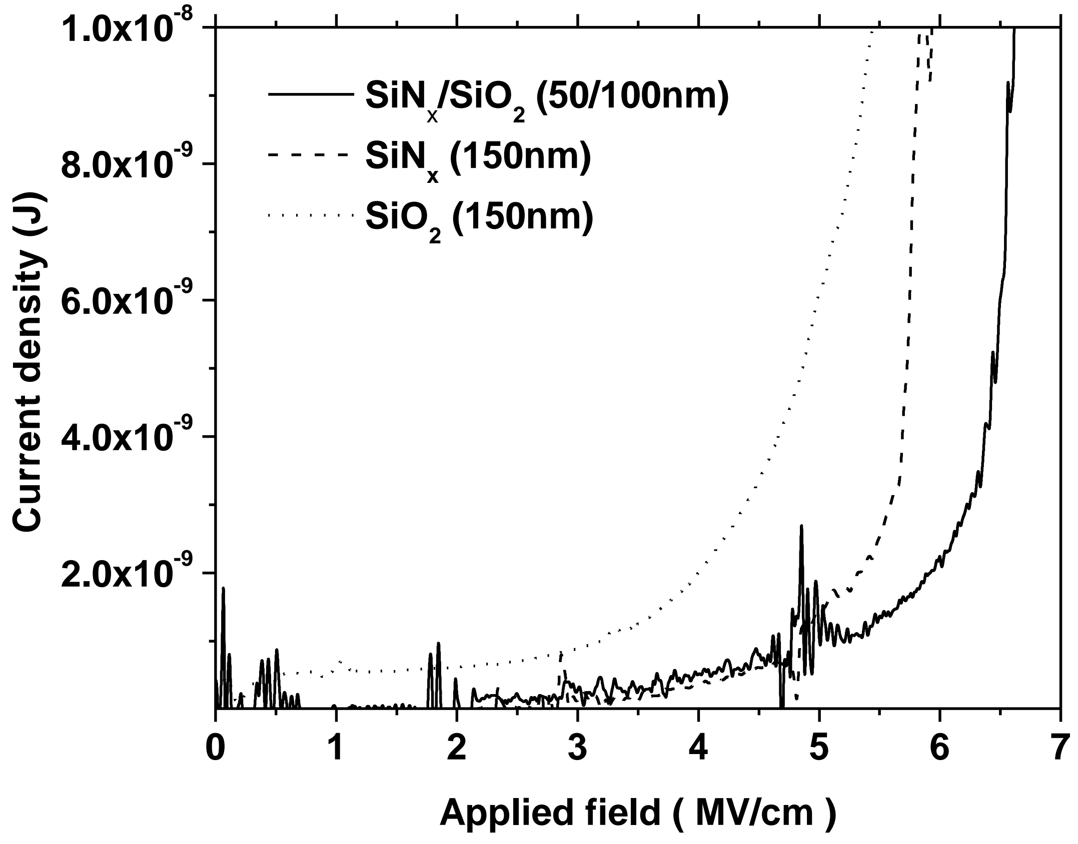


Figure 2-10. Breakdown strength of sputter SiN_x, SiO_2, and dual layer (SiN_x/SiO_2 stack) as a function of applied field

and the hydrogen content, have been studied [56-58]. The N/Si ratio has a key role to determine its properties. In SiN_x, as x increases, the threshold voltage decreases as the material approaches stoichiometric SiN_x from a silicon rich nitride film. The threshold voltage is related to the band bending near the interface between the a-Si:H active layer and the SiN_x gate dielectric since it depends on the defect level in the bulk and at the interface. Generally, when x decreases, more tensile stresses is generated, which results a localized micro voids at the interface. Therefore they have higher interface defect density to trap the electrons. From the refractive index (n) measurement, when n decreases, it indicates a nitrogen or hydrogen rich- SiN_x film typically with a low density of films; meanwhile high n is related to the Si-rich SiN_x films. The density of the SiN_x film is also related to the etch rate. Usually dense SiN_x films have a lower etching rate during reactive ion etching (RIE) or wet etching using HF solution. Table 2-1 shows the summary of SiN_x properties depending on composition of the film.

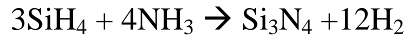
Since PECVD of SiN_x is usually using SiH_4, NH_3, and N_2 gas mixtures, silicon nitride films can contain up to 35% at% of hydrogen, bonded as Si-H and N-H. Though its presence weakens the structural integrity of the cross-linked silicon nitride network, the effect of hydrogen is desirable for TFT to passivate the dangling bonds at the interface between a-SiN_x/a-Si:H. As more hydrogen is incorporated into the a- SiN_x:H films, the refractive index(n) is reduced since there are more favorable Si-H and N-H molecules rather than Si-N bonds, which reduces film density and increases the etch rate. The hydrogen content in the film is also controlled by deposition temperature as well as the feed gas ratio and deposition power. Relatively low deposition temperature allows hydrogen to incorporate in the a- SiN_x network, whereas the hydrogen content is lower at high deposition temperature, because of the lower sticking coefficient at higher temperature.

Table 2-1. Summary of silicon nitride film properties

	Si rich SiN_x	N or H rich SiN_x
composition x (SiNx)	Low x	High x
refractive index (n)	High n	Low n
film density	dense	less dense
stress	toward tensile	toward compressive
etch rate	slow	fast

2.2.4.2. Experimental

Silicon nitride (SiN_x) was deposited by PECVD using SiH_4 and NH_3 gas sources. The deposition reaction is:



$$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$$

The deposition condition of PECVD SiN_x film were 20 Watts RF power, 1200 mTorr pressure, 5%SiH_4-Ar/NH_3 (30/200 sccm) gas flow, and 300°C temperature. The deposition rate was 0.48nm/sec, and the nominal refractive index value was 2.0. 200nm thickness of SiN_x films was prepared.

Dual gate dielectric layers were also prepared to use for poly crystalline silicon based TFTs. Since the interface between the active layer and gate dielectric layer is critical, further optimization was explored. Dual gate dielectric layers were fabricated by 150nm of SiN_x and 50nm SiO_2. All dielectric films were deposited on P-type prime grade silicon wafers. After deposition, Cr layers were deposited on top of the dielectric layers and metal electrode pads were

patterned to measure the I-V and C-V characteristics by using the standard photolithography process. The C-V measurement condition is that voltage range is between -20 and 20 volts, 1MHz frequency, step bias of 0.5 volts, and step time of 0.001 seconds.

2.2.4.3. Results and discussion

Figure 2-11 shows the current densities versus applied field of SiO_2, SiN_x, and dual gate dielectric thin films. From Figure 2-11, SiO_2 showed the highest breakdown strength, and SiN_x showed the weak breakdown. Insulator characteristics of the dual layer had a medium range between SiO_2 and SiN_x. For acting as gate dielectric layer, good capacitance characteristics are required. Figure 2-12 shows the C-V results from the same patterns of (a) SiO_2, (b) SiN_x, and (c) dual gate dielectric layer. From Figure 2-12 SiO_2 shows a large flat band voltage shift and SiN_x has a smaller flat band voltage shift, but the threshold voltage of the SiN_x was higher than SiO_2. As expected, dual layer has an optimized characteristic value of these two kinds of dielectric layer.

Herein, stress issues also should be considered. The measured thin film stress from these thin films shows a relatively high stress. SiO_2 had 180MPa of compressive stress at 200nm, and SiN_x had 300MPa of tensile stress at 200nm. However, only SiN_x film was considered as the candidate for gate dielectric films of amorphous silicon TFTs since the interface between SiO_2 and amorphous silicon layer has a high leakage current due to charge trapping at the interface. To minimize the stress in the gate dielectric layers, further investigating PECVD SiN_x layers were done. When the ratio of SiH_4/NH_3 is changed, intrinsic stress in the film can be varied [59]. To minimize intrinsic stress of SiN_x film, the NH_3 and N_2 gas flow rate was varied, the temperature was increased, and the process pressure was decreased. D. Briggs in the Center for

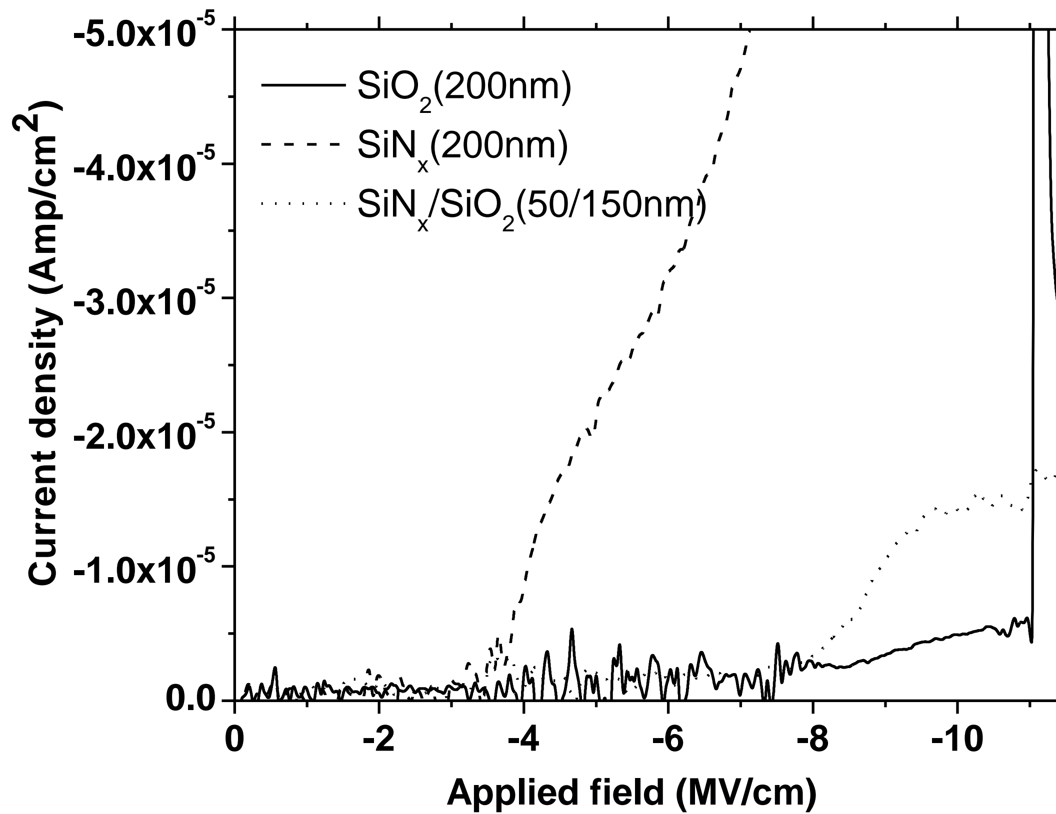
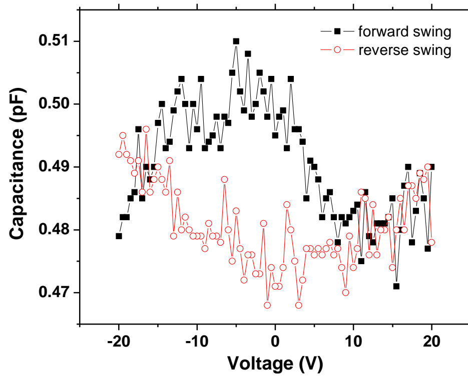
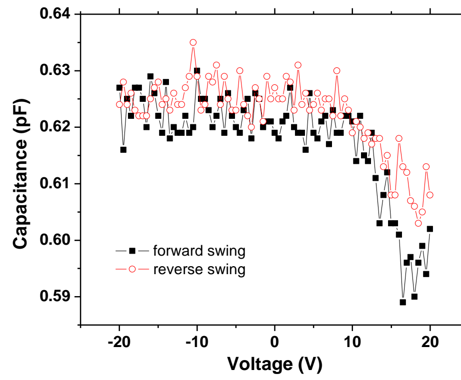


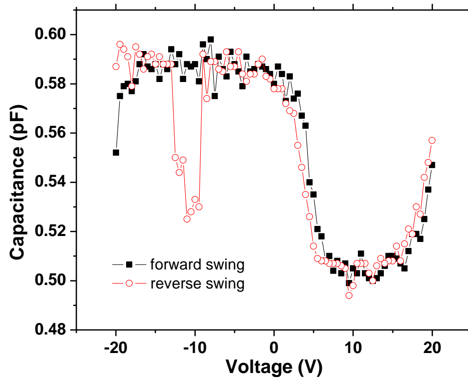
Figure 2-11. Current densities versus applied field of SiO_2, SiN_x, and dual gate dielectric thin films.



(a)



(b)



(c)

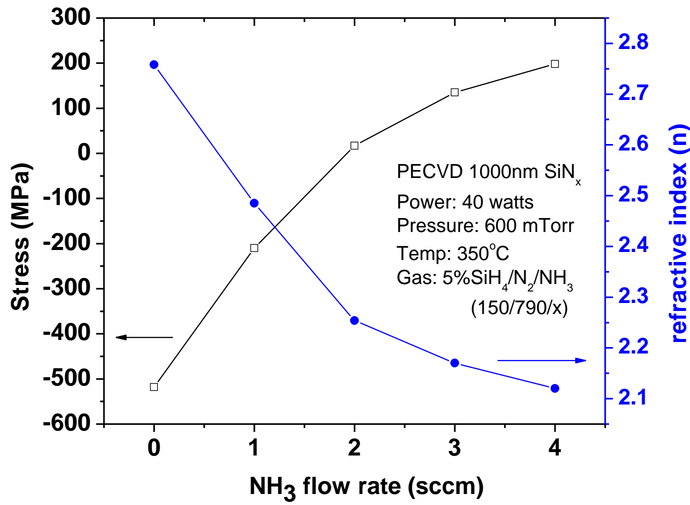
Figure 2-12 (a) Capacitance results of SiO_2 as a function of swing voltages, (b) capacitance results of SiN_x as a function of swing voltages, and (c) capacitance results of dual layers as a function of swing voltages

Nanophase Materials and Science, Oak ridge national laboratory performed the growth and measurements of these SiN_x films. Figure 2-13 (a) shows how the SiN_x film stress was changed from compressive to tensile with an increase in the NH_3 flow rate. Furthermore, the refractive index vale decreased with NH_3 flow rate indicating an increase in the amount of N-H bonds, which are directly proportional to developed tensile stress [60]. To characterize the stress properties of PECVD SiN_x films, the stress was measured for various SiN_x thicknesses (Figure 2-13 (b)).

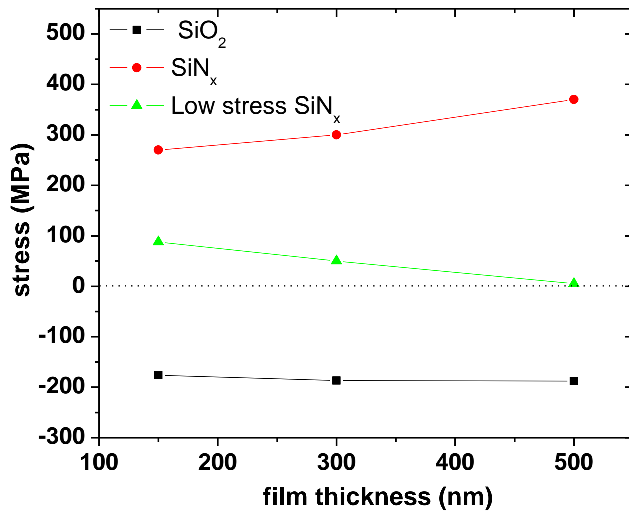
C-V characteristics were also measured by following the same procedure described above. Figure 2-14 shows the C-V for (a) as-deposited low stress SiN_x, and (b) after a 400°C anneal for 30min. The 400°C temperature and 30min anneal was investigated as this mimics the temperature cycle during the passivation layer of SiN_x deposition. From Figure 2-14, as-deposited SiN_x films show a higher value of flat band voltage shift. However, after annealing process, the flat band voltage shift is reduced to nearly zero and has a very low threshold voltage. Therefore, 400°C deposition temperature of low stress SiN_x layer was used to gate dielectric layer.

2.3. Semiconductor materials

Amorphous silicon film has been used as a semiconducting layer in thin film transistor and solar cells. Amorphous phase silicon has a disordered structure. Even though it is not a crystalline structure, it retains the same short-range chemical bonding as in crystalline silicon. Even though amorphous silicon atoms have 4-fold coordinated in a tetrahedral bonding symmetry, bonding lengths and bond angles are different, which depends on the amount of hydrogen. The electric properties of a-Si:H is depended on the bonding disorder since electrons

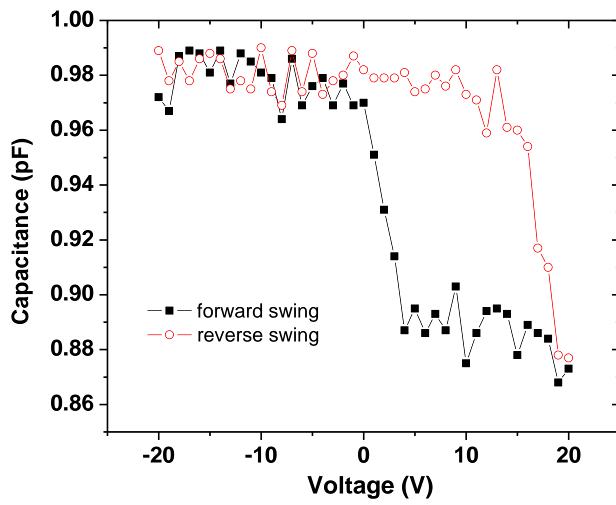


(a)

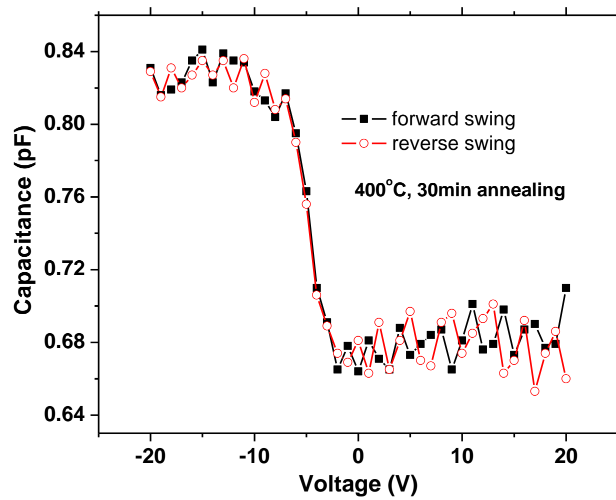


(b)

Figure 2-13. (a) Film stress and refractive index changes as a function of NH_3 flow rate The deposition condition for low stress SiN_x were 40 Watts RF power, 600mTorr pressure, 5%SiH_4-Ar/NH_3/N_2 (150/2/790 sccm) gas flow rate, and 400°C temperature, and (b) Residual stress versus thickness of PECVD SiO_2, SiN_x, and low stress SiN_x thin films.



(a)



(b)

Figure 2-14. C-V characteristics of Low stress SiN_x layer (a) as-deposited, and (b) annealed at 400°C during 30min.

and holes transport are related with the atomic structure. Generally, crystalline silicon has up to 500 cm^2/Vs field effect mobility whereas amorphous silicon has up to 1cm^2/Vs. However, amorphous silicon is not completely disordered. The covalent bonds between silicon atoms are much the same as in crystalline silicon, with the same number of neighbors and the same average bond length and bond angles. The amorphous silicon has the same short range order as the crystalline phase but lacks the long range order. Crystalline silicon contains defects such as vacancies, interstitials, and dislocations, but the definition of a defect of amorphous silicon has to be modified. Since amorphous silicon has a random network, the elementary defect of amorphous silicon is the coordination defect, when an atom has too many or too few neighbors. Significantly, the disorder causes an exponential tail of localized states at the band edges which extend into the energy band gap. The energy dividing the extended and localized states is known as the mobility edge. Conduction of both electrons and holes occurs near the mobility edges, but involves frequently trapping and release from localized states. Furthermore, the effective carrier mobility is reduced by the defect states, which exist in the middle of energy band gap.

Due to the nature of amorphous silicon, a-Si has a dangling bond defects which form defect states. These defect states control the trapping and recombination of carriers, and hence determine the carrier lifetimes and photoconductivity. Therefore, hydrogen is essential for the good electronic properties of a-Si to passivate the dangling bonds to reduce the dangling bond defect density. However, hydrogen incorporation has some deleterious effects. Light can induce higher leakage current under illumination. Hydrogen is more weakly bonded and can diffuse within the silicon network and across the surface. The hydrogen can partially penetrate into the silicon. The stable bonding configurations are the Si-H bonds and unstrained Si-Si bonds. The ability of hydrogen to diffuse in and out of the a-Si:H network has both beneficial and

undesirable effects. The fast diffusivity enables hydrogen passivation at low temperature, however, dehydrogenation is responsible for the instability of a-Si:H at elevated temperature. Hydrogen is completely removed from a-Si:H above about $450^{o}C$, which can degrade the device properties. Diffusion occurs when there is a gradient of the chemical potential. In a uniform material, the chemical potential depends on the concentration, C, resulting in Fick's law.

$$\frac{dC}{dt} = D\frac{d^2C}{dx^2}$$

Where the diffusion coefficient of hydrogen, D, which is thermally activated,

$$D = D_o \exp(-\frac{E_D}{kT})$$

Where the energy E_D is about 1.5eV, and the prefactor D_o is about 10^{-2} cm^2 s^{-1}.

Almost all the hydrogen is bonded to silicon atoms which do not diffuse significantly at lower temperature, so that hydrogen diffusion occurs by breaking a Si-H bond and reforming a bond at a new lattice site. The bonding sites are other silicon dangling bonds and the mobile hydrogen moves in an interstitial site. To release hydrogen from the Si-H bond into an interstitial site, 1.5eV diffusion activation energy is needed, which is smaller than the 2.5~3eV energy of the Si-H bond, $E_{Si\text{-}H}$. The diffusion energy is lower because interstitial hydrogen has a binding energy to the silicon, E_H. Therefore, E_{HD}, the energy to release hydrogen from the Si-H bond, can be written as

$$E_{HD} = E_{Si-H} - E_H$$

Note that the interstitial binding energy of crystalline silicon is about 1~1.5eV.

To summarize, two main effects of hydrogen in the a-Si film are passivation and micro-void formation. The passivation of dangling bonds is the primary beneficial effect of the hydrogen in a-Si:H. However, hydrogen also causes a reconstruction of the silicon network, breaking, and removing weak Si-Si bonds during growth. At elevated temperature, dehydrogenation can occur due to lower activation energy of hydrogen diffusion than the Si-H bond energy, which results the degrading of electrical properties of a-Si:H film.

Poly-crystalline silicon (poly-Si) is also used as active layer of thin film transistor (TFT) due to its high field effect mobility. As grain size increases, the field effect mobility increases because grain boundary scattering is decreased. However, poly-Si TFT have an anomalous leakage current level in the "off" state because the grain boundaries act as trapping sites for electrons and electron scattering sites in the channel region [61]. Overall, poly silicon devices are very attractive because of its higher mobility.

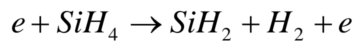
To make good contact between metal electrode and semiconductor materials, a low interface density of states and good ohmic contact properties are required. Low interface density of state is achieved by modifying the morphology of the contacting surface of silicon film. For the case of the source and drain electrode contacts with the semiconductor, breaking vacuum is inevitable. To reduce the contact interface, a plasma treatment (Ar and/or H) technique can be used. Additionally, the electrical characteristics are optimized by doping a proper dopant concentration in a silicon contact layer. Note that for thin film transistor work, n-type dopants are used since electrons act as the major carrier in the channel region, as it operates under the accumulation regime. By changing the Fermi energy level in the semiconductor relative to the intrinsic Fermi energy level, an ohmic contact is easily achieved, which induces the lowering potential barriers for carrier electron. Herein, n-type dopant (phosphorous: P) was used as

dopant for the ohmic contact layer. n-type doped amorphous silicon is noted as n^+ a-Si and n-type doped poly crystalline silicon is noted as n^+ poly-Si.

2.3.1. PECVD hydrogenated amorphous silicon (a-Si:H) film

2.3.1.1. Background

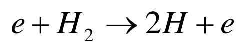
Plasma Enhanced Chemical Vapor Deposition (PECVD) is commonly used to deposit hydrogenated amorphous silicon (a-Si:H) film and SiH_4 gas is typically used as a precursor gas. The simple plasma chemistry reactions involved in the a-Si PECVD process are summarized below:



$$e + SiH_4 \rightarrow SiH_2 + H_2 + e$$

$$e + SiH_4 \rightarrow SiH_2 + 2H + e$$

$$e + SiH_4 \rightarrow SiH_3 + H + e$$

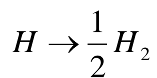


$$e + H_2 \rightarrow 2H + e$$

$$SiH_2 \rightarrow Si_{surface} + H_2$$

$$SiH_3 \rightarrow Si_{surface} + \frac{3}{2}H_2$$

$$4H + Si_{surface} \rightarrow SiH_4$$



$$H \rightarrow \frac{1}{2}H_2$$

2.3.1.2. Experimental

An Oxford Plasmalab PECVD system was used to deposit hydrogenated amorphous silicon (a-Si:H) with various Radio Frequency (RF) powers, working pressures, and flow rates of 5% SiH4+95% Ar while 350°C temperature was fixed.

2.3.1.3. Results and Discussions

a-Si:H deposited with RF power at 10, 15, and 20 watts and gas flow rate of 280 and 500 sccm of 5% SiH4+95% Ar mixture gas did not show the distinguishable difference in the amorphous silicon refractive index (~4.2). As expected, higher RF power resulted in higher deposition rate, however, the film uniformity was decreased. Specifically, the edge region of the 4" inch wafer had a porous silicon layer on the top surface. Next, pressure was considered as a variable to control the deposition rate. Figure 2-15 shows the deposition rate of PECVD deposited a-Si:H films as a function of pressure. Initially, as pressure increased, deposition rate was increased, however, at higher pressure the deposition rate decrease again. Typically, the limiting factor for PECVD deposition is either the diffusion (mass transport limiting) or adsorption (reaction rate limited) of decomposed species. The trend in the figure 2-15 is likely due to an initial increase in the silicon reactant which increases the deposition rate because diffusion is increased, however at higher pressure, the surface concentration likely saturates and the higher pressure effectively reduces the diffusion coefficient in the viscous flow regime.

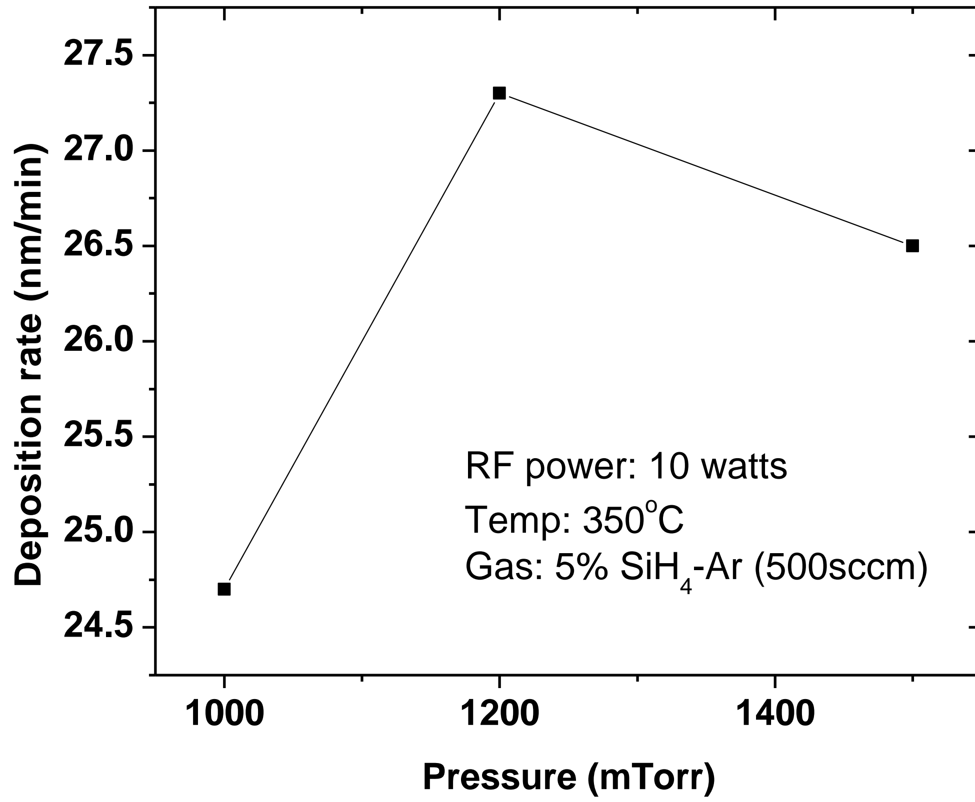


Figure 2-15. The deposition rate change as a function of working pressure in PECVD chamber for a-Si:H films.

2.3.2. Low pressure chemical vapor deposition (LPCVD) poly crystalline silicon (poly-Si) film

2.3.2.1. Background

Poly crystalline silicon can be achieved by using re-crystallization process such as solid phase crystallization (SPC), and excimer laser annealing or direct deposition of poly silicon using low pressure chemical vapor deposition (LPCVD). The field effect mobility of poly-Si is up to $500cm^2/Vs$, which is strongly dependent on the grain size. Even though, large grain size produces higher filed effect mobility, it also increases the leakage “off” state current of the device characteristics since the grain boundaries trap the migrating majority carriers (electrons).

2.3.2.2. Experimental

A Tystar LPCVD system was used to deposit poly-Si. 300 mTorr pressure and 75sccm flow rate of SiH_4 gas was fixed and two different deposition temperatures were used (615^oC and 625^oC). Generally, the crystallinity of silicon film is achieved above 600^oC deposition temperature when an LPCVD is used. However, too high of a deposition temperature may induce device failure due to silicide formation or induce thermal stress during cooling down. An initial experiment was performed to optimize the properties of poly-Si such as low resistivity of the film and higher crystalline fraction in the (111) orientation of the silicon film since the (111) orientation of the film results better conductivity relative to the (220) orientation. Crystallinity was measured with a Philip’s X’pert Pro X-ray diffraction (XRD), Filmetric UV-20 was used to measure the reflectance spectra, and a four-point probe machine was used to measure the resistivity of the films.

2.3.2.3. Results and discussions

As the temperature increased, the deposition rate was increased due to the increased dissociated SiH_4 gas molecules into Si precursor, which is directly deposited onto the substrate. At 615^oC, the deposition rate was 7.5nm/min, however, at 625^oC, ~13nm/min deposition rate was achieved. Figure 2-16 represents the reflectance spectra of the poly-crystalline silicon film deposited at 625^oC. To compare the crystallinity, the reflectance spectra data of a single crystalline silicon and sputter deposited amorphous silicon sample are represented. At 275nm and 375nm wavelength silicon shows the characteristics reflectance peaks. Thus, indirectly the degree of crystallinity of poly-Si can be compared by comparing the reflectance peak intensity. Figure 2-17 shows the X-ray diffraction data comparing the 615^oC and 625^oC deposited silicon. All data was normalized to distinguish the background and characteristic peaks. A strong (220) orientation silicon characteristics peak was detected for the 615^oC growth and there is a relatively small portion of (111) orientation characteristic peak and strong (220) orientation peak for the at 625^oC temperature sample. Generally, LPCVD deposited poly-crystalline silicon shows the stronger (220) orientation (2 theta= ~ 47.5^o) rather than (111) orientation at (2 theta= ~ 27.5^o) peak because the (220) orientation has shorter Si-Si bond length than the (111) orientation [62]. Figure 2-18 represents the XRD intensity results of post-annealed poly-Si, which was deposited at 625^oC. Post annealing condition was 800^oC, 30 min soak in N_2 furnace. The post-annealed sample showed a higher (111) orientation than (220) orientation. The formation of (111) orientated structure during annealing is directly related to relaxation of compressive stress. Grain boundaries in (220) orientated structure are the main source of compressive stress. Thus the stress is reduced when the small (220) grain grow and orient into a larger (111) grain. Therefore,

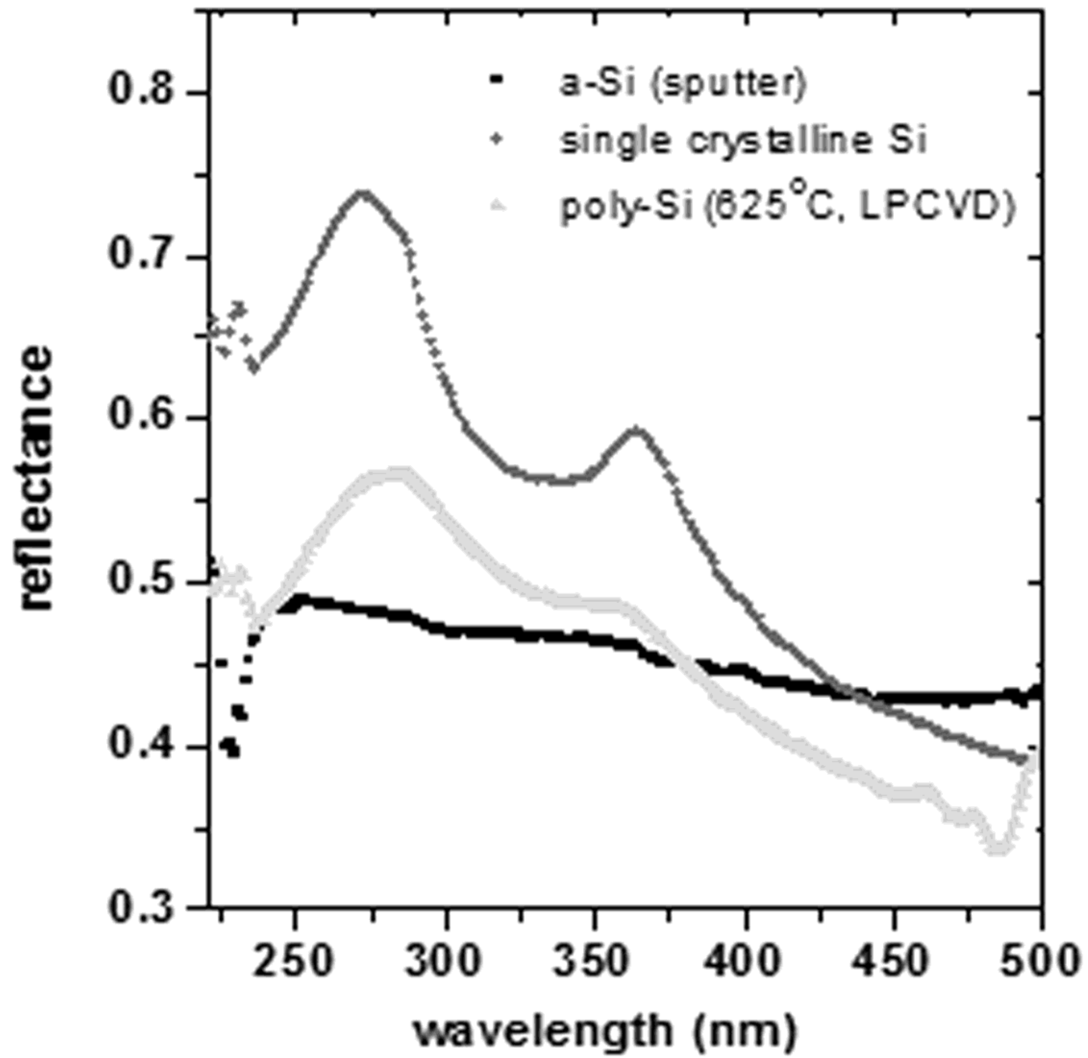


Figure 2-16. Reflectance of deposited LPCVD poly-Si at 625°C temperature to compare the crystalline reflectance data of sputter deposited amorphous silicon and single crystalline silicon wafer is presented

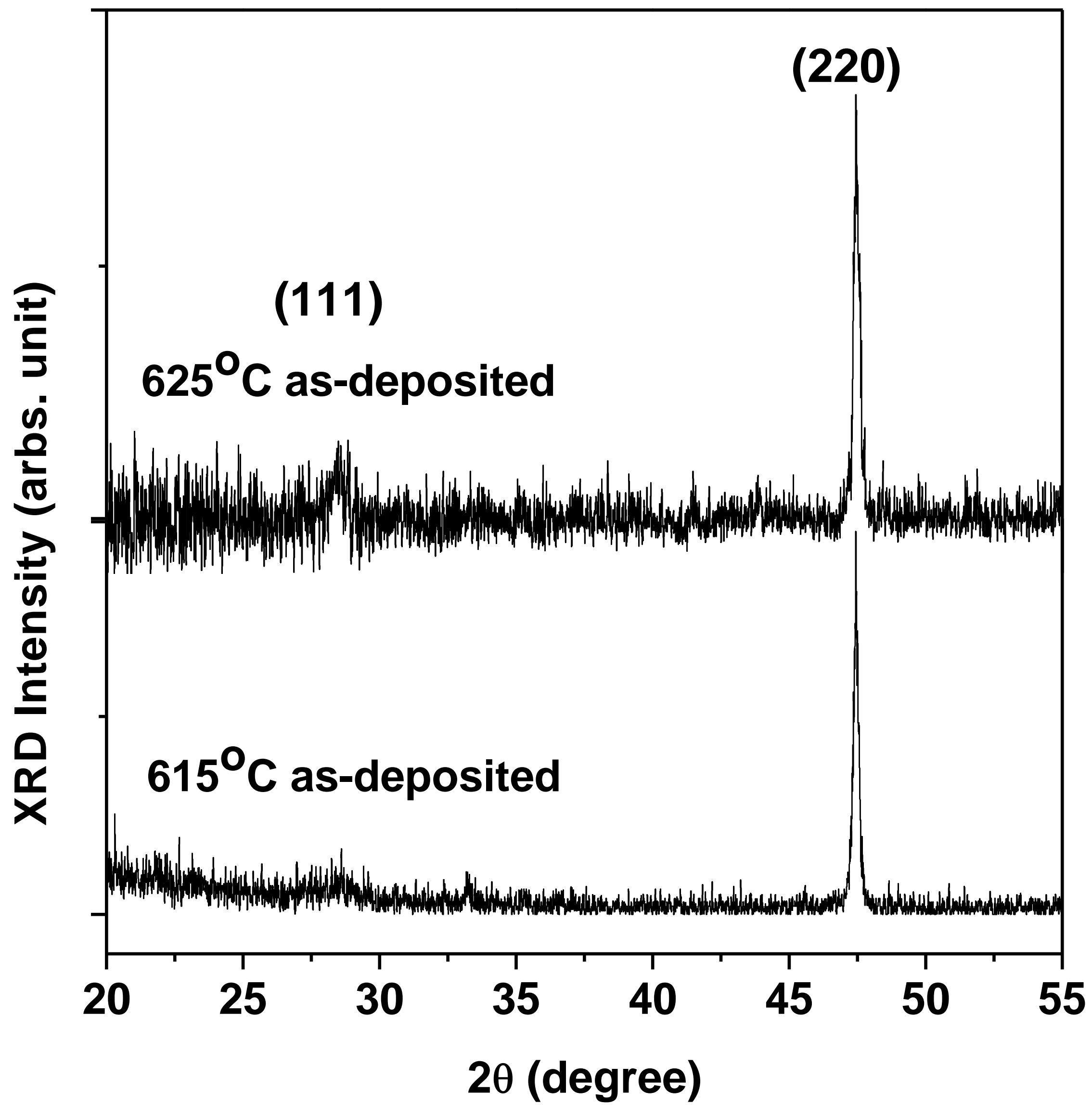


Figure 2-17. XRD intensity data of poly crystalline silicon deposited by LPCVD at 615°C and 625°C process temperature

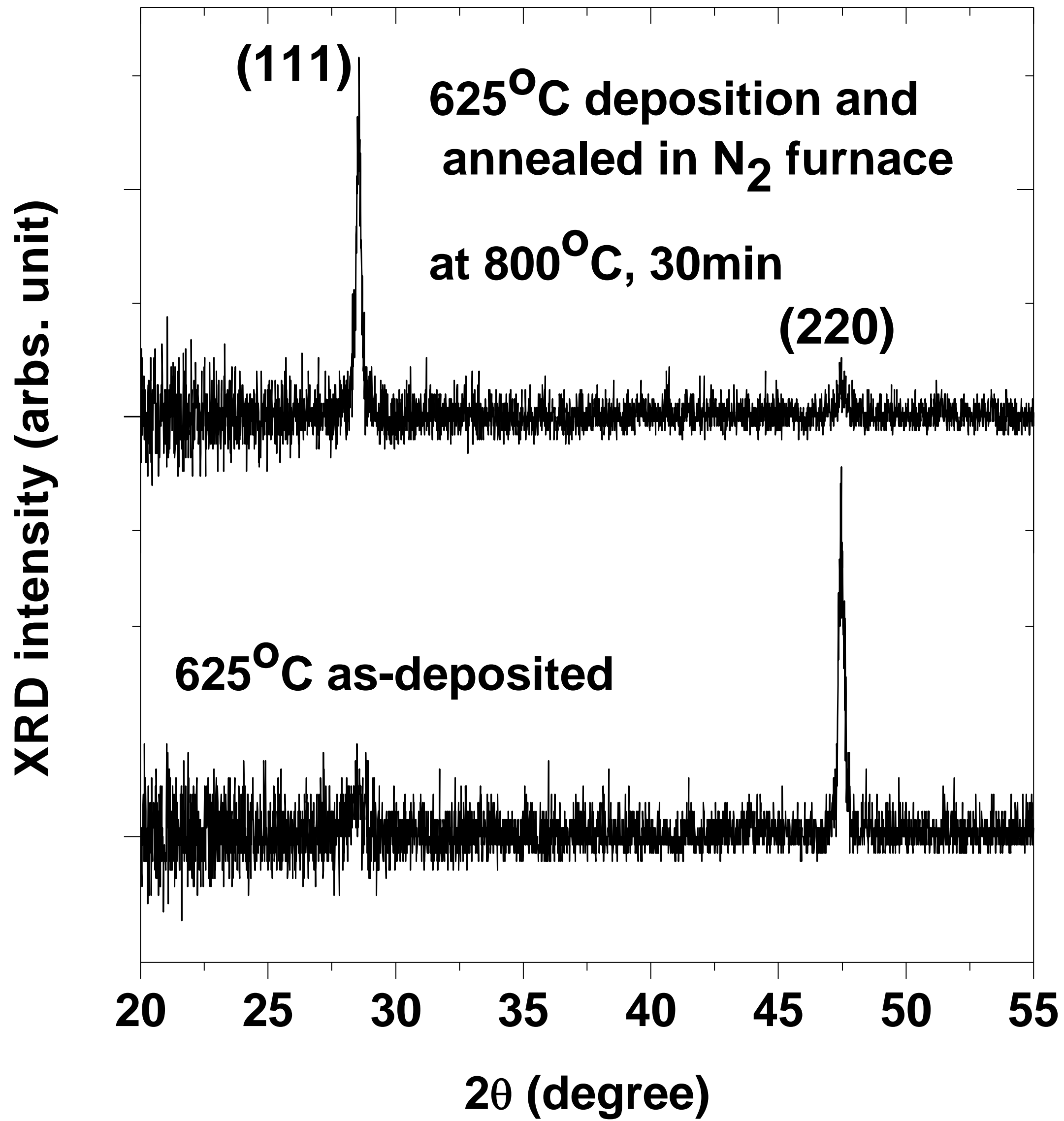


Figure 2-18. XRD intensity data of poly crystalline silicon deposited by LPCVD at 625°C process temperature; as deposited versus post-annealed at 800°C, 30min, in N_2 furnace

during the anneal, the orientation changed from (220) to (111), the compressive stress was reduced, and larger grain size was achieved, which favor a higher field effect mobility. To confirm, the change of grain size, Scanning electron microscopy (SEM) images were taken. Figure 2-19 shows the SEM images of as-deposited poly-Si and post-annealed (800°C) poly-Si initially grown in the LPCVD at 625°C. The two images show distinguishably different grain sizes.

2.3.3. LPCVD n-type doped poly crystalline silicon (n^+ poly-Si)

2.3.3.1. Background

Poly crystalline silicon can be doped either n type or p type, which can be achieved during deposition by adding dopant source gases. n-type silicon is achieved by adding source gases such as phosphine (PH_3) or arsine (AsH_3) and the phosphorus (P) or arsenic (As) substitute for silicon and produce donor states because of the extra electron in the valence shell relative silicon. The addition of these dopant gases typically decreases the deposition rate, by competing with silicon during the growth process. Additionally dopant species can segregate into the grain boundaries, which are electrically inactive. Dopants that incorporate into the lattice contribute to the doping of the poly-Si. When depositing doped poly silicon, the deposition rate and resistivity of the film should be considered. Since larger grain size results in smaller grain boundary area, this is preferred so as to reduce the contact resistance by reducing resistivity of the film.

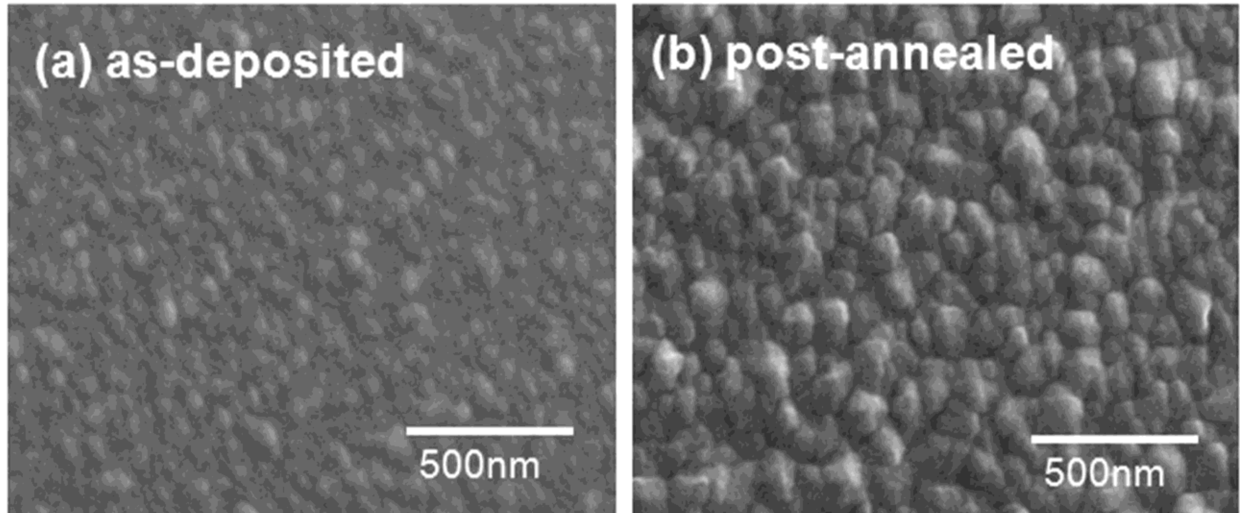


Figure 2-19. SEM images of (a) as-deposited poly-Si (625°C, LPCVD), and (b) post-annealed (800°C, 30min soak) poly-Si

2.3.3.2. Experimental

A Tystar LPCVD system was used to deposit doped poly crystalline silicon films. Various temperatures and gas ratios of SiH_4 and PH_3 were used while working pressure was fixed at 300 mTorr. To achieve the lower resistivity of films, post annealing processes were investigated in a vacuum furnace and N_2 furnace with various temperature and time. To evaluate the crystallinity and resistivity of the film, X-ray diffraction (Philips, X-pert x-ray diffractometer) and a four-point probe system were used, respectively.

2.3.3.3. Results and discussion

To evaluate the gas ratio of SiH_4 and PH_3, two set of experiments were done. SiH_4 gas and a SiH_4+PH_3 mixture gas were used. Gas ratio was calculated from the gas flow rate. For example, for ratio of SiH_4/PH_3=28/1, 77 sccm of SiH_4 and 23 sccm of SiH_4+PH_3 were used.

During 30 minutes deposition, the deposition rate of 28/1 ratio of poly-Si was 2.875 nm/min and 2.00 nm/min for a 15/1 ratio with a pressure and temperature fixed at 300 mTorr and 625°C, respectively. As the concentration of PH_3 increased, the deposition rate was reduced because of competition between Si and P. The deposition rate of doped poly-Si as a function of deposition temperature also examined. The deposition rate at 580°C was 1.77nm/min, while at 615°C, 2.125nm/min was achieved with a fixed gas ratio of SiH_4/PH_3 of 28 to 1. It is clear that as increasing deposition temperature, more active species were available to be deposited onto the substrate. Figure 2-20 represents the x-ray diffraction (XRD) spectra of poly crystalline silicon deposited by LPCVD with different gas ratio of SiH_4 and PH_3. Higher intensities are shown at 28/1 SiH_4/PH_3 ratio at ~28 degree for (111) silicon orientation and ~47.5 degree for (220) silicon orientation since the higher PH_3 concentration inhibits the proper incorporation of silicon species. The effects of deposition temperature are also presented at figure 2-21. At 580°C deposited silicon did not show distinguishable silicon characteristic peaks (amorphous), thus the 580°C XRD results are not included in figure 2-21. At 625°C the deposited silicon shows a higher intensity at (111) and (220) orientation. Compared to the undoped poly-Si at the same temperature and pressure, the doped poly silicon did not have the strong (220) preferred orientation. During deposition, the migration of phosphine in the silicon network decreases the compressive stress in-situ and cause the (220) to orient in the (111) orientation [62]. This also results the decrease of resistivity of the film. Thus, compensation of stress, deposition rate, and resistivity of the film characteristics were all desirable for the ohmic contact layer.

To achieve the better characteristics of poly-Si; low stress, large grain size, and higher crystallinity, post-annealing processes were characterized. At 1000°C temperature for 30 minutes annealing processes was done in a vacuum furnace with or without N_2 gas flow. Figure 2-22

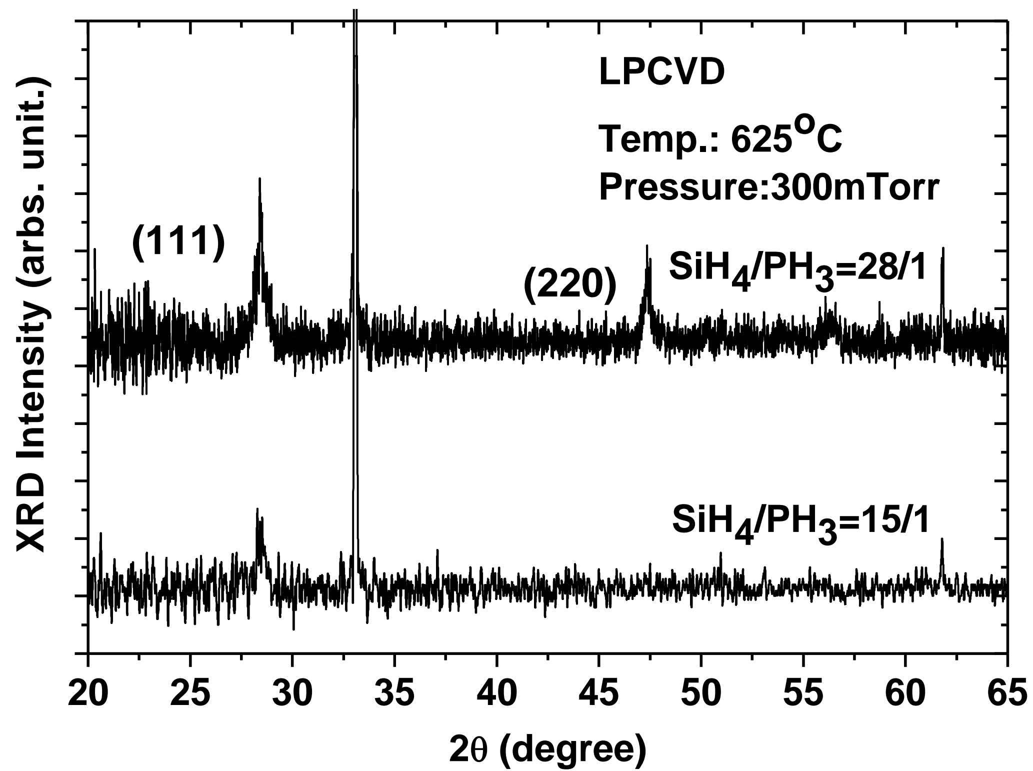


Figure 2-20. X-ray diffraction (XRD) spectra of poly-crystalline silicon deposited by LPCVD to compare the gas ratio effect of SiH_4 and PH_3; 28 to 1 and 15 to 1.

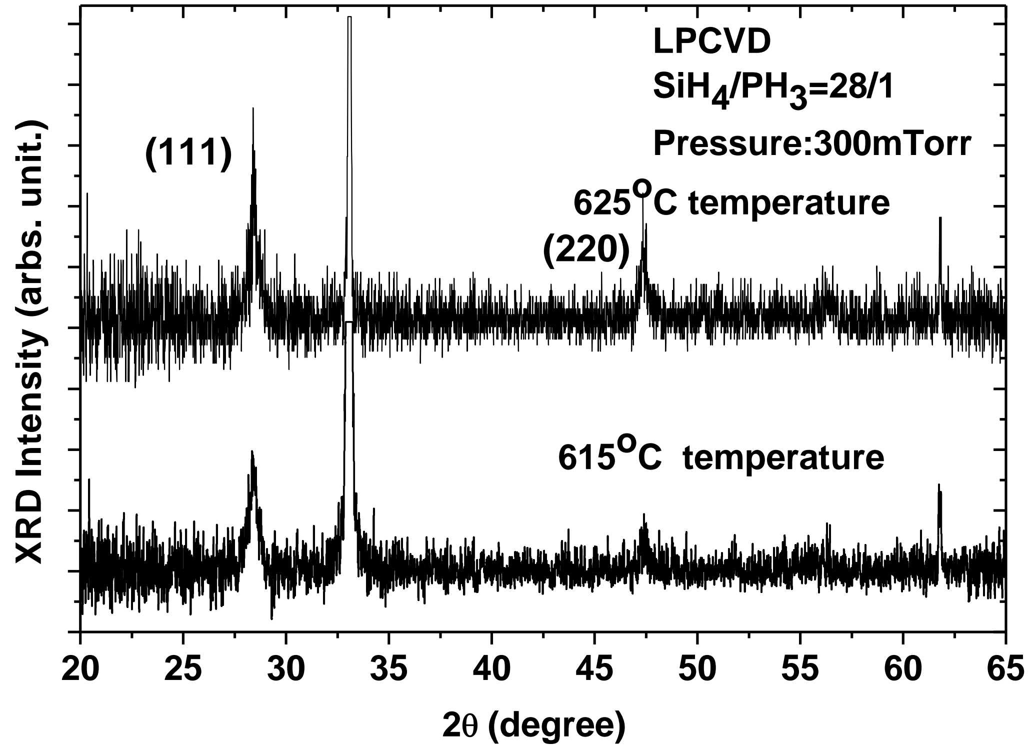


Figure 2-21. X-ray diffraction spectra of poly-crystalline silicon deposited by LPCVD demonstrating better crystallinity is achieved at 625oC temperature than 615oC. SiH_4/PH_3 gas ratio was fixed at 28 to 1 and pressure was 300mTorr.

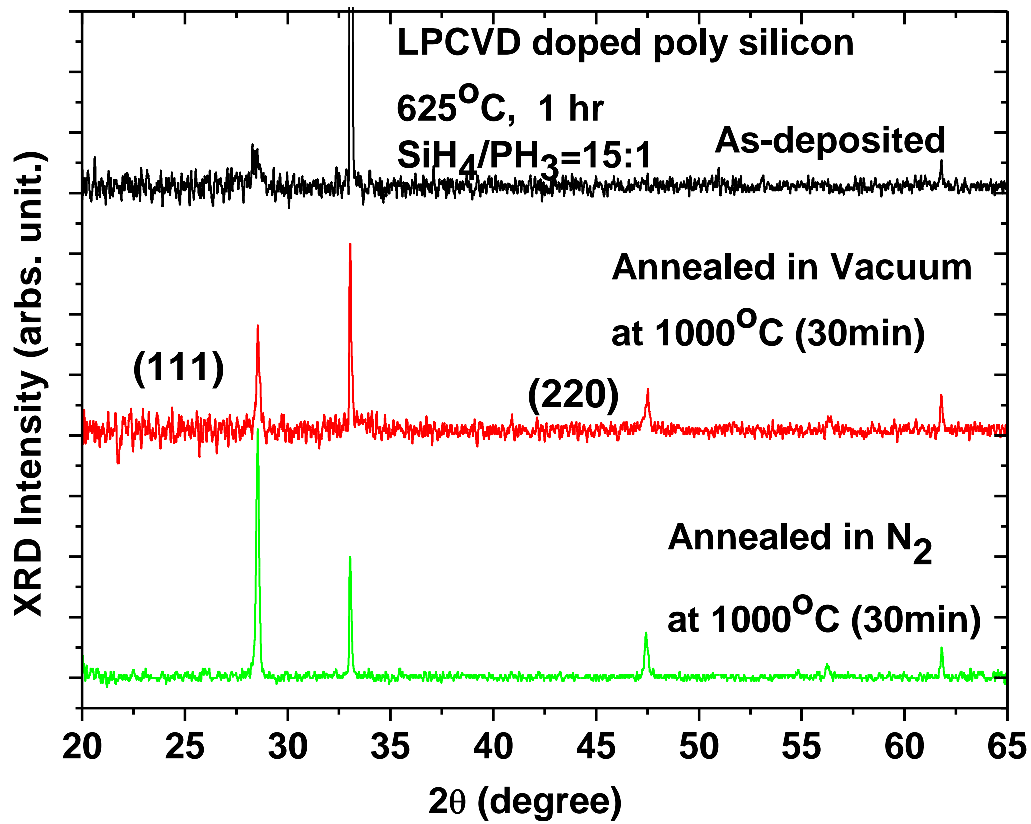


Figure 2-22. X-ray diffraction spectra of poly-crystalline silicon deposited by LPCVD illustrating the post-annealing effects; as-deposited poly-Si, annealed in vacuum ambient, and annealed in N_2 ambient. Post-annealing processes were done at 1000°C for 30min.

shows the XRD spectra of poly-Si as-deposited, annealed in vacuum furnace, and annealed in N_2 ambient. The films annealed in the N_2 furnace had the best preferred (111) orientation, which indicates the film stress was reduced and higher crystallinity was achieved. It is surmised that decreasing silicon oxidation in the furnace by flowing the nitrogen gas resulted in higher crystallinity relatively to the vacuum furnace anneal [63]

The resistivity of deposited poly-Si films were measured as a function of deposition temperature and post annealing temperature while annealing time was fixed at 60 minutes in N_2 furnace. To measure the resistivity, poly-Si was deposited onto thermally grown SiO_2 (1000nm)/Si wafer substrates. After calculating the deposition rate, all layers were deposited to a 50nm thickness. Figure 2-23 shows the resistivity results. Increasing the deposition temperature and post annealing temperature, the resistivity of the films decreased. Though the deposition temperature shows the slight relation to decreasing the resistivity, post annealing temperature strongly decreases the resistivity. The post-deposition anneal decreased the resistivity by two orders of relative to the as-deposited condition. It is obvious that at higher post annealing temperature, larger grains are formed with decreasing the resistivity due to reduced grain boundary scattering. Additionally, post annealing time was also examined. Figure 2-24 shows the resistivity of the film as a function of post annealing time. Increased annealing time, decreased the resistivity, however, the 580°C deposited sample (amorphous) is virtually constant and is suspected to have incorporated very little phosphine in the as-deposited sample.

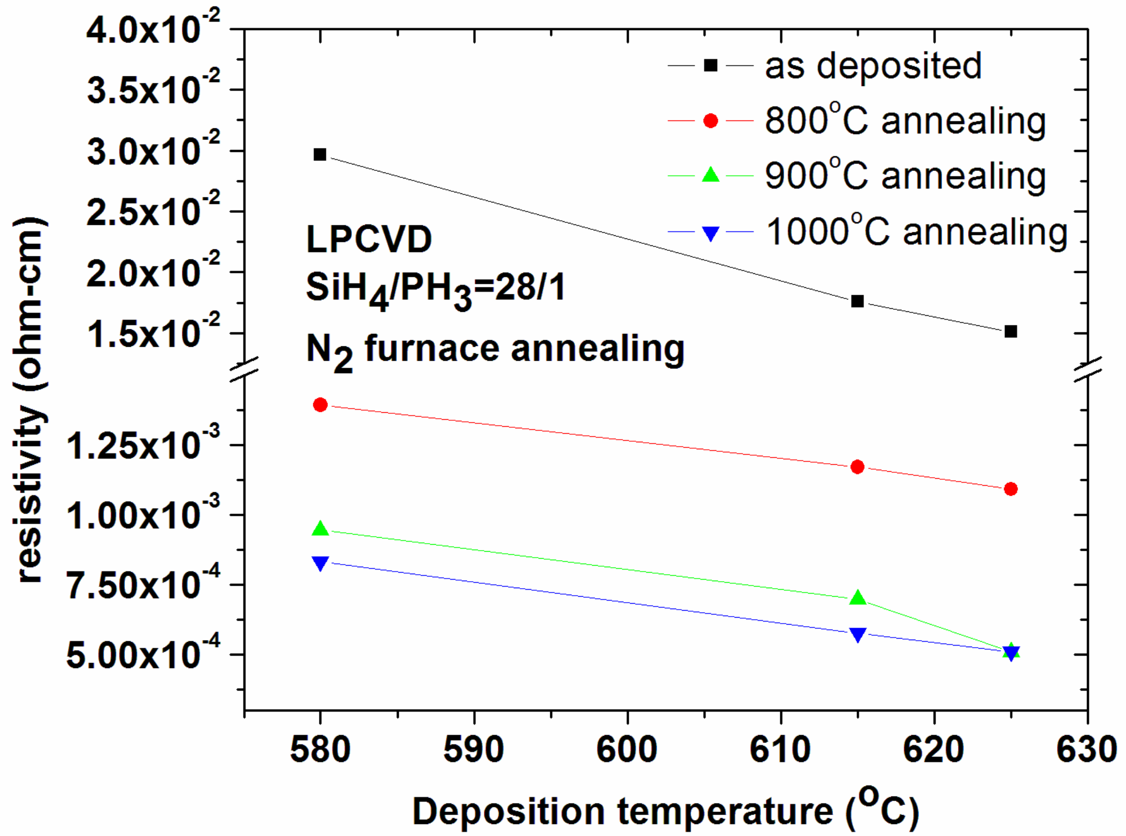


Figure 2-23. Resistivity of poly crystalline silicon film as a function of deposition temperature; post-annealed results also presented (various annealing temperatures for 60 min in N_2 furnace)

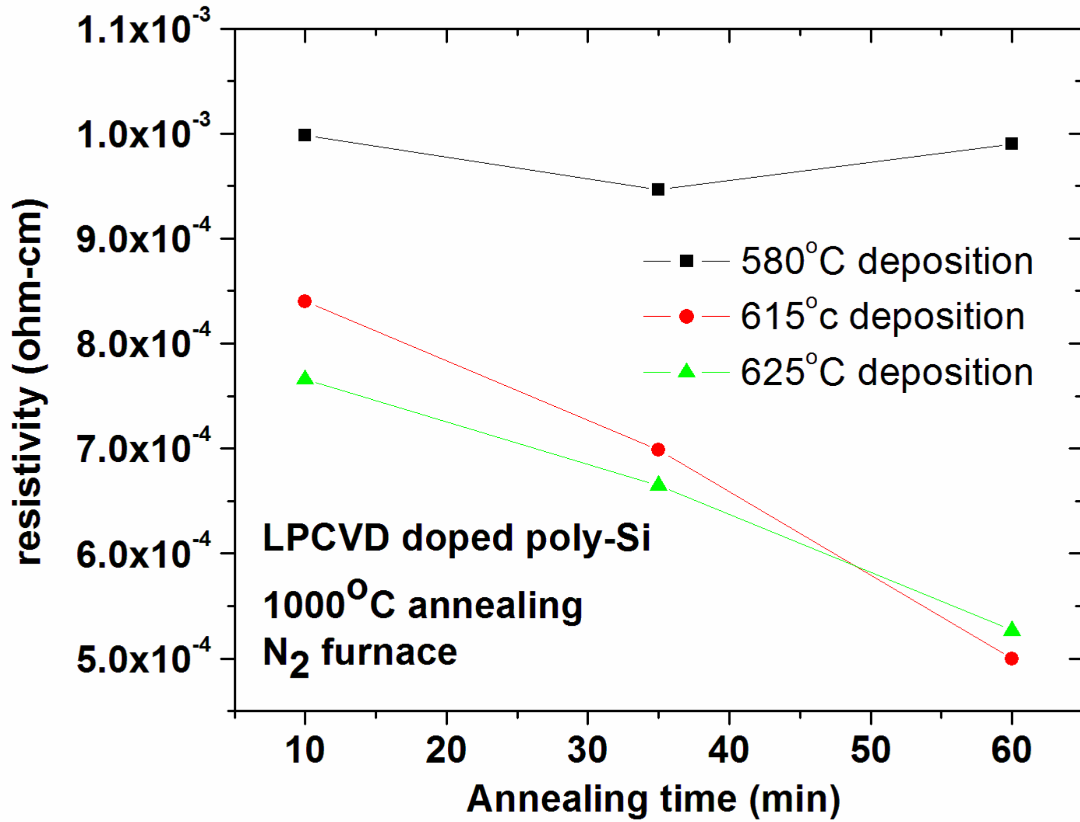


Figure 2-24. Resistivity of poly crystalline silicon film as a function of post annealing time at 1000°C in N_2 furnace; variable deposition temperature of 580°C, 615°C, and 625°C

2.3.4. Sputtered hydrogenated amorphous silicon (a-Si:H) film

2.3.4.1. Background

Sputter deposition is attractive for low temperature large area fabrication process, however, high trapping density is the main drawback of sputtered a-Si:H film. In spite of these defects, low temperature process is attractive for use on plastic substrate for flexible and transparent display applications. a-Si:H films have been deposited by both direct current (DC) and radio frequency (RF) power sputtering. RF sputtering is usually used to deposit a-Si:H film since the alternating voltage avoids charge build up on non-conducting targets, and results in good ionization efficiency density relative to DC sputtering. To hydrogenate the amorphous silicon, Ar-H_2 gas can be used as working gas. The most notable species in the Ar-H_2 plasma are H_3^+, ArH^+, and SiH_x ions relative to the pure Ar gas case.

2.3.4.2. Experimental

An AJA 2000 Radio Frequency (RF) magnetron sputter system was used to deposit hydrogenated amorphous silicon film using an Ar-5%H_2 sputtering gas. 2" diameter 0.25"thick solid intrinsic silicon target (Kurt J. Lesker) was sputtered at 5mTorr pressure, 200 watt RF power, and various temperatures, and substrate powers. The control of the substrate power can modify the morphology and density of a-Si:H, which can affect the crystallinity of the silicon film during a post-annealing process such solid phase crystallization (SPC). The target-to-substrate distance was fixed at 16.5cm.

2.3.4.3. Results and discussions

a-Si:H film was deposited with various substrate power while RF power of 200 watts, 5 mTorr pressure, 200°C temperature were fixed. Figure 2-25 shows the film residual stress and deposition rate of a-Si:H film as a function of substrate power. Increasing the substrate power, decreased the deposition rate of the film. As the potential at substrate increased, Ar ions in the plasma are accelerated towards the substrate which initially has the effect of increasing the film density. Concurrently, a compressive stress was developed in the film. With increasing substrate power to ~20 watts, the stress level was virtually constant. This is mainly due to a saturation in the film density.

To confirm the relation between the density of the film and developed film stress, refractive index value of a-Si:H film was determined and plotted in Figure 2-26. As demonstrated in figure 2-26, there is a correlation in the refractive index (n) value and the film density and compressive stress.

2.3.5. Stress induced crystallization (SIC) of sputtered a-Si:H film

2.3.5.1. Background

There is a growing interest in using polycrystalline silicon (poly-Si) as an active layer for thin film transistors instead of amorphous silicon (a-Si) because the charge carrier mobility of poly-Si is much higher than that of a-Si [64-65]. As a consequence, a variety of methods for lowering the crystallization temperature of a-Si have been developed. C. Spinella et al.

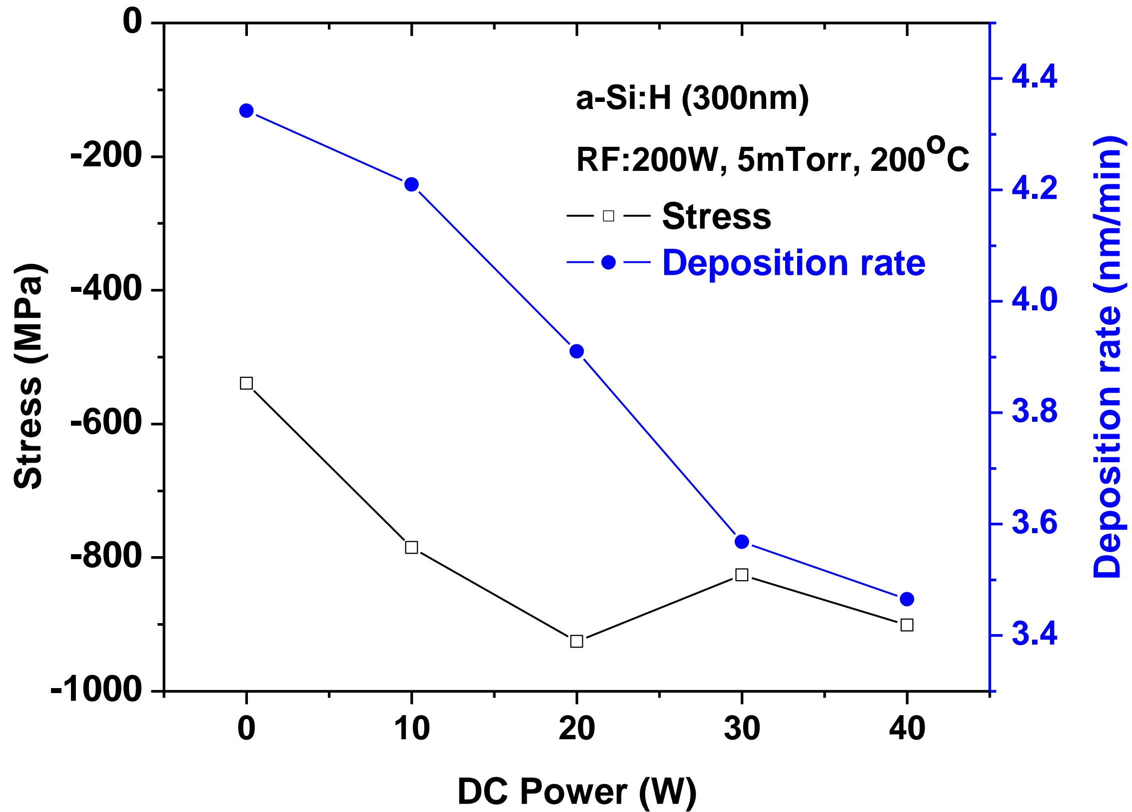


Figure 2-25. The residual stress and deposition rate of a-Si:H films as a function of substrate power during RF magnetron sputtering while RF power, pressure, and temperature were fixed at 200 watts, 5 mTorr, and 200°C

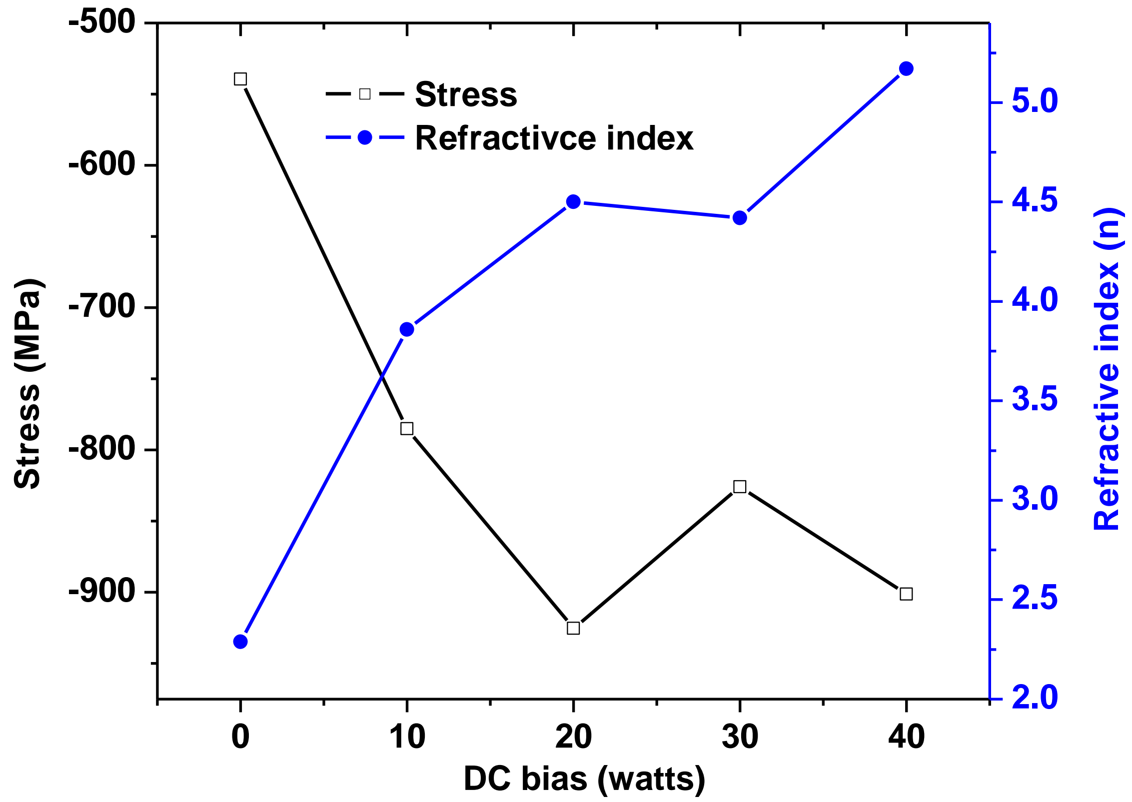


Figure 2-26. Residual stress and refractive index value of a-Si:H films as a function of substrate power during RF magnetron sputtering while RF power, pressure, and temperature were fixed at 200 watts, 5 mTorr, and 200°C

described a solid phase crystallization technique [66]. Excimer laser annealing is a promising way to get large grain size without high substrate temperatures. Its high costs and nonuniform grain size, however, are significant obstacles that prevent its wide use [67]. Metal induced crystallization has been used to obtain large grains at low temperatures with relatively low cost [68-70]. Because of the aluminum oxide capping layer demonstrated here, it is worth mentioning that recently [71-73] the mechanisms responsible for aluminum induced crystallization have been elucidated. It was shown that aluminum lowers crystallization temperature via a free electron screening process from the metallic aluminum which weakens the silicon covalent bonds. The coulomb screening process creates an interfacial layer of ~ 2 monolayers of free silicon which subsequently wets the grain boundaries of the aluminum layer. Finally, crystalline silicon nuclei precipitate from the free silicon atoms in the aluminum grain boundary and silicon interface region with a significantly lower activation energy. The main drawback of metal induced techniques is that metal residues remain after annealing which can degrade the electrical properties of the device. It is well established that crystallization of hydrogenated amorphous silicon (a-Si:H) film is strongly dependent on the hydrogen content, which is related to the residual stress in the film [74-76]. Hossain et al. also showed that the thermal energy provided during annealing is used to relieve the initial compressive stress in the film [77]. Recently, the effects of external mechanical stress on the crystallization of amorphous silicon have been reported by Hashemi et al. [78]. It was shown that tensile stress applied to silicon films during annealing enhanced the crystallization properties of silicon, while an applied compressive stress suppresses the crystallization process.

Although the mechanism of stress effects of a-Si:H film crystallization is not clearly understood, it is suggested that induced biaxial stress facilitates the crystallization process [79-

80]. Kimura et al. reported that silicon nitride (SiN_x) dielectric caps can impose a tensile stress on the underlying silicon layer during a post deposition anneal; they suggested that thermal stress is induced by the difference in the thermal coefficients of expansion (TCE) between a-Si (TCE = 2.3 x 10^{-6} °C^{-1}), and silicon nitride (TCE = 3.3 x 10^{-6} °C^{-1}) [80]. The induced stress enhances the crystallization process during annealing and results in higher crystallinity and larger grain sizes. In this paper, we explore the effects that SiN_x and Al_2O_3 (TCE = 8.4 x 10^{-6} °C^{-1}) capping layers have on the a-Si crystallization process by characterizing capped and un-capped a-Si thin films annealed at various temperatures.

2.3.5.2. Experimental

Hydrogenated amorphous silicon was deposited by using an AJA 2000 RF magnetron sputtering system. The deposition temperature was 200°C; and the sputtering pressure was 5 mTorr, which was maintained using a 25sccm flow rate of Ar-H_2(5%) [81]. 200 Watts Radio Frequency (RF) power was applied to the silicon target and 30 Watts Direct Current (DC) bias was applied to the substrate during deposition. The 300 nm thickness of a-Si:H was deposited on the thermally grown 1μm silicon dioxide layer on top of a single crystal silicon wafer. To induce a thermal tensile stress in the silicon films during annealing, silicon nitride was also deposited by reactive RF magnetron sputtering from an elemental silicon target at 5 mTorr pressure, a constant mixture of Ar-H_2 (5%), and nitrogen gas flow rates of 25 sccm of Ar-H_2 and 25 sccm of N_2. In order to compare the effect of the capping layer, variable SiN_x deposition temperatures between room temperature and 400°C were used and a range of 0 and 40 Watts substrate power was applied during SiN_x deposition. Since each SiN_x procedure had a different deposition rate, to achieve the same thickness of silicon nitride (150nm), the deposition time was varied. In order to

characterize the SiN_x capping layers, five different deposition conditions were used, and the sputtering conditions are given in Table 2-2.

To show that higher TCE capping layer enhance the crystallization process, an Al_2O_3 capping layer was also prepared via reactive sputtering. A 150nm thick Al_2O_3 film was deposited on a-Si:H film using a gas mixture of Ar-H_2(5%) (25 sccm) and O_2 (2.8 sccm) at a sputtering pressure of 3 mTorr. 200 Watts RF power was applied to an elemental aluminum target and the substrate temperature was room temperature. The base pressure of the system before a-Si:H, SiN_x, and Al_2O_3 deposition was < 5.0×10^{-8} Tor. Figure 2-27 shows the schematic diagram of the film structure. Subsequent to deposition, the films were annealed in a conventional furnace. The annealing temperature was varied from 580, 600, and 700°C; all at a constant 20 hour annealing time. After crystallizing the a-Si, the dielectric cap was removed by a hydro-fluoric (HF) acid wet etch with a 10 to 1 water to HF ratio. Reflectance spectra were measured using a Filmetrics ultraviolet-visible F20-UV reflectometer. Fourier transform infrared spectroscopy of the a-SiNx:H films was carried out using a Bruker Equinox 55 (Bruker), covering the frequency range between 600 and 7500 cm^{-1} with 2 cm^{-1} resolution. The Raman spectra were taken with a Renishaw 100 micro Raman system. All measurements were done using 27 μJ of 632.8nm excitation and 50x long distance objective lens which results in a laser spot size of 2 μm on the sample. Each spectrum is an average of three spectra taken at different sample locations. The crystalline fraction of poly Si was calculated from the Raman spectrum using the equation:

$$\chi = \frac{I_p}{I_p + \gamma I_a}$$

Table 2-2. Deposition conditions of SiN_x capping layers (RF: 200 watt, Pressure=5mTorr, and refractive index was measure at 632.8nm) (Refractive index of ideal Si_3N_4 is 2.05)

Sample	$Ar-H_2/N_2$ gas flow rate (sccm)	DC substrate power (W)	Temperature (^oC)	Deposition rate (nm/min)	refractive index(n)
SN-1	25/25	0	R.T.	1.85	2.00
SN-2	25/25	0	400	1.76	2.20
SN-3	25/25	30	200	1.29	1.97
SN-4	25/25	40	165	1.29	2.15
SN-5	25/25	40	R.T.	1.10	1.92

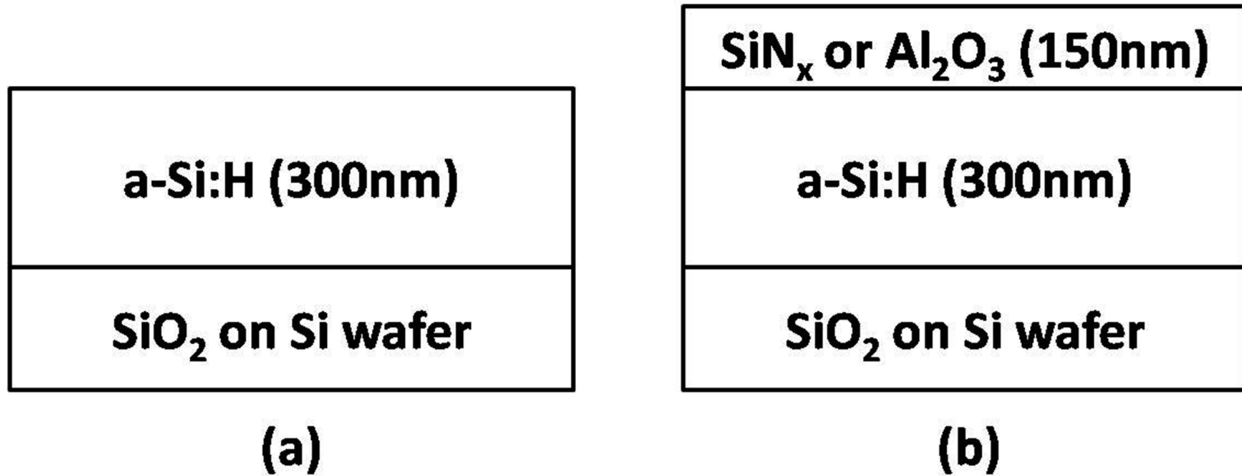


Figure 2-27. Schematic diagram of the film structure: (a) uncapped silicon, and (b) SiN_x or Al_2O_3 capped silicon films.

The peak areas of poly Si and a-Si, I_p and I_a respectively, were obtained by Lorenzian fitting procedures; and γ is 0.88 for small crystalline fractions [80]. Grazing angle X-ray diffraction data was also measured using a Philips Xpert Pro X-ray diffractometer using a CuK_α target. The stress of the thin films was obtained using a Frontier Semiconductor FSM 128 thin film stress measurement system by measuring the curvature of the thin films/substrate. The stress is given by the Stoney equation: [60]

$$\sigma = \frac{ED^2}{6(1-\nu)Rt}$$

where E, D, ν, R, and t are the Young's modulus, the substrate thickness, Poisson's ratio, the beam radius of curvature, and the film thickness, respectively. To understand the evolution of the thin film stress, wafer curvatures were measured at various stages of the thin film processing.

2.3.5.3. Results and Discussions

For the silicon nitride capping layer deposition, the film properties were varied by DC substrate power and deposition temperature. To quantify the change in the SiN_x film with the deposition conditions, the refractive index value was determined. Generally, a lower index corresponds to a reduced density film, typically due to defects. However, nitrogen rich-SiN_x also has a lower refractive index relative to stoichiometric silicon nitride films. The volume expansion of a superstoichiometric SiN_x film induces a compressive stress in the SiN_x film, and the density is reduced [82-83]. Therefore, it was speculated that as the refractive index was reduced from the ideal Si_3N_4 value (~2.05), the TCE value of the SiN_x would increase. The TCE increase should therefore induce more extrinsic thermal stress in the underlying silicon films during annealing. Accordingly, we chose the SN-3 (200°C temperature and 30 watts DC bias) and SN-5 (Room temperature and 40 watts DC bias) deposition conditions as the optimum conditions for the silicon nitride capping layer deposition processes.

Initially, Raman spectra were used to determine the effects that the SiN_x capping layers had on the film stress and ultimately the crystallinity. Figure 2-28 shows the Raman spectra a-Si films without a capping layer, and with SiN_x capping layers (SN-3 and SN-5) that were annealed at 580°C.While the silicon nitride with SN-3 deposition condition revealed a higher poly crystalline silicon peak relative to the un-capped sample, the silicon nitride capped sample with SN-5 deposition conditions did not reveal any crystallization at these annealing conditions. To understand this difference, infrared spectroscopy was used to investigate the SiN_x films.
The data in Figure 2-29 compares the infrared spectra of the two as-deposited silicon nitride films. The infrared spectra of a-SiNx:H is well documented and the peak absorption band

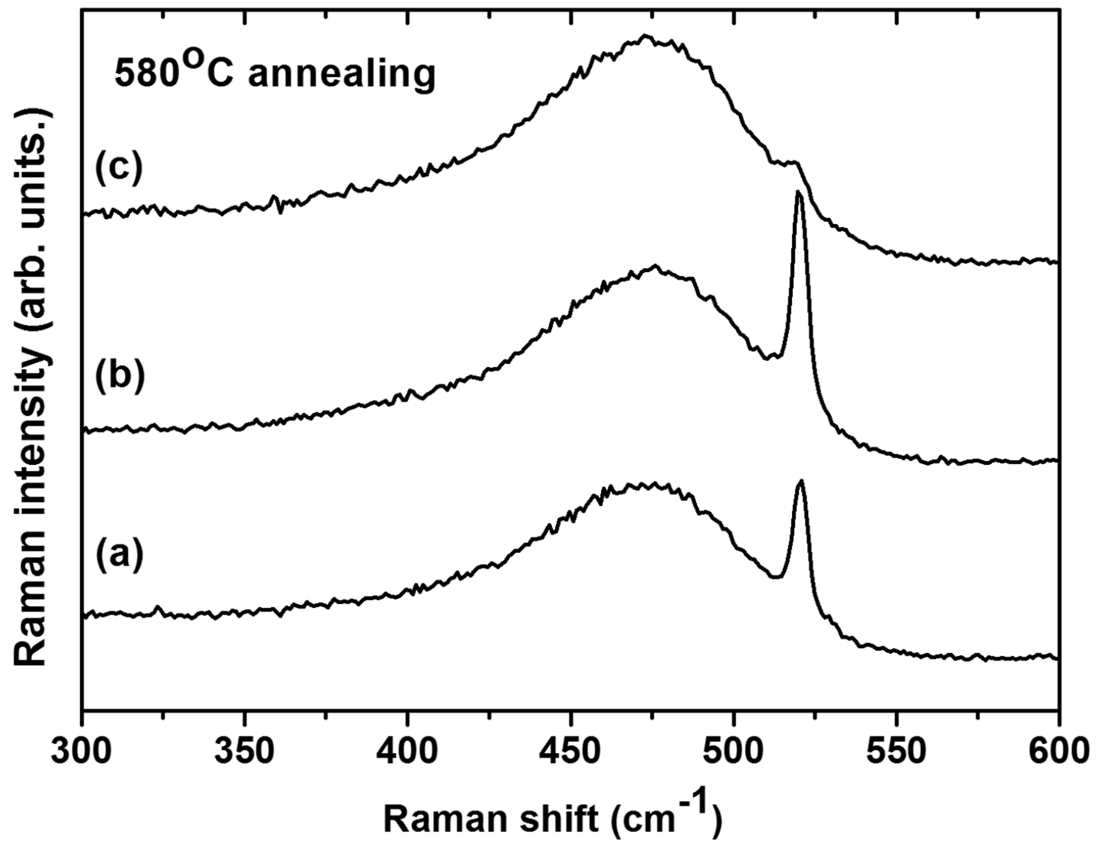


Figure 2-28. Raman spectra of (a) uncapped silicon, and two different deposition conditions of silicon nitride capped silicon after 580°C annealing; (b) SN-3 (200°C temperature and 30 watts DC bias), and (c) SN-5 (room temperature and 40 watts DC bias)

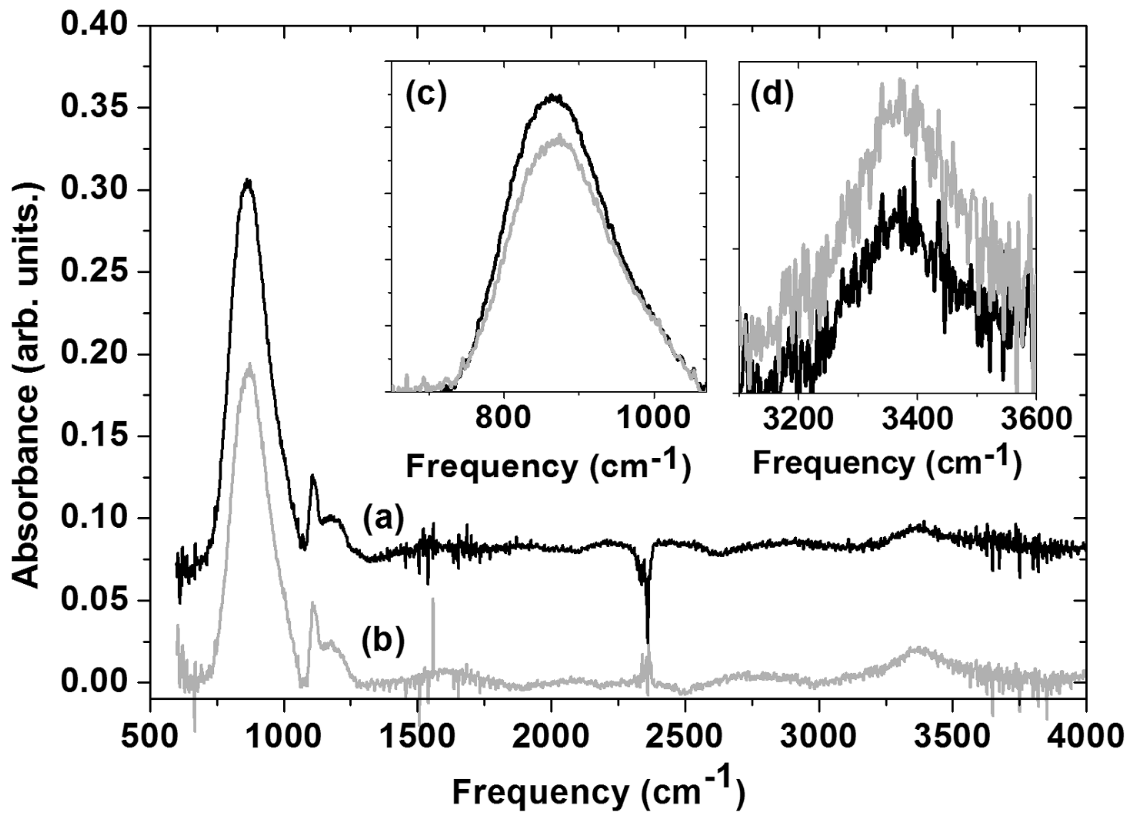


Figure 2-29. Infrared spectra of a-SiN_x:H films deposited using two different deposition conditions: (a) SN-3; 200^oC, 30 watts DC bias and (b) SN-5; R.T, 40 watts DC bias (Table 1). To distinguish the hydrogen content, the insets show infrared peaks (c) near 850 cm^{-1} (Si-N asymmetric vibration) and (d) near 3340 cm^{-1} (N-H stretching)

observed at 3340 cm^{-1} corresponds to a stretching vibration of N-H, and the peak centered at 850 cm^{-1} is assigned as an asymmetric vibration of Si-N [83-87]. The higher intensity of N-H at 3340 cm^{-1} and lower intensity of Si-N at 850 cm^{-1} in the silicon nitride deposited at room temperature and higher DC bias condition (SN-5) relative to SN-3 indicates that there is more hydrogen in the SN-5 SiN_x capping layer. Thus, we attribute the lower refractive index value of silicon nitride deposited at room temperature and higher DC bias to higher hydrogen contents rather than higher nitrogen content. The hydrogen content in SiN_x has been reported to be inversely proportional to the biaxial elastic modulus because hydrogen bonding generates porosity during the SiN_x film growth and lowers the number of Si-N bonds [82]. The reduced modulus in the silicon nitride is expected to generate a smaller volume expansion during annealing, as well as less thermal tensile stress, and thus, did not improve the crystallization.

In order to confirm the enhanced crystallization effect via a stress induced capping layer, an Al_2O_3 capping layer was prepared because Al_2O_3 has an even higher TCE ($Al_2O_3 = 8.4 \times 10^{-6}$ °C^{-1}) than silicon nitride. While it is well-known that aluminum metal [71-73] can enhance the silicon crystallization via a MIC process, the thermodynamic stability of the aluminum oxide should ensure that this mechanism is not operative in this study. Figure 2-30 shows the Raman spectra, respectively, of Si samples annealed at 600°C. To distinguish the shift of Raman peak position clearly, all samples were annealed at 600°C. Samples include silicon films without a capping layer, SiN_x cap (using SN-3 conditions), and Al_2O_3 cap. In order to confirm the induced stress from the TCE mismatch at 600°C annealing, Raman peak position shift was used and is shown in Figure 2-31. To compare the shift of the peak, measured single crystalline silicon data (520.80 cm^{-1}) is also shown. From Figure 2-30 and 2-31, silicon crystallized with an Al_2O_3 capping layer shows enhanced crystallization relative to the films without a cap, and the SiN_x

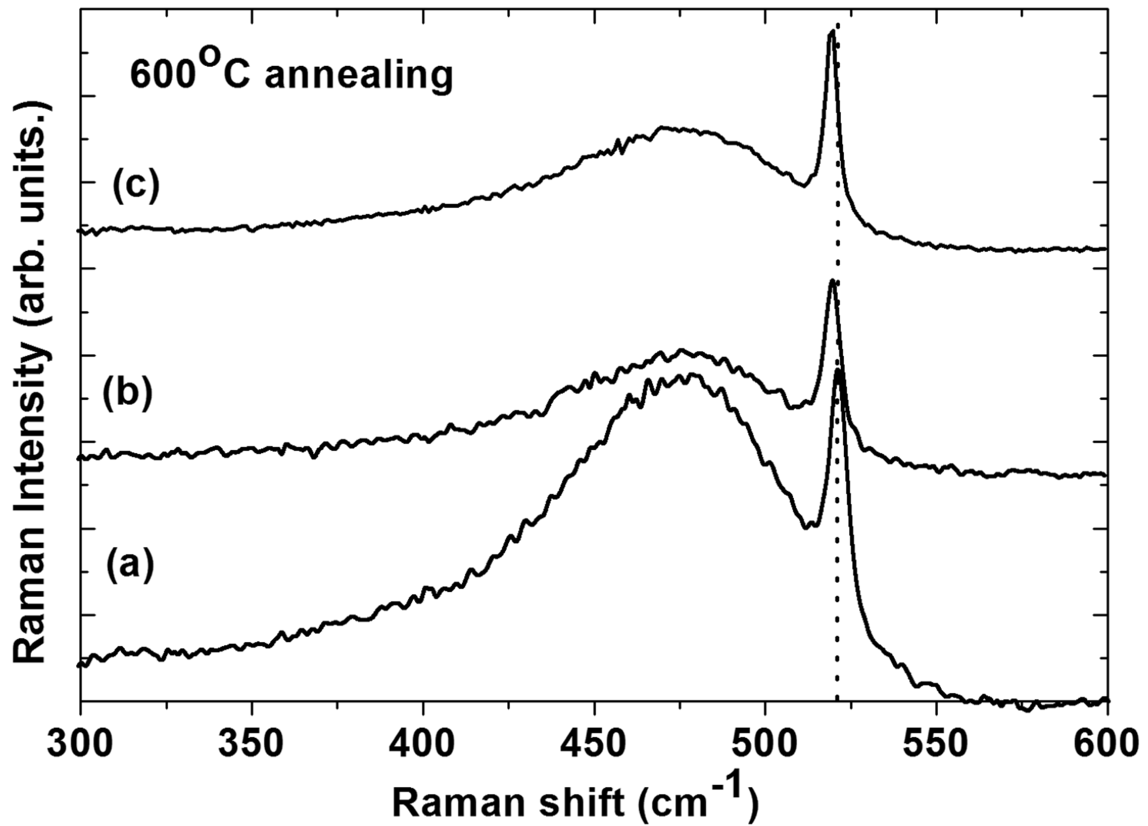


Figure 2-30. Raman spectra of uncapped, SiN_x, and Al_2O_3 capped silicon after 600°C annealing. (a) uncapped silicon, (b) SiN_x capped silicon (SN-3; 200°C temperature and 30 watts DC bias), and (c) Al_2O_3 capped silicon (Dashed line indicates the measured Raman peak position of single crystalline silicon)

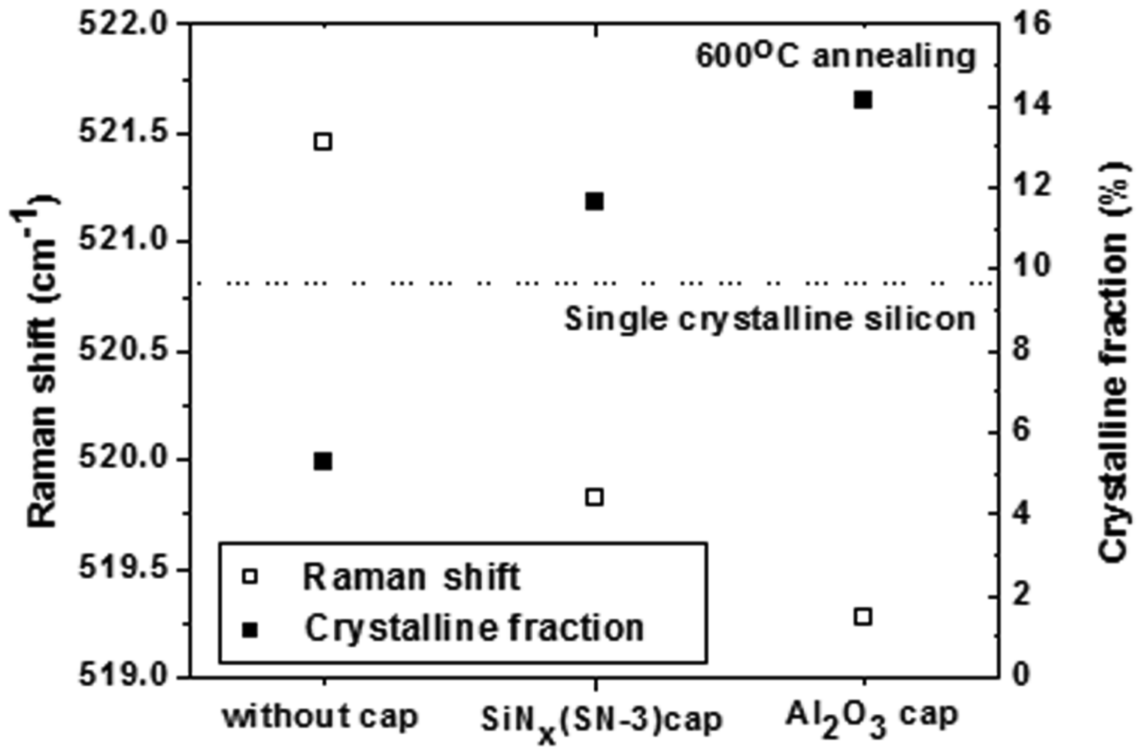


Figure 2-31. The Raman shift position (left axis) and crystalline fraction (right axis) of uncapped silicon, SiN_x capped silicon, and Al_2O_3 capped silicon annealed at 600°C

capped sample. Generally, a decrease of the Raman shift is related to a tensile stress, while an increase indicates a compressive stress. The Raman shift of the SiN_x and Al_2O_3 capped samples decreased relative to the uncapped sample, which suggests that there is more induced residual tensile stress in the silicon film after the post deposition annealing treatment. Moreover, the Al_2O_3 capped silicon has a higher crystalline fraction than SiN_x capped silicon and the uncapped silicon.

In addition to the Raman results, grazing angle X-ray diffraction scans were taken and analyzed to show the stress effects on the crystallinity and orientation. To compare more extensively, the annealing temperature was increased to 700^oC. Figure 2-32 and 2-33 show X-ray diffraction data and peak position of 700^oC annealed samples. The relative amount of the residual stress was estimated from the shift of silicon (111) X-ray diffraction peak positions of the silicon of the uncapped, SiNx capped, and Al_2O_3 capped, films respectively. Figures 2-32 and 2-33 indicate the results of (111) peak position shift. SiN_x and Al_2O_3 cap have a higher peak position than the uncapped silicon sample. The residual stress in the film is related to the shift of X-ray diffraction (XRD) peak position by detecting the slight changes in inter-planar spacing (d-spacing) of the crystal planes. Because the d-spacing is inversely proportional to the shift of peak position, an increase of peak position suggests a bi-axial tensile stress and a decrease of peak position indicates a bi-axial compressive stress. Thus, the XRD data also shows that there is a residual bi-axial tensile stress in the SiN_x and Al_2O_3 cap samples. Additionally, the observed increase in the ratio of (111) and (220) peak intensities is consistent with a relaxation of compressive stress [62,88-89]. In addition to the Raman and XRD data, the reflectance spectra of silicon films annealed at 700^oC with and without capping layers are shown in Figure 2-34. For comparison, single crystal silicon and hydrogenated-amorphous silicon are also presented. Of

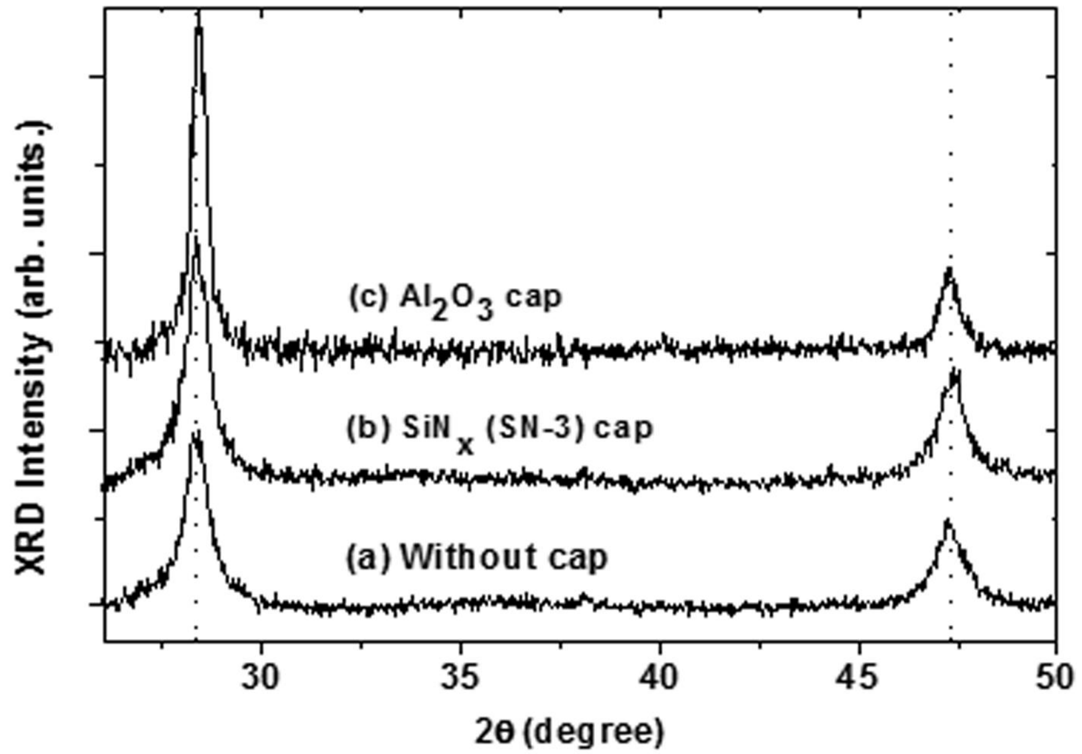


Figure 2-32. X-ray diffraction spectra of (a) uncapped silicon, (b) SiN_x (SN-3) capped silicon, and (c) Al_2O_3 capped silicon annealed at 700°C

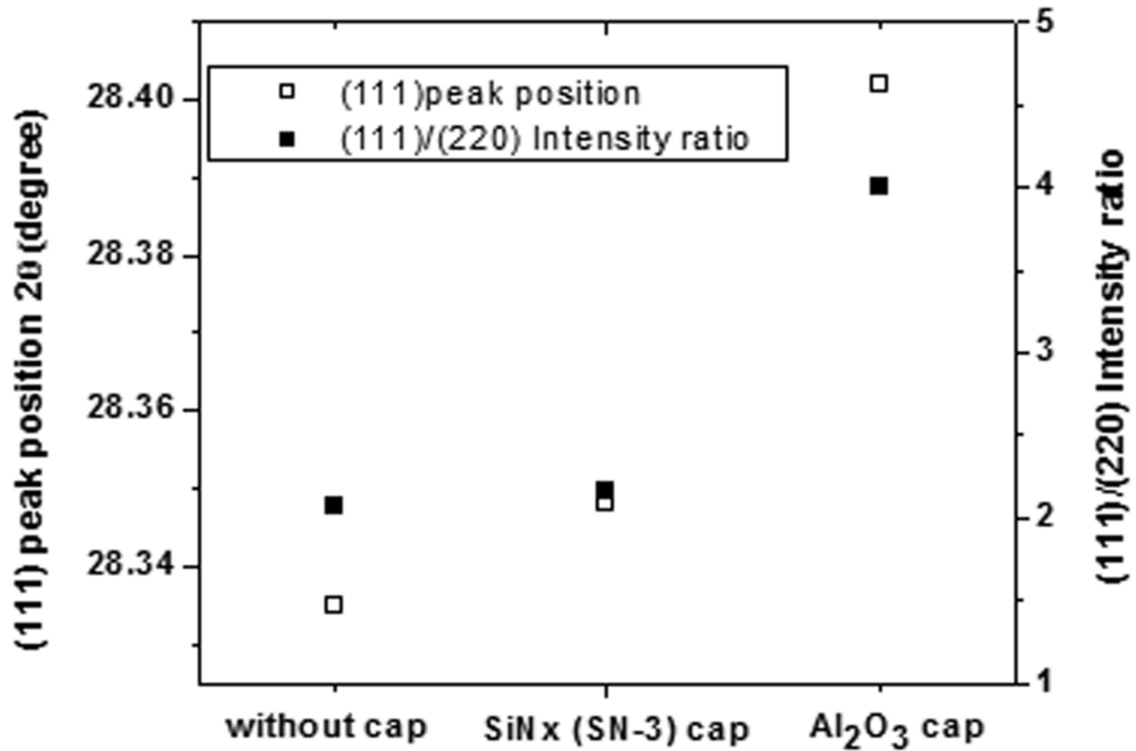


Figure 2-33. X-ray diffraction (111) peak position (left axis) and the ratio of (111)/(220) silicon peak intensity (right axis) of the uncapped silicon, SiN_x capped silicon, and Al_2O_3 capped silicon annealed at 700°C

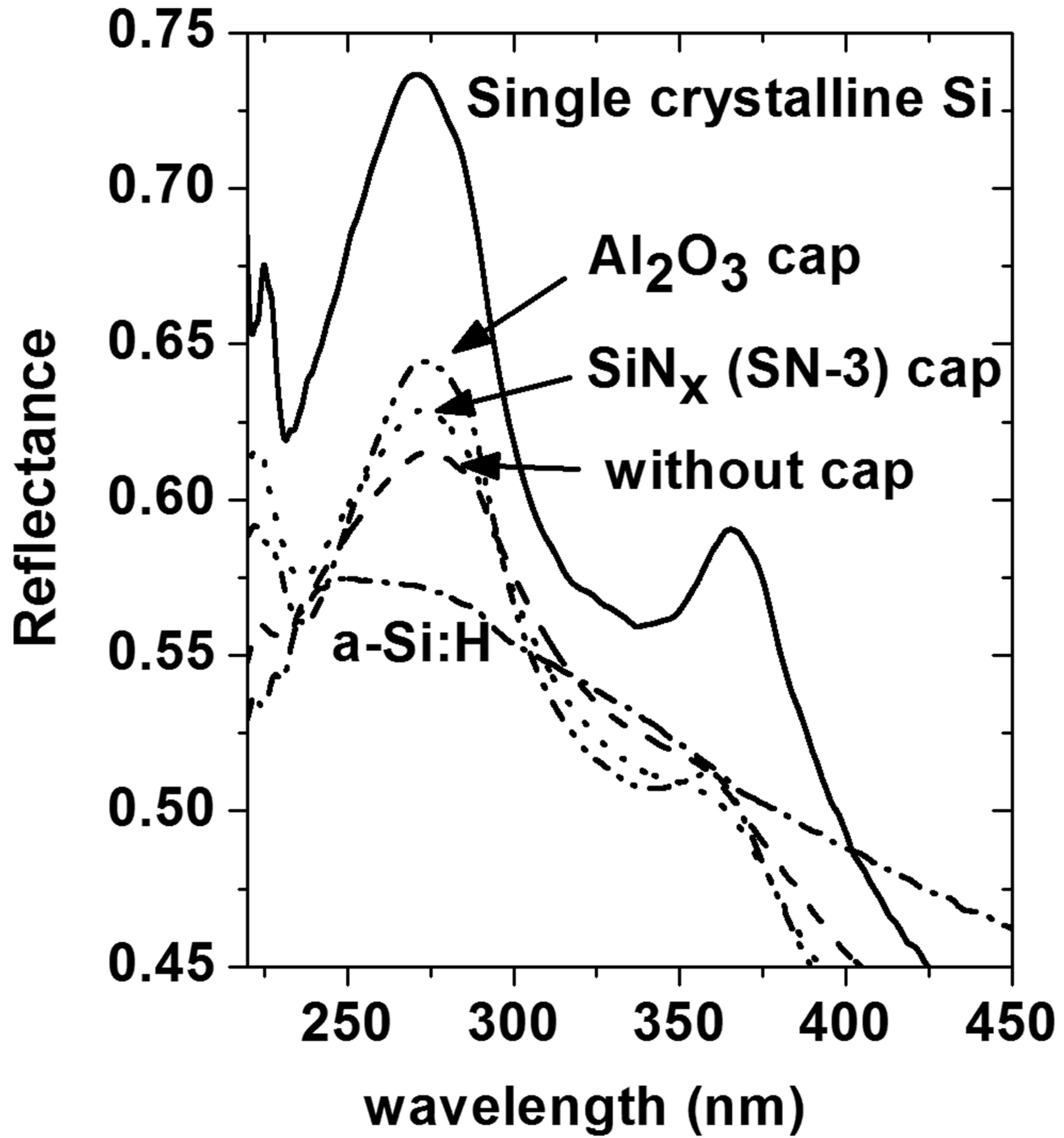


Figure 2-34. Reflectance spectra of uncapped silicon, SiN_x capped silicon, and Al_2O_3 capped silicon annealed at 700^oC. Spectra of single crystalline Si and a-Si:H (not annealed) are presented for comparison

the sputtered films, the Al_2O_3 capped silicon film has the highest UV reflectance and the strongest 275 nm and 360nm peaks; the SiN_x capped film has the next highest reflectance, which is followed by the annealed un-capped silicon film. Finally, the un-annealed amorphous silicon film has the lowest reflectance.

To confirm the thin film stress evolution evidenced in the XRD and Raman results, the calculated thin film stresses were measured and are presented in Table 2-3. The stress of amorphous silicon deposited on the buffered oxide films was obtained by measuring the change in the substrate radius curvature (i.e. before and after the silicon deposition). The three amorphous silicon films deposited by RF sputtering have a similar residual stress, which was ~ -800MPa (using the convention that negative stress is compressive). After annealing the film stacks for $600^{o}C$ for 20 hours and removing capping layer, each sample; Si no capping layer, SiNx capping layer, and Al_2O_3 capping layer had different residual stress values. The un-capped silicon film had the lowest stress level of tensile ~400 MPa, which is consistent with Kulikovsky et al. which reported that sputtered amorphous silicon films have an as-deposited compressive stress and after annealing the residual compressive stress is relieved [90].

The annealed silicon films with capping layers measured higher tensile stress values proportional to the TCE mismatch of each capping film. The Raman and measured stress data indicates that the residual stress of the capped silicon films measured after the cooling cycle has a larger tensile relative to the uncapped silicon. The thermal stress in amorphous silicon films will vary during heating and cooling depending on the TCE of the substrate and capping layer. Figure 2-35 shows schematic representations of the residual stress in the silicon films as a function of the temperature for a-Si films with and without a capping layer. The biaxial stress of the sample without a capping layer during heating is expected to have a constant value because

Table 2-3. Measured thin film stress before and after annealing (600^oC, 20 hours) for the 3 different film stacks. The thickness of amorphous silicon is 300 nm and capping layer is 150nm. (TCE of a-Si is $2.0x10^{-6}$ $^oC^{-1}$)

Sample	Capping film & TCE ($^oC^{-1}$)	Stress of a-Si before capping & annealing (MPa)	Stress of poly- Si after annealing & decapping (MPa)
w/o cap	no	-865	415.7
SN-3 cap	SiN_x;$3.3x10^{-6}$	-825.6	554.6
Al_2O_3 cap	Al_2O_3;$8.4x10^{-6}$	-820.2	841.4

the TCE of a-Si, SiO_2, and the silicon substrate have nearly the same value. During the 20-hour soak at the peak temperature, some of the residual compressive stress in the as-deposited film will be relieved. During the cooling cycle, again, the little thermal stress will be recovered because of the close TCE values of Si and SiO_2.

The stress-temperature cycle for the capped silicon films are somewhat different relative to the uncapped films. During the temperature ramp, the a-Si capped with the SiN_x and Al_2O_3 films will be thermally stressed in biaxial tension during the heating cycle. The slope of stress versus temperature and the magnitude of thermal stress generated during heating by the TCE mismatch are reported to be on the order of 10^8 Pa [91-92]. These values are in agreement with measured stress values.

While the specific mechanism for the stress-induced crystallization is not fully understood, it is surmised that the biaxial tensile strain enhances the silicon atom mobility by expanding the lattice, and can be high enough to actually break Si-Si bonds, thus enhancing the stress relaxation and crystallization [78]. It is worthwhile to note that while experimental evidence exists for biaxial stress enhanced crystallization [93], and diffusion [94], theoretical understandings are not completely resolved relative to the hydrostatic case [95]. Following Figure 2-35, finally, during the cooling cycle the thermal stress will reverse and the net change in the residual stress will be the relieved stress realized during the 20 hours at the peak temperature. The enhanced crystallization of amorphous silicon thin films has been achieved using thin film capping layers to induce a thermal biaxial tensile stress during annealing. X-ray diffraction, Raman spectroscopy, and reflectance data revealed that the silicon films capped with a higher thermal coefficient of expansion material had better crystallinity. Furthermore, the analysis of the XRD, Raman, and stress measurements data confirmed a residual tensile stress in the capped

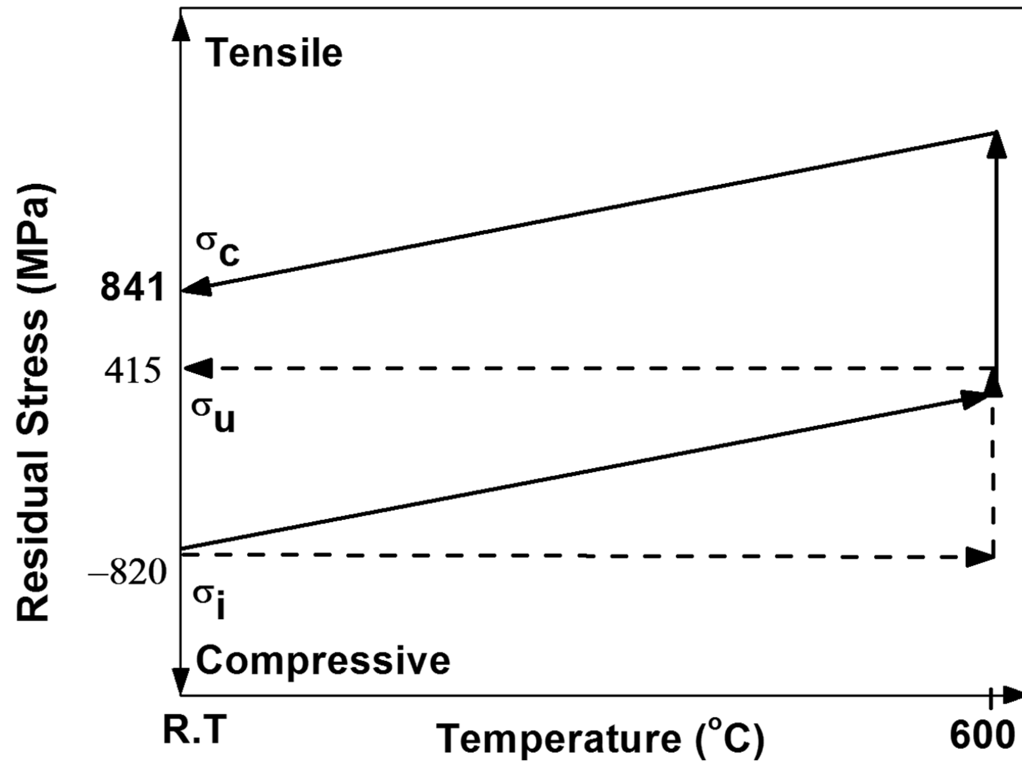


Figure 2-35. Schematic representation of the residual stress of silicon films with SiN_x or Al_2O_3 capping layer (solid line) and uncapped silicon layers (dot line) as a function of temperature (σ_i = initial stress in the silicon film, σ_u = residual stress in the uncapped silicon after annealing and cooling, and σ_c = residual stress in the capped silicon after annealing and cooling

silicon films after annealing relative to uncapped silicon films. The enhanced crystallization observed in the capped a-Si:H films is attributed to the expanded silicon lattice induced by the biaxial tensile stress which results in enhanced silicon atom mobility and consequently crystallization.

2.3.6. Sputtering n-type doped amorphous silicon (n^+ a-Si:H) film

2.3.6.1. Background

Sputtered n-type doped silicon film is deposited by using n-type doped solid target similar to those of sputtering of amorphous silicon with intrinsic silicon target. Various working pressure, temperature, RF power, substrate power, and gas flow will be the function to determine the properties of the film. To achieve good ohmic contact properties, lower resistivity is essential for the film with reasonable deposition rate.

2.3.6.2. Experimental

An AJA 2000 RF sputtering was used to deposit n^+ a-Si film. Solid doped silicon target (Kurt J. Lesker) was used to deposit with Ar and Ar-H_2 working gas. RF power was varied between 100 and 300 watts, pressure were changed from 3 to 10 mTorr, temperature was varied from room temperature to 300°C, and substrate power was controlled from zero to 30 watts. The n^+ a-Si film was deposited onto the 500nm PECVD grown SiO_2 film on Si wafer. For measuring stress, Frontier Semiconductor FSM 128 thin film stress measurement system was used, and thickness of the film was obtained from ultraviolet-visible UV-20 reflectometer.

2.3.6.3. Results and discussions

A process for depositing n^+ a-Si film using Ar-H_2 gas has been performed by a previous [51]. Following his work, two different gases (Ar and Ar-H_2) were used to measure the properties with 5 mTorr pressure, 200 watts RF power, no substrate power, and 200°C temperature. Figure 2-36 shows the residual stress and resistivity of n^+ a-Si film with two different gases. Compared to Ar-H_2 gas, when pure Ar gas was used during sputtering, it shows the lower resistivity and film stress. Since hydrogenated n^+ a-Si film contained hydrogen molecules in the silicon network, hydrogen passivates the structural defects such as dangling bonds and results in the decrease of micro or nano voids in the network, which can play an important role in generating localized tensile stress in the silicon network [74]. Additionally, due to the competition between hydrogen and phosphine, less P atoms were apparently absorbed in the network, which leads a lower resistivity of the film as film resistivity is inversely proportional to the concentration of the dopant. Unfortunately, the main chamber of sputtering system were oxidized or contaminated at the certain periods of the time. It showed the abnormal behavior of resistivity of the n^+ a-Si film. Therefore, n^+ a-Si film resistivity with the same deposition conditions was measured to compare the resistivity with different chamber conditions. Figure 2-37 shows the n^+ a-Si film resistivity with the different chamber conditions while deposition condition was same. Prior to cleaning of the chamber, the resistivity of the film reached up to 375.0 ohm-cm. After cleaning, however, it reduced to 25.2 ohm-cm. Though it reduced one order of magnitude, it still can't be used as ohmic contact layers. For example, used it as ohmic contact layer, the resistivity of the film should be below 10.0 ohm-cm. Herein, I ignored the contact resistance term, which is originated from the interface charge trapping effects,

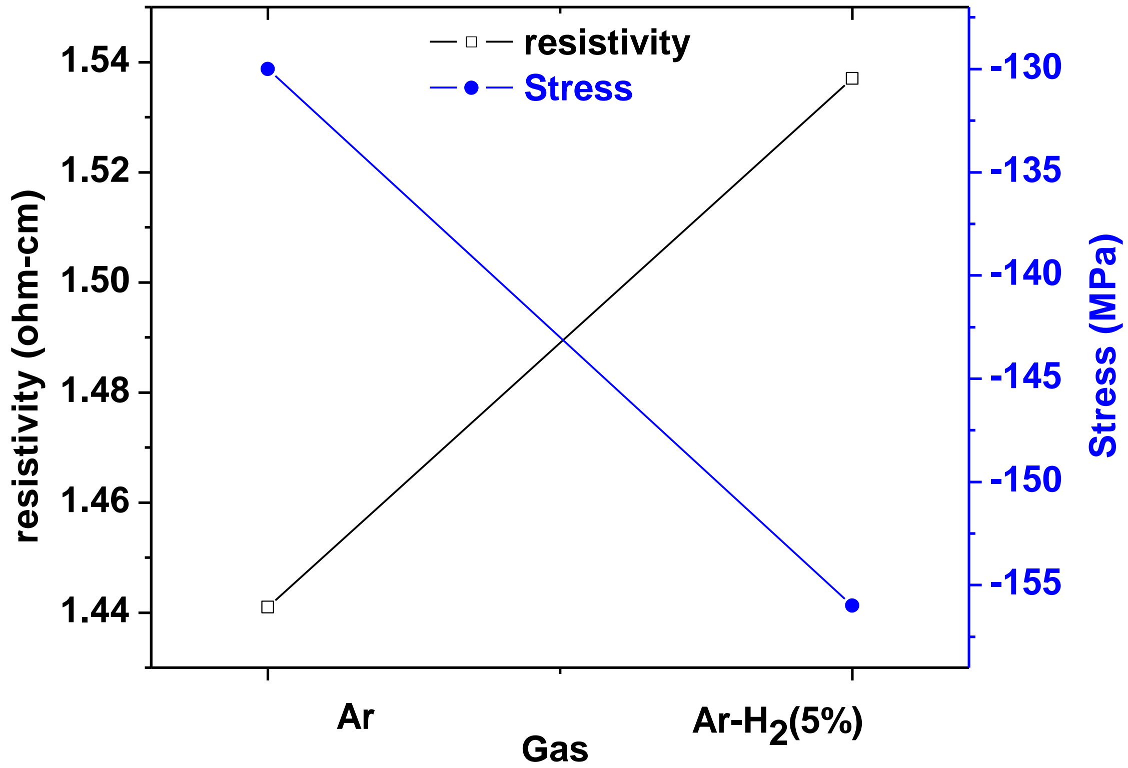


Figure 2-36. Resistivity and residual stress of sputter deposited n^+ a-Si film with different working gas; pure Ar and 5% hydrogenated Ar (Ar-H_2)

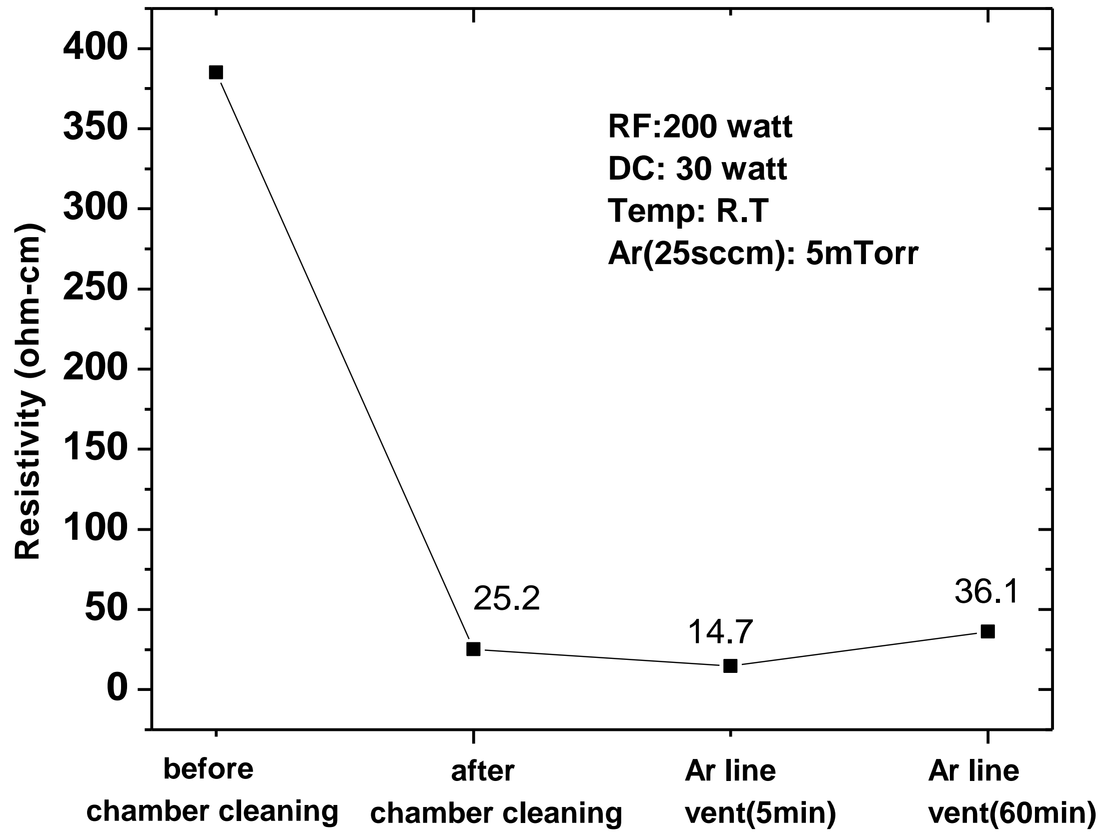


Figure 2-37. Resistivity of the n^+ a-Si film with the conditions of sputtering chamber

since the film resistivity of the bulk n^+ a-Si film acts as a limiting factor to determine the transistor characteristics. Other possibility of abnormal high resistivity of the film was the gas line contamination or leaking. After installing a new Ar gas line and purging for 5min and 60min, the film resistivity were measured to 14.7 ohm-cm and 36.1 ohm-cm, respectively. If the problems were existed in the gas line, as long as venting should have to show a lower resistivity. However, it shows the increased resistivity relatively to the even 5min Ar gas line purge. From all observed results, it is speculated that another source of contamination of oxygen was existed in the main chamber or pressure controller at the gate. Other thin films such as silicon, silicon dioxide, silicon nitride, and metals such as Chromium and Aluminum did not show the significant change of their properties.

For design of experiments (DOE) to optimize the resistivity, RF power, Substrate power, temperature, pressure, and distance between the target and the substrate were varied. The purpose of DOE was to reduce the ability of oxygen contamination onto the substrate during film growth to reduce the film resistivity. Figure 2-38 represent the RF power, and distance effects to the film resistivity while substrate power, pressure, and temperature were fixed at 30 watts, 5 mTorr, and room temperature, respectively. Increasing RF power from 200 to 300 watts, the deposition rate was increased and film resistivity was reduced. Higher power generates more species from target materials and yields high deposition rate resulting lower film resistivity reducing oxygen absorbs in the film. Similar effect also observed in the target-to-substrate distance change. Decreasing the distance between the target and the substrate, decreased the resistivity of the n-doped a-Si. Figure 2-39 shows the resistivity and deposition rate of n^+ a-Si film as a function of substrate power with different temperature. As increasing substrate power, deposition rate was reduced. It’s the same phenomena of what occurs during intrinsic a-Si:H film

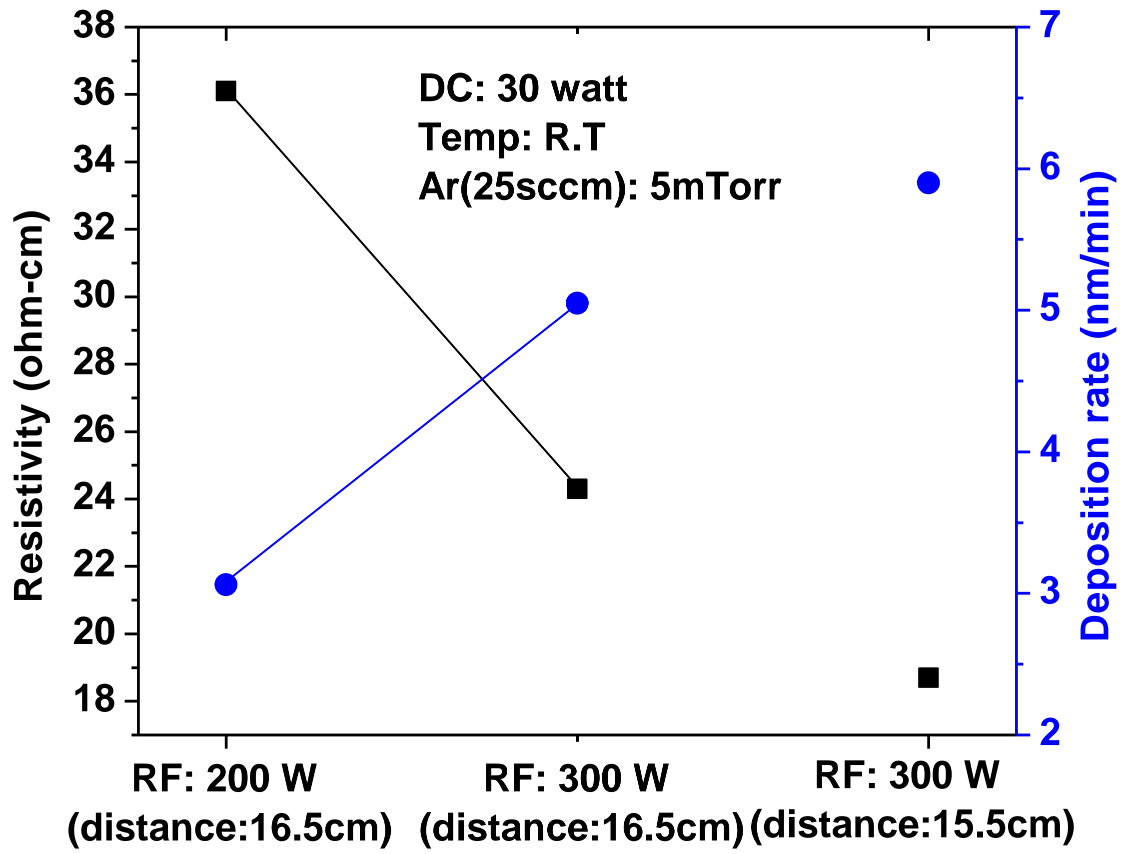


Figure 2-38. The film resistivity and deposition rate of n^+ a-Si film as a function of RF power and distance between the target and the substrate

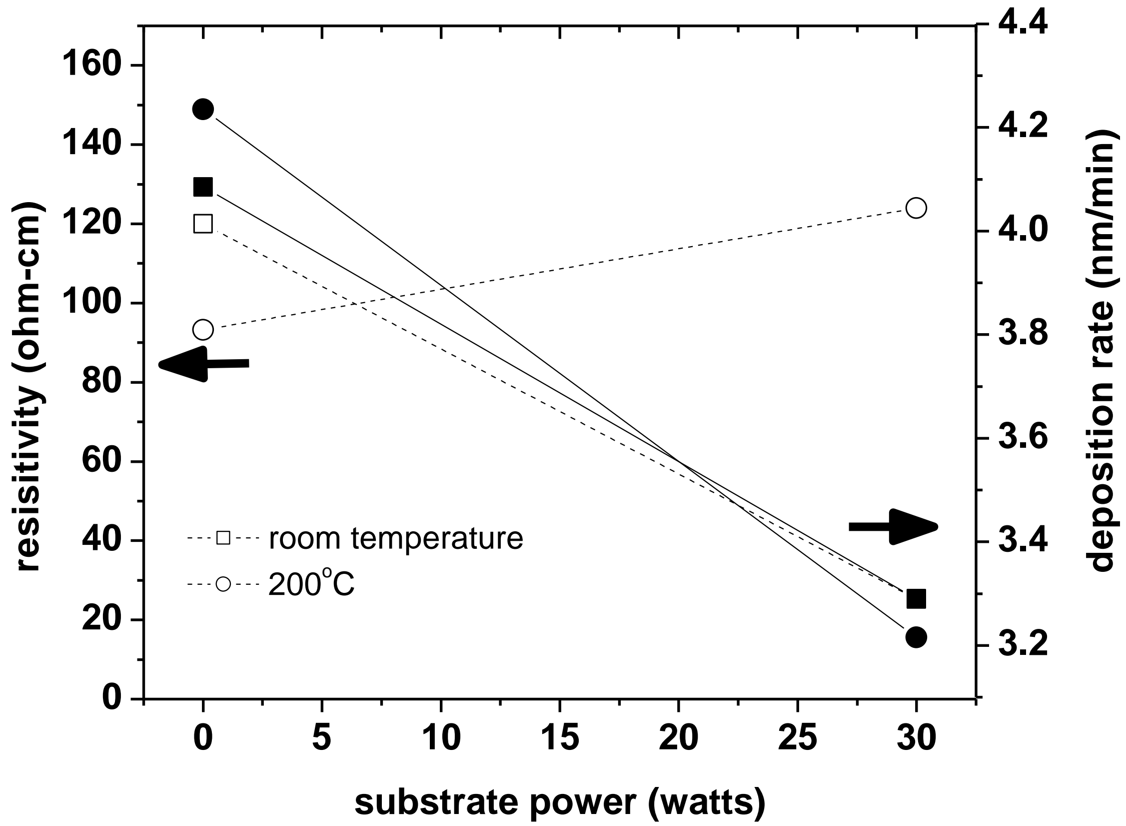


Figure 2-39. The film resistivity and deposition rate of n^+ a-Si film as a function of substrate power during deposition. Solid fills represents the deposition rate, and empty fills represents the film resistivity.

deposition. However, room temperature deposited n^+ a-Si film shows that the film resistivity was reduced with increasing substrate power. At 200°C temperature, however, the deposited n^+ a-Si film shows an increase of the film resistivity. At higher temperature of 200°C, more oxygen likely outgases from the chamber walls incorporates into the film since the activity of oxygen was increased as the working temperature increased.

To reveal the pressure effects, different pressure regime of the deposition conditions were conducted by measuring resistivity and deposition rate. Figure 2-40 represent the results as a function of working pressure. Increasing pressure, the deposition rate was reduced since low pressure results to the longer mean free path of sputtered species, which leads to more directional sputtering and more accumulation on the substrate. However, the resistivity shows the minimum point at 5 mTorr. Increasing the Ar partial pressure during sputtering decreased the film resistivity to a minimum of 14.7 ohm-cm. Further increase in Ar partial pressure from 5 mTorr to 10 mTorr, resulted in an increase in the film resistivity, which is likely due to the reduced sputtering rate. At lower pressures (3mTorr), the arrival energy of the energetic sputtered species likely is too high and preferentially desorbs phosphorus atoms and inhibits their incorporation. Thus 5mTorr appears to be a balance between a high sputtering rate to inhibit oxygen incorporation, but also has a low enough energy distribution for the energetic arriving species which do not inhibit phosphorus incorporation in the lattice.

Additionally, direct current (DC) target power source was used to apply higher power for inducing high ion energy to the silicon and phosphine. Pressure, temperature, and substrate power was fixed at 5 mTorr, room temperature, and no substrate power. Figure 2-41 shows the results, which indicates the same preference of increasing power reducing the resistivity. But, the

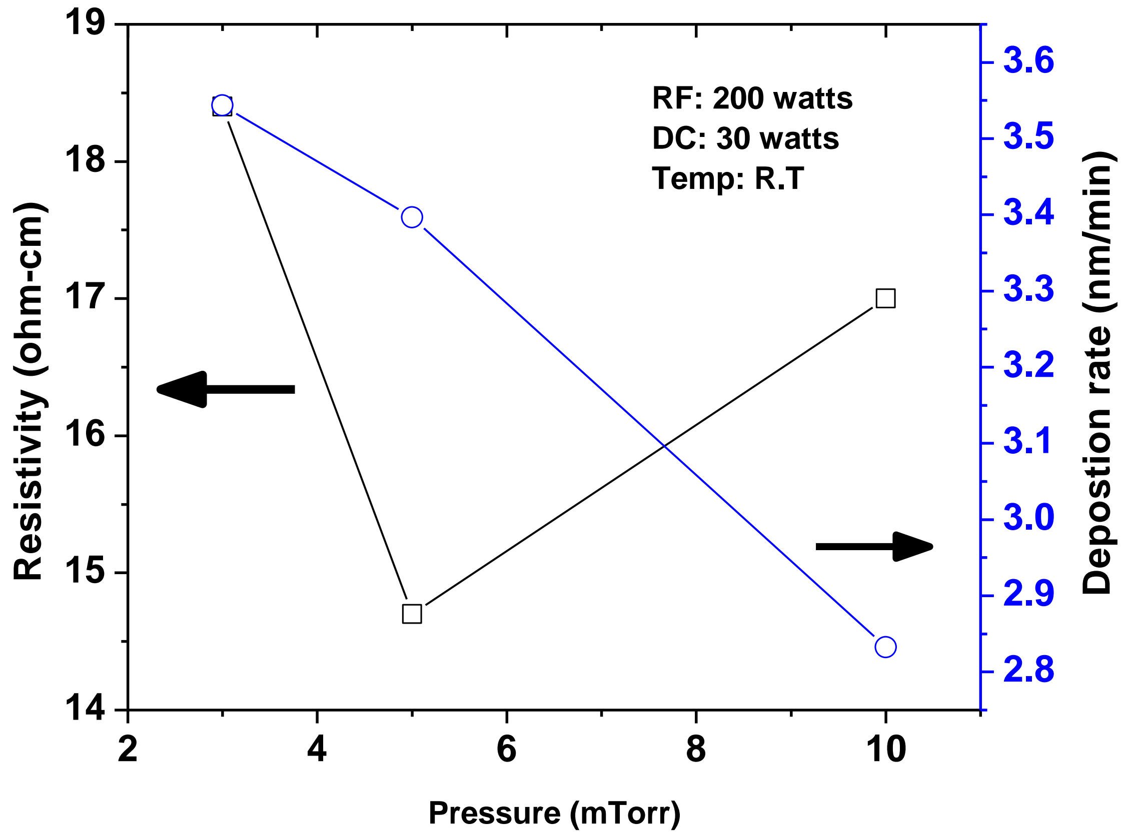


Figure 2-40. The film resistivity and the deposition rate of n^+ a-Si film as a function of working pressure during sputtering

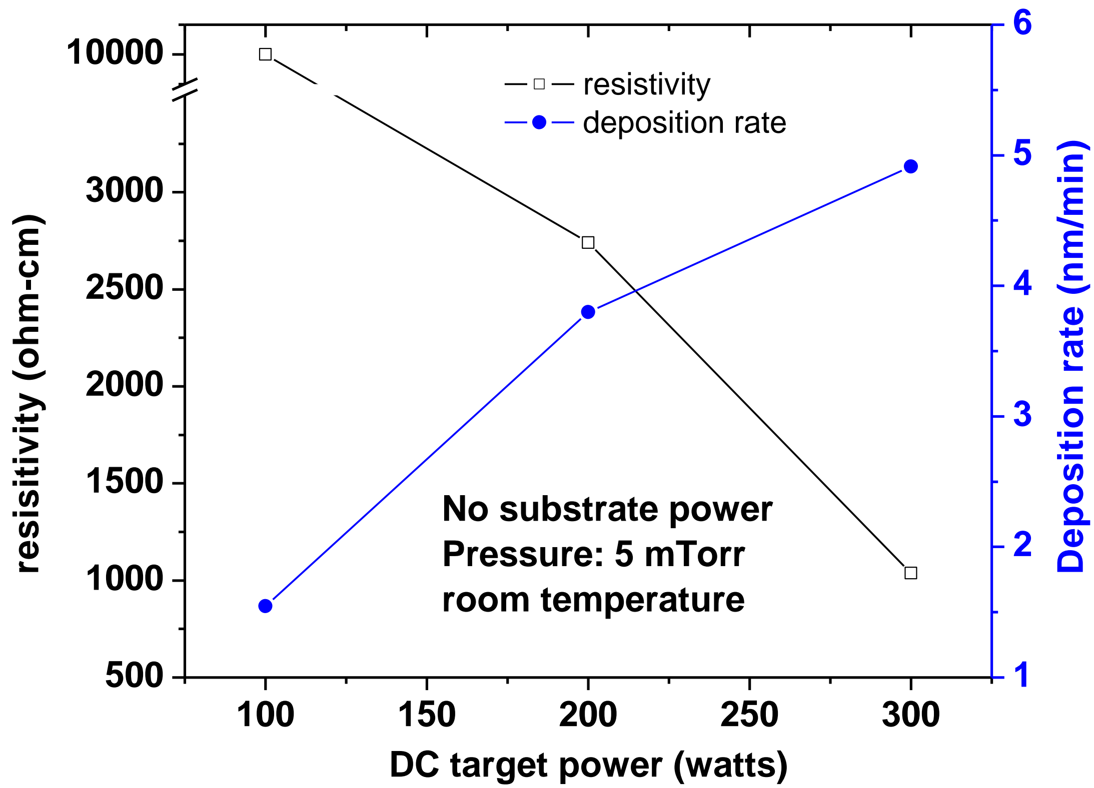


Figure 2-41. The film resistivity and deposition rate of n^+ a-Si film as a function of substrate power when direct current (DC) power supply was used at the target.

resistivity value was three orders of magnitude higher than when RF power was used, and is attributed to the degraded chamber conditions.

Finally, Table 2-4 shows the developed thin film deposition processes compatible for low stress thin film transistor fabrication and Table 2-5 summarizes the standard recipes for thin film deposition, Cr wet etching, and photolithography processes.

Table 2-4. Developed thin film deposition process optimized for thin film transistor

Thin film	Materials	Equipment	Power (watt)	Gas flow rate (sccm)	Pressure (mTorr)	Temp. (^oC)	depo. rate (nm/min)	properties [refractive index(n)] [residual stress(σ)] [resistivity(ρ)]	Comments
Metal electrode	Chromium	RF sputter	RF: 200 DC: 5	Ar (25)	5	200	4.6	σ: 10 MPa (100 & 200nm)	
Gate dielectric	SiO_2	RF sputter	RF: 200 DC: 10	Ar/O_2 (25/3.8)	3	300	6	n: 1.46~1.47	reactive sputtering
		PECVD	RF: 20	5%SiH_4-Ar/N_2O (85/157)	1000	350	68.97	n: 1.45~1.46 σ: - 188 MPa (500nm)	
	SiN_x	RF sputter	RF:200 DC:30	Ar/N_2 (25/25)	5	R.T	3	n: 1.97	reactive sputtering
		PECVD	RF:20	5%SiH_4-Ar/NH_3 (200/30)	1200	300	26.67	n: 2.05 σ: 300 MPa (300nm)	stoichiometric
		PECVD	RF:40	5%SiH_4-Ar/NH_3/N_2 (150/2/790)	600	350	15.42	n: 2.20 ~2.25 σ: 50 MPa (300nm)	Low stress Si-rich SiN_x 400^oC (nearly same)
Semi-conductor	a-Si:H	RF sputter	RF:200 DC:30	Ar-H_2 (25)	5	200	3.57	n: ~4.4 σ: -825 MPa (300nm)	
		PECVD	RF:10	5%SiH_4-Ar (500)	1000	350	27.25	σ: -125 MPa (200nm)	to avoid wafer sliding, add He
	Poly-Si	LPCVD		SiH_4 (75)	300	625	13		
Ohmic contact	n^+ a-Si	RF sputter	RF:200 DC:30	Ar (25)	5	R.T	~3	ρ:1.44 ohm-cm	To reduce resistivity, 1) increase: RF, DC power 2) decrease: temp., distance
	n^+ poly-Si	LPCVD		SiH_4/PH_3 (77/23)	300	625	2.875	ρ:2.0x10^{-2} ohm-cm	
Passivation	SiN_x	PECVD	RF:40	5%SiH_4-Ar/NH_3/N_2 (150/2/790)	600	350	15.42	n: 2.20 ~2.25 σ: ~0 MPa (500nm)	Low stress Si-rich SiN_x 400^oC (nearly same)

Table 2-5. The 1st Standard recipes for each thin film process and photolithography process flow.

Standard recipes for thin film deposition process (chapter 2 & 3)							
Material	equipment	Power (watt)	Gas/flow rate (sccm)	Pressure (mTorr)	Temperature (°C)	Deposition rate (nm/min)	Stress (MPa)
Metal(Cr)	sputter	RF(200) /DC(5)	Ar(25)	5	200	4	~ +10 (G:100nm, S/D: 200nm)
Dielectric (SiO_2)	PECVD	RF(20)	5%SiH_4-Ar/N_2O (85/157)	1000	350	69	~ -180 (buffer:500nm)
Dielectric (low stress SiN_x)	PECVD	RF(40)	5%SiH_4-Ar/NH_3/N_2 (150/2//790)	600	400	14.3	~ +50 (gate dielectric:300nm)
Active (a-Si:H)	PECVD	RF(10)	5% SiH_4-Ar (500)	1000	350	24.7	~ -120 (200nm)
Ohmic contact (n^+ a-Si:H)	Sputter	RF(200) DC(30)	Ar (25)	5	200	3.5	~ -20 (50nm)
Standard recipes for Cr wet etching process (chapter 2)							
Cr	CR14S wet etchant at room temperature						
Standard process for photolithography (chapter 2)							
Photoresist (PR)	SPR™220-2.1 photoresist						
PR spinning	Spinning rpm/time (sec) = 3000 / 60 (1.75 μm thickness)						
pre-bake	(90°C / 60sec)						
Exposure	Quintel contact aligner[Vacuum mode] (depending on the PR thickness & illumination power density)						
Post-exposure bake (PEB)	(115°C / 90sec)						
PR develop (°C)	60 sec (CD26 developer)						
Hard bake	(115°C / 90sec)						
Descum	Technics RIE, RF(400 watt), O_2(10 sccm), 150 mTorr pressure, R.T for 30sec						
Etching	Etching (wet or dry etching)						
PR stripping	Microphosit™ remover 1165 (70°C / 30min)						
Ashing	Technics RIE, RF(400 watt), O_2(10 sccm), 150 mTorr pressure, R.T for 60sec						

3. Fabrication and characterization of Thin Films Transistor array

3.1 Design of photolithographic masks

Tanner L-Edit version 8.30 was used to design photolithographic masks for the TFT arrays and TFT-VACNF integration. Heidelberg instruments, DWL 66, high accuracy photomask and direct write laser writer was used to write the masks to be compatible with the Quintel Mask Aligner Q7500, which was suitable for four inch diameter wafers. The minimum feature dimension of the DWL 66 mask writer was 1.6 μm when the 2mm writer head was installed. For the mask aligner, masks and substrates require alignment marks to align multi-levels to each other. Therefore, several alignment marks were patterned on each mask. All masks were designed with 10 x 10 arrays of active matrix transistor in the center region and 60 test pads were placed on the edge region of each die. Each test pad has a different channel width and length size. For a single four inch wafer size, 20 x 20 dies (400 totals) were fabricated. The processing issues for each mask designs are described below.

3.1.1. Gate electrode mask design

When the gate patterns were designed, the critical dimension (CD) loss was considered to be 1 μm since the CD loss for Cr in Cr wet etchant (CR14S) usually showed less than 1 μm. Undercut effects were usually generated when wet etchants were used. Generally, these isotropic etching effects were desirable to increase step coverage of the pattern. They are not favorable because it narrows the electrode line, which results in a resistance increase. To compensate these effects, Cr wet etchant etching time was examined to optimize the etching profile. To fabricate several cross shape alignment marks, the 20 mm laser head for DWL 66 was used, which has a

minimum feature size of ~2 µm. Six inch rectangular shape photoresist/Cr coated glass mask plates were patterned with the 20 mm laser with 100 Joules. Next the following photoresist was developed in CD-26 solution for 120 seconds. After development, the Cr was etched in Cr wet etchant (CR-14S) with 20% additional time just after visual end point detection. To remove the defect around pattern edge, a descum process was applied for 90 seconds with 400 watts RF power, 10 sccm of oxygen flow, and 150 mTorr pressure. Figure 3-1(a) shows the gate electrode pattern design.

3.1.2. Etch stop mask design

For fabricating channel passivation (CHP) structure for the inverted staggered TFT, an etch stop pattern was designed to protect the channel region in the intrinsic silicon layer. After patterning gate electrode, and depositing gate dielectric layer, intrinsic silicon layer, and etch stop silicon nitride, the etch stop layer is formed on the channel region to protect the channel region during back channel etch of the ohmic contact silicon layer. The targeted thickness of the silicon nitride etch stop layer was between 200 nm and 300 nm with CD loss of 1 µm. For the CHP structure, the active layer of silicon usually has 50nm thickness, as thin active layer thickness has better electrical characteristics. Thus, during back channel etching, targeted etch depth through etch stop layer was ~100 nm. Either wet etching using hydrofluoric (HF) etchant or fluorine based plasma etching such as SF_6, CF_4, or other chemistry requires smooth etching profile to enhance the step coverage since the target thickness of the doped silicon for ohmic contact is 50 nm. The mask fabrication step was the same of gate electrode mask. For alignment, anti-cross marks were patterned to align with cross marks to the gate electrode pattern, and two new two cross marks are patterned for VACNF and S/D anti-cross marks. Additionally, since the

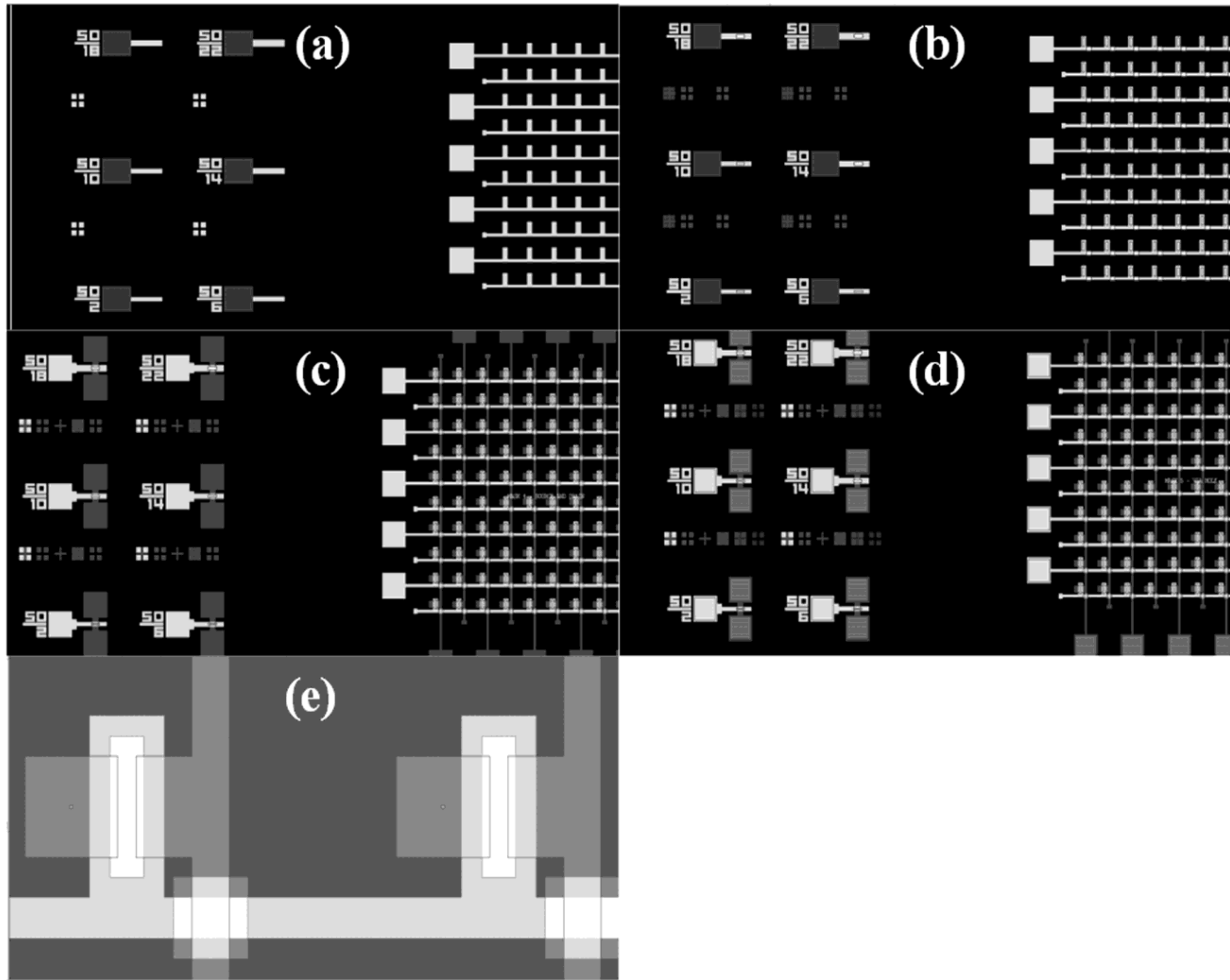


Figure 3-1. Mask design for TFT-VACNF integration; (a) gate electrode, (b) etch stop layer, (c) S/D electrode, (d) via holes, and (e) Ni dot defined on the drain electrode area

CHP structure usually enables an over-etch for the back-channel to disconnect ohmic contact layer on the channel, it results in a very thin gate dielectric layer on the crossover area where the gate line and the S/D line overlapped. This contributes to the leakage current source at 'off' state of TFT. To prevent this gate and S/D short, etch blocking buffer patterns were defined on the crossover area simultaneously when etch stop patterns were defined. Figure 3-1(b) shows the etch stop patterns with etch blocking buffer patterns on the crossover area.

3.1.3. Metal catalysis for VACNF mask design

This initial design for the VACNF integration was to incorporate the fibers onto the drain electrode for sensing and actuating applications. Thus, Ni catalysts need to be patterned on the drain electrode region. Ni dot patterns were defined as 1.0 μm square shapes. To be compatible with DWL 66, the 2 mm laser head was used with 50 Joules energy. Since the ultimate feature size smaller than the specifications of the tool, the tool was optimized to obtain the highest resolution. To get the smallest diameter circular shapes for the Ni dot catalyst, the design, focusing, and energy of laser was manipulated. For the nickel dot mask, the descum process deteriorated the Ni dot shape, thus an accurate development procedure was required. A reduced development time (90 seconds) and reduced Cr etching time was implemented (additional 5 seconds after visual end point detection). Finally, the measured feature size of Ni dots was ~1.6 μm circles. Figure 3-1 (c) shows the design of VACNF catalyst Ni dot mask.

3.1.4. Source and drain mask design

For the source/drain (S/D) electrode masks, the actual channel length and width at the test pads were considered, which defines the channel region as well as line length. Importantly, Cr

has higher resistance than other low resistance metals (Mo, Al, and W). The on/off current ratio and field effect mobility of TFT device will be affected by the channel width and length. Therefore, the channel lengths were designed to be 2, 6, 10, 14, 18, and 22 μm long, and the channel widths were designed between 10 and 100 μm with intervals of 10 μm. The 20x20 active matrix arrays were designed with the channel width and length of 60 μm to 10 μm, respectively. In all, 60 individual transistor devices with different channel width and lengths were patterned on each die. The mask fabrication procedure was the same as the described for the gate electrode mask. The Figure 3-1(d) shows the S/D mask design.

3.1.5. Via hole mask design

To make electrical contact with the gate, source, and drain electrode, via holes need to be defined. During via hole etching the over etch ratio is greater than 50%, since the passivation layer of silicon nitride, active layer of intrinsic silicon, gate dielectric layer of silicon nitride have to be etched away completely to access the gate electrode. This relatively long etch induces significant CD loss. Thus, CD loss for via holes was considered to be 2~3 μm. The fabrication procedure for mask was the same as gate electrode mask. Figure 3-1 (e) shows the via hole mask design.

3.2. Fabrication and characterization of the first thin film transistor process run

The main purpose of this research is the fabrication of intracellular probing device by integrating Vertically Aligned Carbon Nano Fibers (VACNF) and thin film transistors (TFT). The VACNFs on the drain electrode of TFT act as the drain electrode and can be used to penetrate into live cells [15]. For this application, inverted-staggered TFT, bottom gate, structure

was implemented. This structure, however, is slightly more complicated than the staggered TFT, top gate structure since it needs one additional mask step, the etch stop layer and it can be difficult to control the back channel etch depth. Therefore, prior to fabricating the inverted-staggered TFTs, a staggered TFT was considered to optimize each device layer.

3.2.1. Fabrication of the first TFT process run

3.2.1.1. Buffer layer processing

(100) oriented prime grade silicon wafers were used as the starting substrate. For electrical isolation, a silicon dioxide (SiO_2) layer is deposited on each wafer. Before depositing silicon dioxide layer, the curvature of each wafer was measured by Frontier Semiconductor manufacture (FSM), Film stress measurement system so the cumulative stress in the multi-layer TFT device could be measured. The SiO_2 buffer layer was deposited by standard recipe described at table 2-5. 500nm thickness of buffer layer is deposited and the typical stress in the wafer was typically between -170MPa and -190MPa (i.e. compressive).

3.2.1.2. Source and Drain (S/D) electrode processing

For fabricating staggered type TFT; top gate structure, source and drain electrodes were formed as the bottom layer with initial alignment-marks. Chromium (Cr) was used as electrode thin film because Cr has a near zero etch rate in fluorine-based plasma chemistry, which is ideal for the final via hole etch. Initially, the standard Cr deposition recipe was not used since the film stress problems were not recognized; the sputtering conditions were comparable to the standard recipe except that no substrate bias was applied. The chamber base pressure was maintained below 7.5×10^{-8} Torr to reduce the contamination of Cr thin film. The resulting deposition rate

was 5.0nm/min and the sheet resistance (R_s) was 1.25 ohm per square for 150nm thickness. After the deposition of the gate dielectric layer (SiN_x), and amorphous silicon (a-Si), film delamination was observed. From scanning electron image (SEM), the delamination was occurring from the bottom Cr layer. It was expected that a higher tensile stress in Cr layer induce delamination as the other layers were deposited on Cr layer. Therefore, to reduce the initial stress in Cr layer, an additional substrate bias was explored during sputtering. Misra et al. showed that as suitable substrate bias during sputtering could modify the initial stress in Cr thin films from higher tensile stress to lower compressive stress [96]. Approximately 5 watts substrate power during Cr film deposition reduced the residual stress level to below 10 MPa. Otherwise, no substrate powered Cr film shows the 1000MPa tensile stress for 100nm thickness, 1400MPa tensile stress for 150nm, and 2000MPa tensile stress for 200nm thickness. Figure 3-2 show that the resulting residual stress and deposition rate in the Cr layer (150nm) as a function of substrate bias and deposition rate. As shown in Figure 3-2, a higher tensile stress is developed at no bias condition. As the substrate bias increases, the stress in Cr thin film decreased and saturated around 10 watts with -350MPa (compressive). As the substrate power increases, the density of the Cr film increases due to the potential drop and subsequent ion bombardment at the substrate. Consequently, the deposition rate was reduced and the inter-atomic distance among the Cr atoms was reduced, which results to the compressive stress evolution. Therefore, after certain power (from figure 3-2; 10 watts (100 volt)), the stress level was saturated while the deposition rate was still reduced. At higher substrate power, re-sputtering processes likely contributed to the decreased deposition rate. There is negligible change in the sheet resistance of Cr thin film with the substrate bias, therefore, 5 watts power (50 volt) substrate power was applied to Cr deposition condition to reduce the initial stress in the Cr film which caused failure during

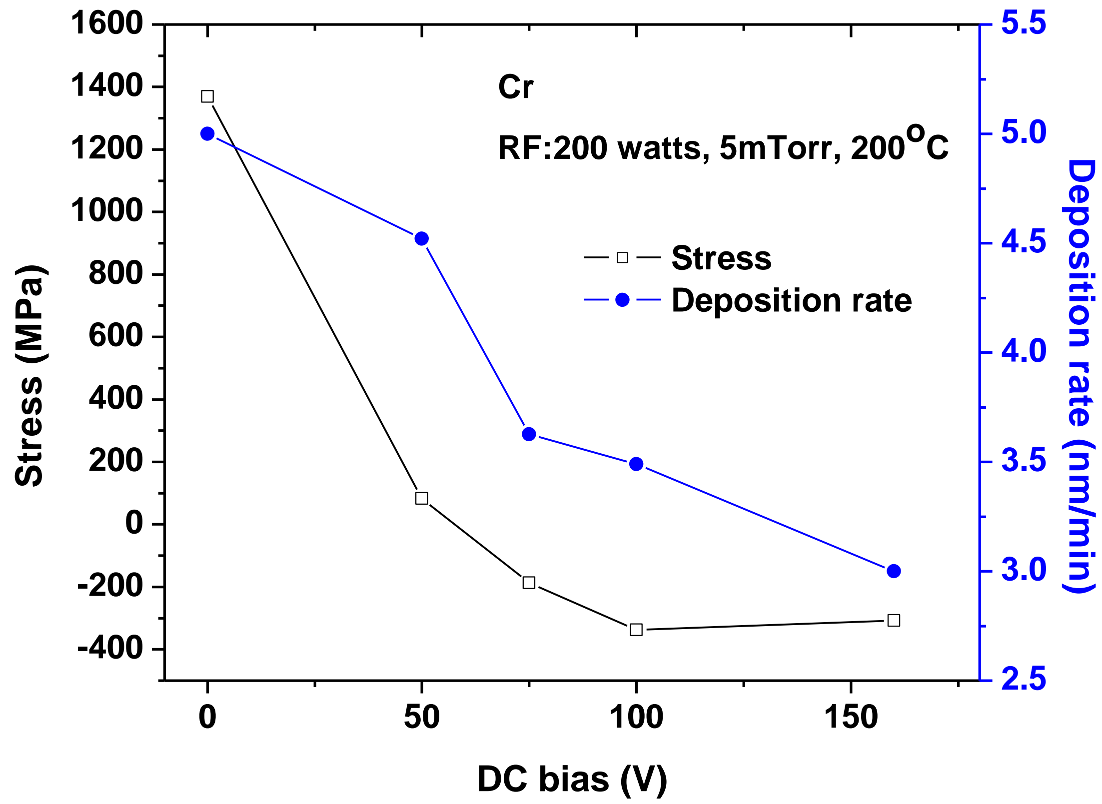


Figure 3-2. The stress and deposition rate of Chromium (Cr) thin film by RF magnetron sputtering as a function of substrate bias (V)

subsequent processing. All subsequent Cr electrode sputter deposition used the 5 Watt substrate biased Cr film deposition recipe as the standard process.

3.2.1.3. n-type doped silicon processing

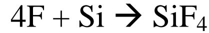
A 99.999% pure n-type (phosphorus) doped silicon target was used for sputtering. The standard n^+ Si deposition condition was used with Ar and Ar-H_2 gas flowing. From figure 2-36, pure Ar gas deposition shows the lower resistivity in the film and lower residual stress at 50nm thickness than Ar-5%H_2 gas used. The deposition rate of both conditions was nearly same of 1.8nm/min. Therefore, for good ohmic contact characteristics, pure Ar gas was used to fabricate TFTs. The resulting resistivity was nominally 1.44 ohm-cm. The residual stress of 50nm thin film was -130MPa. Furthermore, Ar-5%H_2 gas used n^+ Si layer has an undesirable dehydrogenation during gate dielectric layer and passivation layer deposition of silicon nitride. Since the deposition temperature for the silicon nitride layer was between 350°C and 400°C, bubbles were formed on the n^+ Si patterned sites. These hydrogen bubbles can be a leakage current source during device operations.

3.2.1.4. Doped amorphous silicon and source and drain (S/D) electrode patterning

Plasma etching of materials is commonly done by free radicals. Free radicals are electrically neutral species that have incomplete bonding. For example the electron induced reaction for sulfur hexafluoride is given by:

$$e- + SF_6 \rightarrow SF_5 + F + e-$$

In such plasma, SF_6 or CF_4 produce F radicals for the chemical etching of silicon forming violating products, such as SiF_4 which are easily removed from the surface.



$4F + Si \rightarrow SiF_4$

For patterning of n^+ Si and source-drain electrode, the standard photolithography process was used with 4.6 seconds exposure time. After patterning the photoresist, an Oxford Plasma lab RIE was used to etch n^+ Si film based using a SF_6 plasma chemistry since CF_4 based etch chemistry can produce carbon based byproducts through polymerization. The dry etch condition for the 50nm n^+ amorphous silicon was 30 watts RF power, 2000 watts inductive coupled plasma (ICP) power, and 10mTorr pressure, 15°C temperature. The nominal etch rate of this condition is 7.5nm/sec. For complete etching of the n-type doped silicon, a 20% over etch time was applied since the underlying Cr has a near zero etch rate under these etching conditions. The etching of Chromium was done via wet etching using CR-14S Chrome wet etchant. For 150nm Cr S/D etching, 130 seconds etching time was required.

3.2.1.5. Hydrogenated amorphous silicon (a-Si:H) processing

The active layer of intrinsic silicon can be deposited by sputtering, Low Pressure Chemical Vapor Deposition (LPCVD), and Plasma Enhanced Chemical Vapor Deposition (PECVD). For TFT application, PECVD system was choose because contamination from sputtering chamber and the unreliable availability of the LPCVD system. Furthermore, to reduce the contamination in sequential deposition without breaking vacuum for the gate dielectric silicon nitride and active layer intrinsic silicon could be accomplished in the PECVD. This has the benefit of reducing a main source of the leakage current in TFT operation [46].

Hydrogenated amorphous silicon (a-Si:H) active layers were deposited by PECVD and Silane (SiH_4) gas was the source gas. Thus, inevitably hydrogen was incorporated in the a-Si network, which passivates dangling bonds in the bulk region and interface, and reduces the

leakage current and enhances the field effect mobility in the TFTs. The deposition condition was 10 watts RF power, 1000 mTorr pressure, 350°C temperature, and 500 sccm flow rate of 5%SiH_4-Ar. The thickness of the amorphous silicon active layer was nominally 300nm. The goodness of fitness (GOF) of the reflectance data was greater than 90% using ultra-violet (UV) thin film analyzer, therefore the 1000mTorr recipe was used to deposit a-Si. Figure 2-15 shows the pressure effects of a-Si deposited by PECVD. Even though the deposition rate from higher pressure conditions was higher than the 1000mTorr results, the poor uniformity (>20% non-uniformity) prevented its use for the active layer. Additionally, the measured residual stress value of 300nm thickness a-Si:H was between -150 MPa and -200 MPa. This stress value was appropriate since the adjacent silicon nitride and gate metal layer usually has a tensile stress. Therefore, accumulated stress in the TFT should be minimized.

3.2.1.6. Gate dielectric (Silicon nitride) processing

For amorphous silicon based TFTs, silicon nitride (SiN_x) films were usually used as gate dielectric layer. Though the higher interface density of state between SiN_x and amorphous silicon can degrade the device characteristics, the dielectric constant of SiN_x ($k_{SiN_x} = 7.5$) is two times higher than that of SiO_2 ($k_{SiO_2} = 3.7$) allow it to be used as a gate dielectric film of a-Si TFT. The processing of SiN_x as gate dielectric layer will be focused on and the details of various processes are described below.

Deposited films of silicon nitride dielectric layers are capacitively coupled to the active region for TFT operation, as the channel is generated or degenerated by induced charges from the gate electrode. In the ideal case, no gate current is directly allowed to flow at the channel, but,

the current between source and drain is flowed by an induced charge build up from gate bias. Therefore, high electrical breakdown strength, and higher capacitance (dielectric constant) are required for the dielectric layer. Low breakdown strength cause high gate currents from the gate electrode, and inhibits charges build-up in the channel region. Prior to fabricate gate dielectric films, several studies were performed to investigate PECVD silicon nitride films and SiH_4 and NH_3 gases were used.

The deposition condition of PECVD SiN_x film was initially 20 Watts RF power, 1200 mTorr pressure, 5%SiH_4-Ar/NH_3 (30/200 sccm) gas flow, and 300^oC temperature. The deposition rate was 0.48nm/sec, and reflective index value was 2.0. 200nm thickness of SiN_x films was prepared as described in chapter 2. With reasonable breakdown strength and capacitance, initially the TFTs were fabricated and subsequently failed due to thin film delamination. From residual stress measurements, the silicon nitride film exhibited ~ +300 MPa tensile stress. To reduce the residual stress in the silicon nitride, a low stress silicon nitride recipe was developed for PECVD system. To decrease stress, N_2 gas was added, the temperature was increased, and the pressure was reduced with various flow rates of NH_3 gas. [59-60]
The deposition condition for low stress SiN_x were 40 Watts RF power, 600mTorr pressure, 5%SiH_4-Ar/NH_3/N_2 (150/2/790 sccm) gas flow rate, and 400^oC temperature and the resulting low stress silicon nitride shows the refractive index value of ~2.10, indicating a silicon rich silicon nitride with high density film. Figure 2-13 shows the residual stress of the silicon nitride and figure 2-14 (a) shows the capacitance of low stress silicon nitride film. Additionally, figure 2-14(b) shows the capacitance of annealed silicon nitride film. Since 400^oC temperature and 30min procedure is used during the passivation silicon nitride, the same temperature and annealing time was applied. This low stress silicon nitride process deposited by PECVD was

subsequently used as the gate dielectric because it has a higher breakdown strength, low flat band voltage shift and low threshold voltage characteristics with minimized residual stress.

3.2.1.7. Gate electrode processing

Chromium (Cr) is used as gate electrode thin films. The deposition condition was the same of Source and Drain electrode processing. The thickness of source and drain electrode was 200nm. The residual stress of source and drain Cr film was negligible when the optimized 5 watts substrate power was applied during Cr film deposition. The etching procedure was also the same as the gate electrode processing.

3.2.1.8. Passivation layer deposition and contact via holes for Gate and Source/Drain pads

Low stress silicon rich silicon nitride (Si-rich SiN_x) thin films were used to passivate the final device. The standard low stress SiN_x recipe was used and the thickness of the passivation layer was 300nm. For patterning the via hole, the standard photolithography process was used with 4.6 seconds of exposure time. For via hole etching, the Oxford RIE system was used. Initially, to etch the passivation layer of SiN_x, a C_4F_8, and O_2 gas mixture was used. The etch condition was 200 watts RF power, 2000 watts ICP power, C_4F_8/O_2 (45/2 sccm) gas ratio, 7mTorr pressure, 15^0C temperature (recipe name was OPT-SiO_2 and Si_3N_4). The measured etch rate was 3 nm/sec with the photoresist pattern, thus to etch 300nm thickness of passivation films, 150 seconds etch time was applied assuming a with 50% of over etch. Next, to etch the active layer of amorphous silicon, 20 watts RF power, 750 watts ICP power, $C_4F_8/SF_6/Ar$ (27/12/2 sccm) gas, 10 mTorr, 15^oC temperature was used for the recipe for 300nm thickness of amorphous silicon (recipe name - OPT-shallow Si etch). The etch rate of a-Si was nominally 1

nm/sec, for etching 300nm thickness, 450 seconds etch time was applied, assuming a 50% over etch. Finally, the same etch condition of passivation layer was used again to etch gate dielectric SiN_x of 200nm thickness. A 20% over-etch time was applied to etch completely.

3.2.2. Characterization of the first TFT process run

3.2.2.1. Accumulated stress of TFT device

To characterize the stress effects of each thin film, the stress was measured after each layer was processed and is shown in Figure 3-3. Figure 3-3 shows the overall stress change for two wafers: one sputter deposited n^+ Si with pure Ar and one n^+ Si layer sputter deposited with Ar-5%H_2 gas. From this figure, the optimized film layers decrease the overall stress of the completed TFT is approximately -100MPa (compressive).

3.2.2.2. Electrical characteristics of TFT device

From the first fabricated TFT run, however, no drain current-gate voltage (I_{ds}-V_g) electrical characteristics were acquired. During I_{ds}-V_g measurements, contact between the Source and Drain electrode and the probe tip did not show the good electrical contact properties. This suggested that the via etching procedure was insufficient or a residue was left on the electrode pads; likely due to polymerization during the fluorocarbon etching. Initially, an over etch time was applied using same etching conditions, but, the thickness of photoresist was too thin (1.75um) and the photoresist was fully etched away during the additional 150 seconds of via hole etching. Thus the entire passivation and active layers were etched away.

To inhibit the polymerization during the TFT etching, only SF_6 gas etching process was used to etch passivation, active layer of amorphous silicon, and gate dielectrics in situ. The etch

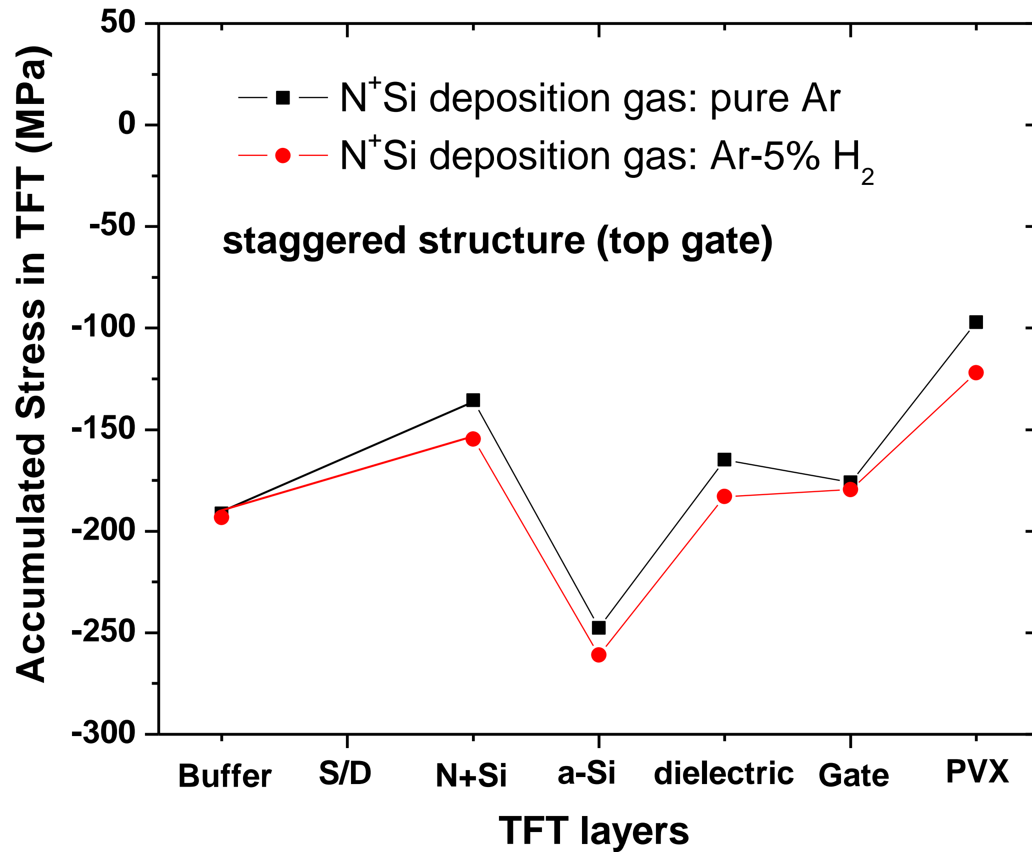


Figure 3-3. The overall stress TFTs as a function of each thin film layer for sputter deposited n^+ Si layer with pure Ar and Ar-5% H_2 gas films

condition that was developed was 30 watts RF power, 2000 watts ICP power, SF_6 (45 sccm) gas, 10 mTorr, 15°C temperature. The etch rate was different for each thin film material; 10 nm/sec for amorphous silicon; and roughly 7.5 nm/sec for low stress SiN_x. Totally, 180 seconds etch time was applied. In this case, the photoresist on the top survived. After etching, photoresist stripping process was done in photoresist stripper for 30 minutes and a 60 seconds of descum procedure was applied to remove the photoresist residues.

From the second via hole etch conditions, I_{ds}-V_g characteristics were measured and again electrical contact between the source/drain pads and the tip of probe was not good. Inspection revealed that the vias were not fully etched and it was determined that the photoresist was underdeveloped. The development problem was determined to be degradation of the illumination power density from the light bulb in the contact aligner. Figure 3-4 shows the illumination power density as a function of time (days). From this figure, the exposure time had to be increased 30% from 4.6 seconds to 6 seconds. It was expected that the residue from the underdeveloped pattern caused the via etch problem. Of the several test pads tested, only one pad showed the I_{ds}-V_g characteristics are shown in figure 3-5 when V_{ds} was at 5.0 Volt. The measured pattern was 40μm of width and 18μm of length. Capacitance per unit area is 2.08×10^{-9} F/cm^2 and threshold voltage is around 6 volt. The device has a lot of leakage drain current in the 'off' state between 10^{-11} and 10^{-10}ampere. However, it shows a relatively high 'on' current around 10^{-6}.

In the saturation region, using the definition of drain current, field effect mobility can be calculated from this equation,

$$I_D = \frac{1}{2}\frac{W}{L}\mu C_i (V_G - V_T)^2$$

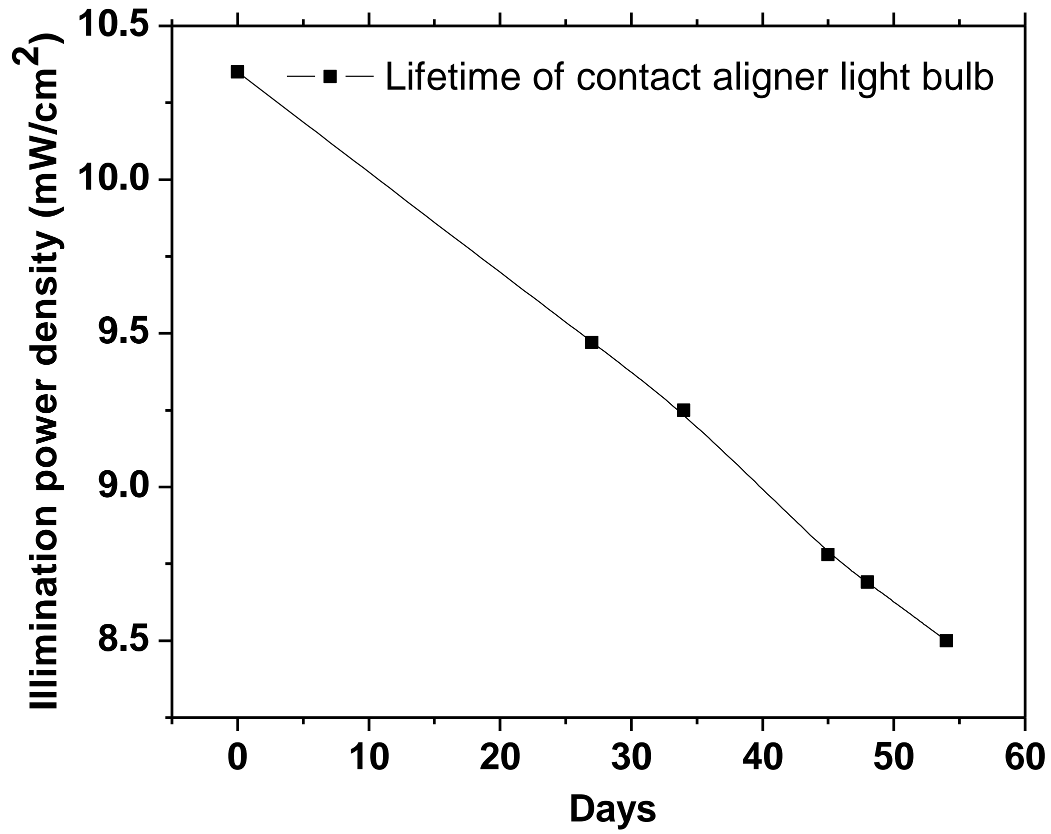


Figure 3-4. The illumination power density of the contact aligner bulb as a function of time (days).

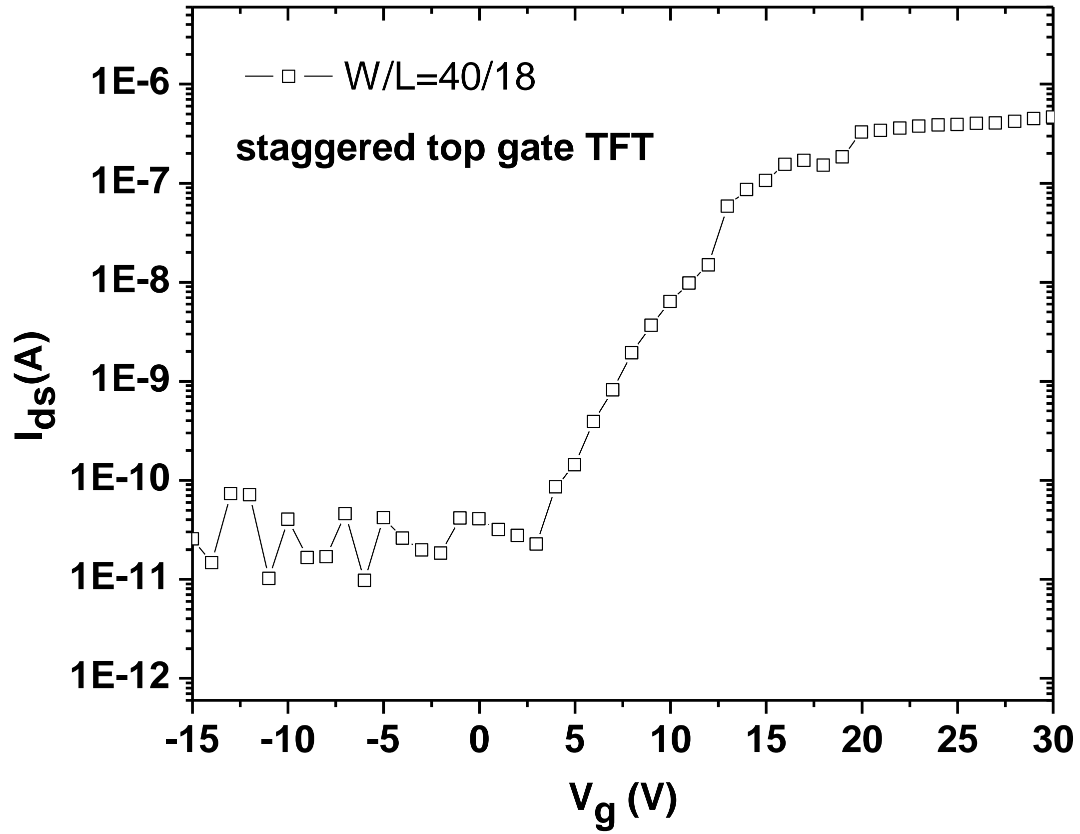


Figure 3-5. The I_{ds}-V_g electrical characteristics of staggered TFT (1st Run)

Where, I_D is drain current, W is channel width, L is channel length,μ is field effect mobility, C_i is capacitance per unit area, V_g is gate voltage, and V_T is threshold voltage.

The staggered TFT had the following electrical characteristics: 0.228 ~ 0.315 cm^2/Vsec field effect mobility, and the on/off current ratio is between 10^4 and 10^5. From Figure 3-6 transconductance (g_m) of the TFT is shown. It has a reasonable g_m value at V_g=20 V, however, between 10 and 20 gate voltage, there are fluctuations in the transconductance graph, indicating contamination or bad interface profile.

3.3. Fabrication and characterization of the second thin film transistor process run

Previously staggered top gate Thin Film Transistors (TFTs) are fabricated to optimize the characteristics of each layer. To integrate Vertically Aligned Carbon Nano Fibers (VACNFs) an inverted staggered bottom gate thin film transistor, channel passivation (CHP-TFT) structures were fabricated to measure the transistor characteristics by using the thin film materials processes developed for the staggered TFT characterization.

3.3.1. Fabrication of the second TFT process run

3.3.1.1. Buffer layer processing

The standard buffer SiO_2 deposition process was used to deposit 500nm thickness on (100) oriented prime grade silicon wafers.

3.3.1.2. Gate electrode processing

For fabricating inverted staggered type TFT; bottom gate structure, the gate electrode is formed at the bottom layer with first alignment marks. Chromium (Cr) was used as electrode

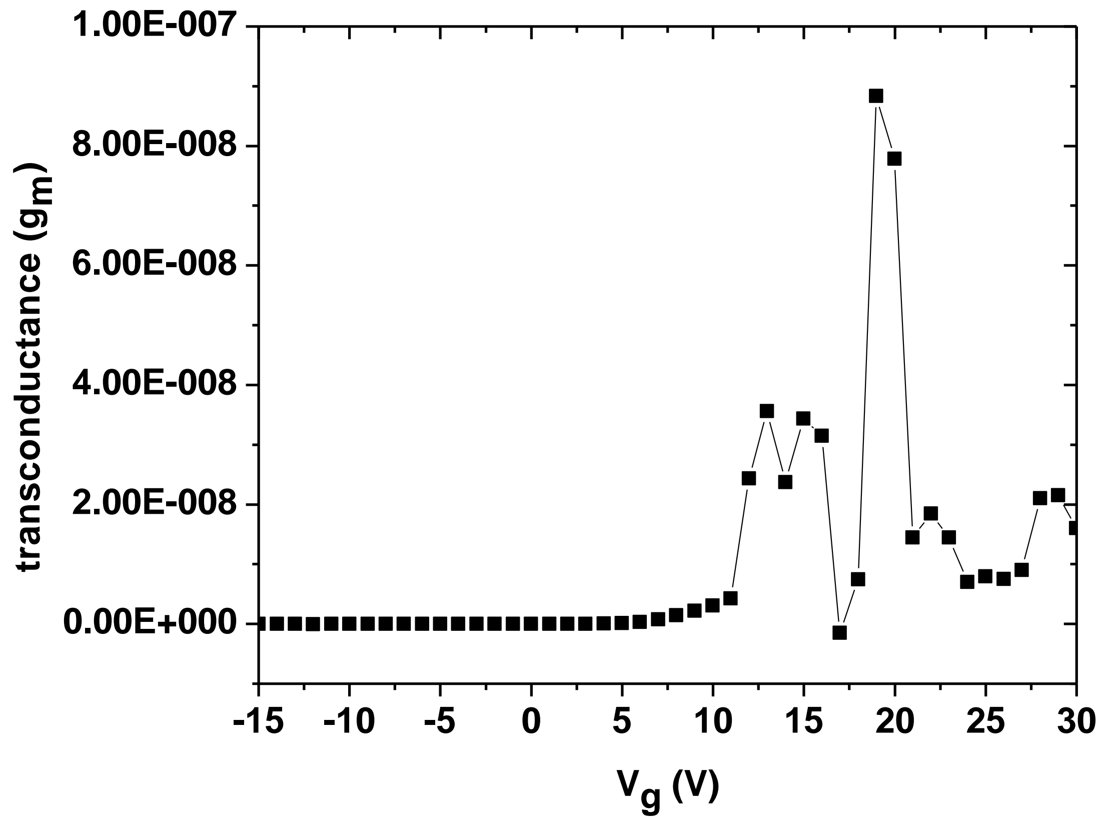


Figure 3-6. Transconductance of staggered TFT (1st Run)

metal and deposited by the standard low stress Cr deposition process. Since a new Cr target was inserted, the deposition rate was initially 5.2nm/min at first time, however, after 3 hour of sputtering, the deposition rate was stabilized to 4nm/min and the measured sheet resistance (R_s) was 1.25 ohm per square centimeters for 150nm thickness. Previous results showed that 5 watts substrate power has 50 volts of substrate voltage and has 50MPa tensile stress at 150nm thickness, however, for the new Cr target, at the same substrate power of 5 watts, 100 volts was observed. Fortunately, the measured stress of 150nm thickness Cr film was -50MPa compressive stress. Though the stress term was changed slightly, it still had a low enough stress level. Therefore, the same deposition condition for Cr was used for fabricating the IS-TFT.

For patterning the gate electrode, the standard photolithography process was used with a resist pre-bake was done at 115°C for 90 seconds and 6 seconds exposure time. Due to continuous decrease of illumination power density of light bulb, every photo lithography exposure time was adjusted to compensate for the power density of the bulb which changed with time. The wet etching of Cr was done by CR14S wet etchant for 90 seconds at room temperature. The additional 5 seconds etching was applied to achieve a good taper angle.

3.3.1.3. Active layer processing

To reduce the interface defect density between the gate dielectric layer and amorphous silicon, the gate dielectric and active layers were deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) in situ. The main issues for these steps was that the low stress SiN_x was deposited at 400°C temperature, but a-Si:H was deposited at 350°C temperature. Changing temperature may generate flakes from the chamber wall due to the difference of thermal coefficients of expansion of these two materials, and these flakes can be deposited on the wafer.

Therefore, a low stress SiN_x of 350°C temperature was developed. All deposition conditions were the same as the standard low stress SiN_x except the temperature. Fortunately capacitance and breakdown strength characteristics were the nearly same of initial low stress SiN_x. To characterize the stress properties of PECVD SiN_x films, residual stress was measured at 300nm thickness. The residual stress value was -16.09MPa and the refractive index value was 2.06. This 350°C low stress SiN_x deposition condition will henceforth be considered as the standard silicon nitride deposition process condition. Kuo et al. has reported that better transfer characteristics of TFT were acquired by using a graded gate SiN_x structure, which had the bulk SiN_x deposited at a high rate and the interface SiN_x deposited at a lower rate [46]. These optimized characteristics were due to a lower interface density between a-Si:H layer and SiN_x layer. Therefore, to reduce the interface density, 250nm thickness of lower density SiN_x were deposited above patterned gate electrode followed by 50nm thickness of high density SiN_x to be contact with a-Si:H film. Simply high density SiN_x was deposited by reducing the RF power from 40 watts to 20 watts. Two different gate dielectric layers were prepared to compare I_{ds}-V_g characteristics. The following post fabrication processes were the same for these two different gate dielectric layers.

a-Si:H film was deposited as active layer. The standard deposition condition was used and the thickness of a-Si:H was reduced to 50nm. For inverted staggered TFT, as the thickness of active layer decrease until sustaining continuity of the active layer, a good transistor characteristic is achieved. However, when the a-Si:H film is too thin, the field effect mobility decreases abruptly if the silicon layer is not continuous [46,97]. Since the thin channel is formed, the effective ohmic contact region easily overlapped the channel. At the channel region thins, there is more possibility of electrons directly flowing through the source and drain electrode via the overlapped ohmic contact region rather than the thick active layer in the on-state under a

given gate voltage. Otherwise lower leakage current at off-state is also achieved because the leakage current is related to hole injection from the drain area, which is inversely proportional to the film thickness [97]. Additionally, the photosensitivity of a-Si:H is controlled by the concentration of electron-hole pair generation under illumination, which is directly related to the film thickness [46].

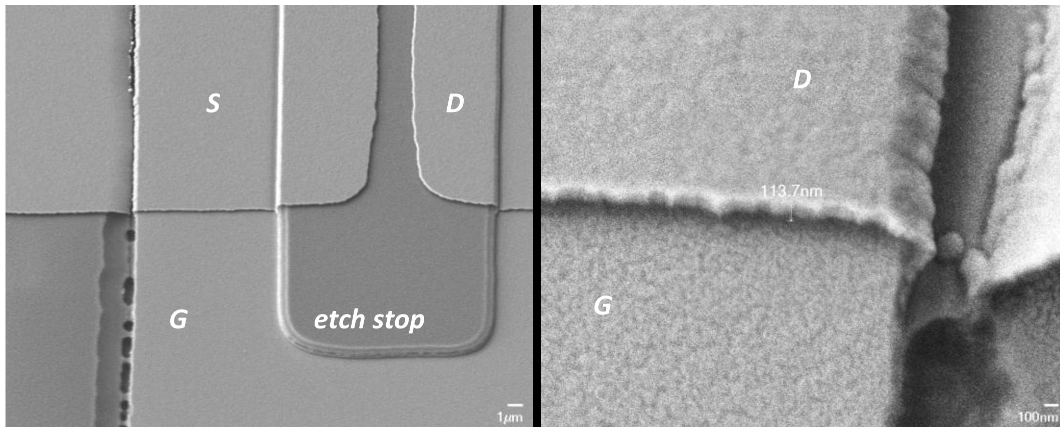
3.3.1.4. Etch Stop Layer (ESL) processing

Etch stop layers are not a mandatory layer for inverted staggered TFT. Due to the difficulty of the back channel etch, however, etch stop layer are widely used for CHP-TFT. Accurate control of the etch depth of n^+ Si and a-Si:H is the critical parameter to optimize the transfer characteristics of inverted staggered TFT. To obtain better I_{ds}-V_g characteristics, it requires two factors. First, the complete etch of n^+ Si is required as any n^+ Si residues can produce a conductive layer and result in diode characteristics between the source and drain. Another factor is to keep the proper a-Si:H channel layer thickness during back channel etching since fluorine based gas plasma for n^+ Si etching also attacks the a-Si:H film. Though thinner a-Si:H film thickness results a good transfer characteristic as mentioned previously, the ion damage during plasma etching also can degrade the characteristic [51]. Thus, for back channel etching processing, there is an optimized etch depth to compensate the thickness of a-Si:H and ion damage during etching. To avoid the difficulty of back channel etch, a silicon nitride etch stop layer was deposited between a-Si:H film and n^+ Si film to passivate the channel region and to reduce the a-Si:H thickness. Usually, SiN_x is used for etch stop layer and patterned by buffered oxide etchant (BOE) since the selectivity of SiN_x to amorphous Si in BOE is very high

[98-99]. After depositing the etch stop layer of SiN_x, it was patterned on the channel region with an extra 1µm at each side.

A 350°C deposited low stress SiN_x was used for etch stop layer, which was deposited onto a-Si:H layer with 300nm thickness. It was patterned with the standard photolithography process flow. During wet etching by BOE 10:1 (ratio of de-ionized water and hydrofluoric (HF) is 10 to 1), the 300nm etch stop SiN_x layer was not etched during a 30 minutes etch time. Thus, the SiN_x etch stop layer was etched by higher fluorine concentration BOE 6:1. However, the results were the same. Finally, 49% HF was used and etch stop SiN_x layer was completely etched in 5 minutes. The slow etch rate was attributed to the silicon nitride being silicon rich. The higher fluorine concentration HF, however, significant undercut the resist and the etch stop photoresist patterns were fully lifted-off. Thus, the measured thickness of etch stop layer SiN_x was reduced from 300nm to 200nm. The most important deleterious effect that the high concentration HF etch has was that it attacked both the a-Si:H film and gate dielectric SiN_x. Figure 3-7 shows scanning electron microscope (SEM) images of step coverage on etch stop layer patterns and gate electrode patterns. These images were taken after back channel etching due to the charging effects from SiN_x during electron imaging. From figure 3-7, it is clear that the wet etch attacked the gate patterned region, where the a-Si:H film and gate dielectric SiN_x film has covered the step.

Another candidate to etch the etch stop SiN_x layer with good etching profile was to use RIE with SF_6 plasma gas chemistry. The dry etch condition that was developed utilized 30 watts RF power, 2000 watts Inductive coupled plasma (ICP), SF_6 (45 sccm), 10mTorr pressure, and 15°C temperature. During the RIE etching tests, two problems were encountered. The first was that it is difficult to etch SiN_x selectively to a-Si:H film. The second problem was that the taper



(a) (b)

Figure 3-7. The SEM image TFTs after back channel etch with 49% HF used to etch the etch stop layer; (a) step coverage on the etch stop layer SiN_x pattern and (b) high resolution image of the gate electrode pattern

angle for the next n^+ Si ohmic contact layer was steep, since RIE usually results in an anisotropic etch profile. Therefore, to compensate the effects a two step etching (dry + wet etch) was applied to achieve the complete etch of etch stop layer and reduce the taper angle. Initially, 250nm thickness etch depth was achieved using a 25 seconds etch with the conditions described above. Secondly, the 49% HF based wet etching solution was applied for 60 seconds to achieve a good taper angle. Although minor undercutting effects were generated, this process was used. The final etching results were determined by observing the wettability of the TFTs surface since amorphous silicon is hydrophobic and silicon nitride is hydrophilic. Figure 3-8 shows the SEM image of etch stop patterns on TFTs patterned with two step etching process.

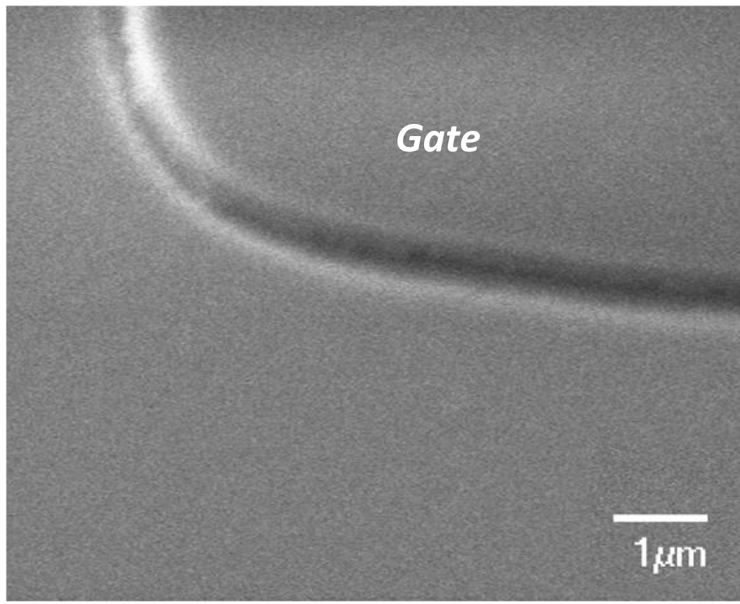


Figure 3-8. The SEM image of etch stop layer pattern with two step etching

3.3.1.5. n^+ Si & Source and Drain electrode deposition

The standard n^+ Si deposition condition was used to deposit 50nm thickness. Since the new n^+ Si target was put into the sputter system, the deposition rate was increased slightly during the initial sputtering runs. The first measured deposition rate was 1.5nm/min, which achieved a 50nm thickness in 33minutes. The thickness of actual n^+ Si film, however, measured by profiler and SEM images was 30nm thickness. The deposition rate was reduced to 1.0nm/min due to the target seasoning. Next, Chromium was deposited on to the n^+ Si. The standard deposition condition was used to achieve 200nm thickness.

3.3.1.6. Source/drain and back channel etching (BCE) process

Back channel etching is the most important processes for transistor characteristics. With the help of etch stop layer, the complete etch of doped silicon layer has much more process latitude. The target etch depth was 80nm, 30nm of doped silicon and 50nm of etch stop layer. For patterning of gate electrode, the standard photolithography process was used with an increased pre-bake time of 120 seconds.

For n-type doped silicon etching and the SiN_x etch stop etching, an SF_6 plasma chemistry was used. The dry etch condition for 30nm etch was that 30 watts RF power, 2000 watts Inductive coupled plasma(ICP), and 10 mTorr pressure, 15^oC temperature. The etch rate for this condition was 10nm/sec for the silicon and for the etch stop SiN_x layer was 7.5nm/sec. Therefore, 10 seconds etch time was applied which includes a 20% over etch for the SiN_x layer. Figure 3-9 shows the channel region after the back channel etching. The measured etch result was 30nm of doped silicon and 75nm for the etch stop layer.

3.3.1.7. Passivation layer deposition and via hole etching

The standard SiN_x thin film (300nm) was also used to passivate the finished devices. Previously, for patterning of via hole etching, the standard photolithography process was used and results in 1.75 μm thickness photoresist, which was insufficient to withstand the entire via etch. Therefore, a new thicker photoresist was used; SPR™ 220-3.0 photoresist was used with 1500 rpm spinning speed during 60 seconds which resulted in a thickness of 3.20 μm. Other lithography processes were the same as the standard process. For via hole etching, the target etch depth was 300nm for the source and drain electrode contact (passivation layer), and 650nm for

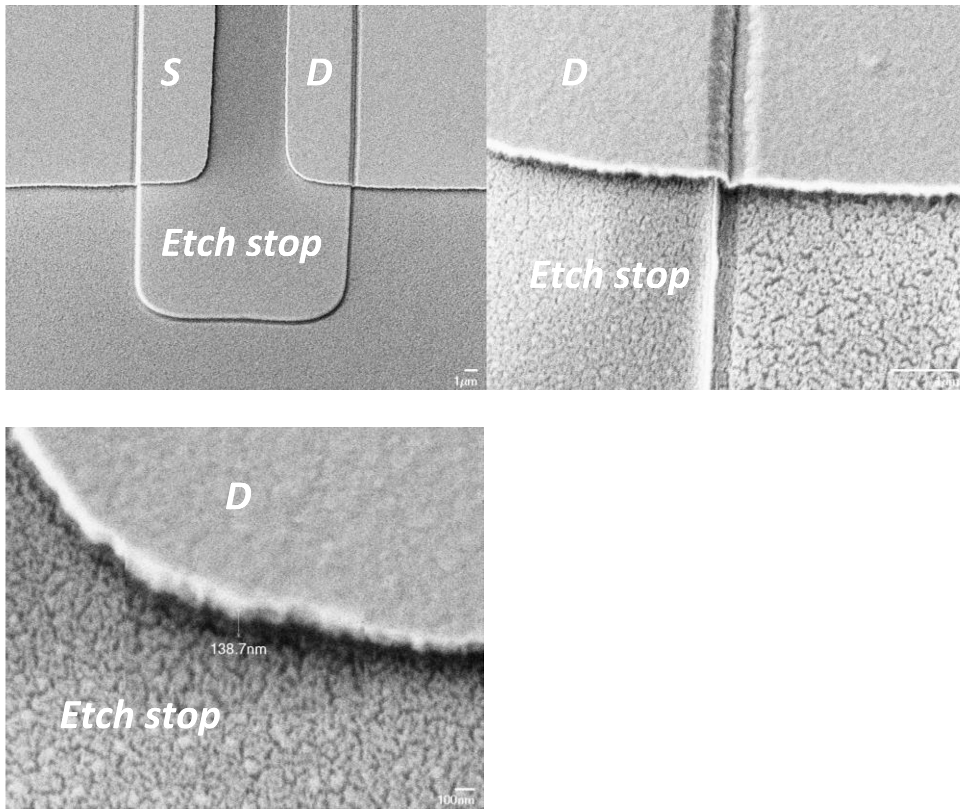


Figure 3-9. The SEM images of back channel etched TFTs and step coverage on etch stop layer pattern

gate electrode contact (etching passivation, a-Si:H, and gate dielectric film). The etching condition was that 30 watts RF power, 2000 watts ICP power, SF_6/Ar(45/1 sccm) gas, 10 mTorr, 15°C temperature. Using the previously determined etch rates of 10nm/sec for a-Si:H film and 7.5nm/sec for SiN_x a 90 seconds etching time was required and applying a 100% over-etch, 180 seconds etching time was applied to ensure the contact between the contact pads and the end of probe tips. Inspection confirmed that the thicker photoresist survived. Figure 3-10 shows the bottom gate electrode scanning electron images tilted 30° degree after via hole etching.

3.3.2. Characterization of the second TFT process run

I_{ds}-V_g transfer characteristics were measured using a Signatone probe station with HP semiconductor analyzer at Oak Ridge National Laboratory (ORNL). Three wafers were initially prepared to measure the I_{ds}-V_g characteristics. The first one had the etch stop layer which was etched by wet HF etchant only. The second one had the etch stop layer etched by dry plasma etch only. Finally the third wafer had the back channel etched via the two step etching process. The first and second wafers did not show the I_{ds}-V_g transfer characteristics. During the etch stop layer etching, the gate Cr line and a-Si:H layer appeared to be attacked, which disconnected the layer just above the channel region. The two step etch stop layer etch wafer also did not show good I_{ds}-V_g transfer characteristics. Though almost TFT test pads were not working, a few pads were seems survived. Initially, the failure of adjusting exposure time of photo lithography work made underexposed the gate line patterns leading to non-uniform etching and poor etching profile of gate Cr electrodes (as revealed by SEM imaging). The poor step coverage at the gate lines, caused the stacked layers to be disconnected. However, measured I_{ds}-V_g transfer characteristics are shown in Figure 3-11. As shown in the Figure, though On-state current is very low, the

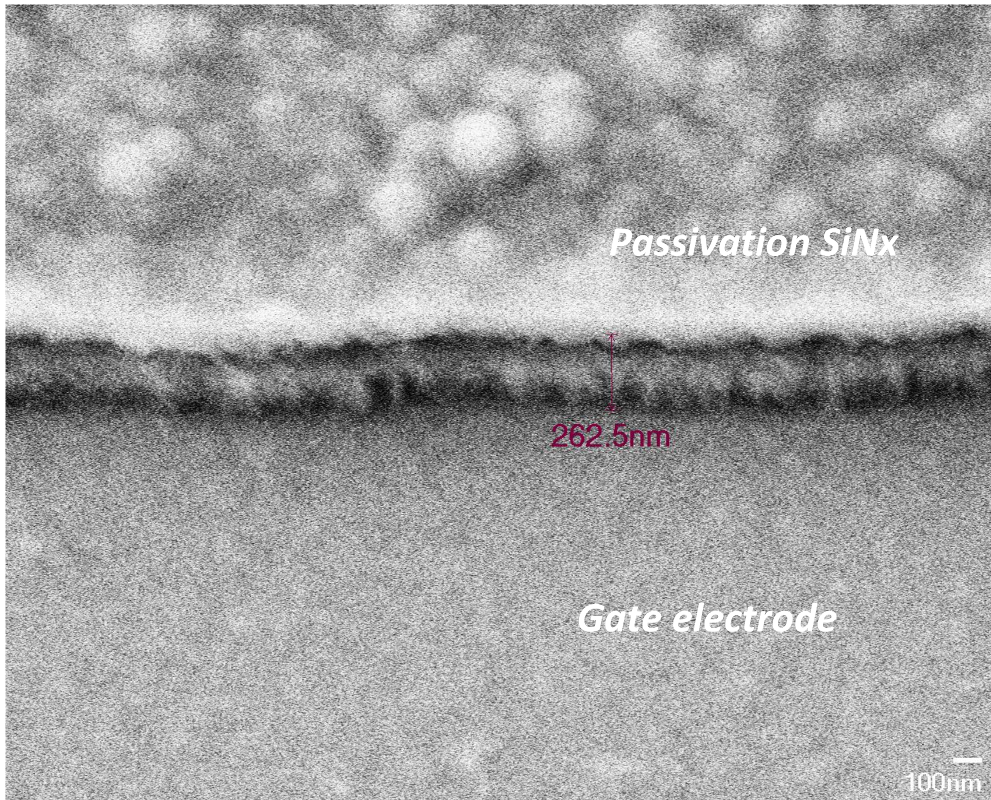


Figure 3-10. The SEM image of gate electrode exposed after via hole etch

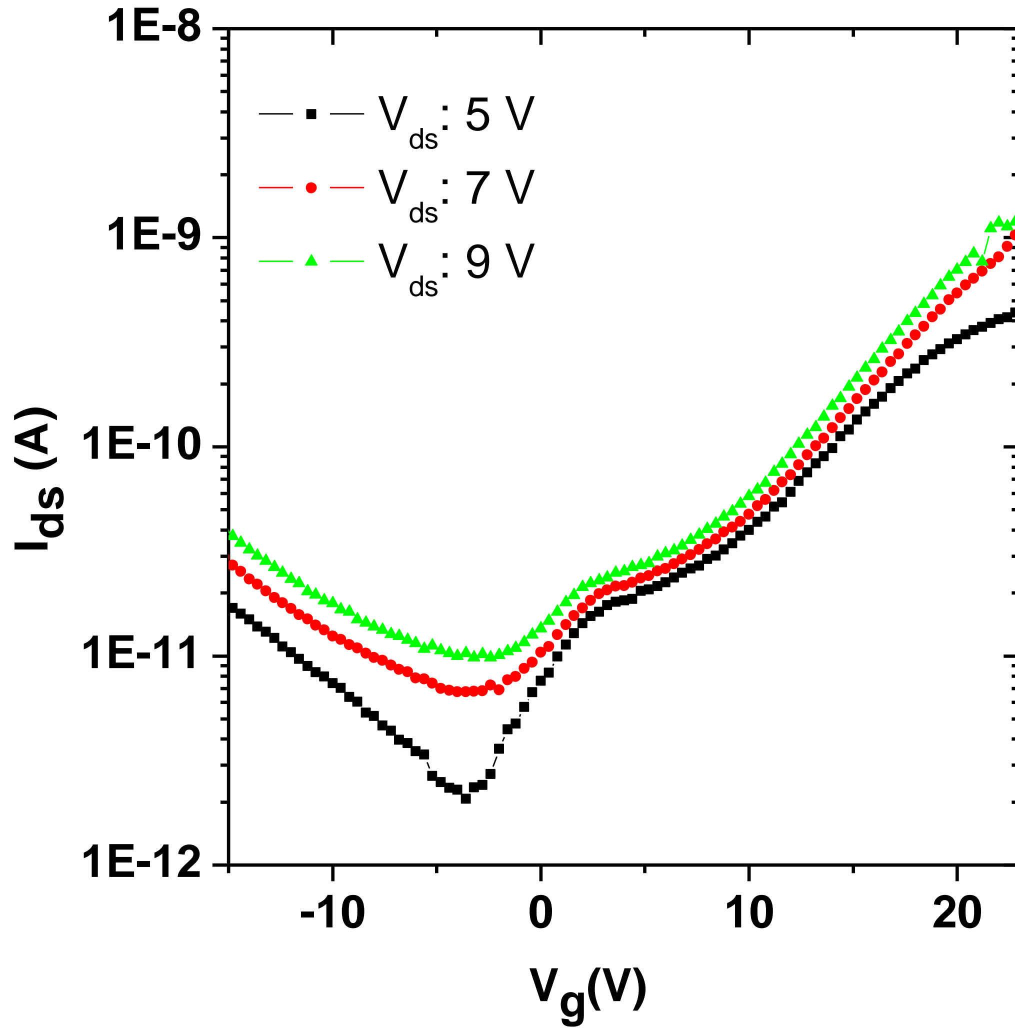


Figure 3-11. Current-Voltage characteristics of 2nd Run inverted staggered channel passivation TFT device with two step etch stop layer etching process

leakage current level is between 10^{-12} when V_{ds}=5 volt and 10^{-11} when V_{ds}=7 volt at V_g= -5 Volt, which indicates the anomalous leakage current behavior similar to poly-Si TFTs. For instance, when the negative gate voltage magnitude is increased, the drain-source current was increased proportionally. It is pointed out that there is a lot of contamination during processing, which are attributed to several sources such as interface states, band gap state, Fermi energy level states, back channel surface, and etch stop layer interface with a-Si:H film. Kuo et al. reported that the CHP-TFT may show these anomalous leakage current behavior due to the poor interface between a-Si:H film and etch stop layer SiN_x, which acts as a trapping site for electrons [46]. However, the main issue was that transfer characteristics curves have a kink in the current at above from V_g= 4 Volt while the threshold voltage (V_{th}) was measured around -4 Volt for all three different V_{ds}.

The kink was determined to be due to contamination in the n^+ silicon ohmic contact layer which had a higher resistivity (0.7 x 10^9 Ohms) than the channel region in the on-state. This resistance correlated well with the slope of the curve in this region (2.0 x 10^9 Ohms). Thus, the contact resistance at source and drain limited the current at higher voltages rather than the channel resistance.

3.4. Fabrication and characterization of the third thin film transistor process run

From 2nd Run of Inverted Staggered CHP-TFT fabrication (3rd overall), the etch stop layer process was developed and it was determined that the photoresist residues can block the etch and ultimately act as a leakage current source. Additionally, the high resistivity of the doped silicon film was considered to the reason of low on/off current ratio. Herein, to reduce the

contamination and improve the step coverage, a modified fabrication process was introduced and is discussed below.

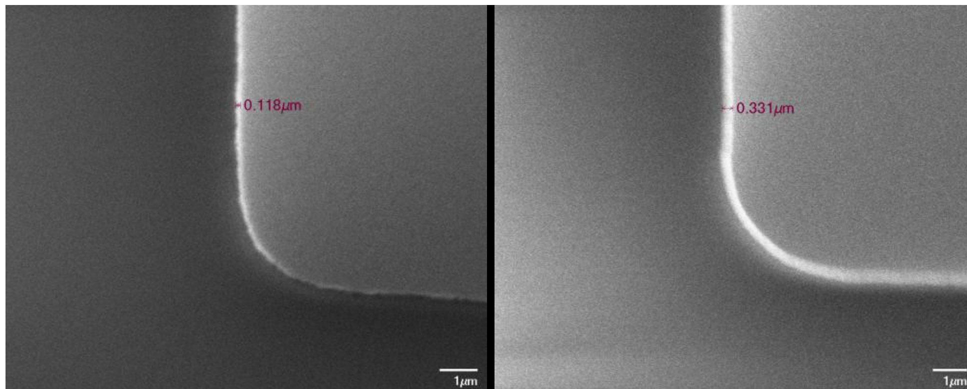
3.4.1. Fabrication of the third TFT process run

3.4.1.1. Buffer layer processing

(100) oriented prime grade P-type (Boron doped) silicon wafers were used as a starting substrate. The standard PECVD buffer SiO_2 film (500nm) deposition condition was used.

3.4.1.2. Gate electrode processing

Chromium (Cr) was used as gate electrode thin film. The standard condition of Cr sputtering and photolithographic work was used. The etching of Cr was done using CR14S wet etchant for 90 seconds. From the 2nd Run IS-TFT results, the taper angle at the gate electrode was not enough to give good step coverage. Therefore, dummy wafers were used to determine a better step coverage without significant erosion of the pattern edges. After 90 seconds of Cr etching in CR14S wet bath, an additional 10, 20, 30 seconds over-etch were performed. Figure 3-12 shows the etch results of gate patterns with 10 and 20 seconds over-etching. From the SEM images, an additional 20 seconds over-etch yielded the best step coverage, meanwhile 30 seconds over-etching shows significant pattern erosion. The additional 20 seconds etch patterns have ~20 degree taper angle, while 10 seconds etched patterns have ~45 degree taper angle. Since the TFTs masks were made with 1μm critical dimension (CD) loss for every direction, there will continuity will be maintained for the staggered layer on the pattern edges.



(a) (b)

Figure 3-12. SEM images of gate electrode patterns with (a) 10 seconds over-etch and (b) 20 seconds over-etch

3.4.1.3. Active layer processing

To reduce the interface defect density between the gate dielectric layer SiN_x, a-Si:H, and etch stop layer SiN_x, the layers were deposited by PECVD in situ (without breaking vacuum). To compare the single gate dielectric layer and graded gate dielectric layer (called dual gate dielectric layer), a low density SiN_x film of 300nm thickness was deposited for single gate dielectric film by using the standard SiN_x deposition condition and 250nm thickness of low density SiN_x following 50nm thickness of high density SiN_x films was deposited for the dual gate dielectric layer. Simply high density SiN_x is deposited by reducing the RF power from 40 watts to 20 watts. Following the gate dielectric, the a-Si:H film and etch stop layer were deposited consecutively without breaking the chamber vacuum. The thickness of amorphous silicon was 50nm.

3.4.1.4. Etch Stop layer processing

Previously, due to the problems of selectively etch for SiN_x to a-Si:H, a two step etching process was used. Therefore, to get a high wet chemical etch rate a low density SiN_x film was also made as an etch stop layer using a “dummy” or un-patterned wafer. The film was prepared in the PECVD with the conditions of 60 watts low frequency power, 200 watts RF power, NH_3/5%SiH_4-Ar /N_2(10/450/1000), 1800mTorr, and 350^oC. The deposition rate was 93nm/min and was 3.3 times faster than low stress SiN_x film. To get 300nm thickness, deposition time was 198 seconds. The first problem was, however, that the film had poor deposition uniformity, the difference of thickness between the center and the edge of the 4 inch wafer was over 50 nm (or 16.7%). Additionally the film had -84.55MPa (compressive) residual stress. The most important problem was that it undercut severely in during the wet etch and lifted off the etch stop layer patterns after photolithography works due to its poor density. In other words, the lateral etching rate was too high. Therefore, the standard low stress SiN_x film was used again for etch stop layer. The film was deposited onto a-Si:H with 300nm thickness in situ. The photoresist coating condition and temperature and time of soft bake, PEB, develop, and hard bake process were the standard photolithography process. The etching process used a two step etch recipe as previously described. The only difference in the 3rd run was to use C_4F_8 and O_2 plasma chemistry, which were used to promote an isotropic etch profile and promote a higher etch selectivity over a-Si:H film. The etching condition was that 200 watts RF power, 2000 watts ICP power, C_4F_8/O_2 (45/2) gas, 7 mTorr pressure, and 15^oC temperature. Since the etch rate was 3.26nm/sec, 90 seconds etch time was applied for leaving a few nanometers of SiN_x. Additionally, a 60 seconds Buffered Oxide Etchant 6:1 was applied to remove the SiN_x residues completely and to get a better

isotropic etch profile for a better step coverage. The etch results were tested/confirmed when the surface of TFTs were hydrophobic.

3.4.1.5. n^+ Si & Source and Drain electrode deposition

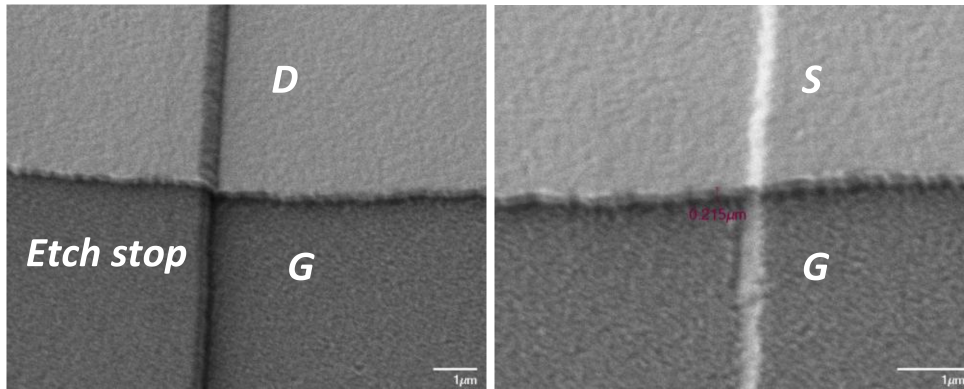
The standard deposition condition of n-type doped silicon was used. Since the RF matching network problem occurred when the RF power was over 160 watts RF power, 150 watts RF power was used and then deposition rate was recalculated from percentage of sheath voltage decrease. The deposition rate was reduced to ~1.0 nm/min.

Following the n^+ silicon deposition, chromium was deposited onto the n^+ Si. To enhance the step coverage and to withstand during the long via hole etch, the source/drain thickness was increase to 200nm. The deposition condition was the same of those of standard electrode deposition.

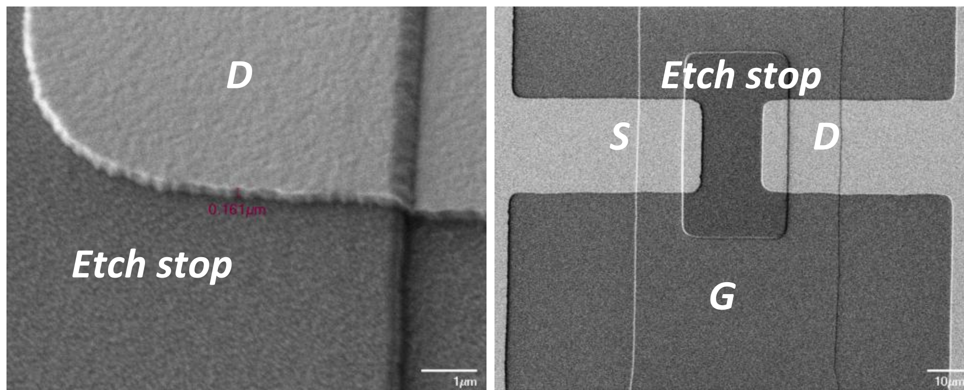
3.4.1.6. Back Channel Etching (BCE) process

For patterning the source and drain electrode, the standard photolithographic work condition was used as described previously. The etching of Cr pattern was done using CR14S wet etchant for 130 seconds. For the source/drain etch, to avoid the isotropic etch profile, no over-etching time was applied due to pattern channel region accurately. Etching to the visual end-point had a sufficient isotropic profile for the passivation layer coating.

To etch the n-type doped silicon etch, an SF_6 and Ar plasma was used. The dry etch condition for 50nm etching was 30 watts RF power, 2000 watts Inductive coupled plasma (ICP), and 10 mTorr pressure, 15°C temperature. Etch rate of n^+ silicon was ~10 nm/sec, and for the same etch recipe, the etch rate of etch stop layer was ~7.5nm/sec. Therefore, 18 seconds etch time was applied to etch 50nm of n^+ Si and 100nm of the etch stop layer. Figure 3-13 shows the



(a) (b)



(c) (d)

Figure 3-13. SEM images of back channel etched TFTs; (a) step coverage on etch stop layer pattern, (b) step coverage on gate pattern, (c) channel with isotropic etch profile, and (d) overall image on TFT channel region

channel images after back channel etching. The real etch result was 50nm of doped silicon and 100nm of etch stop layer roughly.

3.4.1.7. Passivation layer deposition and via hole etching

The standard low stress SiN_x thin film was used and deposited as a passivation layer. The thickness of the passivation layer was 300nm. For patterning of via hole etching, the standard photolithography process was used with thicker photoresist. SPR™ 220 3.0 photoresist was used with 1500 rpm spin speed for 60 seconds (3.20μm). The via hole etching condition was 30 watts RF power, 2000 watts ICP power, SF_6 /Ar(45/1 sccm) gas, 10 mTorr, 15°C temperature. Totally, 90 seconds etch time was required to etch through the gate electrode contact. However, a 100% over-etch was applied, thus 180 seconds etching time was used to ensure the contact between the contact pads and the end of probe tips. Before photoresist stripping, a 30 seconds descum was used to remove the rigid photoresist layers.

3.4.2. Characterization of TFTs from third process run

Figure 3-14 shows the electrical properties of the TFT with different gate dielectric layers; the single gate dielectric and the dual gate dielectric layers. The single dielectric layer has a higher 'on' current state and lower 'off' current state than the dual gate dielectric. The gate voltage was swept from -15 V to 30 V with four different drain-source voltage (V_{ds}) from 3 V to 9V with intervals of 2 V. The leakage current was compared at V_g= -7V. Both single and dual dielectric SiN_x TFT showed the 'on' and 'off' state current ratio between 10^3 and 10^4 and the threshold voltage (V_T) was around -5 V. Both cases showed the drain current kink around V_g= 0V and no saturation regimes were shown. The expected results were that the dual gate

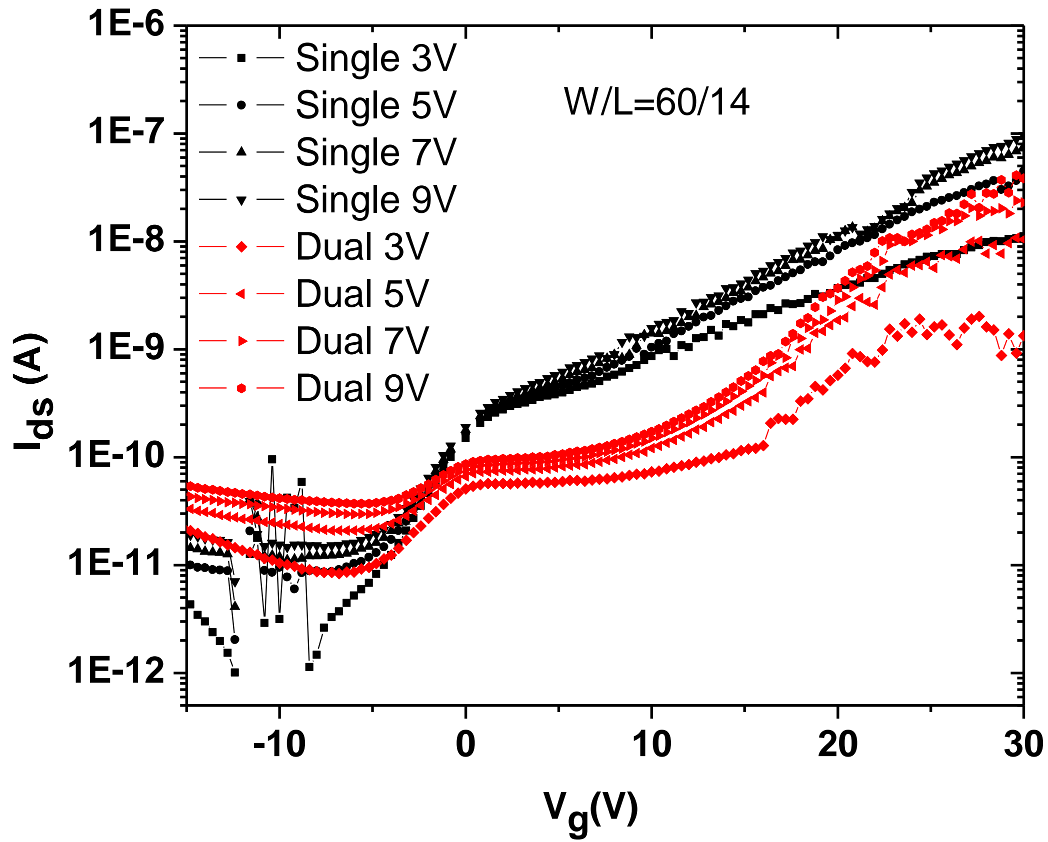
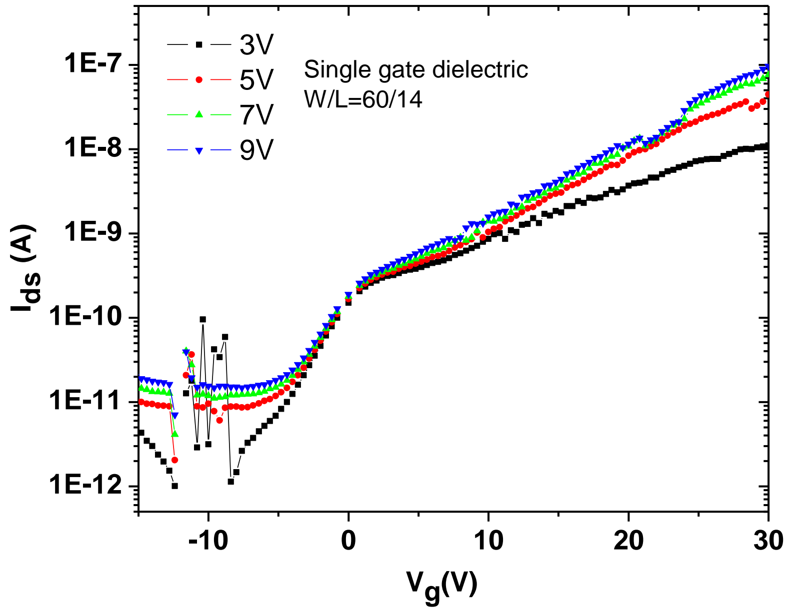


Figure 3-14. The electrical properties of the TFT with single gate dielectric (high RF power) and dual gate dielectric (low and high RF power) used during gate dielectric deposition)

dielectric layers would have better I_{ds}-V_g characteristics since the lower RF power during deposition can reduce the interface defect density between the gate dielectric SiN_x layer and a-Si:H layer. As shown in figure 3-14, the I_{ds}-V_g characteristics of the dual gate dielectric layer used in 3rd Run TFT suggests that the induced charges from gate were trapped at the interface of high density SiN_x and low density SiN_x gate dielectric film since trapped charges act as a leakage current path in the 'off' state. Additionally, at higher gate voltage the drain current shows an exponential increase due to the fact that accumulated charges are released at high gate voltage. Under normal TFT linear region operation, the current should be increased linearly with the increase of gate voltage, and then saturated in the 'on' state. Therefore, the single gate dielectric was used to obtain desirable I_{ds}-V_g characteristics.

To characterize the single gate dielectric TFTs, the gate voltage was swept from -15 V to 35V at interval of 0.5V and drain voltage was varied from 3 V to 9V at 2 V intervals. Figure 3-15 shows the I_{ds}-V_g electrical characteristics of TFT measured in different channel widths and lengths, which shows that the electron mobility in channel region was stable. The TFT has the following electrical characteristics; 7.0 V threshold voltage, 0.133~0.149 cm^2/Vsec field effect mobility, 10^4 on/off current ratio, and less than 10^{-11} ampere leakage current at V_G= -10V. As shown in the figure 3-15, the I_{ds}-V_g transfer curves are kinked around V_g =0V, which suggested that the contact resistance at source and drain acts as a limiting factor to decide the whole device resistance rather than the channel resistance. Thus, the transfer curve should improve with decreased resistivity of ohmic contact, n^+ Si film resistivity.

To improve the n^+ contact layer, a new ordered n^+ Si sputtering target was used for fabricating the 3rd Run IS-TFT, and the properties of n^+ Si sputtering targets are investigated. The newly ordered n^+ Si target (same part # of Kurt J. Lesker product) was used, however, the



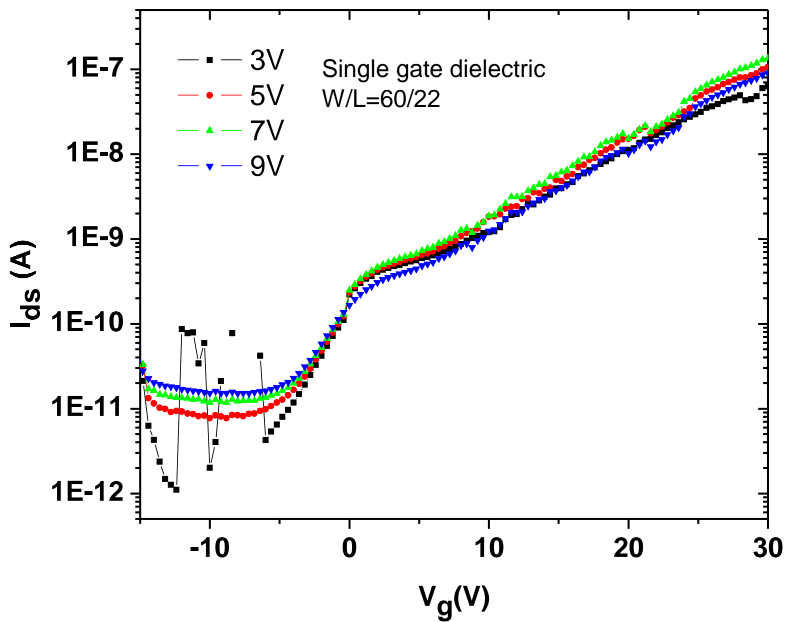


Figure 3-15. Current-Voltage characteristics of the 3rd TFT device for single gate dielectric SiN_x: Width/Length (60/14), and Width/Length (60/22)

resistivity of the target increased five times without indication from the vendor. Therefore, even though the same deposition condition was used, the resistivity of the deposited n^+ Si layer was increased five times. During the design of experiments (DOE) for getting a lower resistivity from new target, significant problems were also detected. A DOE factorial design was done with two factors; substrate power and deposition temperature, however, every case showed poor results with a resistivity around 400 ohm-cm. For simple test, the deposited n^+ Si samples were dipped into BOE solutions. During the brief BOE etch, the n+ Si films were completely etched away in 3 minutes. This indicated that the n+ Si film were partially oxidized even though no oxygen gas was flowed into the chamber. It was speculated that the sputtering chamber was outgassing oxygen or it had a leak. After cleaning chamber walls and target shutters and chimneys, the resistivity of deposited n^+ Si film was decreased to 25.2 ohm-cm with 200 watts RF power, 30 watts substrate power, 5 mTorr working pressure, and room temperature. Previous results produced an n^+ Si resistivity of 1.44 ohm-cm. After cleaning chamber, the similar experiments were done to enhance the electrical properties of n^+ Si film as a function of temperature, substrate power, pressure, and distance between the target and the substrate. The details of the DOE procedure and results were previously described at section 2.3.3.3. As expected, increased substrate and target power, reduced distance, room temperature, and moderate pressure resulted to the lowest resistivity of n^+ Si film. However, the lowest resistivity achieved from the new DOE was 14.7 ohm-cm with 300 watts RF power, 30 watts substrate power, 5 mTorr, room temperature, and 15.6 cm distance between the substrate and target. To improve the resistance, the Ar gas line was changed, and the system was manually checked for leaks (not leak checked with a residual gas analyzer). No specific leaks were detected and this problem was not able to be solved. Thus while the targeted value of resistivity of n^+ Si film was ~1 ohm-cm (resistance

of 5000 ohms for a 50nm thickness), our devices which contained sputtered n^+ silicon suffered due to the high contact resistance.

4. Fabrication and characterization of Thin Films Transistor array with vertically aligned carbon nanofiber

4.1. Vertically aligned carbon nano fiber (VACNF) growth

Vertically aligned carbon nano fibers (VACNFs) were grown at direct current plasma enhanced chemical vapor deposition (dc-PECVD) chamber with metal catalysis. With C_2H_2 and NH_3 mixture gas decomposed onto the catalysis while dc power was applied to grow CNF vertically. Previously to grow VACNF on adequate wafer, several candidates of catalysis materials and complicated technique such as silicon sacrificial layer were tried. Prior to try to integrate VACNF on the TFT device, VACNF growth tests were done with the similar environment of the real TFT case.

4.1.1. Experimental

Initially, fabricated TFTs were used to test VACNF growth after fabricating gate, gate dielectric, silicon, ohmic, and source and drain film structure. However, to reduce time consuming simple test structure was fabricated and used to test VACNF growth later. Since chromium (Cr) film was used as source-drain electrode for the TFT device, Cr film was deposited onto the SiO_2 buffer/Si wafer. SiO_2 film was grown at PECVD chamber with 500nm thickness of the standard deposition condition used as the TFT buffer layer. To make a current path for dc-PECVD between the top clamps and the bottom of the wafer, edge region of the wafer were removed using BOE wet etchant after SiO_2 deposition with the standard photolithographic work. And then Cr film was deposited with the standard deposition condition used at TFT fabrication in the sputtering chamber with the thickness of 200nm, which was the

thickness of source and drain Cr electrode film. To make catalysis for VACNF growth, standard photolithographic work was used to define the dots on the drain electrode region, where the VACNF starts to grow. The thickness of photoresist was around 1.75 μm after descum process. 50nm Ni thin film as a catalysis was deposited by e-beam evaporation. To pattern the Ni dot, conventional lift-off process was done by using acetone for ~ 1 hour at room temperature. Additionally, the photoresist around edge regions was removed by acetone manually.

4.1.2. Results and discussions

First trial of VACNF growth was done at fabricated TFT of poly-crystalline silicon based structure, which was grown at low pressure chemical vapor deposition (LPCVD) system. The growth condition was 0.5 Ampere current, 10 Torr pressure, C_2H_2/NH_3 (50/200) flow rate, and 500°C for 15 minutes. Figure 4-1 shows the scanning microscope (SEM) images of grown VACNF on source and drain electrode.

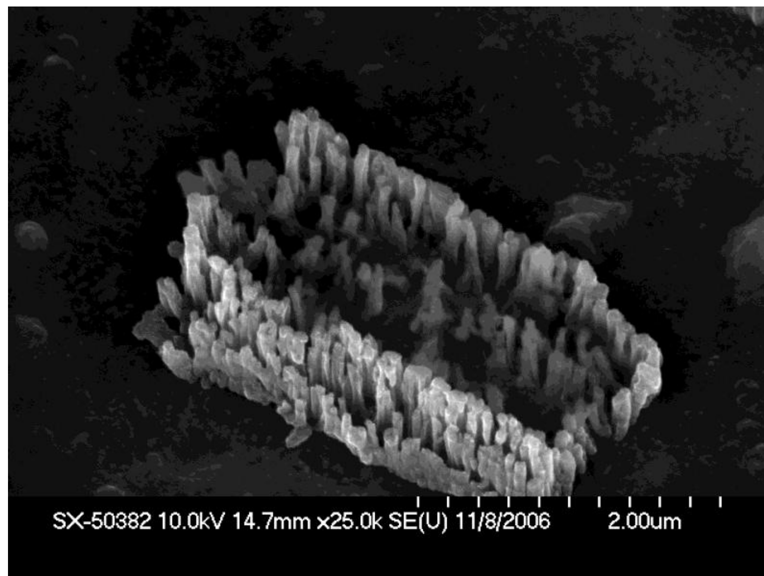


Figure 4-1. SEM images of failed VACNF on the large Ni catalyst area

The CNFs were grown at the edge region of the Ni catalysis area with the short height like carbon nanotube. However, it still showed that the possibility of VACNF growth on the Cr electrode film. To grow CNF vertically well, increased temperature 700°C was applied while other conditions were the same. Figure 4-2 (a) shows the failure of VACNF growth. Due to high temperature, the source and drain Cr film was delaminated initially and no VACNF growth was observed. At that period of time, there was no stress measurement system in facility, and conventional Cr deposition condition was 200 watts RF power, 200°C temperature, 25 sccm of Ar-H_2 gas flow, and 3 mTorr pressure. Film delamination was mainly initiated from the thermal stress for high temperature process since the difference of thermal coefficients of expansion (TCE) between Cr and silicon film. Conventionally, sputtered metal film such as Cr has a high residual tensile stress [96]. To reduce the residual stress in the Cr film, 5mTorr pressure was adopted and figure 4-2 (b) shows the VACNF grown at the same VACNF growth condition. After initial trial of VACNF growth, reduced temperature such as 500°C and 600°C with different ratio of C_2H_2 and NH_3 gas flow rate were tried to reduce the failure by thermal stress. However, all these trials did not showed the good results. The film delamination for CNFs growth or after growth was happened occasionally and VACNFs were not grown or showed very short height or bended.

To overcome the problem, high temperature process was essential to grow VACNF well, which initiate the Cr film delamination. Later, the Cr film residual stress was optimized using substrate power was applied for sputtering and measured the exact value of stress after stress measurement system was installed. To mitigate the high temperature process and to have a desirable height of VACNF, the growth condition was slightly changed. 1.0 Ampere current, 15 Torr pressure, C_2H_2 / NH_3 gas flow rate (85/200 sccm), and 700°C for 19 minutes. Figure 4-3

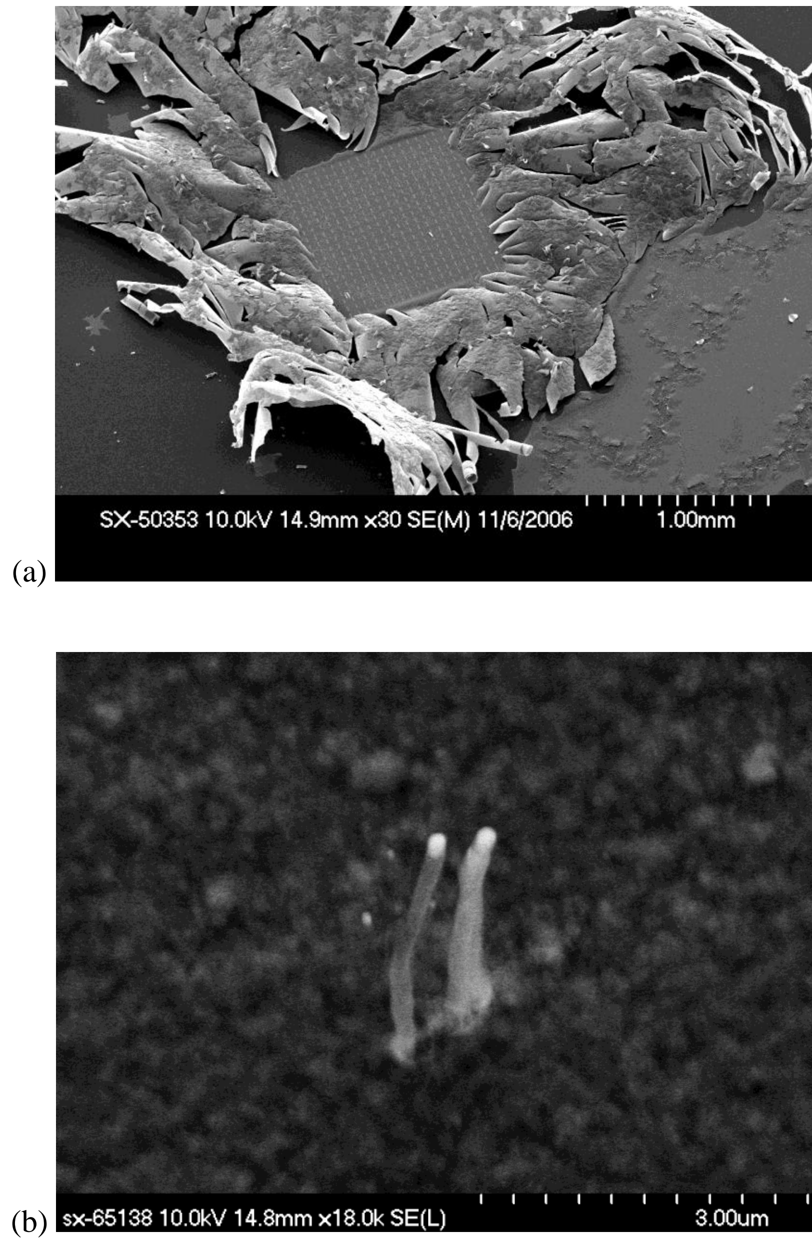
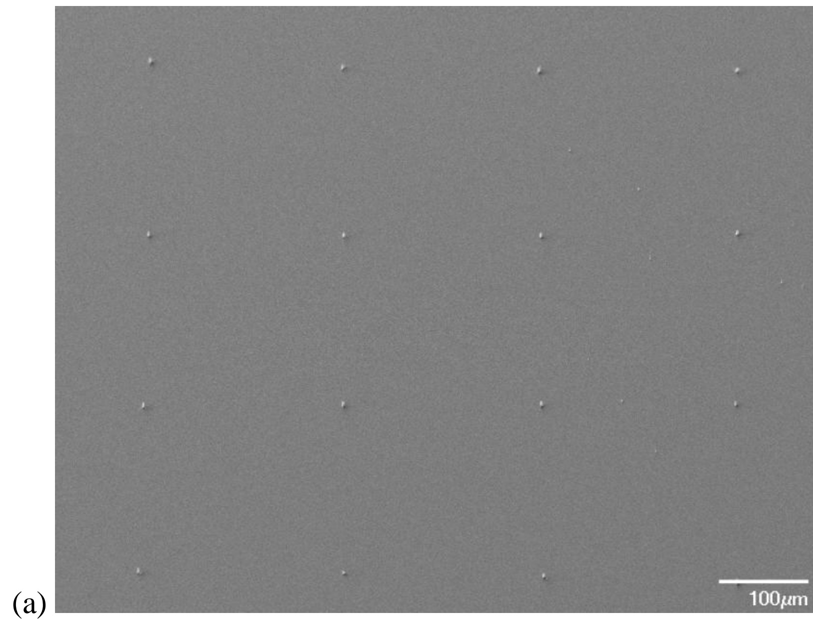


Figure 4-2. SEM images of (a) delaminated source and drain Cr electrode film due to the thermal stress in the film, and (b) VACNF grown after reducing residual stress in the Cr film grown at 5 mTorr working pressure for Cr film sputtering

(a) 

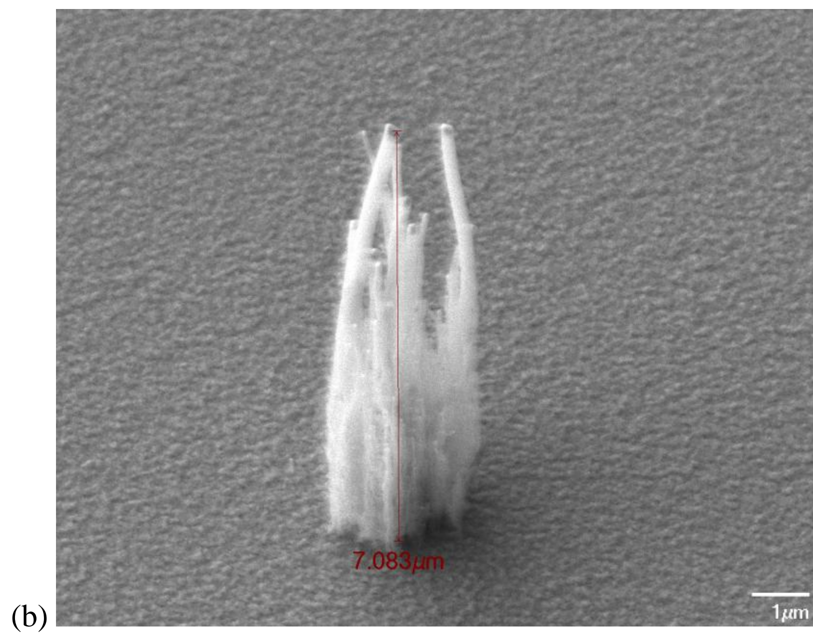
(b) 

Figure 4-3. SEM images of (a) VACNFs grown on the low stress Cr film, and (b) single VACNF with height of 14 μm

shows (a) grown VACNFs on the low stress Cr film, and (b) single VACNF. All images were taken with 30 degree tilted. The key factor to grow VACNF on the Cr film was that to control the residual stress of Cr film and to be grown at relative high temperature (700°C) with optimized pressure, current, and gas mixture ratio.

4.2. Fabrication of characterization of the first TFT-VACNF device process run

From the 3rd Run of Inverted Staggered Thin Film Transistor fabrication, optimized layer processes were well developed except the high resistivity of doped silicon layer. Though the ohmic contact layer had high resistivity, TFT-VACNF integration was performed and characterized to optimize the integration issues.

4.2.1. Fabrication of the first TFT-VACNF device process run

4.2.1.1. Contact via holes for carbon nanofiber growth.

Direct Current Plasma Enhanced Chemical Vapor Deposition (dc-PECVD) was used for carbon nanofiber growth to integrate with the TFT device. The integration process flow is represented in figure 4-4. Since direct current was used, the surface and the bottom of wafers need to be electrically conducting. However due to the n^+ Si, etch stop layer, a-Si:H, SiN_x, and buffer SiO_2 the chromium and nickel layers were mostly electrically isolated from the silicon substrate and substrate holder. Thus, for VACNF growth the plasma arced and caused damage to the devices. Figure 4-5 are SEM images demonstrating the plasma arc damage on the TFT surface after VACNF growth.

To avoid plasma arc damage for VACNF growth, contact via holes were patterned across the entire wafer to make electrical contact from the top Chromium layer to the silicon substrate.

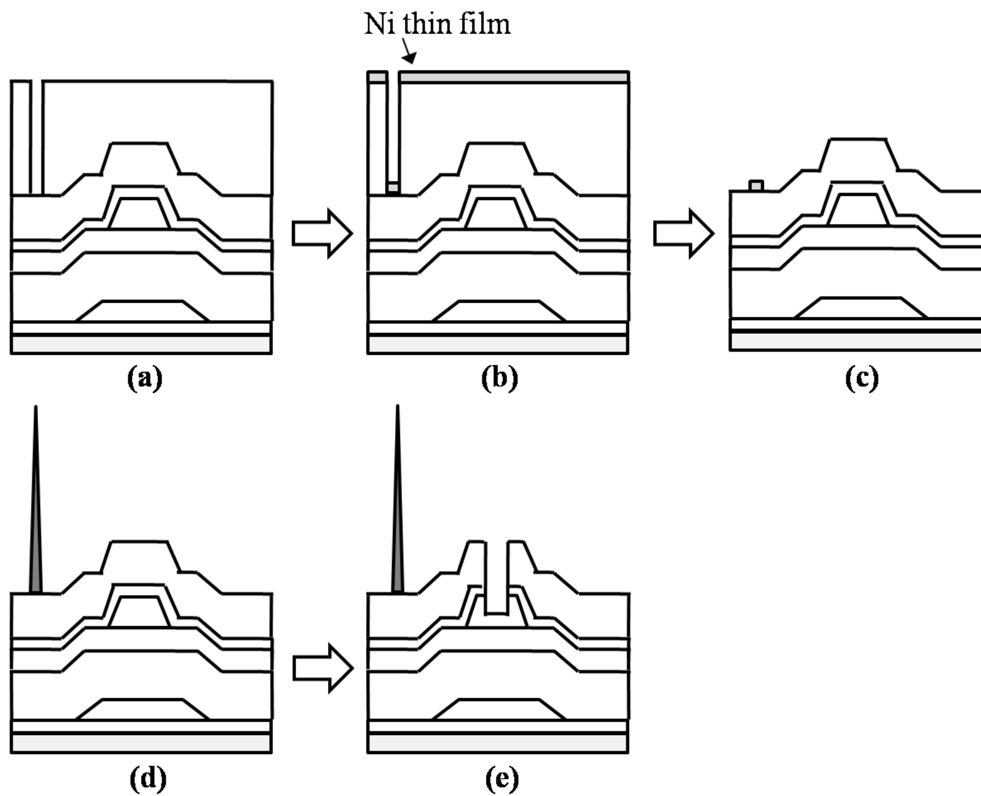


Figure 4-4. Schematic illustrating the fabrication processing sequence for the TFT-VACNF integration. (a) Ni dot patterns are formed on source-drain electrodes using conventional photo-lithography, (b) and Ni deposition by evaporation, (c) the lift off process, (d) illustrates the VACNF growth on the nickel catalyst on the uniform chromium layer which is, and (f) subsequently patterned followed by the active layer back-channel etch process

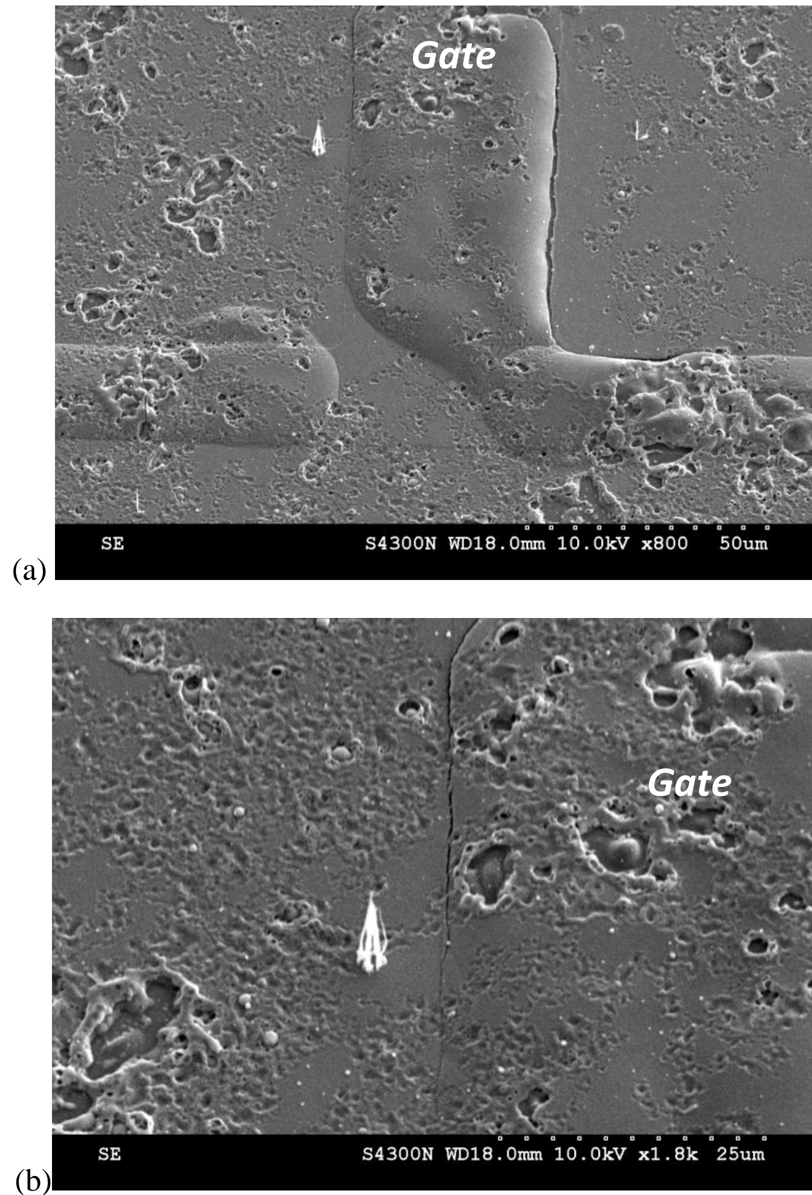


Figure 4-5. SEM images of plasma arc damage of the TFT after VACNF growth (a) shows the top Cr film was attacked in the region of the bottom gate pattern lines, and (b) shows a VACNF grown on top of the drain electrode which was also damaged by plasma arcing

A new photolithography mask was prepared to make eight 0.5cm by 0.5cm squares contact holes. To test the contact holes, a simple n^+ Si (50nm), a-Si:H(50nm), SiN_x (300nm), and SiO_2 (500nm) film stack was deposited onto a silicon wafer. To make electrical contact to the silicon wafer the new mask photolithographic mask was patterned after n^+ Si film deposition and prior to the chromium deposition. The deposition, exposure, and development conditions were the similar of those of via hole etching case. Since reactive ion etching (RIE) was used to etch through from n^+ Si to the bare silicon wafer, thicker PR layer was required to withstand the long plasma etching time. The etching profile of the contact holes was a not an important process issue, but complete etching of insulating film was required. Thus a 100% over etching time was applied for plasma etching, which was followed by a BOE 6:1 wet etch to remove the buffer SiO_2 layer completely. After the via etch to the silicon wafer the chromium film was sputter deposited uniformly across the wafer followed by the Ni catalyst dot patterning, deposition and lift off. Finally, the VACNF growth process was attempted using the same conditions described above.

Observation for the VACNF growth and post deposition inspection revealed that there was no plasma arc damages for VACNF growth for the through via samples. Thus the through vias adequately bleeds off any charge for the dc-PECVD process. The height of VACNFs was measured to be ~ 20 μm under these conditions. Figure 4-6 a) is an SEM image of showing an ~20 microns tall VACNF successfully grown using the through via patterns, and b) shows the grown VACNFs on a the alignment marks which shows evidence of bubbles which form for the VACNF growth.

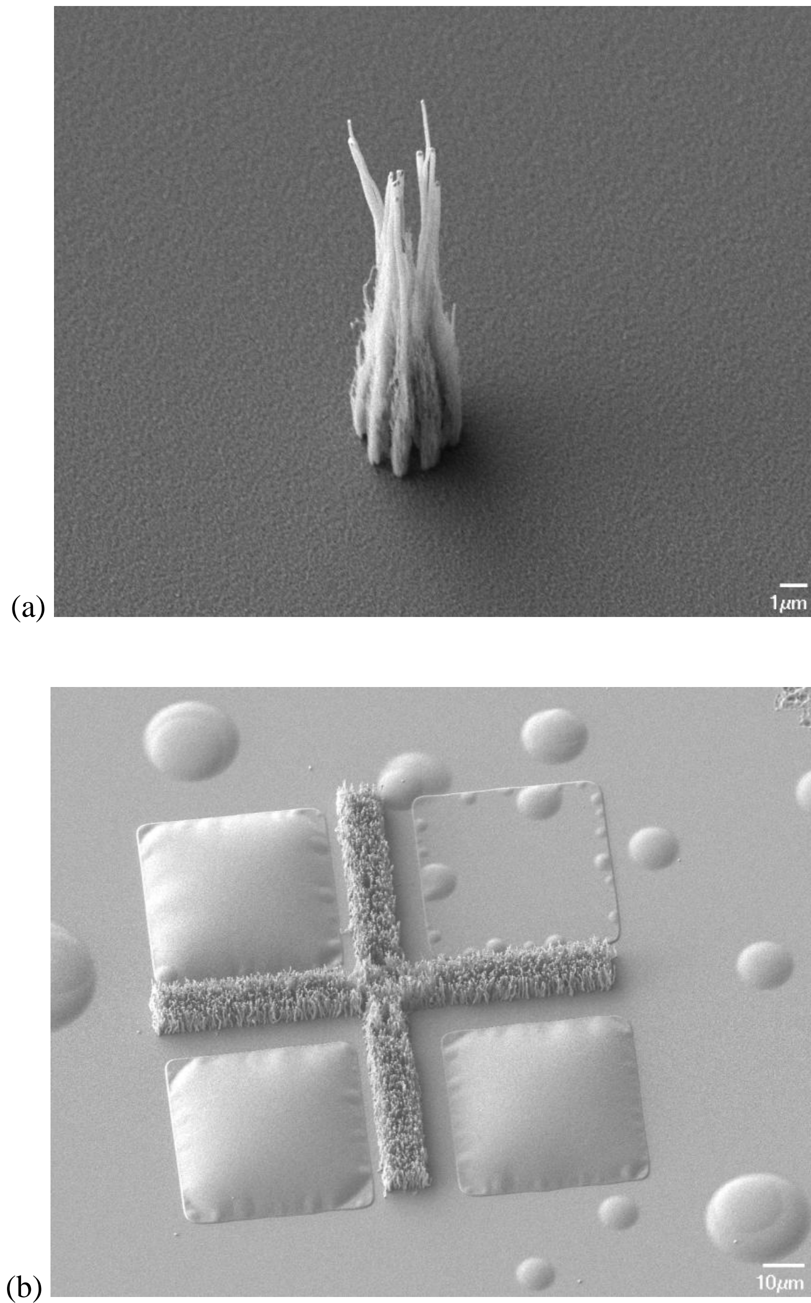


Figure 4-6. a)SEM image of showing an ~ 20microns tall VACNF successfully grown using the through via patterns, and b)SEM image showing bubbles which lift the chromium source and drain electrode for VACNF growth on the region near the alignment marks

4.2.1.2. Dehydrogenation process to remove bubbles

The bubbles, which induced the chromium film delamination for the VACNF growth was attributed to dehydrogenation of the SiN_x, and a-Si:H films. Since SiH_4 gas was used to deposit the films in the PECVD system hydrogen gets easily incorporated into the films for growth. To determine the source of bubbles clearly, pre-VACNF dehydrogenation anneals were performed after making the etch stop layer pattern of the TFT device. Initially a 500°C, 1hr anneal using a 5°C/min ramp rate was applied to remove hydrogen from the films based on reports which have shown that that dehydrogenation can be achieved between 250°C and 600°C [100-101]. To test the efficacy of the dehydrogenation process, another run of TFT-VACNF wafers were ran.

4.2.1.3. Fabrication of TFT-VACNF integration device process

4.2.1.3.1. Buffer layer process

300nm thickness SiO_2 buffer layer were deposited on (100) oriented n-type (Phosphorus doped) silicon wafers using the standard condition reported in table 2-5.

4.2.1.3.2. Gate Chromium (Cr) electrode processing

Another important issue in the VACNF integration is the interlayer thermal stress generated for the VACNF growth. This was particularly true for the chromium films. Initially, no substrate biased was applied for the Cr film for deposition which resulted in for the VACNF growth at high temperature. As described previously, biased sputter deposition reduced the residual tensile stress in the chromium film to a nearly stress free level. After sputtering, the residual stress of Cr films were measured as a function of substrate power and shown in figure 4-

7. 100nm thickness was used for the gate electrode, and 200nm thickness was used for source and drain electrode while other deposition conditions were that 200 watts RF power, 5 mTorr pressure, 25 sccm of Ar gas flow, and 200°C temperature. In both cases, at 5 Watts substrate power the residual stress showed the minimum value between -10 MPa and 10 MPa while the deposition rate of low stress Cr was 4nm/min. The sheet resistance was between 1.21 - 1.29 ohms/sq. To prevent the device failure, 5 watts substrate biased Cr film must be employed for TFT-VACNF integration. For patterning of gate electrode, initially primer was dispensed onto the wafer with 3000 rpm and 60 seconds. Subsequently, SPR^{TM}220-3.0 photoresist was spun with 3000 rpm for 60 seconds. The resulting thickness of photoresist was 2.75 µm. Soft-bake, post exposure bake (PEB), and hard-bake conditions were changed to 115°C with 120sec to fit the exposure condition. Resist development was processed by CD-26 developer for 60 seconds which was followed by the descum using a 400 watts RF power, 10 sccm flow rate of O_2, 150mTorr pressure 30 second plasma treatment. After descum, the thickness of the photoresist was reduced to 2.50µm. The etching of Cr was done by CR14S. After the visual end point was detected, 20 seconds more etching time was applied to have a good taper angle. After gate patterning, the photoresist was removed by Microposit^{TM} remover 1165 at 70°C temperature for 30 minutes and an additional oxygen plasma descum for 2 minutes. This new photolithography process flow is referred to as the 2nd standard photolithography process described in Table 4-1.

4.2.1.3.3. Active layer processing

To reduce the interface defect density of state, 300nm thick gate dielectric SiN_x, 100nm thick a-Si:H, and 200nm etch stop layer SiN_x were deposited in situ without breaking vacuum in the PECVD chamber. For this processes some wafers were repositioned for pump-out procedure

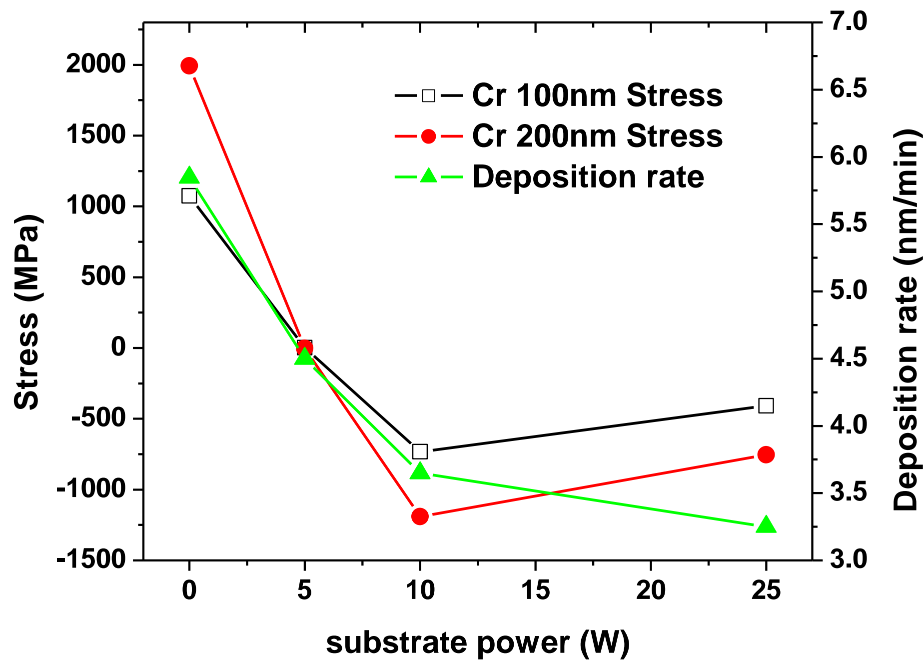


Figure 4-7. Residual stress and the deposition rate of Cr film which evolves for sputtering as a function of substrate power

or deposition, which lead to sliding of the wafer. Technically, it originated from the curvatures of the initial wafer and charging of the wafer. Later all wafers were changed to prime grade to overcome this problem. As described previously, the standard deposition condition for SiN_x, a-Si:H, and etch stop SiN_x films were used. The thickness of a-Si:H film was increase to 100nm due to reduce the risk of deep etch stop layer patterning.

Since the step coverage above the etch stop layer pattern also may generate the disconnection of source and drain electrode lines, the thickness of etch stop layer was reduced to 200 nm. After deposition of the etch stop layer SiN_x film, 500°C, 1 hr annealing process was done to dehydrogenate the films and reduce the bubble formation for VACNF growth process. It was done using a box furnace with 5°C/min ramp rate. To compare the dehydrogenation effects, anther wafer was prepared with the same fabrication process without the dehydrogenation process. After pattering the photoresist for the etch stop layer with the standard process condition described at Table 4-1, a two step etch process was applied. The dry etching condition was a 200 watts RF power, 2000 watts ICP power, C_4F_8/O_2 (45/2) gas, 7 mTorr pressure, and 15°C temperature. The etch rate was determined to be 3.6nm/sec, thus a 55 second etch time was applied to slightly under etch the SiN_x layer. Additionally, a 60 second of BOE (6:1) wet etching was applied to remove the SiN_x residues completely and to promote an isotropic etch profile for better step coverage.

4.2.1.3.4. n^+ Si & Source and Drain electrode deposition

As mentioned previously, the high resistivity of the doped silicon film layer was the main problem of 3rd run TFT process. The deposition condition of 100nm n^+ Si film was 300

Table 4-1. The 2nd standard recipes for each thin film process and photolithography process flow

Standard recipes for thin film deposition process							
Material	equipment	Power (watt)	Gas/flow rate (sccm)	Pressure (mTorr)	Temperature (°C)	Deposition rate (nm/min)	Stress (MPa)
Metal(Cr)	sputter	RF(200) /DC(5)	Ar(25)	5	200	4	~ +10 (G:100nm, S/D: 200nm)
Dielectric (SiO_2)	PECVD	RF(20)	5%SiH_4-Ar/N_2O (85/157)	1000	350	69	~ -180 (buffer:500nm)
Dielectric (low stress SiN_x)	PECVD	RF(40)	5%SiH_4-Ar/NH_3/N_2 (150/2//790)	600	350	14.3	~ +50 (gate dielectric:300nm)
Active (a-Si:H)	PECVD	RF(10)	5% SiH_4-Ar (500)	1000	350	24.7	~ -120 (200nm)
Ohmic contact (n^+ a-Si:H)	Sputter	RF(200) DC(30)	Ar (25)	5	R.T	3.5	~ -20 (50nm)
Standard recipes for Cr wet etching process (chapter 2)							
Cr	CR14S wet etchant at room temperature						
Standard process for photolithography (chapter 2)							
Photoresist (PR)	SPR™220-3.0 photoresist						
PR spinning	Spinning rpm/time (sec) = 3000 / 60 (2.75 µm thickness)						
pre-bake	(115°C / 120sec)						
Exposure	Quintel contact aligner[Vacuum mode] (depending on the PR thickness & illumination power density)						
Post-exposure bake (PEB)	(115°C / 120sec)						
PR develop (°C)	60 sec (CD26 developer)						
Hard bake	(115°C / 120sec)						
Descum	Technics RIE, RF(400 watt), O_2(10 sccm), 150 mTorr pressure, R.T for 30sec						
Etching	Etching (wet or dry etching)						
PR stripping	Microphosit™ remover 1165 (70°C / 30min)						
Ashing	Technics RIE, RF(400 watt), O_2(10 sccm), 150 mTorr pressure, R.T for 120sec						

watts RF power, 30 watts substrate power, 5mTorr pressure, Ar (25 sccm) gas, a 15.5 cm target-to-substrate distance, and room temperature to reduce the resistivity of doped silicon layer. The lowest resistivity acquired from this condition was 18.7 ohm-cm. Even though it still had a higher resistivity for the application, these deposition conditions were used for the doped silicon film.

To reduce plasma arc damage for VACNF growth process, contact holes were patterned to make current path through the bottom of bare silicon wafer. The long etch time required a thicker photoresist. Thus, the standard photolithography process was slightly modified for thicker photoresist. SPR^{TM}220-3.0 photoresist was spun on the wafer with 1500 rpm for 60 seconds resulting in a 3.2μm thickness. The etching of contact holes was processed by RIE with SF_6 and Ar plasma. The etch condition was that 30 watts RF power, 2000 watts ICP power, 10 mTorr pressure, 45 and 1 sccm flow rate of SF_6 and Ar, and 15°C temperature. The measured etch rate of SiN_x, and a-Si:H film were 7.5nm/sec and 10nm/sec, respectively. The target etch depth was 500nm to the bare silicon from the n^+ Si film. Thus, 120 seconds etch time was applied to ensure the etch depth. Next a 180 seconds BOE wet etch was applied to remove buffer SiO_2 film. Subsequent to the via through hole etch, the Cr source and drain film was deposited on to the n^+ Si. To compare the effect of the dehydrogenation anneal, 200nm source and drain Cr film was deposited on the 500°C dehydrogenated TFT, and 300nm source and drain Cr film was deposited on the non-annealed TFT. Both cases, Cr films were deposited with the residual stress free condition with 5 watts substrate power for sputtering.

4.2.1.3.5. Vertically Aligned Carbon Nano-Fiber (VACNF) integration to TFTs

For growing VACNFs a conventional lift-off process was used for making Ni dot patterns. To make a thin photoresist, SPR^{TM}220-0.7 Photoresist was spun on to the wafer with 2000 rpm for 60 seconds. 90 seconds of soft bake process was done at 115°C. The measured thickness of photoresist was around 600nm. 5 seconds of exposure time and 115°C, 90 seconds of PEB process was applied. After CD-26 was used to develop the pattern, 115°C, a 90 second hard bake was done. An additional 15 seconds oxygen plasma descum process relative to the standard process was essential to define the Ni dot patterns. To ensure the electrical conductance through the bottom of the wafers, the backside of the wafers were cleaned by BOE wet etching. Following the preparation of the Ni catalysis, the photoresist around the wafer edge was removed by acetone manually to make it compatible with a dc-PECVD process. This photolithography process for pattering Ni dot catalyst for VACNF growth is the standard photolithography process for Ni dot patterning.

Conventional e-beam evaporation was used to deposit 50nm Ni films followed by a lift-off process which resulted in ~ 1.5 μm in diameter Ni cots on the Cr drain electrode area. VACNFs were grown in dc-PECVD chamber with a condition of C_2H_2/NH_3 (85/200) gas flow, 15 Torr, 1 Ampere current, and 700°C temperature and total time for the growth was 19 minutes. Figure 4-8 shows a 500°C for 1hr dehydrogenated TFT with a few bubbles in the top Cr film after VACNF growth and the measured height of VACNF was ~ 20μm. From the pre-test of dehydrogenation bubble effects at 500°C, no bubbles were observed, but at 700°C, bubbles generated for high temperature process of VACNF growth.

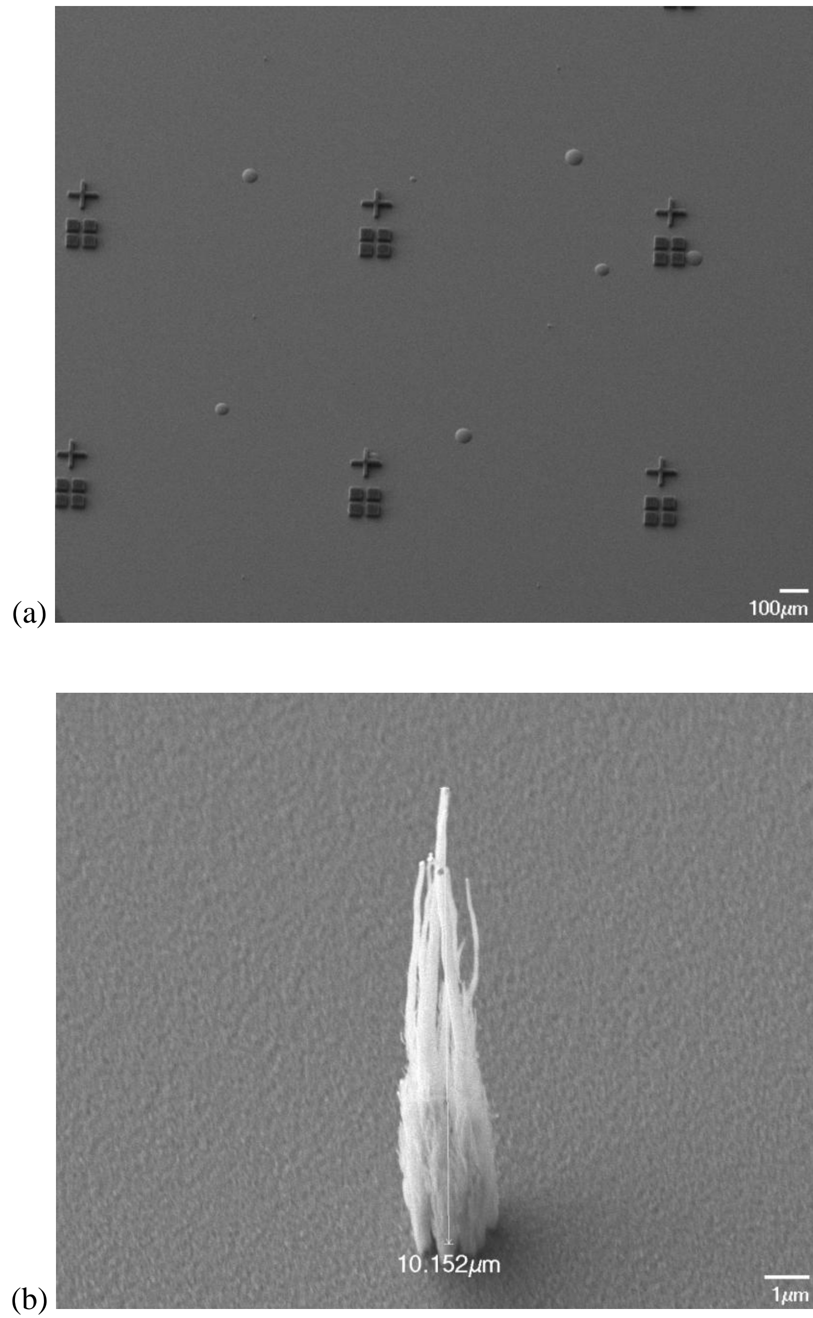


Figure 4-8. SEM images showing the grown VACNF on the Cr layer with hydrogen bubble effects. (prior to source/drain patterning) (a) a few bubbles on the top surface, and (b) single VACNF with a height of ~20 μm

In the case of 500°C annealed TFT, a few bubbles were generated. Otherwise, the non dehydrogenated processed TFT shows severe bubble formation in the chromium film after VACNFs were grown on the Cr film in figure 4-9. Figure 4-9 also reveals the source of hydrogen for VACNF growth. There were two possible hydrogen sources; a-Si:H film and SiN_x film since these two films were deposited from SiH_4 gas in PECVD. From the images, no bubbles were observed on the etch stop layer patterns and its boundaries.

This indicates that the bubbles for high temperature process were coming from the a-Si:H film. To minimize the hydrogen bubbles, another DOE was done as function a-Si:H film deposition temperature and annealing temperature and time. Table 4-2 lists the results of bubble formation test of a-Si:H film as a function of deposition temperature and annealing temperature, time, and ambient. It can be seen from Table 4-2 that the bubbles formed for dehydrogenation process at high temperature VACNF growth process are clearly minimized by an a-Si:H deposition temperature of 400°C followed by a 600°C anneal in air ambient for 2 hrs. From the table, the formation of a few bubbles on the top of Cr film could be controlled from the dehydrogenation process. Since a certain amount of hydrogen in the silicon network is required to passivate the dangling bonds to reduce the charge trapping, as well as reduce the residual stress in the film, the a-Si:H film was deposited at 350°C and coupled with the dehydrogenation process for integrating the VACNF on TFT structures.

4.2.1.3.6. Back Channel Etching (BCE) process

The Back Channel Etch process is essential to isolate the n^+ contact layer between the source and drain electrode for transistor operation. The 2nd standard photolithography process was done using the contact aligner with 40 seconds exposure time. A descum process was not

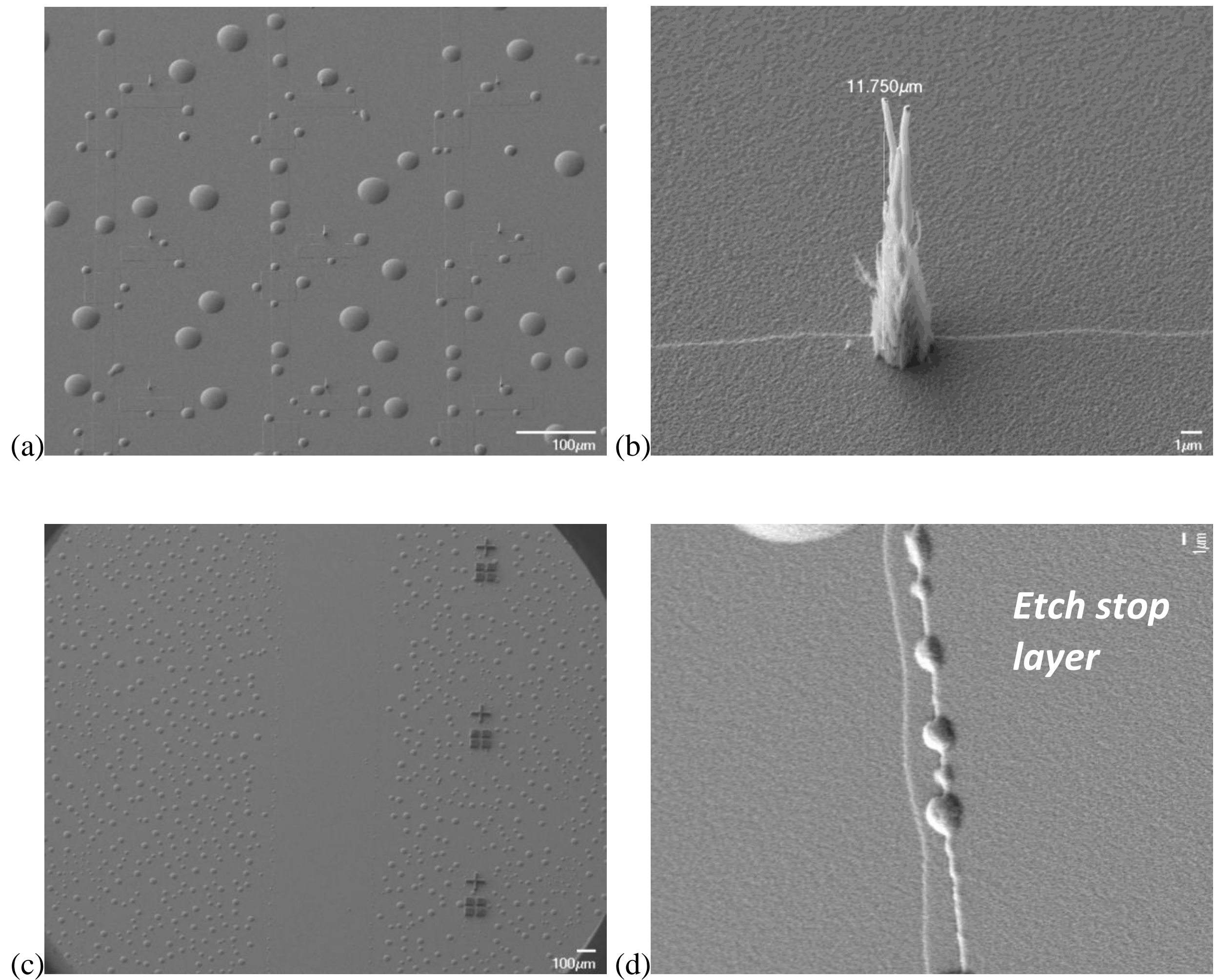


Figure 4-9. SEM images showing the grown VACNF on the Cr layer without dehydrogenation process (prior to source/drain patterning). (a) Severe bubble formation is observed in the top Cr film, (b) single VACNFs, (c) No bubbles are shown at the edge of the etch stop layer pattern boundaries, and (d) hydrogen apparently escapes laterally on the etch stop layer suggesting that hydrogen bubbles are generated from the underlying a-Si:H film.

Table 4-2. Comparison of the bubbles on TFT with the deposition temperature of amorphous silicon and annealing conditions; temperature, time, and ambient

	Annealing Process			
a-Si (100nm)	Temperature, time	H explosion (visual amount)	Surface color	Furnace ambient
350°C	as dep	oo	Pink	
	600°C, 2h	oooo	Pink	air
	650°C, 2hr	oooo	Green	air
	650°C, 2hr	oooo	Bright-pink	N_2
	700°C, 1hr	oooo	Green	N_2 (oxidation)
400°C	as dep	x	Green	
	450°C, 0.5h	x	Gray	
	600°C, 2h	x	Gray	Air
	650°C, 2hr	x	Gray-yellow	Air
	650°C, 2hr	o	Gray	N_2
	700°C, 1hr	x	Green-yellow	N_2(oxidation)

* Layer : a-Si/SiNx/SiO_2/wafer =100nm/300nm/500nm/Silicon wafer

applied to reduce the risk of VACNF etching/damage. The etching of Cr was done with a CR14S wet etchant for 130 seconds. Herein, to avoid the isotropic etch profile, no over-etching time was applied. The source and drain Cr patterns acted as a mask material for n^+ Si film etching process. For n^+ Si film etching, SF_6 and Ar plasma chemistry was used. The dry etch condition was 20 watts RF power, 2000 watts ICP, 10 mTorr pressure, and 15°C temperature. Since etch rate of n^+ Si film and SiN_x was determined to be ~10nm/sec and 7.5nm/min, respectively, 23 seconds etch time was applied to etch 100nm of doped silicon and 100nm of etch stop layer.

4.2.1.3.7. Passivation layer deposition and via hole etching

To passivate the channel region, a SiN_x layer was deposited as quickly as possible after the BCE process was finished using the standard SiN_x deposition condition. The thickness of the passivation layer was 300nm. To pattern via hole, the standard photolithography condition was used except, SPR^{TM} 220-3.0 photoresist was dispensed onto the wafer with 1500 rpm spinning speed for 60 seconds to get thicker photoresist. The resulting thickness of photoresist was 3.20 µm. For via hole etch, the target etch depth was 300nm for Source and Drain electrode contact, and 800nm for Gate electrode contact. Since fluorine based plasma does not attack the Chromium layer, longer etch time was applied to remove the silicon based residues on the metal pads completely. The etching condition was that 30 watts RF power, 2000 watts ICP power, SF_6 /Ar(45/1 sccm) gas, 10 mTorr, 15°C temperature. The etch rate was different for each thin films, and 10nm/sec for a-Si:H film and 7.5nm/sec for SiN_x film was roughly assumed, therefore a total of 90 seconds etch time was required. For 100% over-etching, 180 seconds etching time was applied to ensure electrical contact between the contact pads and the end of probe tips. Finally, in

order to evaporate moisture in devices and enhance electrical properties, the devices were annealed on hot plate for 10 minutes at 300°C.

The TFT-VACNF shown in figure 4-10 was fabricated without dehydrogenation process and had a 300nm thickness of source and drain Cr electrode thickness. Figure 4-10 represents the SEM images of TFT after fully fabricated with VACNF; (a) vertical view of TFT-VACNF array, (b) single TFT-VACNF with 30 degree tilted, and (c) single VACNF on the drain electrode with 30 degree tilted. From the images, though VACNFs were survived through the whole fabrication process, there were several defects due to hydrogen bubbles, which lead a pattern disconnection and film buckling. Moreover, the Source and drain electrode had a poor etch profile mainly due to Cr silicide formation during the VACNF growth which will be discussed in detail in subsequent sections.

Figure 4-11 shows the SEM images of TFTs with dehydrogenation process (500°C for 1hr); (a) vertical view of TFT array, (b) 30 degree tilted single TFT-VACNF, and (c) single VACNF on the drain electrode. From the images, even though the source and drain Cr electrode patterns still had a rough etching profile on the source and drain Cr electrode, it showed a few bubbles and defect sites and less buckling sites

4.2.3. Characterization of the first TFT-VACNF device process run

To characterize the TFTs, the gate voltage was swept from -20 V to 30 V at interval of 0.25 V. The threshold voltage was defined by the gate voltage, which reaches a maximum value of drain current at V_{ds} = 10.0 V. Figure 4-12 shows the representative transfer characteristics of TFT integrated with VACNF of TFT without dehydrogenation process and with 500°C, 1hr dehydrogenation process, respectively.

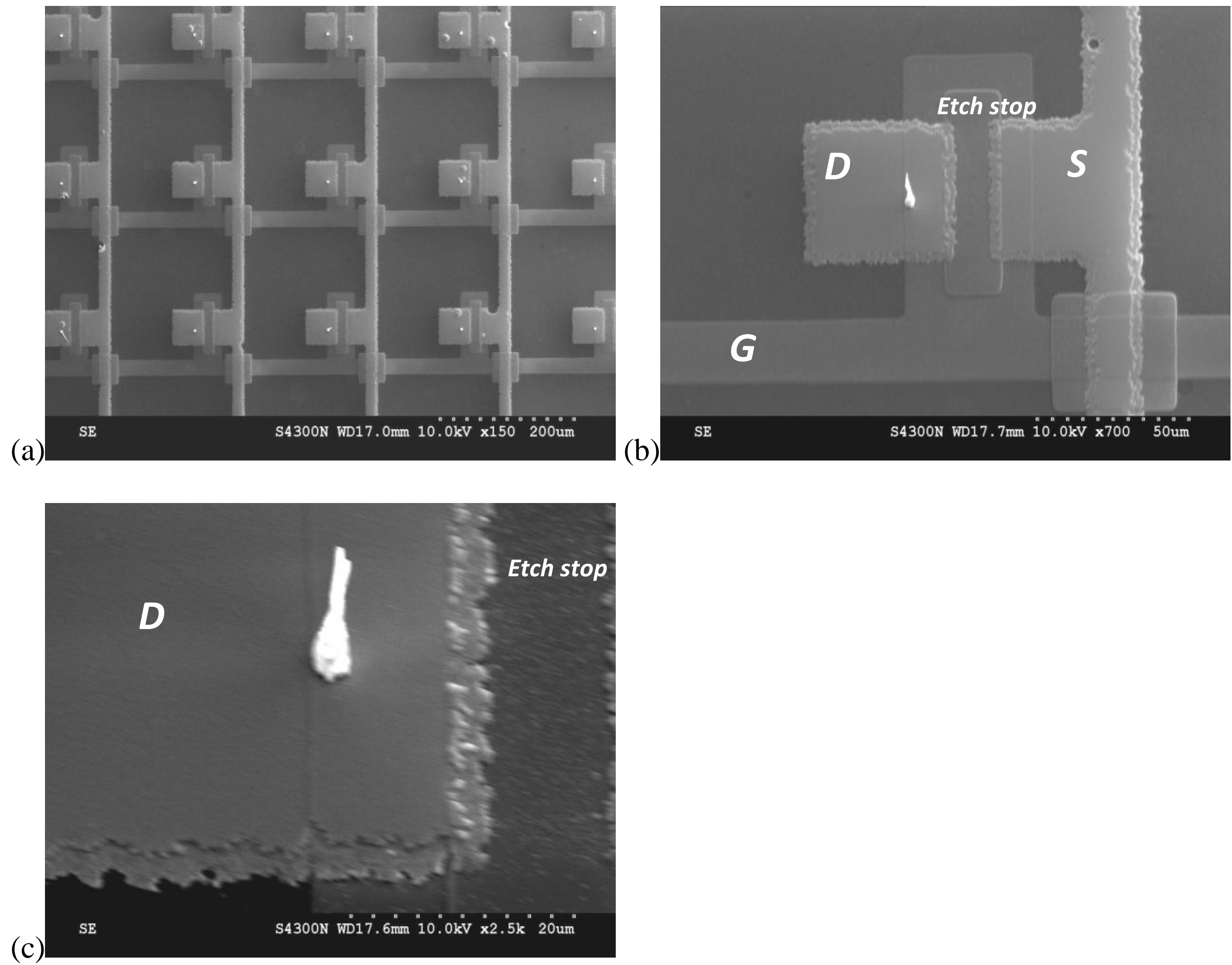


Figure 4-10. SEM images of TFT-VACNFs fabricated without dehydrogenation process. The thickness of S/D electrode was 300nm; (a) top down view of TFT array prior to source drain patterning, (b) 30 degree tilted single TFT-VACNF, and (c) VACNF on the drain electrode with high magnification

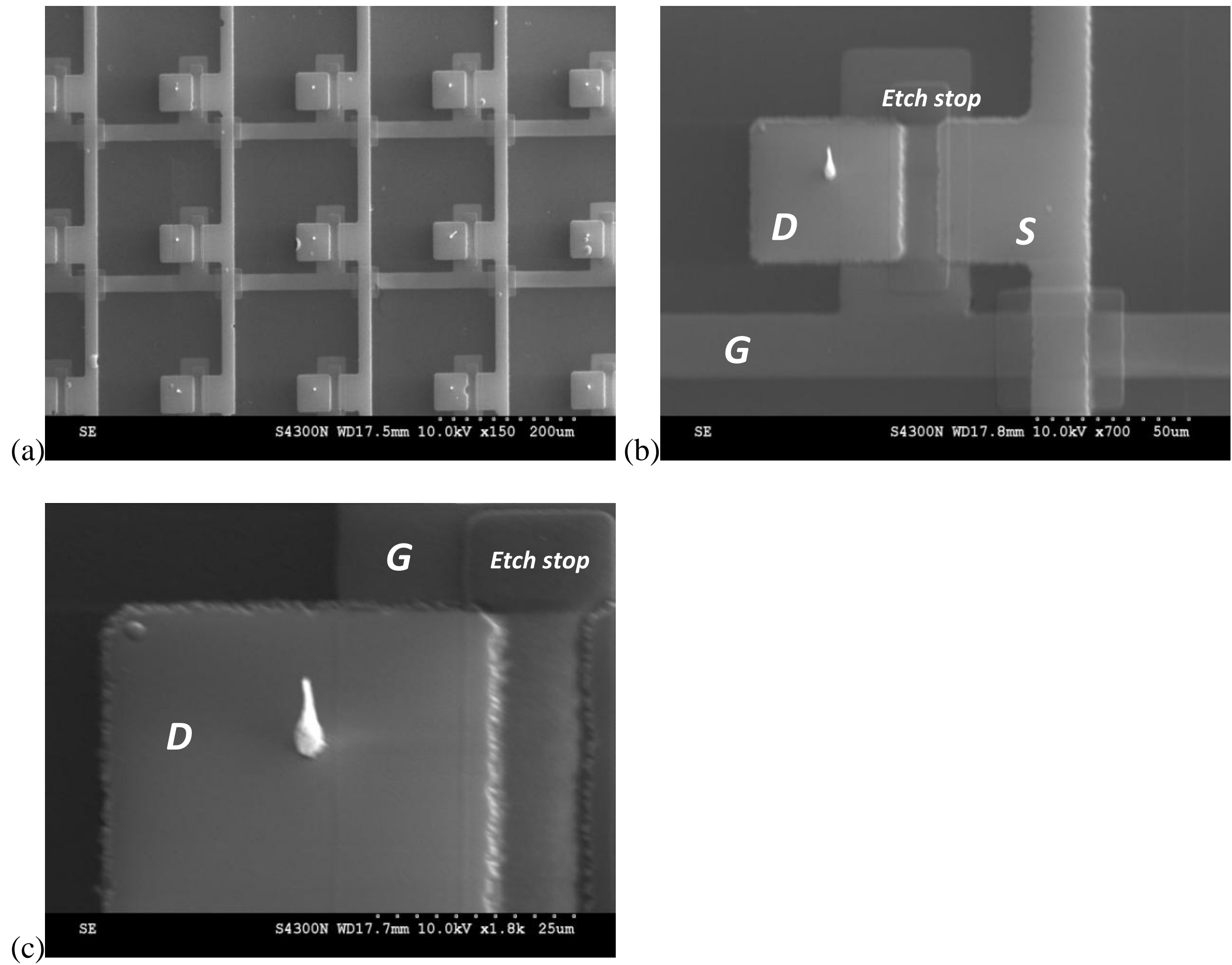


Figure 4-11. SEM images of TFTs integrated with VACNF with a 500°C dehydrongenation anneal; (a) top down view of TFT array, (b) 30 degree tilted single TFT, and (c) higher resolution image of single VACNF on the drain electrode

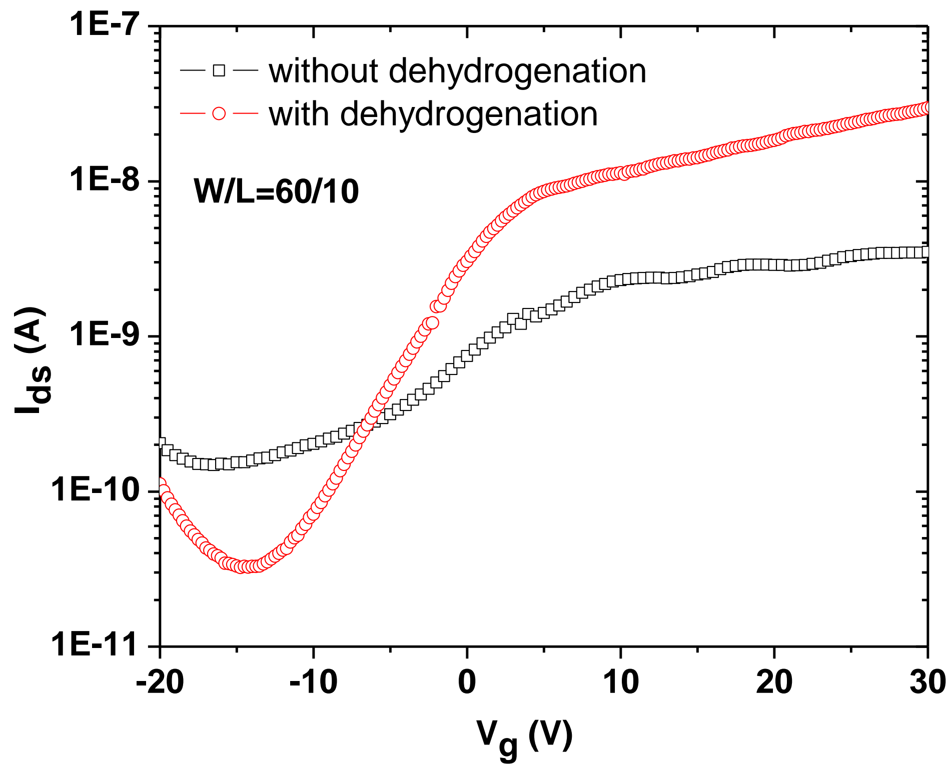


Figure 4-12. I_{ds}-V_g transfer characteristics of TFT-VACNF integrated device of the channel Width/Length (60/10); without dehydrogenation with 300nm source and drain electrode, and 500°C, 1hr dehydrogenated with 200nm source and drain electrode

As shown in the figure 4-12, the TFT-VACNF without the de-hydrogenation anneal has poorer transfer characteristics relative to the annealed TFT-VACNF. The calculated field effect mobility at channel width and length of 60 and 10 μm, respectively, from linear region of the I_{ds}-V_g graph was 0.32cm^2/Vsec; the on/off current ratio was ~10^3; the drain current (I_{ds}) appears saturated at Vg=2 V, however, transconductance (g_m) value was not showing the maximum value from the differentiated I_{ds}-V_g plot. It was surmised that the observed saturation of I_{ds} was originated from the high contact resistance of n^+ Si film. In other words, I_{ds} initially follows the transfer characteristics of the channel region, but as the current increases, the contact layer resistance limits the current rather than the channel resistance. The subthreshold swing (S), which is the voltage required to increase the drain current by a factor of 10, was also calculated to be 7.874 at V_g= -3.5 V. Subthreshold swing is directly proportional to the defect state in the SiN_x and a-Si:H film [102]. Several defects are formed during the fabrication process and they are mainly attributed from the etch stop layer processing since fluorine based wet etchant was applied. It has been reported that the tensile stressed of the top SiN_x film generates the defect density [57]. Furthermore the threshold voltage was shift to the left (V_T= -5V). During the dehydrogenation process, hydrogen is diffused out from the film. Hydrogen acts an important role to passivate the dangling bonds in the silicon network resulting in a threshold voltage shift decrease, and lower leakage current in the 'off' state [46]. As described earlier the dehydrogenation process degrades transfer characteristics of TFT, however, the dehydrogenation process was essential to minimize bubbles formed in the chromium layer during the high temperature VACNF growth process. Additionally, the leakage current in the 'off' state showed an anomalous rise in the leakage current similar to poly-crystalline based TFT which is due to

grain boundaries states or metal residues for silicon films crystallized via metal induced crystallization.

Previously deposited 1st, 2nd, 3rd run TFT showed a lower leakage current level below 10^{-11} and 10^{-12} A. However, the 1st run TFT-VACNF shows a higher leakage current at 'off' state, which was attributed to problems in the PECVD equipment which resulted in wafer sliding and necessitated that the gate dielectric, a-Si active layer and the etch stop layer each be deposited and unloaded to the loadlock chamber, while the chamber was cleaned and then re-loaded for the subsequent films. This problem was resolved using low curvature silicon wafers and by reducing the changing that occurred during the a-Si:H film PECVD deposition by adding He gas during deposition.

4.3. Fabrication of characterization of the second TFT-VACNF device process run

From the 1st TFT-VACNF integration run, several issues were addressed such as the need for via through holes for adequate charge dissipation during VACNF growth (as well as the general need for backside wafer cleaning for good conduction to the substrate holder), hydrogen bubble formation and dehydrogenation effects on the transfer characteristics of the TFT. To compensate these effects and simplify the fabrication process, a back channel etching inverted staggered structure thin film transistors (BCE-TFTs) were fabricated using SiN_x, a-Si:H, and n^+ Si film deposited in situ in the PECVD chamber.

4.3.1. Fabrication of the second TFT-VACNF device process run

For our intracellular probe applications, a bottom gate inverted staggered structure was adopted so the VACNFs could be integrated onto the drain electrode. Figure 4-13 illustrates the

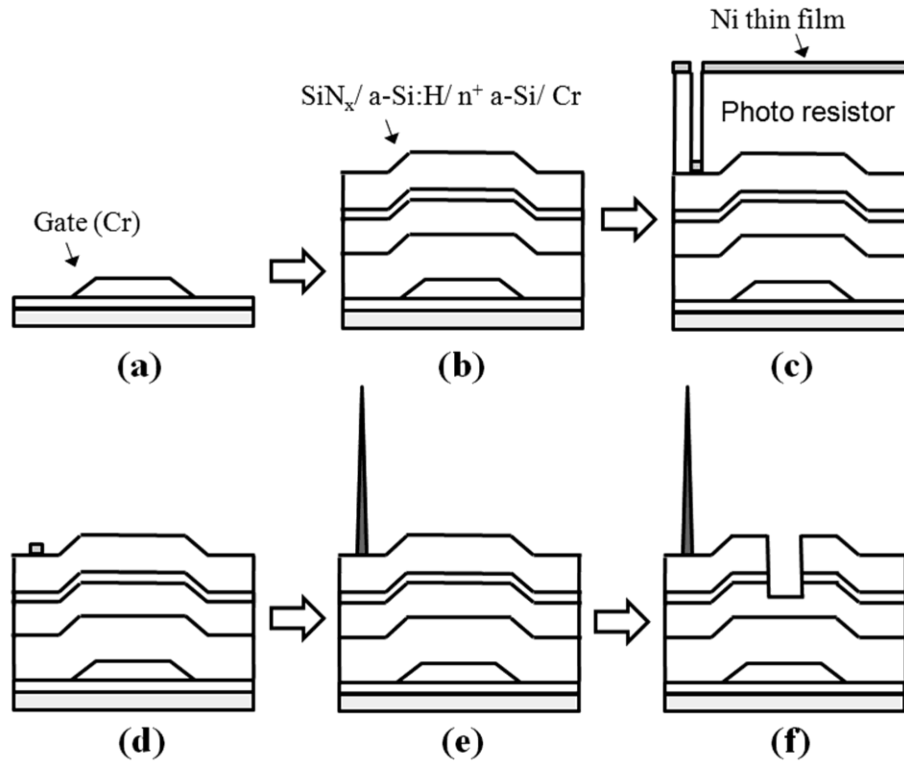


Figure 4-13. Schematic illustrating the processing sequence for the TFT-VACNF integration. (a) Cr film deposition and patterned for gate electrode, (b) a-SiN_x, a-Si:H, and n^+ a-Si deposition in situ using PECVD following Cr film for source-drain electrode deposited, (c) nickel dot patterns are formed on source-drain electrodes using conventional photo-lithography and Ni deposition by evaporation (d) the lift off process. (e) illustrates the VACNF growth on the nickel catalyst on the uniform chromium layer which is (f) subsequently patterned followed by the active layer back-channel etch process

schematic process flow for TFT and VACNF integration. Briefly, PECVD was used to deposit silicon dioxide (500nm) on Si wafer, Chromium (Cr: 100nm) was deposited and patterned with a Cr wet etchant. Silicon nitride (SiN_x: 300nm) gate dielectric, hydrogenated amorphous silicon (a-Si:H: 200nm) active layer, and doped amorphous silicon (n^+ a-Si:50nm) contact layer were all deposited by PECVD without breaking vacuum.

This process does not have an etch stop layer, thus the thickness of a-Si:H film was increased to compensate the margin of etching depth for back channel etching. Initial VACNF growth attempts resulted in bubble formation due to dehydrogenation from the SiN_x and a-Si:H layer deposited using SiH_4 gas in PECVD. Thus, hydrogen is present in the films [74,102]. For the 700°C processing dehydrogenation occurs and causes delamination bubbles. Thus, a pre-annealing dehydrogenation procedure (700°C, 1hr with 10°C/min ramp speed and 600°C, 1hr with 3°C/min ramp speed) was implemented to remove the hydrogen prior to depositing source and drain Cr layer. Another problem was the damage to top metallization and arcing for the growth due to inadequate conduction path for dc plasma current through source and drain electrode to contact clamps. To mitigate the arcing problem, eight contact holes were patterned around the edge region of the wafer and etched through the all the layers down to silicon wafer prior to the source and drain electrode film deposition. After deposition of these three layers, contact holes were etched using SF_6 and Ar plasma etching with relatively thick photoresist of 3.2µm. The other photolithography processes were followed by the 2nd standard process flow. The etching of contact holes was processed by reactive ion etching (RIE) with SF_6 and Ar plasma. The etch condition was that 30 watts RF power, 2000 watts ICP power, 10 mTorr pressure, 45 and 1 sccm flow rate of SF_6 and Ar, and 15°C temperature. 150 seconds etch time was applied to ensure the etch depth, not significantly considering etch profile.

To integrate the VACNFs with the TFT, the standard TFT process flow was slightly varied to accommodate the catalytic synthesis of VACNFs in a direct current-PECVD (dc-PECVD) process. To facilitate adequate grounding for dc-PECVD process, the VANCFs are grown on the blanket Cr source and drain layer (200nm). VACNF growth requires a catalyst film, thus ~50nm thick and ~ 1.5 micron diameter nickel "dots" are patterned onto the drain electrode area. After the nickel is evaporated and patterned via a lift-off process, the VACNFs are grown via a dc-PECVD process using a C_2H_2/NH_3 (85/200 sccm) mixture, 660 Watt (1 A, constant), 15 Torr pressure, 700°C temperature, 19 minutes with a target of ~ 20 μm tall fibers. Figure 4-14 shows the VACNF arrays and single VACNF integrated onto the TFT, which was pre-annealed at 700°C for 1hr with 10°C/min ramp up speed. As shown in figure 4-14, there are some defect sites due to the bubbles. It mainly caused by high ramp up speed (10°C/min) for pre-annealing procedure. Therefore, a reduced ramp up speed (3°C/min) and temperature was applied for pre-annealing process.

Figure 4-15 represent the VACNF arrays and single VACNF on the TFTs, which was prepared with 600°C, 1hr pre-annealing with 3°C/min ramp up speed. A few defects from bubbles are observed from the images and the height of the VACNF fiber was again ~22 μm. Next, the source and the drain were patterned similar to the gate electrode and the back channel (n^+ a-Si/a-Si) was etched using a RIE with SF_6/Ar plasma chemistry. Total etch depth of a-Si:H was 75nm with complete etching of 50nm n^+ a-Si film. After deposition of the passivation SiN_x (300nm), the electrode contact holes were etched using RIE with SF_6/Ar plasma. The images of fabricated TFT-VACNF devices are shown in figure 4-16

(a)

(b)

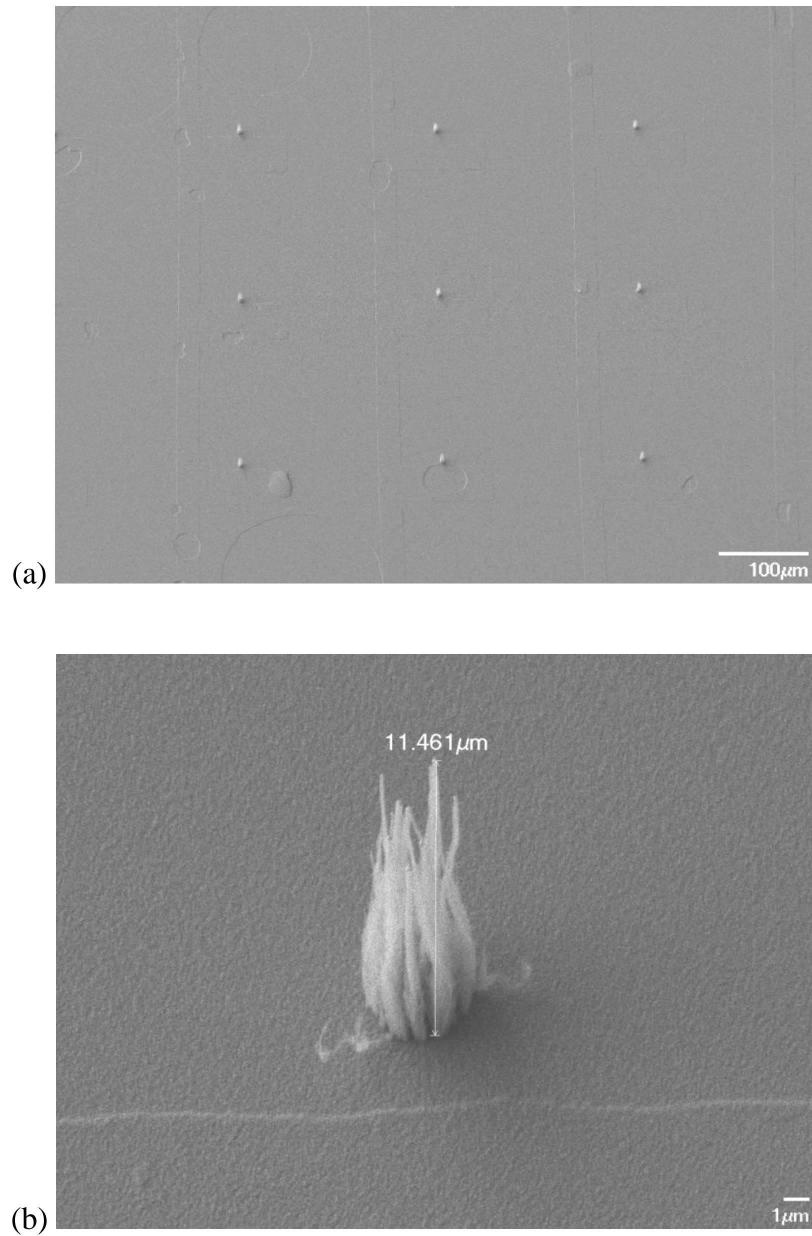


Figure 4-14. SEM images of (a)VACNF integrated onto the TFT (prior to source/drain patterning), which was pre-annealed at 700°C for 1hr with 10°C/min ramp up speed, and (b)single VACNF with ~ 22 μm tall (image was taken with 30 degree tilted)

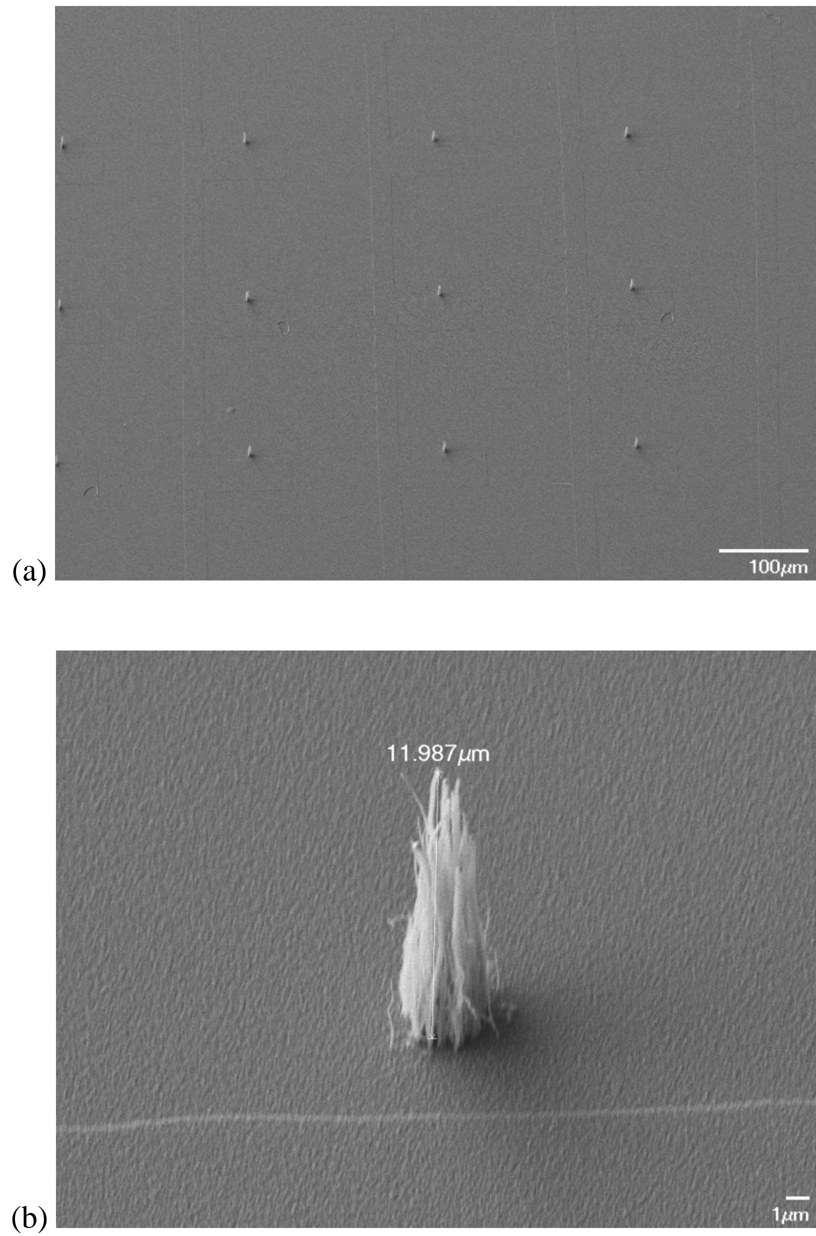


Figure 4-15. SEM images of VACNF integrated onto the TFT (prior to source/drain patterning), which was pre-annealed at 600°C for 1hr with 3°C/min ramp up speed, and single VACNF with ~ 22 μm tall (image was taken with 30 degree tilted)

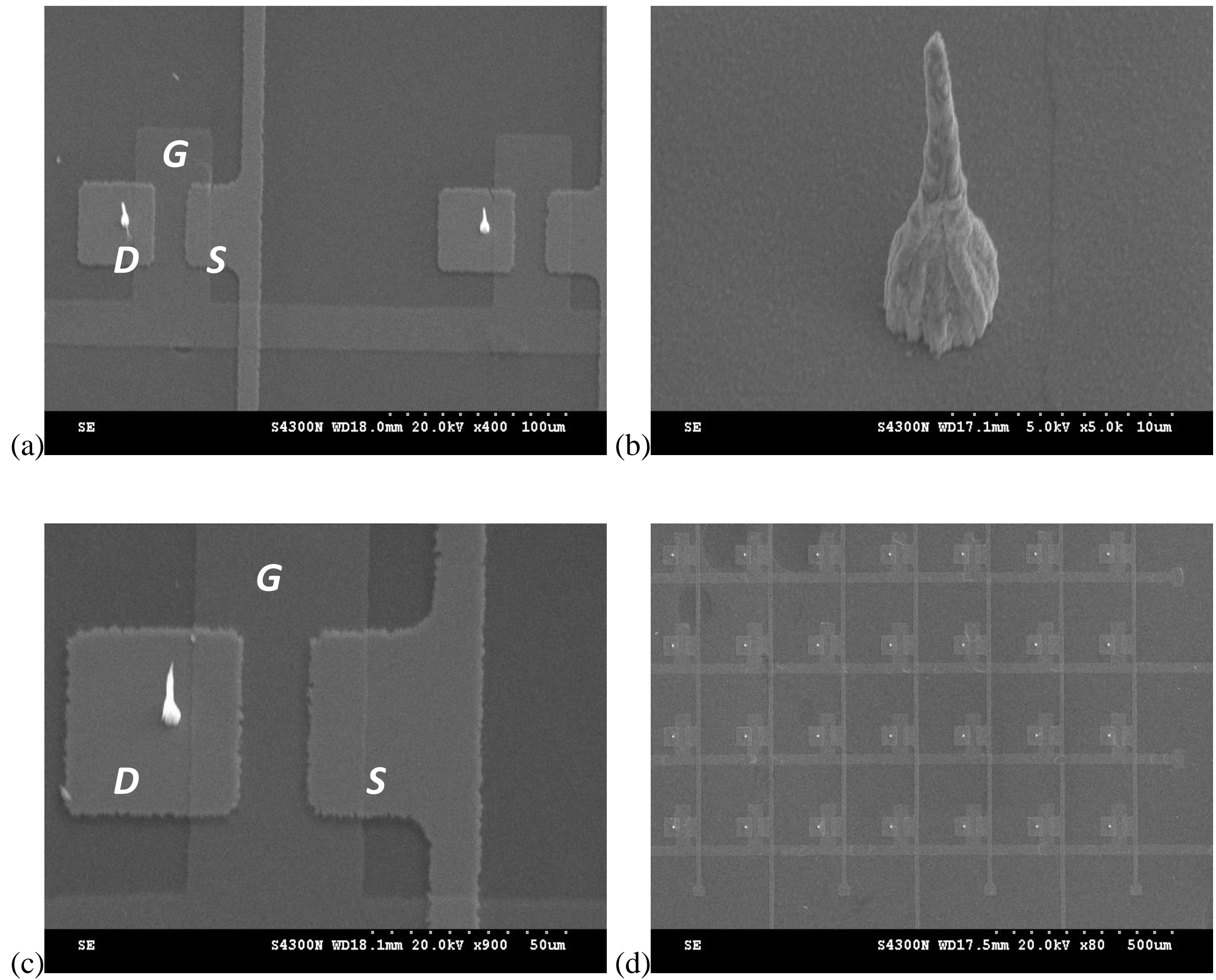


Figure 4-16. SEM images of TFT-VACNF device fabricated with back channel etching inverted staggered structure showing TFT-VACNF arrays and high resolution images of VACNF, which is half-covered with passivation SiN_x film (images were tilted 30° degrees)

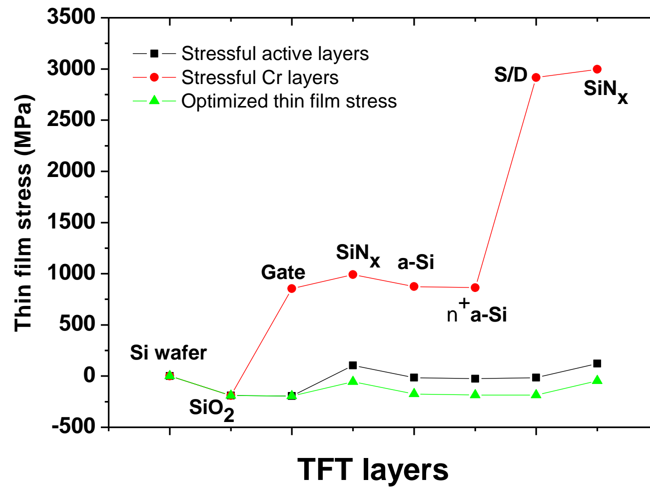
4.3.2. Characterization of the second TFT-VACNF device process run

One of the main obstacles in integrating the VACNFs with TFTs was appropriate control of thin film residual stress and subsequent thermal stress induced for the high temperature process. In particular, the Cr source and drain electrodes failed due to film delamination for the VACNF growth. It is well known that film delamination is related to the internal tensile stress [104]. Gleskova et al. has reported on TFT failure due to mechanical strain induced by high processing temperature [105]. Following the work of Misra et al. [96] we measured the stress of Cr films as a function of substrate bias. Without substrate bias during sputtering, Cr has a tensile stress of 1 ~2 GPa; however, when sputtered with a 5 watt substrate power the stress was reduced below 10MPa and subsequently survived the VACNF growth. Figure 4-17 shows the cumulative stress of each layer in the TFT (a) not optimized, high stress thin film layers of Cr metal, gate dielectric, and semiconductor layer, and (b) after optimization showing the cumulative stress is compressive. Figure 4-17 shows the overall stress was governed by Cr metal layer. The coefficient of thermal expansion, Poisson ratio, and Young's modulus of Cr are nominally 4.9 x $10^{-6}/^{o}C$, 0.21, and 279 GPa, respectively (CRC Handbook of Chem. Phys. (79th)), the total stress in the Cr source/drain film was calculated as follows

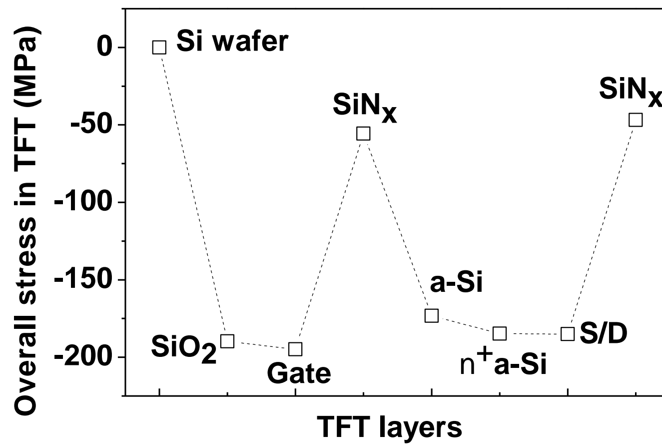
$$\sigma_{total} = \sigma_{residual} + \sigma_{thermal}(T)$$

$$\sigma_{thermal}(T) = \frac{F_f}{d_f w} = \frac{(\alpha_s - \alpha_f)\Delta T Y_f}{1-\nu_f}$$

Then, the calculated total stress of no biased stressful source/drain Cr film was ~2.74 GPa and the total bi-axial strain was ~0.78, while 5 watt biased low stress source/drain Cr film had ~0.70 GPa



(a)



(b)

Figure 4-17.The cumulative stress measured as a function of each thin film layer of the TFT device (a) with stressful Cr metal layer, stressful gate dielectric, and semiconductor layer (b) after optimization

total stress and ~0.19 total biaxial strain. The strain in source/drain Cr film was reduced ~75% by applying optimized substrate bias (5 watt) for sputtering. Consistent with the observed failure, the yield strength of sputtered Cr thin films is reported to be ~ 1.4 GPa [106].

To determine whether the silicon film crystallizes during the VACNF growth, Figure 4-18 shows a Raman and Figure 4-19 shows X-ray diffraction spectra of the silicon layer after VACNF growth and wet etching the requisite chromium layer. It is clear that the silicon crystallized and that a chromium silicide ($CrSi_2$) forms during the 700^oC dc-PECVD process. Formation of $CrSi_2$ has been reported to facilitate the silicon crystallization process [107]. Unlike metal induced crystallization process, Cr silicide act as medium to facilitate the silicon crystallization by breaking the weak bonds of silicon in the network. Additionally, Figure 4-20 shows the scanning microscope images of silicon after 700^oC, 19min in the dc-PECVD chamber process. The right image was taken after a 5 seconds "secco" etchant treatment to increase the contrast between the silicon and grain boundaries. From the images, the surface had several defects from $CrSi_2$, which was formed during annealing. Since $CrSi_2$ formed columnar structures in the matrix of silicon such as a fiber like structures along the direction of silicon solidification at poly-Si [108], it seems to be segregated into the grain boundary region.

To compare the electrical characteristics of the TFTs, TFTs with and without VACNFs were fabricated with the same fabrication process flow. Figure 4-21, figure 4-22, figure 4-23, and figure 4-24 shows the I_{ds}-V_g electrical transfer characteristics, output characteristics, transconducatnace (g_m), and subthreshold swing (S) of the TFT and TFT-VACNF device. Figure 4-21 compares the I_{ds}-V_g transfer characteristics of (a) TFT device fabricated without VACNFs, and (b) a completed TFT-VACNF device. The on/off current ratio, the off-state leakage current

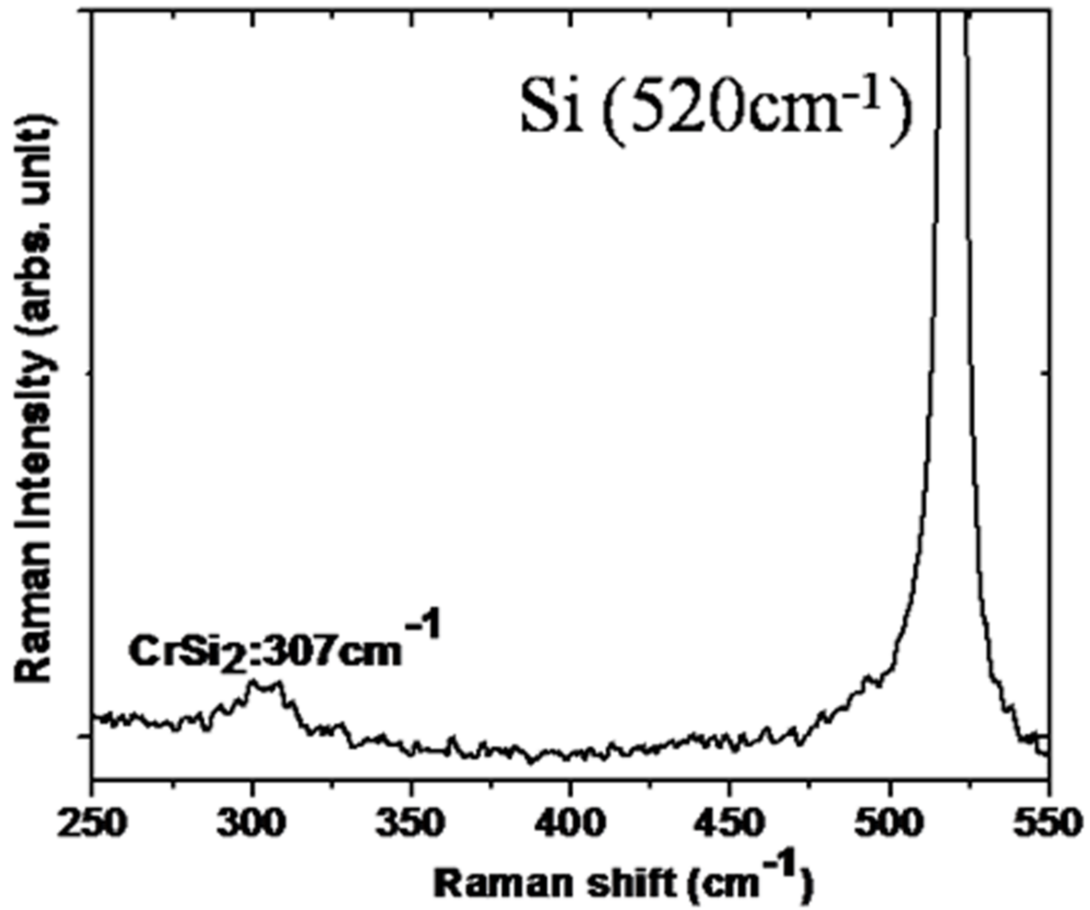


Figure 4-18. Raman spectra of silicon film after 700°C VACNF growth procedure. (top source and drain Cr film was removed after VACNF growth): 307cm^{-1} Raman shift corresponds to $CrSi_2$ formation

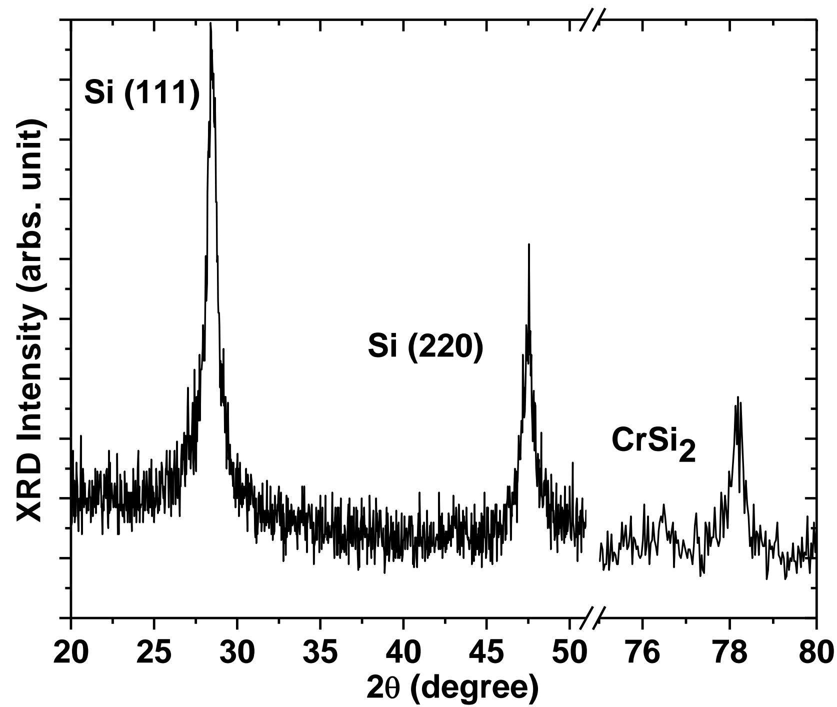
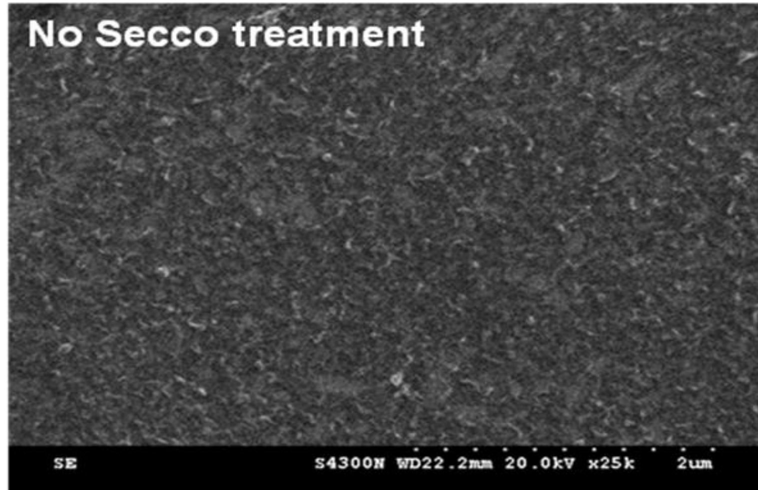


Figure 4-19. X-ray diffraction spectra of silicon film after 700°C VACNF growth procedure. (top source and drain Cr film was removed after VACNF growth): 78 degree peak corresponds to $CrSi_2$



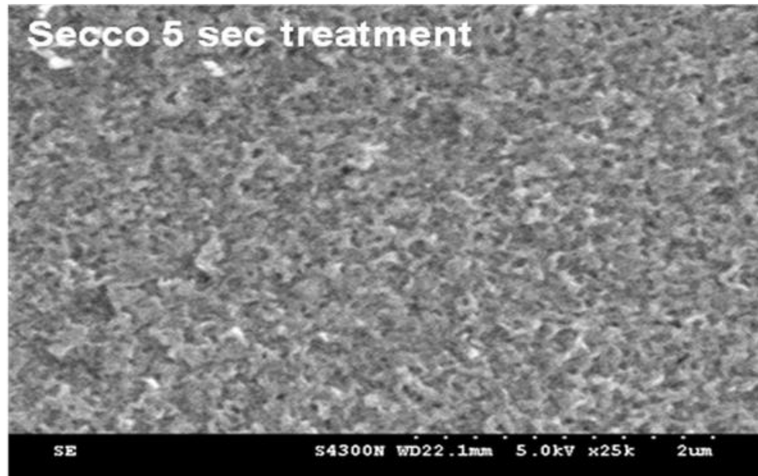


Figure 4-20. SEM images of silicon after VACNF process (700°C, 19min in dc-PECVD chamber), left image was taken with no treatment, and right image was taken after 5 seconds secco etchant

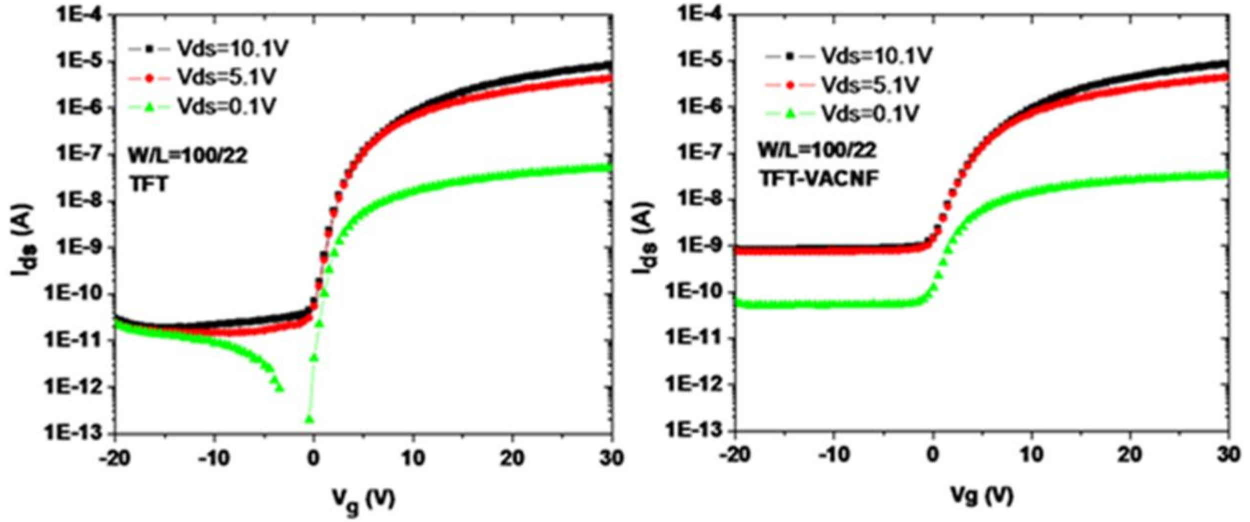


Figure 4-21. I_{ds}-V_g transfer characteristics of comparable TFT and TFT-VACNF

calculated from figure was ~ 10^5, ~ $3x10^{-11}$ A at V_{ds}=10.1V, respectively. The TFT-VACNF results from figure were ~10^4, ~$9x10^{-10}$ A at V_{ds}=10.1V, respectively. The field effect mobility for the TFT and TFT-VACNF devices were determined to be 0.49 cm^2/Vs and 0.27 cm^2/Vs, respectively, at V_{ds}=0.1V using linear portion of the I_{ds}-V_g plot. Furthermore, the threshold voltage was ~0 V for TFT, and ~2.5V for TFT-VACNF. To compare output characteristics, V_{ds}-I_{ds} plot was measured for both the TFT and TFT-VACNF device. As V_{ds} increased, the I_{ds} increased gradually, but the output of TFT was 1.5 times greater than that of TFT-VACNF device at V_{ds}=20 V when V_g was 10V. Following transconductance was calculated by differentiating the linear I_{ds}-V_g plot to find the value of maximum point. Transconducatance (gm) is expressed as

$$g_m = \frac{\delta I_{ds}}{\delta V_g}$$

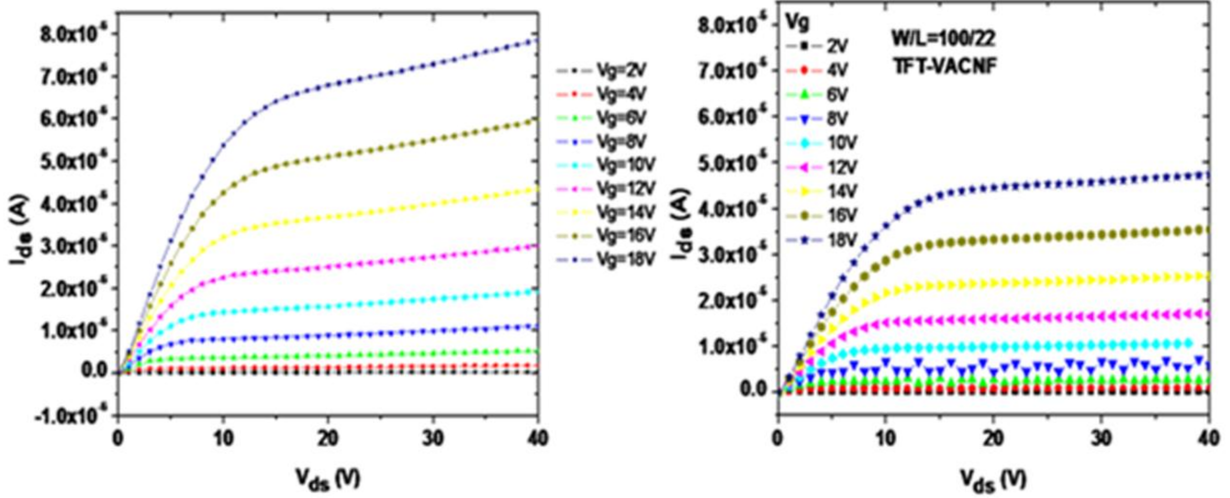


Figure 4-22. Output characteristics of comparable TFT and TFT-VACNF

, which is proportional to the induced charges at the channel region. For TFT, 2.20 x 10^{-7} at V_g=6V and for TFT-VACNF, 1.78 x 10^{-7} at V_g=6V, respectively. Moreover, the subthreshold swing (S) of the TFT and TFT-VACNF was calculated from log I_{ds}-V_g plot. S is expressed as

$$S = \left(\frac{\delta \log(I_{ds})}{\delta V_g} \right)^{-1}$$

where S is defined as the voltage required to increase the drain current as a factor of 10. Measured S of the TFT and TFT-VACNF device was 0.92 V/dec at V_{ds}=0.1V, and 1.87 V/dec at V_{ds}=0.1V, respectively. S is directly proportional to the defect state at the deep level [102]. From the figures, the characteristics of TFT-VACNF are degraded relative to the TFT devices without the VACNFs. The degradation of the device characteristics are attributed to the silicon and silicon nitride dehydrogenation, silicon crystallization, and silicide formation as briefly discussed below.

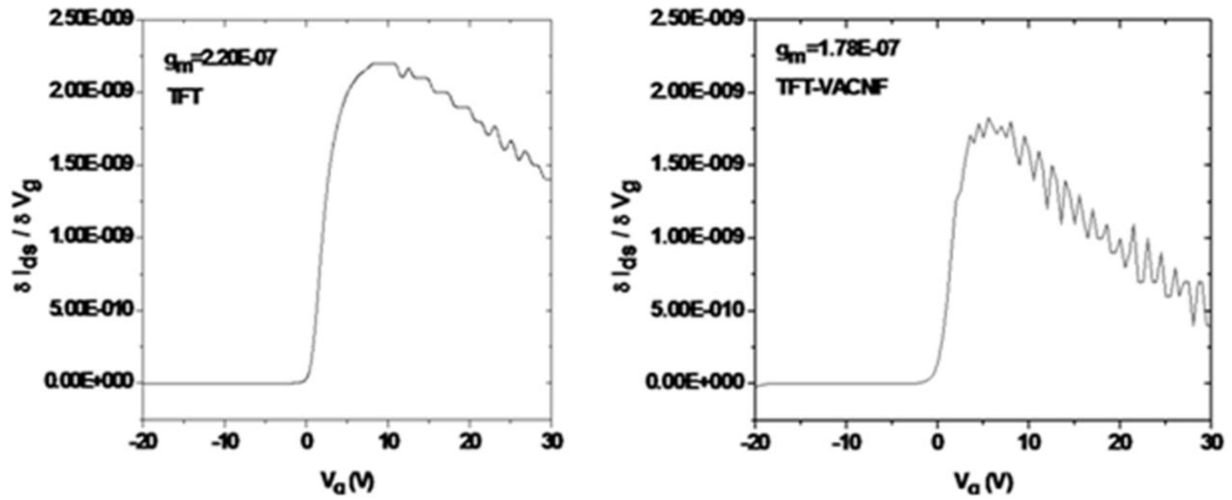


Figure 4-23. Transconductance (g_m) of comparable TFT and TFT-VACNF

The observed increase in the threshold voltage for the VACNF devices is attributed to dehydrogenated silicon and silicon nitride, which leads the increase of defect density in the bulk and at the interface [100,109].

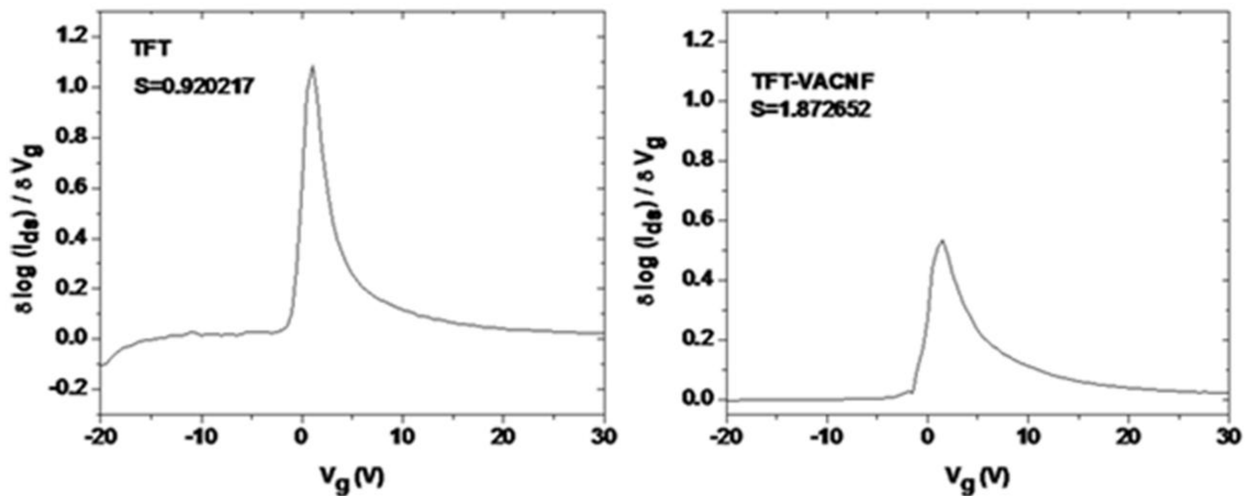


Figure 4-24. Subthreshold swing of comparable TFT and TFT-VACNF

It is surprising that the TFT-VACNF device has a lower mobility and higher subthreshold swing because the silicon was crystallized during the VACNF growth process. We surmise that the lower mobility is due to $CrSi_2$ segregated into the poly silicon grain boundaries, which act as scattering centers for electrons. High resolution scanning electron microscope (SEM) imaging (figure 4-25) revealed some high-brightness "spikes" in the channel region which we believe to be evidence of the $CrSi_2$ segregation. The higher off-state current for the TFT-VACNF device is also ascribed to segregated $CrSi_2$ as well as unpassivated grain boundaries due to dehydrogenation [61].

The fact that the reverse bias leakage is relatively constant instead of gradually increasing is different than typical poly-silicon TFTs and is not fully understood at this time. Figure 4-26 illustrates a cross-section view of the of channel region. The specific layers in the TFT device and evidence of the resultant $CrSi_2$ layer are labeled.

In summary a TFT array with integrated VACNF grown by Ni catalyst in dc-PECVD has been fabricated and characterized. To accommodate the dc-PECVD process, a contact via was etched to ground the pre-patterned S/D electrode to the silicon substrate. To reduce bubbles and film delamination from hydrogen entrapped from SiH_4 PECVD processing a dehydrogenation pre-anneal was performed prior to S/D metal deposit. Moreover, to minimize the residual stress in the S/D layer and prevent delamination during VACNF growth the internal stress of Cr film was controlled by applying a suitable (5W) substrate bias during sputtering. Though the device performance was degraded by VACNF growth process, this device provides great potential to perform electroanalytical function with a high spatial density of electrodes engineered to probe.

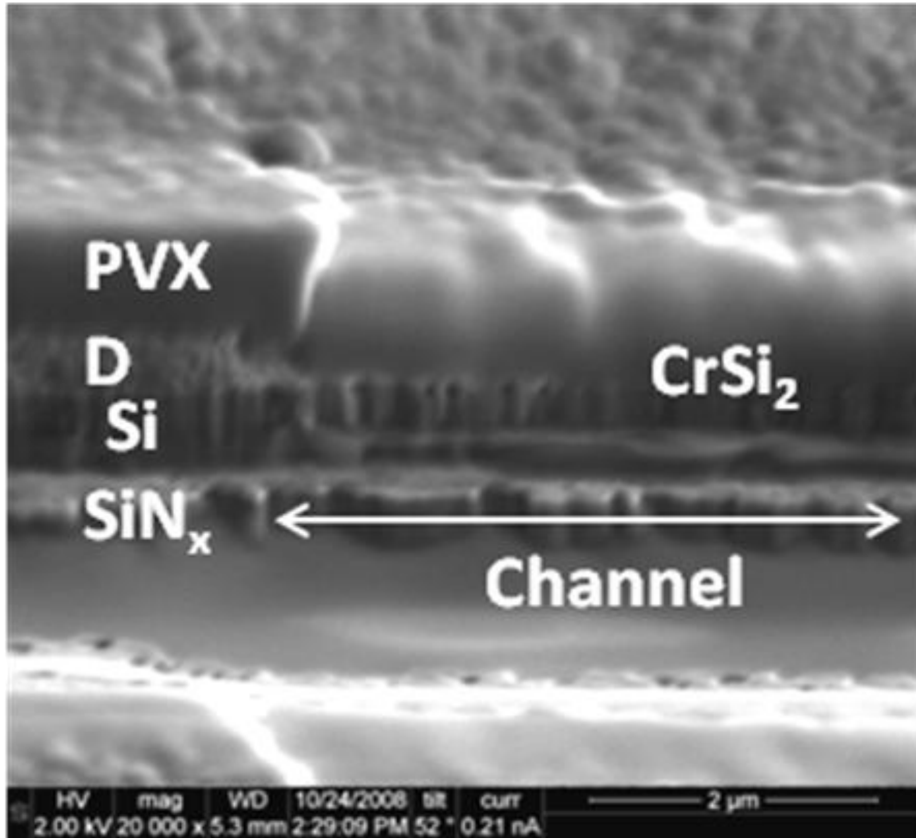


Figure 4-25. SEM images of TFT-VACNF device reveal the bright contrast of $CrSi_2$ layer formed at the Si-Cr interface

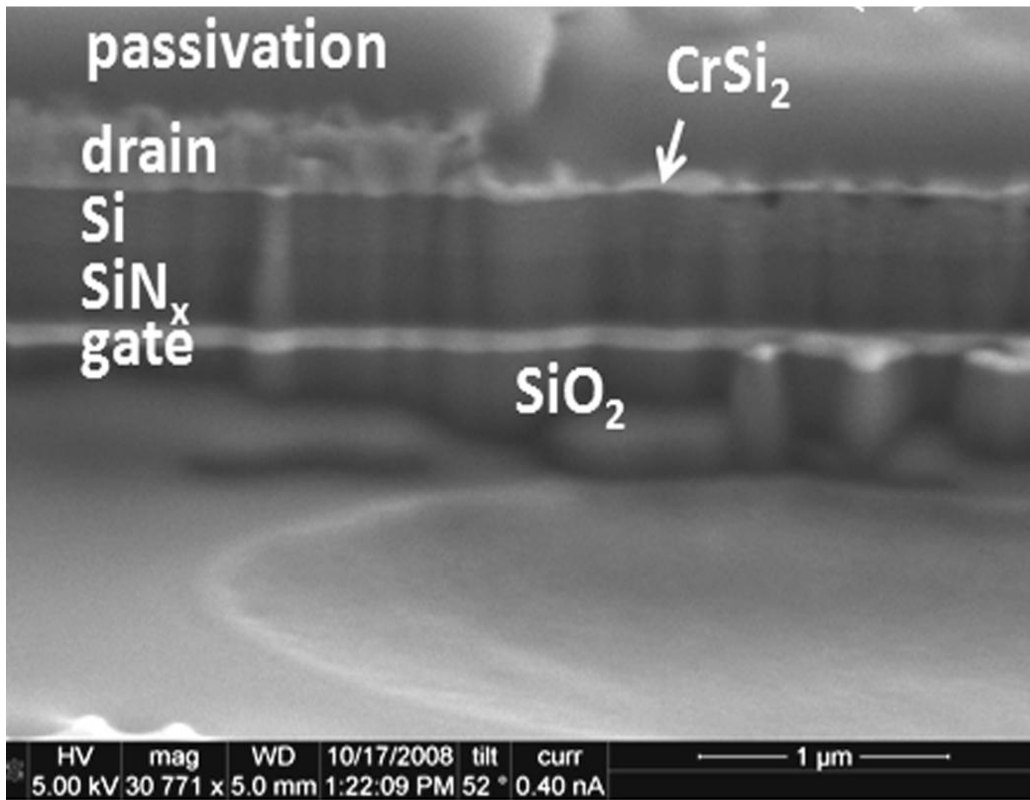


Figure 4-26. Focus ion beam milled cross-section image of the channel region

4.4. Characterization of the diffusion barrier layer effects on TFT-VACNF device

From the previous second run for TFT-VACNF device, Cr silicide formation was observed for dc-PECVD VACNF growth due to the high temperature process, which degraded the device characteristics by forming Cr silicide layer and/or spikes in the silicon network. Additionally, poor etching profile at source and drain patterning was obtained due to Cr silicide. To prevent these deleterious effects, a diffusion barrier layer was deposited between Cr layer and Si layer. Other fabrication process steps were the same as the second process run of TFT-VACNF device.

4.4.1. VACNF growth test

To prevent the Cr diffusion into the silicon network and the Cr silicide formation, diffusion barrier layers of Molybdenum (Mo) and Tungsten (W) were used since the silicide formation temperature of Mo and W is known as over $1000^{o}C$ and $900^{o}C$, respectively. In addition to the stability at high temperature process, Mo and W could be etched in fluorine based dry etching process such as SF_6 and CF_4 gas as well as wet etchants.

4.4.1.1. Experimental

To deposit Mo and W, Radio Frequency (RF) magnetron sputtering system, AJA 2000, was used. Following previously published work the deposition condition of Mo was 200 watts RF power (264 Volt), 25 sccm of Ar flow rate, 8 mTorr pressure, and room temperature [110]. The measured deposition rate of Mo was 5nm/min and sheet resistance of 43.76 ohm/sq. To deposit ~20 nm thickness, 4 min deposition time was applied and the resulting film resistivity was $0.88\text{x } 10^{-5}$ ohm-cm. The deposition condition of W film was 200 watts RF power (326 Volt),

15 watts (166 Volt) substrate power, 25 sccm of Ar flow rate, 8 mTorr pressure, and room temperature resulting in a 3.5nm/min deposition rate. The measured sheet resistance of W film was 14.42 ohm/sq. To deposit 20 nm thickness, 5.7 minutes deposition time was applied and the resulting film resistivity was 0.29 x 10^{-5} ohm-cm. To test VACNF growth on multi-layered Cr/Mo and Cr/W, 300nm SiO_2 buffer layer was deposited on a bare silicon using the standard process. Next the wafer through vias were patterned and etched via a BOE 6:1 wet etchant. 20nm Mo and W films were deposited onto separate contact hole patterned buffer/Si wafers followed by a 200nm thickness of low stress Cr film. Ni dot patterns were formed using conventional photolithography, Ni film evaporation, and lift-off process. Finally VACNF growth was performed using the optimized conditions.

4.4.1.2. Results and discussions

Figure 4-27 shows the VACNF growth on Cr/Mo and figure 4-28 shows the VACNF growth on Cr/W wafer. Both cases show that VACNFs were grown well on the multi-layered top metal film. Following the growth, etching tests were processed to ensure the back channel etching process. Initially, Cr film was patterned with conventional lithographic work and etched by CR14S, Cr wet etchant. For Cr/Mo wafer, both Cr and Mo films were completely etched away after 3 minutes etching time while W film was not etched in Cr wet etchant for the Cr/W wafer. To avoid the additional dry etching process, the Mo film was chosen to be used as diffusion barrier layer with 20 nm thickness.

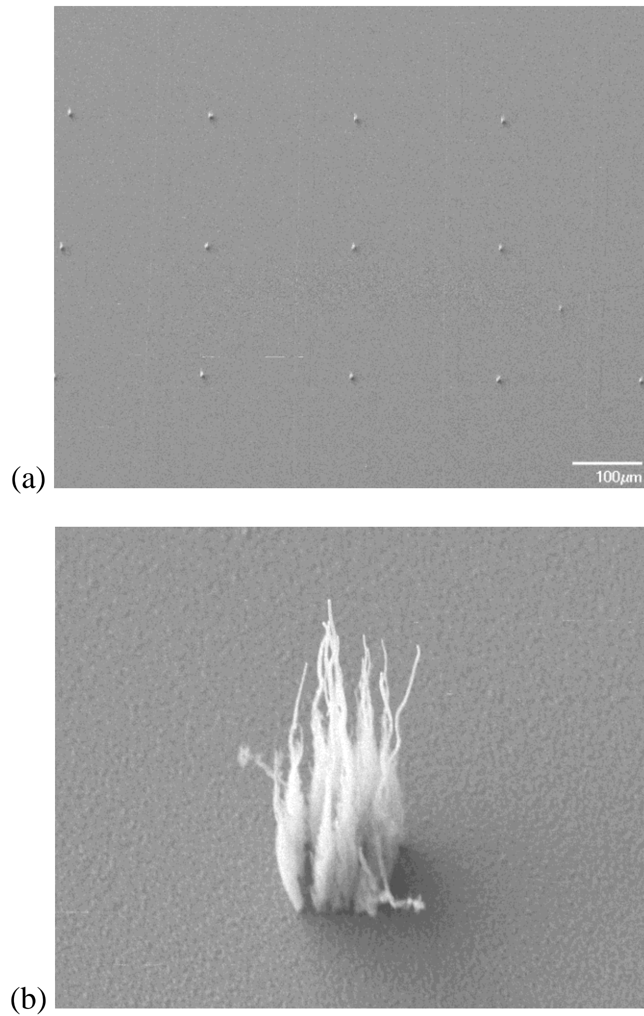
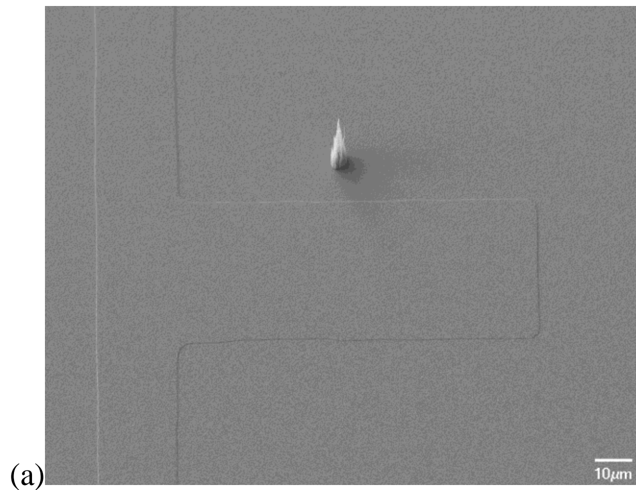


Figure 4-27. SEM images after VACNF growth test on $Cr/Mo/SiO_2/Si$ wafer structure. Prior to Mo film deposition, wafer contact holes were patterned

(a)


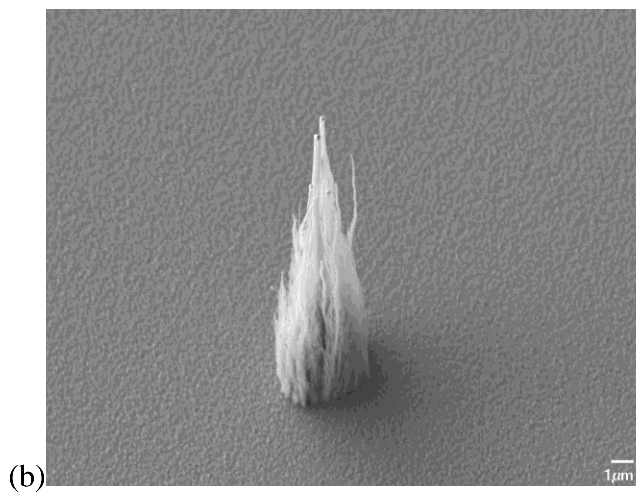
(b)


Figure 4-28. SEM images after VACNF growth test on $Cr/W/SiO_2/Si$ wafer structure. Prior to W film deposition, wafer contact holes were patterned

4.4.2. Fabrication of diffusion barrier layer in TFT-VACNF device

The fabrication flow for the third run of TFT-VACNF was the same as the second run of TFT-VACNF device. After deposit SiO_2 buffer layer (300nm), low stress gate Cr film was deposited on patterned using CR14S, Cr wet etchant. Following SiN_x (300nm), a-Si:H (200nm), and n^+ Si (50nm) films were deposited in situ in PECVD. Then pre-annealing process (600°C, 1hr with 3°C/min ramp) was applied to prevent the bubble formations and contact holes were formed to make a current path for dc-PECVD process. Then, a Mo film (20nm) and low stress Cr (200nm) films were deposited by RF magnetron sputtering. Ni dots were patterned with conventional lithography and Ni film (50nm) was deposited by evaporation, followed by a lift-off process in acetone for 1 hour. VACNFs were grown in dc-PECVD chamber with a condition of C_2H_2/NH_3 (85/200) gas flow, 15 Torr, 1 Ampere current, and 700°C temperature for 19 minutes. Figure 4-29 shows the grown VACNFs on TFT structure. As shown in the figure 4-29, there are defect sites, which were originated from the dehydrogenation process. Previously, in the same dehydrogenation process, less bubble were observed. It is surmised that the furnace status has been changed as the fuse and elements were replaced in between process runs. However, for device operation and testing, there were plenty of un-affected devices.

To pattern the source and drain electrode, the 2nd standard photolithography process was used as described previously. The etching of both Cr and Mo pattern was done using CR14S Cr wet etchant for 3 minutes. To etch the n^+ Si layer, an SF_6 and Ar plasma was used. The dry etch condition for 50nm etching was 20 watts RF power, 2000 watts Inductive coupled plasma (ICP), and 10 mTorr pressure, 15°C temperature. Even though 30 watts RF power was typically used, to reduce the risk of over-etching 20 watts RF power was adopted. Since the etch rate of n^+ silicon

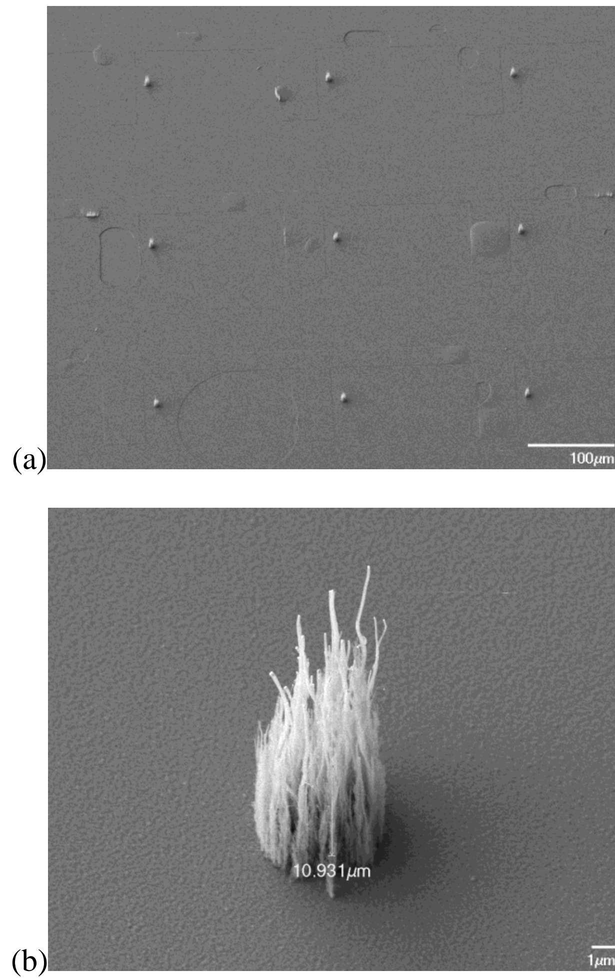


Figure 4-29. SEM images after VACNF growth on Cr/Mo electrode film on inverted staggered TFT structure. Prior to depositing the Cr and Mo films, contact via holes were patterned and dehydrogenation process was done at 600°C for 1 hr

was ~10 nm/sec at 30 watts RF power, 10 seconds etch time was applied initially. However, even at 20 watts RF power, ~300nm etch depth was measured. The etch rate was ~ three times faster than the tested etch rate. This resulted in an over etch through gate dielectric layer (n^+ Si:50nm, Si:200nm, gate dielectric SiN_x:50nm). Thus there was no active layer on the channel region and the devices failed.

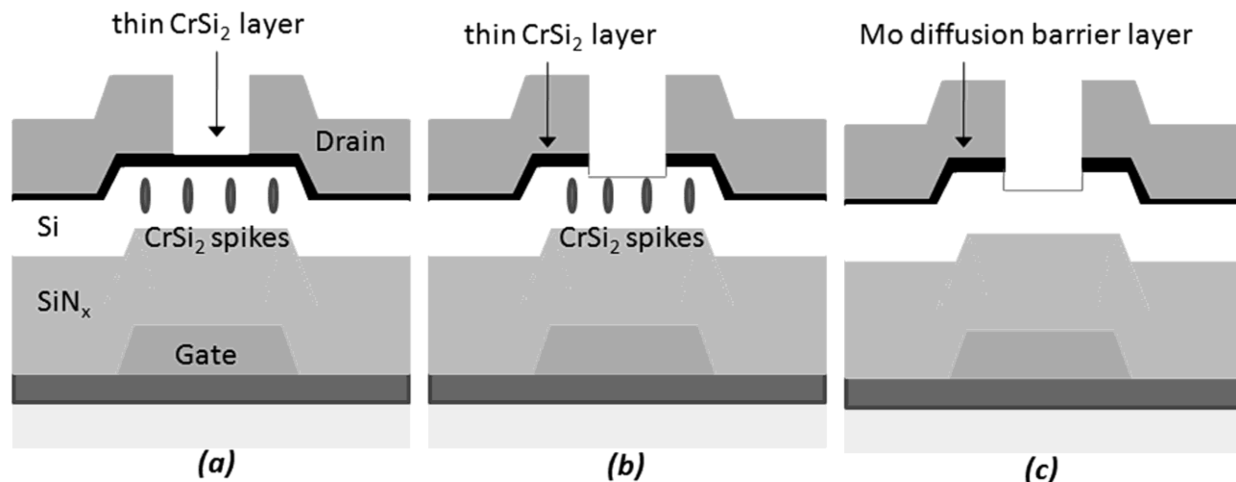
Therefore, to confirm the effectiveness of Mo diffusion barrier layer, a simple test structure was fabricated. All fabrication conditions of each layer were the same as the TFT-VACNF device wafer except the ohmic contact n^+ Si layer. The buffer SiO_2 (300nm) film was deposited onto the Si wafer following by the gate Cr (100nm) which was deposited and patterned. Then gate dielectric (SiN_x:300nm)/active (a-Si:H:200nm) films were deposited by PECVD in situ. Prior to depositing the source/drain electrode (Cr:200nm), the contact through via hole process and dehydrogenation process (600°C, 1hr with 3°C/min ramp) were done. Then the standard VACNF growth was performed to confirm adequate VACNF growth and to compare the role that the diffusion barrier has during high temperature process. After growing VACNF, the source and drain electrode (Cr/Mo) was patterned with CR14S wet etchant and passivation SiN_x(300nm) was deposited by PECVD and the contact vias were photolithographically patterned and etched.

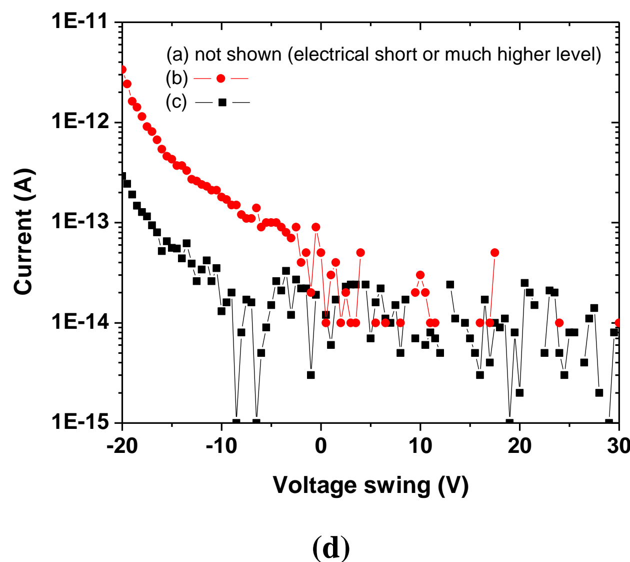
4.4.3. Characterization of diffusion barrier layer in TFT-VACNF device

The main source of the leakage current is comprised of current flowing between gate and drain electrode and current flowing between source and drain electrode. For the TFT-VACNF devices two scenarios were observed when testing the fabricated devices: 1) a continuous Cr-silicide layer would effectively short out the source and drain layer and cause the current to reach

the limit of the probe station (failed devices); or 2) the chrome silicide layer in the channel region was adequately etched and successful transfer characteristics could be measured. For the functional devices there still appears to be a higher leakage current relative to the TFT devices without the VACNFs. This higher leakage was attributed to the silicon crystallization as well as metal residue in the silicon active layer. Figure 4-30 (a),(b), and (c) illustrates the schematic cross-sectional view of the channel region: (a) when the Cr silicide layer formed at the interface between Cr and Si was not etched completely, (b) thin Cr silicide layer was etched, but Cr or Cr-silicide residues remains in the channel region, and (c) for the Cr-Mo dual source drain layer which acts as a diffusion barrier layer to prevent the formation of Cr silicide in the channel region. To explore the lateral current flowing along the channel region, voltage was swept between source and drain metal pads. Figure 4-30 (d) shows the measured current between source and drain metal pads as a function of swing voltage with or without diffusion barrier layer (Mo) of high temperature processed TFT-VACNF device. For case (a), I-V characteristic was not shown since the current level was over the limit of the I-V measurement equipment or it showed very high current level. For case (b), I-V characteristic of TFT-VACNF without Mo diffusion barrier layer was obtained from re-measureing the 2nd run TFT-VACNF device. The leakage current in this device is higher than the device without the VACNFs because the high temperature VACNF crystallizes the silicon and causes the Cr to diffuse into the channel which creates a density of states near the mid-gap which de-populate at higher voltages. However, case (c) with diffusion barrier layer, less current flow between the source and drain is observed relative to the Cr-only source/drain device.

To confirm, the effectiveness of diffusion barrier layer, Mo, X-ray diffraction spectra of the silicon layer after VACNF growth and wet etching the requisite Cr/Mo layers were examined.





(d)

Figure 4-30. Schematic illustration of TFT-VACNF device (a) thin Cr silicide layer formed and not etched during back channel etching at the interface and Cr silicide spikes formed in the channel region, (b) Cr silicide residues remains in the channel region, (c) Using Mo diffusion barrier layer, no Cr silicide was formed, and (d) Source-drain current vs. voltage swing on the channel region with or without Mo buffer layer after the high temperature VACNF growth process.

Figure 4-31 compares the X-ray diffraction spectra of the silicon layer of the single Cr source/drain layer and the dual Mo/Cr source/drain layer after VACNF growth (after a requisite wet etch strip of the passivation and Mo/Cr layer on half of the test structure substrate) It is clear that no Cr silicide has been formed with Mo diffusion barrier layer during high temperature process. And without $CrSi_2$, reduced intensities of crystalline silicon characteristic peaks were observed since the Cr silicide was reported to enhance the crystallization process [107]. Focus ion beam milled scanning electron microscope (SEM) imaging (figure 4-32) showed no significant silicide layer was formed on the channel region with Mo diffusion barrier layer. It is interesting to note however, the formation of a slight amount of Mo silicide ($MoSi_2$) was observed [111], which apparently does not facilitate the silicon crystallization as much nor does the residual $MoSi_2$ affect the leakage current as much. Thus the XRD results indicate that thin Mo film acts as a diffusion barrier for Cr-silicide formation and the I-V results indicate that it reduces the leakage current of the relative to the single Cr source/drain layer.

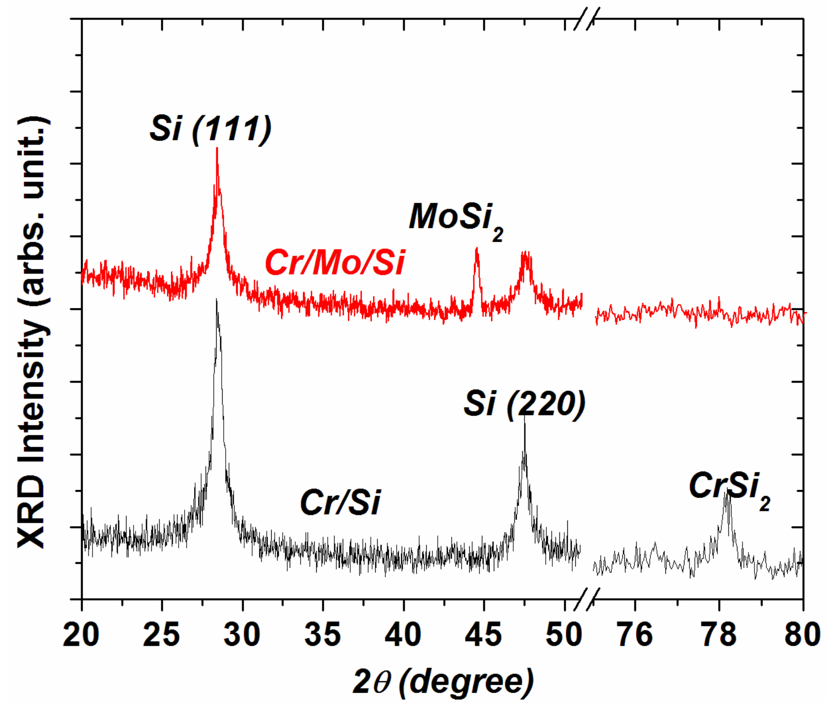


Figure 4-31. Normalized X-ray diffraction spectra of silicon films after VACNF growth with or without Mo diffusion barrier layer (XRD spectra were scanned after top passivation and source drain metal layers were wet etched, respectively)

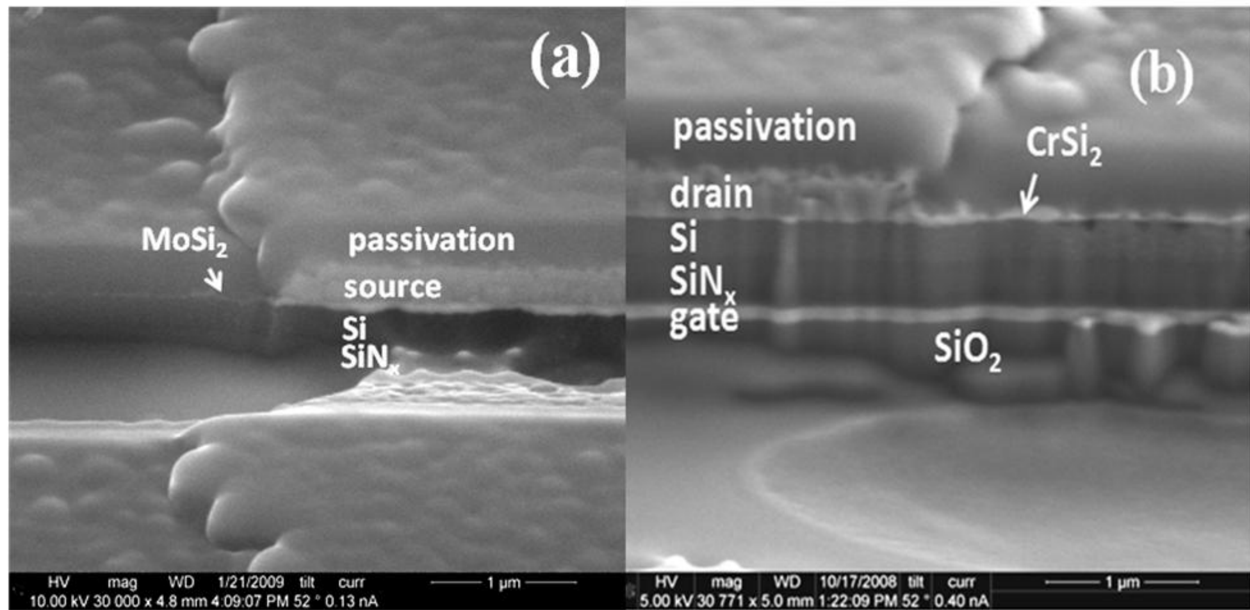


Figure 4-32. Focus ion beam milled SEM images of TFT-VACNF device (a) with Mo diffusion barrier layer, slight amount of $MoSi_2$ layer was formed, and (b) without Mo diffusion barrier layer, significant amount of $CrSi_2$ layer was formed at the Si-Cr interface during high temperature processing

5. Conclusions

In this dissertation vertically aligned carbon nanofibers were integrated with thin film transistor array. Potential applications for the active addressed VACNFs include bidirectional interfacing to provide intercellular probing as well as a multidimensional separation platform. Material characterization was performed to optimize the fabrication of a bottom gate TFT and TFT-VACNF device. For the gate and source/drain metal electrode films, low stress Cr was deposited with 5 watt substrate power during sputtering to reduce the biaxial tensile stress in the as-deposited film. A SiN_x gate dielectric layer was deposited by PECVD which resulted in a high breakdown strength, high capacitance, and low stress film. The low stress SiN_x film was achieved by applying 2 sccm flow rate of NH_3 gas. The active layer of amorphous silicon film was deposited by PECVD, which was optimized to have a compressive stress to compensate the low cumulative stress in the TFT. To enhance the solid phase crystallization process of the amorphous silicon active layer, capping layers were deposited onto the sputtered a-Si film. Using the difference of thermal coefficients of expansion (TCE), SiN_x and Al_2O_3 capping films were used to induce tensile stress into the a-Si film for annealing. The high TCE capping layer enhanced the crystallization process by enhancing the silicon mobility. For sputtered doped amorphous silicon films, lower resistivity of the film was achieved with lower temperature, shorter distance, and higher substrate bias as these parameters minimize the amount of oxygen incorporated into the film.

To fabricate the TFT device, Cr metal film was deposited by RF magnetron sputter and gate dielectric, active semiconductor, and passivation layers were deposited by PECVD. The channel passivation structure with an etch stop layer and back channel etch structures were

fabricated both fabricated and compared. The optimum TFT device (using the back channel etch structure) had a ~0.5 cm^2/Vs field effect mobility, ~10^5 on/off ratio at V_{ds}=0.1V, leakage current of 10^{-10} A at V_{ds}=10.1V, and nearly zero threshold voltage (V_{th}). It also showed 3.0 x 10^{-9} transconductance and 0.90 subthreshold swing.

To integrate TFT-VACNF, the TFT fabrication process was slightly varied. To give adequate grounding for the wafer, contact through via holes were patterned prior to depositing the source/drain metal to accommodate the direct current PECVD (dc-PECVD) which was used to grow VACNF on the drain electrode region. To reduce hydrogen bubble formation due to the hydrogen entrapped during the PECVD a-Si:H film (from the SiH_4 gas), a pre-annealing (dehydrogenation) processes was introduced prior to source/drain metal deposition. The most important requirement to integrate the TFT-VACNF device was adequate control of the thin film stress. A thin film transistor array with integrated VACNF grown in dc-PECVD has been characterized and fabricated with an optimized stress level for each thin film. The Cr film stress was optimized by applying adequate substrate power (5 watt), and SiN_x film stress was optimized by increasing the NH_3 gas flow. The resultant device characteristics of the VACNF integrated device compared favorably with comparable TFT devices without VACNFs. Specifically the relevant parameters for the TFT device compared to the TFT-VACNF device, respectively, were: field effect mobility ~0.50 cm^2/Vs versus ~0.29 cm^2/Vs; on-off current ratio ~10^5 (V_{ds}=0.1V) versus ~10^4 (V_{ds}=0.1V); leakage current ~10^{-10} A (V_{ds}=10.1V) versus ~10^{-9} A (V_{ds}=10.1V); threshold volage ~0 V versus ~2.5V;subthreshold swing ~0.90 versus ~1.57.

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Appendices

Appendix A: Run sheet for TFT-VACNF processing (CHP-TFT)

TFT-VACNF (CHP- TFT)

Layer	Process	Equipment	Condition	time	remark
Buffor	PECVD (SiO2:500nm)	PECVD (oxford) [Silicon dioxide]	RF:20W SiH_4/N_2O(85/157) Pressure: 1000 mTorr Temp: 350°C	7min15sec	Stress:-180MPa
Gate	Deposition (Cr:100nm)	Sputter (#4)	RF: 200W(420V)/5W(**138V**) Gas: Ar(25) Pressure: 5mT Temp: 200°C	25min	4nm/min R.S:1.21~1.29 Stress:~0 Mpa
	Cr pattern	spinner contact aligner (vaccum mode)	SPR3.0 (w primer) 3000 rpm, 60 sec PreBake: 115°C, 120 sec Exposure time=40 sec PEB: 115°C, 120sec Develop:60 sec		PR = 2.75µm (aligner illumination density: ~9.98)
	descum	Technics RIE	RF:400W Gas: O_2(10 sccm) Pressure: 150mTorr	30sec	
	Cr etch	wet etch	Cr 14S etchant (R.T)	End+20sec	
	PR strippin	stirpper	20min		
	ashing	Technics RIE	RF:400W Gas: O_2(10 sccm) Pressure: 150mTorr	2min	
Active & ESL	gate dielectric (SiN_x:300nm)	PECVD (oxford) [Si rich low stress nitride]	RF: 40W Gas: $SiH_4/NH_3/N_2$(150/2//790) Pressure: 600 mTorr Temp: 350°C	21min	
	a-Si:H Deposition (Si:100nm)	PECVD (oxford) [a-Si low rate]	RF: 20W Gas: SiH_4-Ar/He(100/1000) Pressure: 1600 mTorr Temp: 350°C	15min	
	ESL (SiN_x:200nm)	PECVD (oxford) [Si rich low stress nitride]	RF: 40W Gas: $SiH_4/NH_3/N_2$(150/2//790) Pressure: 600 mTorr Temp: 350°C	9min30sec	
	ESL pattern	spinner aligner(vaccum mode)	SPR3.0 (w/o primer) 3000 rpm, 60 sec PreBake: 115°C, 120 sec Exposure time=40sec PEB: 115°C, 120sec Develop:60 sec		PR = 2.75µm (aligner illumination density: ~9.98)
	descum	Technics RIE	RF:400W Gas: O_2(10 sccm) Pressure: 150mTorr	30sec	
	ESL etch #1	Oxford RIE	RF/ICP=200/2000W Gas: C_4F_8/O_2 (45/2) Pressure: 7mTorr Temp: 15°C	55 sec	Etch depth= 190~200nm

Appendix A: Run sheet for TFT-VACNF processing (CHP-TFT) continued

Layer	Process	Equipment	Condition	time	remark
Active & ESL	ESL etch #2	wet bath	BOE 6:1	1min	hydrophobic
	descum	Technics RIE	RF:400W Gas: O_2(10 sccm) Pressure: 150mTorr	30sec	to remove the attached PR by plasma
	PR strippin	stirpper	20min		
	ashing	Technics RIE	RF:400W Gas: O_2(10 sccm) Pressure: 150mTorr	2min	
N+Si & contact holes	n^+ Si deposition (50nm)	RF sputter	RF/DC=200W/30W Gas: Ar(25sccm) Pressure: 5mTorr Temp: R.T	15min30sec	3.1864nm/min resistivity <20 ohm-cm
	contact hole pattern	spinner aligner(vaccum mode)	SPR3.0 (w/o primer) 1500 rpm, 60 sec PreBake: 115°C, 120 sec Exposure time=60 sec PEB: 115°C, 120sec Develop:60 sec		PR = 3.20µm (aligner illumination density: ~9.98)
	descum	Technics RIE	RF:400W Gas: O_2(10 sccm) Pressure: 150mTorr	30sec	
	contact hole etch	Oxford RIE	RF/ICP=30/2000W Gas: SF_6/Ar (45/1) Pressure: 10mTorr Temp: 15°C	3min (overetch)	Etch rate= N^+Si:10nm/sec SiN_x:7.5nm/sec
	PR strippin	stirpper	20min		
	ashing	Technics RIE	RF:400W Gas: O2(10 sccm) Pressure: 150mTorr	2min	
	Dehydrogenation	Box furnace (SMRC)	Temp: 600°C ramp up & down: 3°C/min	60min	
S/D & VACNF	Deposition (Cr:200nm)	Sputter (#4)	RF: 200W(420V)/5W(**138V**) Gas: Ar(25) Pressure: 5mT Temp: 200oC	50min	4nm/min R.S:1.21~1.29 Stress:0
	CNF Ni dot pattern	MASK: VACNF spinner aligner(vaccum mode)	SPR 0.7 (w/o primer) 2000rpm, 60 sec PreBake: 115°C, 120 sec Exposure time=15 sec PEB: 115°C, 120sec Develop:60 sec		PR = 0.70µm (aligner illumination density: ~9.98)
	descum	Technics RIE	RF:400W Gas: O_2(10 sccm) Pressure: 150mTorr	15 sec	
	Ni deposition	Evaporator			

Appendix A: Run sheet for TFT-VACNF processing (CHP-TFT) continued

Layer	Process	Equipment	Condition	time	remark
S/D & VACNF	lift-off	aceton			
	CNF growth	DC-PECVD	Temp: 700°C Gas:C_2H_2/NH_3 (85/200) Pressure:15 Torr Current: 1 A	19 min	~20μm
BCE	Cr pattern	spinner aligner(vaccum mode)	SPR3.0 (w/o primer) 3000 rpm, 60 sec PreBake: 115°C, 120 sec Exposure time=40 sec PEB: 115°C, 120sec Develop:60 sec		PR = 2.75μm (aligner illumination density: ~9.98)
	S/D etch	wet bath	Cr 14S etchant (R.T)	End point	
	PR strippin	stirpper	30min		
	BCE	Oxford RIE	RF/ICP=30/2000W Gas: SF_6/Ar (45/1) Pressure: 10mTorr Temp: 15°C	etch depth monitoring	Etch target depth (n^+Si (50nm) + ESL:100nm)
PVX & Via hole	PVX (Si_3N_4:300nm)	PECVD (oxford) [Si rich low stress nitride]	RF: 40W Gas: $SiH_4/NH_3/N_2$(150/2//790) Pressure: 600 mTorr Temp: 350°C	21min	
	Via hole pattern	spinner aligner(vaccum mode)	SPR3.0 (w/o primer) 1500 rpm, 60 sec PreBake: 115°C, 120 sec Exposure time=60 sec PEB: 115°C, 120sec Develop:60 sec		PR = 3.20μm (aligner illumination density: ~9.98)
	descum	Technics RIE	RF:400W, Gas: O_2(10 sccm) Pressure: 150mTorr	30sec	
	via hole etch	Oxford RIE	RF/ICP=30/2000W Gas: SF_6/Ar (45/1) Pressure: 10mTorr Temp: 15°C	3min30sec (overetch)	Etch rate= n^+Si:10nm/sec SiN_x:7.5nm/sec
	PR strippin	stirpper	20min		
	ashing	Technics RIE	RF:400W Gas: O_2(10 sccm) Pressure: 150mTorr	30sec	

Appendix B: Run sheet for TFT-VACNF processing (BCE-TFT)

TFT-VACNF (Back channel TFT)

Layer	Process	Equipment	Condition	time	remark
Buffor	PECVD (SiO2:500nm)	PECVD (oxford) [Silicon dioxide]	RF:20W SiH_4/N_2O(85/157) Pressure: 1000 mTorr Temp: 350°C	7min15sec	Stress:-180MPa
Gate	Deposition (Cr:100nm)	Sputter (#4)	RF: 200W(420V)/5W(**138V**) Gas: Ar(25) Pressure: 5mT Temp: 200°C	25min	4nm/min R.S:1.21~1.29 Stress:~0 Mpa
	Cr pattern	spinner contact aligner (vaccum mode)	SPR3.0 (w/ primer) 3000 rpm, 60 sec PreBake: 115°C, 120 sec Exposure time=40 sec PEB: 115°C, 120sec Develop:60 sec		PR = 2.75μm (aligner illumination density: ~9.98)
	descum	Technics RIE	RF:400W Gas: O_2(10 sccm) Pressure: 150mTorr	30sec	
	Cr etch	wet etch	Cr 14S etchant (R.T)	End+20sec	
	PR strippin	stirpper	20min		
	ashing	Technics RIE	RF:400W Gas: O_2(10 sccm) Pressure: 150mTorr	2min	
Active	gate dielectric (SiN_x:300nm)	PECVD (oxford) [Si rich low stress nitride]	RF: 40W Gas: $SiH_4/NH_3/N_2$(150/2//790) Pressure: 600 mTorr Temp: 350°C	21min	
	a-Si:H Deposition (Si:200nm)	PECVD (oxford) [a-Si low rate]	RF: 20W Gas: SiH_4-Ar/He(100/1000) Pressure: 1600 mTorr Temp: 350°C	30min	
n^+Si & contact holes & dehydrogenation	n^+ Si deposition (50nm)	RF sputter	RF/DC=200W/30W Gas: Ar(25sccm) Pressure: 5mTorr Temp: R.T	15min 30 sec	3.1864nm/min resistivity <20 ohm-cm
	contact hole pattern	spinner aligner(vaccum mode)	SPR3.0 (w/o primer) 1500 rpm, 60 sec PreBake: 115°C, 120 sec Exposure time=60 sec PEB: 115°C, 120sec Develop:60 sec		PR = 3.20μm (aligner illumination density: ~9.98)
	descum	Technics RIE	RF:400W Gas: O_2(10 sccm) Pressure: 150mTorr	30sec	

Appendix B: Run sheet for TFT-VACNF processing (BCE-TFT) continued

Layer	Process	Equipment	Condition	time	remark
n+Si & contact holes& dehydrogenatio n	contact hole etch	Oxford RIE	RF/ICP=30/2000W Gas: SF_6/Ar (45/1) Pressure: 10mTorr Temp: 15°C	3min (overetch)	Etch rate= N^+Si:10nm/sec SiN_x:7.5nm/sec
	PR strippin	stirpper	20min		
	ashing	Technics RIE	RF:400W Gas: O2(10 sccm) Pressure: 150mTorr	2min	
	dehydrogenatioin	Box furnace (SMRC)	Temp: 600°C ramp up & down: 3°C/min	60 min	
S/D & VACNF	Deposition (Cr:200nm)	Sputter (#4)	RF: 200W(420V)/5W(**138V**) Gas: Ar(25) Pressure: 5mT Temp: 200oC	50min	4nm/min R.S:1.21~1.29 Stress:~ 0
	CNF Ni dot pattern	MASK: VACNF spinner aligner(vaccum mode)	SPR 0.7 (w/o primer) 2000rpm, 60 sec PreBake: 115°C, 120 sec Exposure time=15 sec PEB: 115°C, 120sec Develop:60 sec		PR = 0.70µm (aligner illumination density: ~9.98)
	descum	Technics RIE	RF:400W Gas: O_2(10 sccm) Pressure: 150mTorr	15 sec	
	Ni deposition	Evaporator			
	lift-off	aceton			
	CNF growth	DC-PECVD	Temp: 700°C Gas:C_2H_2/NH_3 (85/200) Pressure:15 Torr Current: 1 A	19 min	~20µm
BCE	Cr pattern	spinner aligner(vaccum mode)	SPR3.0 (w/o primer) 3000 rpm, 60 sec PreBake: 115°C, 120 sec Exposure time=40 sec PEB: 115°C, 120sec Develop:60 sec		PR = 2.75µm (aligner illumination density: ~9.98)
	S/D etch	wet bath	Cr 14S etchant (R.T)	End point	
	PR strippin	stirpper	30min		
	BCE	Oxford RIE	RF/ICP=30/2000W Gas: SF_6/Ar (45/1) Pressure: 10mTorr Temp: 15°C	Etch depth monitoring	Etch target depth n^+Si(50nm) + Si:(50nm)

Appendix B: Run sheet for TFT-VACNF processing (BCE-TFT) continued

Layer	Process	Equipment	Condition	time	remark
PVX & Via hole	PVX (SiN_x:300nm)	PECVD (oxford) [Si rich low stress nitride]	RF: 40W Gas: $SiH_4/NH_3/N_2$(150/2//790) Pressure: 600 mTorr Temp: 350°C	21min	
	Via hole pattern	spinner aligner(vaccum mode)	SPR3.0 (w/o primer) 1500 rpm, 60 sec PreBake: 115°C, 120 sec Exposure time=60 sec PEB: 115°C, 120sec Develop:60 sec		PR = 3.20µm (aligner illumination density: ~9.98)
	descum	Technics RIE	RF:400W, Gas: O_2(10 sccm) Pressure: 150mTorr	30sec	
	via hole etch	Oxford RIE	RF/ICP=30/2000W Gas: SF_6/Ar (45/1) Pressure: 10mTorr Temp: 15°C	3min30sec (overetch)	Etch rate= N^+Si:10nm/sec SiN_x:7.5nm/sec
	PR strippin	stirpper	20min		
	ashing	Technics RIE	RF:400W Gas: O_2(10 sccm) Pressure: 150mTorr	30sec	

Vita

Jung won Park received the Bachelor of Engineering degree in Metallurgical Engineering from Yonsei University, Seoul, South Korea in 2001, respectively. He is currently pursuing the Ph.D degree at the department of Materials Science and Engineering, the University of Tennessee, Knoxville, TN. His research interests include Thin Film characterization, Thin Film Transistor fabrication, and Thin Film Transistor and Vertically Aligned Carbon Nanofibers device integration and fabrication.