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Physics based modeling of multiple gate transistors on Silicon-on-Insulator (SOI)

Touhidur Rahman
University of Tennessee

To the Graduate Council:

I am submitting herewith a dissertation written by Touhidur Rahman entitled "Physics based modeling of multiple gate transistors on Silicon-on-Insulator (SOI)." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Syed K. Islam, Major Professor

We have read this dissertation and recommend its acceptance:

Accepted for the Council:

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PHYSICS BASED MODELING OF MULTIPLE GATE TRANSISTORS ON SILICON-ON-INSULATOR (SOI)

A Dissertation

Presented for the

Doctor of Philosophy

Degree

The University of Tennessee, Knoxville

Touhidur Rahman

May 2009

DEDICATION

This dissertation is dedicated to my wife Sharmin Hai, my parents, my sister and her husband, my in-laws, my nieces and nephew.

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ABSTRACT

G^4FET is a novel device built on Silicon-on-Isulator (SOI). Due to the presence of Bulk-Si, it is impossible to have more than one gate for each transistor in conventional process technology. However, it is possible to have multiple gates for each transistor in SOI devices due to the presence of buried oxide, which can be used as an independent gate. Besides the oxide gates, junction gates can also be introduced. Due to the presence of the thin active layer, the junction gate can reach to the bottom and can be used to isolate and control the conduction in the transistors. As a result, the maximum number of gates that can be achieved in SOI is four. A transistor with four gates is called G^4FET. G^4FET offers all the features of SOI technology. It offers remedies of the drawbacks of Bulk-Si technology. The operation of the multiple gates has applications for mixed-signal circuits, quantum wire, and single transistor multiple gates logic schemes, etc.

The research goal is to understand the device physics of G^4FET. Understanding device physics will provide enough information to set device parameters to optimize device performances. The operation of semiconductor devices depends on several material parameters, device dimensions and structure. The objective of this research is to develop a model that includes material parameters, device dimensions and structure. The second objective of this research is to develop a numerical model from available data. The numerical model is useful for circuit simulation of G^4FET, which provides information about the characteristics of G^4FET, when used as a circuit element.

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CHAPTER ONE

Introduction

1.1 Motivation

Transistors are considered the greatest invention of the twentieth-century [1], or one of the greatest [2]. Transistors are the key active components in practically all modern electronics. The importance of transistors in today's society rests on the ability to be mass-produced using a highly automated fabrication process achieved with astonishingly low per-transistor costs. The low cost, flexibility, and reliability of the transistors have made it a ubiquitous device. Since the invention of the bipolar junction transistor in the late 1940's, semiconductors replaced vacuum tube electronics and provided an enormous increase in speed. The electronic circuits made with vacuum tubes were heavy, power-hungry, and unreliable. On the other hand, semiconductor devices are lightweight, low power, and reliable. The popularity of the semiconductor circuits rose due to the introduction of the Integrated Circuit (IC) concept, introduced in 1958 independently by Jack St. Clair Kilby and Robert Norton Noyce [3-4]. Since the introduction of the Integrated Circuit (IC) concept, the number of circuit components that can be placed on an IC has increased exponentially with time. In order to accommodate more transistors in same area device sizes need to be reduced. Decreasing the device size not only reduces the area, but also provides a faster transistor with a lower power requirement. In 1965, Gordon Moore, co-founder of INTEL®, observed that the number of transistors in an integrated circuit (IC) would double every two years [5, 6].

This observation, known as Moore's Law after Gordon Moore, has been successful in making predictions since 1965. Figure 1.1 shows the original calculation of Dr. Moore. The technological progress in the semiconductor industry has been driven by the desire to achieve the results of Moore's Law. Moore's Law has been the primary driving factor for over the last 40 years for the enhancement of device performances by continuously scaling down the feature sizes of the devices. The competitive drive for improved performance and cost reduction has resulted in the scaling of circuit elements to smaller dimensions [7].

Over the time, the process technology has matured. The Bulk-Si devices have emerged as the unprecedented active element for very large scale integration (VLSI), but a number of fundamental physical limits now hamper the growth of performance of the Bulk-Si devices. The problems include decreasing carrier mobility due to impurity scattering and increasing gate tunneling current as the junction becomes shallower. These

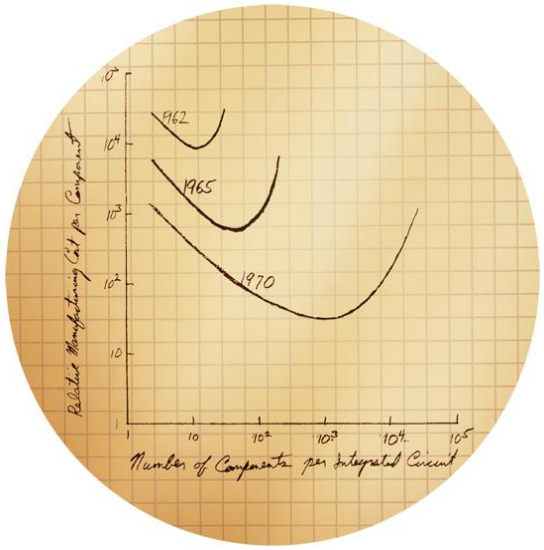


Figure 1.1: Gordon Moore's original graph from 1965.

trends make conventional scaling less feasible. As a result, the operating voltage tends to be set higher than that needed by a scaled-down device in order to achieve the desired speed performance [8]. In the Bulk-Si technology, multiple transistors are isolated from each other by reverse biased p-n junctions. With the rapid progress and the evolution of microelectronics, the junction isolation is not always the best approach for integrated circuits. These junctions introduce extra capacitance and reduce the density of the transistors in the circuits. If the ambient temperature is high enough, leakage currents diminish the isolation between the various circuit components.

In a quest for a new process technology, researchers from around the world probed for a substrate that would meet the necessary requirements of low junction capacitance, low leakage current, and high breakdown voltage. The requirements are fulfilled by utilizing Silicon-on-Insulator (SOI) wafers. Historically, there were three reasons for developing and using SOI. In the 1970s and 1980s, the radiation hardness of SOI circuits was the primary motivator for choosing new substrates. Thin, active Si films minimized the impact of ionizing radiation on device performance. Currently, the performance enhancement needs to motivate many integrated circuit companies to use SOI wafers. For the same supply voltage, digital logic circuits, such as microprocessors, run faster in SOI than in the Bulk-Si. Alternatively, it is possible to reduce power consumption of the SOI chips by lowering their operating voltages, while still keeping the clock rate and their performance the same as in more power-hungry Bulk-Si circuits. Since their introduction, commercial applications of SOI have grown exponentially, and entered the mainstream of ultra large-scale integration (ULSI) electronic

Figure 1.2: History and forecast of market share of SOI.

circuits. Figure 1.2 shows the growth of market share of SOI technology. Silicon-on-Insulator (SOI) technology features a low capacitance that enables high-speed operation. However, the advantages of SOI technology are not limited to the areas of speed and power. They also include good radiation hardness, the ability to withstand high temperatures, the ability to handle high voltage, contain steep subthreshold characteristics, and have small, short-channel effects [8]. In addition, the SOI devices are free from latch-up and can be implemented with a smaller layout area as compared to the Bulk-Si devices.

The SOI technology opens up the possibility of having more than one gate for each transistor due to the presence of two oxide layers. Because of the two oxide layers, Double Gate MOSFET (DGMOSFET) is now attracting attention. DGMOSFET utilizes the two oxide layers as independent gates to control conduction. This offers more control over the channel and completely or partially, eliminates the drawbacks of the Bulk-Si technology. However,

the maximum number of gates in a transistor is not limited to just two [9]. The number of gates can be extended to four for SOI technology includes two junction gates in addition to the two oxide gates. The transistor with four gates is called a Four Gate Field Effect Transistor (G^4FET) [10]. The G^4FET offers all features of the SOI technology. The independent action of the four gates broadens the horizons for mixed-signal applications, quantum wire effects, and quaternary logic schemes.

Different methods of device modeling exist. Physics-based modeling deals with expressing device characteristics in terms of physical phenomena. It takes the exact expressions of the different parameters and obtains a closed form of expression. This method provides insight information into device operation. Another form, the charge control method, considers the device as a sheet of charge that can be varied by gate potential. The charge control method provides single or piecewise functions for device characteristics. It does not provide information about the internal conduction mechanism; however, it can predict device characteristics. An additional method is the numerical method. This method uses experimental data to obtain a model for the device. The numerical model can predict more fitting device behavior than the other two as it is derived from the experimental data. A further advantage for numerical modeling is that it can be readily used for circuit simulation.

1.2 Research Goal

The G^4FET is a novel device that was invented in 2002 [10]. To date a limited amount of research has been conducted on the G^4FET. Due to its enormous potential, a better understanding of the G^4FET is required. By comprehending the device physics of the G^4FET,

the device design can be optimized for better performance. One of the requirements, after designing a device, is to predict the behavior of said device. This can be completed via the charge control method. A device is tested for its performance and application when it is integrated into a circuit. However, it is always preferable to simulate the circuit prior to building it. In order to complete simulation in a circuit model, a circuit containing the device under design must be replicated. The research goals of this dissertation are described as follows:

1. Understand the device physics of a G^4FET by solving carrier transport and Schrodinger wave equations to optimize the device design.
2. Develop a closed form of expression for device characteristic of a G^4FET using a charge control method.
3. Development of a circuit model for a G^4FET to simulate the circuit containing the G^4FET.

1.3 Dissertation Overview

This dissertation is segregated into seven chapters. The limitation of the Bulk-Si technology and the need for SOI technology are explained in Chapter One. The evolution of the G^4FET and necessity of physics based, charge control, and numerical modeling are also discussed in Chapter One. Previous work on the G^4FET and physics based, charge control, and numerical modeling are discussed in Chapter Two. The device structure of the G^4FET is given in Chapter Three. The basics of physics based modeling and the techniques of mathematical solutions are depicted in Chapter Four. The charge control model is developed

in Chapter Five. The numerical modeling is discussed in Chapter Six. Discussions, conclusions and future work are summarized in Chapter Seven.

CHAPTER TWO

Literature Review

2.1 Previous works on G^4FET

A new SOI device has been [10-11] developed that combines two different transistors, a 1-JFET and a 2-MOSFET, superimposed in a single silicon island so that they share the same body. The new devices were named the MOS-JFET [10] and the G^4FET [11].

The results measured from the MOS-JFET transistors, fabricated using a conventional partially-depleted (PD) SOI technology, demonstrating that they were a fully operational device. The G^4FET showed excellent performance under a wide range of operating voltages [10, 12]. The experimental results demonstrated the complex variation of the threshold voltage, subthreshold swing, and breakdown voltage due to the multiple gate control utilized with the G^4FET. The breakdown voltage of 15V was measured for a 3.3V partially-depleted SOI device with an excellent subthreshold swing and high mobility.

Numerical simulation is an excellent tool to use in order to have a better understanding about the conduction mechanism caused by the interaction of multiple gates. The channel characteristics of fabricated experimental devices were reproduced using a numerical simulation with a non-uniform doping profile [13].

The threshold voltage and channel mobility are important parameters for device characteristics. A new method of extraction for the threshold voltage, subthreshold swing, and

mobility in the linear region were performed. The measurement results demonstrated the complex dependence of these parameters on the multi-gate biases [14].

The operation of the G^4FET was governed by the charge coupling between the front, back and. lateral gates [15], and a 2-D analytical relation for the fully-depleted body potential was derived. The front-interface threshold voltage was expressed as a function of the back and lateral gate voltages for all possible back interface conditions.

The operation of the G^4FET rigorously analyzed the interface conditions based on the measured current-voltage, transconductance, and threshold characteristics [16]. The major device parameters (threshold voltage, swing, and mobility) were extracted and shown to be optimal for particular combinations of gate biasing. Numerical simulations are used to clarify the role of volume or interface conduction mechanisms.

The G^4FET shows an improved subthreshold slope compared to that of the conventional MOSFET [17]. The subthreshold slope, which may be defined with respect to either the junction gates or MOS gates, is adjustable using the remaining gates.

The 2-D analytical body potential was derived by assuming a parabolic potential variation between the lateral junction–gates and by solving Poisson's equation [18]. The model was used to obtain the surface threshold voltage of the G^4FET as a function of the lateral gate bias and for all possible charge conditions at the back interface.

The G^4FET exhibits a negative differential resistance (NDR) when used as a complementary pair because of the presence of the JFET. Innovative LC oscillator and Schmitt trigger circuits based on the G^4FET NDR device were experimentally demonstrated [19].

The most important application of the G^4FET is the formation of the quantum wire. The quantum wire is formed when the conducting channel is surrounded by depletion regions induced by independent vertical metal-oxide-semiconductor gates and lateral JFET gates [20]. This unique conduction mechanism, named depletion-all-around (DAA), enables the majority of carriers to flow in the volume of the silicon film far from the silicon/oxide interfaces. The lateral JFET gates have the highest degree of control on the conduction channel when their interfaces are biased to inversion and the sensitivity of the channel to the oxide and interface defects is minimized. This effect provides excellent analog performance, low noise, and immunity to ionizing radiation.

2.2 Previous works on device physics

The most important parameters that influence the conduction mechanism are the carrier mobility and carrier recombination-generation. The carrier mobility depends on temperature, doping density, and normal and longitudinal electric fields. The carrier generation and recombination depends on carrier density and temperature.

A semi-empirical model for carrier mobility in silicon inversion layers was presented by Lombardi [21]. The model is appropriate for a wide range of normal electric fields, channel impurity concentrations ($5 \times 10^{14} < \boldsymbol{N_A} < 10^{17}$ cm^{-3}, $6 \times 10^{14} < \boldsymbol{N_D} < 3 \times 10^{17}$ cm^{-3}), and temperatures ($200 \text{ K} < \boldsymbol{T} < 460 \text{ K}$).

An analytical expression had been derived for the electron and hole mobility in silicon layers based on experimental data [22]. The expression is valid for electron and hole mobility as a function of concentration up to 10^{20} cm^{-3} and wide temperature ranges (250-500 K).

Massetti [23] proposed a concentration dependent mobility that is valid for different types of doping materials (**P**, **As**, and **Br**). It also predicts carrier mobility for doping concentration well above 10^{21} cm^{-3}. Reggiani [24-25] of the University of Bologna, Italy proposed a unified model of mobility that included dependences on temperature, doping, and electric field. This model is also known as the University of Bologna mobility model. The electric field and the doping dependence of mobility were discussed in detail by Caughey [26]. An expression was derived from the experimental results to include the effect of temperature and electric field. Canali [27] derived an empirical relationship that describes the high field velocity saturation and temperature dependence of mobility. Hall [28] and Shottky-Read [29] independently established a universal expression for carrier recombination and generation almost simultaneously. The carrier lifetime is the most important parameter as it determines the recombination-generation rate. The carrier lifetime depends on temperature and doping density. The dependence of carrier lifetime on temperature and the doping density is explained in [30, 31].

2.3 Previous works on physics based modeling

In the early days of device modeling, most of the work was concentrated on deriving terminal parameters. With the reduction of the device dimensions and the increasing complexity of device structure, these models can no longer predict the device characteristics. The existing models failed because they did not include the different physical phenomenon that arose from the small dimensions and complex structure. Soon, researchers began to

realize that a new model had to be developed that takes into account all the physical phenomenon that can occur during the device operation.

Gummel [32] was the first to try to develop a model that introduced different physical parameters into the model equation. He used the finite difference method to solve the model equations. This model not only provides the terminal characteristics, but also provides information about internal parameters such as potential and electric field distributions and mobility degradation due to the doping density and the electric field. Thus, this model provides a complete picture of the device.

Gummel's model was modified by Scharfetter-Gummel [33]. They eliminated the limitations of the previous model and established a new discretization technique to ensure convergence.

Slotboom [34] proposed a new model that made use of the Scharfetter-Gummel algorithm. He proposed two new artificial variables in order to linearize the differential equations. This model is easily implemented in computer code.

Mayergoyz [35, 36] proposed algorithms for device simulation that can be executed on parallel processors. However, this method is limited for device simulation in thermal equilibrium.

2.4 Previous works on charge control model

The charge control method has been a widely used method for modeling field effect transistors for quite some time. This method can be used to model a large range of devices,

such as the Metal-Oxide-Field Effect Transistor (MOSFET) [37, 38] and the High Electron Mobility Transistor (HEMT) [39].

The attractive feature of this method is that it does not deal with device physics in depth. This model assumes the conduction channel is a high charge sheet [40]. The density of the charge sheet depends on the potential applied at different terminals. Utilizing this relationship, this method culminates with a closed form of analytical expression. The expression is useful in predicting the behavior of the device in terms of terminal potentials.

The charge control model is applied to multiple gate transistors [41]. However, due to the complex geometric structure, some additional effects such as charge coupling between different gates are introduced. The charge control model is applied to the G^4FET [15, 21] to derive the closed form expression of the drain current and the threshold voltages. However, these analyses were done for a special condition. There is no charge control reported that is applicable for all conditions of the terminal potentials.

2.5 Previous works on numerical modeling

Numerical models offer an alternative to the physics-based analytical models for rapid and accurate device modeling. Although this approach does not provide any physical insight, these models serve as excellent tools for quick circuit simulation [42-50]. In general, this approach uses measured data to accurately reproduce the complex nonlinear behavior of the semiconductor devices. In most cases, they are equally applicable to different flavors of transistors (MOSFET, MESFET, HEMT, etc.) fabricated using various process technologies. A large number of works on numerical device modeling have been reported since the 1970's

[42]. The most commonly used methods involve the utilization of a look-up table and quadratic and higher order polynomials. Authors in [49] proposed numerical MOSFET modeling based on multi-dimensional Bernstein interpolation as a means to improve simulation efficiency. Hermite polynomials based on simple bi-cubic surface patch generation was presented in [50] for the evaluation of the device operating point. The interpolation function may exhibit bumps though the original set of data which could be monotonic and concave/convex in either direction. In [51], the triode region was modeled by quadratic fits whereas linear fits were used for the saturation region. Discontinuities in the conductance arise as the operating point shifts from the triode region to the saturation region, and vice versa. More data points are needed to reduce the discontinuity, however, that will increase the experimental cost. The basic cubic spline based multidimensional interpolation techniques are presented in [46]. The spline parameters are optimized for monotonic preserved interpolation.

The method for the look-up table is very simple to implement [43-45]. However, it requires a high density of data points and consumes significant amounts of computational time during the search process. It also depends on local approximation rather than global approximation. This restricts the look-up model and it can only be used within a limited range of operations. Another family of numerical approaches uses quadratic polynomials, or higher order polynomials, for interpolation [46-48]. These methods determine the coefficients of a predetermined polynomial from the available data. Due to the use of predetermined polynomials, the interpolation methods suffer from large truncation errors. For some special polynomials, such as Bernstein [49] and Hermite [50], the interpolation method involves the

determination of factorials and derivatives. These types of models tend to slow down significantly when large numbers of polynomial terms are used for interpolation.

CHAPTER THREE

G4FET Structure and Basic Operations

3.1 Silicon-on-Insulator (SOI)

Silicon-on-Insulator technology (SOI) refers to the use of a layered silicon-insulator-silicon substrate in place of the conventional silicon substrates in semiconductor manufacturing, especially microelectronics, to reduce parasitic device capacitance and thereby, improve performance [9]. SOI-based devices differ from the conventional Bulk-Si devices in that the silicon junctions are formed on an insulator. The key feature of the SOI structure is the layer of silicon dioxide just below its surface. The layer is called the buried oxide (BOX). The thin film of Si on the SiO_2 is called the active Si layer. This is the layer where all devices are fabricated. The Si layer beneath the BOX is called the substrate, handle, or base wafer. Figure 3.1 shows the SOI wafer and the cross section of SOI structure. This figure shows that the device layer is separated from handle wafer by BOX. As a result the conduction is confined in a thin layer of Si thereby reducing the loss due to bulk conduction.

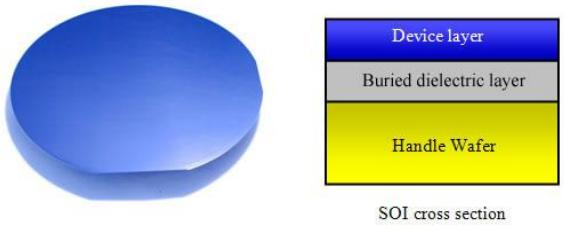


Figure 3.1: SOI wafer and the cross section of SOI structure.

The implementation of SOI technology is one of several manufacturing strategies employed to allow the continued miniaturization of microelectronic devices, colloquially referred to as the extension of Moore's Law. Reported benefits of the SOI technology, relative to the conventional silicon processing, includes a lower parasitic capacitance due to isolation from the bulk silicon. This improves power consumption at matched performance and resistance to latch up due to the complete isolation of the n- and p- well structures.

From a manufacturing perspective, SOI substrates are compatible with most conventional fabrication processes. In general, an SOI-based process may be implemented without special equipment or significant retooling of an existing factory. Among the challenges unique to a SOI are novel metrology requirements to account for the buried oxide layer and concerns about differential stress in the topmost silicon layer. The primary barrier to SOI implementation is the drastic increase in the substrate cost, which contributes an estimated 10 - 15% increase to total manufacturing costs [52].

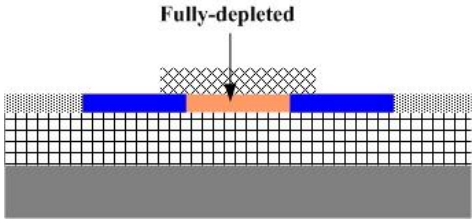
The physics of SOI devices is highly dependent on the thickness and doping concentration of the silicon film on which they are constructed. Two types SOI wafers. Fully Depleted (FD) and Partially Depleted (PD) SOI, exist. The thickness and doping density of the Si film of the FDSOI is less than that of the PDSOI. As a result, the Si film of a FDSOI is more easily depleted than the PDSOI at thermal equilibrium. A FDSOI exhibits steep subthreshold characteristics, negligible floating body effects, and small, short channel effects. On the other hand, a PDSOI offers multiple conduction modes (surface and volume) with higher current density. Moreover, a PDSOI can be converted to a FDSOI with appropriate bias gate conditions. In order to take full advantages of SOI technology, it is preferable to

have a device with a PDSOI. Figure 3.2 shows cross section of (a) FDSOI and (b) PDSOI wafers. It is clear from the figure that the active silicon layer of FDSOI is thinner than that of the PDSOI. It also shows that the channel of the DSOI is fully depleted whereas the channel of the PDSOI is partially depleted.

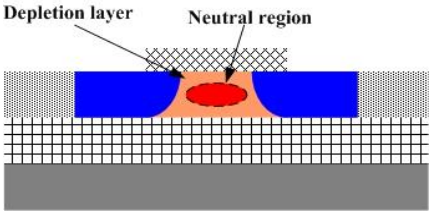
3.2 G^4FET device structure

The G^4FET is a new device built on a PDSOI. It takes advantage of the isolation properties of the SOI technology to unite both the Metal-Oxide-Semiconductor (MOS) field-effect and the Junction Field-Effect (JFET) devices to control conduction within a single transistor channel [10]. The G^4FET combines two different transistors: one – a JFET in the lateral direction and two – MOSFETs in a vertical direction superimposed on a single silicon island to share the same body. The G^4FET acts as a four-gate transistor with two side junction-based gates, the top MOS gate and the back gate activated by SOI substrate biasing. Implementation of multiple independent gates in Bulk-Si technology is difficult. On the other hand, via the combination of MOS gates and junction-based gates, the SOI-based G^4FET allows implementation of multiple gates. Figure 3.3 shows the three-dimensional and cross section views of a G^4FET. It shows that G^4FET combines JFET and MOSFET to share a common conduction channel. It also shows that the conduction channel is surrounded by different gates and can be controlled by independent action of each gate.

The G^4FET is formed using the traditional layout of a SOI MOSFET with two additional explicit body contacts on opposite sides of the MOSFET. The n-channel

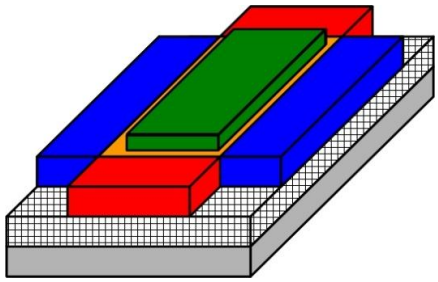


(a)

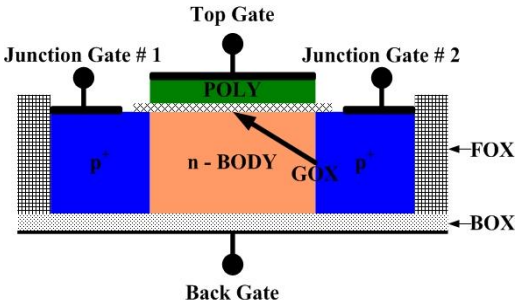


(b)

Figure 3.2: Cross section, showing depletion of channel, of (a) FDSOI and (b) PDSOI.

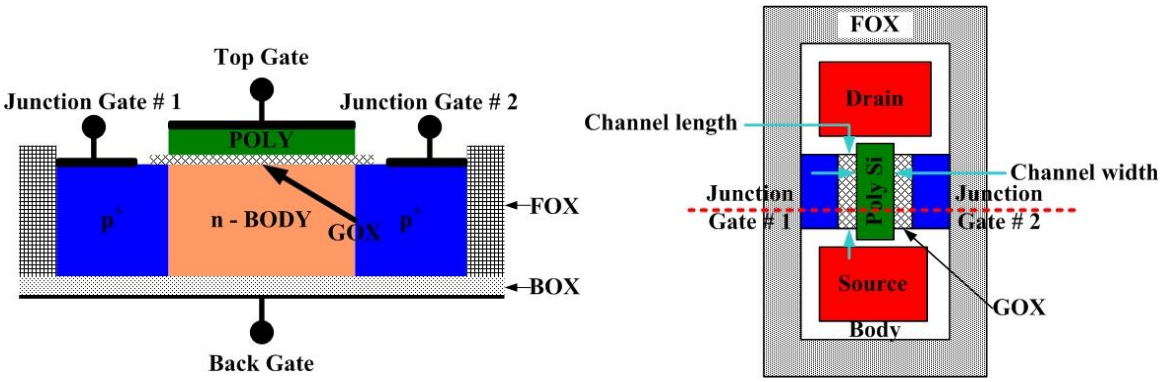


(a)



(b)

Figure 3.3: (a) 3 Dimensional view of G4FET; (b) Cross section of G4FET along x-x as shown in (a).



(a) (b)

Figure 3.4: G4FET structure: (a) cross-section and (b) top view.

G^4FET (shown in Figure 3.4) can be constructed from a regular p-channel MOSFET that has two independent body contacts located on either side of the channel. The former source and drain of the original p-channel MOSFET are p+ doped, and now act as lateral junction gates used to control the width of the conductive path. The former body contacts are used as the source and drain for the n-channel G^4FET. The channel of the G^4FET is coincident with the body of the MOSFET Therefore, an inversion-mode, p-channel MOSFET is converted into an accumulation/depletion-mode n-channel G^4FET. The gate length of the MOSFET defines the channel width of the G^4FET and vice-versa. It is clear from the G^4FET structure that no specialized fabrication step is necessary to manufacture the device. The maximum extension of the conductive path corresponds to the gate length of the original MOSFET, whereas the JFET channel length is defined by adjusting the width of the MOSFET. Table 3.1 shows the conversion of parameters between the G^4FET and a common MOSFET. This conversion reflects that the n-channel G^4FET can be constructed from a p-channel SOI MOSFET. It also shows the transformation of geometrical aspect of p-channel MOSFET to G^4FET.

Table 3.1: Conversion from MOSFET to G^4FET [53]

MOSFET	⇔	G4-FET
p-channel	⇔	n-channel
n-channel	⇔	p-channel
Width	⇔	Length
Length	⇔	Width
Source/Drain	⇔	Lateral junction gates
Body contacts	⇔	Source/Drain

3.3 Operation

The G^4FET combines MOSFET and JFET principles into a single SOI device. Each of the four gates can control the conduction characteristics of the transistor. In a G^4FET, the drain current is composed of majority carriers and flows in a direction perpendicular to that of the original inversion-mode MOSFET and both the MOS gates are converted to accumulation-mode devices [3]. The only way to modulate conduction is to vary the total number of carriers in the channel. Two different ways exist to vary the number of carriers in the channel. One is to change carrier density keeping the conduction area fixed. The second way is to change conduction area keeping the carrier density fixed. Each of the MOS gates has three distinct regions of operations. The top and back MOS gates modulate the channel conductivity through accumulation, depletion, or inversion. On the other hand, the JFET gates change the channel conductivity only by depletion. Due to the presence of different conduction mechanisms for each gate, a large number of combinations of conduction

mechanisms are possible. Numerical simulations of the G^4FET are conducted using Synopsys® TCAD Sentaurus. The simulations are used to gain insight into the mechanisms controlling the conductive path inside the body of the transistor. The simulations show that the channel cross section can be controlled to some extent by each gate.

Figure 3.5 shows the cross section of a G^4FET channel under no bias conditions, and at thermal equilibrium. It will be used to compare the effect of different gate biases on the channel. Figure 3.6 shows the effect of the top gate bias. It shows accumulation, depletion, and inversion of the top gate. In accumulation, the conduction area remains unchanged. However, the current is expected to increase due to the increase in carrier concentration under the top gate. In the depletion condition, the conduction area gradually decreases until the onset of inversion. At inversion, the depletion area reaches its maximum. Therefore, the conduction area is minimized. Figure 3.7 shows the effect of the back gate bias. The back gate has the identical effect on the channel that the top gate does. However, the values of the different parameters vary due to the different thicknesses of the oxide. It shows accumulation, depletion, and inversion of the back gate. In accumulation, the conduction area remains unchanged. However, the current is expected to increase due to the increase in carrier concentration over the back gate. In the depletion condition, the conduction area gradually decreases until the onset of inversion. At inversion, the depletion area reaches its maximum. Therefore, the conduction area is minimized.

Figure 3.8 shows the effect of the JFET gates. Upon application of a reversed bias, the depletion region of the reversed biased p-n junction increases. Therefore, with an increase of

the reverse bias the channel width decreases. Either of the junction gates can be biased independently. However those can also be operated simultaneously for maximum effect.

However, combined effects from the top, back, and side gates provide the ultimate control of the cross-section of the conductive path. Adding the JFET bias in addition to the top and the back MOS gate biases provides maximum control over the channel. A special situation occurs when the top and the back MOS gates are biased in the depletion/inversion mode and the JFET gates are biased in reversed bias; the conduction is confined to a small area and is located near the center of the channel. Under these conditions, the conduction channel formed in the center portion of the body of the transistor is in effect a variable size wire. Furthermore, by varying the level of depletion of each gate the size and position of the wire can by varied within the film. Interestingly, since the conduction aperture can be sized to very fine dimensions, a quantum wire may be realizable when utilizing this structure. Figure 3.9 shows the size and location of the quantum wire that can be varied by the different gate potentials. Figure 3.9 (a) shows a conduction channel with a large diameter. The area of the conduction channel decreases with the application of reverse bias at junction gates and depletion biases at the top and the back gates as shown in Figure 3.9 (b). Figure 3.9 (c) shows that the conduction channel shifted downward with the reduction of depletion bias at the back gate. Figure 3.9 (d) shows the movement of the conduction channel in the upward direction with the reduction of depletion bias at the top gate.

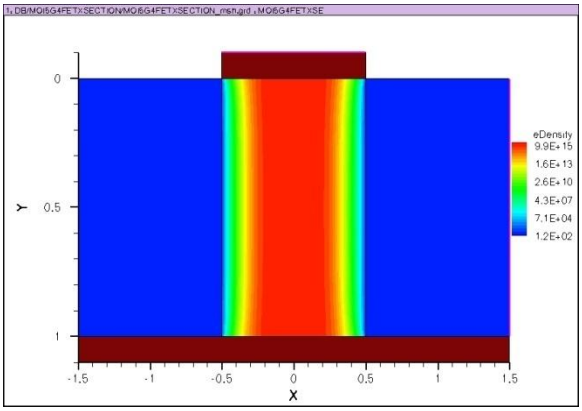
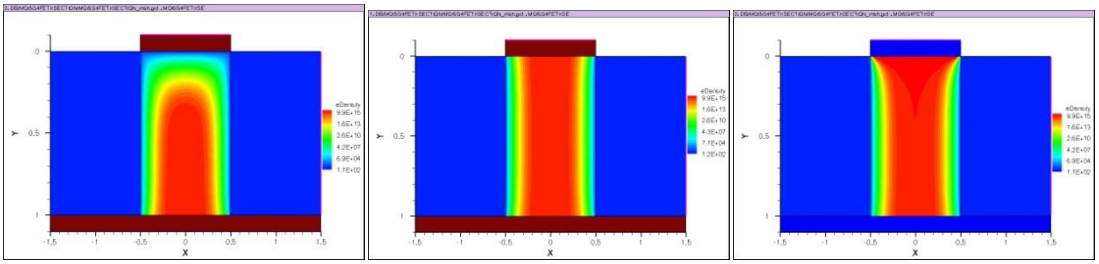
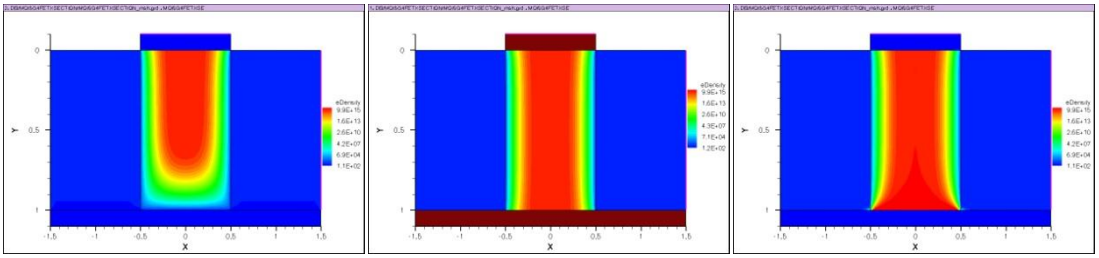


Figure 3.5: Cross section of G4FET under thermal equilibrium.



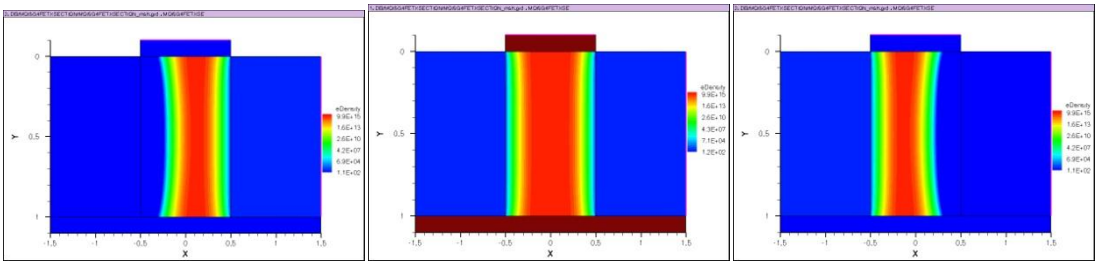
(a) (b) (c)

Figure 3.6: Effect of the bias at the top gate(a) accumulation; (b) depletion and (c) inversion.



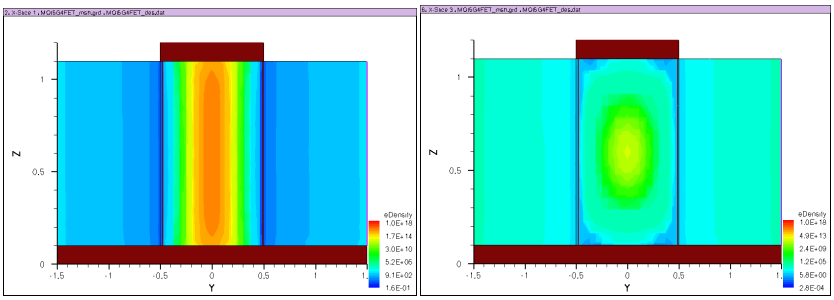
(a) (b) (c)

Figure 3.7: Effect of the bias at the back gate (a) accumulation; (b) depletion and (c) inversion.

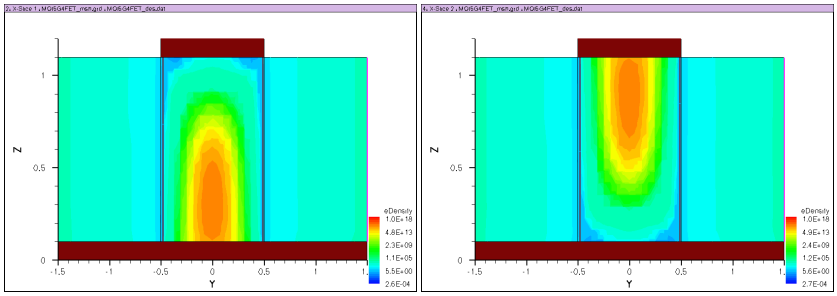


(a) (b) (c)

Figure 3.8: Effect of the bias at the junction gates (a) left gate; (b) both gates and (c) right gate.



(a) (b)



(c) (d)

Figure 3.9: Size and location of quantum wire (a) conduction channel with large area; (b) conduction channel with very small area located near the center of the channel; (c) conduction channel shifted downward due to action of back gate; (d) conduction channel shifted upward due to action of top gate.

3.4 Chapter Summary

This chapter describes the physical structure of a SOI wafer. The formation of G^4FET from a conventional SOI MOSFET is also discussed in this chapter. It is shown that G^4FET can be fabricated with conventional process without any significant retooling. This chapter also describes the operational modes of G^4FET. These operational modes are basic building blocks of understanding G^4FET operation and applications. These are also used to develop different models for G^4FET.

CHAPTER FOUR

Carrier Transport Modeling

4.1 Overview

The semiconductor devices produce a complex system due to the simultaneous occurrence of different physical phenomena. The complexity increases with the reduction of the device sizes due to the introduction of a high electric field, carrier velocity saturation, and quantum mechanical effects. Depending on applications and accuracy, the physical phenomena are depicted by a set of nonlinear, partial differential equations of varying levels of complexity. Various physical parameters (such as mobility, generation-recombination rate, and material-dependent parameters) and boundary conditions (interfaces and contacts) of the partial differential equations can be sophisticated and are strongly influenced by material properties, the device structure, and the applied potentials at different terminals.

4.2 Transport Equations

The governing equations for charge transport in semiconductor devices are three coupled nonlinear partial differential equations [54]; (i) the Poisson equation; (ii) the electron continuity equation and; (iii) the hole continuity equation.

The Poisson equation relates the electrostatic potential to the electric charge distribution. For linear and homogeneous materials the Poisson equation is given by

$$\nabla.(\varepsilon\nabla\psi) = -q(p - n + N) \tag{4.1}$$

where, ε is the electrical permittivity, ψ is the electrostatic potential (***EP***), q is the absolute value of the charge of an electron, p is the mobile hole density, and n is the mobile electron density. N is the net ionized doping density, given by

$$N = N_D^+ - N_A^- \tag{4.2}$$

where, N^+_D is the ionized donor density and N^-_A is the ionized acceptor density. The vector differential operator ∇ is given by

$$\nabla = \hat{x}\frac{\partial}{\partial x} + \hat{y}\frac{\partial}{\partial y} + \hat{z}\frac{\partial}{\partial z} \tag{4.3}$$

where, $\hat{x}$, $\hat{y}$, and $\hat{z}$ are the unit vectors in the x, y, and z directions respectively. $\frac{\partial}{\partial x}$, $\frac{\partial}{\partial y}$ and $\frac{\partial}{\partial z}$ are the partial derivatives with respect to x, y, and z, respectively.

The continuity equations ensure that electrons and holes are conserved, locally in space. These equations account for the different mechanisms of the carriers generation and recombination. The electron and hole continuity equations are shown below, respectively

$$\nabla.J_n = qR + q\frac{\partial n}{\partial t} \tag{4.4}$$

$$-\nabla.J_p = qR + q\frac{\partial p}{\partial t} \tag{4.5}$$

where, R is the net electron-hole recombination rate, J_n is the electron current density, J_p is the hole current density, and $\frac{\partial}{\partial t}$ is the partial derivative with respect to time.

4.3 General Drift-Diffusion Model

The net flow of the electrons and holes in a semiconductor generates current. Two basic conduction mechanisms exist in semiconductor devices: drift and diffusion [55]. The drift-diffusion model is widely employed for the simulation of carrier transport in semiconductors. It is defined by the basic semiconductor equations (Equation 4.1, Equation 4.4, and Equation 4.5). Current densities for the electrons and the holes are given by the following, respectively

$$\boldsymbol{J}_n = q\boldsymbol{D}_n \nabla \boldsymbol{n} - q\mu_n \boldsymbol{n} \nabla \psi \tag{4.6}$$

$$\boldsymbol{J}_p = -q\boldsymbol{D}_p \nabla \boldsymbol{p} - q\mu_p \boldsymbol{p} \nabla \psi \tag{4.7}$$

where, $\boldsymbol{D_n}$ is the electron diffusion coefficient, $\boldsymbol{\mu_n}$ is the electron mobility, $\boldsymbol{D_p}$ is the hole diffusion coefficient, and $\boldsymbol{\mu_p}$ is the hole mobility.

The electron and hole concentrations are related to the electrostatic potential as shown by the Fermi-Dirac probability distribution [56]. The electron and the hole densities are shown in the following, respectively

$$\boldsymbol{n} = \boldsymbol{n}_i \exp\left(\frac{\psi - \phi_n}{\frac{\boldsymbol{KT}}{\boldsymbol{q}}}\right) \tag{4.8}$$

$$\boldsymbol{p} = \boldsymbol{n}_i \exp\left(\frac{\phi_p - \psi}{\frac{\boldsymbol{KT}}{\boldsymbol{q}}}\right) \tag{4.9}$$

where, K is the Boltzmann's constant, T is the absolute temperature in Kelvin, n_i is the intrinsic carrier concentration of the semiconductor, and ϕ_n and ϕ_p are the Electron Quasi Fermi Potential (***EQFP***) and Hole Quasi Fermi Potential (***HQFP***), respectively. Two explicit variables, Φ_n and Φ_p, are defined in order to express the transport equation in linear form [34]. These two variables are expressed below, respectively, as

$$\Phi_n = \exp\left(-\frac{\phi_n}{\frac{KT}{q}}\right) \tag{4.10}$$

$$\Phi_p = \exp\left(\frac{\phi_p}{\frac{KT}{q}}\right). \tag{4.11}$$

Therefore, the electron and the hole densities are given by the following equations, respectively, in terms of these explicit variables

$$n = n_i \Phi_n \exp\left(\frac{\psi}{\frac{KT}{q}}\right) \tag{4.12}$$

$$p = n_i \Phi_p \exp\left(-\frac{\psi}{\frac{KT}{q}}\right). \tag{4.13}$$

The electron and hole current densities can be expressed in terms of electrostatic potential and the explicit variables. Replacing n in Equation 4.6 with the results from Equation 4.12 results in

$$J_n = qD_n \nabla \left(n_i \Phi_n \exp\left(\frac{\psi}{\frac{KT}{q}} \right) \right) - q\mu_n n_i \Phi_n \exp\left(\frac{\psi}{\frac{KT}{q}} \right) \nabla \psi \quad . \tag{4.14}$$

Expanding the derivative of the first term in Equation 4.14 provides

$$J_n = \begin{pmatrix} qD_n n_i \exp\left(\frac{\psi}{\frac{KT}{q}} \right) \nabla \Phi_n + qD_n n_i \Phi_n \exp\left(\frac{\psi}{\frac{KT}{q}} \right) \frac{1}{\frac{KT}{q}} \nabla \psi \\ - q\mu_n n_i \Phi_n \exp\left(\frac{\psi}{\frac{KT}{q}} \right) \nabla \psi \end{pmatrix} . \tag{4.15}$$

The relationship between the carrier mobility and carrier diffusion coefficient is provided by Einstein's relation in the following formula

$$\frac{D}{\mu} = \frac{KT}{q} \tag{4.16}$$

Where, D is the diffusion coefficient of the carriers (electron/hole) and μ is the carrier mobility. Replacing D_n in Equation 4.15 with Einstein's relation provides

$$J_n = \begin{pmatrix} qD_n n_i \exp\left(\frac{\psi}{\frac{KT}{q}} \right) \nabla \Phi_n + q\mu_n n_i \Phi_n \exp\left(\frac{\psi}{\frac{KT}{q}} \right) \nabla \psi \\ - q\mu_n n_i \Phi_n \exp\left(\frac{\psi}{\frac{KT}{q}} \right) \nabla \psi \end{pmatrix} . \tag{4.17}$$

After cancelling the second and third terms, Equation 4.17 reduces to

$$J_n = qD_n n_i \exp\left(\frac{\psi}{\frac{KT}{q}}\right)\nabla\Phi_n \quad . \tag{4.18}$$

Replacing Φn in Equation 4.18 with Equation 4.10

$$J_n = qD_n n_i \exp\left(\frac{\psi}{\frac{KT}{q}}\right)\nabla\left(\exp\left(-\frac{\phi_n}{\frac{KT}{q}}\right)\right). \tag{4.19}$$

Expanding the derivative in Equation 4.19 gives

$$J_n = -q\frac{\frac{D_n}{KT}}{q} n_i \exp\left(\frac{\psi-\phi_n}{\frac{KT}{q}}\right)\nabla\phi_n \quad . \tag{4.20}$$

Using Equation 4.8 and Equation 4.16 in Equation 4.20 provides

$$J_n = -q\mu_n n\nabla\phi_n . \tag{4.21}$$

Similarly, replacing p in Equation 4.7 with the results from Equation 4.13 is depicted as

$$J_p = -qD_p\nabla\left(n_i\Phi_p \exp\left(-\frac{\psi}{\frac{KT}{q}}\right)\right) - q\mu_p n_i\Phi_p \exp\left(-\frac{\psi}{\frac{KT}{q}}\right)\nabla\psi \quad . \tag{4.22}$$

Expanding the derivative at the first term in Equation 4.22 shows

$$\boldsymbol{J}_p = \begin{pmatrix} -q\boldsymbol{D}_p \boldsymbol{n}_i \exp\left(-\dfrac{\psi}{\dfrac{\boldsymbol{KT}}{\boldsymbol{q}}}\right)\nabla\Phi_p + q\boldsymbol{D}_p \boldsymbol{n}_i \Phi_p \exp\left(-\dfrac{\psi}{\dfrac{\boldsymbol{KT}}{\boldsymbol{q}}}\right)\dfrac{\boldsymbol{1}}{\dfrac{\boldsymbol{KT}}{\boldsymbol{q}}}\nabla\psi \\ -q\mu_p \boldsymbol{n}_i \Phi_p \exp\left(-\dfrac{\psi}{\dfrac{\boldsymbol{KT}}{\boldsymbol{q}}}\right)\nabla\psi \end{pmatrix}. \quad (4.23)$$

Replacing $\boldsymbol{D_p}$ in Equation 4.23 with the Einstein's relation provides

$$\boldsymbol{J}_p = \begin{pmatrix} -q\boldsymbol{D}_p \boldsymbol{n}_i \exp\left(-\dfrac{\psi}{\dfrac{\boldsymbol{KT}}{\boldsymbol{q}}}\right)\nabla\Phi_p + q\mu_p \boldsymbol{n}_i \Phi_p \exp\left(-\dfrac{\psi}{\dfrac{\boldsymbol{KT}}{\boldsymbol{q}}}\right)\nabla\psi \\ -q\mu_p \boldsymbol{n}_i \Phi_p \exp\left(-\dfrac{\psi}{\dfrac{\boldsymbol{KT}}{\boldsymbol{q}}}\right)\nabla\psi \end{pmatrix}. \quad (4.24)$$

After cancelling second and third terms, Equation 4.24 reduces to

$$\boldsymbol{J}_p = -q\boldsymbol{D}_p \boldsymbol{n}_i \exp\left(-\dfrac{\psi}{\dfrac{\boldsymbol{KT}}{\boldsymbol{q}}}\right)\nabla\Phi_p \quad . \quad (4.25)$$

Replacing $\boldsymbol{\Phi_p}$ in Equation 4.26 with Equation 4.11 gives

$$\boldsymbol{J}_p = -q\boldsymbol{D}_p \boldsymbol{n}_i \exp\left(-\dfrac{\psi}{\dfrac{\boldsymbol{KT}}{\boldsymbol{q}}}\right)\nabla\left(\exp\left(\dfrac{\phi_p}{\dfrac{\boldsymbol{KT}}{\boldsymbol{q}}}\right)\right). \quad (4.26)$$

Expanding the derivative in Equation 4.26 provides

$$J_p = -q\frac{D_p}{\frac{KT}{q}} n_i \exp\left(\frac{\phi_p - \psi}{\frac{KT}{q}}\right)\nabla\phi_p \quad . \tag{4.27}$$

Using Equation 4.9 and Equation 4.16 in Equation 4.27

$$J_p = -q\mu_p p\nabla\phi_p \quad . \tag{4.28}$$

The total current is given by Equation 4.29 [56]

$$J = J_p + J_n \quad . \tag{4.29}$$

Equation 4.1, Equation 4.4, Equation 4.5, Equation 4.21, and Equation 4.28 are the five fundamental equations for device simulation for three quantities, namely ***EP*** (ψ), ***EQFP*** (ϕ_n), and ***HQFP*** (ϕ_p). Equation 4.21 and Equation 4.28 involve differentiation of the exponential functions that introduce large errors when these equations are solved by finite difference method. Equation 4.18 and Equation 4.25 are alternative forms of Equation 4.21 and Equation 4.28, respectively, in terms of the linear explicit variables, Φ_n and Φ_p, as defined earlier. The error due to the differentiation of exponential functions can be eliminated by using the linear Equation 4.18 and Equation 4.25.

4.4 G^{4}FET Transport Model Equations and Boundary Conditions

For the semiconductor device analysis, the electric field, the electron, and the hole concentrations represent the state of a region of semiconductor material [32]. Equivalent information is provided via an alternate set of parameters: the electrostatic potential (***EP***), the electron, and the hole quasi Fermi potentials (***EQFP***, ***HQFP***) [57]. A useful and

computationally efficient variant exists that utilizes two explicit variables derived from ***EQFP*** and ***HQFP*** [34].

4.4.1 Driving Formulae

The only active material in the device is **Si**. There are $\mathbf{SiO_2}$ regions in a few sections portions of the device, but their effect comes through only the boundary conditions, and will be described later. Therefore, an isotropic permittivity can be considered for the material system. According to this, assumption Equation 4.1 reduces to

$$\nabla^2\psi = -\frac{q}{\varepsilon_{Si}}\left(p - n + N\right) \tag{4.30}$$

where, ε_{Si} is the isotropic electrical permittivity of **Si**. Replacing n and p in Equation 4.30 with Equation 4.12 and Equation 4.13, respectively, provides

$$\nabla^2\psi = -\frac{q}{\varepsilon_{Si}}\left(n_i\Phi_p \exp\left(-\frac{\psi}{\frac{KT}{q}}\right) - n_i\Phi_n \exp\left(\frac{\psi}{\frac{KT}{q}}\right) + N\right). \tag{4.31}$$

In the case of steady state conduction, all the time dependent terms in any equation should equate to zero. As a result, Equation 4.4 and Equation 4.5 can be rewritten as

$$\nabla . J_n = qR \tag{4.32}$$

$$-\nabla . J_p = qR \tag{4.33}$$

Using Equation 4.18 and Equation 4.25 in Equation 4.32 and Equation 4.33 respectively, provides

$$\nabla\left(D_n n_i \exp\left(\frac{\psi}{\frac{KT}{q}}\right)\nabla\Phi_n\right) = R \tag{4.34}$$

$$\nabla\left(D_p n_i \exp\left(-\frac{\psi}{\frac{KT}{q}}\right)\nabla\Phi_p\right) = R \tag{4.35}$$

.

Therefore, the system reduces to three equations (Equation 4.31, Equation 4.34 and Equation 4.35), for the three unknown quantities, ψ, Φ_n and Φ_p. These three equations are nonlinear, second-order, partial differential equations. In order to solve for the unknown quantities, the three nonlinear equations are expanded into linear equations with the appropriate approximations and mathematical techniques.

The linearization technique of Equation 4.31 involves replacing ψ with $\psi + \delta$ [32], where, δ is the error between the available trial solution and the exact solution.

Let

$$\psi \Rightarrow \psi + \delta \,. \tag{4.36}$$

Substituting Equation 4.36 into Equation 4.31

$$\nabla^2(\psi + \delta) = -\frac{q}{\varepsilon_{Si}}\left(n_i\Phi_p \exp\left(-\frac{\psi+\delta}{\frac{KT}{q}}\right) - n_i\Phi_n \exp\left(\frac{\psi+\delta}{\frac{KT}{q}}\right) + N\right) \tag{4.37}$$

$$\nabla^2\psi + \nabla^2\delta = -\frac{q}{\varepsilon_{Si}} n_i \begin{pmatrix} \Phi_p \exp\left(-\frac{\psi}{\frac{KT}{q}}\right)\exp\left(-\frac{\delta}{\frac{KT}{q}}\right) \\ -\Phi_n \exp\left(\frac{\psi}{\frac{KT}{q}}\right)\exp\left(\frac{\delta}{\frac{KT}{q}}\right) \end{pmatrix} - \frac{q}{\varepsilon_{Si}} N \quad . \qquad (4.38)$$

The exponent of a variable x can be expressed as

$$\exp(x) = 1 + \frac{(x)^1}{1!} + \frac{(x)^2}{2!} + ... + \frac{(x)^n}{n!} \quad . \qquad (4.39)$$

The truncated form of Equation 4.39 up to the second term is

$$\exp(x) = 1 + \frac{(x)^1}{1!} + O(x^2) \quad . \qquad (4.40)$$

Using Equation 4.40, Equation 4.38 can be written as

$$\nabla^2\psi + \nabla^2\delta = -\frac{q}{\varepsilon_{Si}} \begin{pmatrix} n_i\Phi_p \exp\left(-\frac{\psi}{\frac{KT}{q}}\right)\left(1-\frac{\delta}{\frac{KT}{q}}\right) \\ -n_i\Phi_n \exp\left(\frac{\psi}{\frac{KT}{q}}\right)\left(1+\frac{\delta}{\frac{KT}{q}}\right) \end{pmatrix} + \frac{q}{\varepsilon_{Si}} N + O(\delta^2) \quad . \qquad (4.41)$$

Rearranging the different terms provides

$$\left(\nabla^2 - \frac{q}{\varepsilon_{Si}}\frac{1}{\frac{KT}{q}} n_i \left(\Phi_p \exp\left(-\frac{\psi}{\frac{KT}{q}}\right) + \Phi_n \exp\left(\frac{\psi}{\frac{KT}{q}}\right)\right)\right)\delta$$
$$= -\nabla^2\psi - \frac{q}{\varepsilon_{Si}} n_i \left(\Phi_p \exp\left(-\frac{\psi}{\frac{KT}{q}}\right) - \Phi_n \exp\left(\frac{\psi}{\frac{KT}{q}}\right)\right) - \frac{q}{\varepsilon_{Si}} N + O(\delta^2) \quad . \qquad (4.42)$$

Neglecting terms of the second order and the higher order, Equation 4.42 can be considered a linear differential equation for δ, and written as

$$\left(\nabla^2 - \frac{q}{\varepsilon_{Si}}\frac{1}{\frac{KT}{q}} n_i \left(\Phi_p \exp\left(-\frac{\psi}{\frac{KT}{q}}\right) + \Phi_n \exp\left(\frac{\psi}{\frac{KT}{q}}\right)\right)\right)\delta$$
$$= -\nabla^2\psi - \frac{q}{\varepsilon_{Si}} n_i \left(\Phi_p \exp\left(-\frac{\psi}{\frac{KT}{q}}\right) - \Phi_n \exp\left(\frac{\psi}{\frac{KT}{q}}\right)\right) - \frac{q}{\varepsilon_{Si}} N \quad . \qquad (4.43)$$

Equation 4.43 is solved with a finite difference method by considering δ at a sufficiently dense set of points and converting the differential equation into a system of difference equations. Let, ***j***, ***i***, and ***k*** be the directional indices in the ***y***, ***x***, and ***z*** directions, respectively. Therefore, the equivalence central difference equation of Equation 4.43, for unequal mesh spacing, can be written as follows

$$\frac{\dfrac{\delta(j,i+1,k)-\delta(j,i,k)}{x(i+1)-x(i)}-\dfrac{\delta(j,i,k)-\delta(j,i-1,k)}{x(i)-x(i-1)}}{\dfrac{x(i+1)-x(i-1)}{2}}+\frac{\dfrac{\delta(j+1,i,k)-\delta(j,i,k)}{y(j+1)-y(j)}-\dfrac{\delta(j,i,k)-\delta(j-1,i,k)}{x(i)-x(i-1)}}{\dfrac{y(j+1)-y(j-1)}{2}}$$

$$+\frac{\dfrac{\delta(j,i,k+1)-\delta(j,i,k)}{z(k+1)-z(k)}-\dfrac{\delta(j,i,k)-\delta(j,i,k-1)}{z(k)-z(k-1)}}{\dfrac{z(k+1)-z(k-1)}{2}}-\frac{q}{\varepsilon_{Si}}\frac{1}{\dfrac{KT}{q}}n_i\left(\begin{array}{l}\Phi_p(j,i,k)\exp\left(-\dfrac{\psi(j,i,k)}{\dfrac{KT}{q}}\right)\\ +\Phi_n(j,i,k)\exp\left(\dfrac{\psi(j,i,k)}{\dfrac{KT}{q}}\right)\end{array}\right)\delta(j,i,k)$$

$$=\frac{\dfrac{\psi(j,i+1,k)-\psi(j,i,k)}{x(i+1)-x(i)}-\dfrac{\psi(j,i,k)-\psi(j,i-1,k)}{x(i)-x(i-1)}}{\dfrac{x(i+1)-x(i-1)}{2}}+\frac{\dfrac{\psi(j+1,i,k)-\psi(j,i,k)}{y(j+1)-y(j)}-\dfrac{\psi(j,i,k)-\psi(j-1,i,k)}{y(j)-y(j-1)}}{\dfrac{y(j+1)-y(j-1)}{2}}$$

$$+\frac{\dfrac{\psi(j,i,k+1)-\psi(j,i,k)}{z(k+1)-z(k)}-\dfrac{\psi(j,i,k)-\psi(j,i,k-1)}{z(k)-z(k-1)}}{\dfrac{z(k+1)-z(k-1)}{2}}-\frac{q}{\varepsilon_{Si}}\left(\begin{array}{l}n_i\Phi_p(j,i,k)\exp\left(-\dfrac{\psi(j,i,k)}{\dfrac{KT}{q}}\right)\\ -n_i\Phi_n(j,i,k)\exp\left(\dfrac{\psi(j,i,k)}{\dfrac{KT}{q}}\right)\end{array}\right)-\frac{q}{\varepsilon_{Si}}N(j,i,k) \tag{4.44}$$

At this point, ψ, $\boldsymbol{D_n}$, $\boldsymbol{D_p}$, and ***R*** are considered known quantities for Equation 4.34 and Equation 4.35. These linear equations are replaced by two sets of difference equations for $\boldsymbol{\Phi_n}$

and Φ_p. The difference equation for Equation 4.34 at point (***x(i)***, ***y(j)***, and ***z(k)***) is given by Equation 4.45

$$\frac{a_n\left(i+\frac{1}{2},k\right)\left(\Phi_n(i+1,k)-\Phi_n(i,k)\right)}{x(i+1)-x(i)}-\frac{a_n\left(i-\frac{1}{2},k\right)\left(\Phi_n(i-1,k)-\Phi_n(i,k)\right)}{x(i)-x(i-1)}$$
$$\frac{x(i+1)-x(i-1)}{2}$$
$$+\frac{\frac{a_n\left(+\frac{1}{2},i,k\right)\left(\Phi_n(+1,i,k)-\Phi_n(i,k)\right)}{y(j+1)-y(j)}-\frac{a_n\left(-\frac{1}{2},i,k\right)\left(\Phi_n(-1,i,k)-\Phi_n(i,k)\right)}{y(j)-y(j-1)}}{\frac{y(j+1)-y(j-1)}{2}}$$
$$+\frac{\frac{a_n\left(i,k+\frac{1}{2}\right)\left(\Phi_n(i,k+1)-\Phi_n(i,k)\right)}{z(k+1)-z(k)}-\frac{a_n\left(i,k-\frac{1}{2}\right)\left(\Phi_n(i,k-1)-\Phi_n(i,k)\right)}{z(k)-z(k-1)}}{\frac{z(k+1)-z(k-1)}{2}}$$
$$=\frac{R}{n_i} \tag{4.45}$$

where,

$$a_n(i,k)=D_n(i,k)\exp\left(\frac{\psi(i,k)}{\frac{KT}{q}}\right) \tag{4.46}$$

$$a_n\left(\pm\frac{1}{2},i,k\right)=\frac{D_n(\pm1,i,k)+D_n(i,k)}{2}\exp\left(\frac{\frac{\psi(\pm1,i,k)+\psi(i,k)}{2}}{\frac{KT}{q}}\right) \tag{4.47}$$

$$a_n(i,i\pm1,k)=\frac{D_n(i,i\pm1,k)+D_n(i,i,k)}{2}\exp\left(\frac{\frac{\psi(i,i\pm1,k)+\psi(i,i,k)}{2}}{\frac{KT}{q}}\right) \tag{4.48}$$

$$a_n(i,k\pm1)=\frac{D_n(i,k\pm1)+D_n(i,k)}{2}\exp\left(\frac{\frac{\psi(i,k\pm1)+\psi(i,k)}{2}}{\frac{KT}{q}}\right) \quad (4.49)$$

The difference equation for Equation 4.35 at point (***x(i)***, ***y(j)***, and ***z(k)***) is given by Equation 4.50

$$\frac{\frac{a_n(i+\frac{1}{2},k)(\Phi_p(i+1,k)-\Phi_p(i,k))}{x(i+1)-x(i)}-\frac{a_n(i-\frac{1}{2},k)(\Phi_p(i-1,k)-\Phi_p(i,k))}{x(i)-x(i-1)}}{\frac{x(i+1)-x(i-1)}{2}}$$
$$+\frac{\frac{a_n(i+\frac{1}{2},i,k)(\Phi_p(i+1,i,k)-\Phi_p(i,i,k))}{y(j+1)-y(j)}-\frac{a_n(i-\frac{1}{2},i,k)(\Phi_p(i-1,i,k)-\Phi_p(i,i,k))}{y(j)-y(j-1)}}{\frac{y(j+1)-y(j-1)}{2}}$$
$$+\frac{\frac{a_n(i,k+\frac{1}{2})(\Phi_p(i,k+1)-\Phi_p(i,k))}{z(k+1)-z(k)}-\frac{a_n(i,k-\frac{1}{2})(\Phi_p(i,k-1)-\Phi_p(i,k))}{z(k)-z(k-1)}}{\frac{z(k+1)-z(k-1)}{2}}$$
$$=\frac{R}{n_i} \quad (4.50)$$

where,

$$a_p(i,k)=D_p(i,k)\exp\left(-\frac{\psi(i,k)}{\frac{KT}{q}}\right) \quad (4.51)$$

$$a_p(i\pm\tfrac{1}{2},k)=\frac{D_p(i\pm1,k)+D_p(i,k)}{2}\exp\left(-\frac{\frac{\psi(i\pm1,k)+\psi(i,k)}{2}}{\frac{KT}{q}}\right) \quad (4.52)$$

$$a_p\left(i,i\pm\tfrac{1}{2},k\right)=\frac{D_p\left(i,i\pm1,k\right)+D_p\left(i,i,k\right)}{2}\exp\left(-\frac{\frac{\psi\left(i,i\pm1,k\right)+\psi\left(i,i,k\right)}{2}}{\frac{KT}{q}}\right) \quad (4.53)$$

$$a_p\left(i,i,k\pm\tfrac{1}{2}\right)=\frac{D_p\left(i,i,k\pm1\right)+D_p\left(i,i,k\right)}{2}\exp\left(-\frac{\frac{\psi\left(i,i,k\pm1\right)+\psi\left(i,i,k\right)}{2}}{\frac{KT}{q}}\right) \quad (4.54)$$

As described in Chapter Three, the carriers in the channel are confined in a 2-D potential well. Therefore, the energy state in the conduction and valance bands are quantized. In order to include the effect of quantization time independent of the 2-D Schrödinger's equation is solved.

The time independent Schrödinger equation is given by

$$-\frac{\hbar^2}{2m^*}\nabla^2\omega+\psi\omega=E_n\omega \quad (4.55)$$

where $\hbar$ is the reduced Planck's constant given by

$$\hbar=\frac{h}{2\pi} \quad (4.56)$$

where m^* is the effective mass of the carriers, ω is the wave function of the carriers, and E_n quantized energy states. Discretizing Equation 4.55 yields

$$-\frac{\hbar^2}{2m^*}\left(\begin{array}{l}\frac{\omega\left(i+1,i,k\right)-2\omega\left(i,i,k\right)+\omega\left(i-1,i,k\right)}{dy^2}\\+\frac{\omega\left(i,i,k+1\right)-2\omega\left(i,i,k\right)+\omega\left(i,i,k-1\right)}{dz^2}\end{array}\right)+\psi\left(i,i,k\right)\omega\left(i,i,k\right)=E_n\omega\left(i,i,k\right) \quad (4.57)$$

4.4.2 Boundary Conditions

The partial differential equations are subjected to the appropriate boundary conditions. A unique solution for the partial differential equation is obtained by applying appropriate boundary conditions. The boundary conditions are imposed at the edges of the material or at the interface of the two materials. According to the device structure, there are three types of boundaries present in the device: (1) ohmic contact; (2) boundary without contact; and (3) interface between two materials. Each of the boundaries enforces various restrictions on different unknown variables.

4.4.2.1 Ohmic contact

Ohmic contact is produced between the interface of highly doped semiconductor and metal. In this device, there are four ohmic contacts. Among these, two are source and drain contacts and two are junction gates. Charge neutrality and thermal equilibrium conditions are assumed at the ohmic contacts [57]. These conditions are justified for ideal contacts, on which excess carriers immediately vanish. In other words, they possess an infinite recombination rate, as shown in the following equations

$$n_0 + N_A^- = p_0 + N_D^+ \tag{4.58}$$

$$n_0 p_0 = n_i^2 \tag{4.59}$$

where n_0 and p_0 are the mobile carrier density of electrons and holes respectively at thermal equilibrium and N^+_D and N^-_A are the ionized donor and acceptor concentrations, respectively. From Equation 4.59, Equation 4.60 can be extrapolated

$$p_0 = \frac{n_i^2}{n_0} \quad . \tag{4.60}$$

Replacing p_0 in Equation 4.58 provides

$$n_0 - \frac{n_i^2}{n_0} = N_D^+ - N_A^- \quad . \tag{4.61}$$

After rearranging and solving for n_0, the equation becomes

$$n_0 = \sqrt{\frac{\left(N_D^+ - N_A^-\right)^2}{4} + n_i^2} + \frac{N_D^+ - N_A^-}{2} \quad . \tag{4.62}$$

Similarly, p_0 can be written as

$$p_0 = \sqrt{\frac{\left(N_D^+ - N_A^-\right)^2}{4} + n_i^2} - \frac{N_D^+ - N_A^-}{2} \quad . \tag{4.63}$$

Substituting n_0 and p_0 in Equation 4.58 via Equation 4.8 and Equation 4.9, respectively, produces

$$n_i \exp\left(\frac{\psi - \phi_n}{\frac{KT}{q}}\right) - n_i \exp\left(\frac{\phi_p - \psi}{\frac{KT}{q}}\right) = N_D^+ - N_A^- \quad . \tag{4.64}$$

For the condition of thermal equilibrium in Equation 4.59, $\phi_n = \phi_p$. Lets define this equilibrium value as $\phi_n = \phi_p = \phi_f$, shown below

$$n_i \exp\left(\frac{\psi - \phi_f}{\frac{KT}{q}}\right) - n_i \exp\left(\frac{\phi_f - \psi}{\frac{KT}{q}}\right) = N_D^+ - N_A^- \tag{4.65}$$

$$n_i \exp\left(\frac{\psi - \phi_f}{\frac{KT}{q}}\right) - n_i \exp\left(-\frac{\psi - \phi_f}{\frac{KT}{q}}\right) = N_D^+ - N_A^- \tag{4.66}$$

$$2n_i \sinh^{-1}\left(\frac{\psi - \phi_f}{\frac{KT}{q}}\right) = N_D^+ - N_A^- \tag{4.67}$$

$$\sinh^{-1}\left(\frac{\psi - \phi_f}{\frac{KT}{q}}\right) = \frac{N_D^+ - N_A^-}{2n_i} \tag{4.68}$$

$$\psi = \phi_f + \frac{KT}{q}\sinh^{-1}\left(\frac{N_D^+ - N_A^-}{2n_i}\right) . \tag{4.69}$$

At the ohmic contact, equilibrium Fermi potential is equal to the applied voltage at the contact. Therefore, if V is the applied potential at the ohmic contact, then

$$\psi = V + \frac{KT}{q}\sinh^{-1}\left(\frac{N_D^+ - N_A^-}{2n_i}\right) . \tag{4.70}$$

4.4.2.2 Boundaries without contacts

A metal free semiconductor surface is characterized by a zero recombination that is opposite to the ideal ohmic metal electrode [57]. On such a surface, it is reasonable to assume a zero normal component for the electron and the hole current density

$$\overrightarrow{J_n}.\vec{\eta} = 0 \tag{4.71}$$

$$\overrightarrow{J_p}.\vec{\eta} = 0 \tag{4.72}$$

where, η is the unit vector normal to the surface. This means that both the drift and diffusion of both carriers are zero normal to the surface. The condition of zero drift current is satisfied by

$$\vec{E}.\vec{\eta} = -\frac{d\psi}{d\eta} = 0 \tag{4.73}$$

where, $\boldsymbol{E}$ is the electric field and the condition of zero diffusion current is satisfied by

$$\frac{dn}{d\eta} = 0 \tag{4.74}$$

$$\frac{dp}{d\eta} = 0 \tag{4.75}$$

.

4.4.2.3 Semiconductor/Oxide interface

At the **Si**/**SiO$_2$** interface, the boundary condition can be derived by the assumption of the continuity of electric flux density at the interface [59].

$$D_{Si} = D_{ox} \tag{4.76}$$

where D_{Si} and D_{ox} are the electric flux density in **Si** and **SiO$_2$**, respectively. From Gauss's law

$$D = \varepsilon E \tag{4.77}$$

.

Using Equation 4.77, Equation 4.76 can be written as

$$\varepsilon_{ox} E_{ox} = \varepsilon_{Si} E_{Si} \tag{4.78}$$

where ε_{ox}, E_{ox}, and E_{Si} are the electric permittivity, the electric field in the **SiO_2** at the interface, and the electric field in the **Si** at the interface. Let the **EP** at the interface be ψ_s, which is also known as surface potential. Therefore, Equation 4.78 can be written as

$$\varepsilon_{ox}\frac{V_G+\phi_m-\psi_s}{t_{ox}}=\varepsilon_{Si}\left.\frac{d\psi}{d\eta}\right|_{surface} \tag{4.79}$$

where V_G is the applied gate potential, ϕ_m is the work function of the gate material, and t_{ox} is the oxide thickness.

At the interface, both electron and hole currents densities will be zero. From Equation 4.21 and Equation 4.28, electron and hole current can only be zero if the respective Fermi levels remain constant. Therefore

$$\left.\frac{d\phi_n}{d\eta}\right|_{surface}=0 \tag{4.80}$$

$$\left.\frac{d\phi_p}{d\eta}\right|_{surface}=0 . \tag{4.81}$$

The boundary conditions for Schrodinger equations are different from those for transport equations. Thus, the boundary conditions for Schrodinger's equations are required to be treated separately. The carriers are confined in a two dimensional potential well only in the channel region and it is only reasonable to solve the Schrodinger's equation inside the channel region. The channel is surrounded by oxides and reverse biased JFET junctions. If zero leakage current occurs through the oxides and the reversed biased JFET junctions, it follows that both the magnitude and its derivatives of the wave functions are zero at those boundaries [58]. Therefore

$$\omega\big|_{surface} = 0 \quad . \tag{4.82}$$

It also requires that

$$\left.\frac{d\omega}{d\eta}\right|_{surface} = 0 \tag{4.83}$$

where, η is the direction normal to the surface.

4.4.3 Additional Parameters

There are two more parameters yet to be defined, carrier mobility and recombination-generation. These parameters appear in the transport equations and play an important role in the conduction mechanism.

4.4.3.1 Carrier mobility

The carrier mobility depends on temperature, doping density, electric field, and surface roughness.

The constant mobility model [21] assumes that the carrier mobility is only affected by phonon scattering and, therefore, is dependent only on the lattice temperature

$$\mu_{const} = \mu_L \left(\frac{T}{T_0}\right)^{-\zeta} \tag{4.84}$$

where, μ_L is the mobility due to bulk phonon scattering, T is the lattice temperature, and T_0 = 300 K. The default values and exponents are listed in Table 4.1.

The most widely used doping-dependent mobility model in silicon was proposed by Masetti et al. [23]

$$\mu_{dop} = \mu_{\min 1} \exp\left(-\frac{P_c}{N_i}\right) + \frac{\mu_{const} - \mu_{\min 2}}{1 + \left(\frac{N_i}{C_r}\right)^{\alpha}} - \frac{\mu_1}{1 + \left(\frac{C_s}{N_i}\right)^{\beta}} \tag{4.85}$$

where, $N_i = N^+_D - N^-_A$ denotes the total concentration of ionized impurities. The reference mobilities, μ_{min1}, μ_{min2}, and μ_1, the reference doping concentrations P_c, C_r, and C_s, and the exponents α and β are listed in Table 4.2.

The carrier mobility, due to inversion layer mobility degradation, which in turn is due to the aquatics phonon scattering and surface roughness, can be expressed as [60]:

$$\mu_{\perp} = \mu_{dop}\, g(E_{\perp}) \tag{4.86}$$

where, $\mu_{\perp}$ is the mobility of the electrons/holes as a function of temperature and doping concentration. The normal electric field, μ_{dop}, is the mobility of the electrons/holes as a function of temperature and doping concentration and $g(E_{\perp})$ is the degradation factor. The function of the normal electric field, $E_{\perp}$, $g(E_{\perp})$, is given by

$$g(E_{\perp}) = (1 + \alpha E_{\perp})^{1/2} \tag{4.87}$$

where, α is 1.54e-5 cm/V for electrons and 5.35e-5 cm/V for holes.

The experimental results of mobility for the normal electric field can be approximated by the empirical expression [27]

$$\mu_{hf} = \frac{\mu_{\perp}}{\left(1 + \left(\frac{\mu_{\perp} E_{||}}{v_{sat}}\right)^{\beta}\right)^{1/\beta}} \tag{4.88}$$

where, μ_{hf} is the mobility of electrons/holes as a function of the temperature and doping concentration, normal electric field, and longitudinal electric field. The exponent β is temperature dependent, according to

$$\beta = \beta_0 \left(\frac{T}{300} \right)^{\beta_{\exp}} . \tag{4.89}$$

The saturation velocity, v_{sat}, is temperature dependent, according to

$$v_{sat} = v_{sta,0} \left(\frac{300}{T} \right)^{v_{sat,\exp}} . \tag{4.90}$$

The β_0, β_{exp}, $v_{sat,0}$, and $v_{sat,exp}$ are listed in Table 4.3.

4.4.3.2 Carrier recombination-generation

Shockley-Hall-Read recombination: Recombination through deep levels in the gap is usually labeled as the Shockley–Read–Hall (SRH) recombination [28, 29].

$$R_{net}^{SRH} = \frac{np - n_i^2}{\tau_p (n + n_1) + \tau_n (p + p_1)} \tag{4.91}$$

with,

$$n_1 = n_i \exp\left(\frac{E_{trap}}{kT} \right) \tag{4.92}$$

and

$$p_1 = n_i \exp\left(-\frac{E_{trap}}{kT} \right) \tag{4.93}$$

where, E_{trap} is the difference between the defect level and the intrinsic level. The silicon default value is $E_{trap} = 0$. The minority carrier lifetimes, τ_n and τ_p, are modeled as a product of the doping-dependent and temperature-dependent factor

$$\tau_c = \tau_{dop} f(T), c = n, p \quad . \tag{4.94}$$

The doping dependence of the SRH lifetimes is modeled utilizing the relation in [61]

$$\tau_{dop}(N_i) = \tau_{\min} + \frac{\tau_{\max} - \tau_{\min}}{\left(\frac{N_i}{N_{ref}}\right)^{\gamma}} \quad . \tag{4.95}$$

The temperature dependent lifetime is given by [30]

$$\tau(T) = \tau_{dop}\left(\frac{T}{300}\right)^{\alpha} \tag{4.96}$$

The parameters for the doping- and temperature-dependent SRH lifetime are given in Table 4.4.

Surface SRH recombination: At interfaces, an additional formula is used which is structurally equivalent to the bulk expression of the SRH generation-recombination

$$R_{surf}^{SRH} = \frac{np - n_i^2}{\frac{n + n_1}{s_p} + \frac{p + p_1}{s_n}} \tag{4.97}$$

where, n_1 and p_1 are given by Equation 4.92 and Equation 4.93. The recombination velocities at the surfaces depend, in general, on the concentration of dopants [29, 31, 61].

Table 4.1: Constant mobility model: Coefficients for Silicon

Symbol	Electrons	Holes	Unit
μ_L	1417	470.5	$cm^2/(V.s)$
ζ	2.5	2.2	

Table 4.2: Coefficients for the Masetti model

Symbol	Electrons	Holes	Unit
μ_{min1}, μ_{min2}	52.2, 52.2	44.9, 0	$cm^2/(V.s)$
μ_1	43.4	29.0	$cm^2/(V.s)$
P_c	0	9.23e16	cm^{-3}
C_r	9.68e16	2.23e17	cm^{-3}
C_s	3.34e20	6.10e20	cm^{-3}
α	0.680	0.719	
β	2.0	2.0	

Table 4.3: Parameters for high field mobility

Symbol	Electrons	Holes	Unit
β_0	1.109	44.9	
β_{exp}	0.66	0	
$v_{sat,0}$	1.07e7	8.37e6	cm/s
$v_{sat,exp}$	0.87	0.52	

The doping dependence of surface recombination velocities is

$$s = s_0\left(1 + s_{ref}\left(\frac{N_i}{N_{ref}}\right)^{\gamma}\right) \quad . \tag{4.98}$$

The surface SRH parameters are given in Table 4.5.

Auger recombination: The rate of band-to-band Auger recombination is R^A given by

$$R^A = \left(C_n n + C_p p\right)\left(np - n_i^2\right) \tag{4.99}$$

with temperature-dependent Auger coefficients [22, 30]

$$C_n(T) = \left(A_{A,n} + B_{A,n}\left(\frac{T}{T_0}\right) + C_{A,n}\left(\frac{T}{T_0}\right)^2\right)\left(1 + H_n \exp\left(-\frac{n}{N_{0,n}}\right)\right) \tag{4.100}$$

$$C_p(T) = \left(A_{A,p} + B_{A,p}\left(\frac{T}{T_0}\right) + C_{A,p}\left(\frac{T}{T_0}\right)^2\right)\left(1 + H_p \exp\left(-\frac{p}{N_{0,p}}\right)\right) \quad . \tag{4.101}$$

Auger recombination is usually important at high carrier densities. Therefore, this injection dependence can only be viewed in devices where extrinsic recombination effects are extremely low, such as high-efficiency silicon solar cells. The coefficients of Auger recombination model are given in Table 4.6.

4.5 Application of carrier transport model

The application of the carrier transport model is employed to generate information about the conduction mechanism of the G^4FET. This information will guide the optimization of the device design by changing the different parameters to obtain a better performance. This approach to modeling provides information about potential and electric field distribution and

about charge distribution. The potential and electric field distributions are important to verify to determine if a device exceeded the breakdown field. Charge distribution is also important and is used to determine the conduction path. The carrier transport model predicts the existence of quantum wire in the G^4FET. Therefore, the carrier transport model is important for an understanding of the device physics.

A G^4FET device is simulated with the developed model following the algorithm as shown in Figure 4.1. A MATLAB® code was written to solve the carrier transport equations, Equation 4.44, Equation 4.45 and Equation 4.50, with several associated parameters and appropriate boundary conditions, to obtain information about three fundamental quantities: electrostatic potential, electron distribution, and hole distribution.

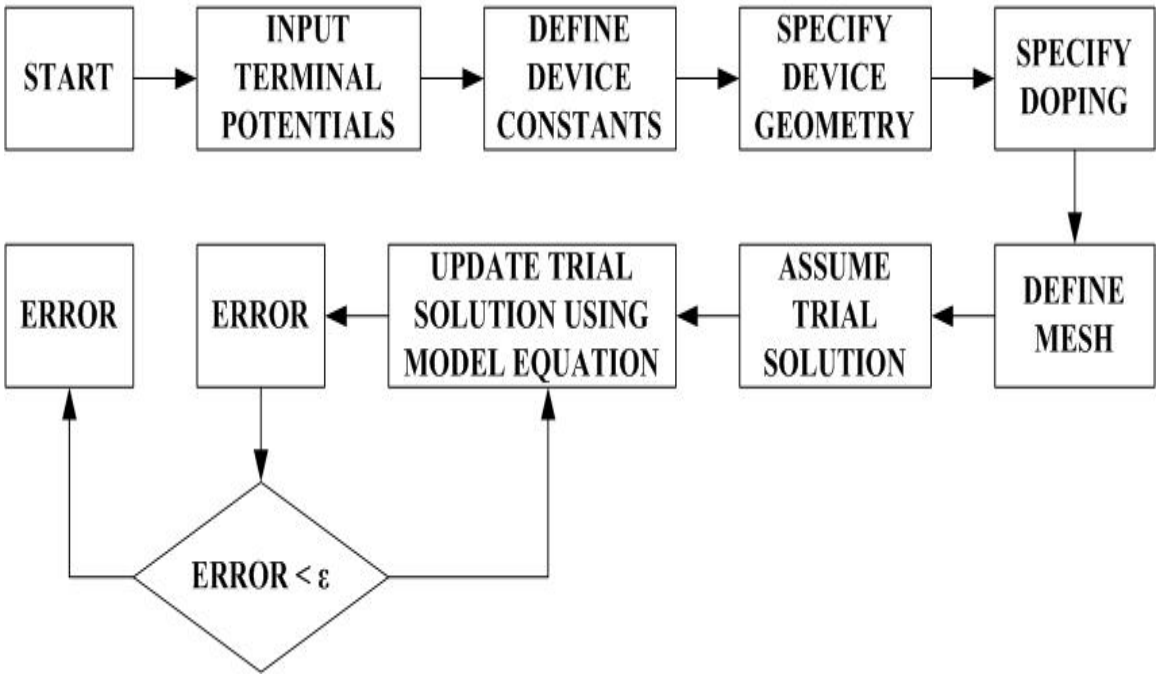


Figure 4.1: Flowchart to solve carrier transport equation.

Table 4.4: Parameters for doping- and temperature-dependent SRH lifetime

Symbol	Electrons	Holes	Unit
τ_{min}	0	0	S
τ_{max}	1e-5	1e-5	S
N_{ref}	1e16	1e16	cm^{-3}

Table 4.5: Surface SRH parameters

Symbol	Electrons	Holes	Unit
s_0	1e3	1e3	cm/s
s_{ref}	1e3	1e3	
N_{ref}	1e16	1e16	cm^{-3}
γ	1	1	
E_{trap}	0	0	eV

Table 4.6: Coefficients of the Auger recombination model

Symbol	A_A (cm^6/s)	B_A (cm^6/s)	C_A (cm^6/s)	H	N_0 (cm^{-3})
Parameter name	A	B	C	H	N_0
Electrons	0.67e-31	2.45e-31	-2.2e-32	3.46667	1e18
Holes	0.72e-31	4.50e-33	2.63e-32	8.25688	1e18

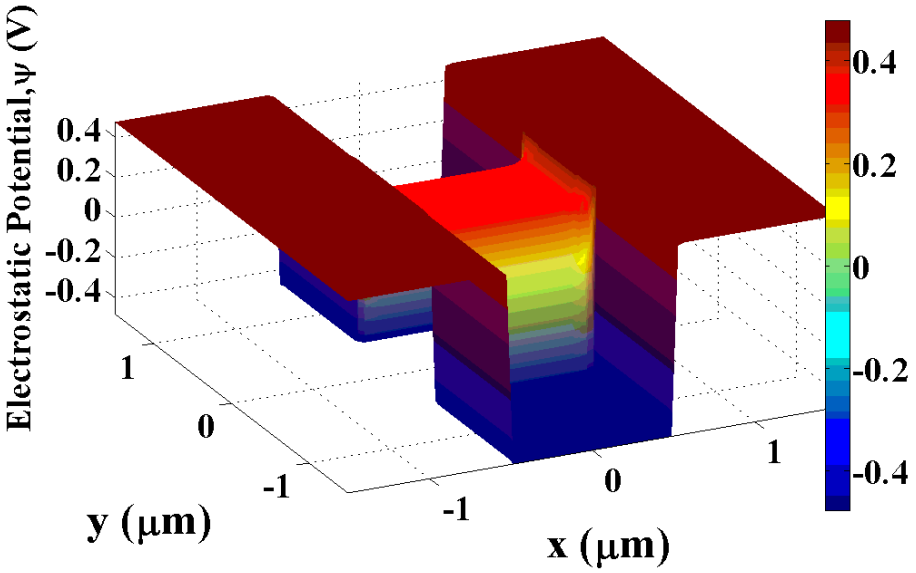
The simulation starts with different terminal potentials. Afterwards it defines different physical constants such as, Boltzmann constant, charge of an electron, etc. then it defines the device geometry and doping. After that the device is divided into a number of sections and a trial solution is approximated at each section. The trial solution is updated by using Equation 4.44, Equation 4.45 and Equation 4.50 with appropriate boundary condition. The iteration ends when the updated values and the trial solutions differ by less than a very small predefined value. The results provide valuable information about the device operation. From these result the region with of extreme electric field can be determined and counter measure can be taken in order to reduce this stress from the electric field. Moreover, the charge distribution and the potential distribution can also be obtained from this simulation. The sharing of charge between different terminals and current crowding can be observed from the charge distribution.

Figure 4.2 shows (a) 3 dimensional and (b) 2 dimensional potential distributions inside a G^4FET device under no bias condition. These figures (Figure 4.2 (a) and (b)) help to visualize the potential distribution of fabricated device. It helps to understand the location and the shape of different junctions. It is clear from the figure that there are junction between two junction gates and the source and the drain. The formation of the junction can be identified with abrupt change of both magnitude and sign of the electrostatic potential. There are also junctions between the channel and the two junction gates. It may appear there are junctions between the channel and the source and the drain. However, as described before, although the magnitude of the potentials changes at the source/channel and the drain/channel interface, the

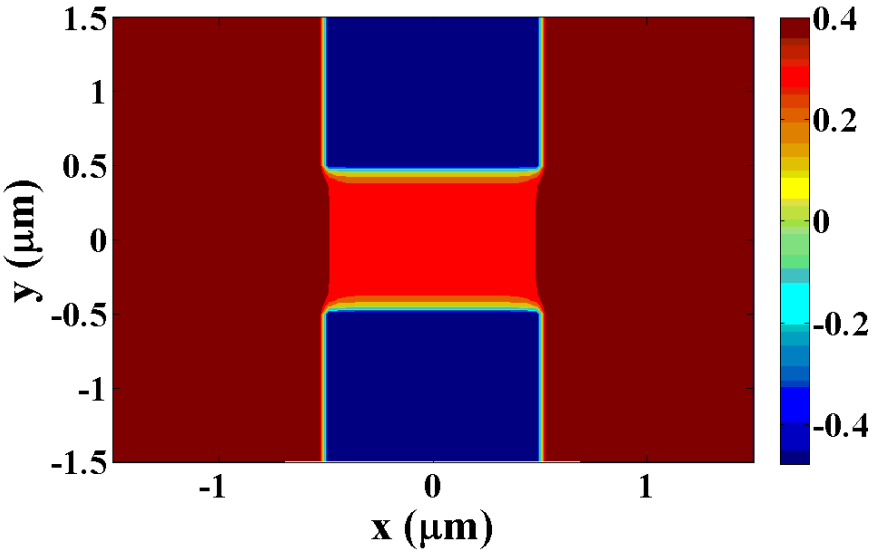
sign remain same. Therefore, the source/channel and the drain/channel form conduction paths with different potentials.

Figure 4.3 shows the electric field distribution along with potential distribution. The electric field distribution provides information about the location of maximum electric field. The location of maximum electric field has greater possibility of high voltage breakdown. If the location of maximum electric field is known, the remedial action can be taken in order to avoid possible breakdown.

Figure 4.4 shows the charge distribution of a G^4FET device under no bias condition. The charge distribution provides information about the conduction path in the channel. This figure shows that the source and drain regions are doped with high density ***n*** type material and two junctions are doped with high ***p*** type material. However, the channel id doped with ***n*** type material of moderate density. As source and drain form p-n junctions with two junction gates, current can only flow through the moderately doped channel region.



(a)



(b)

Figure 4.2: (a) 3 dimensional (b) 2 dimensional views of potential distribution under no bias condition.

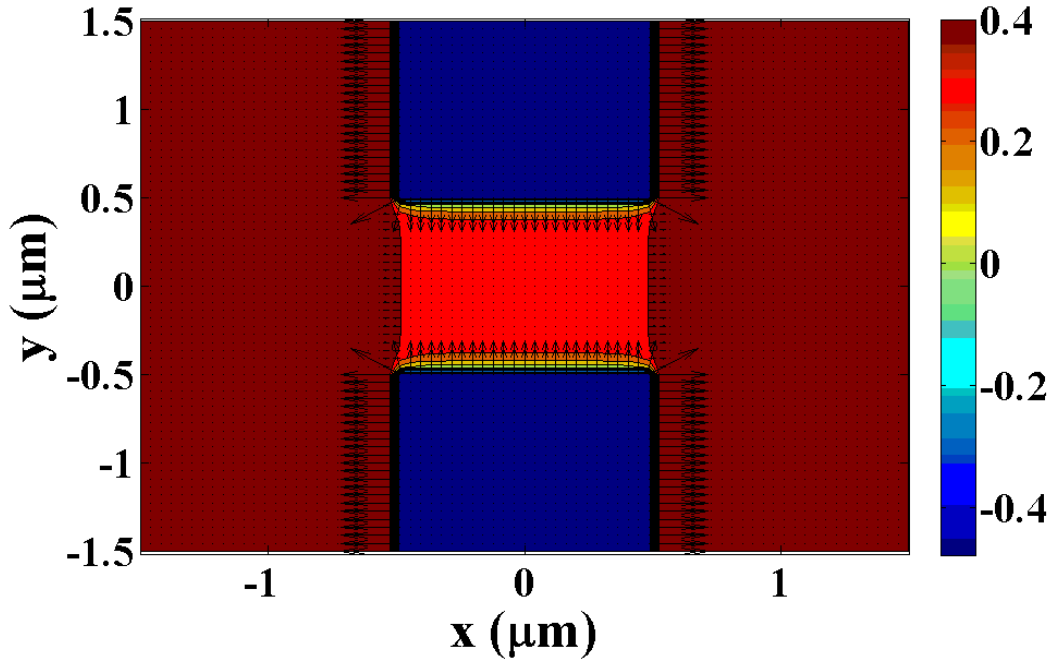


Figure 4.3: 2 dimensional view of electric field distribution under no bias condition.

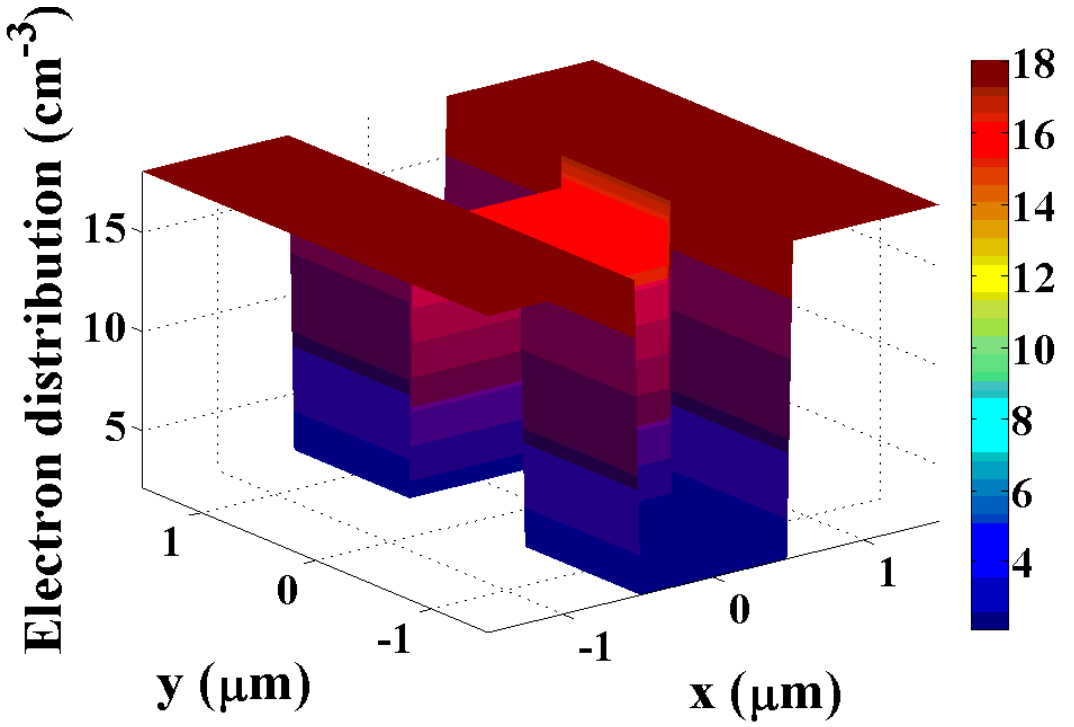
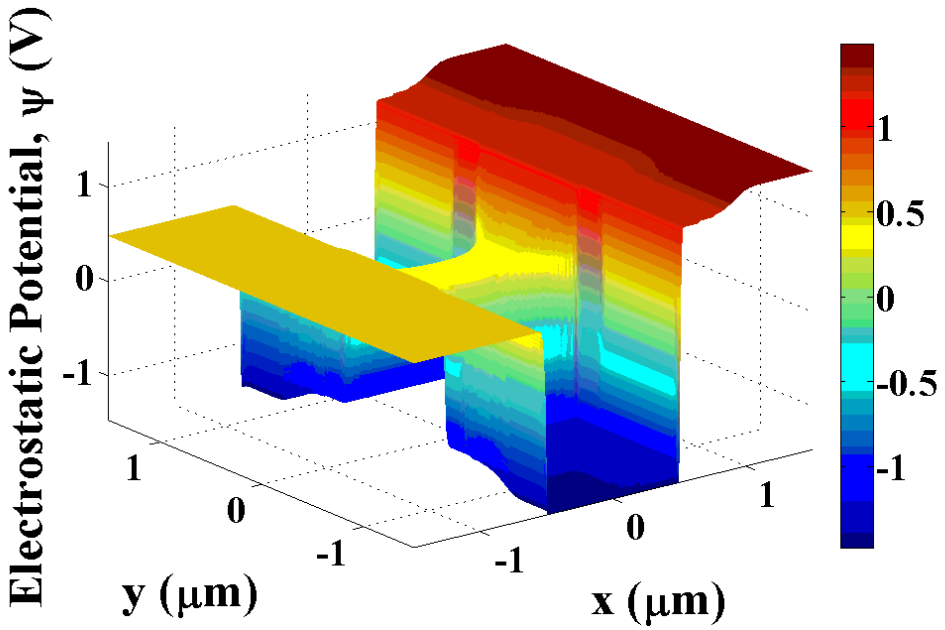


Figure 4.4: 3 dimensional view of log of electron concentration.

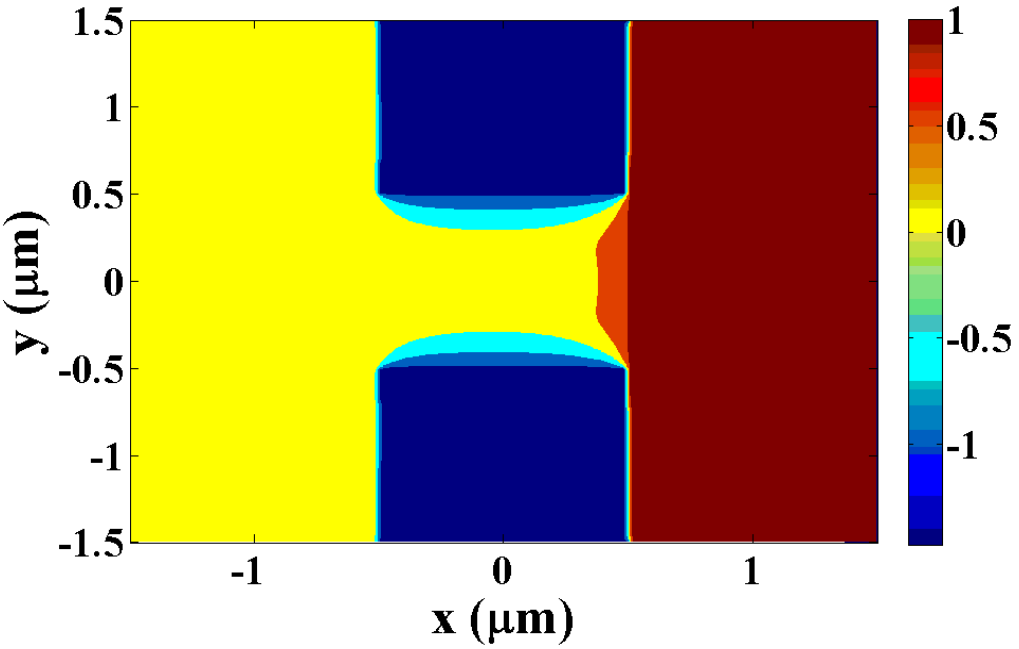
Figure 4.5 shows the potential distribution ((a) 3 dimensional and (b) 2 dimensional) of G^4FET under a certain bias condition (drain at 1V and all other terminals are grounded). The figure shows that the electrostatic potential at drain region is elevated due to application of potential, while other regions are at same potential level under no bias condition. However, there are differences in potential distributions in the channel near the drain region. The potential distribution gradually decreases from drain to source within the channel. The gradual potential distribution causes the current to flow from drain to source.

Figure 4.6 shows the electric field distribution ((a) complete cross section and (b) location of maximum electric field) of a G^4FET device with bias condition same as for Figure 4.5. It shows that the electric distribution changes from the no bias condition, due to application drain potential. The location of maximum electric field is shifted to the junction between drain and two junctions. The relocation of maximum electric field is expected as the potential difference between drain and the junction gates is greater than no bias condition.

Figure 4.7 shows the electron distribution ((a) 3 dimensional and (2) 2 dimensional) inside a G^4FET under same bias condition as for Figure 4.5. this figure shows that the electron distribution is maximum near the drain at the channel. The channel area is reduced near the drain due to the application of drain potential. in order to to maintain current continuity the electron density s increased near drain. This effect is called current crowding. Current crowding is closely related to the self heating of device. The temperature increases near the region of high current density that might lead the device into destruction.

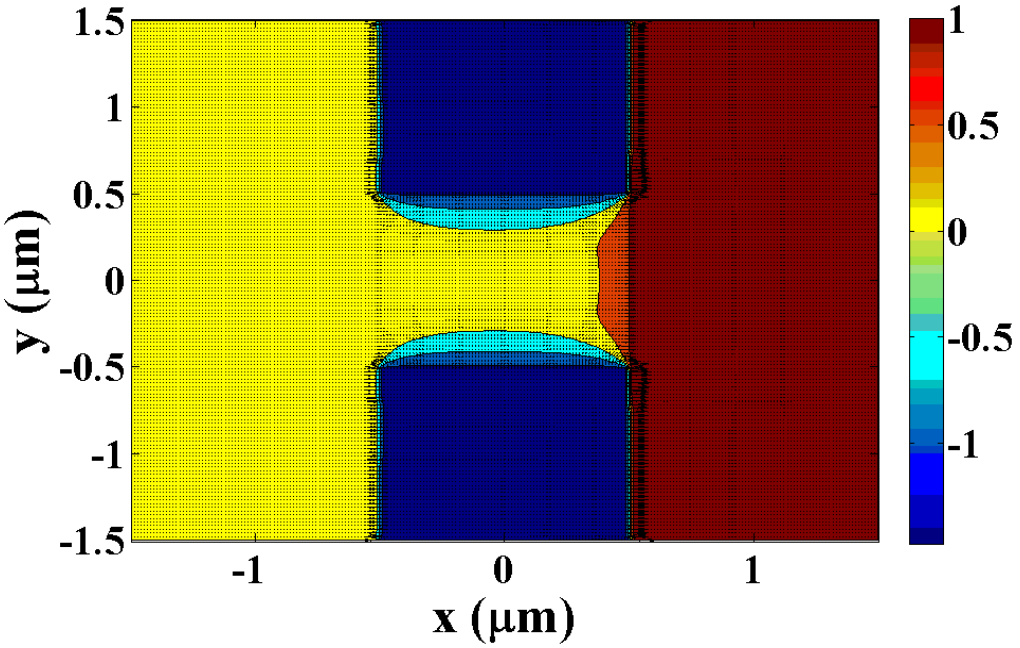


(a)

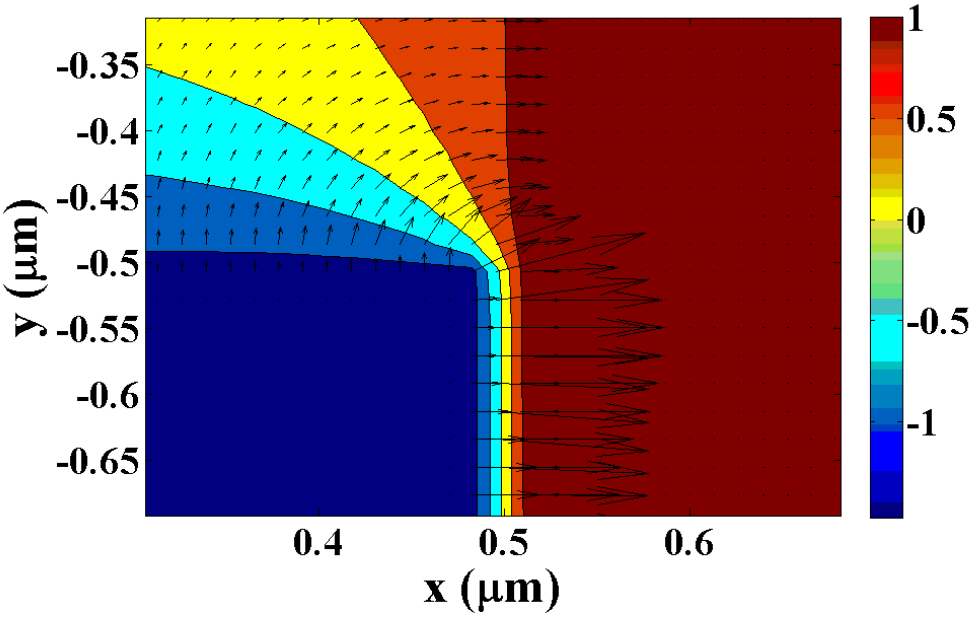


(b)

Figure 4.5: (a) 3 dimensional (b) 2 dimensional views of potential distribution with different potential at different terminals.

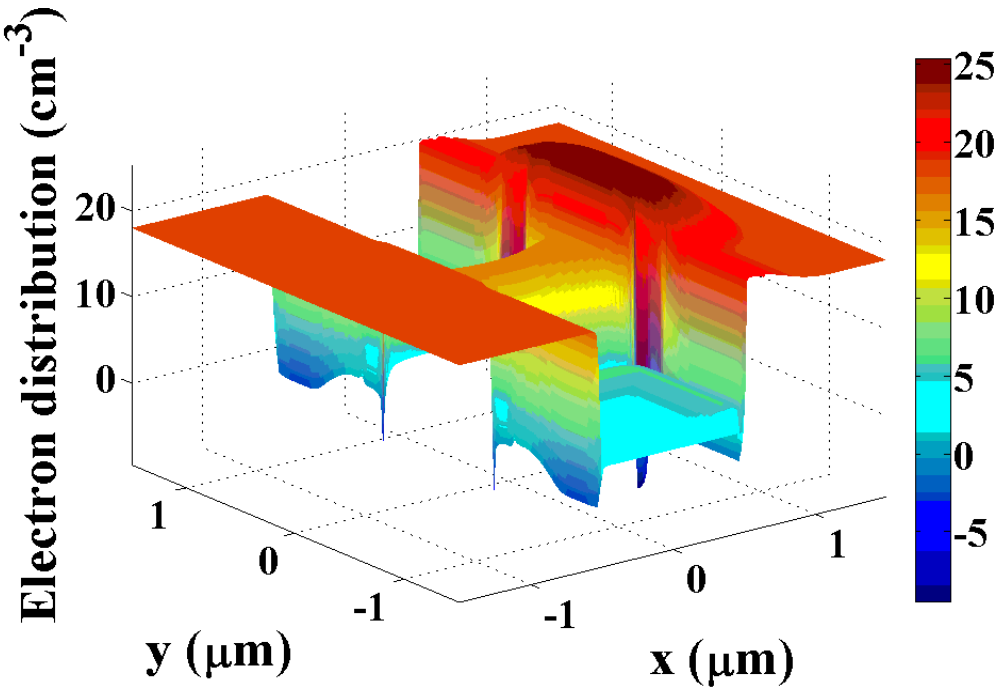


(a)

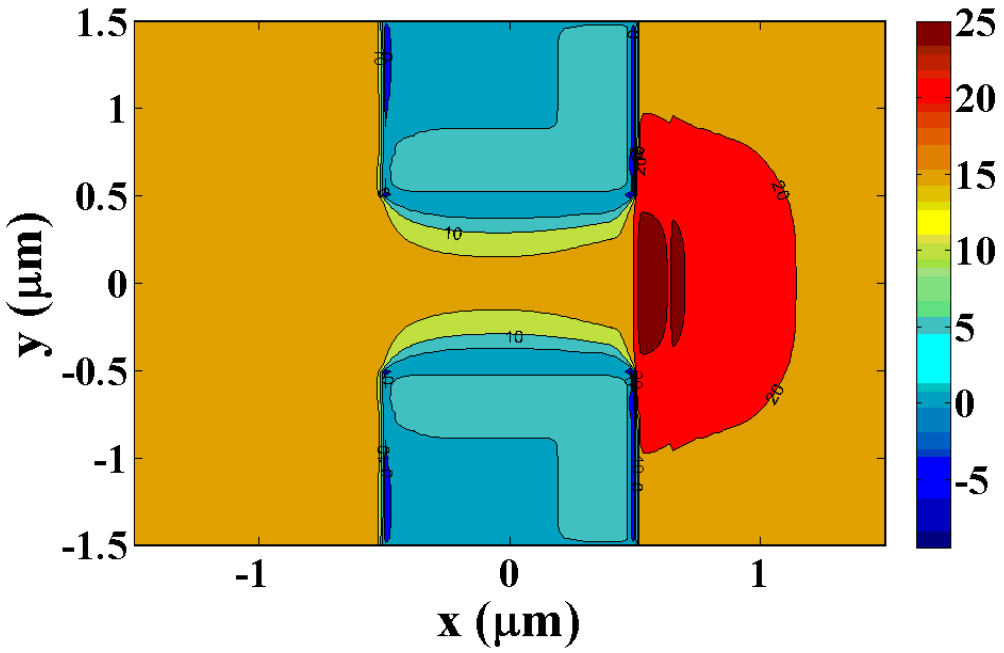


(b)

Figure 4.6: (a) 2 dimensional view of field distribution; (b) magnified view of location of maximum electric field.



(a)



(b)

Figure 4.7: (a) 3 dimensional (b) 2 dimensional views of log of electron concentration.

4.6 Chapter summary

Carrier transport model deals with different physical parameters of a device. These physical parameters include carrier mobility and recombination-generation. These parameters depend on temperature, doping, electric field, etc. Carrier transport model involves solving three coupled partial nonlinear differential equations. Due to the complex nature of these equations, this system of equations is solved with finite difference method. This model provides information about the conduction mechanism in the device. It provides information about potential distribution and electric field distribution in the device. Electric field distribution provides information of location of maximum electric field. Different remedial action can be taken once the location of maximum electric field is known. It also provides information about charge density. The location of maximum current density can be determined from the distribution of charge density. The device may be subjected to self heating due to localized high current density. If the distribution of current density is known different methods can be implied in order to distribute the current uniformly over the entire channel area.

CHAPTER FIVE

Charge Control Model of G^4FET

5.1 Motivation

As described in the previous chapter, the carrier transport model deals with the physics of carrier conduction via the semiconductor. It involves solving three coupled nonlinear differential equation simultaneously. These equations include different physical parameters such as mobility and carrier generation-recombination. These physical phenomena are complex in nature and are influenced by doping and temperature. The differential equations can become extremely complex and are sometimes analytically intractable once the exact expression of mobility and generation-recombination is inserted for better accuracy. It is customary to solve the differential equations with a finite difference method. The finite difference method involves dividing a device into a number of sections and solving for different parameters at each section. Therefore, a discrete solution is obtained instead of a continuous solution. The dimensions of these modern devices are very small. However, terminal potentials are not appropriately scaled down. Thus, different parameters change abruptly within the device. In order to get a precise solution for that region, it should be segregated into fine regions. It is not impossible, but time consuming, to solve for a large number of sections. The carrier transport method is best used in the device design step. In order to check performance, once the design is complete, it is preferable to have a model that relates to different parameters without going into the details of device physics. It may not be

as accurate as the carrier transport model, but is accurate and simple enough to obtain device characteristics quickly.

There have been several attempts to derive a charge control model [15, 20]. However, those models cover only a part of the regions of operation of a G^{4}FET.

5.2 Analytical model of G^{4}FET

Let us consider a cross section of the channel of a G^{4}FET, as shown in Figure 5.1. The figure shows there are two p-n junctions in the horizontal direction and two oxide gates in the vertical direction. The width and the height of the channel are defined by $\boldsymbol{W}$ and $\boldsymbol{H}$ respectively. $\boldsymbol{y_d}$ and $\boldsymbol{z_d}$ are the depletion width due to p-n junction and **Si**/**SiO$_2$** respectively. The potentials for top gate, back gate, junction gates are defined by $\boldsymbol{V_{TS}}$, $\boldsymbol{V_{BS}}$, and $\boldsymbol{V_{JG}}$, respectively. The area of the conduction channel is less than the geometric area by the area under the depletion region, as show in the figure. The potential at each of the gates affects the charge and potential distributions in the channel. As current is

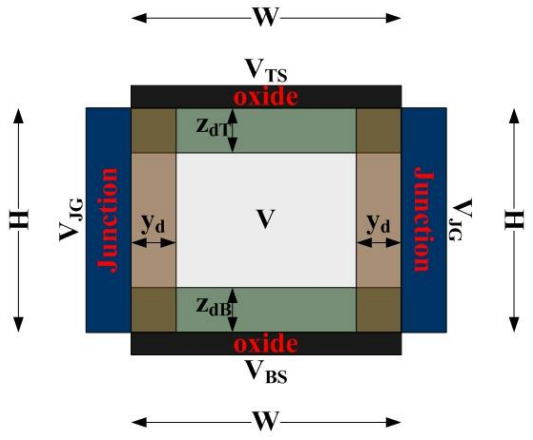


Figure 5.1: Cross section of a G^{4}FET within the channel.

directly proportional to charge, the total current through the channel can be varied by applying the potential at different gates. In order to estimate the total current, it is necessary to determine the charge and potential distributions in the channel.

In order to determine the charge and potential distribution, a 2-D Poisson equation needs to be solved. However, in small dimensional devices, the electric field in the different direction is strong enough to be considered independent. Therefore, the 2-D Poisson equation reduces to a 1 dimensional equation in each direction, as given by

$$\frac{\partial^2 \psi_y}{\partial y^2} = -\frac{\rho_y}{\varepsilon_{Si}} \tag{5.1}$$

$$\frac{\partial^2 \psi_z}{\partial z^2} = -\frac{\rho_z}{\varepsilon_{Si}} \tag{5.2}$$

where, ψ_y and ψ_z are the potential distributions in the y (horizontal) and z (vertical) directions, respectively, and ρ_y and ρ_z are the charge distributions in the y and z directions, respectively.

Due to the presence of the two back to back p-n junctions in the horizontal direction, there are two depletion regions in the channel and the full depletion of charge is approximated. Therefore, the charge distribution in the horizontal direction can be given by

$$\rho_y = \begin{cases} -\dfrac{qN_d}{\varepsilon_{Si}} & -\dfrac{W}{2} \le y < -\dfrac{W}{2} + y_n \\ 0 & -\dfrac{W}{2} + y_n \le y \le \dfrac{W}{2} - y_n \\ -\dfrac{qN_d}{\varepsilon_{Si}} & \dfrac{W}{2} - y_n < y \le \dfrac{W}{2} \end{cases} \tag{5.3}$$

where, y_n is the depletion width and N_d is the channel doping concentration. The boundary conditions are

$$\psi_y\left(-\frac{W}{2}+y_n\right)=0$$

$$\psi_y\left(\frac{W}{2}-y_n\right)=0$$

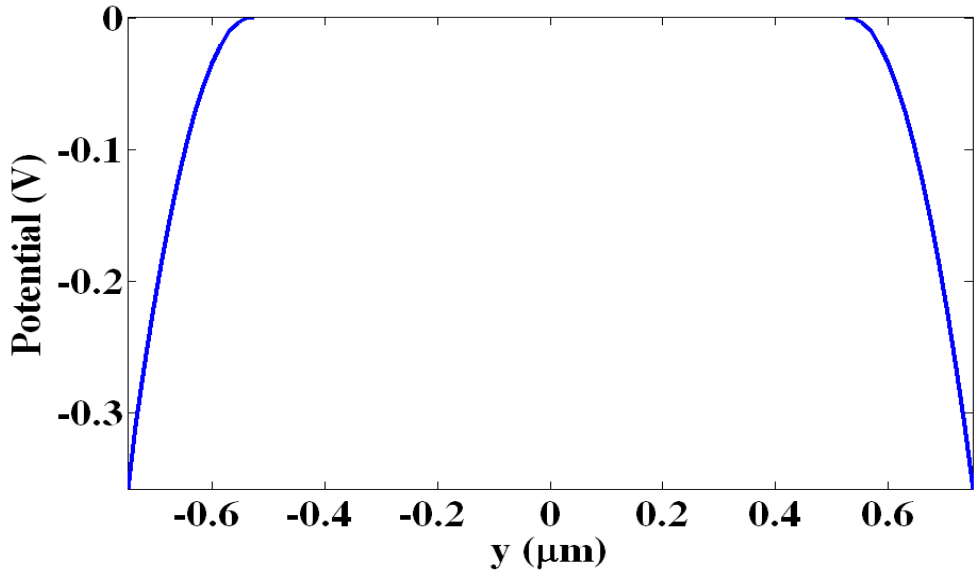
$$\left.\frac{d\psi_y}{dy}\right|_{y=-\frac{W}{2}+y_n}=0$$

$$\left.\frac{d\psi_y}{dy}\right|_{y=\frac{W}{2}-y_n}=0 \quad . \tag{5.4}$$

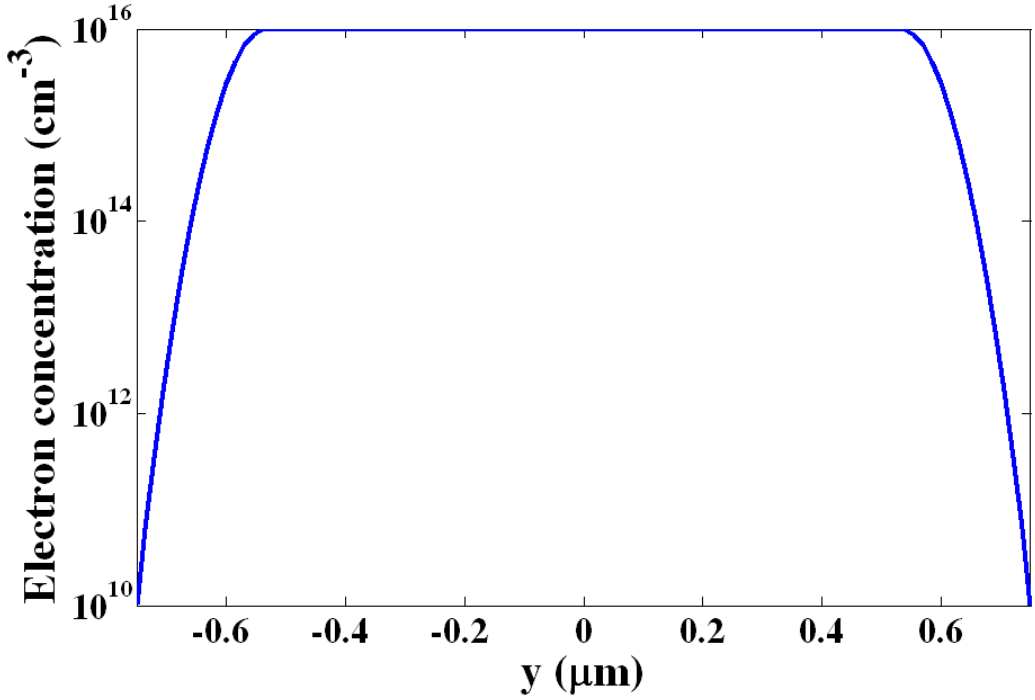
The potential distribution in the horizontal direction can be found by inserting Equation 5.3 in Equation 5.1 and applying the boundary conditions of Equation 5.4. The potential distribution in the horizontal direction is depicted by

$$\psi_y=\begin{cases}\dfrac{q}{\varepsilon_{Si}}N_a\dfrac{\left(y+\frac{W}{2}\right)^2}{2}+\dfrac{q}{\varepsilon_{Si}}N_d y_n\left(y+\frac{W}{2}\right)-\dfrac{q}{\varepsilon_{Si}}N_d\dfrac{y_n^2}{2} & -\dfrac{W}{2}\le y<-\dfrac{W}{2}+y_n\\ 0 & -\dfrac{W}{2}+y_n\le y\le\dfrac{W}{2}-y_n\\ \dfrac{q}{\varepsilon_{Si}}N_a\dfrac{\left(y-\frac{W}{2}\right)^2}{2}+\dfrac{q}{\varepsilon_{Si}}N_d y_n\left(y-\frac{W}{2}\right)-\dfrac{q}{\varepsilon_{Si}}N_d\dfrac{y_n^2}{2} & \dfrac{W}{2}-y_n<y\le\dfrac{W}{2}\end{cases} \tag{5.5}$$

Figure 5.2 shows the potential distribution in the horizontal direction. It shows that the depletion region due to p-n junction extend in to the channel (Figure 5.2 (a)). The depletion region is void of mobile majority carrier. Therefore, the carrier concentration is reduced in these regions (Figure 5.2. (b)) and the current density is reduced accordingly.



(a)



(b)

Figure 5.2: (a) Potential distribution; (b) Electron distribution, due to the presence of p-n junctions in the horizontal direction.

Due to the presence of the oxide gate, the conduction of the semiconductor bends near the interface. The exact solution of band bend is difficult to solve, but not impossible. Therefore, a piecewise linear function is assumed for the band bending, as shown in Figure 5.3. The piecewise linear approximation is not as accurate as the exact solution. However, it provides a first order approximation of the potential distribution in the vertical direction.

The potential distribution follows the same function as the conduction band, but with the opposite sign. The piecewise linear potential distribution is given by

$$\psi_z(z) = az + b \tag{5.6}$$

where, ***a*** and ***b*** are two constants to be determined. The constants, ***a*** and ***b***, can be determined by applying the appropriate boundary condition, which is given by

$$\psi_z(0) = 0$$

$$\varepsilon_{ox}\frac{V_{TS} - V_{FBT} - \Phi_{MST} - \psi_z\left(\frac{H}{2}\right)}{t_{oxT}} = \varepsilon_{Si}\left.\frac{d\psi_z}{dz}\right|_{z=\frac{H}{2}}$$

$$\varepsilon_{ox}\frac{V_{BS} - V_{FBB} - \Phi_{MSB} - \psi_z\left(-\frac{H}{2}\right)}{t_{oxB}} = -\varepsilon_{Si}\left.\frac{d\psi_z}{dz}\right|_{z=-\frac{H}{2}} . \tag{5.7}$$

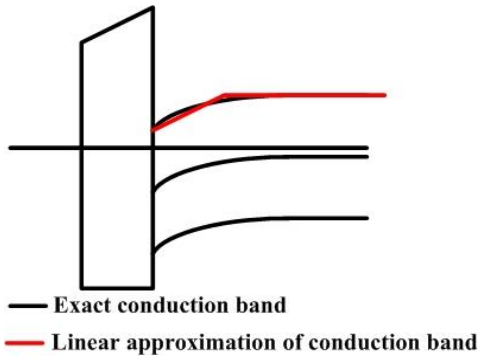


Figure 5.3: Linear approximation of conduction band.

After applying boundary conditions of Equation 5.7 into Equation 5.6, a and b can be expressed as

$$b = 0$$

$$a = \frac{\varepsilon_{ox}}{\left(-\varepsilon_{ox} - \frac{H\varepsilon_{ox}}{2t_{oxB}}\right)t_{oxB}}\left(V_{BS} - \Phi_{MSB}\right), -\frac{H}{2} \le z < 0$$

$$a = \frac{\varepsilon_{ox}}{\left(\varepsilon_{ox} + \frac{H\varepsilon_{ox}}{2t_{oxT}}\right)t_{oxT}}\left(V_{TS} - \Phi_{MST}\right), 0 \le z < \frac{H}{2} \tag{5.8}$$

Since, the current flow is predominantly from the source to the drain along the x-axis, the electric field, due to drain potential, is also in the x-direction. Let us assume the potential at the center of the channel to be V. Therefore, the potential distribution can be given by

$$\psi(y,z) = \psi_y + \psi_y + V \tag{5.9}$$

After obtaining the potential distribution, the charge distribution can be written as

$$n(y,z) = N_d \exp\left(\frac{q(\psi(y,z) - V)}{KT}\right) = N_d \exp\left(\frac{q(\psi_y + \psi_z)}{KT}\right) \tag{5.10}$$

The potential distribution under depletion bias at all four gates is shown in Figure 5.4. This figure shows the existence of depletion regions in the horizontal direction due to the presence of p-n junctions. It also shows the potential distribution in the vertical direction as approximated with piecewise linear function. Figure 5.5 shows the charge distributions in the channel area under same bias condition as in Figure 5.4. As all four gates are in depletion mode the carriers are depleted from all four gates. It is shown in Figure 5.5, as depletion regions end near the center of the channel, the carrier

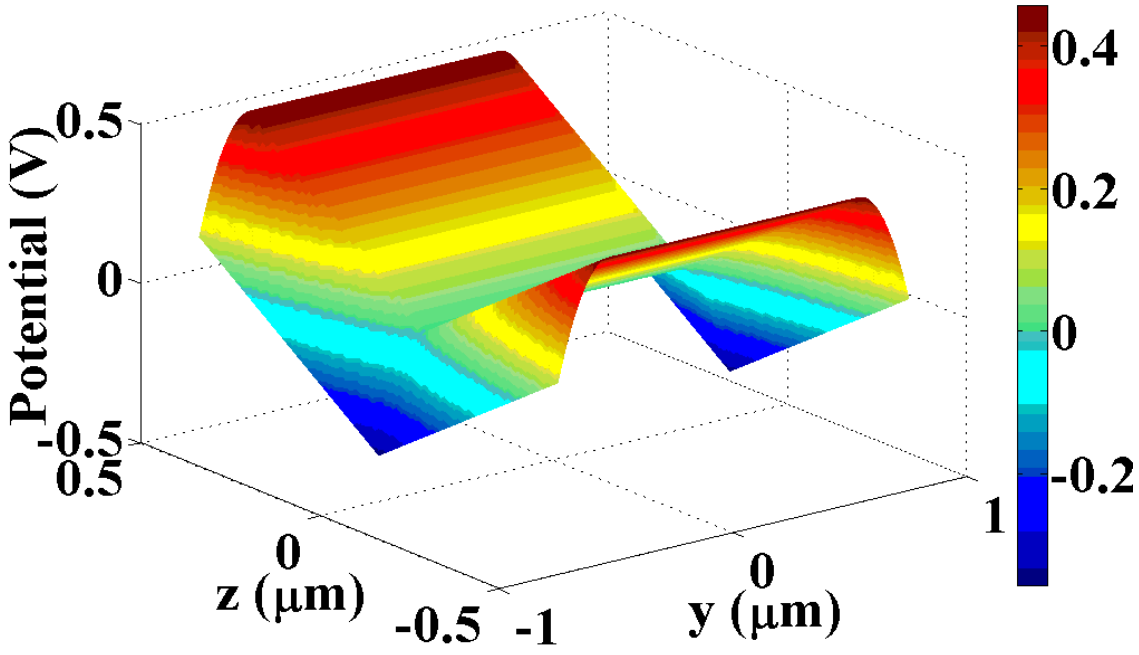


Figure 5.4: 2-dimensional potential distribution.

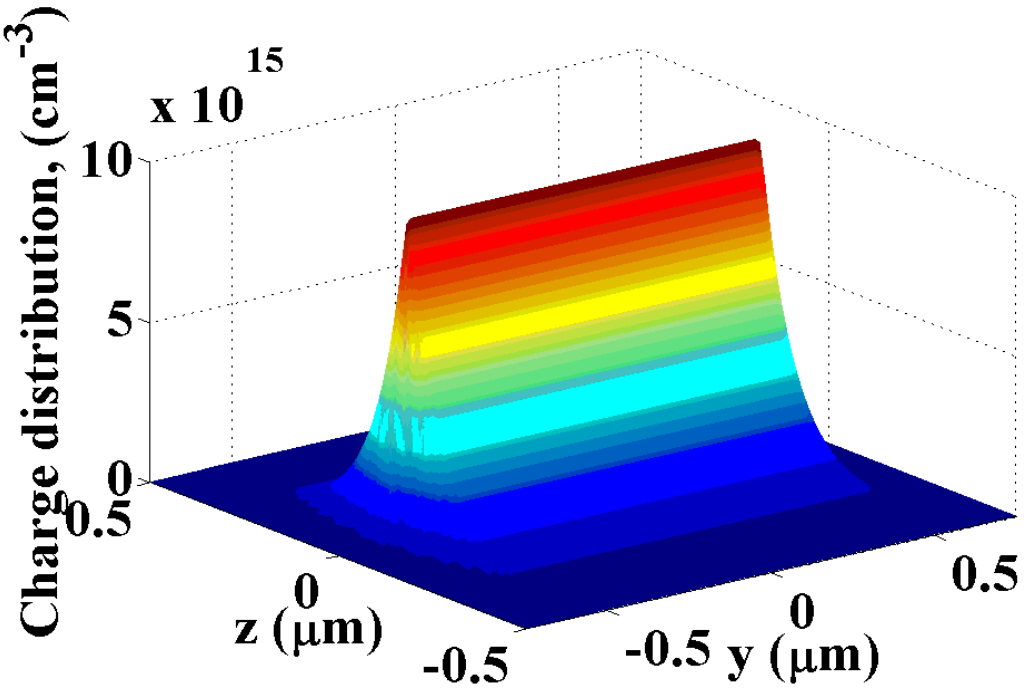


Figure 5.5: Charge distribution in the channel with all four gates biased at depletion.

concentration remains the same as the channel doping. Therefore, the conduction area exists only near the center of the channel, forming a quantum wire.

5.3 Expression for drain current

For the field effect transistor, the channel current is comprised of the drift component. Channel current density is given by

$$J = q\mu n(x)\frac{dV}{dx} \quad . \tag{5.11}$$

The total current can be obtained by integrating current density over the whole cross sectional area.

$$I_{DS} = q\mu n(x)WH\frac{dV}{dx} \tag{5.12}$$

Equation 5.12 states that if the charge distribution is known, then the drain current can be determined. From the previous discussion, the charge distribution can be given by Equation 5.10.

A unique approach is followed to determine the channel current. First, we get an expression of current over a small distance and small potential difference.

$$\begin{cases} \int_{x_1}^{x_2} I_{DS}\,dx = q\mu WH \int_{V_1}^{V_2} n(x)\,dV \\ I_{DS}(x_2 - x_1) = q\mu WH \dfrac{(n(x_1) + n(x_2))}{2}(V_2 - V_1) \end{cases} \tag{5.13}$$

If both sides of Equation 5.13 is divided by I_{DS}, Equation 5.13 becomes

$$(x_2 - x_1) = q\mu WH \frac{(n(x_1) + n(x_2))(V_2 - V_1)}{I} \quad . \tag{5.14}$$

If the right side is observed carefully, voltage difference is divided by a current that corresponds to a resistor. If an equivalent resistor is introduced we have

$$(x_2 - x_1) = q\mu WH \frac{(n(x_1) + n(x_2))}{2} R_{eq} \tag{5.15}$$

Rearranging the different terms, we get an expression for equivalent length that corresponds to R_{eq}, as shown in Equation 5.16

$$x_2 = x_1 + q\mu WH \frac{(n(x_1) + n(x_2))}{2} R_{eq} \quad . \tag{5.16}$$

In order to determine the actual resistance, R_{eq} is normalized to actual device length, L, shown as

$$R = \frac{R_{eq}}{X} L \tag{5.17}$$

Therefore, current is given by

$$I_{DS} = \frac{V_{DS}}{R} \tag{5.18}$$

Figure 5.6 shows the comparison between the results obtained from device simulator and the results from the model. These figures show that model is in good agreement with the numerical simulator. These figures show that the model matches better with the simulated results for low values of top gate and back gate potentials. it deviation increases with the potentials at the top and the back gates. The increase of deviation is contributed by the linear approximation of potential distribution at **Si**/**SiO$_2$** interfaces. This deviation can be reduced by higher order of approximation of potential distribution at **Si**/**SiO$_2$** interfaces.

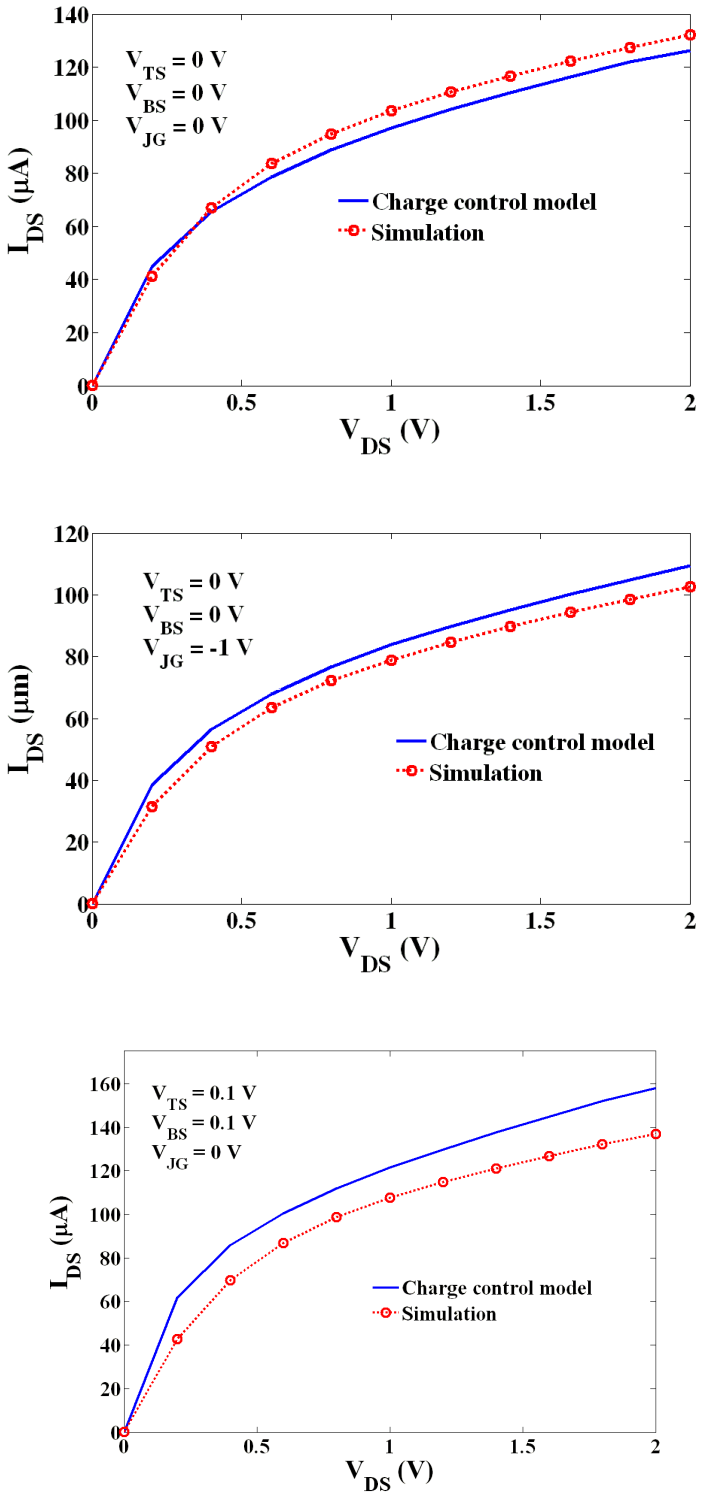


Figure 5.6: Comparison between the simulation results and the model results.

5.4 Chapter summary

The charge control method is a simple alternative to the carrier transport model. It provides a closed form of expression for the characteristics of a G^4FET. This model excludes the procedure of solving complex expression as for the carrier transport model. Instead, a few assumptions are made to simplify the computational complexity. These assumptions include negligible diffusion current, independent potential distribution in the channel at different directions, piecewise linear potential distribution at **Si**/**SiO_2** interfaces. This model predicts the device characteristics very closely to the results obtained from a device simulator. The main source of deviation is the linear approximation of the potential at **Si**/**SiO_2** interfaces. The deviation can be reduced by higher order approximation of the potential distribution.

CHAPTER SIX

DC Modeling of G^{4}FET for Circuit Simulation

6.1 Motivation

All semiconductor devices are designed to be used as circuit elements. The independent actions of the four gates open new perspectives for mixed-signal applications, quantum wire effects, and quaternary logic schemes. The operation of the multiple gates has applications for single transistor multiple gate logic schemes. G^{4}FET demonstrates an excellent performance under a wide range of operating voltages [12]. The experimental results demonstrate the complex variations of the threshold voltage, subthreshold swing, and breakdown voltage due to the multiple gate control employed with the G^{4}FET. The breakdown voltage of 15 V was measured for a 3.3 V PDSOI device with an excellent subthreshold swing and high carrier mobility.

6.2 Circuit model

Integrated circuits, unlike the board-level designs composed of discrete components, are impossible to breadboard prior to manufacturing. Further, the high costs of photolithographic masks and other manufacturing prerequisites make it essential to design the circuit as perfectly as possible before the integrated circuit is first manufactured. Simulating the circuit with a circuit simulator is the industry-adopted, standard method to verify the

circuit operation at the transistor level before committing to the manufacturing of an integrated circuit.

Board-level circuit designs can often be breadboarded for testing. Even with a breadboard, some circuit properties may not be accurate when compared to the final printed circuit board (PCB), such as the parasitic resistances and capacitances. These parasitic components can often be estimated more accurately using a circuit simulator.

6.3 Compact expression

Thousands of transistors exist in an integrated circuit. If we use physics based expressions, which require solving a number of coupled nonlinear partial differential equations for each transistor, it would be a hard, if not impossible, task to complete. The task would be time consuming and a solution is not guaranteed. However, if there is a closed form of expression for the transistor, then the solution will be easy. For any industry, time is money and a fast and accurate solution is needed. Thus, a compact model is an essential requirement.

A circuit model is a compact mathematical expression for the behavior of a device. It can predict the values of a certain parameter as a function of other parameters.

6.4 Numerical device modeling

Analytical models are important to understanding the physical operation of the semiconductor devices and optimizing their structures for specific applications. A number of physical phenomena, such as high-field mobility, carrier velocity saturation, recombination-generation, charge trapping, and hot carrier effect dictate the semiconductor device

characteristics. The physical phenomena are highly nonlinear in nature, and working with these complex functions is not an easy task. A closed form of analytical expression, even in piecewise form, becomes almost impossible without a number of approximations. Moreover, computation with complex expressions is also a time consuming task. In addition, these models are not fast enough to be utilized in most circuit simulators.

Numerical models offer an alternative to physics-based analytical models for rapid and accurate device modeling. Although this approach does not provide any physical insight, these models serve as excellent tools for quick circuit simulation [42-50]. In general, this approach uses measured data to reproduce the complex nonlinear behavior of semiconductor devices. In most cases they are equally applicable to different types of transistors (MOSFET, MESFET, HEMT, etc.) fabricated using various technologies. A large number of works on numerical device modeling have been reported since the 1970's [42]. The most commonly used methods involve the application of a look-up table and quadratic and higher order polynomials. Authors in [49] proposed a numerical MOSFET model based on a multidimensional Bernstein interpolation as a means to improve the simulation efficiency. Hermite polynomials, based on a simple bicubic surface patch generation, was presented in [50] for the evaluation of the device operating point, but this interpolation function may exhibit bumps, even though the original set of data might be monotonic and concave/convex in either direction. In [51], the triode region was modeled by quadratic fits whereas linear fits were used for the saturation region. Discontinuities in the conductance arise as the operating point shifts from the triode region to the saturation region, and vice versa. To reduce the discontinuity, additional data points are needed, but these can cause an increase in the

experimental cost. Basic, cubic spline-based multi-dimensional interpolation techniques are presented in [46]. The spline parameters are optimized for a monotonicity preserved interpolation.

The look-up table method is simple to implement [43-45]. However, it requires a high density of data points and consumes a significant portion of computational time in the search process. It also depends on a local approximation rather than a global approximation. This forces the look-up model to be restricted to within a limited range of device operation. Another area of a numerical approach uses quadratic or higher order polynomials for interpolation [46-48]. These methods determine the coefficients of a predetermined polynomial from the available data, but the use of predetermined polynomials cause these interpolation methods to suffer from large truncation errors. For some special polynomials, such as Bernstein [49] and Hermite [50], the interpolation method involves the determination of factorials and derivatives. Those models tend to slow down significantly where large numbers of polynomial terms are used for interpolation.

The numerical modeling approach is inherently faster than the analytical model by reducing the computational effort to evaluate the device equations. Technology changes in the device fabrication (material and structure) can be more easily absorbed into numerical modeling simply by computing a new set of parameters from the experimental data. This is much faster than developing an analytical model from a physical understanding of all device properties. Another important feature of numerical modeling is its ease of incorporation into a circuit simulator. Table methods require a large memory allocation to accommodate the

tabular values for different parameters. On the other hand, polynomial methods utilize functional forms, but most are unable to incorporate the different device parameters.

A Lagrange polynomial was used to derive the numerical model from the available data set. A Lagrange polynomial is the highest degree of polynomial for any given set of data. As a result, it can incorporate the effects of different phenomena for the maximum possible combinations. For this reason, a Lagrange polynomial was chosen for the development of this model. In addition, the developed model uses only one expression to predict the device characteristics over the entire region of device biasing, and for all regions of operation. This means, via this method, only one equation is needed for transistor characteristics, for all gate biasing voltages, and for both the triode and saturation region operations. The integration of the developed model with a circuit simulator is also discussed.

Developing an expression to model a set of data involves fitting a polynomial to a set of data points such as (x_0, y_0), (x_1, y_1)… (x_m, y_m). These points are available from either experiments or simulation. If additional sets of data are required, the entire experiment or simulation needs to be repeated. This is an expensive process to obtain data. In order to solve this problem, traditionally an algebraic polynomial $f(x)$ is constructed, such that

$$y_i = f(x_i), \quad i = 0,1,\ldots,m \tag{6.1}$$

where, $f(x)$ is called the interpolation polynomial and the points, x_i, $i = 0, 1, \ldots, m$, are called the interpolation points.

The Taylor series expansion is a way of approximating general functions by polynomials, but this has limited usefulness. Interpolation is a more practical way of constructing polynomial approximations. Interpolating polynomials can be completed in

multiple ways. The method of evaluation of the undetermined coefficients is simple and intuitive, and gives results with a minimum of effort [52]. However, this method is not always suitable, especially since the system tends to become ill-conditioned quickly as m increases. This also does not give a very explicit form of the polynomial and makes it difficult to use for analysis. The Lagrange polynomial, investigated by the mathematician Joseph-Louis Lagrange (1736-1813), overcomes some of the limitations.

The Lagrange interpolating polynomial, denoted by $P(x)$, is the unique polynomial of degree m for which $P(x_i) = f(x_i)$ for $i = 0, 1, \ldots, m$. This can be expressed as [53]

$$P(x) = \sum_i L_i(x) f(x_i) \tag{6.2}$$

where $(x_0, x_1, \ldots, x_m)$ are the interpolating or node points, and the Lagrange coefficient, $L_i(x)$ is given by

$$L_i(x) = \frac{(x - x_0)(x - x_1)\ldots(x - x_{i-1})(x - x_{i+1})\ldots(x - x_m)}{(x_i - x_0)(x_i - x_1)\ldots(x_i - x_{i-1})(x_i - x_{i+1})\ldots(x_i - x_m)} = \prod_{j=0, j\neq i}^{m} \frac{(x - x_j)}{(x_i - x_j)} \quad . \tag{6.3}$$

The coefficients have several properties that deserve attention [54]. Lagrange coefficients formed for the $m + 1$ points $(x_0, y_0), (x_1, y_1) \ldots (x_m, y_m)$ is a polynomial of degree m which vanishes at $x = x_0 \ldots x = x_i - 1, x = x_i + 1 \ldots x = x_m$, but at $x = x_i$ it assumes the value of 1 *(one)*. As a result, the error is zero if the interpolating point coincides with the data point. The form of the Lagrange coefficient, as given in Equation 6.3, shows that it depends only on the given x's and is entirely independent of the y's. The Lagrange polynomial is invariant if the variable x is replaced by a new variable through the linear transformation. Direct use of the coordinates, and discounting the difference tables and factorial polynomial, makes the calculation of the Lagrange polynomial less expensive.

The Lagrange polynomial can be extended for two independent variables as follows

$$P(x,y)=\sum_i L_i(x)\left(\sum_j L_j(y)\,f(x_i,y_j)\right) \tag{6.4}$$

where, $L_i(x)$ and $L_j(y)$ are expressed as in Equation 6.3. The equation shows that the Lagrange polynomial can be written in a recursive fashion. For more than two variables, the Lagrange polynomial can be expanded in the same manner as in Equation 6.4. For example, the recursive formulation for three independent variables can be written as

$$P(x,y,z)=\sum_i L_i(x)\left(\sum_j L_j(y)\left(\sum_k L_k(z)\,f(x_i,y_j,z_k)\right)\right) \tag{6.5}$$

.

As stated earlier, the Lagrange polynomial is invariant to the change of variables. If the variables (u, v, w and x) in Equation 6.5 are replaced with V_{DS} (drain-to-source voltage), V_{TS} (top gate-to-source voltage), V_{BS} (back gate-to-source voltage), and V_{JS} (junction gate-to-source voltage), the expression for the drain current can be expressed in the form of Lagrange polynomials. The drain current, in terms of Lagrange polynomial is expressed as follows

$$I_{DS}(V_{DS},V_{TS},V_{BS},V_{JS}) = \sum_i L_i(V_{DS})\left(\sum_j L_j(V_{TS})\left(\sum_k L_k(V_{BS})\sum_l L_l(V_{JS})\,f(V_{DS},V_{TS},V_{BS},V_{JS})\right)\right) \tag{6.6}$$

The modeling effort starts with a set of available data from either an experiment or a simulation. The Lagrange polynomials for different parameters are evaluated from Equation 6.3, and then these polynomials are inserted into the Equation 6.6.

6.5 G^4FET model development and verification using available Data

The numerical model of the G^4FET model is developed from both experimental and simulated data. The procedure for evaluating the model equation is the same as the procedure described in section 6.4.

6.5.1 Test result: Device 1

A device is fabricated with a commercial process. Its parameters are shown in Table 6.1. Then the expression for drain current is determined from the test results. Figure 6.1 shows the comparison of results from experiment and the model. The potentials at the back gate and the junction gates are held constant at 0V. The potential at top gate is varied from -1V to 2V with step of 1V. This figure shows that the 2^{nd} order model fits the experimental data with maximum error of 22% for lowest top gate potential. The error is reduced with the increase of bias potential and the error is 6% at 2V of top gate potential. Figure 6.2 shows the comparison of results from experiment and the model for the same bias condition as for Figure 6.1. However, the model is developed with 4^{th} order approximation. The maximum error for 4^{th} order approximation is for lowest top gate potential is 1.4%. The error is reduced with the increase of bias potential and the error is 0.4% at 2V of top gate potential. It is noticeable from Figure 6.1 and Figure 6.2 that the error is reduced drastically, for each top gate potential, with higher order of approximation.

Figure 6.3 shows the comparison of results from the experiment and the model. The potentials at the back gate and the junction gates are held constant at -20V and 0V

respectively. The potential at top gate is varied from -1V to 2V with step of 1V. This figure shows that the 2^{nd} order model fits the experimental data with maximum error of 80% for lowest top gate potential. The error is reduced with the increase of bias potential and it is 10% at 1V of top gate potential. Figure 6.4 shows the comparison of the results from the experiment and the model for the same bias condition as for Figure 6.3. However, the model is developed with 4^{th} order approximation. The maximum error for 4^{th} order approximation is for lowest top gate potential is 55%. The error is reduced with the increase of bias potential and it is 2% at 2V of top gate potential. It is noticeable from Figure 6.3 and Figure 6.4 that the error is reduced drastically, for each top gate potential, with higher order of approximation.

Figure 6.5 shows the comparison of results from the experiment and the model. The potentials at the top gate and the back gate are held constant at 0V and -3V, respectively. The potential at junction gates are varied from -1V to 0V with step of 1V. This figure shows that the 4^{th} order model fits the experimental data with maximum error of 20% for lowest junction gate potential. The error is reduced with the increase of bias potential and it is 1% at 0V of junction gate potential. Figure 6.6 shows the comparison of the results from the experiment and the model for the same bias condition as for Figure 6.5. However, the model is developed with 8^{th} order approximation. The maximum error for 4^{th} order approximation is for lowest junction gate potential is 5%. The error is reduced with the increase of bias potential and it is 2% at 0V of junction gate potential. It is noticeable from Figure 6.5 and Figure 6.6 that the error is reduced drastically, for each junction gate potential, with higher order of approximation.

6.5.2 Test result: Device 2

The results from the model are compared with the results from [10]. Figure 6.7 shows the comparison of the results from the experiment and the model. The potentials at the junction gates and the back gate are held constant at 0V. The potential at top gate is varied from 0V to 3V with step of 1V. This figure shows that the model fits the experimental data with maximum error of 11% for lowest top gate potential. The error is reduced with the increase of bias potential and the error is 3% at 3V of top gate potential.

Figure 6.8 shows the comparison of results from experiment and the model. The potentials at the top gate and the back gate are held constant at 0V. The potential at junction gates are varied from -2V to 0V with step of 1V. This figure shows that the model fits the experimental data with maximum error of 23% for the lowest junction gate potentials. The error is reduced with the increase of bias potential and it is 1% at 0V of junction gate potentials.

6.5.3 Test result: Device 3

The results from the model are compared with the results from [20]. Figure 6.9 shows the comparison of results from experiment and the model. The potentials at the top gate and the back gate are held constant at 0V. The potential at junction gates are varied from -1.5V to 0V with step of 1.5V. This figure shows that the model fits the experimental data with maximum and minimum error of 2% and 0.5%, respectively.

Figure 6.10 shows the comparison of results from experiment and the model. The potentials at the top gate and the junction gates are held constant at 0V. The potential at back

gate is varied from -3V to 0V with step of 3V. This figure shows that the model fits the experimental data with maximum and minimum error of 2% and 1%, respectively.

Figure 6.11 shows the comparison of the results from the experiment and the model. The potentials at the back gate and the junction gates are held constant at 0V. The potential at top gate is varied from -3V to 0V with step of 3V. This figure shows that the model fits the experimental data with maximum and minimum error of 3.5% and 1%, respectively.

Figure 6.12 shows the comparison of results from experiment and the model. The potentials at the back gate and the top gate are held constant at -3V and 0V respectively. The potential at junction gates are varied from -1.5V to 0V with step of 1.5V. This figure shows that the model fits the experimental data with maximum and minimum error of 6% and 1%, respectively.

Figure 6.13 shows the comparison of the results from the experiment and the model. The potentials at the back gate and the top gate are held constant at -3V and -3V respectively. The potential at junction gates are varied from -1.5V to 0V with step of 1.5V. This figure shows that the model fits the experimental data with maximum and minimum error of 7% and 1.75%, respectively.

Figure 6.14 shows the comparison of the results from the experiment and the model. The potentials at the junction gates and the top gate are held constant at 0V and -1.5V respectively. The potential at back gate is varied from -3V to 0V with step of 3V. This figure shows that the model fits the experimental data with maximum and minimum error of 6% and 1%, respectively.

Figure 6.15 shows the comparison of the results from the experiment and the model. The potentials at the junction gates and the back gate are held constant at -1.5V and -3V respectively. The potential at top gate is varied from -3V to 0V with step of 3V. This figure shows that the model fits the experimental data with maximum and minimum error of 7% and 1%, respectively.

6.5.4 Test result: Device 4

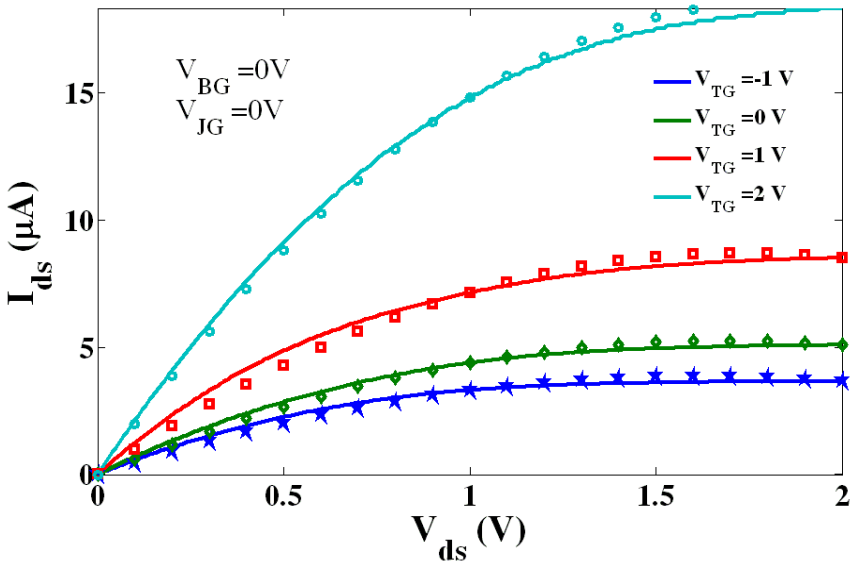
The results from the model are compared with the results from [17]. Figure 6.16 shows the comparison of the results from the experiment and the model. The potentials at the top gate and the junction gates are held constant at 1V and 0V respectively. The potential at back gate is varied from 0V to 10V with a step of 10V. This figure shows that the model fits the experimental data with maximum and minimum error of 14% and 2%, respectively.

Figure 6.17 shows the comparison of the results from the experiment and the model. The potentials at the back gate and the junction gates are held constant at 0V. The potential at top gate is varied from 0V to 1V with step of 1V. This figure shows that the model fits the experimental data with maximum and minimum error of 14% and 2%, respectively.

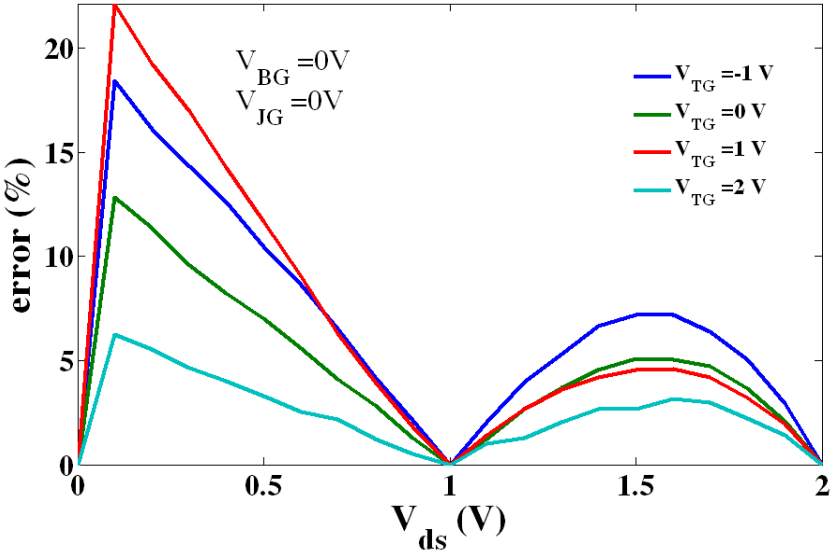
Figure 6.18 shows the comparison of the results from the experiment and the model. The potentials at the back gate and the top gate are held constant at 0V. The potential at junction gates is varied from -0.4V to 0V with step of 0.4V. This figure shows that the model fits the experimental data with maximum and minimum error of 15% and 5%, respectively.

Table 6.1: Device parameters of device # 1

Doping		Geometry		Operating potential	
Drain / Source	1e18 cm-3 Phosphorus	Top oxide thickness	0.01 μm	Drain-to-source	0, 1, 2, 3, 4, 5 V
Channel	1e16 cm-3 Phosphorus	Bottom oxide thickness	1 μm	Top gate	0, 1, 2, 3 V
Junction	1e18 cm-3 Boron	Channel length	1 μm	Bottom gate	0, 1, 2, 3 V
Top and bottom gate metal work function	3.5 eV	Channel width	0.35 μm	Junction gate	-3, -2, -1, 0 V

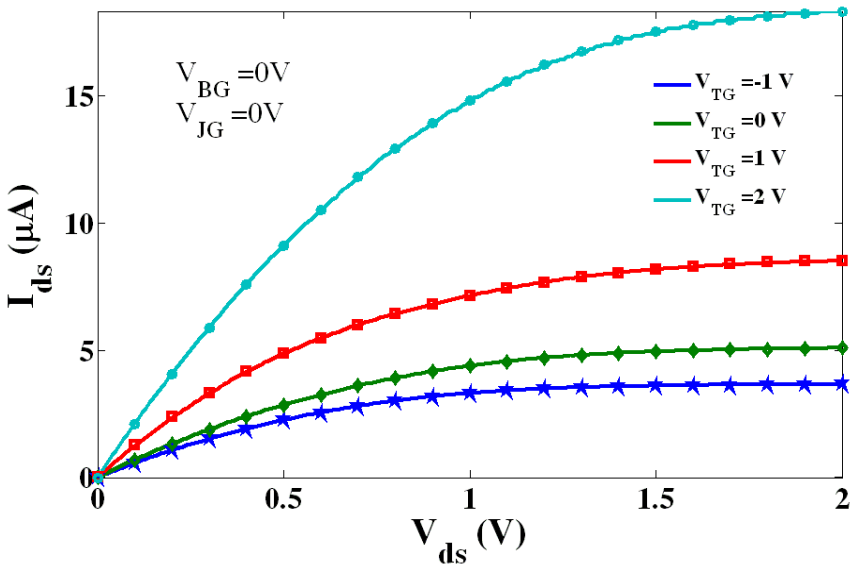


(a)

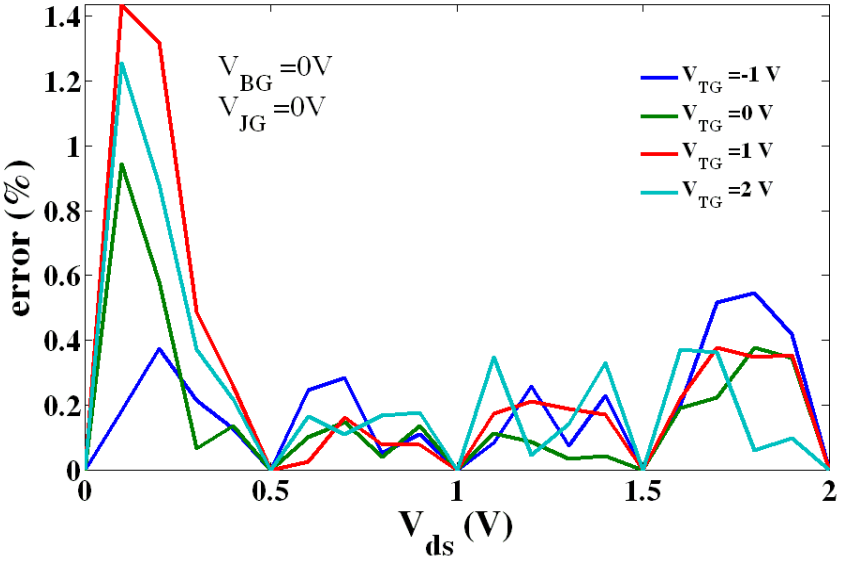


(b)

Figure 6.1: (a) Comparison between experimental results and numerical model of device # 1; (b) error between experimental results and numerical model f device # 1; with Lagrange polynomial of order 2.

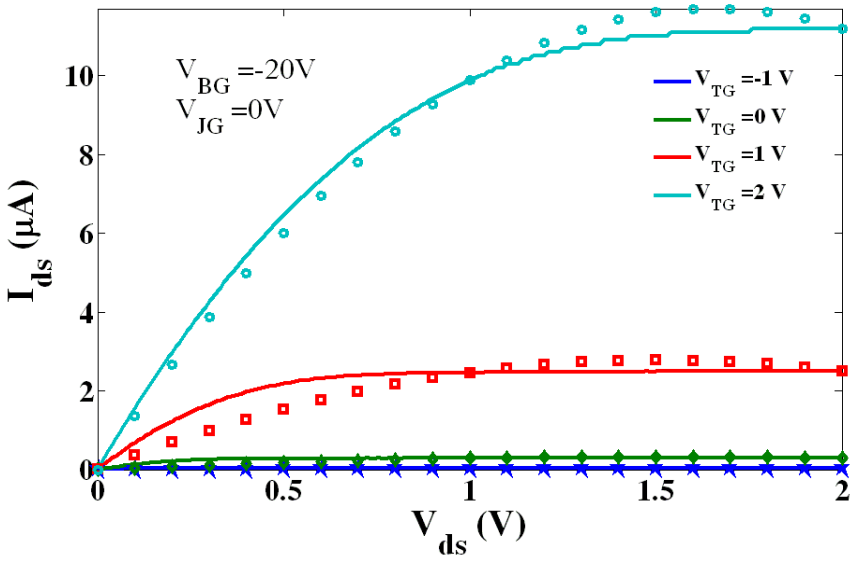


(a)

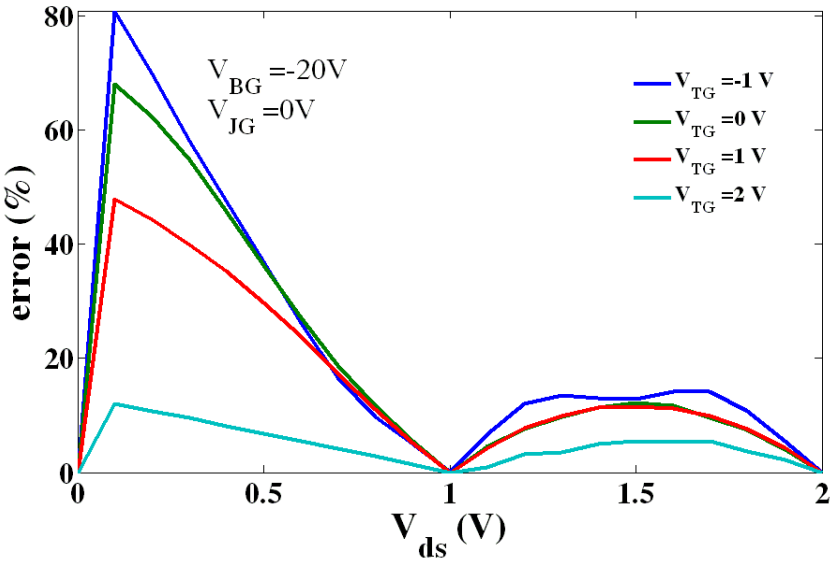


(b)

Figure 6.2: (a) Comparison between experimental results and numerical model of device # 1; (b) error between experimental results and numerical model f device # 1; with Lagrange polynomial of order 4.

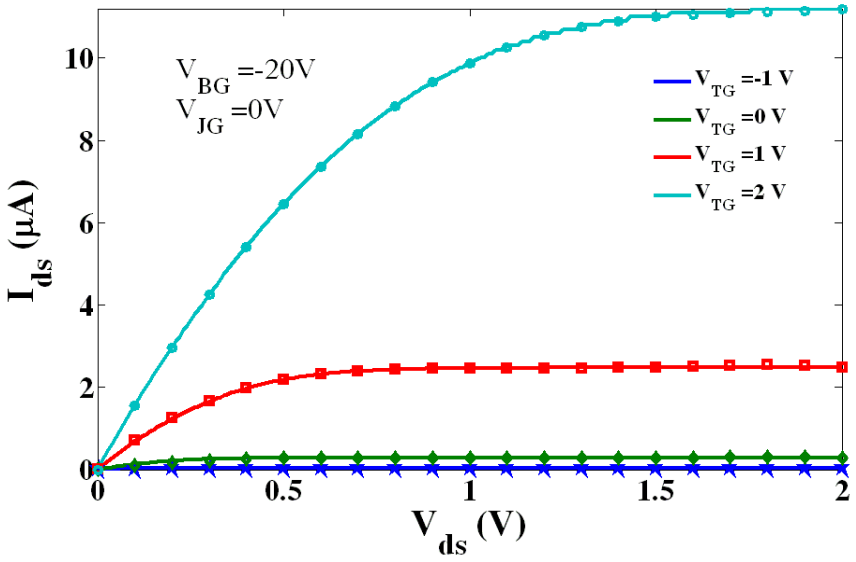


(a)

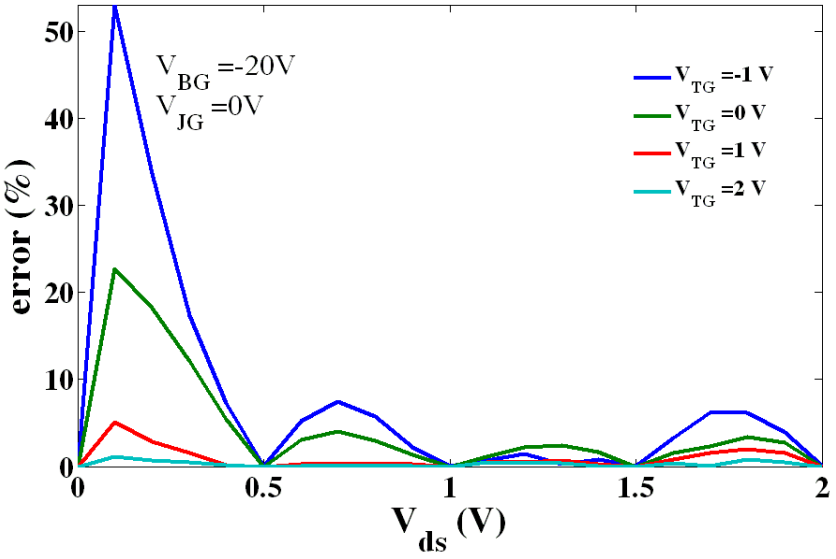


(b)

Figure 6.3: (a) Comparison between experimental results and numerical model of device # 1; (b) error between experimental results and numerical model f device # 1. ; with Lagrange polynomial of order 2.

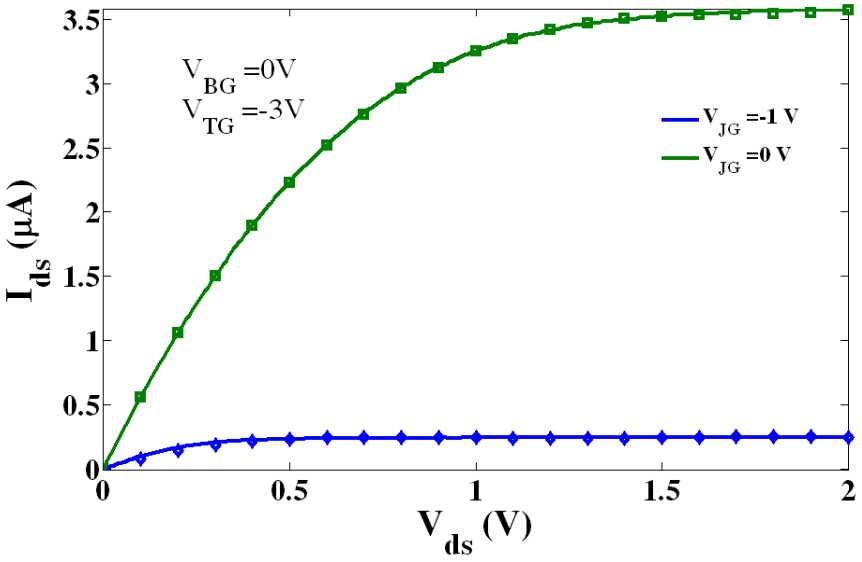


(a)

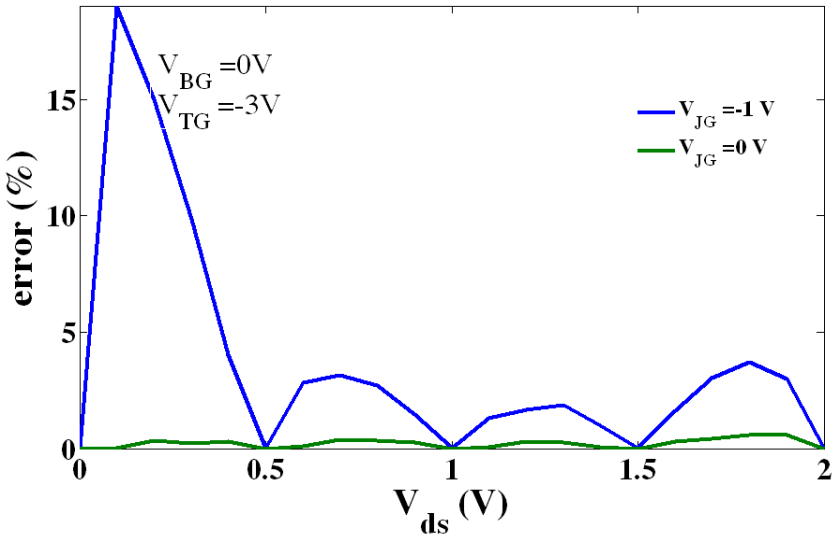


(b)

Figure 6.4: (a) Comparison between experimental results and numerical model of device # 1; (b) error between experimental results and numerical model f device # 1. ; with Lagrange polynomial of order 4.

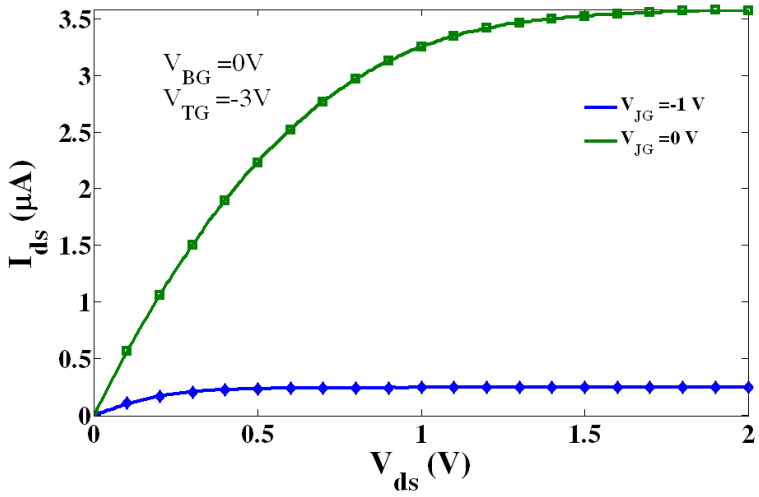


(a)

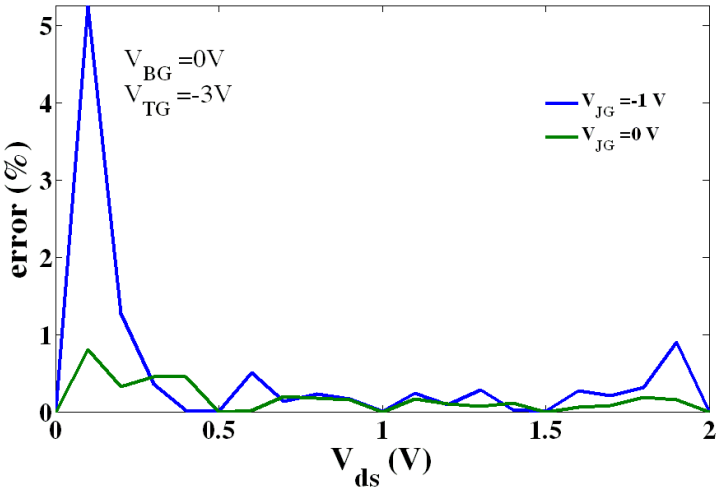


(b)

Figure 6.5: (a) Comparison between experimental results and numerical model of device # 1; (b) error between experimental results and numerical model f device # 1. ; with Lagrange polynomial of order 4.

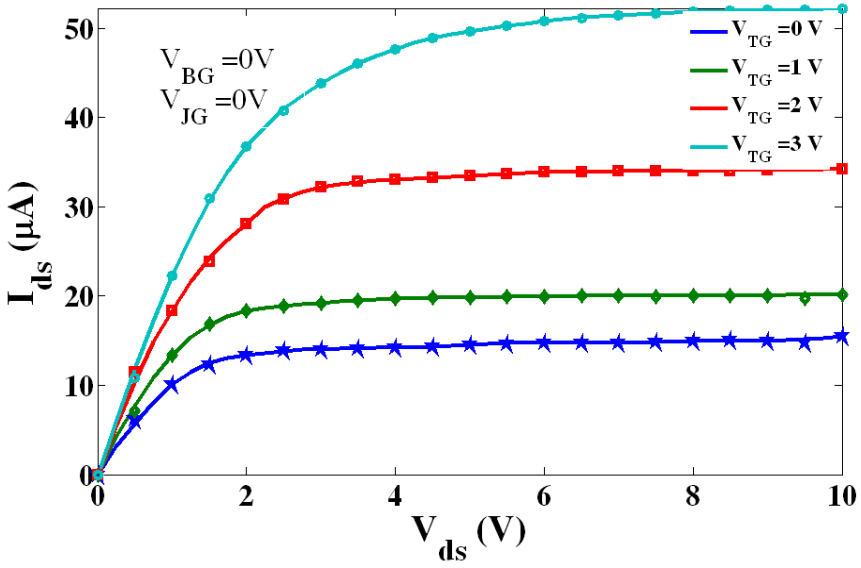


(a)

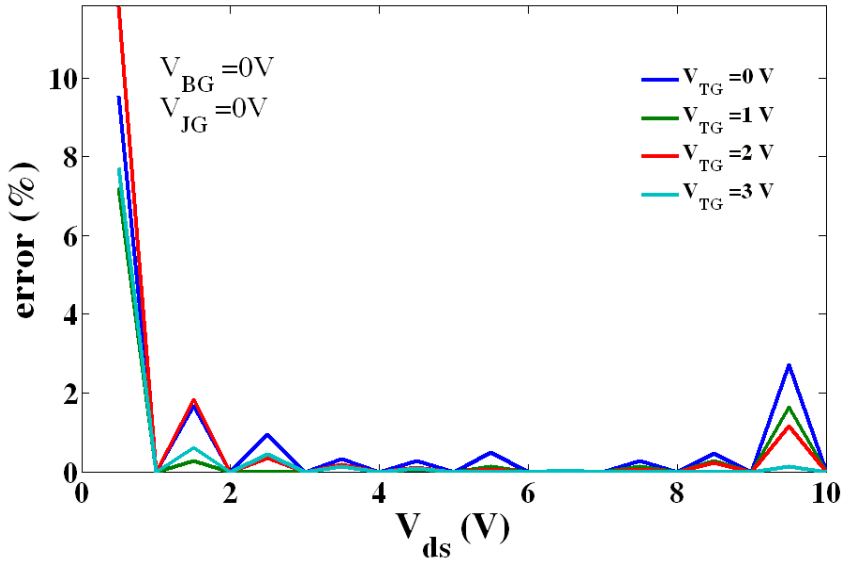


(b)

Figure 6.6: (a) Comparison between experimental results and numerical model of device # 1; (b) error between experimental results and numerical model f device # 1. ; with Lagrange polynomial of order 8.

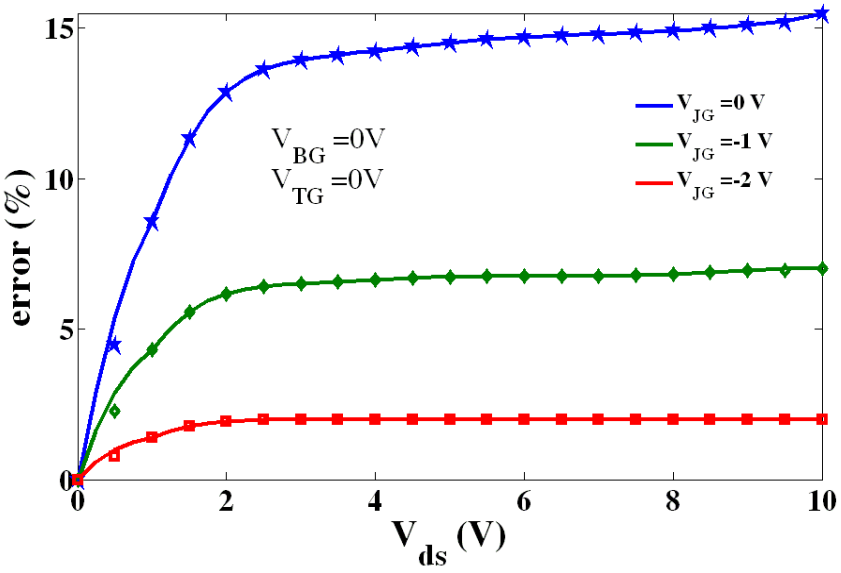


(a)

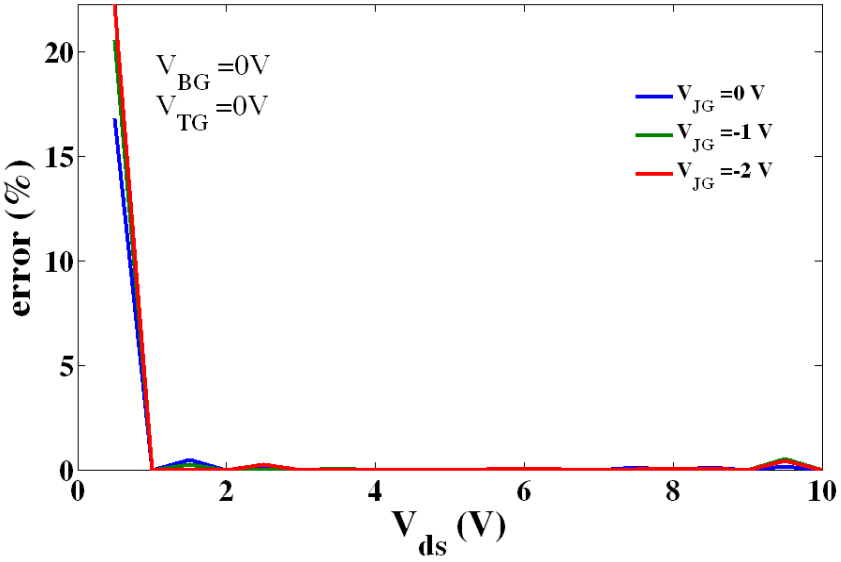


(b)

Figure 6.7: (a) Comparison between experimental results and numerical model of device # 2; (b) error between experimental results and numerical model of device # 2.

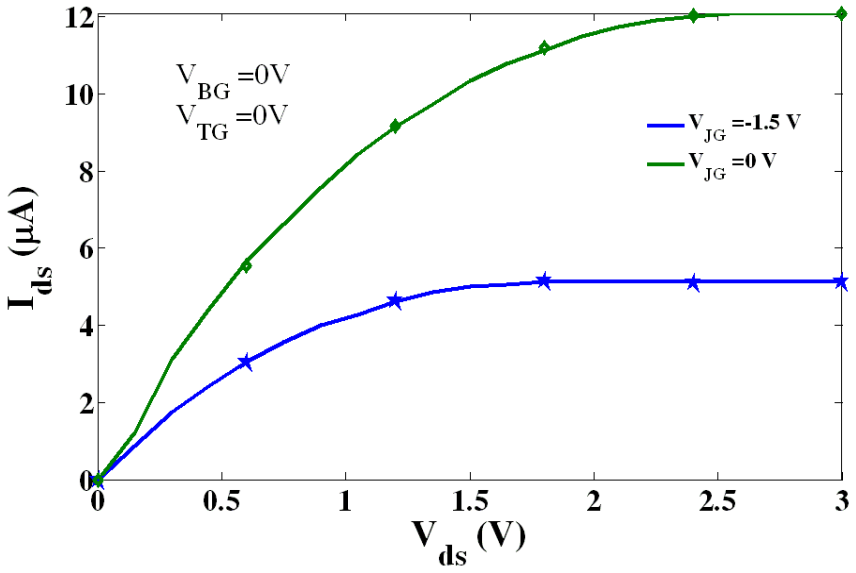


(a)

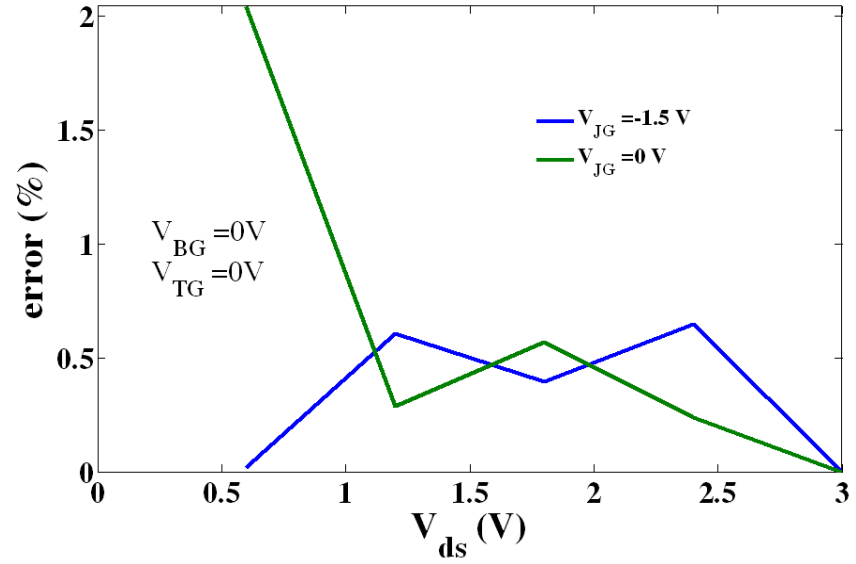


(b)

Figure 6.8: (a) Comparison between experimental results and numerical model of device # 2; (b) error between experimental results and numerical model of device # 2.

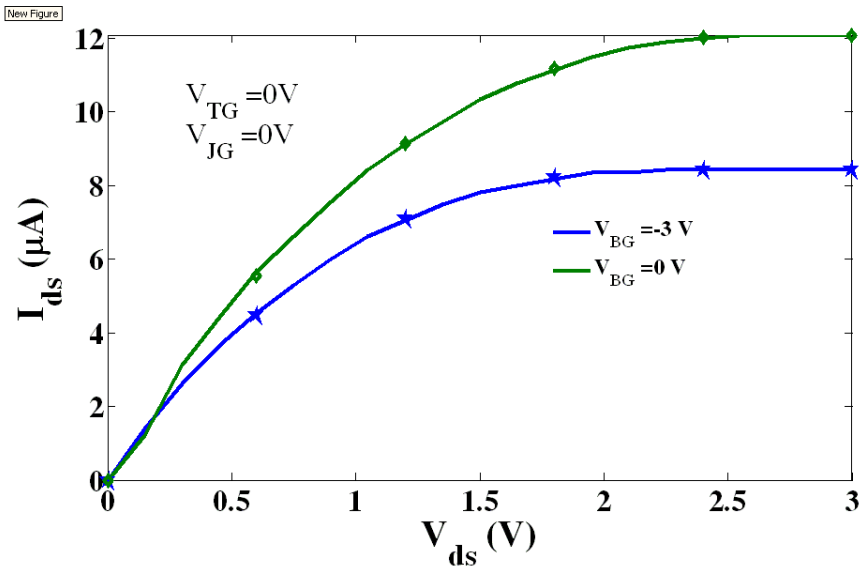


(a)

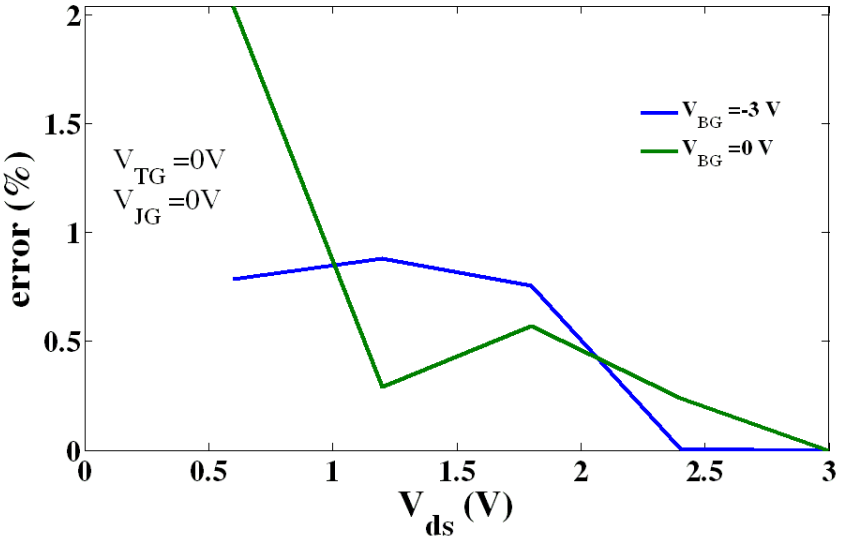


(b)

Figure 6.9: (a) Comparison between experimental results and numerical model of device # 3; (b) error between experimental results and numerical model of device # 3.

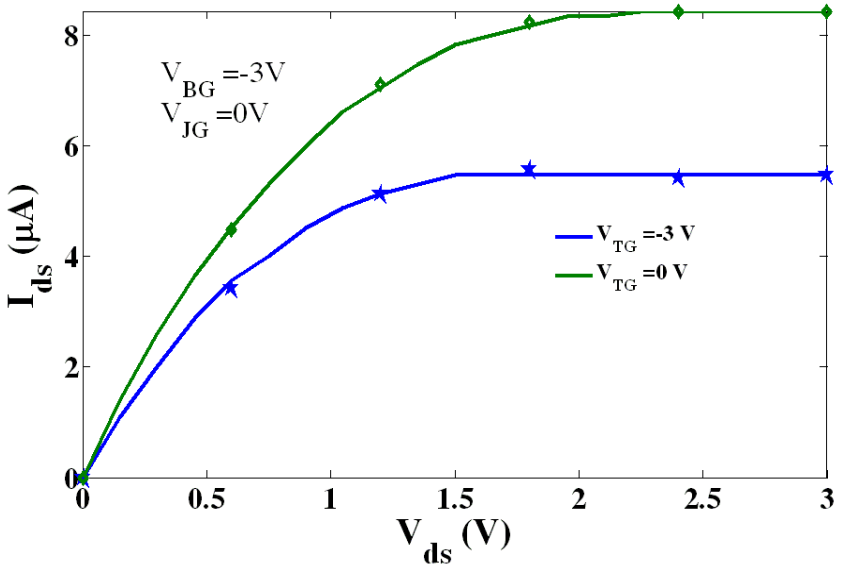


(a)

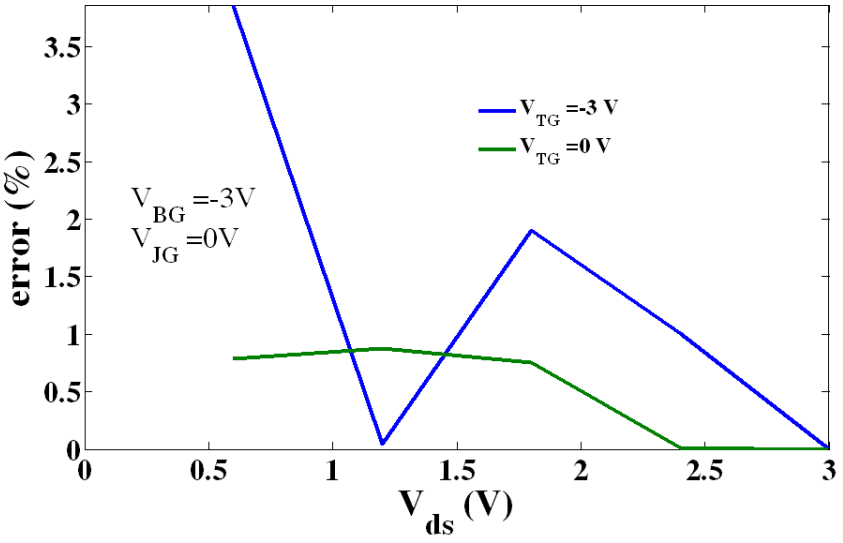


(b)

Figure 6.10: (a) Comparison between experimental results and numerical model of device # 3; (b) error between experimental results and numerical model of device # 3.

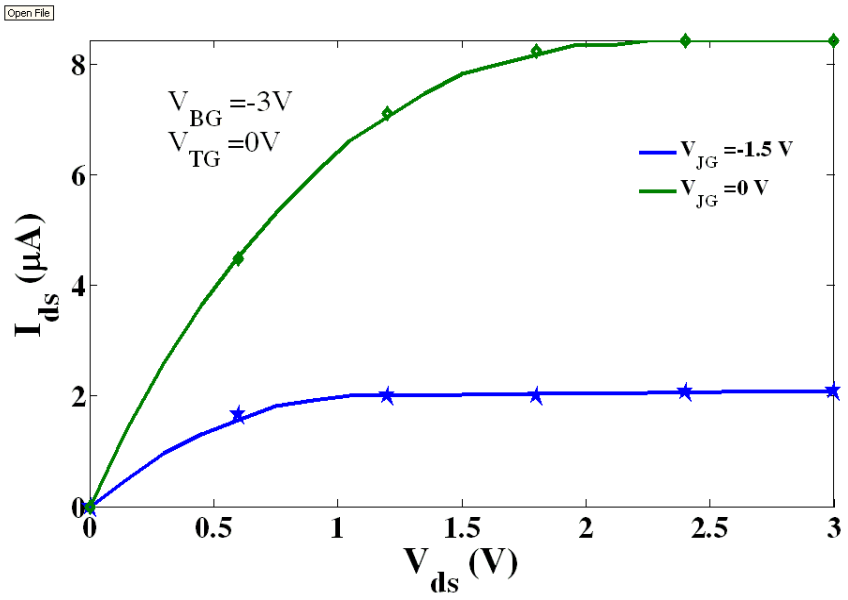


(a)

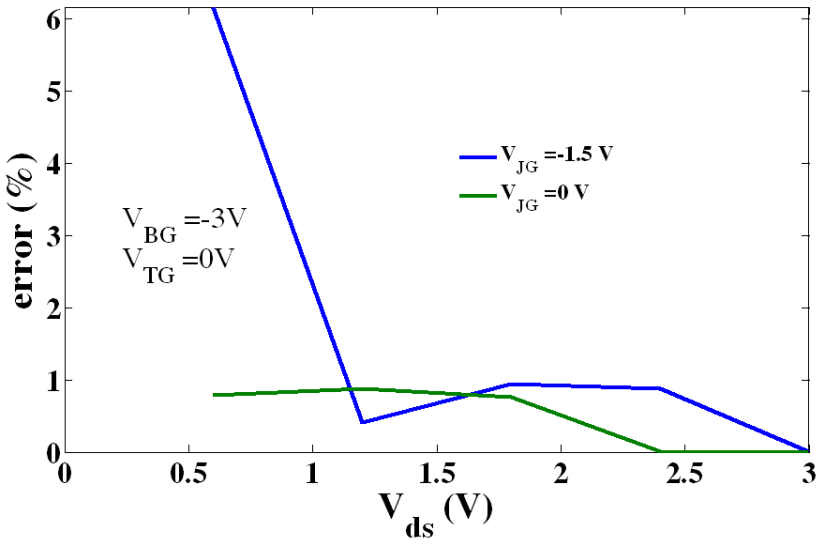


(b)

Figure 6.11: (a) Comparison between experimental results and numerical model of device # 3; (b) error between experimental results and numerical model of device # 3.

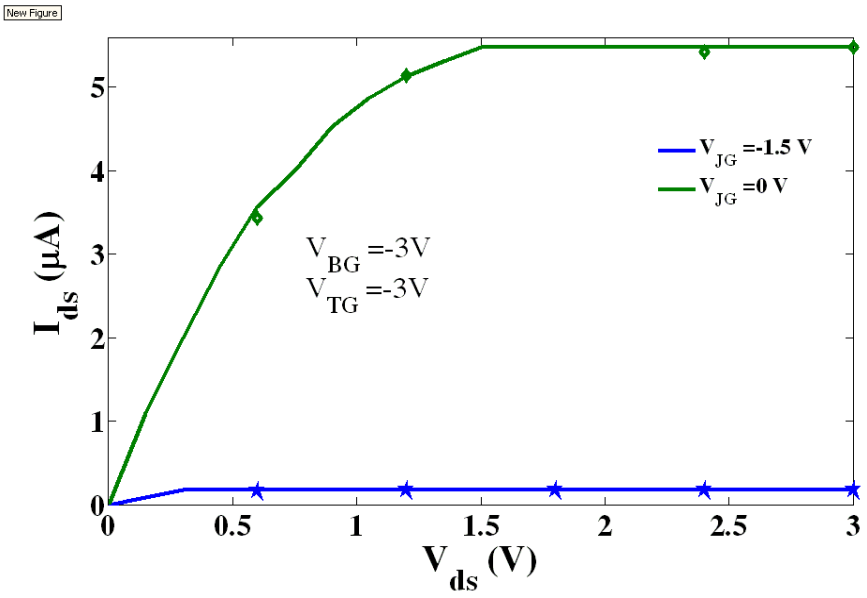


(a)

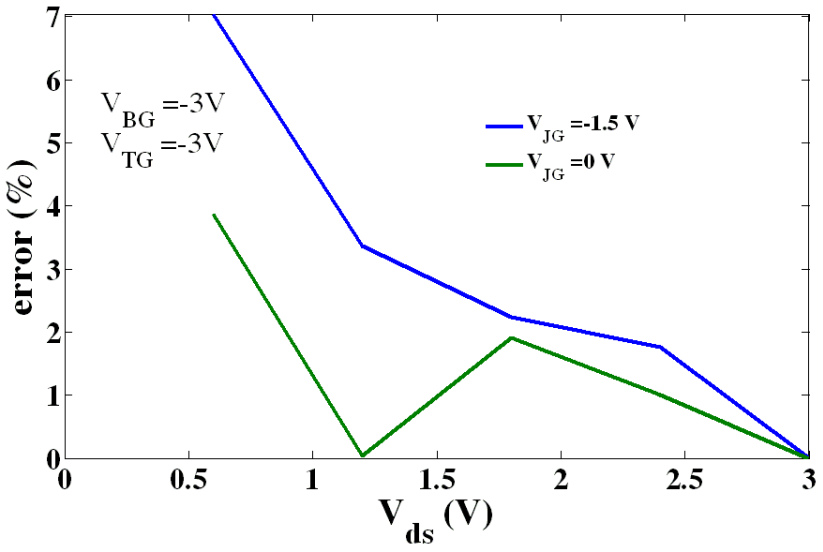


(b)

Figure 6.12: (a) Comparison between experimental results and numerical model of device # 3; (b) error between experimental results and numerical model of device # 3.

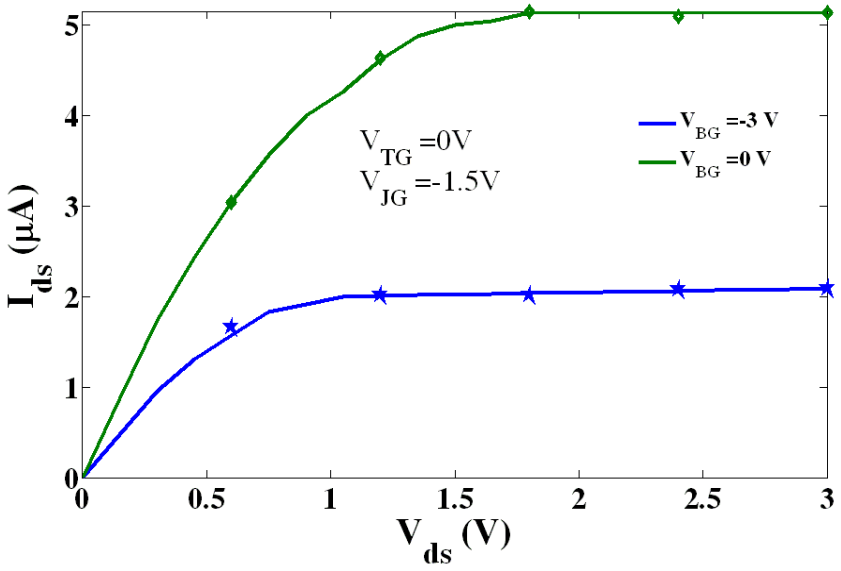


(a)

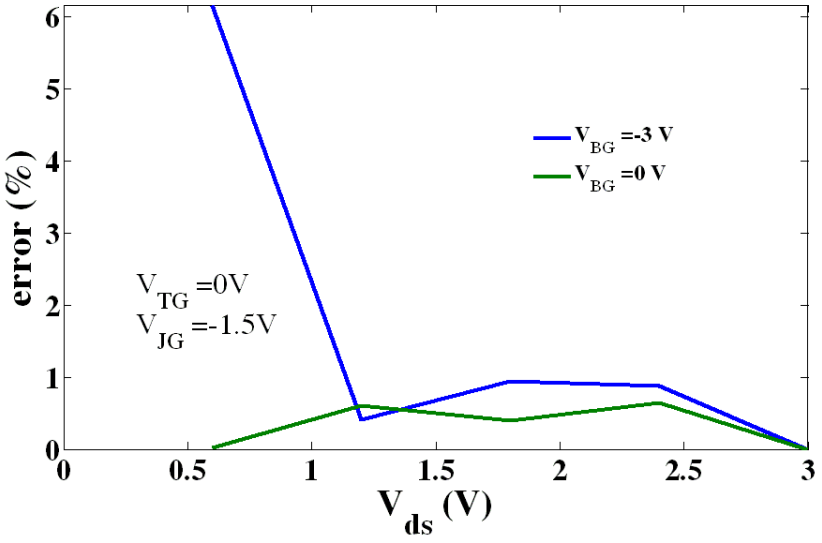


(b)

Figure 6.13: (a) Comparison between experimental results and numerical model of device # 3; (b) error between experimental results and numerical model of device # 3.

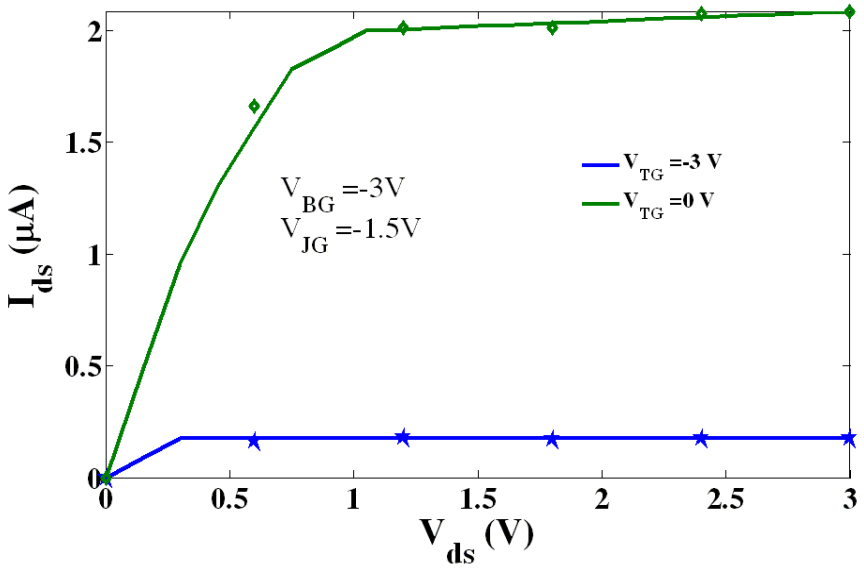


(a)

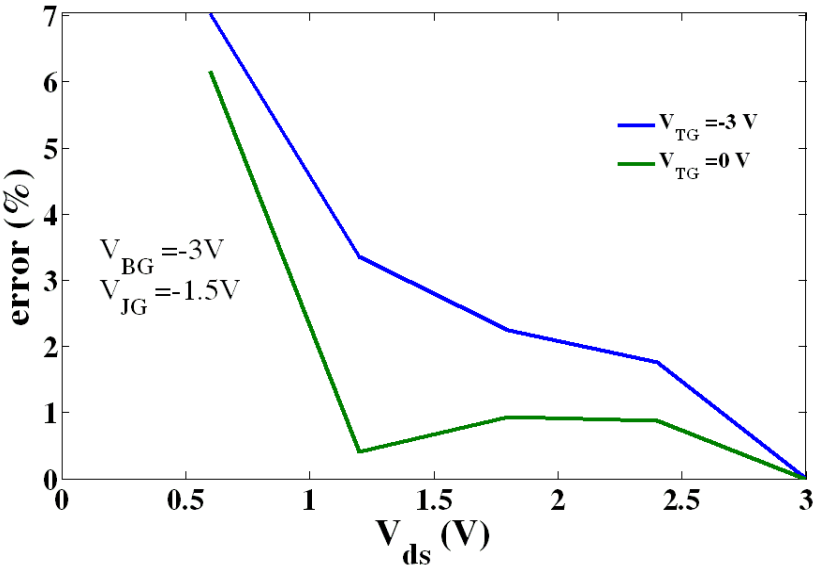


(b)

Figure 6.14: (a) Comparison between experimental results and numerical model of device # 3; (b) error between experimental results and numerical model of device # 3.

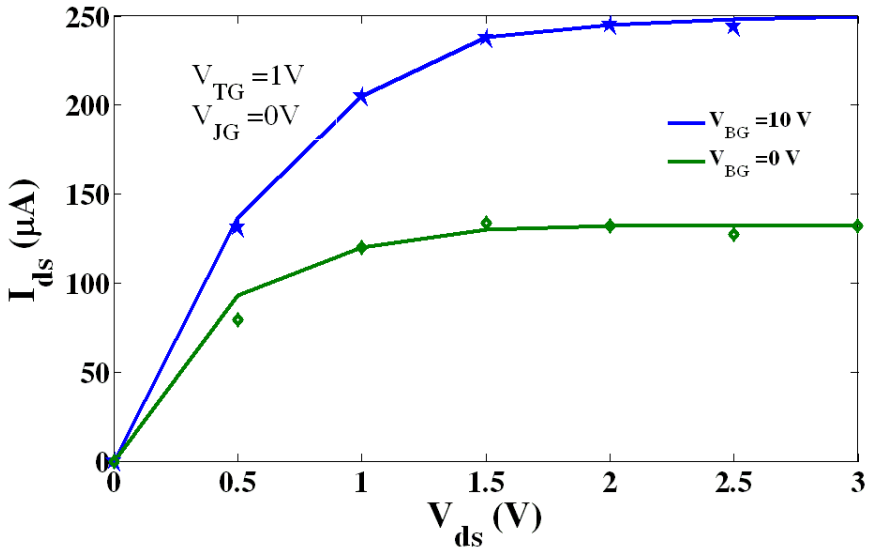


(a)

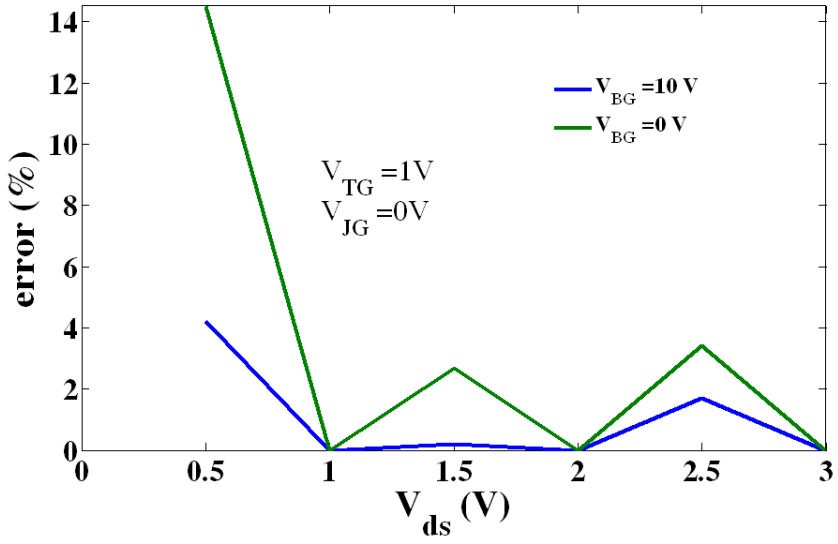


(b)

Figure 6.15: (a) Comparison between experimental results and numerical model of device # 3; (b) error between experimental results and numerical model of device # 3.

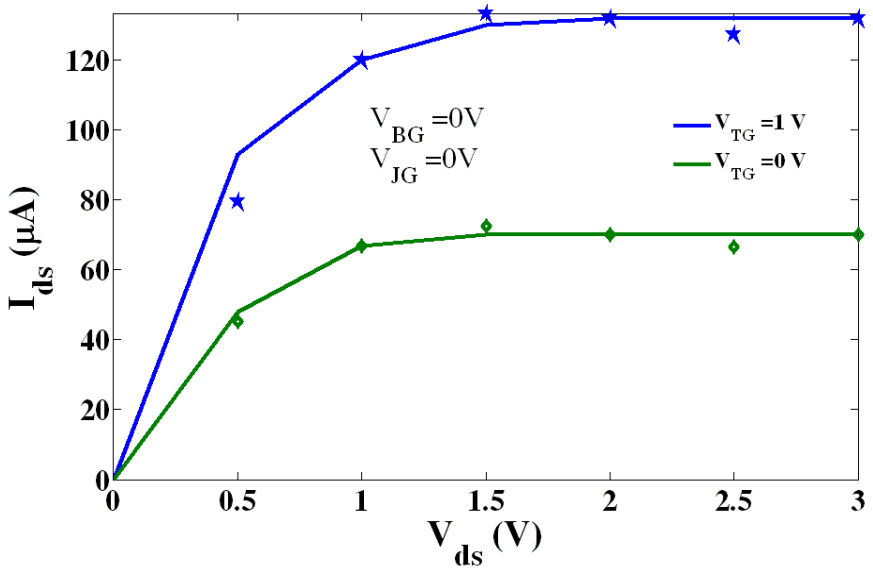


(a)

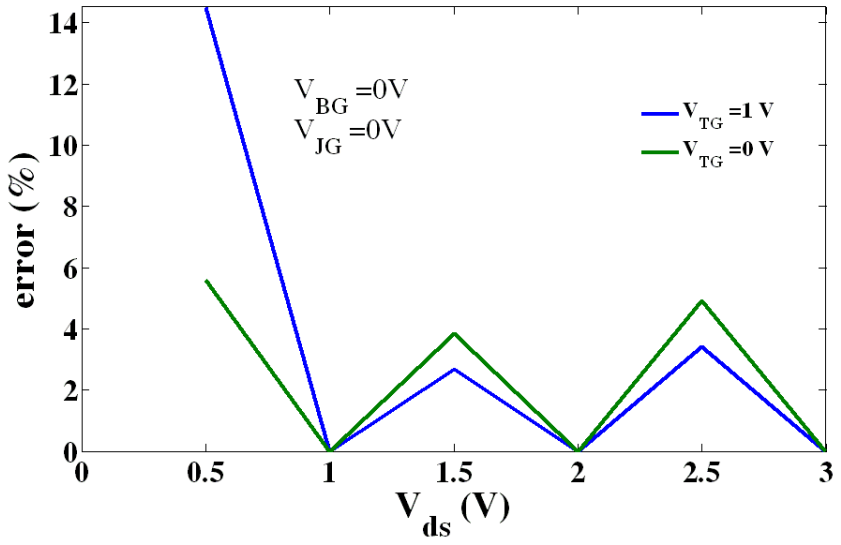


(b)

Figure 6.16: (a) Comparison between experimental results and numerical model of device # 4; (b) error between experimental results and numerical model of device # 4.

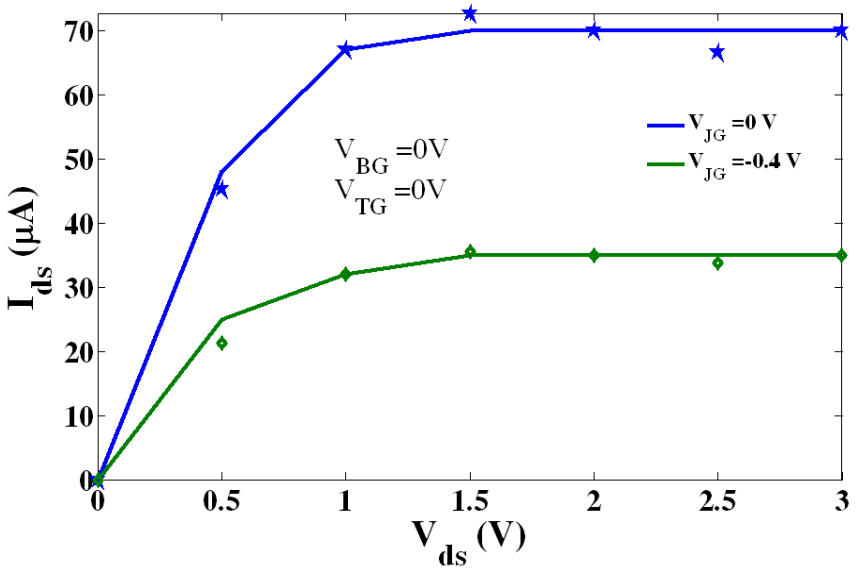


(a)

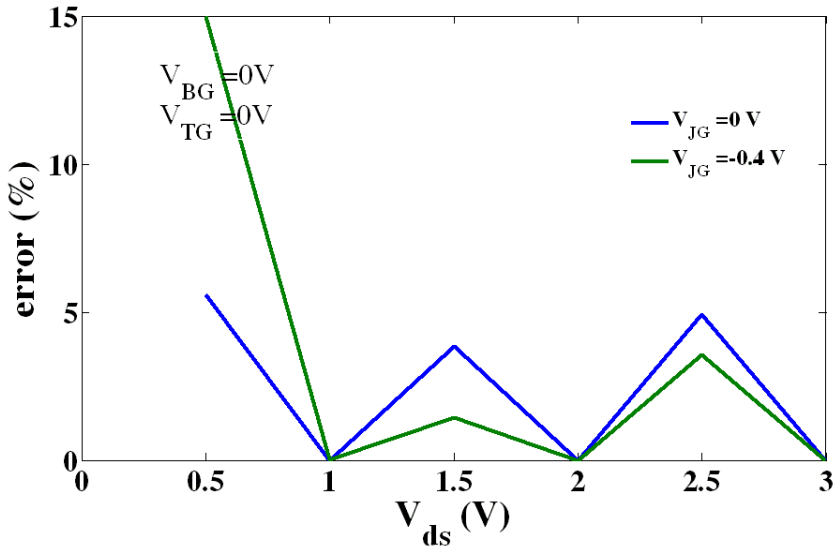


(b)

Figure 6.17: (a) Comparison between experimental results and numerical model of device # 4; (b) error between experimental results and numerical model of device # 4.



(a)



(b)

Figure 6.18: (a) Comparison between experimental results and numerical model of device # 4; (b) error between experimental results and numerical model of device # 4.

6.5.5 Simulated results

This section presents the model development and verification using the data generated from the device simulator of the devices under consideration. The modeling procedure described above is now applied to the development a numerical model for a G^4FET.

A hypothetical G^4FET is simulated using the parameters as shown in Table 6.1. The device is simulated for the drain current as a function of different terminal potentials. Figure 6.19 shows the available simulated data for the drain current obtained from the numerical simulator. The available data covers wide range of operating potentials for the top gate, the back gate, the junction gates and the drain voltage. The simulated data is used to generate Lagrange coefficients and Lagrange polynomial for the drain current as a function of different terminal potentials.

The Lagrange polynomial obtained from the available data is used to predict the device characteristics for different terminal potentials. Figure 6.20 shows the comparison between the model results and the available data. It shows that the model is in good agreement with the available data. The comparison is done for wide ranges of terminal potentials. Therefore, the numerical model is application for a wide range of operation.

Figure 6.21 shows the comparison between the available data and the results obtained from the model for different order of Lagrange polynomials. It shows that for same gate potentials the error is less for higher order of polynomial. However, as the order increases the error tends to flatten at a certain value. The reduction of error is very small for further increase of order of polynomials.

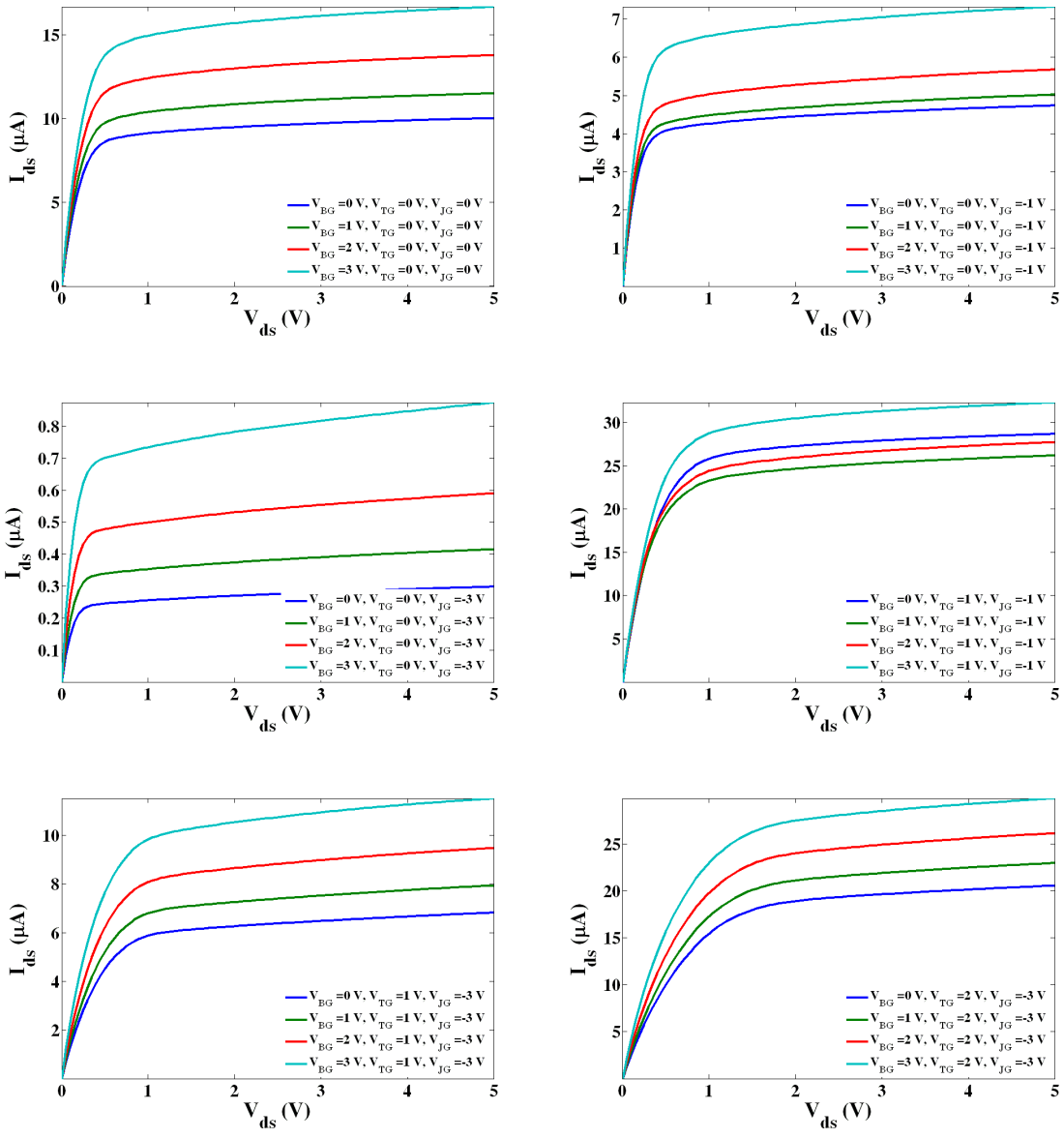


Figure 6.19: Available data from numerical simulator for the drain current for wide range of potentials at different terminals.

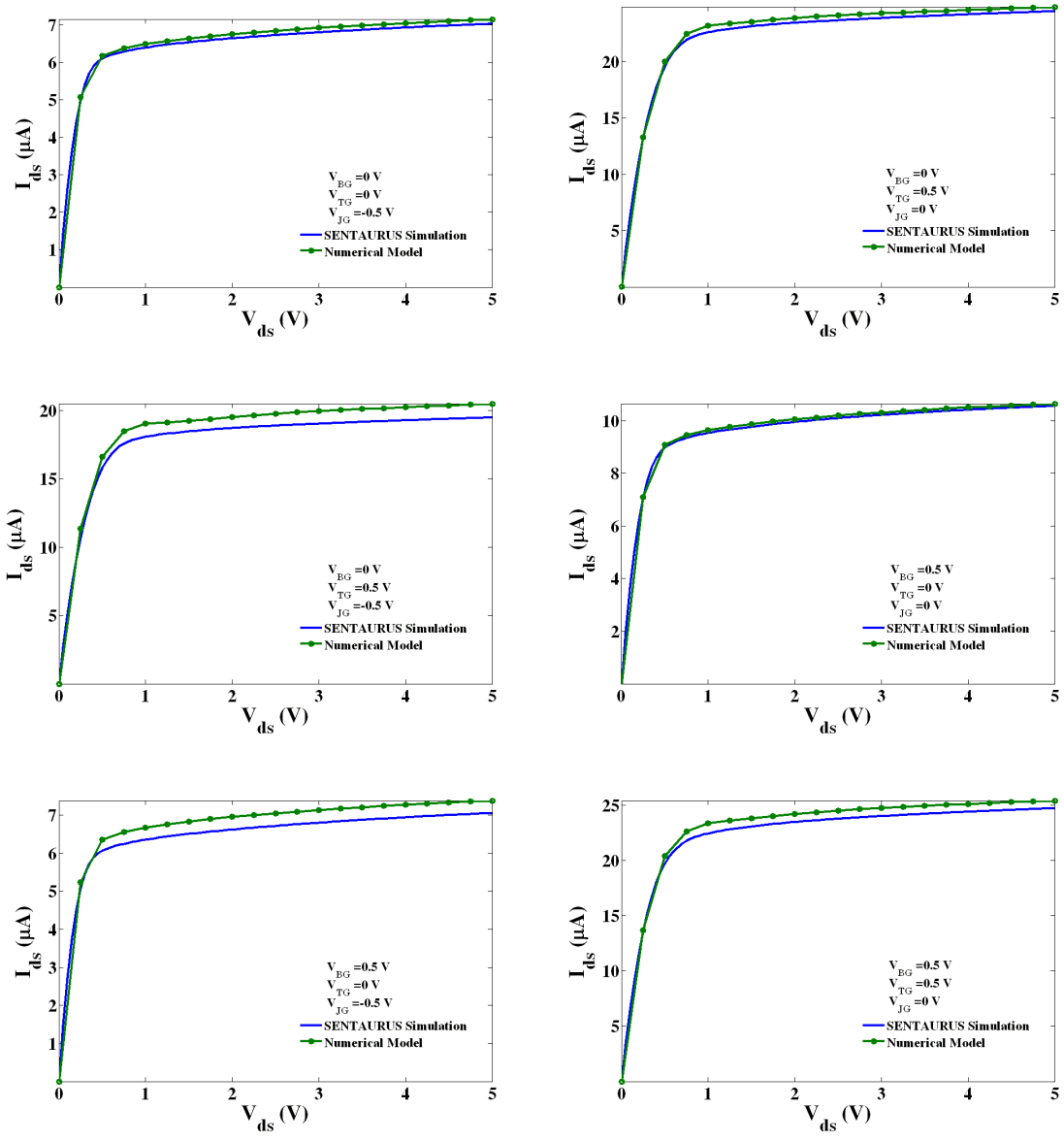


Figure 6.20: Comparison of available data and model results.

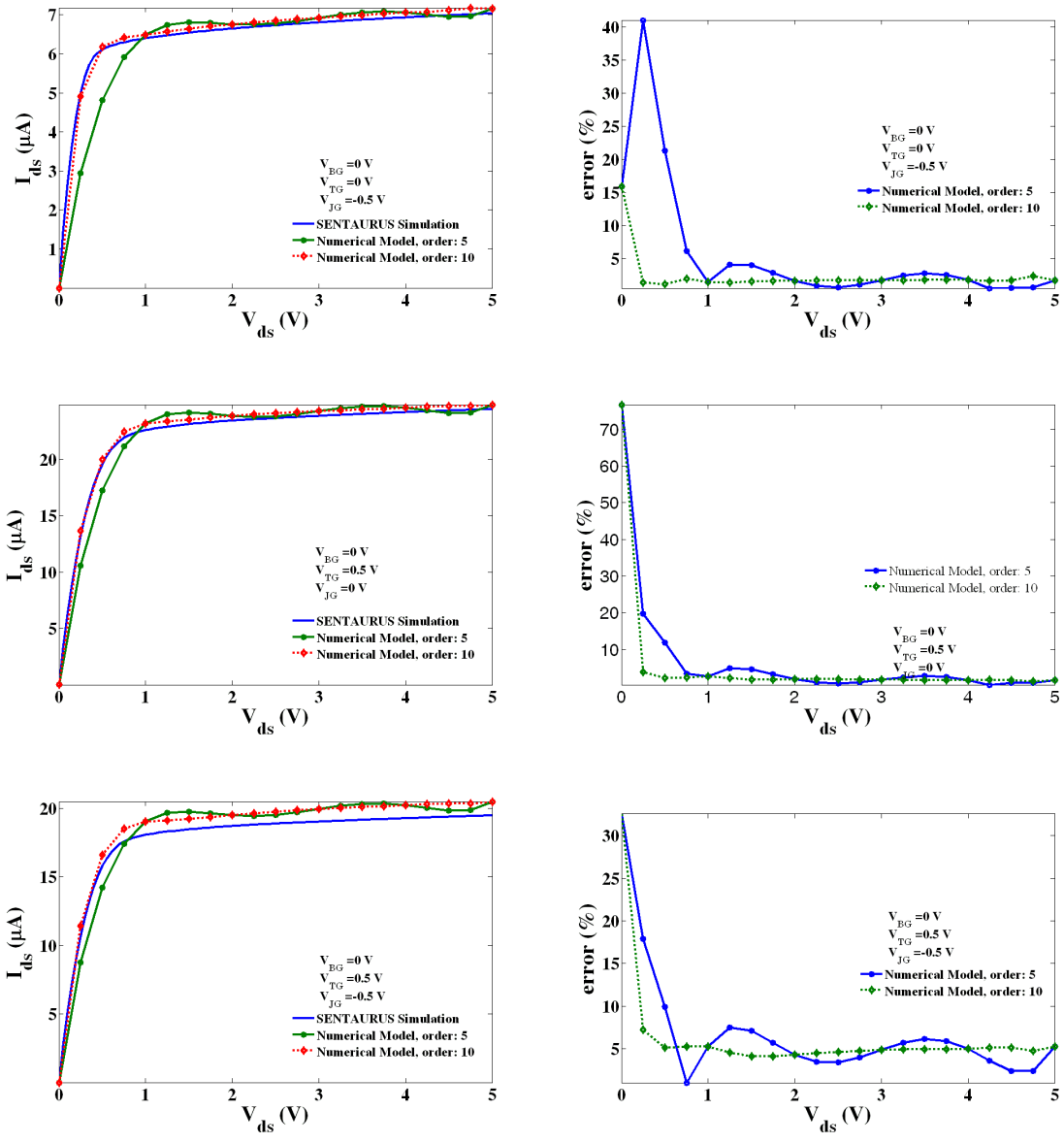


Figure 6.21: Comparison of different orders of the model.

6.6 SPICE model of G^4FET

SPICE, or the Simulation Program with Integrated Circuit Emphasis, was developed at the University of California, Berkeley by Larry Nagel [65]. SPICE is an open-license program which is one reason for its popularity. Now it is used by almost all electrical engineers. SPICE is a general-purpose electronic circuit simulator. It is a powerful program used in integrated circuit (IC) and board-level design to check the integrity of circuit designs and to predict circuit behavior.

Circuit simulation programs, of which SPICE and derivatives are the most prominent, take a text netlist describing the circuit elements (transistors, resistors, capacitors, and transistors) and their connections, then translate them into equations to be solved. The general equations produced are nonlinear differential algebraic equations which are solved using implicit integration methods, Newton's method, and sparse matrix techniques.

A component in SPICE is represented by two ways: model and subcircuit. A model is collection of predefined parameter; whereas a subcircuit can be modified according to user specifications. The model works well for traditional circuit components. However, the subcircuit can describe a nontraditional circuit component like the G^4FET.

A G^4FET has six independent terminals: one source, one drain, one top oxide gate, one bottom oxide gate, and two lateral junction gates. Generally, the source is tied to the ground and all the potentials at different terminals are applied with respect to the source. For simplicity, both of the junction gates are tied together. Therefore, the current flowing through the channel from the drain to the source is a function of the potentials of the drain, the top oxide gate, the bottom oxide gate, and the junction gates. Figure 6.22 shows the DC

equivalent circuit of a G^4FET for SPICE simulation. It shows that a current source is connected between the drain and the source. The direction of current is defined from the drain to the source. The magnitude of the current depends on the values of the potentials at the top, the back and the junction gates. The gate terminals are left unconnected as these are physically isolated from the channel either by oxide layers or by a reverse biased p-n junction.

The formation of the subcircuit of a G^4FET starts with generating the Lagrange polynomial of the drain current as a function of the potentials of the drain, the top oxide gate, the bottom oxide gate, and the junction gates. Thereafter, this polynomial is inserted into a subcircuit file written with the format specified by SPICE as shown in Figure 6.23. The subcircuit includes names of all terminals. It also includes a current source connected between the drain and the source. The value of the current passing through the current source is defined by the Lagrange polynomial, which is from the available data. The subcircuit can be used for simulating any circuit containing a G^4FET.

6.6.1 DC simulation of G^4FET

The subcircuit for G^4FET is used to simulate the DC characteristics. Figure 6.24 shows the comparison between the available data and the results from the SPICE simulation for different gate potentials. The deviation between the SPICE simulation and the available data is due to the fact that SPICE utilizes matrix algebra, instead of direct

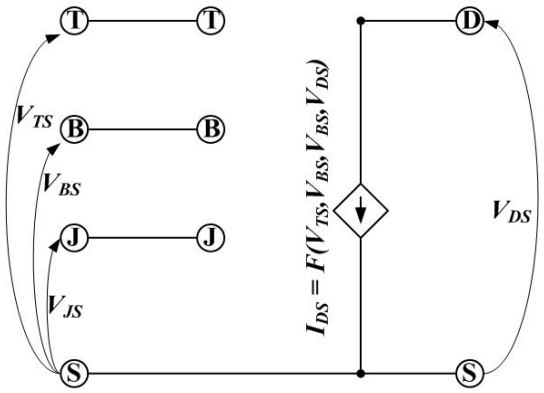


Figure 6.22: DC equivalent circuit of G^{4}FET.

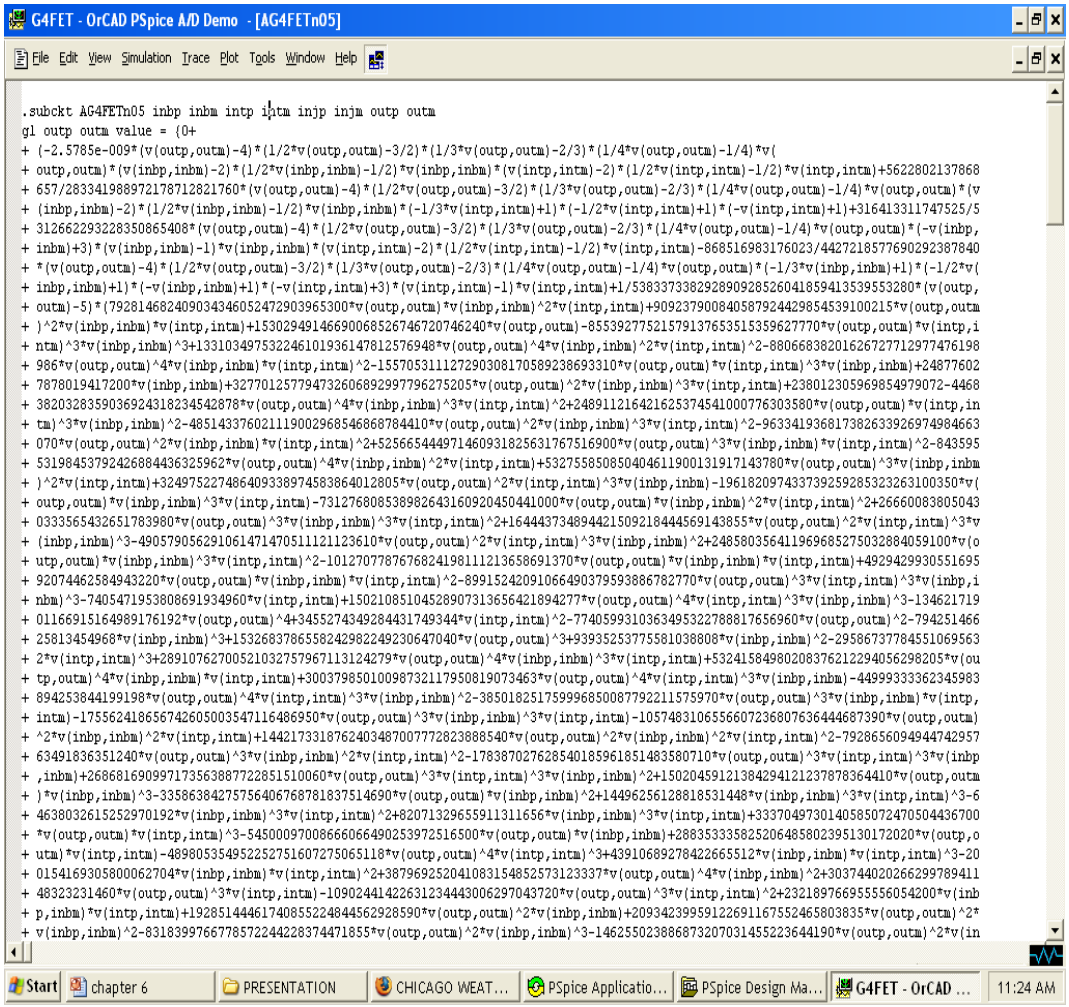


Figure 6.23: G^{4}FET subcircuit description for PSPICE.

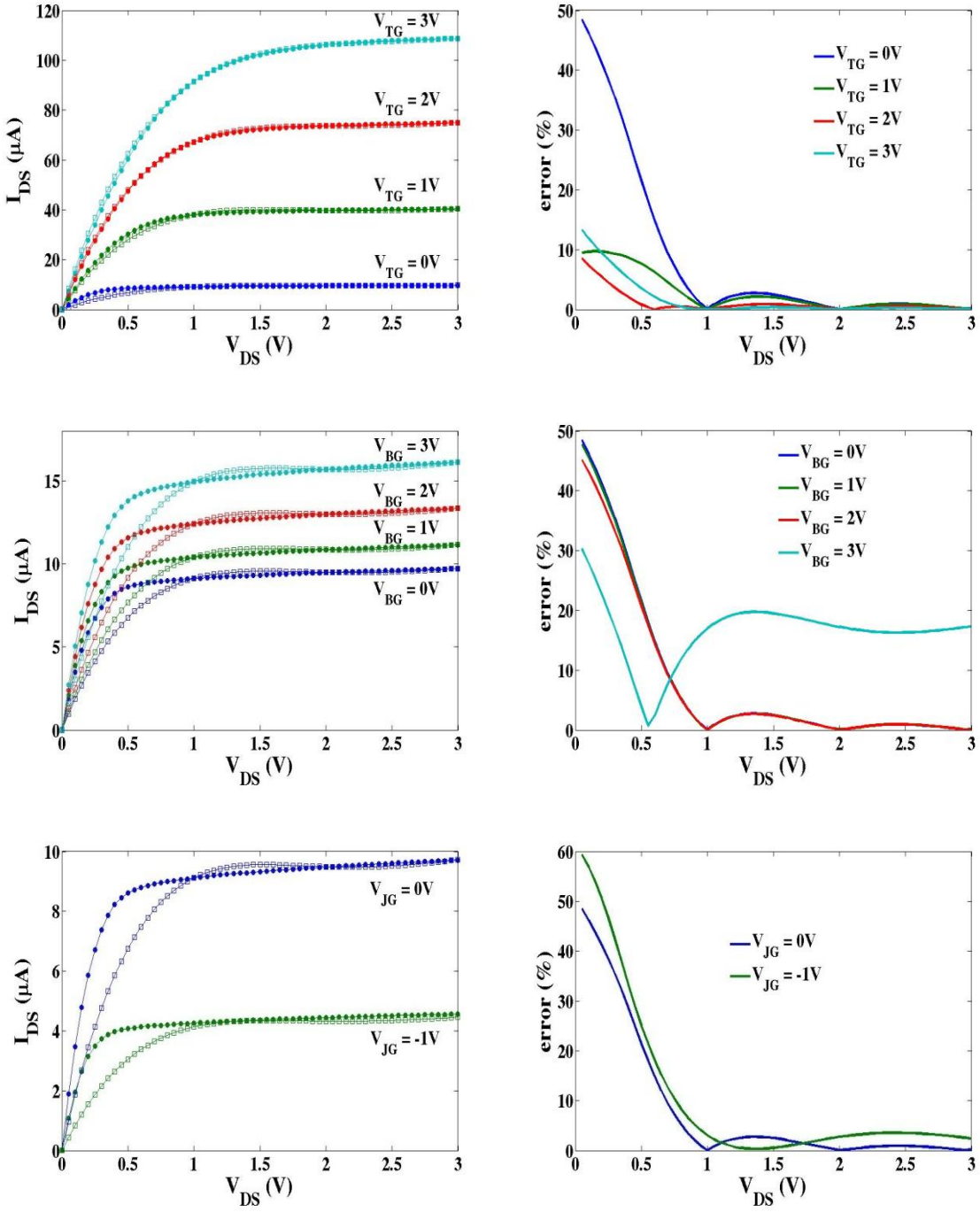


Figure 6.24: Comparison between the available data and SPICE DC simulation.

evaluation of polynomial, to solve potentials at different nodes. The figure shows that the error is smaller in the saturation region than that in the triode region.

6.6.2 Current mirror using G^{4}FET

G^{4}FET has versatile applications. Mixed-signal circuits can be developed using G^{4}FET. The fundamental building block of an analog circuit is a current mirror. A current mirror, as shown in Figure 6.25, is designed to sink 100 µA of current. The current mirror utilizes the conduction property of the top gate. Other gates are always tied to source. As the top gate is a depletion mode MOSFET the gate potential can be lowered to as low as 0V. The value of the resistance is selected such that the top gate potential is kept at 0V.

Figure 6.26 show the output characteristics of the current mirror as shown in Figure 6.25. For output voltage of 1.1V or above, it can sink 100 µA. The output voltage cannot be lowered below 1.1V as the top gate of G^{4}FET is depletion mode device, it requires higher drain voltage, than the enhancement mode MOSFET, to be operated in the saturation region.

6.6.3 Differential amplifier using G^{4}FET

A differential amplifier is designed as shown in Figure 6.27. A 100 µA ideal current source is used to bias the circuit. The back and the junction gates are tied to the source. The differential inputs are applied at the top gates. The resistors share the equal amount of current while the differential input is 0V. Therefore, the differential output is also 0V. When the input at any of the top gate is larger than that of the other, the resistor no longer shares equal

amount of current. Therefore, there will an imbalance between the potential drops across the resistors. It causes a potential differential difference between the drains of two G^4FET.

Figure 6.28 shows the transfer characteristics for DC (Figure 6.28 (a)) and transient (Figure 6.28 (b)) analysis. It shows that the input-output relation is linear over a limited range of input potential. It also shows that the offset is 0V at the quiescent point of operation.

6.6.4 Inverter using G^4FET

An inverter is designed as shown in Figure 6.29. Due to the lack of model for p-G^4FET the inverter is designed with a resistor connected at the drain of p-G^4FET. The back gate and the junction gates are connected to ground, which is also the source of G^4FET. The time varying input is applied at the top gate and output is observed at the drain terminal.

Figure 6.30 shows the input-output relation of the inverter as shown in Figure 6.29. It shows that output-high is less than the supply potential, which is 3V for this simulation. This is due to the fact that the top gate of G^4FET is a depletion mode device. It does not turn off when the input voltage is 0V. Moreover, the output-low is higher than the ground potential, which is 0V for this simulation.

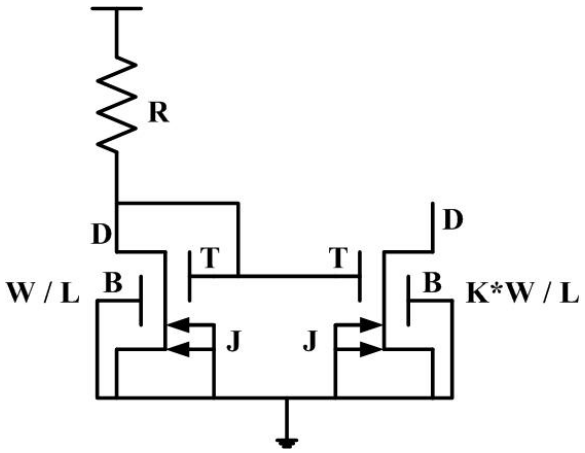


Figure 6.25: Current mirror using G^{4}FET.

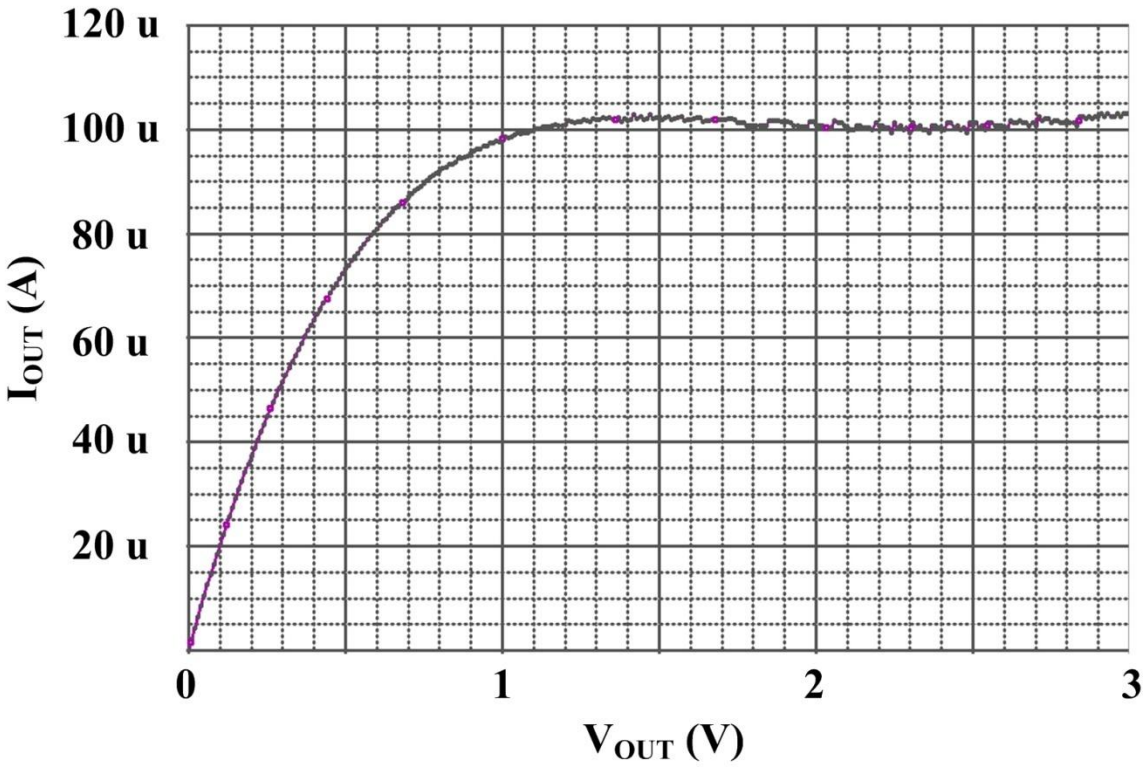


Figure 6.26: Output characteristics of current mirror using G^{4}FET.

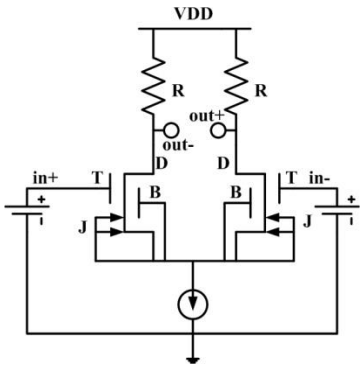
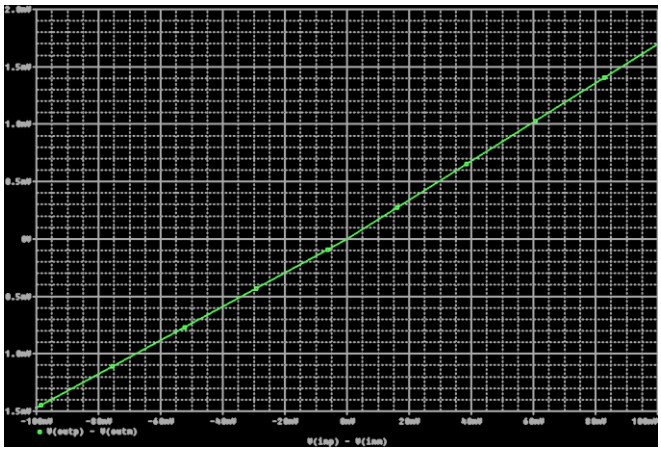
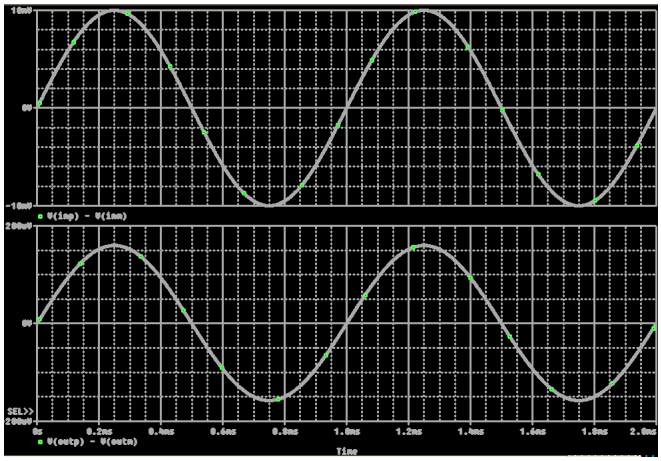


Figure 6.27: A differential amplifier using G^4FET.



(a)



(b)

Figure 6.28: The transfer characteristics of differential amplifier (a) DC; (b) transient.

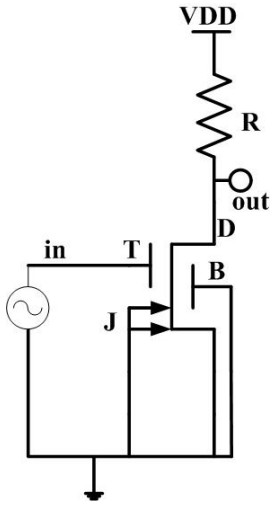


Figure 6.29: The schematic of an inverter with G^4FET.

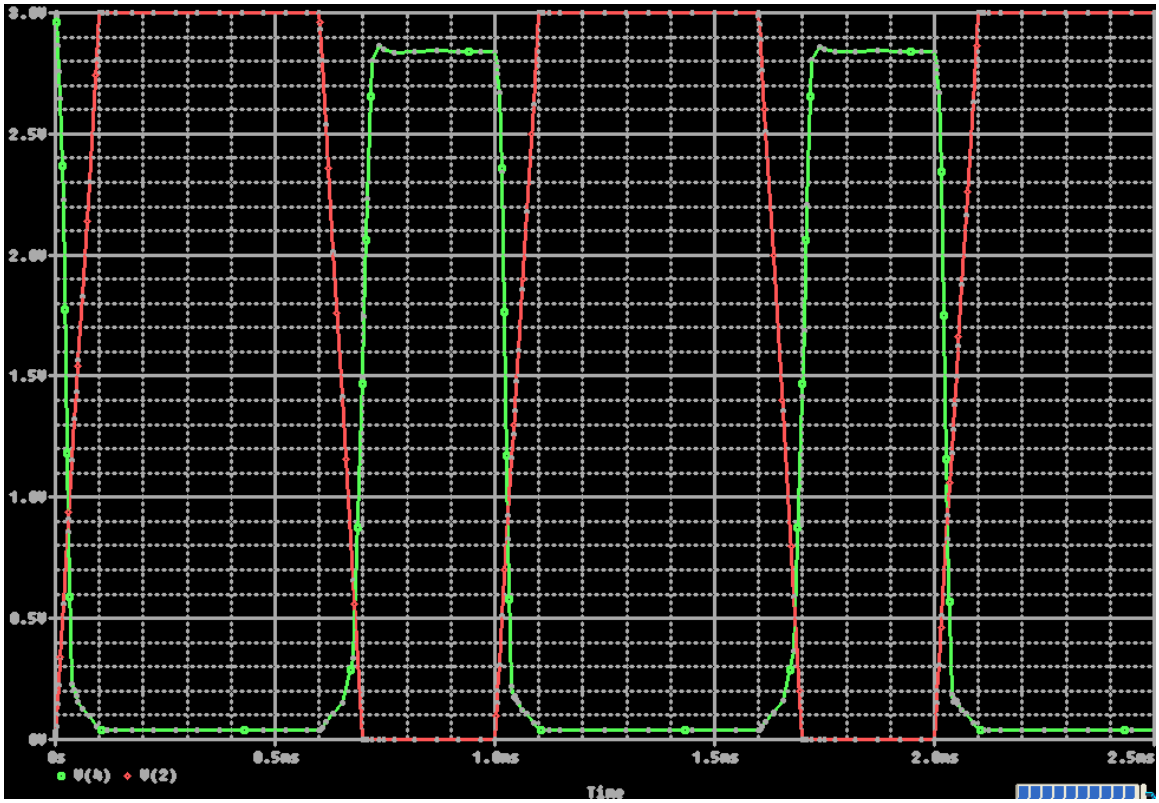


Figure 6.30: the input and the output of an inverter using G^4FET.

6.7 Conclusion

The model developed in this chapter is efficient in terms of derivation and computation and is always reliable as it is derived from the available data. Although this model is developed for potential variations at different terminals, it can be easily extended for any number of variables such as device length and width and operating temperature, provided the experimental results are available. The model, described in this chapter is based on Lagrange polynomial, and provides a single expression that is applicable over the entire region of operations and can be considered a global function.

The developed numerical model can be used to develop a SPICE subcircuit for G^4FET. This subcircuit can be used to simulate any circuit containing G^4FET. A current mirror, a differential amplifier and an inverter are simulated with SPICE using the subcircuit of G^4FET.

CHAPTER SEVEN

Conclusion and Future Work

7.1 Original contributions

G^4FET is a novel device, which has been invented in 2002. There are very few works reported in literature on modeling of the G^4FET. First effort on modeling of G^4FET was reported on 2007 [20]. The threshold potential of different gates of the G^4FET was formulated with the assumption of complete depletion of channel by the junction gates. The potential distribution was assumed to be parabolic inside the channel.

Another approach of the G^4FET modeling was reported on 2006 [15]. An analytical model was proposed for a special condition of depletion of all four gates. The charge control method was used to develop the model. It also utilized an empirical number to fit the model with the available data.

This work includes a different method of modeling of the G^4FET. There are three different methods for analyzing semiconductor devices: physics based carrier transport modeling, charge control modeling and numerical modeling. Physics based modeling includes developing analytical expressions of carrier mobility and carrier recombination-generation. The variations of these parameters with temperature, doping, and velocity saturation are also considered. Physics based modeling is a valuable tool which can be used to understand the device operation. It is the first step of device modeling that provides information about the device operation. Physics based charge control model is the most comprehensive model and it

does not consider any approximation. This work is the first reported carrier transport model on for the G^4FET and no other work on the carrier transport model has been reported.

The second method of device modeling is the charge control method. This method also involves solving fewer equations than the physics based modeling. Moreover, the analysis is simplified with a few assumptions. In this method, the gate and the channel charges are calculated in terms of the gate voltages. The charge control method provides a closed form of expression for the device characteristics. This method does not use any empirical relation to estimates the area of the conduction channel as done in the literature. Rather it uses the distribution of the carrier concentration to determine the conduction area in the channel.

The third method of modeling is the numerical modeling. It involves developing an interpolation expression for the device characteristics from the experimental data. In this work Lagrange polynomial is used to develop a numerical model of the G^4FET. The essence of Lagrange polynomial is that it provides a single expression for the entire range of device operation. It can also be used to develop a circuit of the G^4FET. There is no report on numerical model of G^4FET and this work is the first of this type.

The numerical model can be used to develop a SPICE model for the G^4FET. SPICE is a valuable tool for circuit simulation. In order to validate the circuit design, it is industry standard that the circuit be simulated with SPICE. There is no report of SPICE model for the G^4FET and the very first SPICE model has been developed in this work.

Therefore, the original contributions of this research can be summarized as:

- Physics based carrier transport model: It is the most extensive model, without considering any approximation. It includes the effects of mobility, carrier generation-recombination, temperature, doping, and electric field. It is used to design the device for optimum performance. This work represents the first carrier transport model of the G^4FET ever reported.
- Charge control modeling: It is used to predict the characteristics of G^4FET without going into the details of device physics. It is an alternative but not a substitute to the carrier transport model. It can be used for fast prediction of device performance. This work assumes no empirical relation as reported previously in literature.
- Numerical model: Both the carrier transport model and the charge control model deal with different physical parameters to predict the device performance. These methods do not reflect the actual device characteristics. The numerical method is used to model a device which physically exists. In this work Lagrange polynomial is used to develop a numerical model of the G^4FET. The essence of Lagrange polynomial is that it provides a single expression for the entire range of device operation. It can also be used to develop a circuit of the G^4FET. This work is the first numerical model of G^4FET ever reported.
- SPICE model: SPICE is the industry standard circuit simulator. In order to validate the circuit design, SPICE is used to simulate the circuit for the functionality. Due to wide range application of the G^4FET, it has become a

necessity to develop a SPICE model for the G^4FET. This work is the first SPICE model of for the G^4FET ever reported.

7.2 Dissertation summary

The characteristics and applications of the G^4FET are extensively investigated in this dissertation. The G^4FET is analyzed for the carrier transport model, the charge control model, and the numerical model. Each approach of modeling has its own advantages. The carrier transport model provides information about the conduction mechanism of the G^4FET. This information is useful in designing a G^4FET for optimum performance with different constrains. The charge control method provides a closed form of expression to predict the characteristics of a G^4FET in terms of the different terminal potentials. This method also assists in determining the threshold voltages and different regions of operation. The numerical analysis results in a circuit model that can be used in the circuit simulator to simulate a circuit containing a G^4FET and has an important practical impact.

Few disadvantages are found in the above mentioned methods. No individual method is complete and sufficient to describe a G^4FET. In order to understand the device physics, predict device characteristics, and use them in a circuit, all three models are required.

7.3 Future Works

Although the characteristics and applications of a G^4FET are extensively investigated in this dissertation, there is room for further contributions in the research of a G^4FET. The immediate requirement for future works includes:

1. Finite element solution of the carrier transport equation;
2. Inclusion of the channel length modulation with the charge control modeling; and
3. Extension of the Lagrange polynomial based numerical method to include the effect of channel length, width, temperature, etc.

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