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Low-power switched capacitor voltage reference

Suheng Chen
University of Tennessee

To the Graduate Council:

I am submitting herewith a dissertation written by Suheng Chen entitled "Low-power switched capacitor voltage reference." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Benjamin J. Blalock, Major Professor

We have read this dissertation and recommend its acceptance:

Accepted for the Council:

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Low-power Switched Capacitor Voltage Reference

A Dissertation

Presented for the

Doctor of Philosophy Degree

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Suheng Chen

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Abstract

Low-power analog design represents a developing technological trend as it emerges from a rather limited range of applications to a much wider arena affecting mainstream market segments. It especially affects portable electronics with respect to battery life, performance, and physical size. Meanwhile, low-power analog design enables technologies such as sensor networks and RFID. Research opportunities abound to exploit the potential of low power analog design, apply low-power to established fields, and explore new applications.

The goal of this effort is to design a low-power reference circuit that delivers an accurate reference with very minimal power consumption. The circuit and device level low-power design techniques are suitable for a wide range of applications. To meet this goal, switched capacitor bandgap architecture was chosen. It is the most suitable for developing a systematic, and ground-up, low-power design approach. In addition, the low-power analog cell library developed would facilitate building a more complex low-power system.

A low-power switched capacitor bandgap was designed, fabricated, and fully tested. The bandgap generates a stable 0.6-V reference voltage, in both the discrete-time and continuous-time domain. The system was thoroughly tested and individual building blocks were characterized. The reference voltage is temperature stable, with less than a 100 ppm/°C drift, over a –60 dB power supply rejection, and below a 1 μA total supply current (excluding optional track-and-hold). Besides using it as a voltage reference, potential applications are also described using derivatives of this switched capacitor bandgap, specifically supply supervisory and on-chip thermal regulation.

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Chapter 1 INTRODUCTION

1.1 Motivation of Low Power Design

From the first integrated circuit (IC), as demonstrated by Jack Kilby in 1958, to more advanced IC products now found in virtually every corner of the world, the semiconductor industry has continued forward from its first success by fast-pacing improvement trends of higher integration levels, lowered costs, higher speeds, lower power consumption, increased compactness, and newer functionality [1].

Interestingly, awareness of power consumption was not widely recognized until the early 1990s [2]. Before then, only a narrow range of applications were dedicated to a power-constrained design space. Such applications included wristwatches, hearing aids, hand-held calculators, and pacemakers. Today, power consumption has come to represent a more important design interest to almost all major IC product market segments. For portable applications that are battery-powered, power consumption directly determines battery life between recharge cycles, functionality, system performance, and the physical dimensions/weight of the system. On the other hand, for wired application that are less constrained by mobility, such as desktop computing and network communication, higher energy efficiency and minimum off-state power consumption not only translates to lower utility bills, but also leads to the benefits of less heat generation and hence, improved product reliability. It also promotes a less stringent requirement of thermal packaging and heat sink, and therefore, a reduction of system volume and weight. In a broader perspective, efficiency awareness initiatives such as Energy Star have become the industry standard and have demonstrated their benefits such as cutting green house gas emission [3]. New emerging industry efforts, such as Climate Saver Computing Initiatives [4], are advocated by major computer industry players including Google Inc. and Intel Inc. This clearly indicates a technological trend towards improved energy efficiency.

Nevertheless, the opportunity for low-power design lies far beyond solving existing problems. Arguably, low-power has become an enabling technology that encourages and fosters new and unconventional applications. RFID (radio-frequency identification) is one technology that would not be so widespread and successful without low-power design. It is expected that by advocating low-power design and recognizing it as an important aspect of the industry roadmap, newer applications of IC products enabled by low-power technology will emerge on our horizon.

1.2 Applications for Low Power

Besides conventional applications, including the wristwatch, hearing aid, and pacemaker, new applications using low-power are appearing daily. Generally, these applications tend to have low speed, low accuracy requirements, and low activity rates, but at the same time, can greatly benefit from an energy efficiency that allows more portability, a reduced complexity, and cost reduction.

One important application area of low-power is the micro-sensor. A micro-sensor is a small-profile device that is capable of sensing, event detection, and computation. Some micro-sensors are equipped with wireless transceivers that allow individual sensor nodes to collaboratively sense, process data, and relay useful information to the host. Examples of emerging applications using the micro-sensors include infrastructure security, environment and habitat monitoring, industrial sensing, traffic control [5], and structural monitoring [6].

Another important application using low-power is RFID. The technology allows object identification within an effective range by transmitting and receiving radio-frequency signals between the reader and transponder. The transponder, often referred to as the RFID tag, can be passive or active, depending on whether it is powered with backscattering from the carrier wave reader, or powered with an internal supply. Benefits of using the passive transponder with a low-power IC [7] include a smaller size and reduced cost, so the tag can be embedded into product labels, and the integration of more advanced features enabled by on-chip logic and memory. A recent thrust towards a more secured RFID tag requires more complex features on the IC to apply cryptographic technique, which does consume more power.

As portable electronics perform more complex features, most require a low-power digital signal processor (DSP) or microcontroller (MCU) IC. A DSP IC performs signal processing in the digital domain, and is often used to implement features in consumer electronics such as audio signal processing, speech recognition, image/video processing, and more. Microcontrollers can be programmed for a dedicated task or generalized computations. To extend the system range and battery lifetime, a wide array of power/performance modes are devised to optimize power efficiency. An example is the wireless handset IC that requires peak performance when in high activity mode to carry out tasks such as phone calls, data communication, TV, and uses minimum energy during low activity modes to maximize standby time.

As low-power enabled technology becomes more popular, industry specifications focusing on low-speed, low-cost ubiquitous communication are being devised, including IEEE 802.15.4

[8] and ZigBee®, to standardize resource allocation, communication protocol, and provide a platform for new applications.

1.3 System Driver and the Role of Low Power Analog Design

Four major system drivers are often characterized to drive different applications. They are the system-on-a-chip (SoC), microprocessor (MPU), analog/mixed-signal (AMS), and embedded memory [9]. For low-power applications, these are consistent except that tight constraints are placed on their power consumption.

Among the four system drivers, analog plays an important role when dealing with real-life, continuously variable signals in the presence of variations due to process, voltage, temperature, and noise. Although some signals are converted into the digital domain to allow processing and storage, analog circuits remain dominant in the most fundamental functions including interfacing between analog and digital domain, and almost all events of detection and triggering. Common examples include providing on-chip supply and voltage/current bias, detecting on-chip/off-chip events relating to power, ambient and open/close circuit, buffering signals off-chip and driving LEDs, and very importantly, applying a power management scheme to maximize efficiency.

For low-power applications, all analog functions mentioned above are delivered with the least compromise of performance, and with an extra emphasis on static/short-circuit power consumption. Not surprisingly, tight power budget impose significant challenges on established circuit topologies, conventional device biasing techniques, and the familiar design practices that warrant reexamination for low-power applications. In the meantime, tight system power budget place elaborate power management scheme in an ever important position to maximize current and therefore power efficiency at the system level. Common power management schemes include low power (i.e. *stand-by* and *sleep*) modes to disable features and cut back performance to conserve energy. More elaborate, application-specific power management schemes can include multiple low-power modes to drop the system power to the bare minimum.

Above all, evidence shows that low-power analog circuit and device-level designs are the frontline in meeting power specifications and delivering essential features, which is parallel with the system, algorithm, and architecture-level low-power consideration in the recommended top-down low-power design methodology [10].

1.4 Scope and Application of this Effort

This research effort is to focus on a circuit and device level low-power analog design to enable minimum system power suitable for a wide range of applications. More specifically, the effort researches a low-power voltage reference generator that not only delivers its primary function, providing a reference voltage, but can also be re-configured to a versatile low-power watch-dog circuit or sensor network. Either is able to function as a stand-alone unit or be integrated into a large scale system.

Voltage reference design is chosen for its ubiquitous existence and role in providing a fundamental feature. A voltage reference generates a fixed voltage that is insensitive to process, voltage, and temperature (PVT) variation. In most circumstances, the reference generator is active throughout all modes of operation. This makes it particularly meaningful in providing a reference voltage without consuming significant amounts of power, especially in low-power states. In this research, besides the primary goal of minimizing power consumption, a significant amount of design effort is focused on improving precision in the presence of trade-offs such as a degrading offset, increased transistor mismatch, and elevated noise in the direct exchange of low-power.

Besides delivering a well-controlled reference voltage for on-chip circuits, the derivatives of the reference circuit can be used in a wide range of applications; many of which would benefit greatly from its low-power consumption. One of its most important applications is to provide on-chip watch dog circuits such as the power-on-reset (POR) control. The task of the POR is monitoring the power supply when the system is powered up and generating a *power-good* signal to enable analog circuits and initialize on-chip digital logics to a known state. For applications that allow a system to enter low-power mode, the same circuit could also provide the *sleep/wakeup* function. Another important application that benefits from the circuit's low-power characteristics is a temperature sensor that can function as a stand-alone block, or as a part of an on-chip thermal regulation system. When on-chip thermal regulation is used, multiple copies of identical sensors are placed at different locations across the chip to monitor localized die temperature. Performing this function without adding to the power budget will allow further optimization of performance and reliability.

1.5 Overview of Dissertation

This dissertation is organized into 5 chapters. Chapter 1 discusses the motivation for research on low-power analog design, reviews established as well as emerging energy-

constrained applications that benefit from low-power technology, highlights the significance of low-power circuit design research and finally, dissects the low-power voltage reference as a demonstration vehicle for this effort.

Chapter 2 reviews prior-art literature and serves as a precursor for this effort. The first section reviews voltage reference applications, with the goal of establishing the design specification. The second section reviews past literature on IC voltage reference designs to better identify the most suitable circuit topology. In the third section, low-power design techniques are reviewed as preparation for this design.

In Chapter 3, circuit design and simulation are revealed in detail, and follows the design procedure through the process of device selection, verification of the device model, construction of the analog sub-cells, design of the individual circuit blocks, and finally, system assemblage.

Chapter 4 covers the IC test and characterization. It includes test procedures, presents measurement results, and provides further comparison with the design goal.

Finally, Chapter 5 provides a conclusion of this research and identifies future directions.

Chapter 2 REVIEW OF THE LITERATURE

2.1 Introduction

This chapter of literature review covers three main sections: voltage reference applications, prior-art voltage references, and literature on subthreshold analog design. The voltage reference circuit has a broad range of applications and has been a popular research focus in analog IC design, proven by the large number of patents and papers published. However, only a few of the key architectures that are the most unique and suitable for contemporary IC processes are selected for review to help identify the design goal and topology of this effort. Towards the end of this chapter subthreshold device characteristics are reviewed that are pertinent to low-power design as well as the review of select low-power subthreshold circuits that also influence this effort.

2.2 Applications of Voltage Reference

The voltage reference is truly an essential and versatile circuit to almost all electronics systems. Its application encompasses on-chip design, used to interface circuit blocks on a common IC; and off-chip design, used to interface other ICs within a system. In addition to providing a reference voltage, various circuits have been derived that branch out to further applications.

As a voltage reference circuit, one of most common applications is to generate different levels of bias voltage for system function and provide voltage thresholds for detecting various events. The generated voltage needs to be stable and accurate to qualify as a good reference to ensure system functionality and precision requirements. Another important application of the voltage reference is data conversion, where the reference serves as a full-scale voltage that is a direct function of the output, in which case the reference accuracy directly affects the conversion resolution [11].

An immediate addition to a voltage reference is the capability of supplying a load current, which provides a voltage regulator. Combining its capability of supplying output current with its insensitivity to PVT, the voltage regulator is often used as a power supply for other circuits. A low dropout regulator is a variation of the voltage regulator with a minimum input-output voltage drop, which preserves the maximum voltage headroom for subsequent circuits. Its desirable merits primarily include insensitivity to PVT variation, low output impedance, and stability under different loading conditions.

Besides supplying a voltage, a common application of the voltage reference is to generate bias current for circuits on a common IC, or for other components within the system. Rendering bias current from a voltage reference is reliable and relatively inexpensive, and is often implemented using an amplifier and a resistor [12]. The end use can range from biasing amplifiers and oscillators, to an op-amp offset adjustment, and providing a floating reference for a window comparator [13].

By combining the core functionality of the voltage reference and additional peripheral circuits, a variety of applications can be derived that assist in the area of power management. Examples include a dedicated supply sequencer and monitor, display control, battery management, and temperature sensor. For on-chip circuits, usages include POR [14], brown-out protection [15] [16], and on-die thermal regulation [17].

The applications of the voltage reference are not limited to those reviewed. Also, realize that the design specification and emphasis for voltage reference circuits are often application specific. This effort places an emphasis on low-power design, while the generic design merits applied to the voltage reference are considered in the next chapter.

2.3 Voltage Reference Prior Art

2.3.1 Reference Standard and Reference Device

The voltage reference is a type of circuit that generates a well-controlled voltage. Ideally, it is insensitive to loading, supply variation and temperature, and the voltage can be used as a reference standard by other circuits within the system. The selection of a qualified reference needs to meet three criteria: universal, replicable, and practical. Among the many physical parameters, the energy gap between valence band and conduction band for a given semiconductor device is commonly chosen based on the three criteria.

The extraction of the energy gap, or *bandgap*, can be realized using semiconductor devices with a reasonable cost and complexity. A diode, or a diode-connected bipolar junction transistor (BJT) device, is most often the preferred reference device. When using an N-type BJT, or NPN device in this discussion, a current is injected into the base-collector node and the base-emitter junction voltage, $V_{BE,}$ can be acquired at different temperatures. The V_{BE} increases as temperature decreases, or equivalently, V_{BE} has a negative temperature coefficient. By extrapolating the linear relationship of V_{BE} vs. T to lower temperatures, it was expected that the extrapolated V_{BE} at 0 K is approximately the energy gap, E_g, or 1.2 V [18] for silicon. The sum of a CTAT (complementary-to-absolute-temperature) voltage established using a NPN V_{BE}

voltage, with an opposite trend or PTAT (proportional-to-absolute-temperature) voltage, can generate a temperature stable voltage. Figure 1 shows the concept of the bandgap circuit generating a temperature stable voltage (V_{BG}) by summing PTAT and CTAT voltages. (Figures appear in the appendix.)

2.3.2 Continuous-time Bandgap

The continuous-time bandgap refers to a bandgap voltage reference whose output voltage is valid at all times. The term continuous-time is used to distinguish them from their discrete-time counterparts, which will be reviewed in the following section. Various implementations of continuous-time bandgap circuits exist in literature with a time span of more than 30 years. The goal of this section is to highlight several key uses of the continuous-time bandgap, which can also serve as a comparison with its discrete-time counterparts to gain a better understanding of the pros/cons of either category.

2.3.2.1 Brokaw Bandgap

The bandgap voltage reference circuit invented by Brokaw, or called the Brokaw cell [19], along with its numerous variations, is the most prominent implementation of all bandgap architectures. In a simplified schematic of a Brokaw cell, as shown in Figure 2, the PTAT voltage is established with two different-sized NPN devices biased with same the current density, which can be written as

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{kT}{q}\ln\frac{J_1}{J_2} = \frac{kT}{q}\ln M \qquad \text{Equation 1}$$

where M is the ratio of emitter area between two NPN devices Q_1, Q_2 and J_1, J_2 are their current density. Amplified with the resistor ratio, the PTAT voltage is summed with the CTAT voltage, V_{BE1}, to generate the final voltage V_{OUT}.

$$V_{OUT} = V_{BE1} + 2\frac{R_1}{R_2}\cdot\frac{kT}{q}\ln\frac{J_1}{J_2} \qquad \text{Equation 2}$$

The start-up circuit is missing from the simplified circuit which is generally necessary for self-bias circuits. When powered up, the start-up circuit will push the bandgap circuit out of its zero-current stable operating point towards the desired operating point, then later shut itself off to avoid nonlinear disturbance. The implementation of the Brokaw cell requires BJT devices, which

are available in most bipolar or Bi-CMOS (complementary metal-oxide-semiconductor) processes.

2.3.2.2 CMOS Bandgap and Sub-1 V CMOS Bandgap

For bandgap circuits implemented in CMOS, a vertical PNP is often the preferred reference device as it tends to have better process control. For the vertical PNP device, its emitter is a P+ diffusion inside an N- well, which serves as its base region, and its collector is the P-substrate given that the process uses a P-type substrate material. To use the vertical PNP in a bandgap circuit, a slightly different circuit configuration is needed since the collector of the PNP device is connected to the substrate and hence, should always be connected to ground or V_{SS}. Figure 3 shows a simplified circuit configuration that is CMOS compatible [20].

The nominal output voltage of a common bandgap circuit is 1.2 V, by summing V_{BE} of a single diode and a PTAT established by the V_{BE} difference of two diodes. For applications requiring a higher bandgap voltage, the output of an integer multiple of 1.2 V can be achieved by applying amplifier gain. It is also possible to achieve a higher reference voltage with a voltage regulator. However, to get a bandgap voltage lower than 1.2-V, a sub-1 V bandgap architecture is almost always needed.

With a sub-1 V bandgap circuit, the bandgap output can be lower than the predetermined bandgap voltage, or 1.2 V. Among various designs of sub-1 V configurations, the current-mode sub-1 V bandgap proposed by Banba *et. al* [21] is one of the most frequently used. Instead of summing in the voltage domain, the PTAT and CTAT voltages are converted into the current domain, summed together, and converted back to voltage. Figure 4 shows the simplified schematic.

Although implementations of bandgap circuitry vary, the primary general specifications are applicable. Common specifications include that the generated voltage be repeatable, temperature stable, be reasonably insusceptible to supply ripple, have a robust start-up in all operating conditions, and be relatively area efficient.

Although a continuous-time bandgap can be simplistic in its architecture, the complexity involved in circuit optimization, adjustment for IP reuse, and migration to newer processes is high. Realize that the number of components for implementing a simplistic continuous-time bandgap is relatively low. However, the stand-alone architecture increases the difficulty in making adjustments to any subsection of the circuit without affecting the circuit as a whole. A relatively simple modification, such as increasing the supply rejection by 10 dB could prompt a

complete redesign. For the same reason, customization of a bandgap circuit is high, and makes IP reuse less viable for a range of similar temperature-related applications.

2.3.3 Discrete-time Bandgap

A discrete-time bandgap represents a different category of bandgap implementations as compared to the continuous-time bandgap reference circuit. Using a similar principle of extracting bandgap voltage, as described earlier in 2.3, a discrete-time bandgap establishes the bandgap voltage using a switched capacitor network. The generated output voltage is not continuous in time and is most often used in clocked systems. With the popularity of CMOS processes, the switched capacitor bandgap can be a good candidate to support most commercial CMOS processes. Another benefit of using a discrete-time bandgap is replacing resistors with capacitors which can generally lead to better component matching and hence, improved yield. However, the apparent disadvantage would be that such a voltage reference can not be used for biasing, which often requires a reference voltage to be present at all times. With the pros and cons of discrete-time bandgap in mind, two representatives of switched capacitor bandgap implementations were selected for review in the next section.

2.3.3.1 Switched Capacitor Bandgap by Ulmer *et. al*

Figure 5 shows the switched capacitor bandgap developed by Ulmer *et. al* [22]. The circuit uses two different-sized substrate NPN devices, along with an op-amp and switched capacitor network to generate a temperature stable voltage, V_{REF}. The operation of the circuit consists of two phases, a pre-charge phase and a valid output reference phase. Applying charge transfer and conservation, the output voltage during the valid output phase can be calculated by balancing the charge over both phases and can be written as

$$V_{REF} = V_{BE} + \Delta V_{BE} \cdot \frac{C_{34}}{C_{28}} \qquad \text{Equation 3}$$

The output voltage during the pre-charge phase is at *analog ground* for this circuit. The output waveform alternates between the two voltage levels. A non-overlapping clock generator controls the opening and closing of the CMOS switches to ensure a proper charge conservation, transfer, and redistribution.

2.3.3.2 Gilbert's Switched Capacitor Bandgap

Another important representation of a discrete-time bandgap is proposed by Gilbert *et. al* [23]. Figure 6 shows a simplified schematic of the switched capacitor bandgap. Only one diode

is used in the circuit, which is different from the previous configuration. The two different V_{BE} levels are established by injecting two ratio-sized currents into a common diode, Q_{18}. By using a single diode, the benefits can include improved matching, savings in silicon area, and much more efficient trimming.

Another major difference is the configuration of the switched capacitor network and op-amp. The op-amp is connected in a non-inverting configuration, compared to an inverting configuration in the previous circuit by Ulmer. The input common-mode voltage would then be V_{BE}, instead of *analog ground*, for easier implementation in the design. Another observable difference is the lower number of switches used and the simplified switch control signals for the switched capacitor operation. In addition, the mismatch of different switches would not contribute to the output error.

Other than the differences mentioned above, the operation of this switched capacitor bandgap is quite similar to the one by Ulmer. Using the same calculation balancing the charge from both phases, the output voltage can be written as

$$V_O = V_{BE} + \frac{C_1}{C_2} \cdot \Delta V_{BE} \qquad \text{Equation 4}$$

Both switched capacitor bandgap circuits generate a discrete-time output. This did not create a problem in its first application, an RGB-TV Encoder, where the circuit was refreshed during the line sync interval [24]. A variation of this circuit was also used in a temperature senor, as shown in Figure 7 [25].

When it is observed with as a switched capacitor bandgap, the voltage reference circuit is more modular. The sub-circuits generating bias current, PTAT, and CTAT voltage can function autonomously from the switched capacitor network. This not only enables it to be free from using a start-up circuit, but also allows the switched capacitor bandgap to be more easily modified and converted to other systems.

2.4 Analog Design in Deep Subthreshold Region

Unlike transistors in digital circuits that operate in either of two opposing states, ‘on’ and ‘off’, most devices in a given analog circuit are biased in a predetermined quiescent state to perform linear analog functions. To accomplish this, devices are biased with a known current. With the exception of a buffer and a few nonlinear circuits, the total power consumption depends

directly on the applied bias current. Therefore, in order to constrain the power consumption of analog circuits, the most effective method is to scale the bias current.

Early studies by Enz *et. al* revealed that analog circuits can still function with a bias current on the order of nA [26]. In the I_D vs. V_{GS} of the MOS transistor characteristics, this level of current corresponds to a V_{GS} of lower than device threshold voltage V_T [27], and was named the subthreshold region. When a transistor is biased with such a low level of current, the channel underneath the gate is weakly inverted, as compared to strong inversion when V_{GS} is larger than V_T. "Weak inversion" is also used to describe this operation region.

In the following sections, the device characteristics of weak inversion are reviewed. On the flip side of a low bias current and low power, weak inversion design trade-offs are also discussed. Towards the end of this chapter, a selected range of circuits using weak inversion designs are reviewed.

2.4.1 Weak Inversion Device Characteristics

2.4.1.1 Large-signal Characteristics

As the name suggests, the channel underneath the MOSFET (metal-oxide semiconductor field-effect transistor) device in weak inversion is weakly inverted. There is virtually zero potential across the horizontal locations along the channel, and therefore, the current through the channel is caused by diffusion. Figure 8 adapted from [28] shows the I_D-V_G characteristics from weak to strong inversion. In weak inversion, the drain current is exponential to the voltage applied on the gate-source terminals, written as

$$I_D = I_S \cdot \exp\left(\frac{V_{GS} - V_T}{nU_T}\right) \qquad \text{Equation 5}$$

where I_S is the specific current for the device, V_T is the threshold voltage, U_T is the thermal voltage, and n is the ideality factor.

2.4.1.2 Small-signal Characteristics

From the large-signal I_D-V_{GS} characteristics, its small-signal transconductance can be derived

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial\left[I_S \cdot \exp\left(\frac{V_{GS}-V_T}{nU_T}\right)\right]}{\partial V_{GS}} = \frac{1}{nV_T}\left[I_S \cdot \exp\left(\frac{V_{GS}-V_T}{nU_T}\right)\right] = \frac{I_D}{nU_T} \qquad \text{Equation 6}$$

The g_m of the weak inversion MOSFET is almost identical to that of a BJT device, except for the additional ideality factor n. The ideality factor n can range from 1 to 2, depending on the level of the drain current I_D. Also, the g_m of the weak inversion MOSFET is independent of the device sizing, in contrast to the case for strong inversion.

To constrain power consumption, a significant portion of MOSFET devices within the proposed circuit are biased with tens of nA currents. Even though the MOSFET in a weak inversion has higher transconductance efficiency, g_m/I_D, than that of strong inversion, the effective g_m with such a low I_D is much lower. Performance tradeoffs associated with lower g_m include lower bandwidth, slew rate, and smaller intrinsic transition frequency, f_T.

2.4.1.3 Device Matching

Device matching is an important aspect of analog design. In many cases, matching affects circuit performance so profoundly that it determines some key accuracy specifications. For low power analog design, the percentage error caused by mismatch is larger and the impact previously affecting accuracy could now jeopardize functionality. For example, Monte-Carlo simulation shows cascode current mirror errors due to mismatch were as high as 300 % for weak inversion operation. Normally, the error would be in the range of 30 % to 50 % with the same design in a strong inversion.

Generally, mismatch is categorized into a systematic or random mismatch. Systematic mismatch is more dependent on unbalanced circuit architecture or biasing and can generally be minimized by design. In low-power design, mismatch caused by an unbalanced configuration should be minimized.

On the other hand, random mismatch is mainly caused by variations due to the process. The major physical properties linked to random mismatch are threshold voltage, mobility, and body effect parameter [29]. The variations of all the three major components of random variation remain inversely proportional to the gate area. Using the EKV model equation of threshold voltage with a mismatch adjustment as an example [30] , the threshold voltage of a long-channel device, including the mismatch component, can be written as

$$VTO_a = VTO + \frac{AVTO}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_{eff}}} \qquad \text{Equation 7}$$

where *VTO* is the threshold voltage, *AVTO* is the area related to the threshold voltage mismatch parameter, *NP* is the number of devices in parallel, *NS* is the number of devices in series, and W_{eff} and L_{eff} are the effective channel width and length.

2.4.1.4 Device Leakage

Leakage current is not generally a serious consideration for analog designs. However, for low-power circuits where the leakage is a much higher percentage of the quiescent current, the device leakage could very likely cause detrimental effects to normal operation. For switched capacitor networks where the charge conservation is critical to its accuracy, taking leakage into the design consideration is critical.

Multiple components of leakage exist that are taken into consideration for this work. One of the main leakage components, subthreshold leakage (I_{SUBTH}), refers to the drain-source current that occurs when the device is turned off. It is size and bias dependent, and can be written as

$$I_{SUBTH} = \mu \cdot C_{OX} \cdot \frac{W}{L} \cdot U_T^2 \cdot \exp\left(\frac{V_{GS} - V_{TH}}{nU_T}\right)\left[1 - \exp\left(-\frac{V_{DS}}{U_t}\right)\right] \qquad \text{Equation 8}$$

where μ is mobility, C_{OX} is unit gate oxide capacitance, and both are constants for a given process. *W/L* is the device aspect ratio, U_T is the thermal voltage, and V_{TH} is the threshold voltage.

Another important type of leakage is junction leakage (I_J), which refers to the current through any reversed-bias *p-n* junctions, or simply

$$I_J = I_S \cdot \exp\left(\frac{V_D}{U_T}\right) \qquad \text{Equation 9}$$

where I_s is the reverse saturation current and V_D is the voltage across reverse-bias junction. Note that the junction leakage increases rapidly as the temperature rises. This is caused by I_S being proportional to the square of the intrinsic carrier concentration, n_i, which has a strong temperature dependency [31]. The most commonly used model, Berkeley Short-channel IGFET Model (BSIM3), includes support for subthreshold and junction leakage [32].

For deep sub-micron feature-size processes, leakage due to gate-induced-drain leakage (I_{GIDL}) and gate tunneling (I_G) are more significant and can not be neglected [33]. Both of these leakage components are difficult to model and were newly included in the BSIM4 model [34].

As most leakage components have a strong temperature dependency, sufficiently modeling leakage temperature sensitivity is extremely important for reference circuit design. As the device model development is almost always slower than process development, it is a mitigated risk to choose a larger feature-size process where the leakage component with an insufficient model support represents a smaller percentage error.

2.4.2 Low Power Circuits

2.4.2.1 Low Power Current Reference by Vittoz

One of the circuits utilizing weak inversion operation is a current reference by Vittoz [35]. The schematic of the circuit is shown in Figure 9. The transistors T_1 and T_3 are different sizes, but both operate in a weak inversion. The current is generated by the voltage V_R across resistor R, where voltage V_R is the difference of V_{GS} between T_1 and T_3, which can be simplified as

$$V_R = U_T \ln\left(\frac{S_3}{S_1}\frac{S_2}{S_4}\right) \qquad \text{Equation 10}$$

where U_T is the thermal voltage, and S_1 through S_4 is the effective W/L ratio of transistors T_1 to T_4. Realize that the voltage V_R is PTAT, and therefore the established current would be near-PTAT if the TC (temperature coefficient) of the resistor is small.

The beauty of the circuit is manifested by its simplicity. The circuit core has only 5 transistors and one passive device, which minimizes variation by reducing the total number of contributing sources. Except for the resistor R, the PTAT voltage is only dependent on device ratios, which can be well controlled. As discussed in earlier sections, establishing a well-behaved current has a particular significance in analog design. A derivative of the current reference was adapted in this effort and will be discussed further in later chapters.

2.4.2.2 Low-Voltage Cascode Bias by Minch

As discussed earlier, analog circuitry relies heavily on proper biasing. When the voltage headroom is constrained, true in many cases with a heavily scaled process having deep sub-micron feature size and low supply voltage, the low-voltage bias technique is introduced to the cascode structure to maximize output impedance and voltage swing.

The Minch cascode bias cell is shown in Figure 10 [36]. By sizing the current ratio *n* between the top-most P-type MOSFETs, and the device size ratio *m* of the middle two N-type MOSFETs, the degree of inversion of the bottom device can be written as

$$\frac{I_F}{I_R} = 1 + m(1+n) \qquad \text{Equation 11}$$

where I_F is the forward current and I_R is the reverse current. When this ratio is much larger than 1, the bottom device is considered to be in saturation. The gate voltage of the bottom device, V_G, is established using the ratios *m* and *n*. The cascode bias, V_{cn}, is one V_{GS} voltage above V_G, and thus maintains the cascode structure for saturation operation with minimum voltage headroom. V_{cn} can readily be used to bias a cascade tail current source.

Realize that the degree of saturation, defined by I_F/I_R, only depends on device size ratios, therefore the circuit can work over a wide range of currents. It was shown in [36] that the saturation current level ranges from 100 pA to 1 mA, fully demonstrating its potential for low power applications.

2.4.2.3 Nanopower Voltage Reference

A few recent publications [37] [38] [39] exist on nanopower voltage references. The operation of the nanopower bandgap can be understood from Figure 11. The current generator uses a similar principle to generate a low-level current, as shown previously in section 2.4.2.1 [35]. The reference voltage V_{REF} is generated by injecting current, MI_0, into R_1, R_2, M_7 and M_8, written as

$$V_{REF} = \left(1 + \frac{R_1}{R_2}\right) V_{GS8} - V_{GS7}\,. \qquad \text{Equation 12}$$

Note that with proper design, the TC of M_7 and M_8 cancel out and yield a zero-TC voltage reference. In later revisions, the passive resistors R_1 and R_2 are replaced with an all-transistor implementation, as shown in [38]. And further, in [39], shown in Figure 12, the current generator plays a larger role in canceling the TC of the final voltage, which can be written as

$$V_{REF} = V_{th0} + \frac{nU_T}{\sqrt{S_4/S_2} - 1}\sqrt{\frac{S_4}{S_{10}}}\ln\left(\frac{S_3}{S_1}\right) \qquad \text{Equation 13}$$

where *n* is the subthreshold slope factor and S_1 to S_4 are the effective W/L ratio of the transistors M_1 to M_4.

It is acknowledged that the series of recently published low-power voltage references by S. De Vita *et. al* pushed this research to the apex of the nanopower regime. Similar circuit concepts can be found in [40], [41], and [42].

2.5 Conclusion

Chapter 2 reviews the prior art that sets the foundation for this work. It is clear that voltage references comprise a broad category of circuits for use in a wide range of applications. The goal of this work is to focus on low-power analog while aiming for a wide range of applications. The second section reviewed the various classical bandgap architectures that are the primary foundation for this work. The potential of the discrete-time bandgap reference is also discussed. In the last section, aspects of weak inversion analog design are reviewed, as well as a few unique circuits that either find their way into this work or are sufficiently novel for the purpose of comparison. In the next chapter, the design of a low-power switched capacitor bandgap will be discussed in detailed.

Chapter 3 DESIGN OF LOW-POWER SWITCHED CAPACITOR BANDGAP

3.1 Overview

3.1.1 Selecting Circuit Architecture

The goal of this effort is to design a low power voltage reference system that encompasses key analog features and is versatile enough to accommodate different applications. Among the different implementations of bandgap voltage reference previously reviewed, the switched capacitor bandgap architecture is the most suitable. Its modularity not only allows implementing and optimizing sub-circuits individually, but is also the most easy to readapt for other applications.

The sub-circuits comprising the system include a bandgap core, current generator, clock generator, and trimming circuitry, shown in Figure 13. As mentioned earlier, a discrete-time bandgap delivers a discrete-time voltage output that is suitable for most clock-driven systems. Furthermore, in order to expand on the potential applications of this effort, an integrated track-hold device can be added to offer the system the capability of generating a continuous-time output.

3.1.2 Process Information

Available to this project is a 0.35-μm linear Bi-CMOS process from Texas Instruments. The 3 different CMOS devices, available with different gate oxide thicknesses, work with 3-V, 5-V, and 7-V supplies. For each gate oxide device, different options of threshold adjustments are available for standard and low threshold voltage. In order to use the circuit in wide number of applications, 7-V oxide devices were chosen. And due to the low-power requirement of this work, a standard threshold device was chosen over low threshold devices.

Other devices used in the design include a bipolar NPN, a poly capacitor, and a poly resistor. On occasions where accuracy is more important, a poly1-poly2 capacitor and a low-sheet resistivity poly resistor were chosen because of their lower temperature and voltage coefficient. In other instances, components that are the most area efficient are generally preferred.

3.1.3 Design Procedure

A ground-up approach was used to design this low-power voltage reference system. The design starts from the very bottom, or with transistor characteristics, to promote an understanding of how weak inversion affects circuit operations. After that, common analog sub-circuits with a nA-bias were designed before moving into the more complicated sub-circuits that comprise the system. Various design challenges are presented during this process, among which are performance tradeoffs due to low bias current and the limitations of conventional circuit topologies are revealed. To meet specifications, some unique circuits are tailored for this application and detailed in this chapter. Other sub-circuits will be shown for completeness in the appendix. Finally, the system is assembled and optimizations are completed.

In the following sections, the discussion will follow the ground-up design procedure.

3.2 Device Level Consideration

3.2.1 BSIM3 for Weak Inversion Analog Design

Circuit simulations were extensively utilized in every phase of this effort. To ensure the correct prediction of the pre-silicon simulation, model validity and limitations need to be reviewed. Specifically, the review is to verify whether the weak inversion, or subthreshold operation, is sufficiently covered by the vendor provided BSIM3 model. Included are two aspects: to verify the BSIM3 equation set models subthreshold operation and to verify device subthreshold region was sufficiently covered in parameter extraction.

The BSIM3 model does reasonably well for subthreshold operation. BSIM3 models the strong inversion and subthreshold region with different equations and uses a single smoothing function to generate continuous I-V and C-V characteristics [43]. Using the single equation smoothing function improves the numerical robustness of the BSIM3. However, one of the drawbacks is a compromised accuracy at the intermediate region between strong inversion and subthreshold regions [44], often referred to as the moderate inversion region. For the targeted deep subthreshold region, it was shown how well BSIM3 can perform [45] [46], given that the parameter fitting is done at such a low level current region. For this effort, most devices are biased with a very low current (10s of nA), and hence, using BSIM3 provides relatively good model support.

Besides using BSIM3 to support the circuit simulation, the EKV model is used to assist with the design in this work. The EKV model is a charge-based MOSFET model motivated by a

low-power effort in developing the first electronic wristwatch by The Horological Electronics Center or Centre Electronique Horloger (CEH) [47]. Because the EKV was originally tailored for weak inversion operation and the model parameters and equation set were chosen carefully to be concise, EKV equations [30] are used for some hand calculations and analysis in the design process.

The second aspect of verifying the model is equally important, since simulation accuracy ultimately relies on an accurate parameter fitting when generating the model. Attention should be given especially to models from a process that targets predominantly digital applications, in which the case digitally-oriented models can be justified in trading minimal accuracy for simulation speed. In such a case, it is best to extract key device parameters from the characterization data to ensure the accuracy of the subthreshold operation. Some useful extraction procedures can be found in [46].

In this effort, choosing an analog-oriented process simplifies the verification of the device model, or skipping the parameter extraction. However, it is still important to verify key process parameters with hand calculations and simulation results to identify model weakness and to help exercise judgment in interpreting the simulation results.

3.2.2 Hand Calculation

Based on the subthreshold current equation, shown below in Equation 14, the subthreshold slope factor n and saturation current I_s can be extracted from the simulation and compared with the value provided in the manual process extraction.

$$I_D = I_S \cdot \exp\left(\frac{V_{GS} - V_T}{nU_T}\right). \qquad \text{Equation 14}$$

First, use a long channel NMOS device to extract n from its I_D vs. V_{GS} characteristics. Figure 14 shows the linear relationship of the drain current to its gate-to-source voltage in logarithmic scale. Taking two points from the linear portion of the graph (V_{GS} < 0.5 V in this case), the subthreshold slope factor n can be calculated as

$$n = \frac{V_{GS2} - V_{GS1}}{U_T \cdot \ln(I_2 / I_1)}. \qquad \text{Equation 15}$$

The n calculated is between 1.7 and 1.9, or close to n ≈ 2 where recombination dominates with a very low forward-bias voltage [47]. The corresponding subthreshold slope is approximately 90

mV/dec, which is within the boundary defined in the process manual. Also shown in Figure 14 is a fitted curve with the I_D vs. V_{GS} characteristic, expressed below as

$$I_D = 1.5nA \cdot \exp\left(\frac{V_{GS} - 0.5}{1.6\,U_T}\right). \qquad \text{Equation 16}$$

In a weak inversion, the device transconductance, g_m, depends on the drain current and the subthreshold slope factor, n, as shown in Equation 17, which can be readily calculated once n is known.

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{I_D}{n \cdot U_T}. \qquad \text{Equation 17}$$

Worth noting is that the transconductance efficiency (g_m/I_D) of a weak inversion device is close to that of a BJT device except for the factor n. However, with the very low level current in this effort, on the order of 10s of nA, g_m turned out to be very low. To quantify the difference, with a bias current of 20 nA, the g_m of this long-channel device is approximately 460 nS, or 460 A/V. This is approximately 20X-50X smaller than when the same device is in moderate to strong inversion, biased with a 1 μA to 5 μA current. The direct impact of a lower g_m is slower speed and lower bandwidth.

Output impedance is another important parameter that can be estimated by hand calculation, and is used to first guess single-stage voltage gain by multiplying g_m with g_{ds}, or output impedance. The simplified equation of g_{ds} as a function of bias current is written as

$$g_{ds} = \lambda \cdot I_D \qquad \text{Equation 18}$$

where λ is the channel length modulation parameter, and is defined as the variation of the depletion layer length under the gate oxide as a function of drain-to-source voltage, or

$$\lambda = \frac{1}{L_{eff}} \cdot \frac{dX_{dl}}{dV_{DS}}. \qquad \text{Equation 19}$$

Observed at the weak inversion region, λ of the unit length is estimated as 0.2 V^{-1}, which is close to 2X the value for strong inversion. The lower drain current associated with weak inversion operation decreases g_{ds} which helps offset some of the single-stage voltage gain loss.

Another characteristic affecting the design is the unity-gain frequency (f_T) that determines the useful upper limit frequency of a given device, expressed as

$$f_T = \frac{g_m}{2\pi C} = \frac{I_{DS}}{nU_T}\frac{1}{2\pi C} \qquad \text{Equation 20}$$

where C is the gate-source capacitance. With 20 nA of bias current and a capacitance of 0.2 pF from an input device sized based on matching considerations, f_T is calculated to be around 370 kHz. For occasions that require handling faster signals, additional bias current and/or a smaller-size device would be needed.

The device characteristics obtained with hand calculations help establish design boundaries and better assist the design decisions. Besides nominal values, boundary values were calculated based on simulation, shown in Table 1.

3.3 Sub-circuits Design

3.3.1 Single Gain Stage

The single gain stage, including the common-source, common-drain, and common-gate amplifier, remains essential in low power design. Figure 15 is a common-source stage. Design equations deriving voltage gain and input and output impedance remain unchanged. To keep the discussion concise, key results are given below with the intermediate derivation omitted. The voltage gain can be written as

$$A_V = \frac{g_{mN1}}{g_{dsN1} + g_{dsP1}} \qquad \text{Equation 21}$$

Where the numerator g_{mN1} is the transconductance of input device N_1, and the denominator is the impedance at V_{OUT}. The unity-gain frequency is determined by g_{mN1} and the parasitic capacitance at V_{OUT}, or

$$\omega_u = \frac{g_{mN1}}{C_{par}}. \qquad \text{Equation 22}$$

The thermal and 1/f drain current noise of the input device can be written as [28]:

$$i^2 = \frac{8}{3} \cdot kT \cdot g_m \cdot \Delta f \qquad \text{Equation 23}$$

and

$$i_f^2 = \frac{K_F \cdot I_D}{L^2} \cdot \frac{\Delta f}{f} \,. \qquad \text{Equation 24}$$

In terms of the circuit performance, a reduced bias current impacts large-signal performance more than small-signal. Biasing with nA-level vs. μA-level bias current, voltage gain drops around 10 % depending on sizing, and is not too detrimental to performance. Large signal characteristics take a larger toll with low current bias, and it directly follows the linear relationship shown below

$$\Delta T = C_{par} \cdot \frac{\Delta V}{I} \qquad \text{Equation 25}$$

where ΔT represents the time required to charge or discharge node capacitance C_{par} for an associated node voltage swing ΔV, given bias current I. The direct result is a slew rate reduction by 100X or more. Further, the slew rate of the rising and falling edge becomes extremely asymmetrical. With a pMOS current source, its rising edge is much slower than its falling edge, and vice versa with an nMOS current source biasing a pMOS common-source amplifier.

3.3.2 Current Mirror

The current mirror is another universal analog cell design. It is used to replicate current, amplify signal in the current domain, and serve as an active load. Assuming the current mirror is properly sized for matching and no offset is introduced in the layout, the residue mismatch can be traced to random mismatch or any systematic offset. The former refers to errors contributed by an inherent unbalance in circuit topology or voltage. The latter refers to errors due to the inevitable process variation introduced during manufacturing that causes mismatch between otherwise identical devices.

Matching in a weak inversion operation is worse when compared to strong inversion operation. To quantify such a difference, the percentage mismatch of either case is compared. The current mismatch in weak inversion can be written as

$$\frac{\Delta I}{\bar{I}} = \frac{I_{D1} - I_{D2}}{0.5 \times \left(I_{D1} + I_{D2}\right)} = 2 \times \left| \frac{1 - \exp\left(\Delta V_T / nU_T \right)}{1 + \exp\left(\Delta V_T / nU_T \right)} \right| \cong \left| 1 - \exp\left(\Delta V_T / nU_T \right) \right| \qquad \text{Equation 26}$$

where ΔV_T refers to the variation in threshold voltage. Likewise, the current mismatch in strong inversion can be written as

$$\frac{\Delta I}{\bar{I}} \cong \frac{2\Delta V_T}{V_{GS} - V_T}. \qquad \text{Equation 27}$$

Because the threshold difference is introduced during the manufacturing process, it is safe to assume ΔV_T does not depend on whether the device operates in strong or weak inversion. Figure 16 shows the percentage of current mismatch as a function of threshold mismatch. A fixed gate overdrive is used for the comparison, where V_{GS}-V_T is 0.5 V. With a ΔV_T of 1 mV for both cases, the percentage error for weak inversion would be approximately 3 % to 5 %, while with strong inversion the percentage error could well be less than 0.5 %. The smaller the threshold mismatch, the more narrow the gap is between a weak and strong inversion. Unfortunately, threshold mismatch can not be reduced much below 1 mV, without resorting to an elaborate layout technique and increased gate area, pointed out in Equation 7. This translates to a percentage error of 10X or more when operating in a weak inversion. Also, realize in strong inversion the percentage error can be affected by varying the gate overdrive, represented by the denominator. However, for weak inversion, this means of reducing error is not effective.

With g_m being so much lower with a nA-bias, the impact of current mismatch is more profound than an equivalent voltage mismatch would be in weak inversion operation. Therefore, an iterative effort is needed to find a satisfactory design trade-off between mismatch, parasitic capacitance, and area. A statistical design tool, or Monte-Carlo simulation, becomes *the* most effective design tool to optimize the circuit and avoid over or under design.

Even with the design technique described here applied, some residue mismatch will remain. Where matching is critical, trimming circuits can be added. Also, dummy and spare devices are generously added in the layout in case the circuits need to be revised.

3.3.3 Biasing

Most devices within an analog circuit are biased in a quiescent state. With a limited supply voltage available, only by careful selection of the biasing scheme can the limited voltage headroom be fully optimized for performance gain. Additional design challenges also come with weak inversion operation.

Because of the exponential current-voltage relationship of the subthreshold operation, conventional bias techniques need to be re-examined. The most common, stacked diode-

connected biasing, remains applicable in a weak-inversion design, as shown in Figure 17. The penalty for using this biasing scheme is a higher voltage headroom requirement and more systematic offset. To better utilize voltage headroom, a low-voltage cascode current mirror is commonly used. Figure 18 shows an implementation of a low voltage cascode current mirror whose cascode transistor is biased with a diode-connected MOSFET. However, this biasing technique is based on a strong inversion square-law operation and is not suitable for weak inversion. In a strong inversion, the voltage across a MOS-diode using the square-law equation is

$$V_{GS\_SI} = \sqrt{\frac{2I_D}{\mu C_{OX}}\frac{L}{W}} + V_{TH} \,. \qquad \text{Equation 28}$$

Here V_{GS} is a rather strong function of the MOS-diode aspect ratio, or *L/W*. In the case of weak inversion, the V_{GS} across a MOS-diode is

$$V_{GS\_WI} = nU_T \ln\left(\frac{L}{W}\cdot\frac{I_D}{I_S}\right) + V_{TH} \qquad \text{Equation 29}$$

which is a much weaker function of (*L/W*). An elegant biasing scheme would use the Minch technique [36]. Figure 19 shows the implementation of biasing an N-type, low-voltage cascode current mirror. The minimum voltage required for the output, V_X, to satisfy saturation is approximately two overdrive voltages. This biasing technique allows for explicitly aligning the degree of saturation of the mirror device, M_{N4}, with the physical device ratios, *m* and *n*. This allows better control over process corners and temperature.

The regulated cascade bias is another useful biasing scheme, as shown in Figure 20. The benefits are increased output impedance by the amplifier loop gain and a further decrease in the voltage requirement on V_X. In most instances, a single common-source amplifier will suffice for the amplifier's need. The benefit of the increased output impedance is used for a current mirror load to boost gain, or a amplifier's tail current mirror is used to enhance the common mode rejection.

3.4 Design Switched Capacitor Bandgap

3.4.1 Synopsis of Switched Capacitor Bandgap

The switched capacitor bandgap core, shown in Figure 21, applied in this effort was first shown by the author in [48]. Different than its predecessor designed by Gilbert *et. al* [23], the

current design is capable of generating a sub-1 V output with a few additional components, a capacitor, C_3, and two additional switches.

The circuit operation is similar to the discrete-time bandgap shown in 2.3.3. Two phases are involved in its operation, a pre-charge/reset phase (Φ_1) and a reference output phase (Φ_2). During the two phases, two different levels of current are injected into D_1, generating two different voltage drops used to emulate the ΔV_{BE} from two BJT-based diodes with different emitter sizes, as in a conventional BGR. With the switching operation, a PTAT voltage is generated and combined with a CTAT voltage to achieve a temperature stable voltage during Φ_2. During Φ_1, the switches S_1, S_4 are closed and S_2, S_3 are open. With the current I_1 being injected into D_1, the negative feedback action of the op-amp places voltage V_{D1} across the parallel capacitors C_1 and C_3, where V_{D1} is given by

$$V_{D1} = nU_T \ln\left(I_1/I_S\right) \qquad \text{Equation 30}$$

where U_T is the thermal voltage and n is the emission coefficient of the diode.

During Φ_2, the switches S_1, S_4 are open and S_2, S_3 are closed, and the sum of the currents I_1 and I_2 is injected into D_1. The voltage at the op-amp's minus input terminal becomes

$$V_{D2} = nU_T \ln\left[\left(I_1 + I_2\right)/I_S\right]. \qquad \text{Equation 31}$$

Alternating between these two phases, the charge stored in the capacitor, a combination of C_1 and C_3, is conserved and redistributed among C_1, C_2, and C_3. Thus, the output voltage in Φ_2 can be written as

$$V_{OUT} = \frac{C_2}{C_2 + C_3}\left[V_{BE} + \frac{C_1 + C_3}{C_2}\ln\left(\frac{I_1 + I_2}{I_1}\right)\cdot U_T\right]. \qquad \text{Equation 32}$$

Note that the sub-1-V BGR output voltage is a bandgap voltage scaled by the factor of $C_2/(C_2+C_3)$. Instead of generating a 1.2-V reference, the final output voltage can be freely chosen, depending on what the target application needs.

3.4.2 System Partition and Design Emphasis

The switched capacitor bandgap can be treated more as a system, as compared to a stand-alone circuit in the case of the continuous-time bandgap reference. The main sub-circuits include the switched capacitor bandgap core, current generator, clock generator, and trimming circuits.

Although the complexity of the switched capacitor bandgap is perceived to increase, the modular approach allows its functions, as well as performance requirements, to be divided into smaller units, and each sub-circuit can be treated systematically and independently optimized. The temperature stability is dependent on the switched capacitor bandgap core and the bias current generator, as well as the trimming circuits. The supply rejection is more dependent on the sub-regulator and op-amp. The load driving capability is associated with the output stage of the op-amp. And finally, the power consumption is dependent on each individual block.

With the sub-circuits performing different roles in the system, the design focus and challenge is different for each one. Since the switched capacitor network is the core of the system and affects system accuracy, various parameters need to be optimized. They include offset, gain, and bandwidth. With the total supply current limited, a significant portion of the supply current is directed to the op-amps to better facilitate the design goal. The current generator of this design produces a bias current on the order of 10s of nA, which immediately poses a serious design challenge. The bias current is used to bias other circuits within the system, and therefore its variation will be propagated. Silicon area is a tradeoff to contain such a variation. Another challenge is to extend the usage of the bias current across a useful temperature span, in this work – 40 °C to 100 °C, while maintaining the stable performance of the circuits being biased. Another essential focus of this work is the oscillator which drives the switched capacitor network. The design challenge of the oscillator is limiting its supply current. Being that it is a circuit that bridges the analog and digital domains, a large portion of the supply current is the short circuit current consumption that needs to be minimized.

In the next section, the design highlights of the sub-circuits mentioned above will be discussed.

3.5 Building Block Design

3.5.1 Design of Current Generator and Supply Sub-regulator

3.5.1.1 Design

Establishing a nA-level bias current is of the highest priority, not only due to the fact that the bias current is generally the foremost quantity established in analog circuits, but more importantly, it is the key to low supply current and low power. In order to limit the supply current within a few hundred nA, the bias current is targeted for a small fraction of the total supply current.

With the purpose of providing the bias current, a PTAT current is chosen over a constant current. For biasing low power circuits, and subsequently weak inversion operation, a PTAT current has the advantage of g_m remaining relatively constant over temperature:

$$g_m = \frac{I_D}{n \cdot U_T} = \frac{I_{PTAT}}{n \cdot U_T} = \frac{M \cdot U_T}{n \cdot U_T} = \frac{M}{n} \qquad \text{Equation 33}$$

where U_T is the thermal voltage, n is the subthreshold slope factor that has a weak temperature dependency, and M is a constant. The bias current is generated by establishing a ΔV_{GS} between two weak-inversion nMOS devices with different current densities across resistor R, or

$$I_{PTAT} = \frac{V_{GS1} - V_{GS2}}{R} = \frac{nU_T \ln K}{R} \qquad \text{Equation 34}$$

where K is the current density ratio [35].

The implementation depicted in Figure 22 combines a bias current generator and supply sub-regulator in one circuit. Table 2 lists the corresponding device sizes. The core of the circuit is the current generator and consists of M_{P1}, M_{P2}, M_{N1} to M_{N6}, and R. The PMOS devices M_{P1} and M_{P2} are matched, the nMOS devices M_{N1} and M_{N2}, M_{N3} and M_{N4} are matched and M_{N5}-M_{N6} have a sizing ratio of 2:1. The resistor R is 2 MΩ and converts ΔV_{GS} into the current I_B, which is approximately 20 nA at room temperature. The output current, I_{OUT}, of 10 nA can be conveniently generated as a unit bias current.

Another important feature of this circuit is its ability to reject the supply ripple coupled from digital circuits, or any other switching sources. A supply sub-regulator is designed to provide the regulated supply voltage for subsequent circuits. The supply sub-regulator consists of the devices M_{P3}, M_{P4}, and M_{N7} to M_{N12}. With the negative feedback established around M_{P5}, M_{N11}, M_{N12}, M_{N10}, and M_{P2}, V_{SUBREG} is isolated from V_{DD}. V_{SUBREG} is set to four times the V_{GS} voltage and is approximately 2.1 V at room temperature. The voltage fluctuation over temperature does not pose a negative effect for the subsequent circuits. This is due in part to the threshold voltage having a negative TC as the supply voltage and therefore, the voltage headroom has a similar temperature trend. The generated current, I_B, is reflected in the sub-regulator and subsequently amplified by M_{N11} and M_{N12} to provide a supply current for the circuits that are powered from V_{SUBREG}.

Using the approach of supply sub-regulation, the total supply rejection achieved in the low-power switched capacitor bandgap reference system would be a combination of the supply

rejection provided by the sub-regulator and the supply rejection provided by the op-amp. As the PSRR (power supply rejection ratio) of the op-amp decreases at higher frequency, the combined supply rejection is able to hold up to much higher frequency. For low-power applications where the bandwidth and the op-amp PSSR is relatively low, this approach could provide an invaluable supply rejection that would not otherwise be available.

Like all self-biasing circuits, a startup feature is essential for the circuit to be powered into a proper operating state. Extra caution is warranted since the transient startup current could be an order of magnitude higher than the nA-level quiescent current, hampering the normal circuit operation. In this design, the startup circuit consists of M_{S1}, M_{P6} to M_{P8}, M_{N13}, M_{N14}, and C_{ST}. M_{S1} powers the bias generator core by creating a direct current path from its supply rail, V_{SUBREG}, to ground. M_{P8} provides the supply current for the current generator core before I_B is stabilized and reflected to M_{N12}. After the bias circuit stabilizes, M_{P8} is turned off by the current comparator, consisting of M_{P7} and M_{N14}. Both conduct currents derived from I_B and M_{P7} overrides M_{N14} when the bias current is stabilized, indicating the circuit is powered up.

3.5.1.2 Simulations

A selected set of simulations are shown in this section to highlight key characteristics of this circuit.

The generated bias current, I_{OUT}, increases with the temperature, while the voltage, V_{SUBREG}, has an opposite trend. Figure 23 shows I_{OUT} and V_{SUBREG} from –40 °C to 120 °C, with temperature steps of 1 °C. The data is extracted from a DC sweep, with a *typical* process model used as the default.

With process variation in mind, Monte-Carlo simulations were run to assist with design decisions in trading off the silicon area with the process variation. The device sizes shown in Table 2 are a product of this iterative process. To sufficiently account for multiple contributors of process variation, 100 simulations were conducted with each process parameter randomly varied according to its respective, often normal, distribution, and to determine its statistical behavior characterized by the mean and variation. Because of the volume of data generated from the Monte-Carlo simulations, the output current is characterized at three temperatures, –40 °C, 25 °C, and 125 °C. The temperatures in-between can be extrapolated. With the result following a normal distribution, the mean of the output current and four times the variation, +/– 4σ, are plotted in Figure 24. With a +/– 4σ symmetric confidence internal, 99.993666% of the output current falls within the drawn boundary.

To verify startup, transient simulations were run with a combination of different supply ramp rates, process corner models, and temperatures. Figure 25 shows the I_{OUT} and V_{SUBREG} while ramping up the supply voltage from 0 V to 5 V in 1 msec, with the three process-temperature corners. The nominal corner is at 25 °C, the strong corner is at –40 °C, and the weak corner is at 125 °C.

The power supply rejection (PSR) on V_{SUBREG} is simulated and shown in Figure 26. The PSR at DC is close to –60 dB.

3.5.1.3 Layout

The layout of the current generator is shown in Figure 27. The drawn dimensions are 225 µm by 255 µm. The 2 MΩ poly resistor converting voltage to current and mirror devices providing the supply current for the V_{SUBREG} rail are the largest devices in the layout. Current mirrors are placed compactly in the center of the layout and carefully arranged in a common-centroid manner as an attempt to minimize the impact due to process gradient.

3.5.2 Op-amp

3.5.2.1 Design

As previously shown in Figure 13, two amplifiers are used in this switched capacitor bandgap system. The amplifier in the switched capacitor bandgap core does not require an output stage, and therefore, can be an operational transconductance amplifier, or OTA. However, the amplifier in the track-and-hold block needs a low impedance output stage.

Figure 28 shows the simplified schematic of the OTA and device sizing information is included in Table 3. The input stage uses pMOS to accommodate the low input common-mode voltage. The differential input stage, M_{P5} and M_{P6}, is folded into the low-voltage regulated-cascode current mirror, M_{N1} to M_{N4} and M_{P1} to M_{P4}. The amplifiers, G_1 and G_2, are used to boost output impedance and can be implemented simply with a simple common-source amplifier, where G_1 is equivalent to I_{B1} and M_{P7}, and G_2 is equivalent to I_{B2} and M_{N5}. Boosting the output impedance is useful in maintaining voltage gain in the presence of degrading g_m with very low bias current, which minimizes errors in the switched capacitor network.

Figure 29 shows the implementation of the tail current source (depicted as I_{TAIL} in Figure 28). It utilizes a regulated cascode biasing technique, previously mentioned in 3.3.3, for better current matching and a lower voltage headroom requirement. Table 4 shows the sizing. Note that M_{P5} is much smaller in size than M_{P2}. As it turns out, the output impedance is not compromised. In the meantime, the parasitic capacitance seen at the output is reduced by

shielding M_{P11}. Although the main use of this circuit is preserving the voltage headroom, minimizing the parasitic capacitance can be useful in other scenarios.

Another challenge to using a low-power design and subsequently a low bias current, is a much higher channel impedance now compromises the signal path. With a very low bias current, 10 nA to 100 nA in this work, the direct result would be a pole locations several decades lower in frequency, which seriously degrades the signal bandwidth and complicates stability.

In this work, a low output impedance source follower is used for driving the resistive load. Figure 30 shows a simplified schematic of a source follower that can be used as a low-impedance buffer. The device, $M_{F,}$ is the main follower, with its gate being the input and its source being its output. The effective output impedance observed at V_{OUT} is reduced from $1/g_{mF}$ to $1/g_{mF}$ divided by the loop gain established around M_F, M_3, and M_D [49] [50].

Figure 31 shows a full schematic of a low-Z_{OUT} buffer using this technique. The device sizing is shown in Table 5. Likewise, the device, $M_{F,}$ is the source follower device and the negative feedback loop is established with M_F, M_{P16}, and M_{N10}. The device M_{P15} serves as a regulated cascode amplifier that boosts the impedance on node P. The closed-loop output impedance on V_{OUT} is reduced by the loop gain, and is written as

$$Z_{O\_CL} = \frac{Z_{O\_OL}}{1 + A\beta} = \frac{1/g_{mF}}{1 + g_{mN10} r_{oP}} \qquad \text{Equation 35}$$

where g_{mN1} is the transconductance of M_{N10} and r_{oP} is the small-signal resistance at node P. The device M_{P17} supplies the current that is delivered to the output load, shielding M_F and other devices in the feedback loop from the loading effects. The output range of the buffer is roughly between $V_{GSN}+V_{DSAT}$ to $V_{DD}-V_{GSP}-V_{DSAT}$.

3.5.2.2 Simulation

First, compare the regulated-cascode tail current source to a simple current mirror, in terms of output impedance and output headroom requirement. The simple current mirror is sized to the same dimensions as the mirror devices in the regulated-cascode version, equivalent to M_{P10} and M_{P11} in Figure 29, or 16/8 and 160/8. Figure 32 shows the output current of both current sources with gradual decreasing voltage headroom. Clearly, the regulated-cascode version has an undisputed advantage over the simple current mirror.

With the OTA as the center of the switched capacitor network, its stability is evaluated. With a 2-pF capacitor at the output, the OTA is unconditionally stable. Figure 33 is the Bode plot indicating an open-loop gain of 99.1 dB near DC, a gain-bandwidth product (BW) of 59 kHz, and

a phase margin (PM) is 84°. Figure 34 shows the output of the OTA in a unity-gain, non-inverting configuration responding to a small-signal step response, from 0.5 V to 0.6 V.

With the output stage added, the stability of the op-amp is very similar to that of the OTA. Since the op-amp is not directly driving the external load, the load capacitor of 1 pF is added to the op-amp output. Stability simulations were run with the three process and temperature corners, including 25 °C with the nominal corner, 125 °C with the weak corner, and –40 °C with the strong corner. The open-loop gains and phases for the three cases are shown in Figure 35. At 25 °C with the nominal corner, the PM is 74° and the gain margin (GM) is –23 dB; at 125 °C with the weak corner, the PM is 78° and the GM is –23 dB; and at –40 °C with the strong corner, the PM is 66° and the GM is –22 dB.

The PSRR and CMRR of the op-amp are also characterized, as shown in Figure 36 and Figure 37, respectively.

The output impedance of the buffer is characterized as a stand-alone circuit to verify the hand calculated estimate. The simulation applies an AC current source at the output and derives the output impedance as a quotient of the output voltage and output current over frequency. The result is shown in Figure 38. At DC the effective resistance is 12.5 Ω, which agrees well with the hand calculation estimate.

The simulation estimates that $1/g_{mF}$ is approximately 230 kΩ, which is divided by a loop gain of 17,900 to provide a Z_{OUT} of 12.6 Ω at DC. When the output stage is embedded into the op-amp (OTA followed by low Z_{OUT} buffer), the closed-loop output impedance is further divided by the voltage gain of the OTA. Figure 39 shows the simulation result of the op-amp's closed-loop output impedance, which indicates 0.25 mΩ at DC.

3.5.2.3 Layout

The layout of the low power op-amp is shown in Figure 40. The drawn size is 210 µm by 160 µm. The PMOS device, $M_{P17,}$ supplies the output current and is the largest device within the layout. Matched devices are laid out in a common-centroid configuration to cancel out part of the process gradient. Dummy devices are placed on both ends of the diffusion to shield active devices from inconsistent diffusion-doping concentration and mechanical stress. To shield from substrate noise and collect the injection due to switching, guard rings were also generously added. The capacitors in the layout are used for compensation purposes. They are flexibly shaped and placed on the periphery for an overall rectangular-shaped layout.

3.5.3 Oscillator

3.5.3.1 Design

The operation of the switched capacitor network requires a clock. Generating an on-chip clock using an oscillator is preferred over driving the IC with an off-chip clock signal, since the switched capacitor bandgap system would function as a stand-alone unit and be fully integrated. The generated clock will feed the switch drivers to further generate multiple non-overlapping clocks to drive the switches in the circuit. Given that only a few hundred nA of supply current are budgeted for the oscillator, extra caution is taken with the design to meet functionality while trading off little power or area.

During the oscillator operation, the internal multi-vibration is converted to the digital output, '0' or '1'. The short circuit current consumed during this translation is minimized by design in the presence of a severe slew rate limitation. Meanwhile, because the circuits driven by this clock have a low bandwidth, the oscillator frequency targeted needs be very low.

Figure 41 shows the design of the oscillator, consisting of a dual-slope ramp generator, two comparators, and a few logic gates. A fixed current, I_{BIAS}, is integrated and de-integrated on the capacitor, C_R, to generate a triangle ramp. The comparators trip when the ramp, V_R, crosses either the high-side threshold, V_{REF_HI}, or the low-side threshold, V_{REF_LO}. The output of either comparator is latched to generate the oscillator output, CLK_{OUT}.

To minimize the short circuit current (between V_{DD} and ground), an AND-OR latch is used to latch only the fast edges of either of the comparators. The OR-gate latches the output of the nMOS-input comparator, I_{CMP_N}, that has fast rising edges, and the AND-gate latches the output of the pMOS-input comparator, I_{CMP_P}, that has fast falling edges. V_{REF_LO} and V_{REF_HI} are established by directing current into two matched pMOS diodes, M_{P6} and M_{P7}, off either of the supply rails. By using identical pMOS diodes and matching the current source and sink, the output clock duty cycle will be very close to 50 %.

3.5.3.2 Simulation

To better understand the oscillator circuit operation, a transient simulation result is shown in Figure 42 including the oscillator internal nodes. The first strip shows where the triangle ramp, $V_{R,}$ crosses the reference voltages V_{REF_LO} and V_{REF_HI}. In the second and third strips, the comparator outputs, V_{CMP_N} and V_{CMP_P}, are shown. The severe slew limitation on either edge is very noticeable in the graph. Finally, the bottom strip shows the generated clock signal from the AND-OR latch and its subsequent driver.

To show the effectiveness of minimizing the total current consumption, the average supply current is extracted from three transient simulations over the –25 °C and 125 °C span, with nominal, strong, and weak process corners. From Figure 43 it is estimated that the supply current would be approximately 100 nA. From this 100 nA supply current, 80 nA is attributed to static current, leaving merely 20 nA to be dissipated by the short circuit current draw and switching loss.

With the frequency of the oscillator being a strong function of the bias current, the oscillator output frequency is captured when biased with both a constant current and an ideal PTAT current with a temperature exponent of 1. Figure 44 shows the simulation result from –25 °C to 125 °C, in 25 °C steps. Note that when the oscillator is biased with the constant and PTAT current, it yields opposite trends with respect to temperature. The generated bias current is closer to PTAT, and the oscillator frequency temperature characteristics increase over temperature.

The oscillator frequency variation is characterized by Monte-Carlo simulation at –40 °C, 25 °C, and 125 °C. The mean and 4σ boundary of the oscillator is shown in Figure 45.

3.5.3.3 Layout

Figure 46 shows the layout of the oscillator. The oscillator drawn size is 70 μm by 100 μm, and the size of the 2.7-pF capacitor is 55 μm by 68 μm. For the oscillator, the current mirrors, comparators, and a few logic gates are the main area contributors. The metal lengths of the switching nets are minimized by strategic placement, and their metal width is also minimized to reduce parasitic capacitance. The same principle applies to routing the complementary clocks for the driving switches where such nets are drawn apart to reduce parasitic capacitance. Guard rings are added to each block of diffusion as well as to the periphery of the oscillator to mitigate substrate injection due to switching.

3.5.4 Track-and-Hold

3.5.4.1 Design

The track-and-hold feature is included to generate a continuous time reference voltage based on the discrete-time output from the switched capacitor bandgap. With a limitation on the total supply current, it would be beneficial to use the same op-amp for both the track-and-hold feature and buffering the output.

Figure 47 shows an implementation that fulfills both requirements and only requires one op-amp. The circuit operation involves two phases: Φ_1 when the output tracks the input and Φ_2 when the output holds its voltage. During Φ_1, the hold capacitor, C_{hold}, is connected to the

amplifier output in a unity-gain, non-inverting configuration, and during Φ_2, the stored voltage on C_{hold} is applied to the input and drives the output terminal with the amplifier configured as a unity-gain buffer.

3.5.4.2 Simulation

Figure 48 shows a typical track-and-hold operation when applying a sinusoidal signal at the input. The top strip shows the clock signal Φ_1, and the second stripe shows the input sine-wave overlaying V_{IP}, the non-inverting input of the track-and-hold amplifier. The third stripe shows $V_{TR\_HD,}$ which is the output of the track-and-hold amplifier.

3.5.4.3 Layout

The layout of track-and-hold stage is shown in Figure 49. The drawn size is 210 µm by 215 µm. 95 % is the op-amp and hold capacitor. Care was exercised in routing the switching nets, such as the voltage input and clocks, to minimize the short circuit current draw due to parasitic capacitance.

3.6 Switched Capacitor Bandgap

3.6.1 Design

After the sub-circuits of the switched capacitor bandgap are designed, the switched capacitor bandgap core is ready for assembly. Figure 50 shows again the schematic of the switched capacitor bandgap.

One of the design decisions remaining to the circuit is the selection of the diode and bias current to be injected into the diode. There are three NPN devices with different emitter areas that are supported by this process. The drawn sizes of the three devices are 13.5 µm by 13.5 µm, 6.3 µm by 6.3 µm, and 3.3 µm by 3.3 µm. To find the most suitable device to use in the circuit, simulations were run to discern which one has I-V characteristic closest to an ideal exponential relationship. Next, sweep the V_{BE} voltage and plot the collector current, I_C, for all three sizes of the NPN device, in Figure 51. With the bias current near 10 nA, the corresponding V_{BE} voltage is approximately 0.4 V. In Figure 52 the linearity of the V_{BE} voltage is further examined by taking the derivative of $\ln(I_{CE})$. Among the three NPN devices, the NPN device with an emitter area of 6.3 µm by 6.3 µm performs the best. Using the NPN device with an emitter area of 6.3 µm by 6.3 µm, the next step is to determine the level of unit current needed to generate ΔV_{BE} that is closest to the ideal PTAT. Figure 53 shows the voltage of ΔV_{BE} generated with a unit current of 10 nA, 20 nA, and 40 nA. A higher unit bias current yields better PTAT characteristics and lower shot

noise. This limits potential applications that require multiple copies of diodes, such as an integrated on-chip temperature regulation, previously discussed in 1.4. Therefore, the unit bias current of 20 nA is chosen.

The clock signal driving the switches is generated by a non-overlapping clock generator using a NAND-feedback structure, described in [51], and followed by a pseudo-differential clock driver that minimizes the clock skew between the positive and negative phases [52]. The two clock phases, Φ_1 and Φ_2, are designed to have an asymmetrical duty-cycle to maximize the reference output phase Φ_2. In this case, the circuit that generates the 25%/75%-duty clock was simply a DFF clock divider and a few logics.

Since leakage current is important in the design, ESD devices were carefully chosen to minimize such a penalty. Two types of ESD device were included to protect the IC from potential static discharge during processing, packaging, and handling. The ESD devices used on the bond pads of the IC are shown in Figure 54. Reversed-bias *pn*-diodes were chosen for due to low leakage and were connected between the bond pads to the ground current and to the supply, respectively. ESD cells were added to provide the local charge-device model (CDM) protection from the gate oxide device, as shown in Figure 55 [53].

3.6.2 Simulation

Figure 56 shows different switched driver signals driving the switched capacitor network. The signals plotted; from the top to the bottom of the strip are the clock signals out of the oscillator, clock Φ_1, the pseudo-differential drive signal, Φ_{1_P} Φ_{1_N}, clock Φ_2, and the pseudo-differential drive signals, $\Phi_{2\_P,}$ Φ_{2_N}.

The skew between the positive and negative phases is minute. Figure 57 shows the inputs and outputs of the pseudo-differential switch driver. The rise and fall time of either phase of the drive signal is approximately 1.2 nsec.

A nominal simulation of the circuit operation is shown in Figure 58. During Φ_1, the output follows the voltage of the input, V_{BE} with 20 nA of collector current. And during Φ_2, the output generates the reference voltage, or in this case, half of the bandgap voltage. Figure 59 shows the temperature characteristics of the output reference, from –40 °C to 125 °C, simulated with 9 different process corners. The temperature's characteristics depend on the capacitor ratio to help cancel the positive and negative temperature coefficient of the PTAT and CTAT component. The design is centered on the nominal process corner, where the maximum voltage

drift is expected to be less than 1.5 mV. At the worst-case corner, the voltage drift is under 4.5 mV.

Simulations with corner models help establish boundaries where the circuit will likely behave in the presence of the inevitable process variation. Knowing that variation is introduced in every step of the fabrication process; some variations affects a specific component while others may affect a group of components. The corner models supported in this process allow the customization of multiple combinations of skews of components including the resistor, capacitor, n-MOS, p-MOS, and more.

3.6.3 Layout

The temperature characteristics of the switched capacitor bandgap also largely depend on the layout, especially capacitor matching. Figure 60 shows the common centroid arrangement of the poly capacitors C_1, C_2, and C_3, surrounded by dummy capacitors to eliminate differences in the oxide between the outer and inner edges of the capacitor. The size of the dummy capacitors can be much smaller than the unit capacitors, provided one edge has the same length and they are placed the same distance from the unit capacitors as the distances between the unit capacitors.

The layout of a switched capacitor bandgap is shown in Figure 61. The total drawn is 205 μm by 255 μm. To minimize leakage current integration into the feedback capacitors C_2 and C_3, the diffusion of the OTA inverting input were carefully minimized. For this same reason, the capacitors were placed close to the OTA to specifically shorten the routing length to the OTA inverting input terminal.

3.7 Conclusion

This chapter discussed the design side; going through a step by step selection of the circuit architecture, hand calculations, sub-circuit, and finally, top level design and optimization.

The next section will explain the measurement aspects of this work; hoping to provide a different perspective by putting more emphasis on actually using the system.

Chapter 4 MEASURE LOW-POWER SWITCHED CAPACITOR BANDGAP

4.1 Introduction

This chapter presents the measurements of the low-power switched capacitor bandgap, as well as characteristics of some of the individual sub-circuits. Measurement is done on multiple silicon samples to verify the validity of the design and to expose limitations. By correlating the measurement data with the simulation, a better understanding of the circuits is expected to be achieved along with suggested steps for future work.

Besides characterizing the voltage reference, sub-circuits used in the system were characterized to build up a low-power analog cell library for later IP reuse. Sub-circuits include the op-amp, oscillator, current reference, supply sub-regulator, and track-and-hold. Besides the measured results, test setups will also be discussed in this chapter.

4.2 Test Setup

The wafers were diced into dies sized 1430 μm by 1430 μm, including an 80-μm scribe on each side of the chip. The chosen package is a 28-pin ceramic DIP (dual in-line package), and the bond wires used were 0.96 mil. Figure 62 shows the microscopic photo taken on a packaged die, with major circuits circled and designated. Figure 63 shows the bonding diagram used in conjunction with the chosen leadframe. The corresponding pin names and descriptions are listed in Table 6.

Two different test boards were made to accommodate a room temperature characterization and temperature sweep test. A room temperature board was designed with enough versatility to allow different test configurations with jumpers and test points. Figure 64 shows the 2-layer FR4 PCB board. The test configuration of the temperature board was more simplistic, and in most cases, connections are soldered to guarantee a good electrical connection at temperature extremes. Figure 65 shows the 4-layer PCB temperature board, which accommodates the 4 samples being tested, in parallel, to maximize test bandwidth.

For a room temperature test, two types of test equipment were specifically used to provide the necessary support to this work. A digital multimeter Keithley 2002 with current resolution of 10 nA was used to measure the supply current of the system. A network/gain-phase/impedance analyzer, the HP4194A, was used to characterize the supply rejection and output impedance. And finally, a spectrum analyzer, the HP3589, was used to characterize noise.

The temperature test setup uses a Delta temperature chamber (model# 9023) with a liquid nitrogen (LN_2) coolant, to cover the temperature range of –73 °C to 315 °C. The test board with a DUT (device-under-test) is placed inside the chamber with test leads through the wiring holes in the front panel connecting the test equipment.

4.3 Measure Switched Capacitor Bandgap

The designed switched capacitor bandgap can be configured to generate either a discrete-time reference or a continuous-time reference with the optional track-and-hold stage enabled or disabled. To better reveal circuit performance, either configuration was selected for evaluative tests, as described below.

4.3.1 Functional Test

The first test is to start the system and turn on the current generator and supply sub-regulator. To fully test startup behavior, the circuit supply is ramped to varying final voltages at different rates to test whether the start-up function correctly places the self-biasing current generator into the desired stable state. The bias current is not directly sent to the external current, but instead the voltage on V_{SUBREG} is monitored to observe it settling to its final voltage of approximately 2.1 V.

The voltages of V_{DD} and $V_{SUBREG,}$ captured from the two selected tests, are shown in the oscilloscope plot in Figure 66. The upper section shows the settling of V_{SUBREG} when V_{DD} is ramped from 0 V to 4 V in 20 msec. The lower section shows the case when V_{DD} is stepped up from 0 V to 4 V in 100 µsec. V_{SUBREG} settles to approximately 2.1 V when the voltage on V_{DD} is at or above 2.5 V. It can be identified when the startup pMOS M_{P8}, only temporarily *on* during startup, was later turned off by the built-in current comparator, indicated by the arrows Figure 66.

In the event of brown out conditions, or when the supply voltage drops below the level required for a normal circuit operation, it is important for the circuit have the capability to recover. The test is performed by dropping V_{DD} to 1.5 V from 4 V, well below the dropout voltage of 2.5 V at room temperature, and later, V_{DD} recovers to 4 V. Figure 67 shows the voltage on V_{SUBREG}, before, during, and after brownout conditions.

With the current generator properly started, the switched capacitor bandgap can be tested. Figure 68 shows a steady-state switching waveform of the switched capacitor bandgap, including V_{SUBREG}, discrete-time bandgap voltage V_{BG_SC}, and the clock signal. Note that V_{BG_SC} alternates between 0.51 V and 0.6 V, and has a 25%:75%-duty cycle. The glitches on V_{BG_SC} are due to the

injection of the clock signal. Figure 69 shows a continuous-time bandgap voltage with the track-and-hold feature enabled, overlapping discrete-time voltage V_{BG_SC}. The track phase and hold phase also has a 25% to 75 % duty cycle, indicated by arrows in the figure.

4.3.2 DC Line Regulation

DC line regulation measures the generated voltage's capability of rejecting a low-frequency supply ripple. The test increased the supply voltage from 3 V to 7 V and measured the output voltages at each point. Figure 70 shows V_{BG_CT} vs. V_{DD}, with V_{DD} increasing from 3 V to 7 V in 0.5 V increments. Another test is to characterize output voltage disturbance in the presence of each voltage increase on the supply. The line regulation was estimated to be approximately –62 dB, using the equation below

$$LineREG = 20 \times \log \frac{V_{O1} - V_{O2}}{V_{DD1} - V_{DD2}}. \qquad \text{Equation 36}$$

In Figure 71, the discrete output V_{BG_SC} shows a 7-mV bump due to the 1-V step on V_{DD}. The recovery time is approximately 30 µsec. The magnitude of disturbance due to the V_{DD} step is small, because a significant portion of its frequency content is filtered out at the track-and-hold stage.

4.3.3 Temperature Test

Another important aspect of the reference circuit is its capability of providing a temperature stable reference. The temperature test was conducted from –25 °C to 125 °C. However, further challenges are expected when the temperature rises above 100 °C and elevated leakage is present.

Ten chip samples were measured for the temperature test. The results of V_{BG_CT} vs. temperature are shown in Figure 72, from –25 °C to 125 °C in 25 °C steps. The bandgap output voltage falls at an increased rate above 100 °C, but prior to 100 °C the variation was much smaller. (Note the commercial temperature range is typically 0 °C to 85 °C.) Figure 73 has the 125 °C data point removed, providing a clearer picture of temperature behavior when leakage is relatively low. In the temperature range of 0 °C to 100 °C, 8 out of the 10 samples had a total variation of less than 10 mV, and 6 out of the 10 samples had less than a 5 mV variation. This is equivalent to a TC of 60 ppm/°C to 100 ppm/°C.

4.3.4 Supply Current Measurement

The total supply current of the low power switched capacitor bandgap was measured. The supply current of the whole IC is combined and measured at 25 °C, 50 °C, 75 °C, 100 °C and 125 °C by monitoring the total ground current. The supply current of the oscillator can be roughly estimated by taking the difference with the oscillator enabled and then disabled.

The supply current measurement agrees with the full chip simulation, except for an elevated leakage at higher temperatures. Figure 74 shows the total supply current with a 3-V and 6-V supply, from both the simulation and measurement. The total supply current consumption varies from 1300 nA at 25 °C to 1900 nA at 125 °C.

The simulation and measurement of the supply current agree reasonably well. This allows the current consumption break down for each circuit within the system. Figure 75 shows the supply current's consumption of the main blocks. The main supply current consumers were track-and-hold stage taking 41 % of total supply current and switched capacitor bandgap core taking 24 %. Excluded the optional track-and-hold stage, the goal of limiting supply current of the switched capacitor bandgap below 1 μA was met.

4.3.5 Noise Measurement

Noise is both unwanted, and inevitable, in almost all electronics. In the case of the reference circuit design, noise can be an important detail, which could affect the accuracy of subsequent circuits within a system.

Generally, an increase in noise is often associated with weak inversion design. With a MOS transistor operating in weak inversion, the thermal and shot noise is elevated. Also, the noise of the BJT device increases with lower bias current, as pointed out in [18].

Although low noise has not been the design focus of this effort, carrying out a noise measurement on the designed switched capacitor bandgap will help identify noise impact when used in conjunction with other circuits. Figure 76 shows the output noise spectrum of the switched capacitor bandgap output, on V_{BG_SC}, measured at room temperature.

The data was taken with a HP3589 spectrum analyzer by measuring a single point noise spectral density (normalized to a 1-Hz bandwidth). The test was repeated over the frequency ranges of interest. To correctly measure the switched capacitor bandgap noise, the clock signal from the oscillator is used to trigger the HP3589 to perform the gated measurement.

4.3.6 Supply Rejection

Supply rejection measures the attenuation a circuit provides with respect to disturbances on its supply rail. A sufficient rejection at DC and low frequency is often more important since a disturbance at a higher frequency can be bypassed. In fact, the supply rejection measured at DC and low frequency should compare with the DC line regulation.

Measurements show that the supply rejection is between –60 dB to –65 dB. This agrees well with the DC line regulation. Also, the supply rejection during output phase (Φ_2) is much lower than the preset/recharge phase (Φ_1). This is mainly due to the fact that switched capacitor bandgap was effectively in open-loop configuration at DC and low frequency where ripple coupled to output can not get divided by open-loop gain. Thanks to the supply sub-regulator, bandgap supply rejection was significantly improved.

Also, note that simulation consistently overestimates the supply rejection, as compared to the measurements. This can be attributed to the exclusion of device mismatch in a nominal simulation where devices the same size are deemed identical. For circuits that have a symmetrical architecture, the unrealistic exclusion of device mismatch helps boost the rejection since part of disturbance is cancelled out. To better correlate to the measurement results, Monte-Carlo simulations were run to include device mismatch. The result is shown in Figure 77, indicating reasonable agreement between the measurements and the simulation, from DC to 100 kHz.

The test setup used in measuring supply rejection is shown Figure 78. An AC source generated from HP4194A was capacitive-coupled and superimposed with DC to supply the bandgap. An inductor of 1 mH was inserted between power supply and V_{DD} to block any AC component off the power supply. The bandgap supply rejection was measured by referencing the bandgap output to its supply.

4.3.7 Voltage Distribution

To evaluate impact of random process variation on the bandgap output, a total of 35 samples were tested at room temperature. The mean and standard deviation of the continuous-time bandgap output, V_{BG_CT}, were calculated to be 617 mV and 11 mV, respectively. A histogram of the measured results is shown in Figure 79.

4.4 Characterize Sub-Circuits

4.4.1 Current Generator

With the output current of the bias generator as low as 10 nA, direct measurements could be challenging. Instead of testing the output current directly, the output current's characteristics can be revealed by characterizing the oscillator frequency, which depends primarily on its bias current. This will be discussed in a later section. Also, the test of the current generator start-up was verified when starting the system, as shown previously in 4.3.1.

4.4.2 Sub-Regulator

The supply sub-regulator provides isolation from the supply, attenuating ripple, further shielding subsequent circuits to keep them from being affected. The supply rejection of V_{SUBREG} from V_{DD} was characterized using a gain-phase analyzer, specifically the HP4194A for this work. The test was completed by coupling a small-signal sinusoidal signal of 0.2-Vpp and measuring the output on V_{SUBREG} referenced to V_{DD} to calculate the supply rejection. Such tests were repeated from 10 Hz to 100 kHz in logarithmic steps, as shown in Figure 80. Observe that at DC the rejection reaches –60 dB and at 1 kHz the attenuation is –20 dB. A bypass capacitor can be readily added on V_{SUBREG} to further improve the high frequency attenuation.

4.4.3 Low Power Oscillator

After the bias generator is started and the bias current established, the oscillator can be turned on by setting the EN high, as shown in Figure 81. The oscillation frequency is measured as approximately 660 Hz at room temperature, which is 18% lower than the expected 800 Hz predicted by the simulation. Part of the discrepancy can be attributed to leakage and parasitic capacitance that is not sufficiently modeled. Data from multiple samples reveal such a shift is systematic. The output clock duty is close to 50%, measured with the statistical function of the oscilloscope. Over a sampling of 180 clock cycles, the average percentage duty is 50.67% with a standard deviation of 2.84%.

Verifying the bias current's temperature dependency follows the functionality test and is expected to be PTAT as shown in Equation 34. As mentioned previously, the output current of the bias generator can as low as 10 nA, thus direct measurements are not practical without extraordinary effort. Instead, the output current is characterized by measuring the oscillator switching frequency as it primarily depends on its bias current.

Figure 82 shows the measured clock frequencies at –25, 0, 25, 50, 75, and 125 °C, taken from 4 different chip samples. The bias current increases with temperature and its temperature exponents, as calculated from the data points, are approximately 1.1 to 1.3.

The spread of the oscillator output frequency is characterized from a total of 37 chip samples which measure CLK_{OUT} at room temperature. The histogram is shown in Figure 83, and has a frequency mean of 643 Hz and a standard deviation of 61 Hz.

This observed variation combines both the contribution of the bias current generator and the oscillator. Correspondingly, statistical simulations were run to estimate the variation of the bias generator alone, the variation of the oscillator frequency when biased with an ideal current source, and the overall variation of the bias generator and oscillator, as shown in Table 7. This may serve as optimization guideline for reuse this low-power oscillator.

4.4.4 Op-amp

A low-Z_{OUT} buffer is used as the output stage of track-and-hold op-amp within the switched capacitor bandgap. During characterization, the op-amp closed-loop output impedance was measured. The op-amp was configured in a unity-gain, non-inverting configuration. Its closed-loop output impedance is derived by coupling a small-signal sinusoidal voltage from a gain-phase analyzer, the HP4194A, that measures the associated current across a small resistor, and calculating the impedance by taking their quotient. The op-amp's output impedance is related to its closed-loop impedance by

$$Z_{OUT\_CL} = \frac{Z_{OUT\_OL}}{1 + A\beta} \qquad \text{Equation 37}$$

where $A\beta$ is the loop gain comprised of open-loop gain A and feedback factor β. β is 1 in this test configuration.

The output impedance is measured over the frequency range of 10 Hz to 1 MHz and is shown in Figure 84. Due to high open-loop gain at low frequency, the closed-loop output impedance is below 1 Ω at DC, among which a significant portion is cable impedance that is outside of amplifier feedback loop. At 10 kHz the output impedance remains well below 100 Ω. The test setup measuring the output impedance is depicted in Figure 85.

The closed-loop, small-signal step response is shown in Figure 86 and Figure 87. The overshoot is approximately 40%. Based on the correlation table of percentage overshoot and phase margin [54], the estimated phase margin is approximately 30 °, which is lower than what was predicted in simulation shown in the previous chapter. After further reexamination it was

realized that time-domain simulations could have provided more accurate prediction of circuit stability, where 32 % of overshoot was observed.

The underestimation using frequency-domain simulation was mainly due to the circuit simulator's assumption of quiescence operating point, which could be considerably disturbed in low-bandwidth circuits when responding to input signals with fast edges. In contrast, time-domain simulation does not have this limitation.

4.4.5 Track-and-hold

The track-and-hold stage is characterized as a stand-alone circuit. Its functionality is shown in Figure 88. The input signal, V_S, is a sinusoidal signal with a frequency of 200 Hz, and amplitude of 500 mV peak-peak. The output, V_{TR_HD}, alternates between a tracking phase and a holding phase for 25% and 75% of its own period, respectively. The frequency of the clock driving the track-and-hold stage is approximately 2.5 kHz. No significant voltage droops were observed in this test. Since the track-and-hold stage was designed for converting discrete-time bandgap voltage into continuous-time format, the dynamic characteristics were not the focus of this work.

4.5 Conclusion

This chapter covers the characterization of a switched capacitor bandgap. Measurement results were provided for the switched capacitor bandgap system. Also characterization data on key individual circuits were also provided for design insight and assist IP reuse. The measurements showed the switched capacitor bandgap delivered satisfactory performance as a reference circuit. The design goal of low power consumption was achieved. Characterization of the sub-circuits revealed how individual building blocks affected system performance, which help provide guidelines for further design improvement as well as circuit applications.

Chapter 5 CONCLUSION AND FUTURE WORK

5.1 Original Contributions

With the technological trend towards low-power design, as well as new applications of low-power electronics emerging, the design and research conducted in this work can be readily applied on a much broader scale. Original contributions of this work include:

- Demonstrated low-power switched capacitor bandgap, with output in both discrete-time and continuous-time forms. Sub-circuits within the system can be readily re-customized to other usages, such as for temperature sensors and supply supervisory circuits.
- Met supply current design target by a successfully constrained static and short circuit current consumption. Implemented analog functions with a severe current constraint, with the majority of the circuits biased with a 10 nA to 50 nA current.
- Developed a low-power analog cell library for IP reuse, including op-amp, comparator, current reference, oscillator, current mirror, and low-voltage biasing structures. Larger circuits developed include the switched capacitor network, the track-and-hold, and the low-Z_{OUT} buffer.

5.2 Future Work

Overall, the switched capacitor bandgap meets the design target, especially in terms of the two key areas: accuracy and power consumption. During characterization, some design pitfalls were revealed. The most prominent one is the stability of the low-power op-amp, which was revealed to have an overshoot and limited amount of ringing, as observed in its small-signal step response, shown in section 4.4.4.

In addition to the design improvements of the designed switched capacitor bandgap, circuit applications abound for reconfiguring the existing design. A supply supervisory circuit is one potential application for monitoring battery voltage, input voltage from the adapter, system voltage, etc.

Figure 89 shows a simplified diagram of a supply supervisory circuit that monitors the supply voltage, V_{DD}, against an internal reference. The switched capacitor supply supervisory circuit allows the monitoring of multiple supplies with one channel, and also allows the duty-

cycle to minimize its own power consumption. The monitoring circuit can also be conveniently switched between *on* and *off*, taking virtually no start-up time.

Figure 90 shows another potential application that can be derived from the switched capacitor bandgap. It is an integrated on-chip thermal regulation function. With enhanced performance and features crowded onto a silicon substrate, the increased heat generated often becomes the bottle neck of future frontiers without trading off reliability, or even causing catastrophic failure.

The switched capacitor on-chip thermal regulation allows measurement of the absolute temperature as well as the thermal gradient across the IC. As the thermal-related event occurs, the IC regulates its power consumption by reducing supply current, or operating frequency. The switched capacitor approach maximizes the reuse of hardware by monitoring multiple diodes across different locations of the IC.

By enabling on-chip temperature measurement and further including die temperature in the design, it would not only improve the IC reliability, but would also allow reliable integration of more features onto a limited-size silicon chip using smaller packages, and further reducing the IC footprint in the system.

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Appendices

APPENDIX A: FIGURES

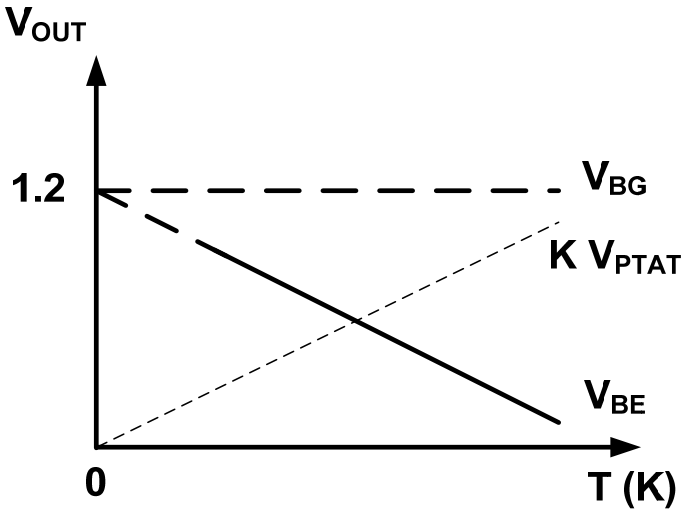

Figure 1 Generation of Temperature Stable Output with PTAT and CTAT Voltage

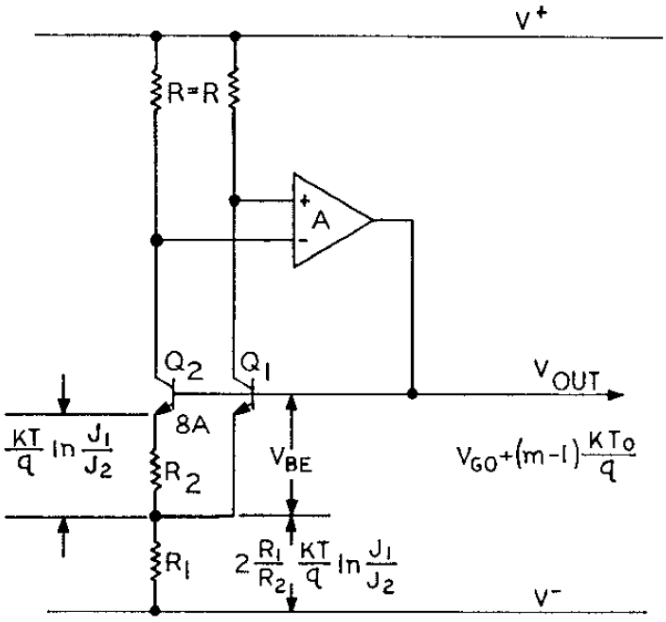

Figure 2 Simplified Schematic of Brokaw Bandgap by Brokaw
Adapted from [19]

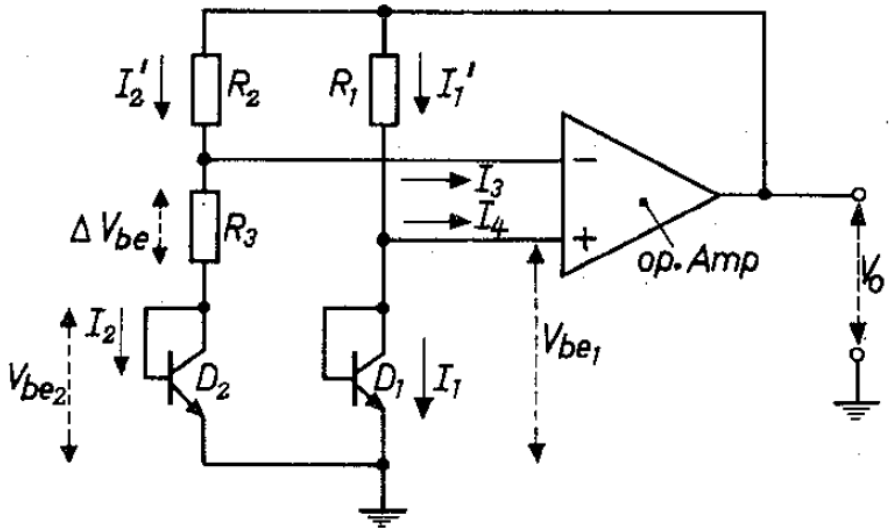

Figure 3 Simplified Schematic of CMOS Bandgap by Kuijk

Adapted from [20]

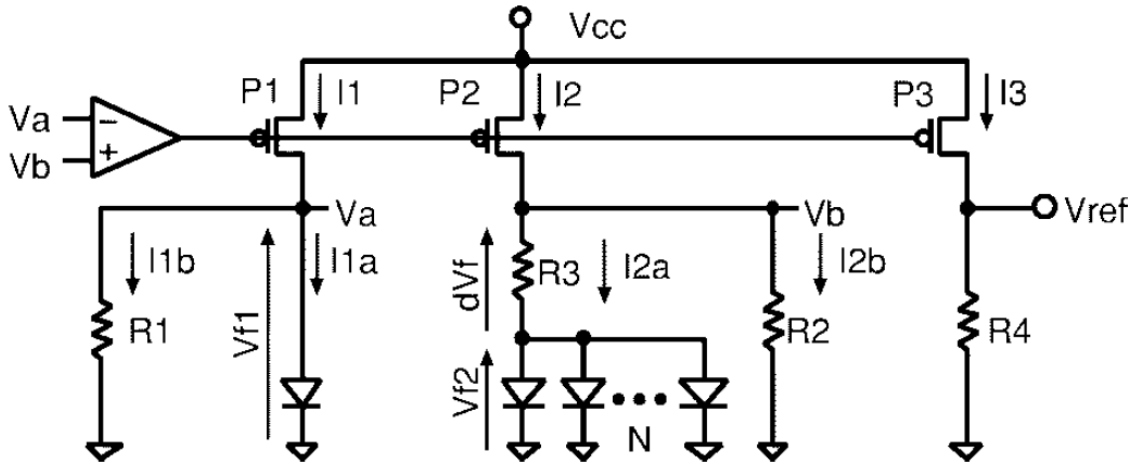

Figure 4 Current-mode Sub-1 V Bandgap by Banba *et. al.*

Adapted from [21]

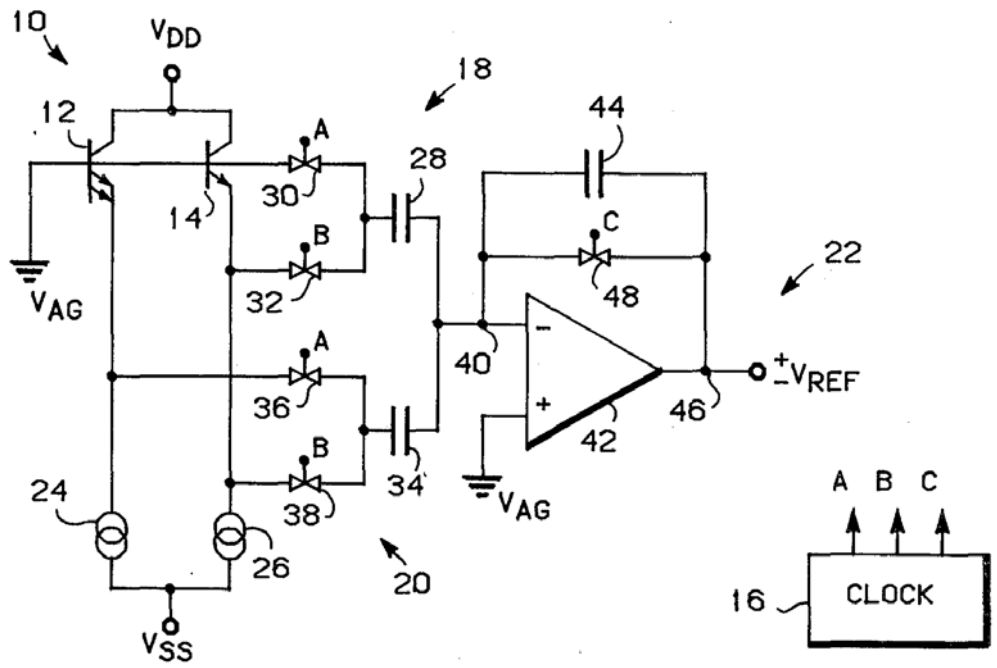

Figure 5 Switched Capacitor Bandgap by Ulmer *et. al.*

Adapted from [22]

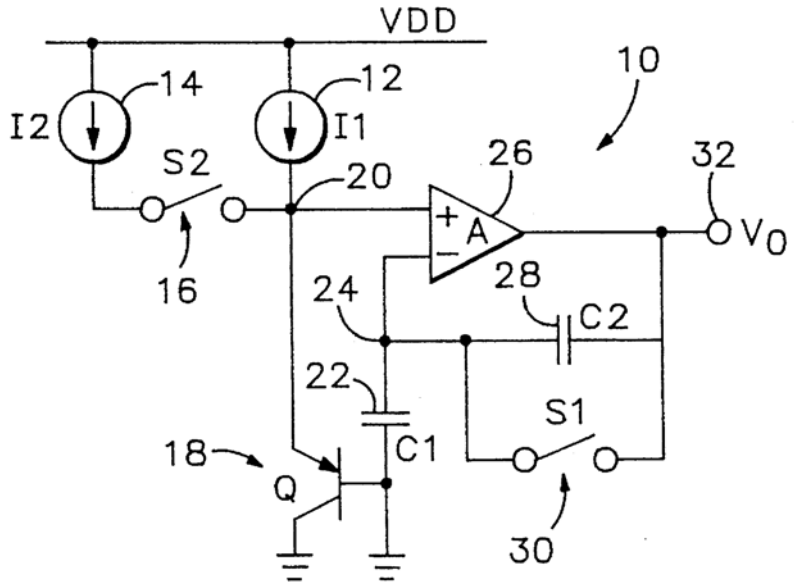

Figure 6 Switched Capacitor Bandgap by Gilbert *el. al.*

Adapted from [23]

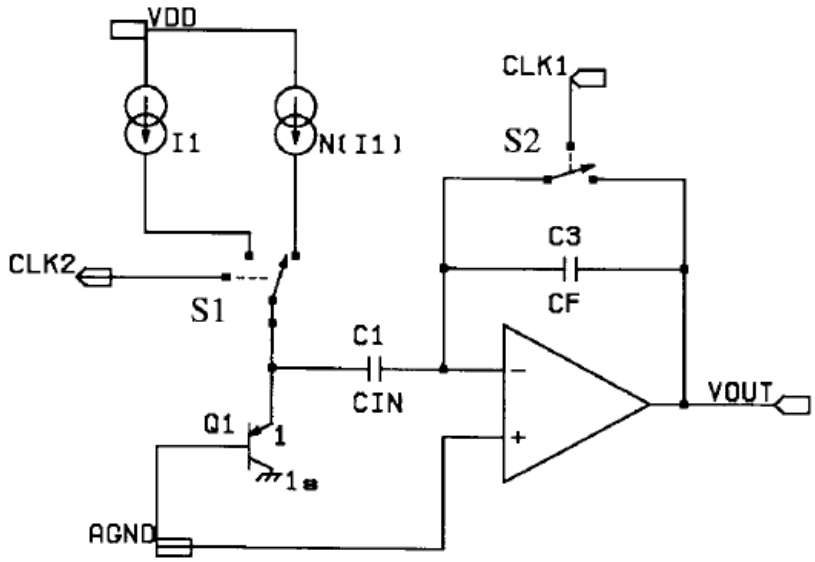

Figure 7 Simplified Schematic of Switched Capacitor Temperature Sensor Adapted from [25]

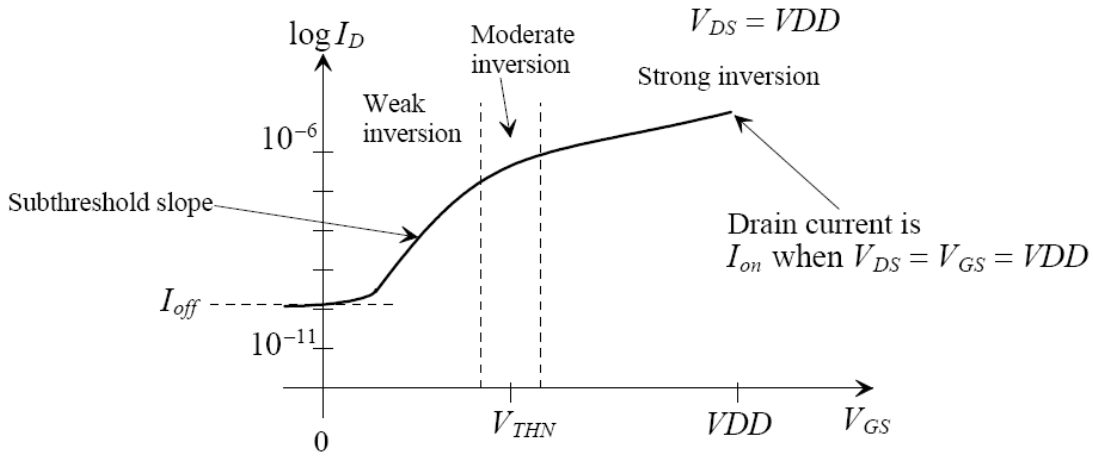

Figure 8 I_D vs. V_G from Weak to Strong Inversion

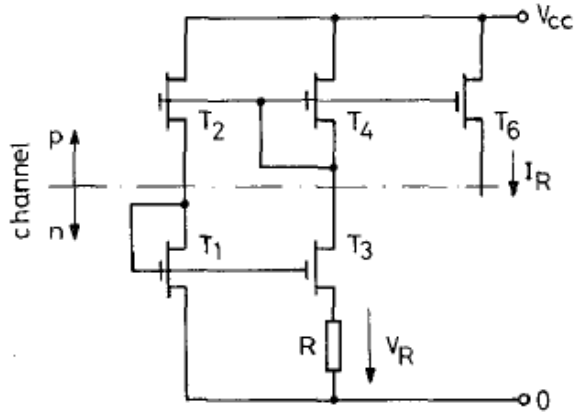

Figure 9 PTAT Current Reference by Vittoz

Adapted from [35]

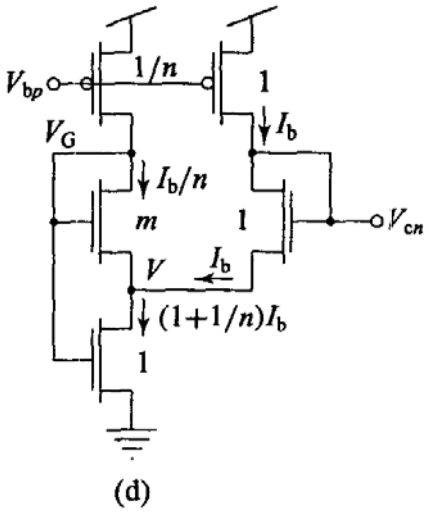

Figure 10 Low-voltage Cascode Biasing by Minch

Adapted from [36]

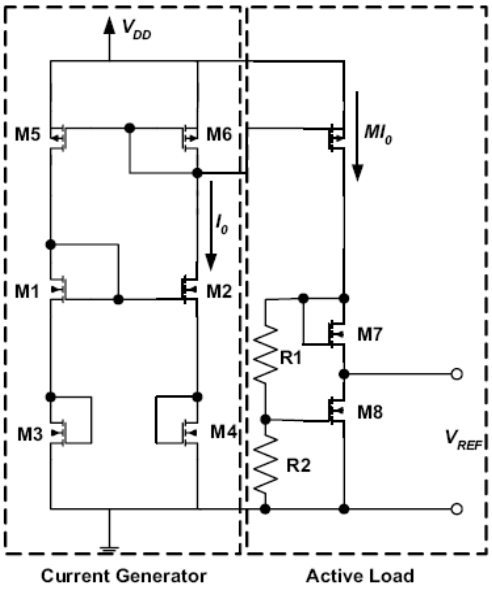

Figure 11 Nanopower BGR by G. De Vita *et. al.*

Adapted from [37]

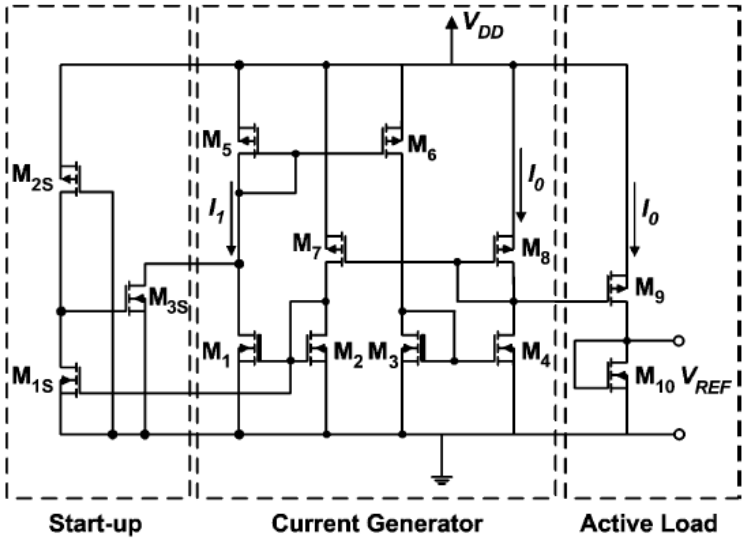

Figure 12 Resistor-less Nanopower BGR by G. De Vita *et. al.*

Adapted from [39]

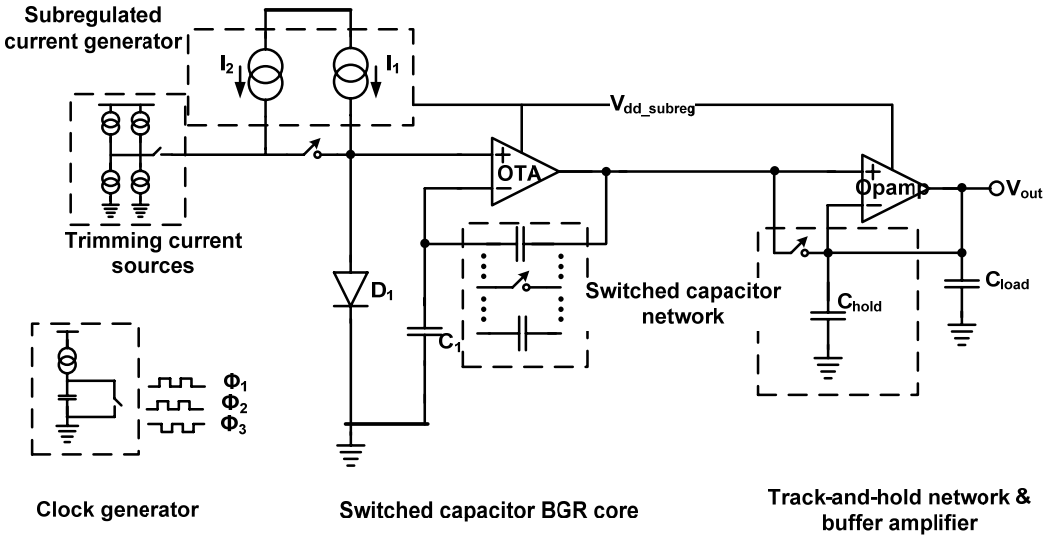

Figure 13 System Diagram of Low-power Switched Capacitor Sub-1 V Bandgap

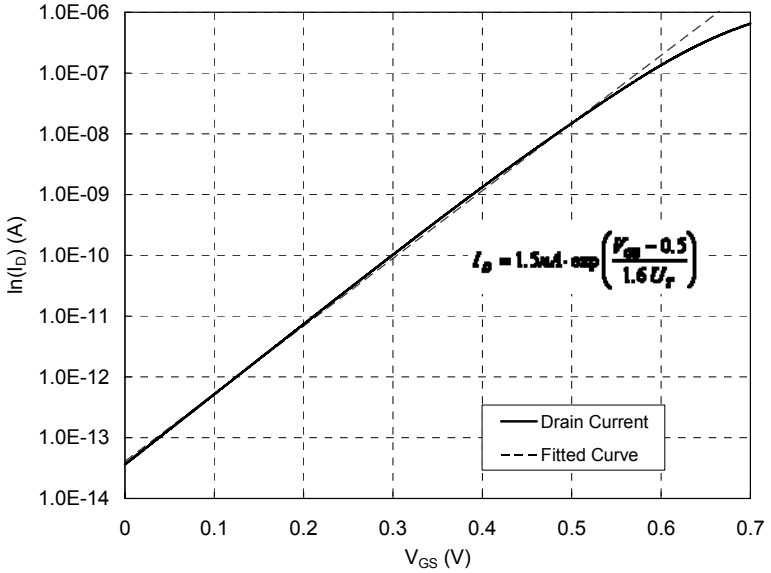

Figure 14 I_D vs. V_{GS} Characteristics & Fitted curve from a long-channel NMOS device

W/L= 10 µm/10 µm

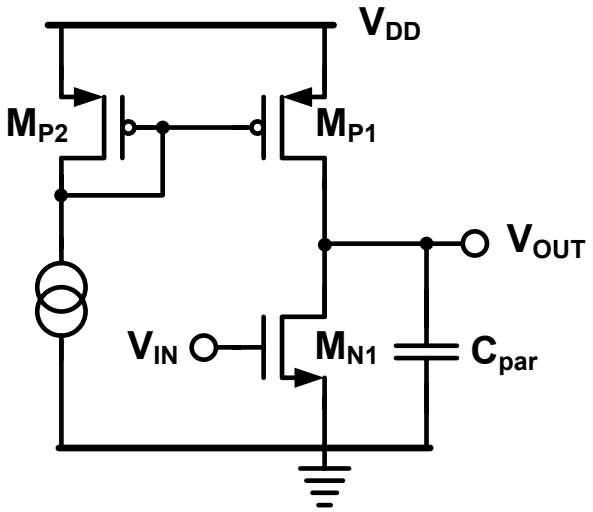

Figure 15 A single commons-source gain stage

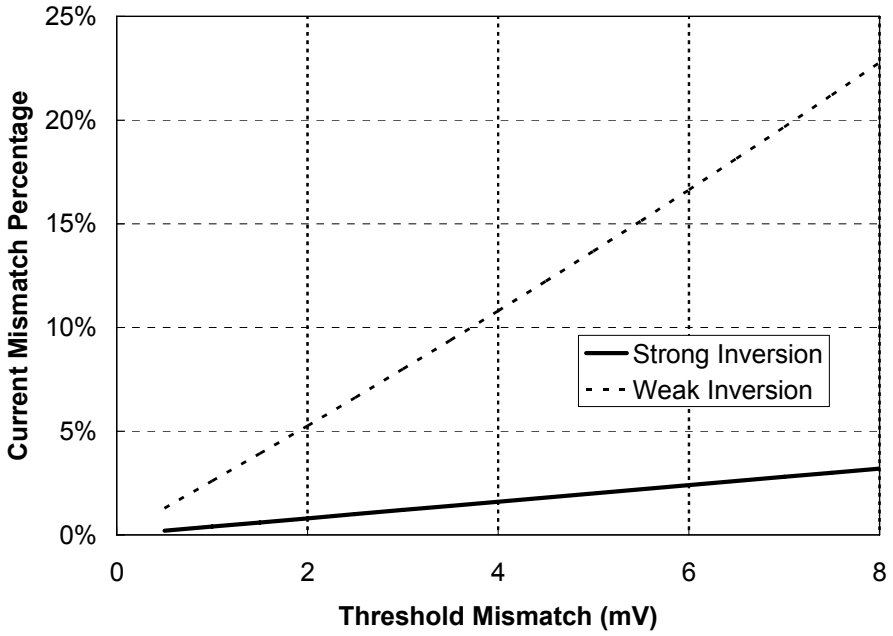

Figure 16 Current Mismatch Comparing Strong Inversion and Weak Inversion

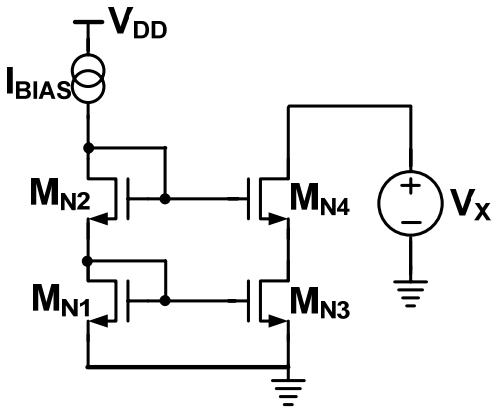

Figure 17 Cascode Current Mirror

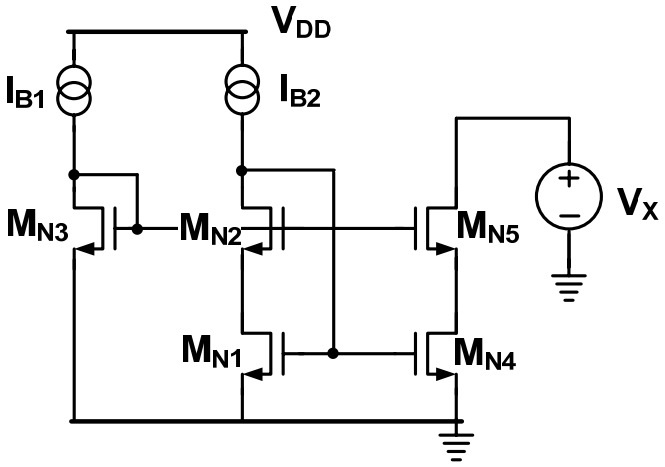

Figure 18 Low Voltage Cascode Current Mirror Biased with Diode-Connected Bias

(Applicable in strong inversion)

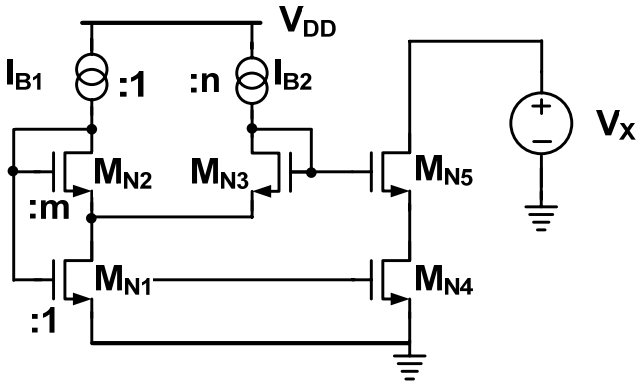

Figure 19 Low voltage cascode bias applicable in weak inversion operation

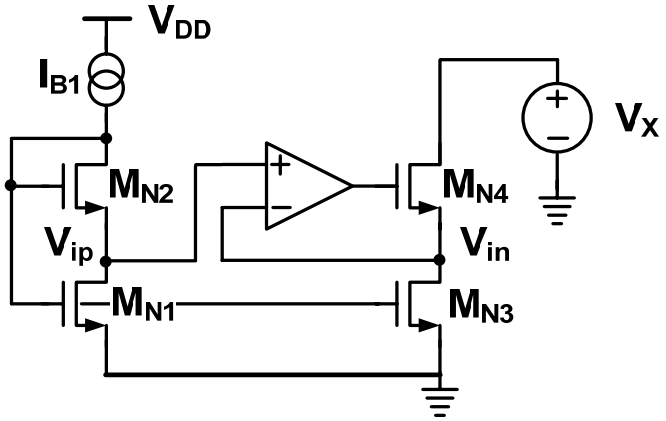

Figure 20 Regulated cascode bias

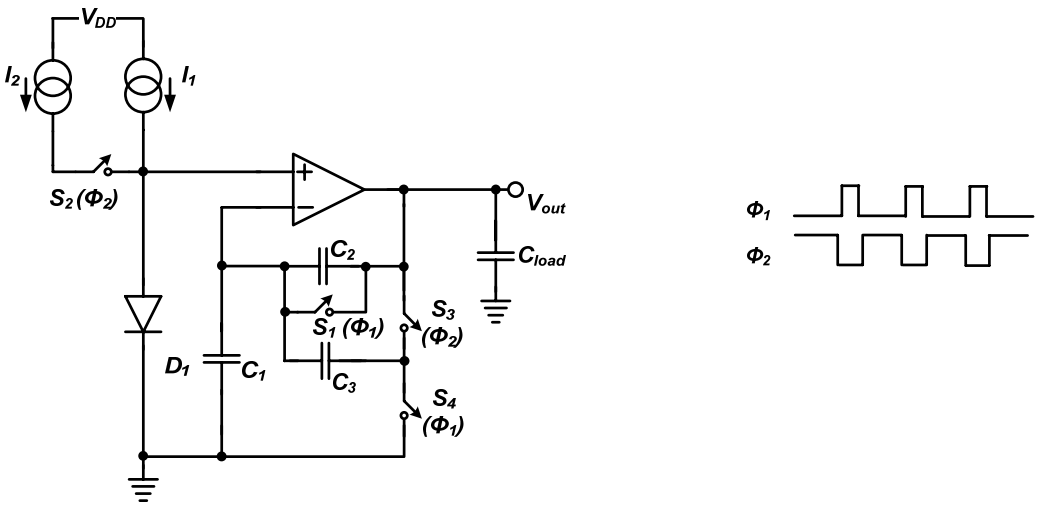

Figure 21 Sub-1 V switched capacitor bandgap core

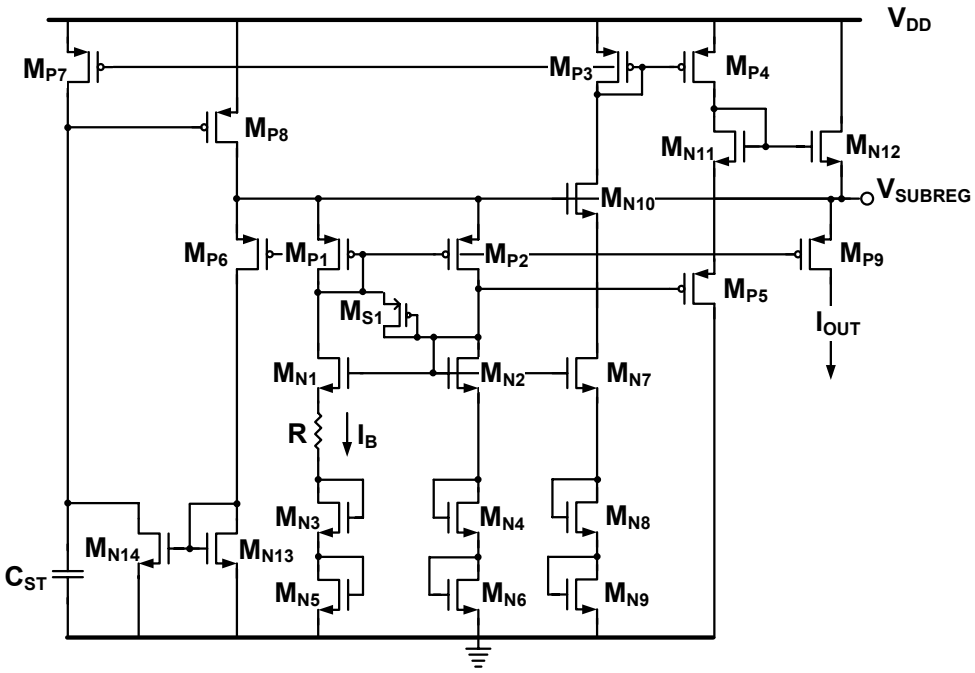

Figure 22 Supply sub-regulator and bias current generator

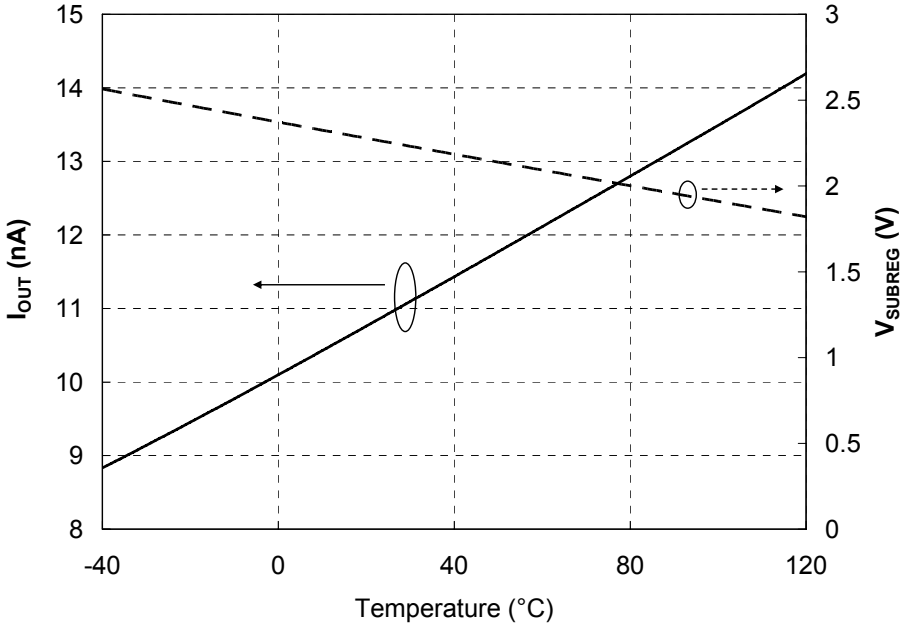

Figure 23 Bias Current vs. Temperature

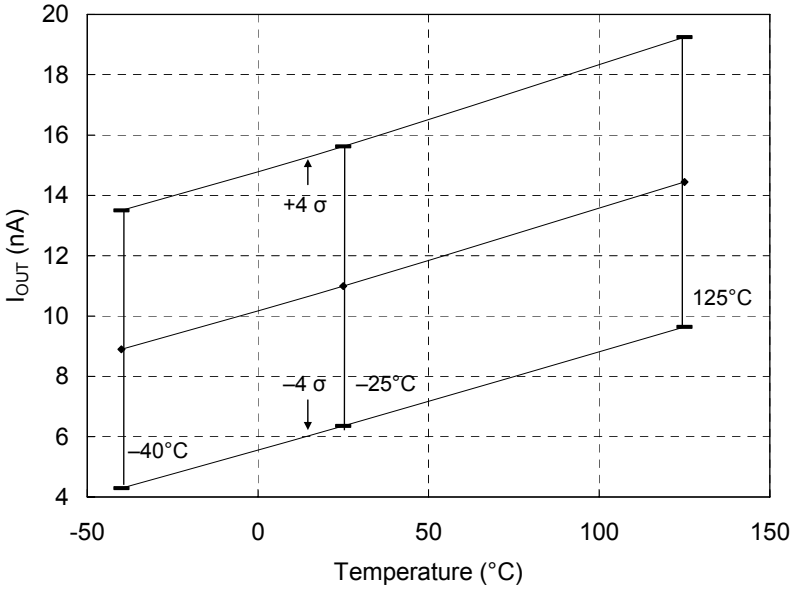

Figure 24 Bias Current 4-Sigma Variation

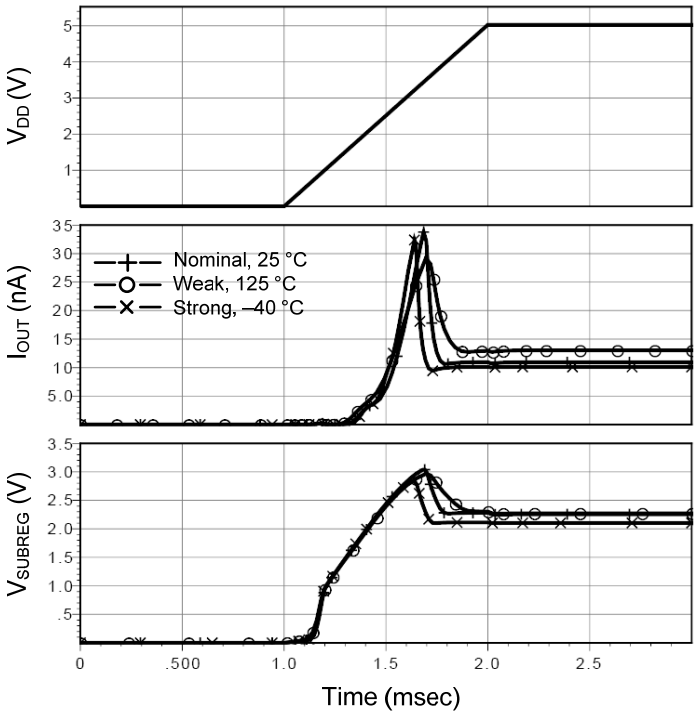

Figure 25 Startup Characteristics

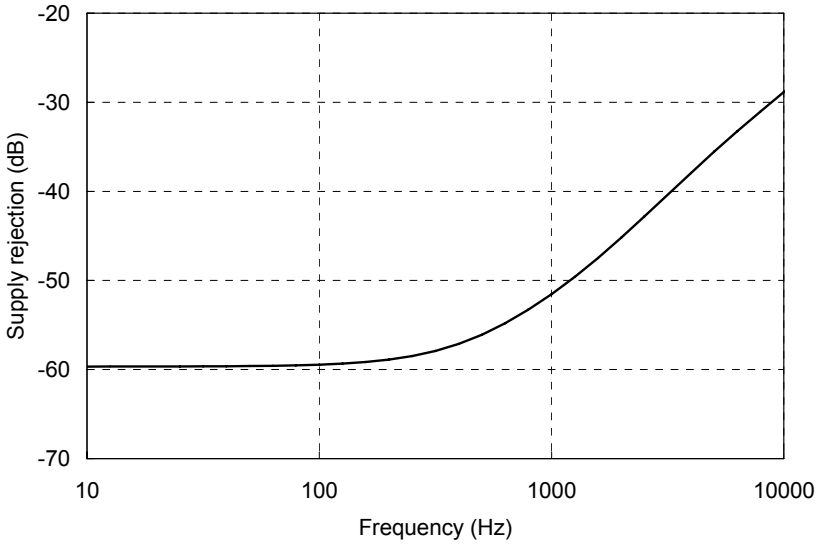

Figure 26 Supply Rejection on V_{SUBREG}

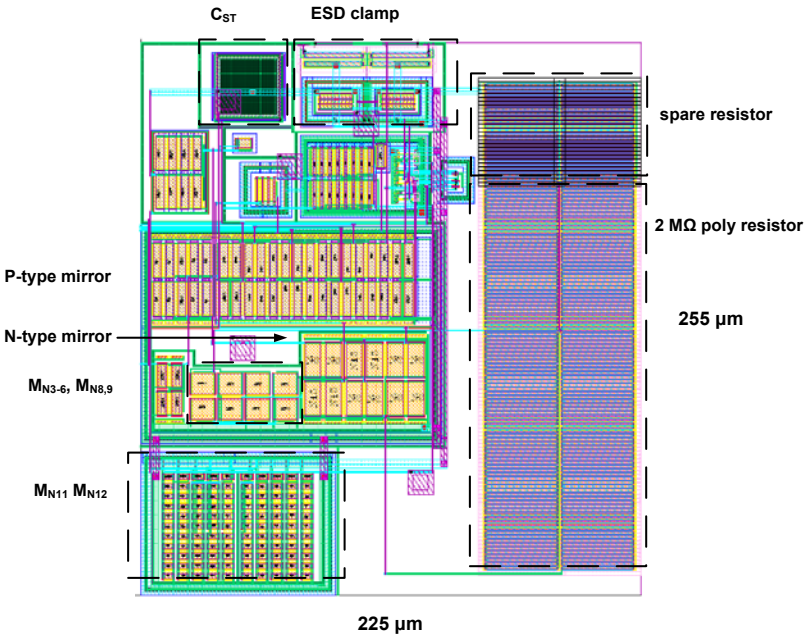

Figure 27 Layout of Current Generator

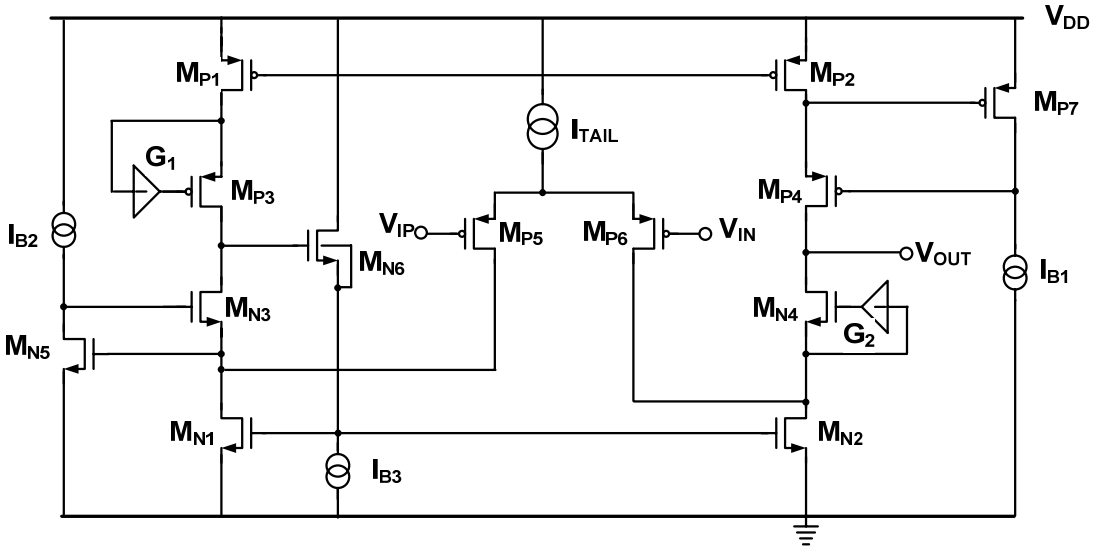

Figure 28 Folded Cascode OTA for Switched Capacitor Bandgap Core

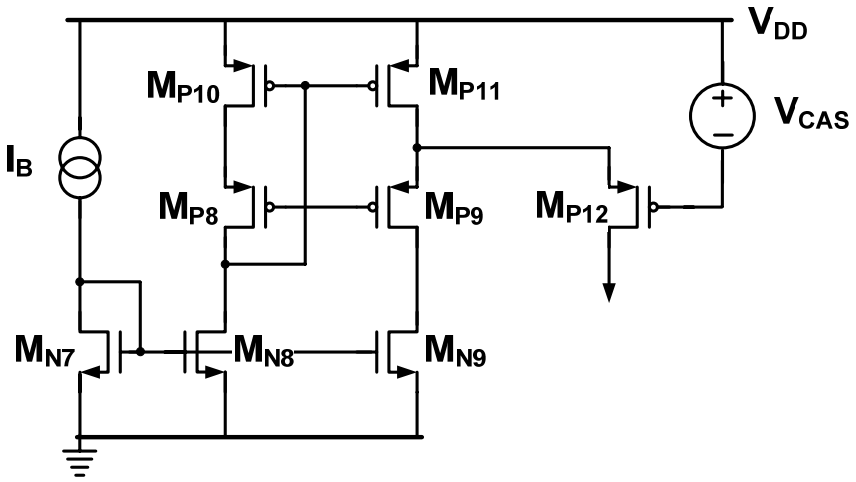

Figure 29 Tail Current of Folded Cascode OTA

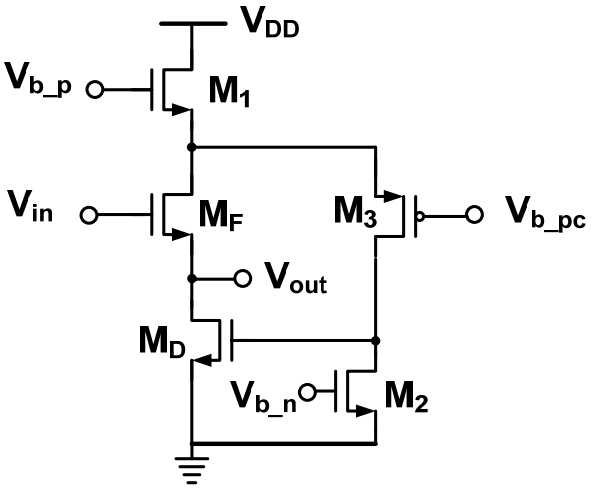

Figure 30 Simplified Schematic of Low-Z_{OUT} Buffer

Adapted from [49]

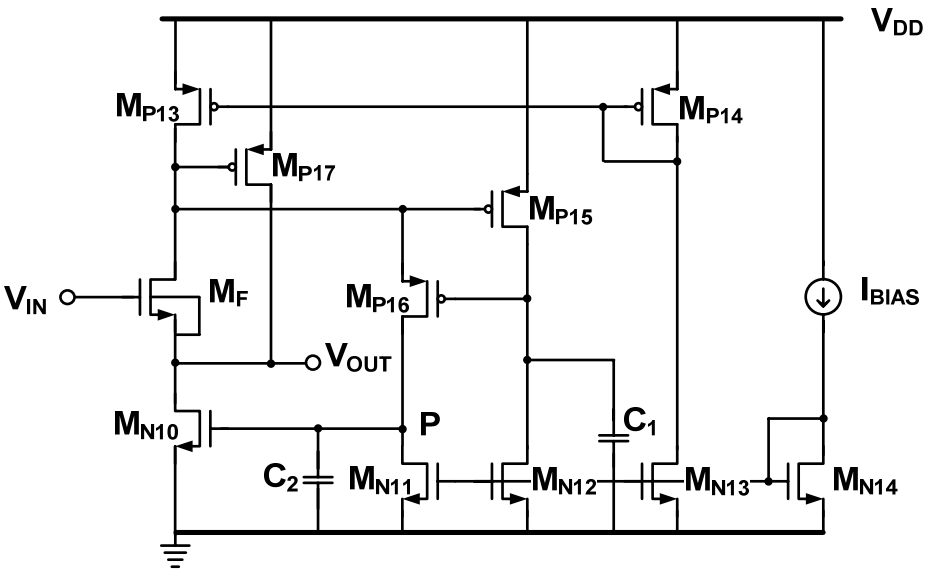

Figure 31 Schematic of Low-Z_{OUT} Buffer

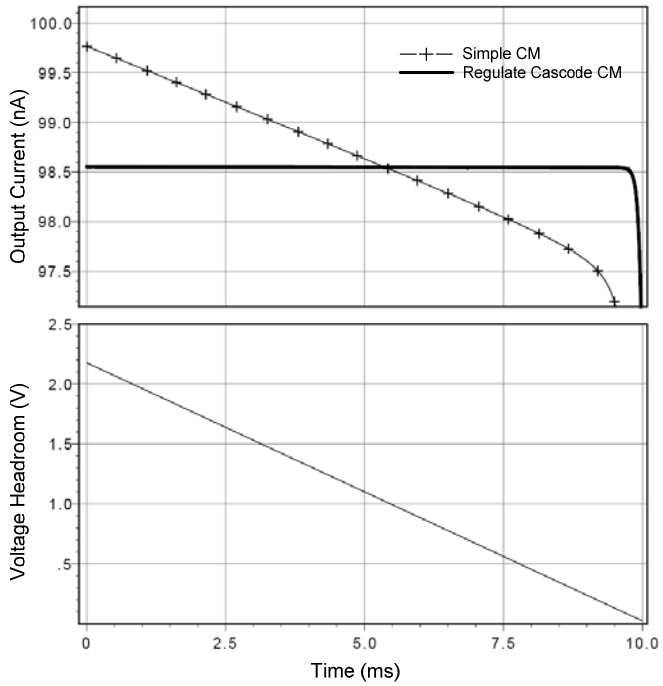

Figure 32 Comparison of Regulated-Cascode Current Mirror and Simple Current Mirror with Transient Simulation

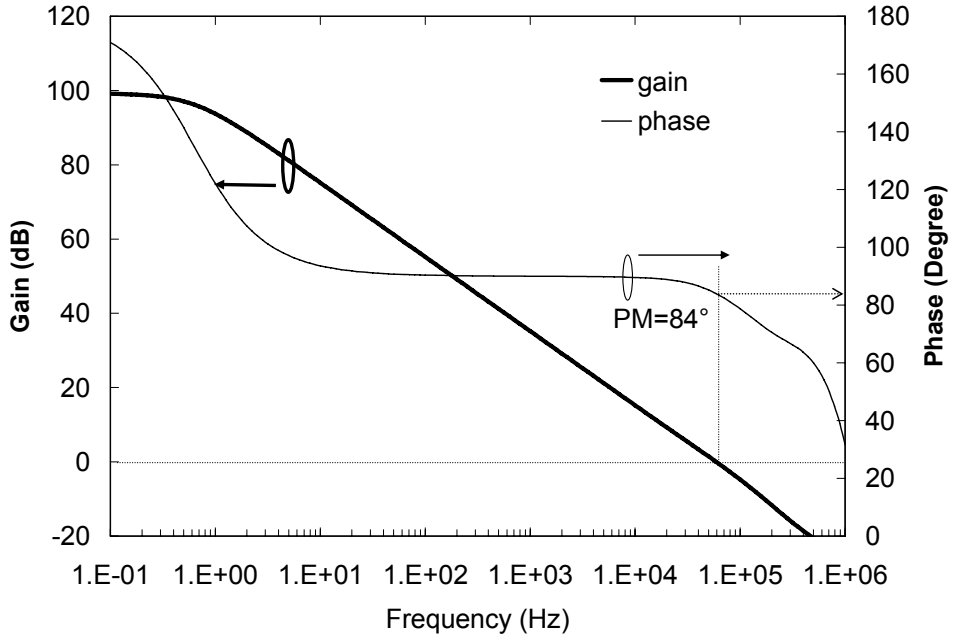

Figure 33 Bode Plot of OTA

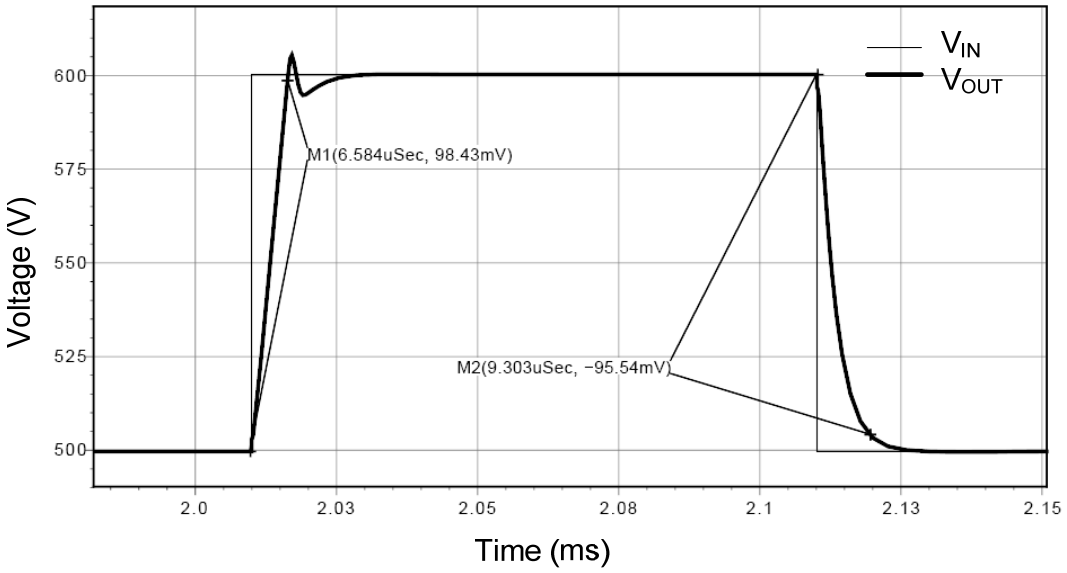

Figure 34 OTA Small-Signal Step Response

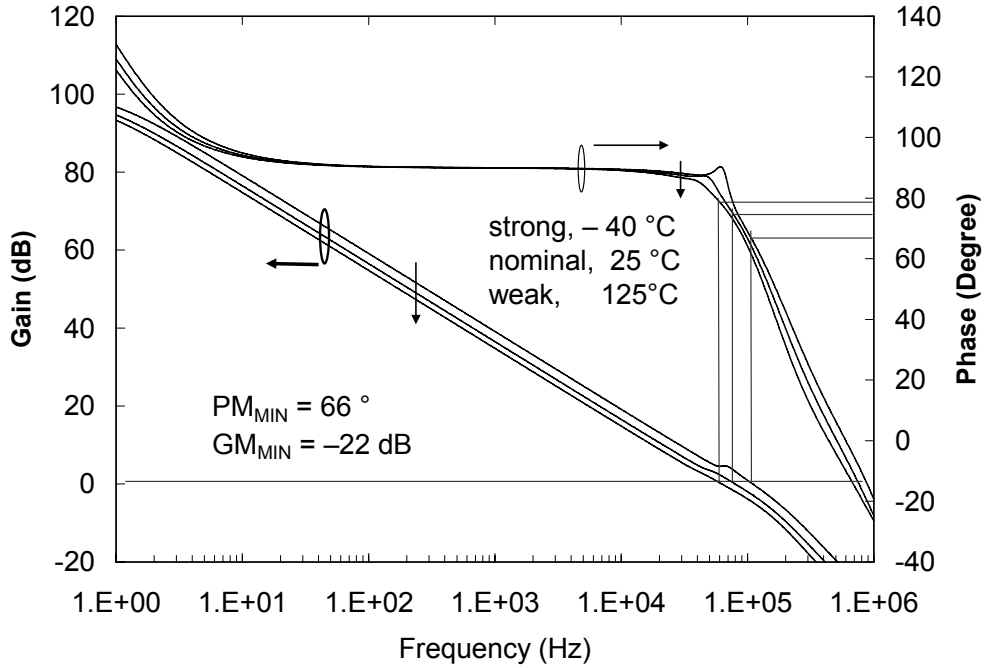

Figure 35 Op-amp Bode Plot at 3 Corners

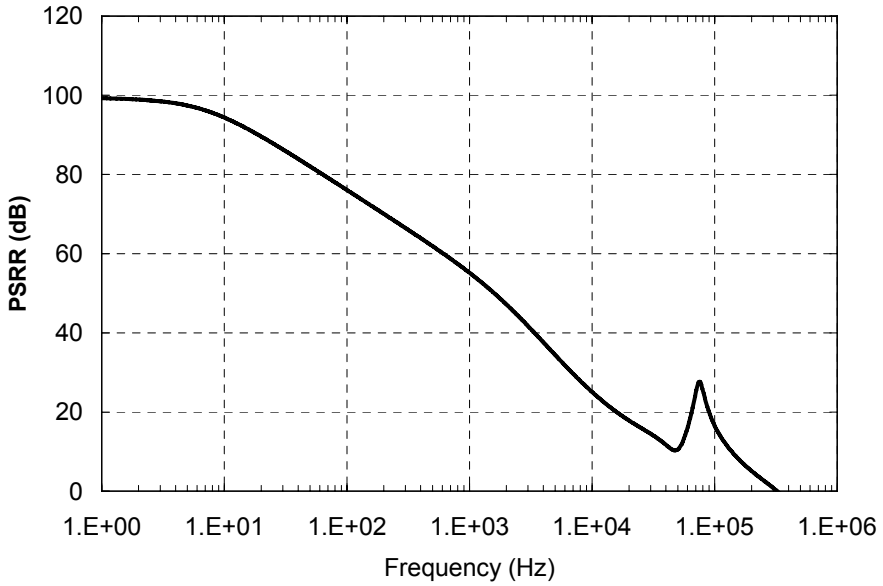

Figure 36 Op-amp PSRR

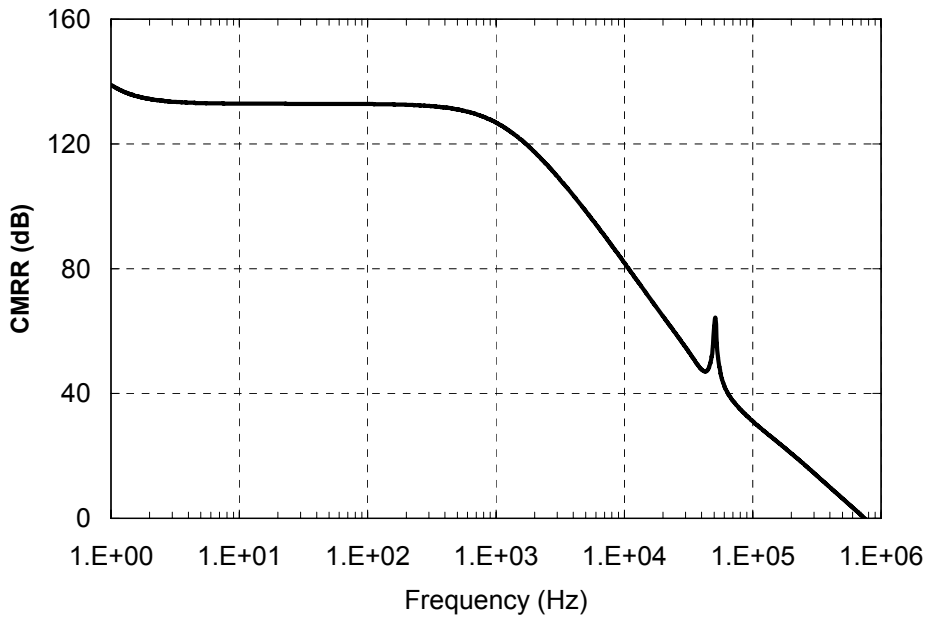

Figure 37 Op-amp CMRR

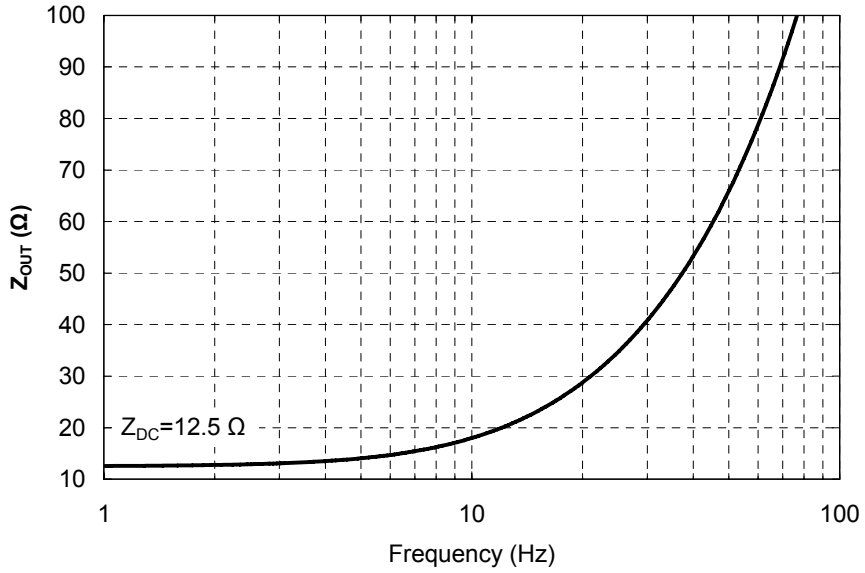

Figure 38 Low-Z_{OUT} Buffer Open-Loop Output Impedance

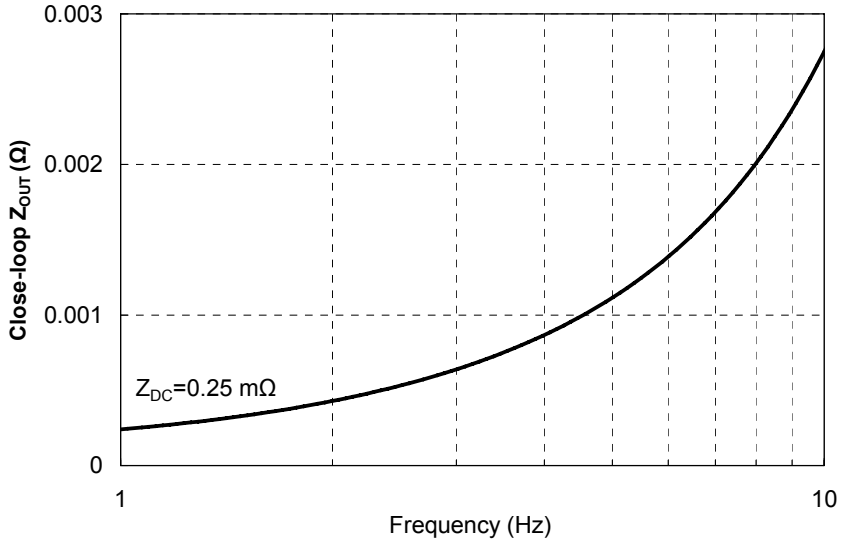

Figure 39 Closed-loop Output Impedance of Op-amp

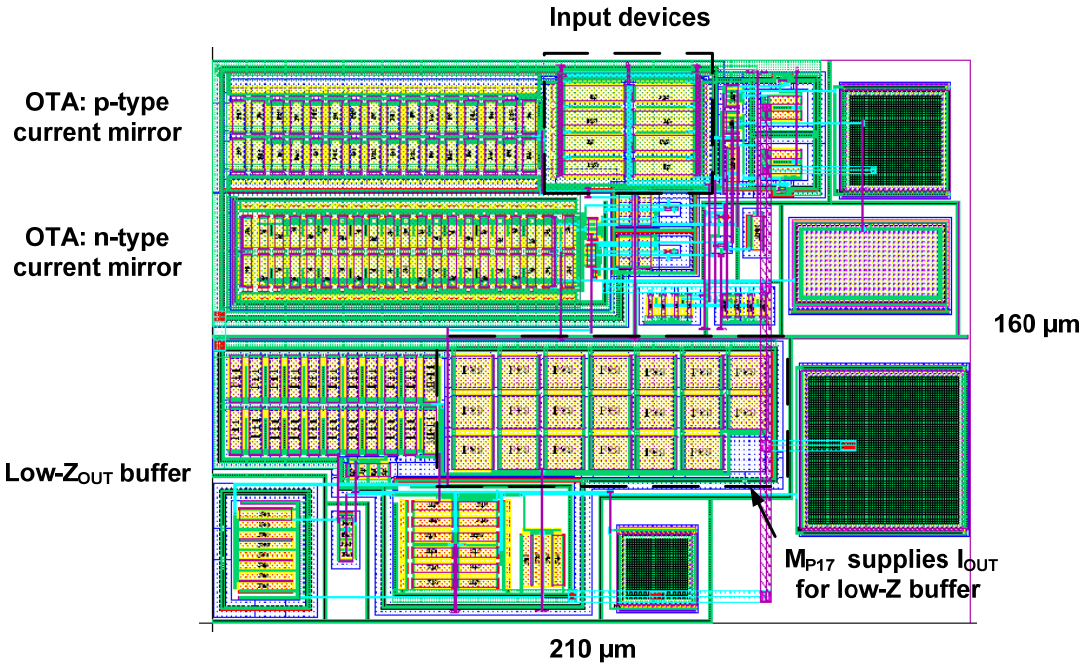

Figure 40 Layout of Op-amp

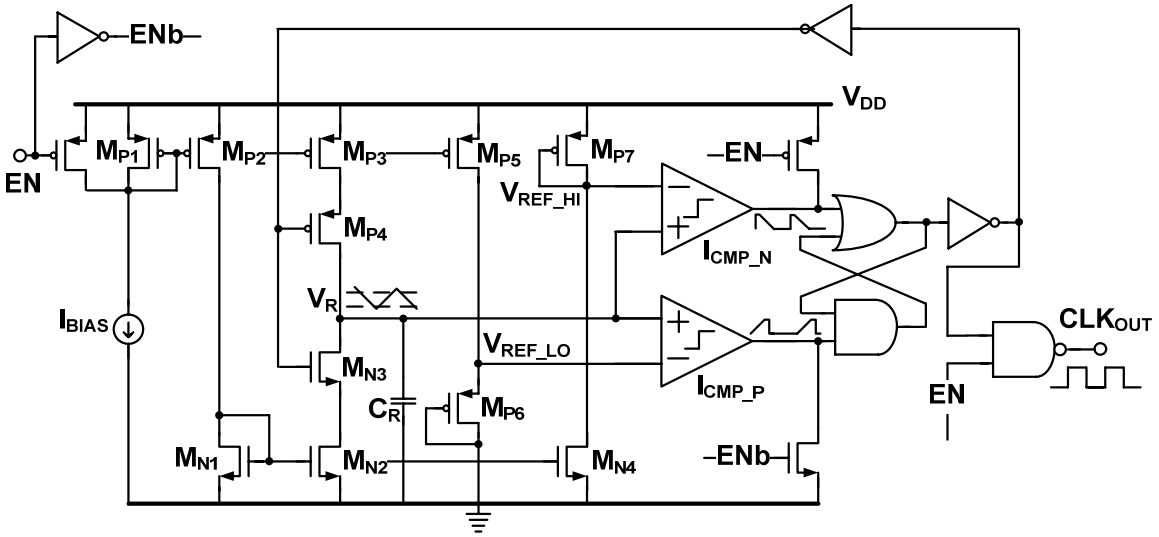

Figure 41 Low-Power Oscillator

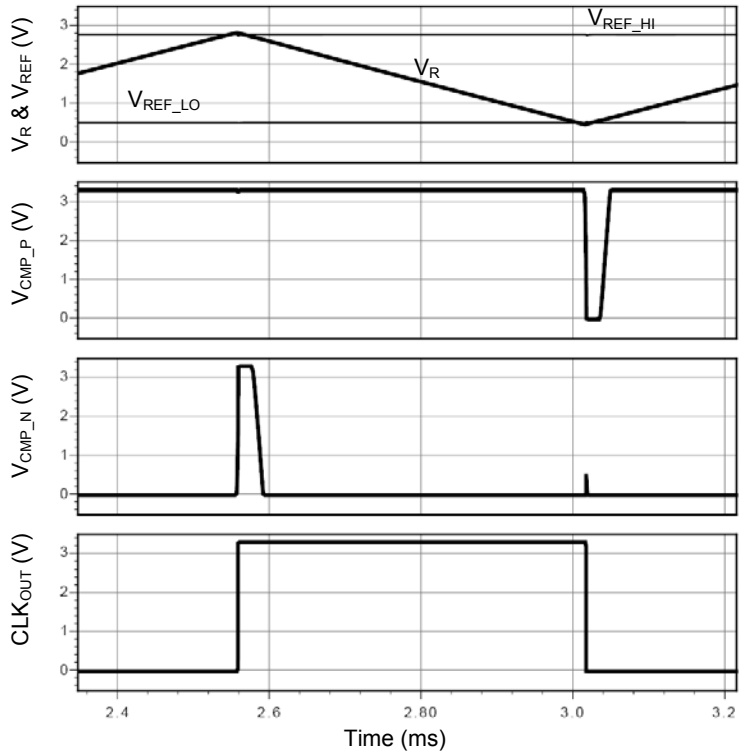

Figure 42 Oscillator Functionality

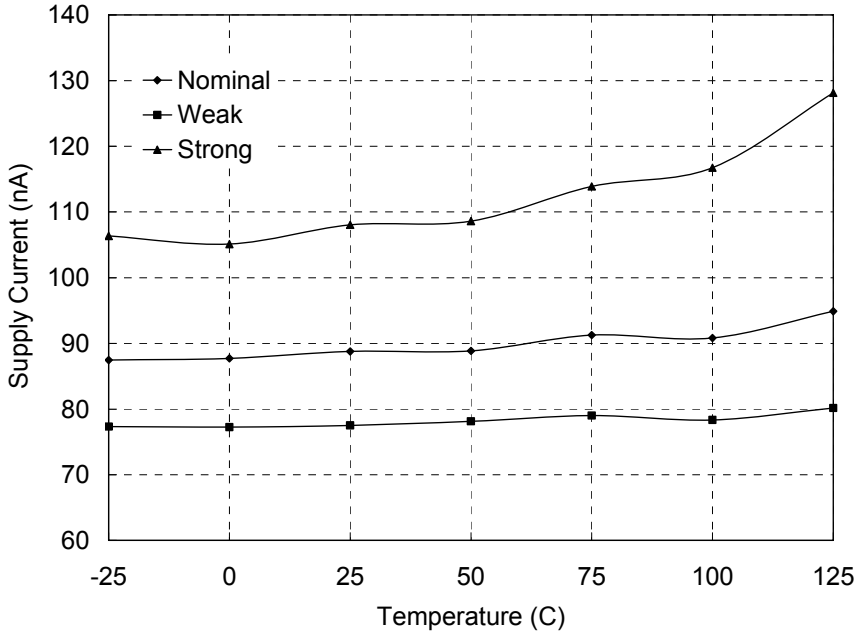

Figure 43 Supply Current of Low-Power Oscillator

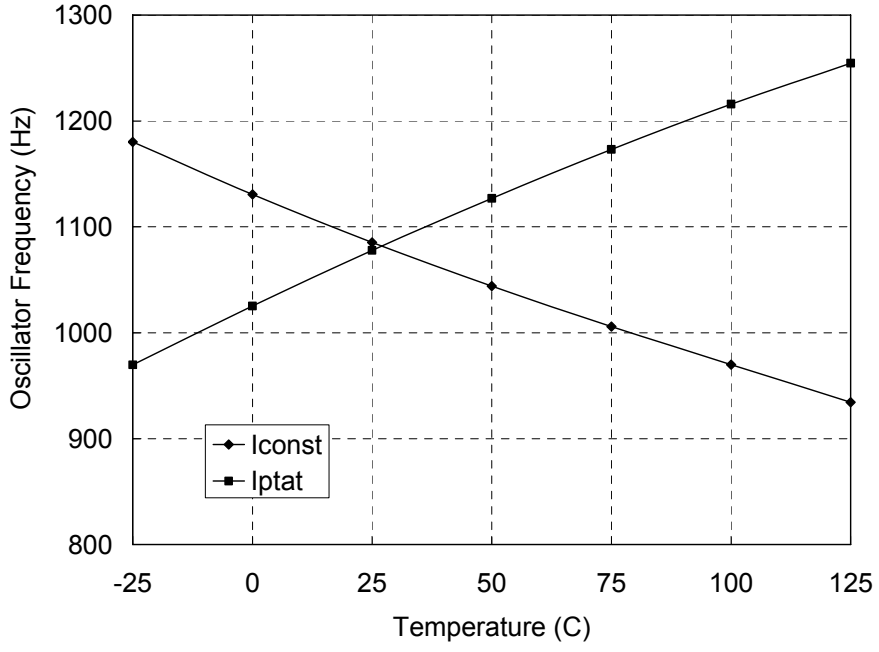

Figure 44 Oscillator Frequency vs. Temperature

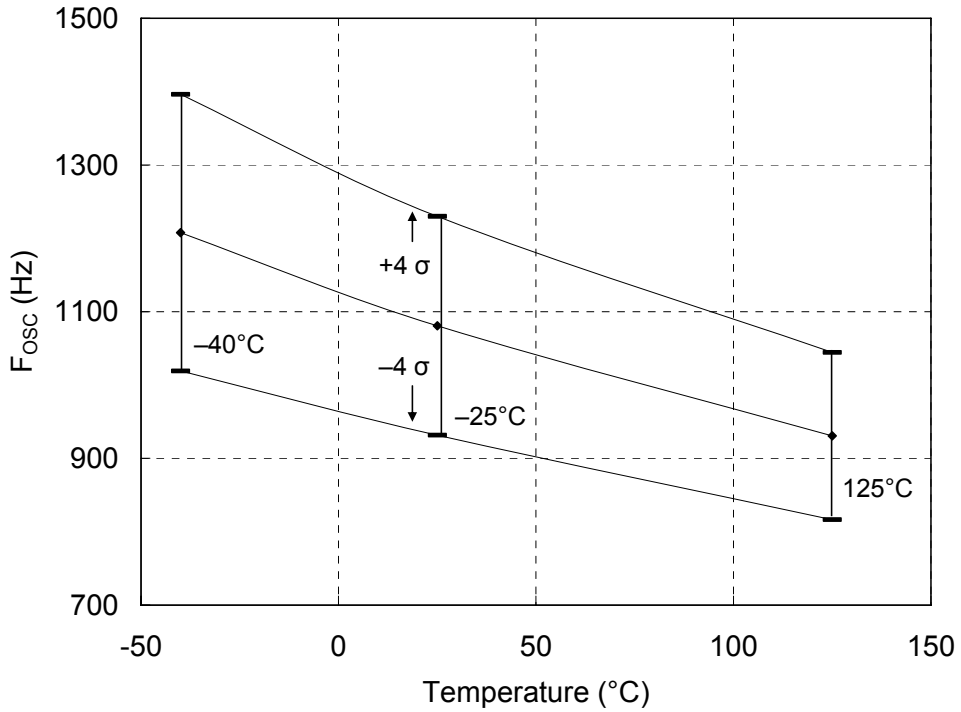

Figure 45 Oscillator Output Frequency Variation vs. Temperature

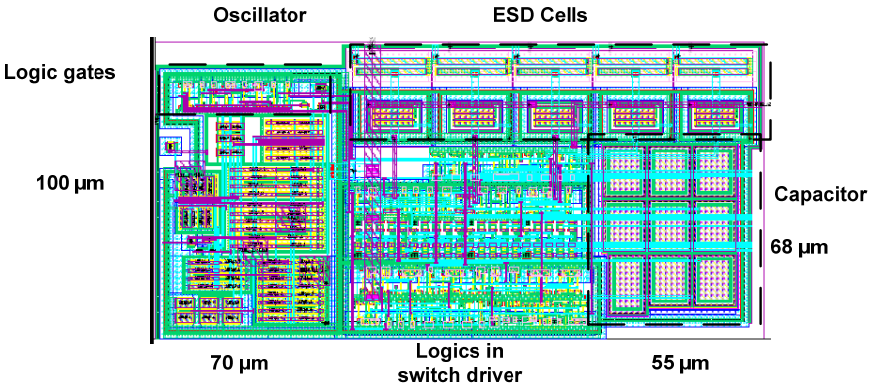

Figure 46 Layout of Oscillator

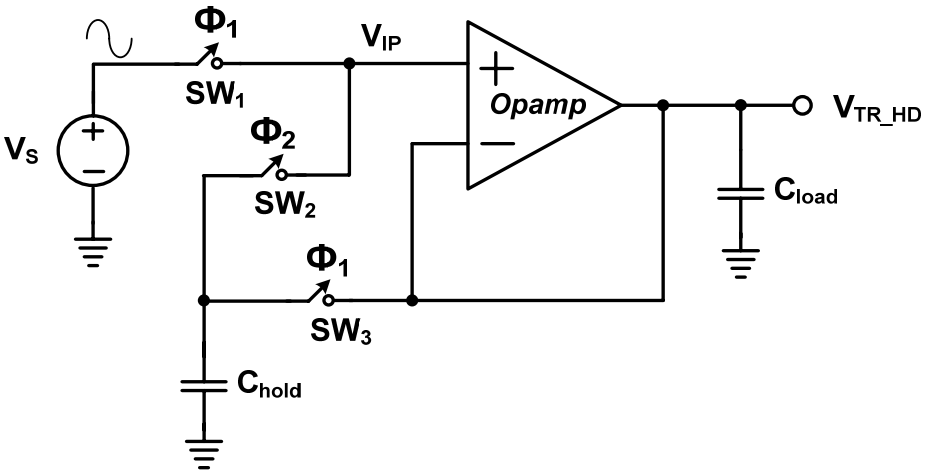

Figure 47 Simplified Schematic of Track-and-Hold

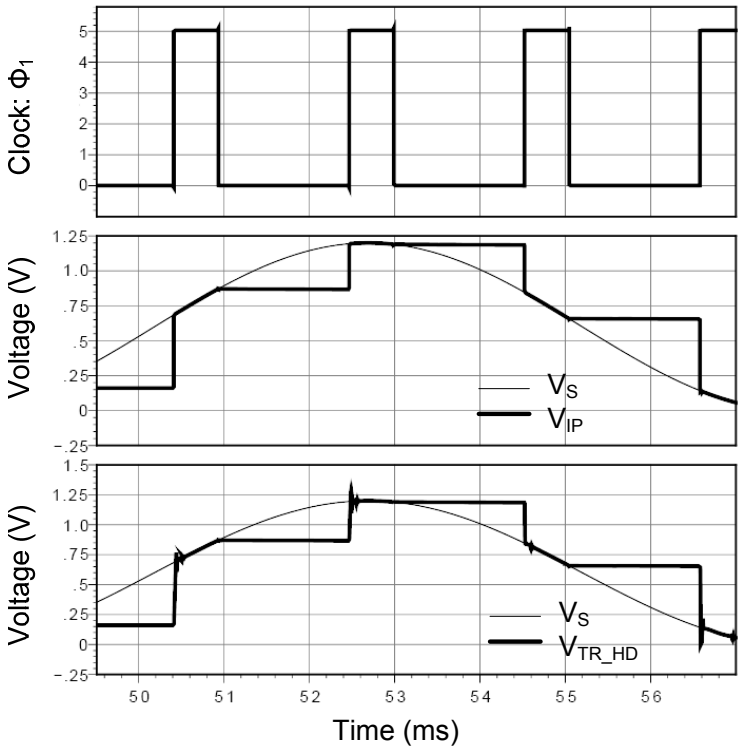

Figure 48 Track-and-hold Functionality

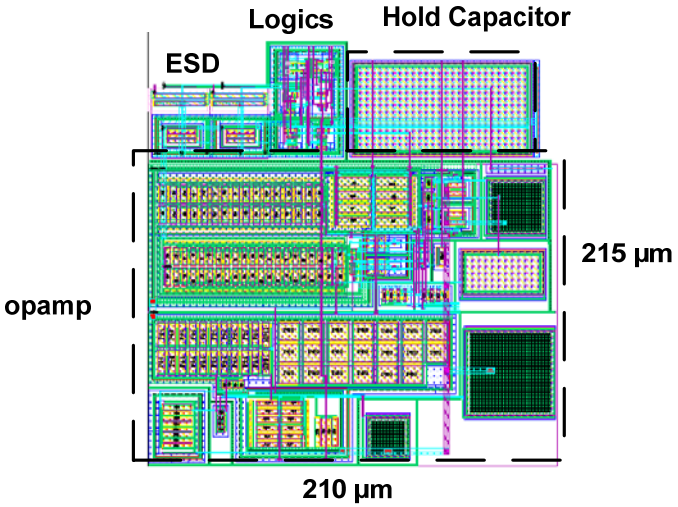

Figure 49 Layout of Track-and-Hold

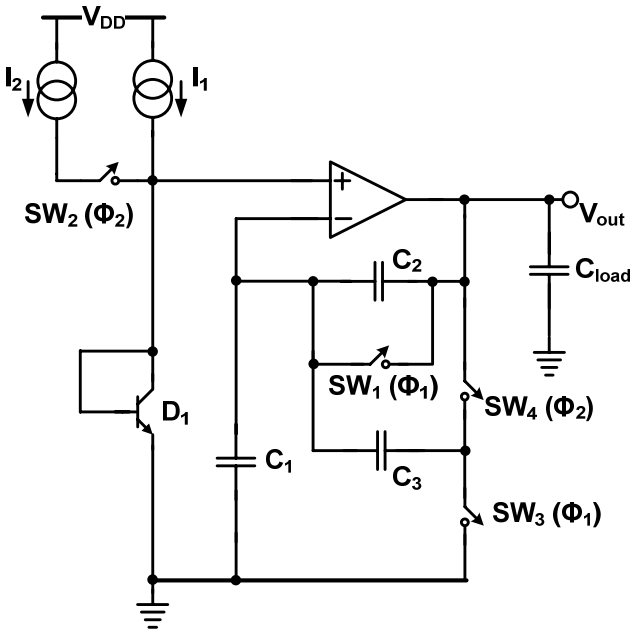

Figure 50 Schematic of Switched Capacitor Bandgap Core

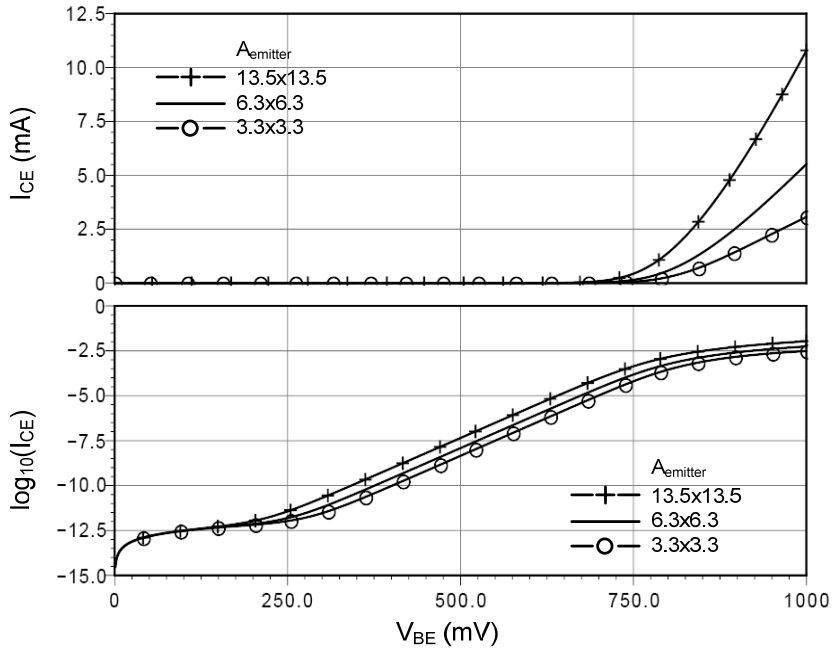

Figure 51 I_C vs. V_{BE} Characteristics of NPN Devices with Different Emitter Sizes

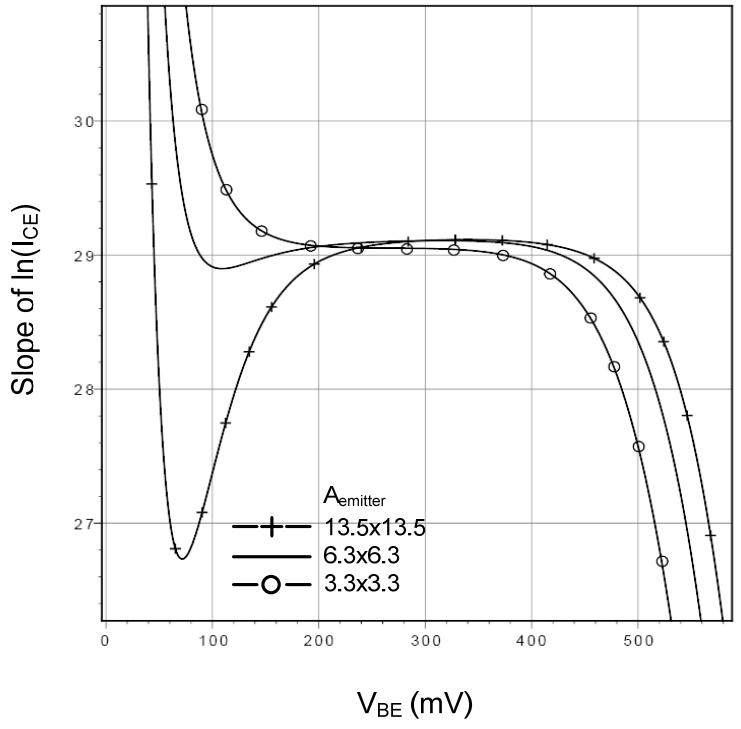

Figure 52 Slope of Collector Current in Logarithmic Scale

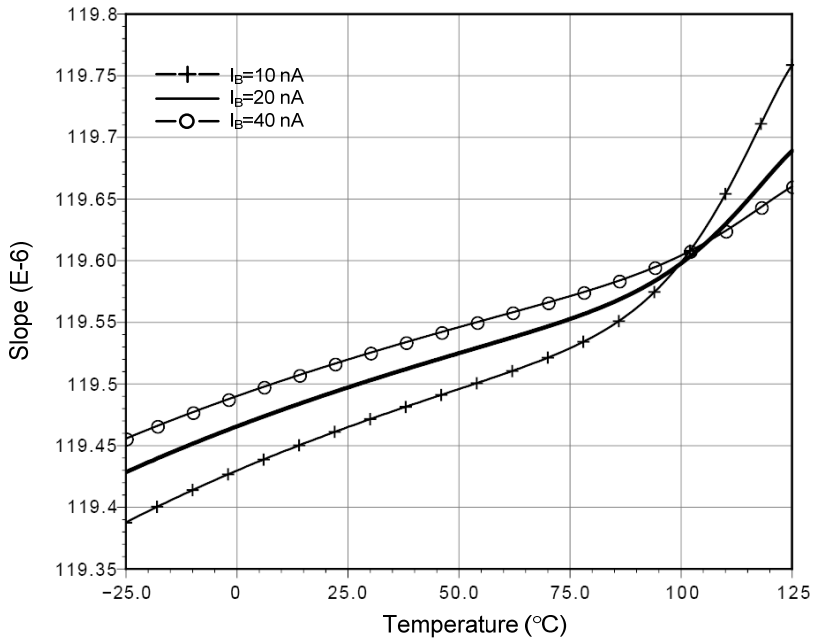

Figure 53 Slope of PTAT Voltage vs. Temperature

Collector Current 10 nA, 20nA, and 40 nA

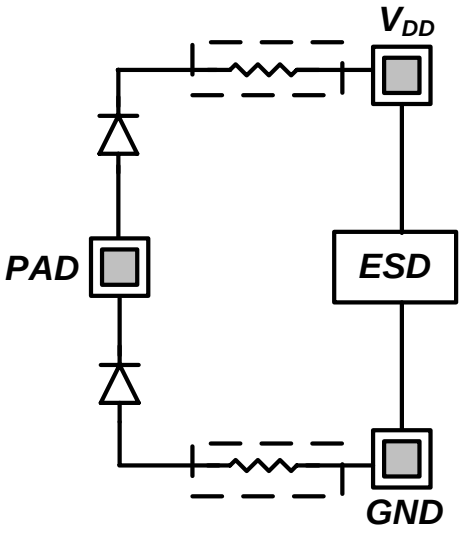

Figure 54 ESD Cells

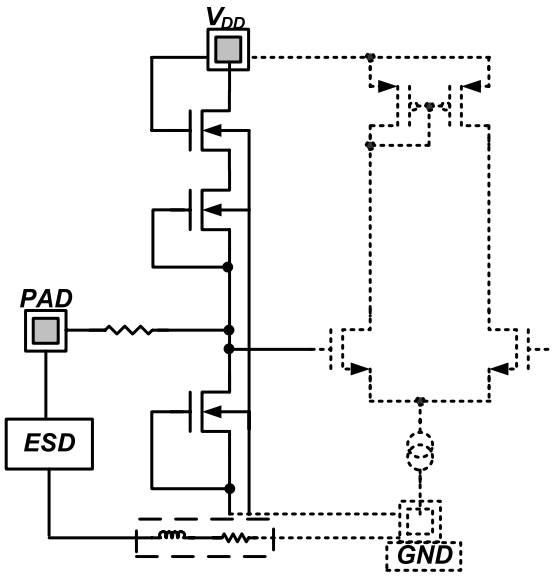

Figure 55 Fail-safe CDM Clamp

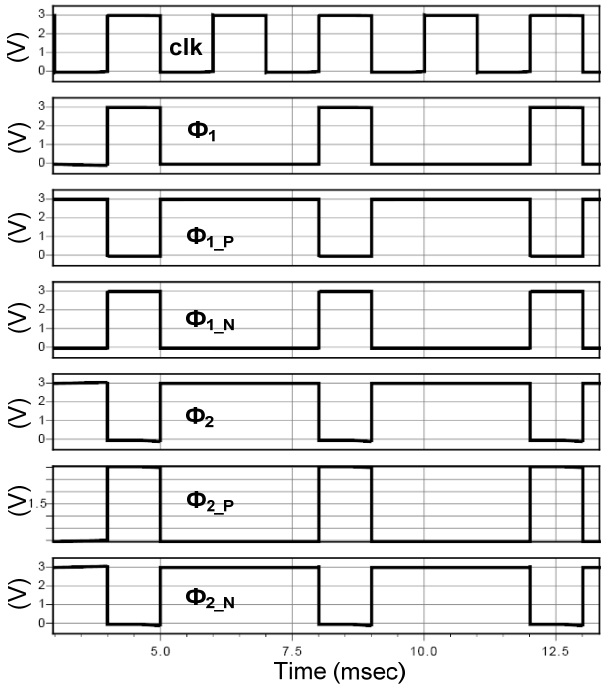

Figure 56 Switch Driving Signals

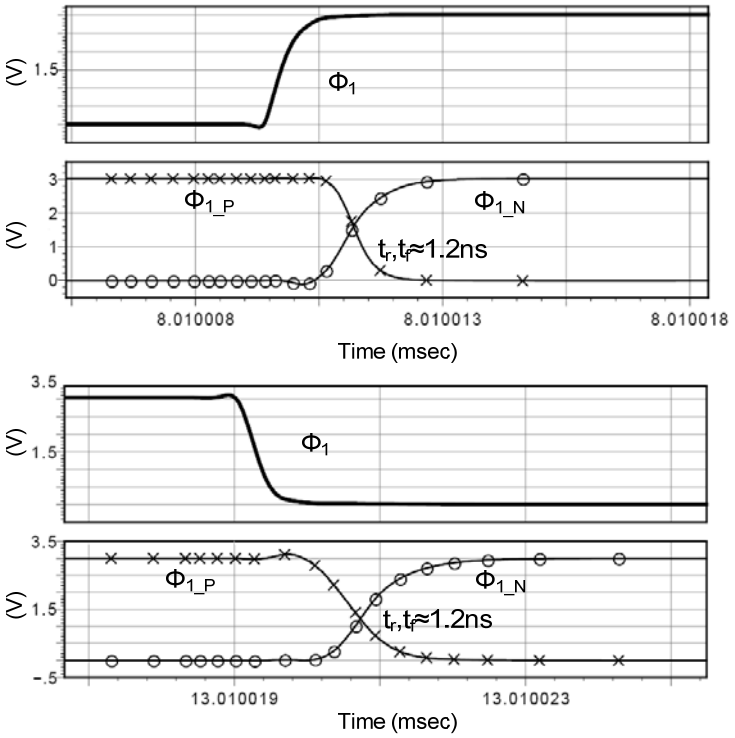

Figure 57 Low-Skew Complementary Switch Driving Signals

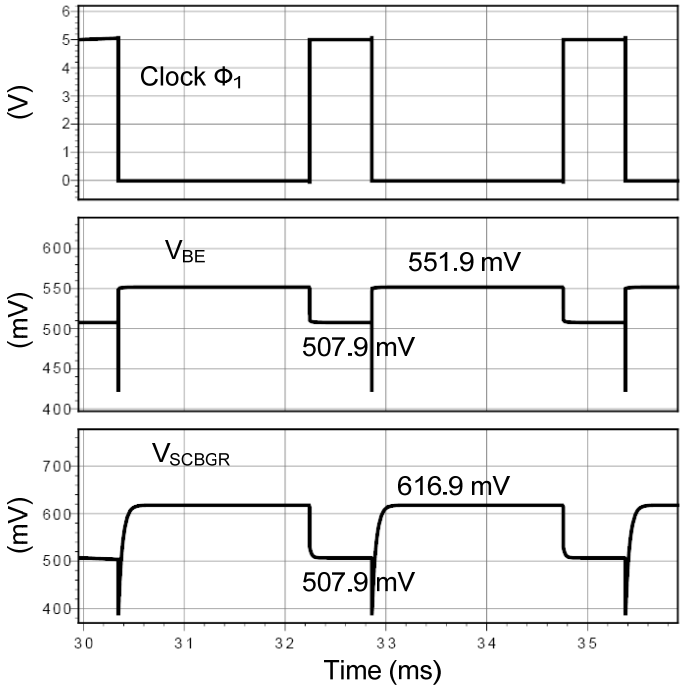

Figure 58 Switched Capacitor Bandgap Functionality with Simulation

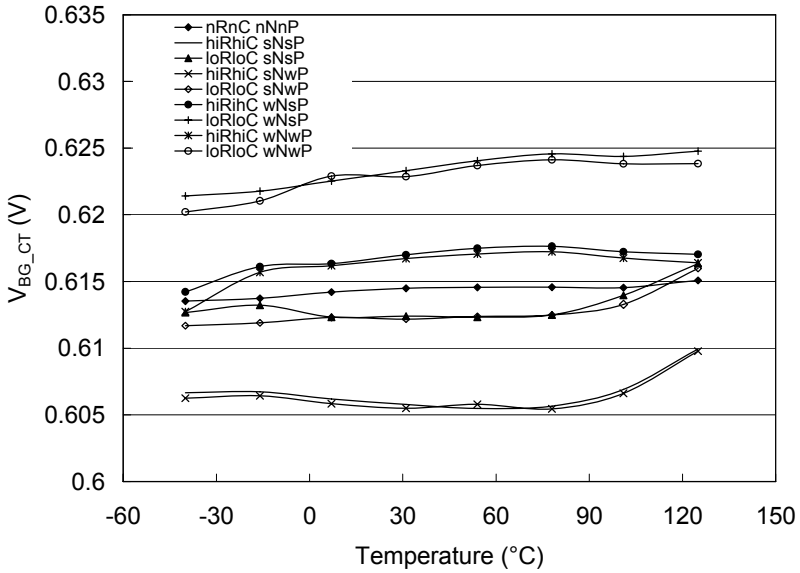

Figure 59 Simulated Bandgap Output Voltage vs. Temperature with 9 Process Corners

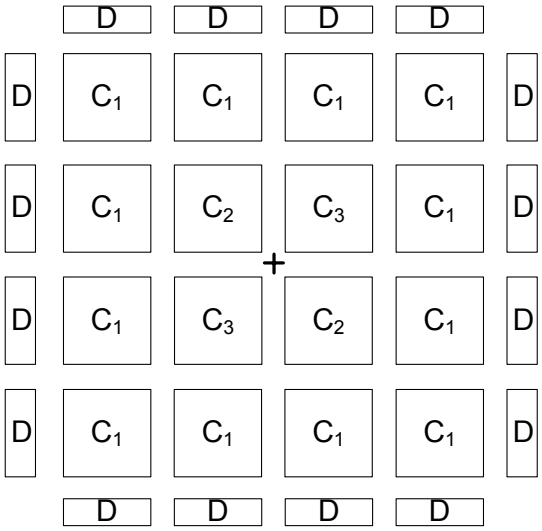

Figure 60 Arrangement of Matched Capacitors in Switched Capacitor Bandgap Core

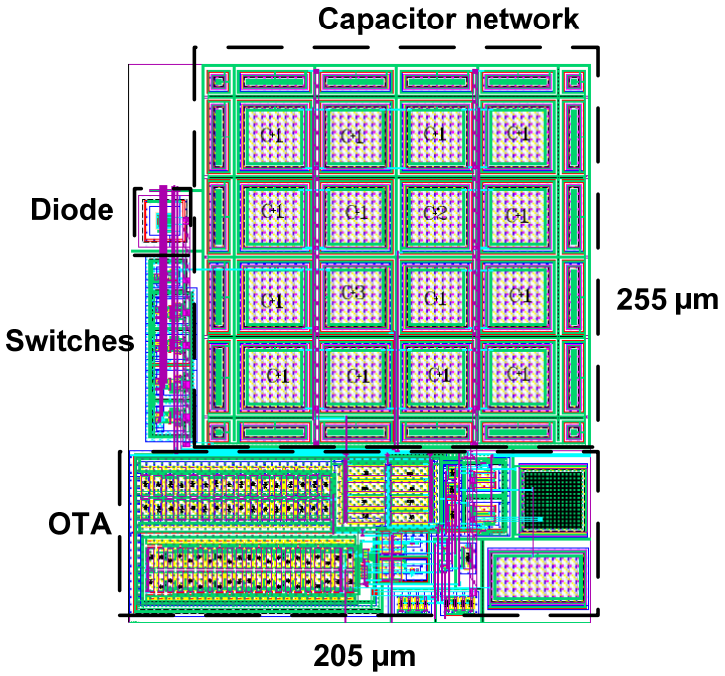

Figure 61 Layout of Switched Capacitor Bandgap Core

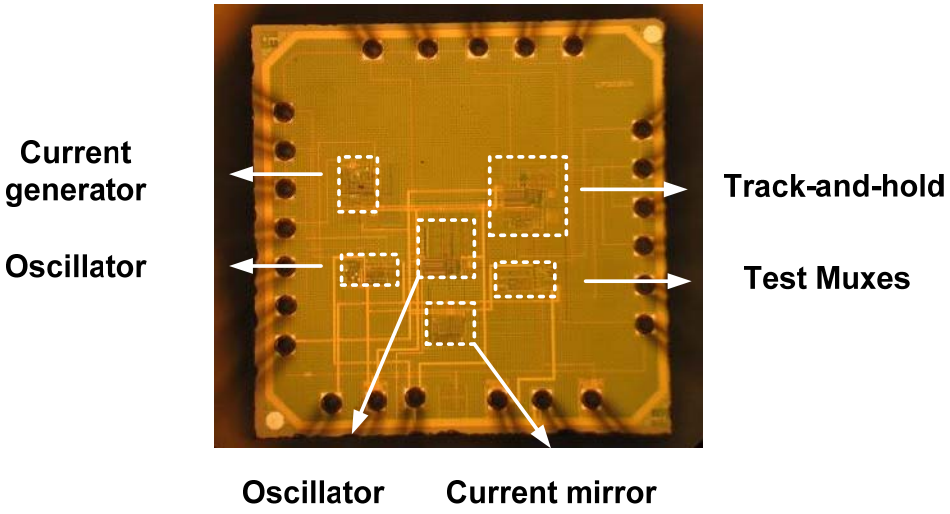

Figure 62 Chip Photo

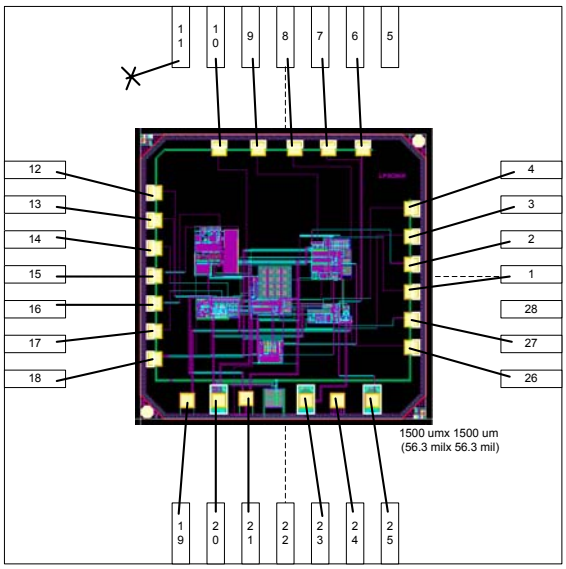

Figure 63 Bonding Diagram for 28-pin DIP Package

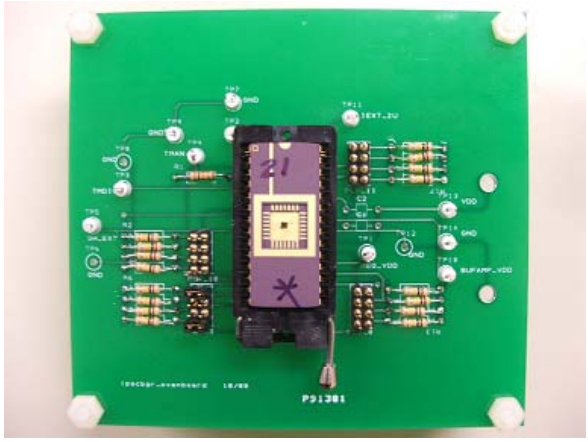

Figure 64 PCB Board for Room Temperature Tests

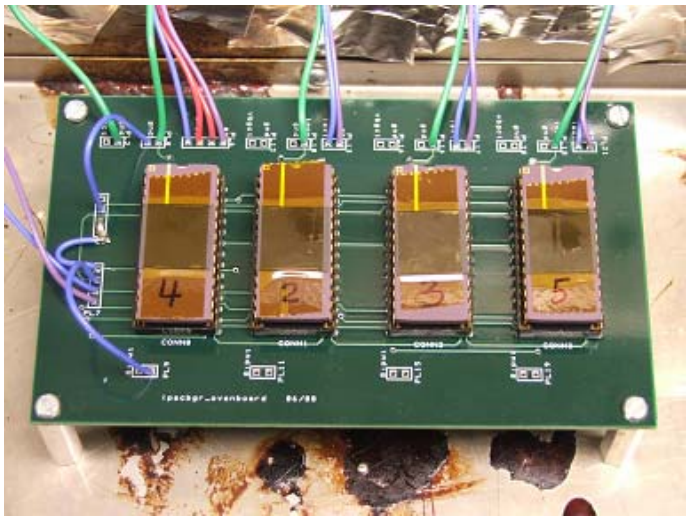

Figure 65 PCB Board for Temperature Tests

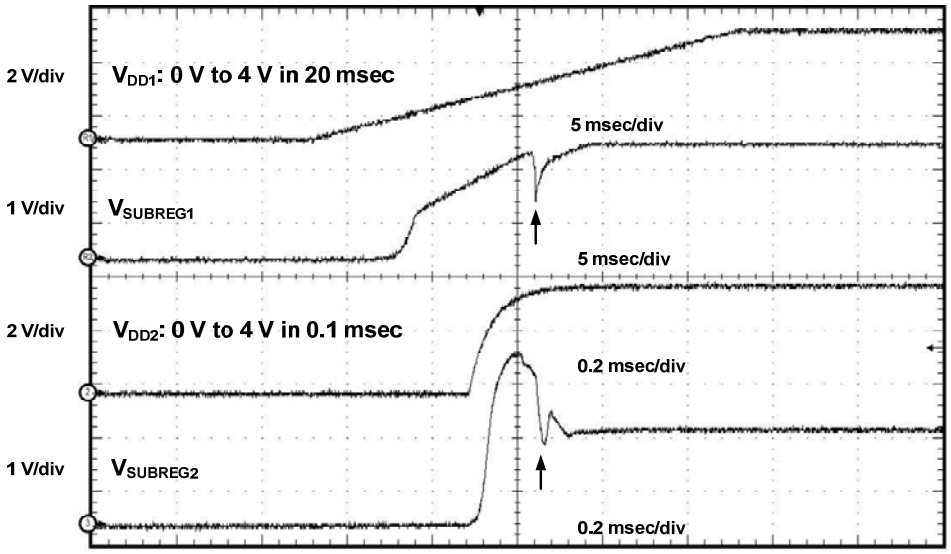

Figure 66 Current Generator Start-up: Measured V_{SUBREG} when supply is turned on

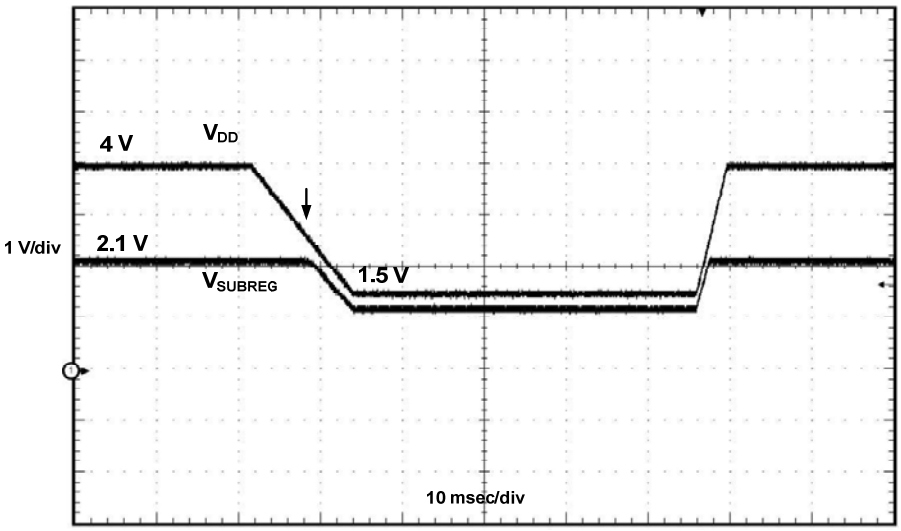

Figure 67 Current Generator Start-up in Brownout Condition: measured V_{SUBREG} before and after brownout on V_{DD}

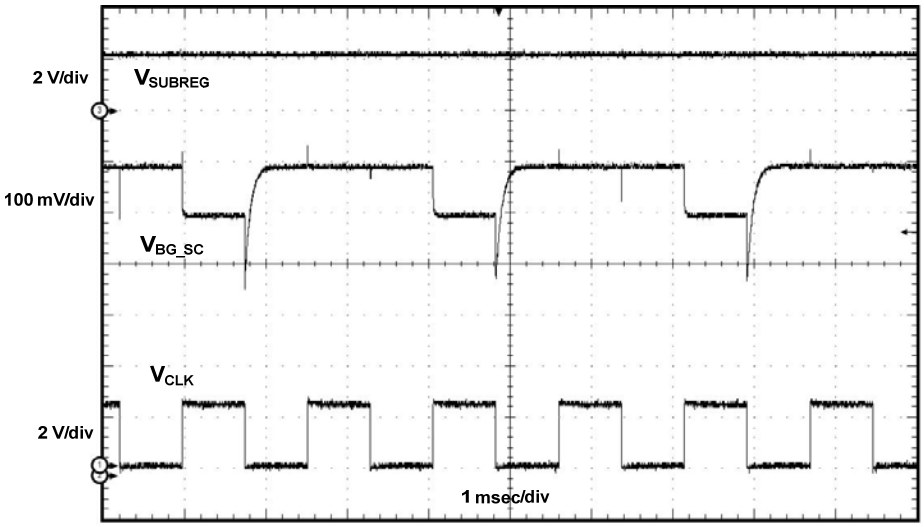

Figure 68 Switched Capacitor Bandgap Discrete-time Output

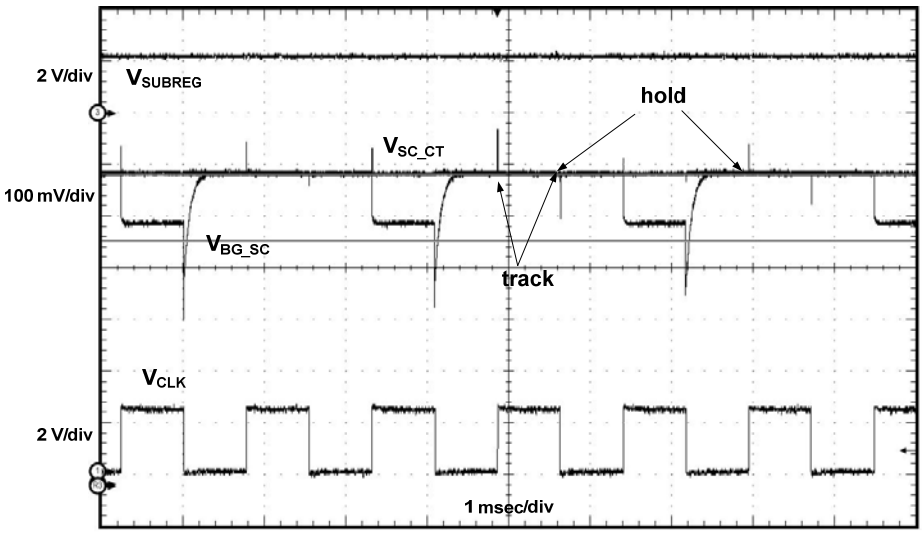

Figure 69 Switched Capacitor Bandgap Discrete and Continuous-time Output

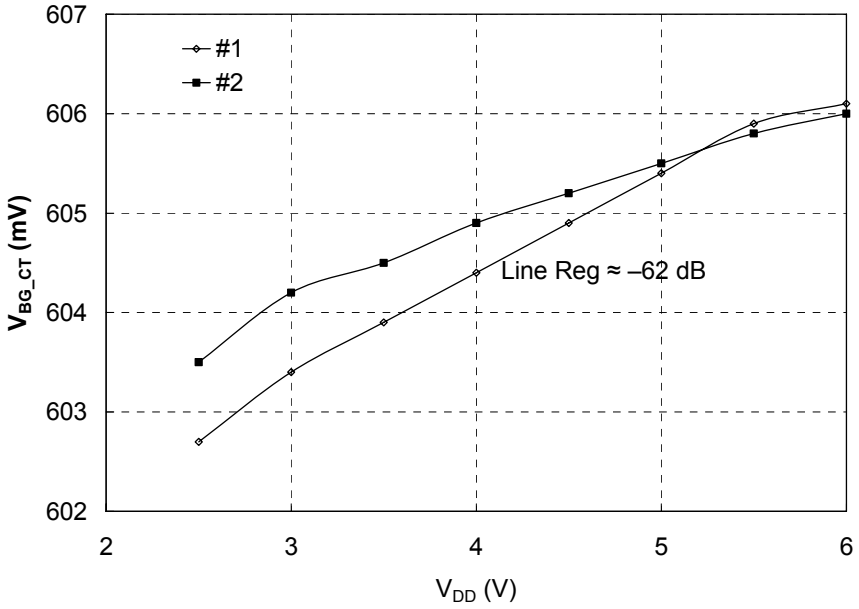

Figure 70 Bandgap DC Line Regulation: measured V_{BG_CT} vs. V_{DD} on 2 DUT samples

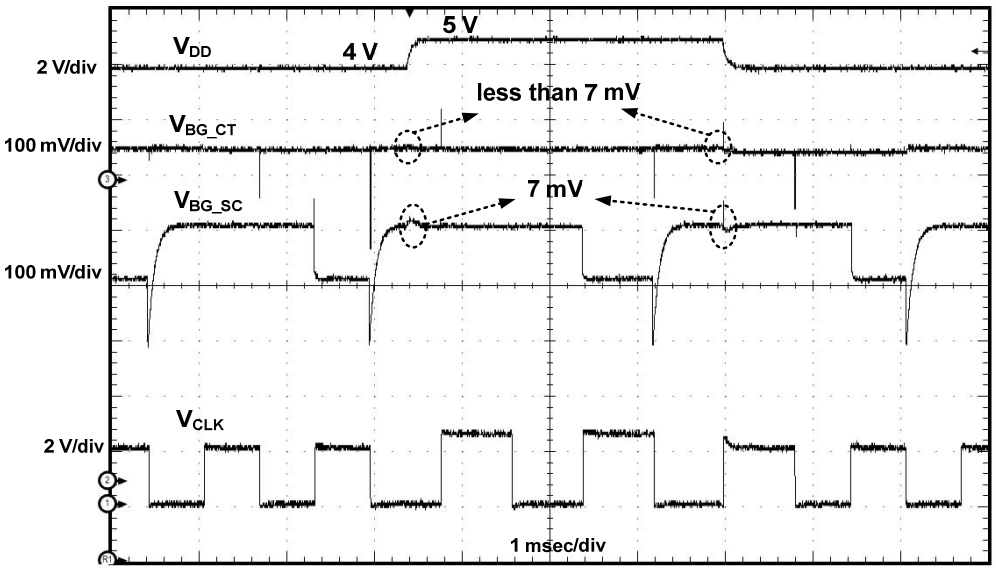

Figure 71 Bandgap Outputs with Supply Line Step: measured V_{BG_SC} and V_{BG_CT} with 1-V step on V_{DD}

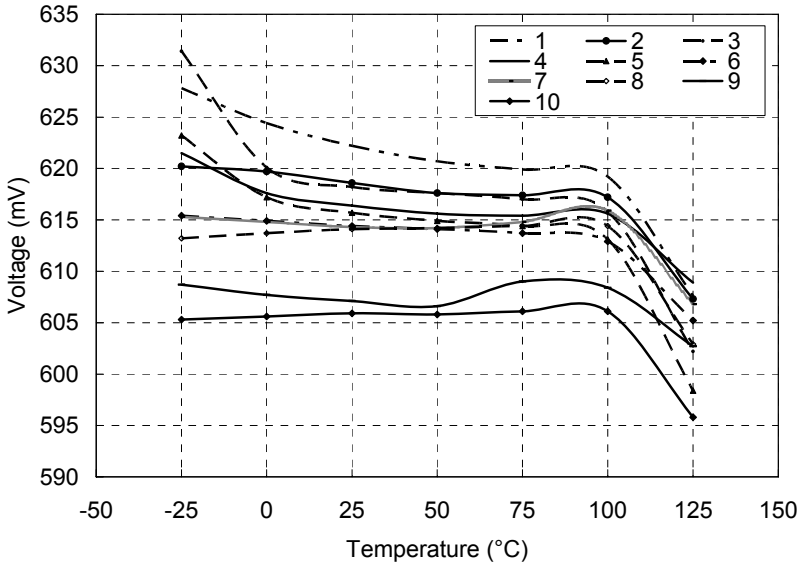

Figure 72 Bandgap Output Voltage vs. Temperature

Measured V_{BG_CT} from –25 °C to 125 °C with 10 samples

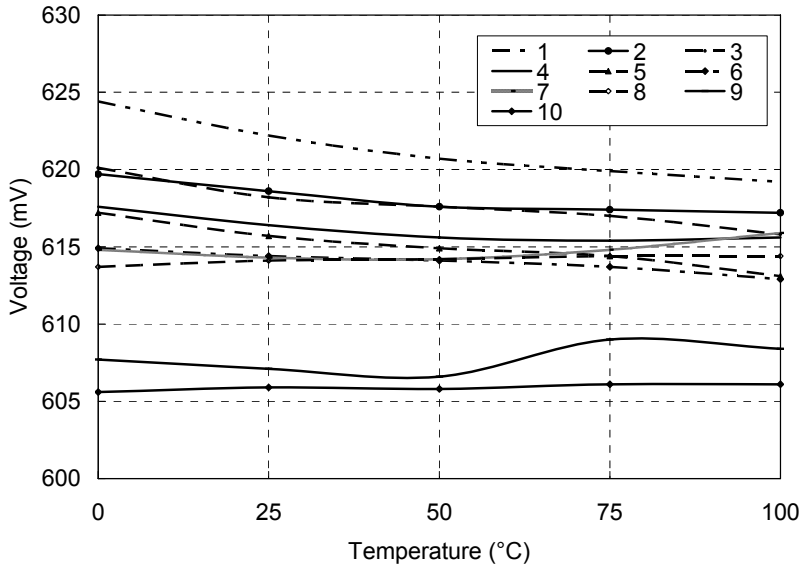

Figure 73 Bandgap Output Voltage vs. Temperature excluding –25 °C and 125 °C data

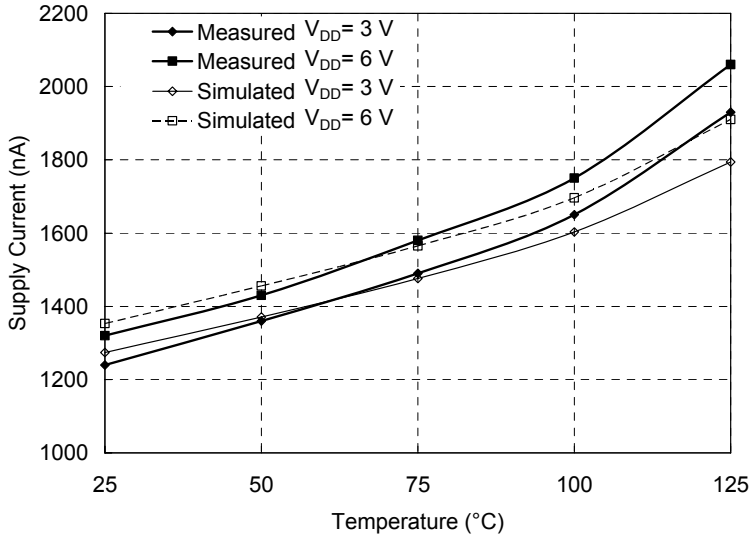

Figure 74 Total Supply Current vs. Temperature with V_{DD} of 3 V and 6 V

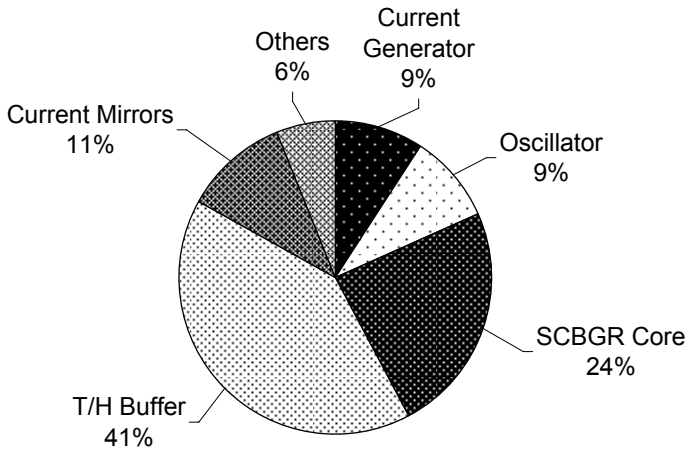

Figure 75 Supply Current by Circuit Block Estimated with Simulation

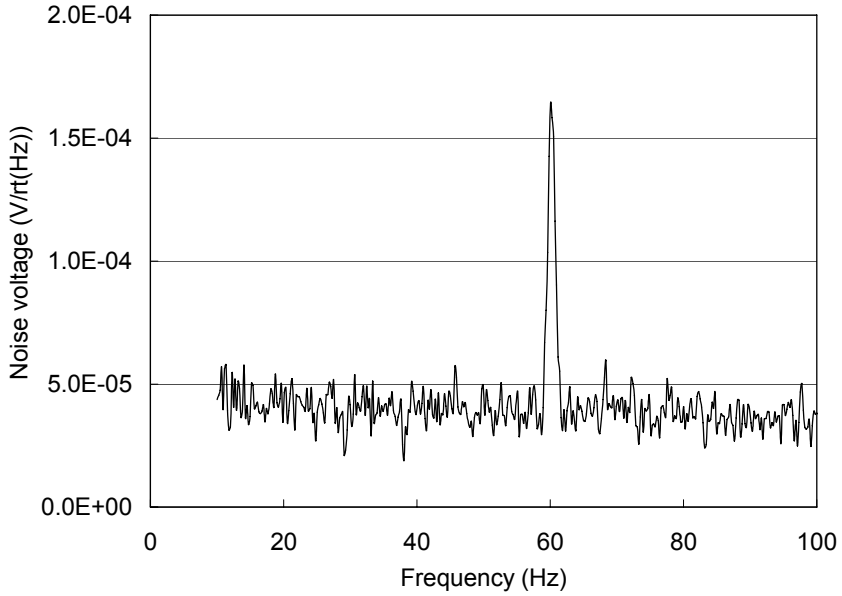

Figure 76 Switched Capacitor Bandgap Output Noise

Measured V_{BG_SC} output noise spectrum from DC to 100 Hz

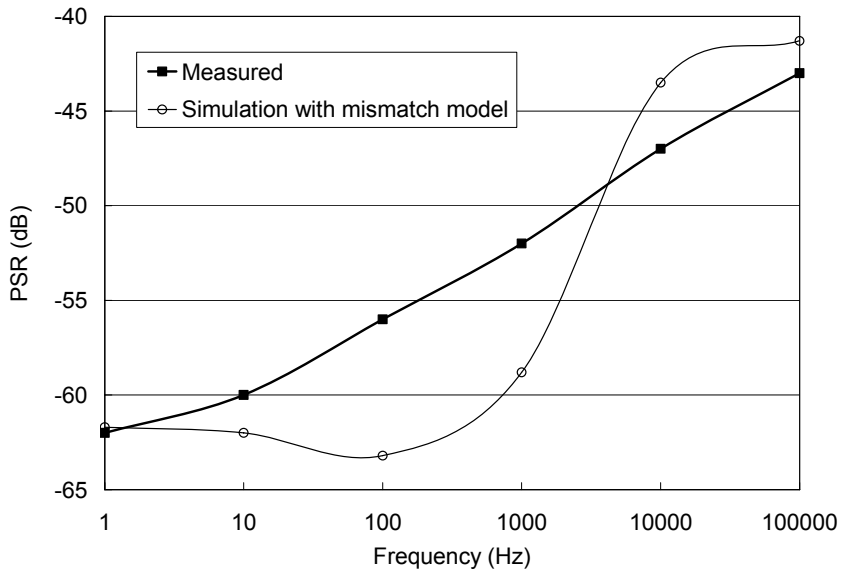

Figure 77 Switched Capacitor Bandgap Supply Rejection

Measured on V_{BG_SC} from DC to 100 kHz

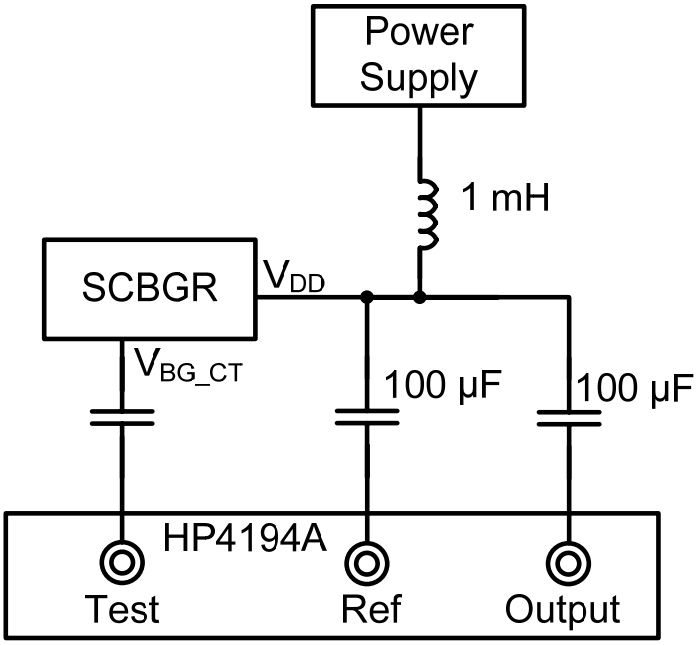

Figure 78 Test Setup for Measuring Supply Rejection

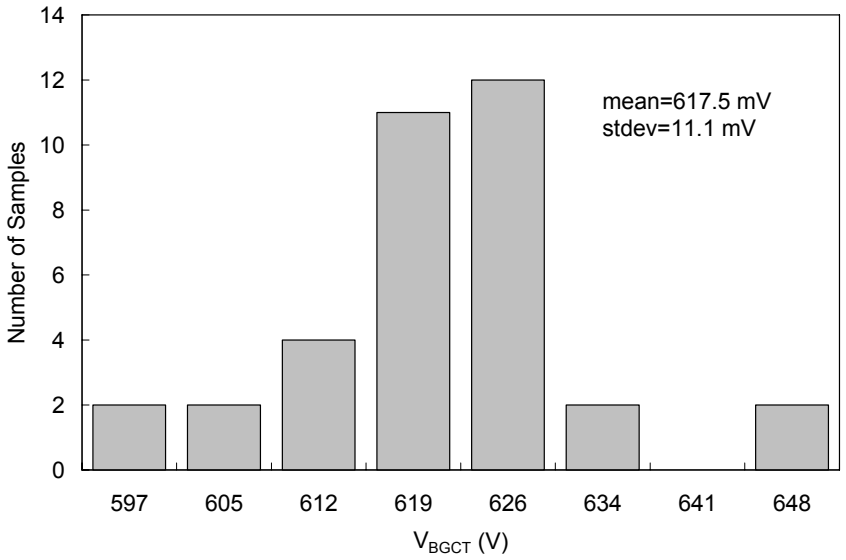

Figure 79 Bandgap Output Voltage Distribution

Measured V_{BG_CT} at room temperature for 35 samples

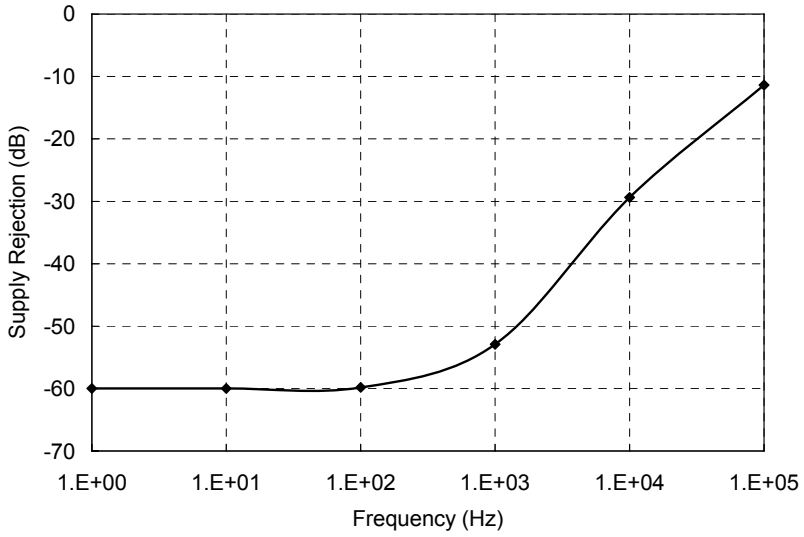

Figure 80 Sub-regulator Supply Rejection

Measured V_{SUBREG} vs. frequency

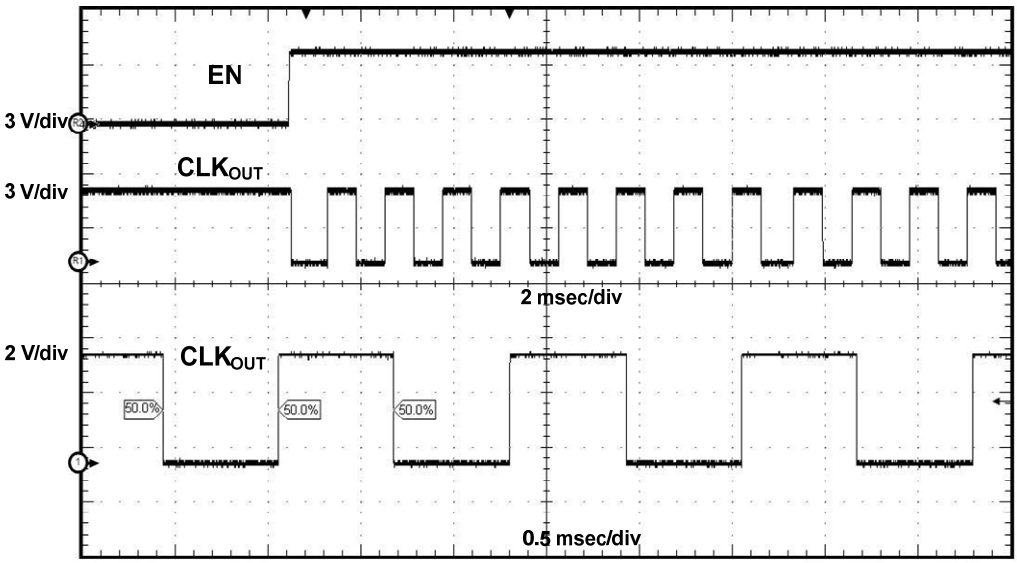

Figure 81 Oscillator Functionality

Measured CLK_{OUT} before and after enabling oscillator

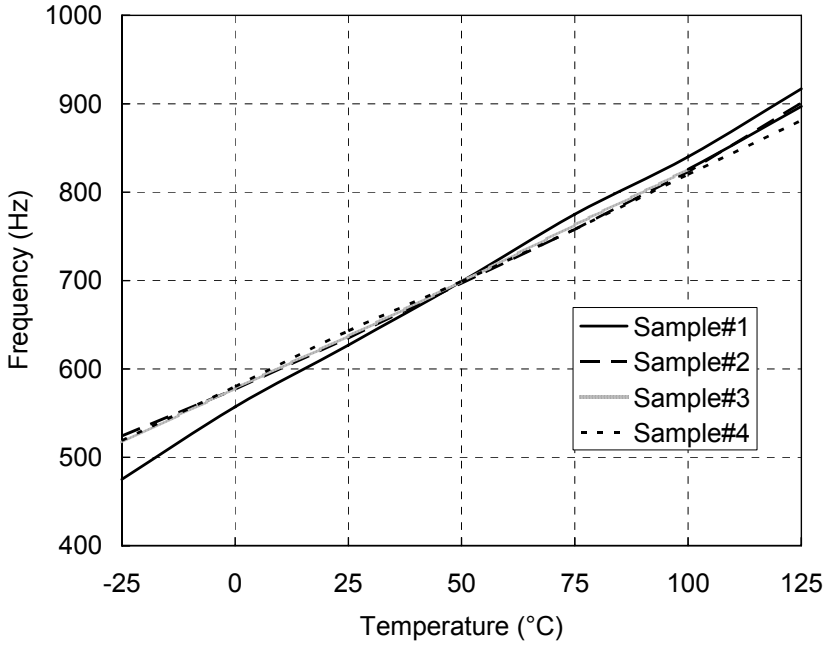

Figure 82 Oscillator Frequency vs. Temperature

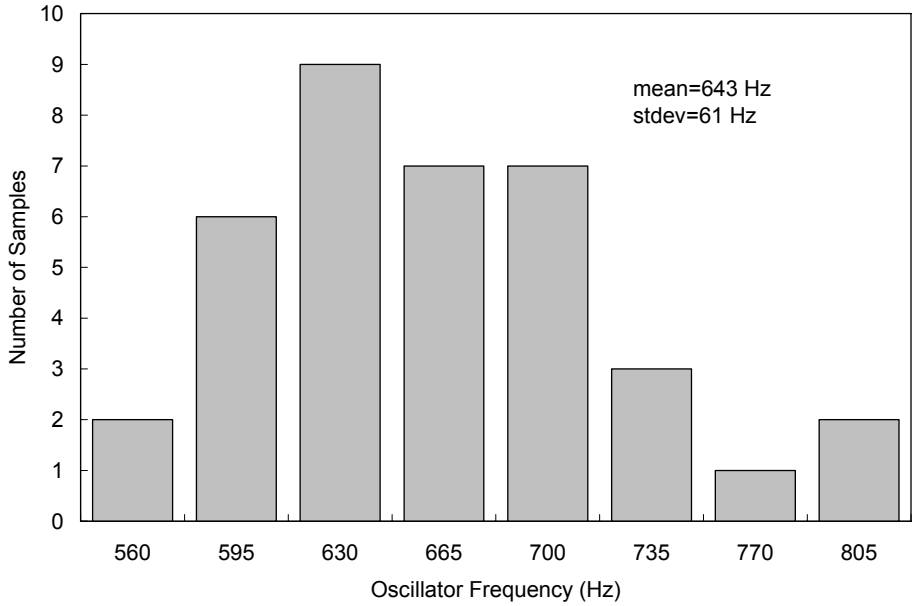

Figure 83 Histogram of Oscillator Frequency

Measured on 37 samples

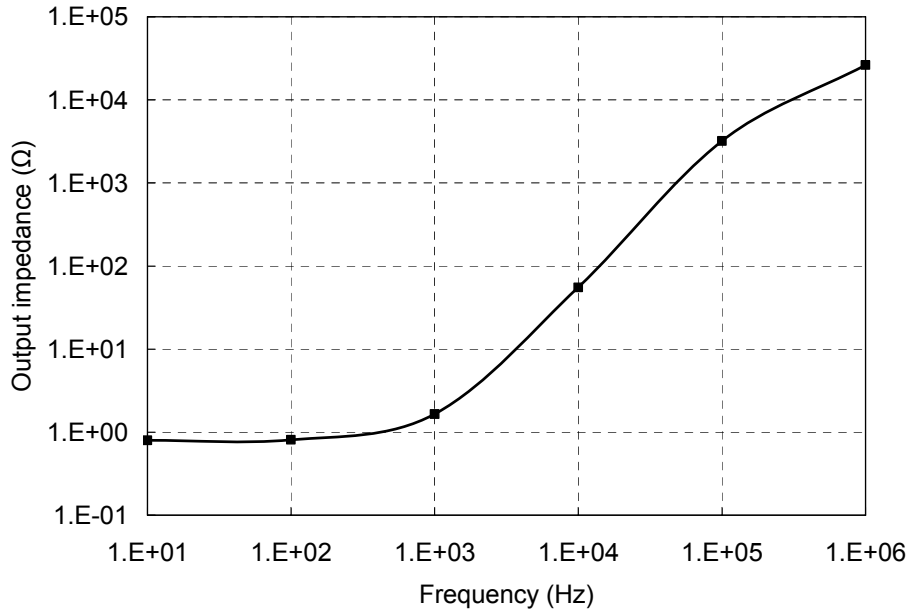

Figure 84 Low-Z_{OUT} Buffer Output Impedance vs. Frequency

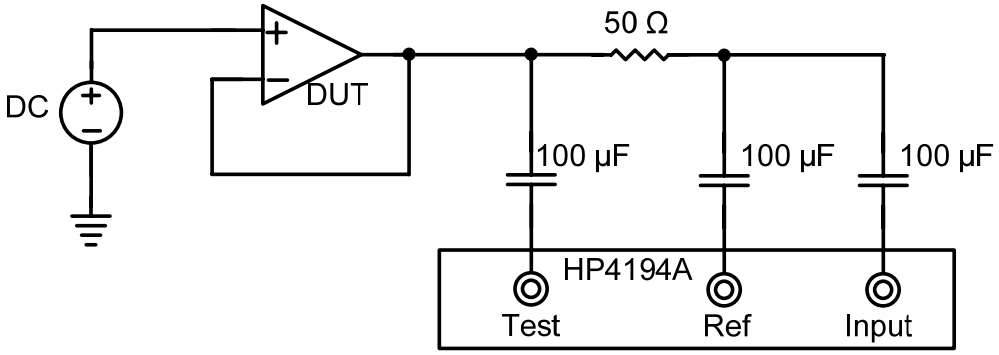

Figure 85 Test Configuration for Measuring Op-amp Closed-Loop Output Impedance

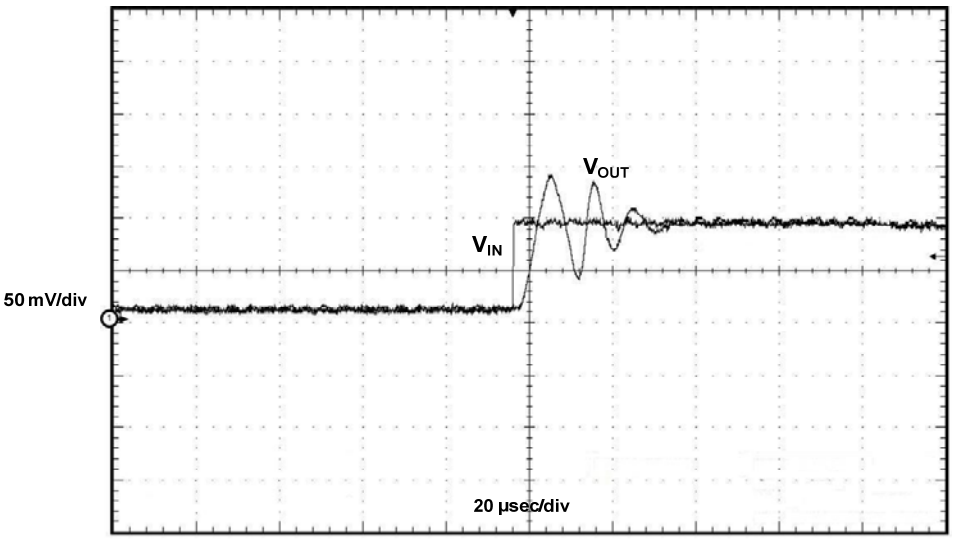

Figure 86 Op-amp Small-Signal Step Response Rising Edge

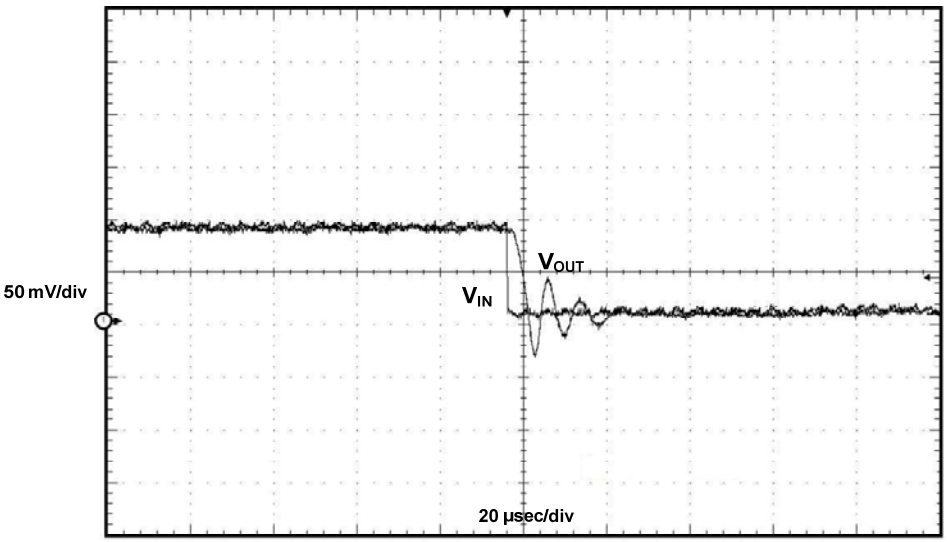

Figure 87 Op-amp Small-Signal Step Response Falling Edge

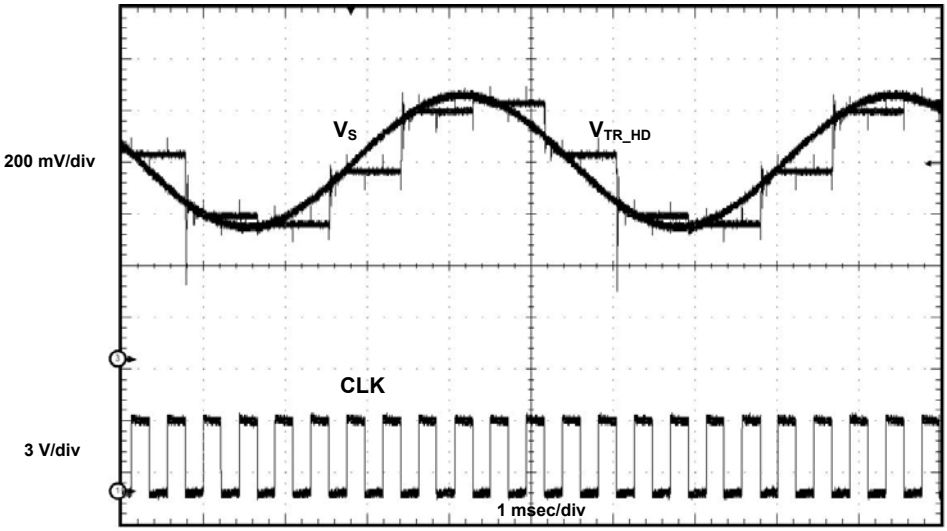

Figure 88 Track-and-hold Functionality

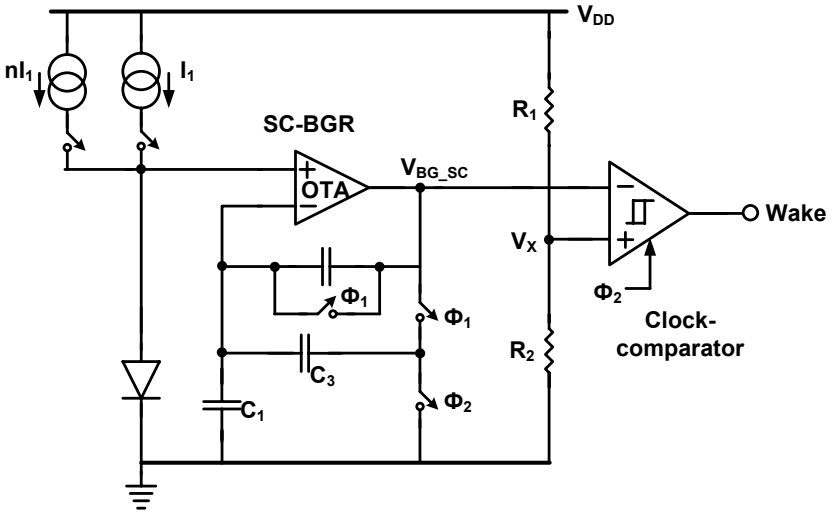

Figure 89 Simplified Diagram of a Supply Supervisory Circuit

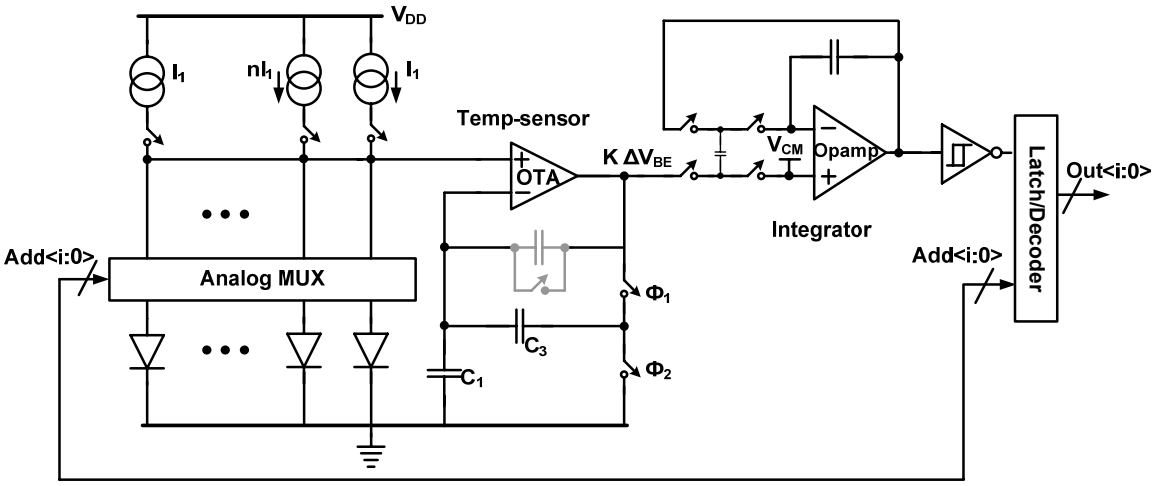

Figure 90 Simplified Diagram of a Thermal Regulation System

APPENDIX B: TABLES

Table 1 Key Device Characteristics

	n	I_O	g_m	λ	f_T
Nominal	1.8	1.5 n	460 n	0.2	350 kHz
Strong	1.6	1.7 n	510 n	0.2	370 kHz
Weak	1.9	1.4 n	420 n	0.2	330 kHz

Table 2 Device Sizes of Current Generator

pMOS	Sizes (W/L)	nMOS	Sizes (W/L)
M_{P1}, M_{P2}, M_{P9}	16/15	M_{N1}, M_{N2}, M_{N7}	32/15
M_{P3}, M_{P4}	8/12, 16/12	$M_{N3\text{-}4}$, M_{N6}, $M_{N8\text{-}9}$	10/10
M_{P5}, M_{P6}	32/15, 8/15	M_{N5}	20/10
M_{P7}	8/12	M_{N10}	4/10
M_{P8}	4/10	M_{N11},M_{N12}	6/4, 240/4

Table 3 Device Sizes of OTA

pMOS	Sizes (W/L)	nMOS	Sizes (W/L)
M_{P1}, M_{P2}	64/8	M_{N1}, M_{N2}	54/8
M_{P3}, M_{P4}	16/0.5	M_{N3}, M_{N4}	12/0.5
M_{P5}, M_{P6}	20/16	M_{N5}	0.9/0.4
M_{P7}	0.9/0.4	M_{N6}	1/0.5

Table 4 Device Sizes of OTA Tail Current Source

pMOS	Sizes (W/L)	nMOS	Sizes (W/L)
M_{P1}, M_{P2}, M_{P9}	16/15	M_{N1}, M_{N2}, M_{N7}	32/15
M_{P3}, M_{P4}	8/12, 16/12	M_{N3-4}, M_{N6}, M_{N8-9}	10/10
M_{P5}, M_{P6}	32/15, 8/15	M_{N5}	20/10
M_{P7}	8/12	M_{N10}	4/10
M_{P8}	4/10	M_{N11},M_{N12}	6/4, 240/4

Table 5 Device Sizes of Low-Z_{OUT} Buffer

pMOS	Sizes (W/L)	nMOS	Sizes (W/L)
M_{P1}, M_{P2}	80/12, 8/12	M_{N1}	60/2
M_{P3}, M_{P4}	16/2	M_{N2}, M_{N5}	6/10
M_{P5}	200/10	M_{N3}, M_{N4}	12/10
C_1, C_2	1 pF, 5 pF	M_F	120/2

Table 6 Pin Diagram on DIP-28 Package

Pin #	Pin Name	I/O	Description
1	VBG_CT	O	Continuous-time reference output without buffer amp, when #2= VDD; high-Z when #2= 0 V.
2	VBGCT_INT_BUFZ	I	Control bit. When high, output of track-and-hold is directly sent out, without buffer amp; when low, output
3	TM_AN	O	Output of analog test buffer.
4	TM_DIG	O	Output of digital buffer.
5	N/C		
6	ADDR_TMDIG<0>	O	Digital buffer select bit 0.
7	ADDR_TMDIG<1>	O	Digital buffer select bit 1.
8	SH_EXT	I	External input of track-and-hold amplifier, for test purpose.
9	SH_INT_EXTZ	I	Control bit. When high, track-and-hold takes internal input, which is output of switched capacitor bandgap; when low, track-and-hold takes external input (#8).
10	CLK_INT_EXTZ	I	Control bit. When high, system takes internal generated clock; when low, system runs on external clock (#14).
11	SUBC	I	Electrical contact of package cavity.
12	ADDR_CLKFREQ<0>	I	Clock frequency tune bit 0. When high, output clock frequency is lower.
13	ADDR_CLKFREQ<1>	I	Clock frequency tune bit 1. When high, output clock frequency is lower.
14	EXT_CLK	I	External clock input.
15	TMPTRIM_IRATIO<1>	I	Address bit 1 for trimming bandgap TC.

Table 6 Cont. Table Pin Diagram on DIP-28 Package

Pin #	Pin Name	I/O	Description
16	TMPTRIM_IRATIO<0>	I	Address bit 0 for trimming bandgap TC.
17	EN	I	Enable bit for oscillator.
18	REG_VDD	I/O	Regulated supply.
19	TESTCIR_GND	I	Ground of analog and digital test buffer.
20	AVDD	I	Supply for all circuitries, except analog and digital test buffer.
21	AGND	I	Common ground for all circuitries, except analog and digital test buffer.
22	N/C		
23	BUFAMP_AVDD	I	Supply for analog test buffer.
24	PBKG	I	Back gate contact of IC.
25	IEXT_2U	I	2 μA bias current input for buffer amplifier, for test purpose.
26	ADDR_TMAN<0>	I	Address bit 0 for programming analog test buffer.
27	ADDR_TMAN<1>	I	Address bit 1 for programming analog test buffer.
28	N/C		

Table 7 Variation of Oscillator and Bias Current Variation

Sources of Variation	Mean	Std. Dev.
Oscillator with bias current (measured)	643 Hz	61 Hz
Oscillator with bias current (simulated)	633 Hz	83 Hz
Bias current (simulated)	10.83 nA	1.44 nA
Oscillator (simulated)	631 Hz	19 Hz

VITA

Suheng Chen was born in Fuzhou, China on January 17, 1979. He attended Fuzhou No.3 High School and Fuzhou University. Suheng received the Bachelor of Science in Computer Engineering from Fuzhou University in 2001, focusing on computer architecture and digital design. In 2004, Suheng received the Master of Science degree in Electrical Engineering at the University of Tennessee, focusing on analog/mixed-signal IC design. During his master's study, Suheng worked as a graduate research assistant in ICASL (Integrated Circuits and Systems Laboratory), led by Dr. B. J. Blalock.

Since 2004, Suheng has continued his graduate study at the University of Tennessee and research assistantship at ICASL while pursuing the Doctor of Philosophy degree under the advisement of Dr. B. J. Blalock. During his Ph.D. work, Suheng participated in and led a wide range of research projects at ICASL, including research that led to an analog multiplier and high-voltage amplifier using an innovative four-gate transistor (G^4-FET) for Silicon-On-Insulator (SOI) CMOS; a SiGe BiCMOS voltage and current reference, as well as low-power high-speed counter, all for a 12-bit Wilkinson ADC targeting wide temperature and cryogenic applications; and a switched-capacitor low-power bandgap reference. This effort resulted in ten conference publications, two journal publications, and two U.S. patents. Suheng also co-authored proposals for the research of his switched-capacitor voltage reference and said research was funded by CDADIC (Center for Design of Analog-Digital Integrated Circuits) for two continuous years, 2005 and 2006.

During Suheng's graduate study, he worked with Agere Systems, in Longmont, Colorado in the Summer of 2005 and worked with Texas Instruments, in Knoxville, Tennessee in the Spring of 2007. In June 2007, Suheng joined the Battery Charge Management group of Texas Instruments at its Knoxville design center.

Suheng is a member of IEEE and Eta Kappa Nu. He is also a martial-art enthusiast, and currently holds the rank of third-degree brown belt in Jujitsu.

Suheng is married to Chunlei Zhang, M.B.A.