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Characterization of a 12-bit pipeline analog to digital converter

Saeed Ramzi Ghezawi
University of Tennessee

To the Graduate Council:

I am submitting herewith a thesis written by Saeed Ramzi Ghezawi entitled "Characterization of a 12-bit pipeline analog to digital converter." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Benjamin J. Blalock, Major Professor

We have read this thesis and recommend its acceptance:

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

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Syed K. Islam

Leon M. Tolbert

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Characterization of a 12-Bit Pipeline Analog to Digital Converter

A Thesis

Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

Saeed Ramzi Ghezawi

May 2009

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Abstract

This thesis presents the characterization of the 12-bit pipeline analog-to-digital converter (ADC) designed by Mark Hale, Ph.D. graduate from the University of Tennessee. An overview of the pipeline ADC architecture is discussed first, and then the specifics of the testing procedure and results are detailed. The differential nonlinearity (DNL), integral nonlinearity (INL), DC offset error, and gain error for the pipeline ADC are the DC characteristics of interest. The DC characterization was performed in order to analyze the linearity of the ADC output over the analog input range. Additionally, the DNL and INL results were used to determine if the ADC exhibited undesirable effects, such as missed codes.

The characterization was performed at room temperature using differential sinusoidal inputs. Labview was utilized to efficiently gather the digital output levels of the ADC, and Matlab was employed to compute the characteristics of the tested ADC.

During the testing process several difficulties were encountered. Characterization results were negatively impacted by the presence of noise both at the output of the sample-and-hold and on the supply rails. Through iterative testing, the results improved. However, the effective number of bits for the tested ADC did not attain the desired 12-bits.

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Chapter 1 Introduction

1.1 Function of Analog-to-Digital Converters (ADC)

With the increasing popularity of digital circuitry in today's marketplace, analog-to-digital converters (ADCs) are becoming a core area for analog designers to find employment. All real world signals are analog by nature. Thus, a need exists for analog signals to be quantized into discrete digital signal levels that are readily understandable by digital systems. This process reduces the inherent noise of the input signal, but also introduces quantization error, which is commonly called quantization noise. Figure 1.1 shows the effects of data conversion between the analog and digital domains. First, the analog signal is passed through a low pass filter (LPF) to remove spurious noise from the input. Next, the filtered input is sampled and held. At this point an ADC is employed to digitize the analog voltage, which produces a digital code output. Often it is necessary to take a digital signal back to the analog domain to interface with peripheral devices. A digital to analog converter (DAC) is employed for this task. However, the analog output, as shown in Figure 1.1c, exhibits the aforementioned quantization noise. Another

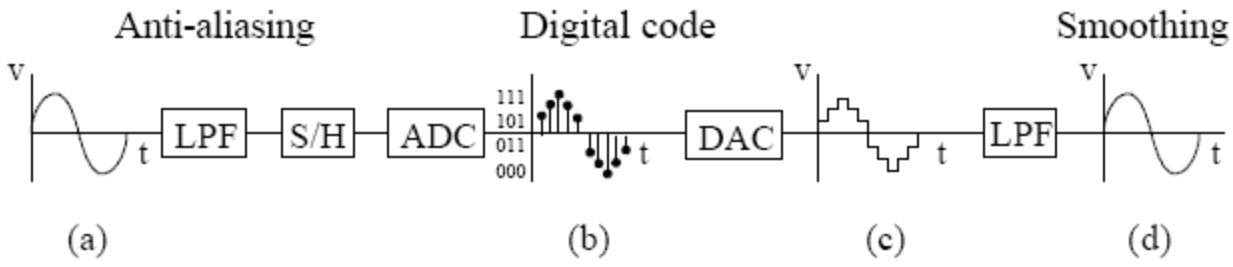

Figure 1.1 Analog-to-digital (AD) and digital-to-analog (DA) block diagram example

(a) Analog signal. (b) Quantized analog signal (c) Reconstructed analog signal showing quantization error (d) Reconstructed analog signal with quantization error filtered out [1].

LPF is employed to smooth out the signal. Theoretically, the analog signal in Figure 1.1a and 1.1d are identical. The linearity of the ADC and DAC and the sampling frequency will determine how closely the signals match.

Sampling theory states that in order to faithfully reproduce an analog signal that has been quantized, the sampling rate used by the sample-and-hold circuitry must be a minimum of two times greater than the highest frequency component found in the input analog signal, which is called the Nyquist Frequency or Nyquist Criterion [1]. As the sampling rate and number of samples increases, the accuracy of the ADC increases. Therefore, accuracy of an ADC depends both on the number of bits it can output and the sampling rate used by the sample-and-hold circuit.

The quantity of discrete output levels an ADC is capable of producing will ultimately determine the magnitude of the quantization error. The more discrete levels that are available, the less quantization error will be added to the analog signal.

The effect of quantization error can be easily viewed in the lower bit count ADCs. The effect manifests itself as a stair step pattern, as shown in Figure 1.1c. The more quantization levels an ADC can produce, the smaller the steps will become. For higher bit ADCs the steps can be too small to view without magnifying the voltage characteristic curve.

A designer must be cautious when selecting the number of bits and sampling frequency. As the number of desired bits increases, the ADC must discriminate between smaller voltage changes from the incoming input signal, assuming the ADC reference voltage remains constant.

The primary limitations will be noise, the linearity of the ADC, and DC offsets introduced by the circuits comprising the ADC. A critical point exists where the signal level will be overcome by the noise level. This is the reason a low pass filter (LPF) is placed at the input of

the ADC. The LPF limits the bandwidth of the ADC, which reduces the input noise. Fortunately, all implementations of sample-and-hold circuits provide a partial ability to filter higher frequencies. However, the corner frequency of the sample-and-hold may exceed the requirements for the desired input signal frequency range.

1.2 Thesis Organizational Overview

The remainder of this thesis is comprised of four chapters. Chapter 2 discusses the pipeline ADC design architecture, the ideal characteristics for an ADC, and the non-idealities found in all ADCs. All characterization parameters measured in this thesis will be explained and discussed.

Chapter 3 describes the procedure used to characterize the ADC. The LabView and Matlab code used to conduct the characterization will be discussed in full detail. Additionally an overview of the test board and its operation will be detailed. Finally, the problems encountered during the characterization testing will be discussed along with some possible solutions.

Chapter 4 analyzes the data obtained from the test procedure. The raw data collected is converted into meaningful plots that show the various characterization parameters and discusses how each parameter is determined.

Chapter 5 concludes the thesis. It summarizes the characteristics of the ADC tested. This chapter also proposes future work and research yet to be completed.

Chapter 2 Fundamental Pipeline ADC Theory

2.1 High Level Design of Pipeline ADC

Several circuit topologies exist that are used to create ADCs, but since the ADC characterized in this thesis is a pipeline ADC, that is the only topology discussed. Figure 2.1 shows a generic block diagram representation of a pipeline ADC. For this simple block diagram, the number of stages in a pipeline ADC is equal to the number of bits it can output.

The generic pipeline ADC architecture works by first sampling the input signal. An amplified quantization error of each stage's output is being used as the next stage's input [8]. For a pipeline architecture this signal is called the residue [7]. The sample and hold circuits serve the purpose of isolating the individual stages so each stage can operate independently on the residue of the prior stage [9]. The sampled input is then compared to half the reference voltage. The comparator acts as a 1 bit ADC. This portion of the pipeline architecture can be replaced by any N-bit ADC. However, the optimal conversion speed is realizable when the bit resolution per

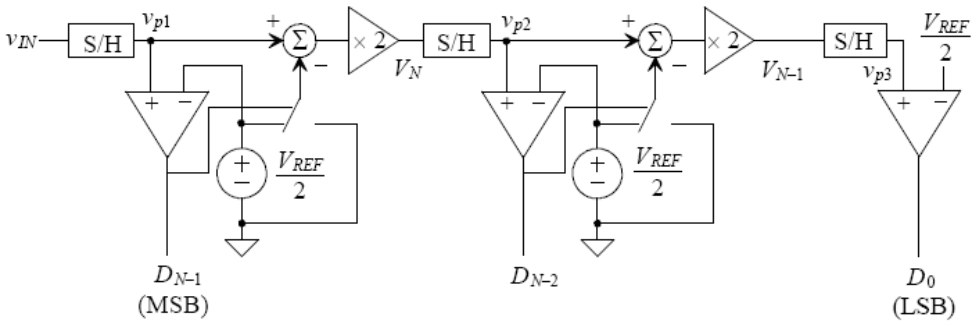

Figure 2.1 Pipeline ADC block diagram

The pipeline ADC is comprised of cascaded blocks consisting of a sample and hold, comparator (Sub-ADC), summer, and gain block [1].

stage is minimized [9]. The reason the conversion speed peaks for lower resolution per stage is because the interstage gain can be minimized due to the larger quantization error from a lower resolution sub-ADC [10]. The lower interstage gain translates into faster settling time, thus faster conversion rates [10]. Yet, the optimal linearity of the ADC is achieved when the bit resolution per stage is maximized [9]. The designer must carefully consider the trade-off between conversion speed and linearity while determining the bit resolution per stage [9]. However, the trade-off can effectively be eliminated with the introduction of digital correction [11]. By selecting the minimum bit resolution per stage, including digital correction, not only is the conversion rate maximized, but the die area and power dissipation are minimized [11]. The linearity of the ADC will suffer, but with digital correction the effect can be minimized as long as the interstage gain is no less than two [11]. Therefore, it is commonplace for designers to select 1.5 bits per stage, which is the minimum bit resolution per stage with the inclusion of digital correction techniques. The number of stages implemented and the capability of the ADC incorporated into each stage will determine the maximum number of bits achievable by the pipeline ADC. The output of the first stage's comparator, or lower bit count ADC, is the most significant bit (MSB), or higher bits of the ADC, of the digital output. Next the input is either reduced by half the reference voltage or left at full strength depending on whether the output of the comparator is a logic high or logic low. The subtracted signal will be half the reference voltage if the input voltage for the stage generates a digital high output. Otherwise, the sampled signal is propagated to the next stage's sample-and-hold ideally without any reduction in signal level. The output of the summing junction is then multiplied by two and sent to the next stage, where the same operations are performed again. Keep in mind that if the ADC used in each pipelined stage is greater than a 1 bit ADC, then an equal bit DAC must be implemented to

produce the subtracted signal instead of using a simple switch. This process propagates continually through all the ADC stages until it reaches the final stage. In the final stage the incoming voltage is only compared to half the reference voltage, which outputs the least significant bit (LSB) of the digital output.

The ADC characterized for this thesis is a 12-Bit pipeline ADC. However, the architecture used has been slightly modified to comprise of 10 pipelined stages outputting 1.5 bits per stage and a 2 bit flash ADC, instead of using 12 cascaded stages. One bit is taken from each stage in addition to the 2 bits from the final flash ADC stage. This accounts for the total 12 bits. The 0.5 redundancy bits from each stage are used for digital correction. Two bits are taken from each digitally corrected stage, where one bit is the digital output for the stage and the other bit is used for digital correction. Only three of the four possible 2-bit states are permissible, excluding the case of '11', where both the output bit and digital correction bit are high [10].

The digital correction mitigates the errors introduced by capacitor mismatch, charge injection, and comparator offsets [6]. Other sources of error include gain error from the sample and hold circuits and amplifiers, and the operational amplifier settling time [9]. Digital correction can be implemented with the addition of pipelined latches and a digital correction logic circuit [9].

If the gain of the amplifier used in the sample and hold circuit is high enough, then the linearity error of the ADC is caused only by capacitor mismatches [6]. During normal operation of the ADC, the digital correction signals are added to the output of each calibrated stage [6]. Therefore, a digitally calibrated stage only requires an additional summing circuit [6]. For a pipeline ADC it is not necessary to calibrate all stages, because the accuracy of a pipelined ADC is heavily dependent on the accuracy of the earlier stages [1].

The 1.5 bits per stage pipeline ADC architecture has been shown to exhibit a favorable combination of high speed and low power characteristics [7]. The comparator design constraints for the DC offset and DC gain are relaxed with the presence of digital correction [7] [8] [13]. The comparator can exhibit up to an absolute value of a fourth of the reference voltage range in error before the linearity and the SNR of the ADC are compromised [6] [8] [10] [12]. This is due to the presence of a redundant quantization level in the sub-ADC [8].

The main advantages of using the pipeline ADC architecture are the ability for each stage to operate on the output of the prior stage simultaneously and a reduced silicon area requirement [1] [9].

The simultaneous operations allow for faster conversion rates after the initial conversion latency [1]. However, the sampling rate of a flash ADC architecture typically will outperform any pipelined architecture [9]. The silicon area can be reduced by up to 10 times what would be required for an equivalent bit flash ADC [9]. This area savings comes from requiring fewer comparators in the pipelined architecture [9]. The main disadvantage is having an initial latency that is equal to the number of stages multiplied by the period of a clock cycle [1] and the requirement of parasitic insensitive operational amplifiers for the sample and hold circuits [9]. Depending on the application of the ADC this initial latency may not negatively impact the operation of the ADC [1]. After the initial latency, the ADC will complete one conversion every clock cycle [1] [10]. However, operational amplifiers will be an ultimate limiting factor for the conversion speed of the ADC because it is challenging to design high speed operational amplifiers [9]. Additionally, it is challenging to design high open loop gain operational amplifiers as the supply voltage continues to scale down along with feature size [12]. The error

induced by finite open loop gain is inversely proportional to the magnitude of the open loop gain [12].

It is important to realize the pipeline ADC accuracy is heavily dependent on the accuracy of the earlier stages [1]. If the earlier stages are poorly designed in either the implementation or layout, then the error introduced will continue throughout the remaining stages and compound into a significant error when the conversion is complete [1].

2.2 Ideal Characteristics

The ideal voltage transfer characteristic curve is shown in Figure 2.2. As the analog input increases, the quantization error also increases until the analog input has a magnitude sufficient enough to be interpreted as the next higher digital level. The quantization error is undefined at the point where the analog voltage is exactly equal to the voltage required for a certain digital output. In reality, if any ADC comparators were placed in this region, they would fluctuate between the two digital output states due to the presence of random noise in the signal. This situation would make the ADC unreliable and unpredictable near the transition points. Figure 2.3 depicts how this problem is solved. The staircase voltage transfer curve is shifted by half of a LSB such that the LSB multiples of the analog input are centered on each code step. This reduces the quantization error by 50% in all cases, except where the input voltage goes to the reference voltage level. This is acceptable considering the final ADC step has an undefined width. Additionally, when the input analog voltage is equal to some multiple of LSBs not outside the ADC's reference voltage, the ADC will be able to produce a reliable and stable digital output with the maximum noise margin possible.

The staircase voltage characteristic curve ideally has completely flat quantized states of

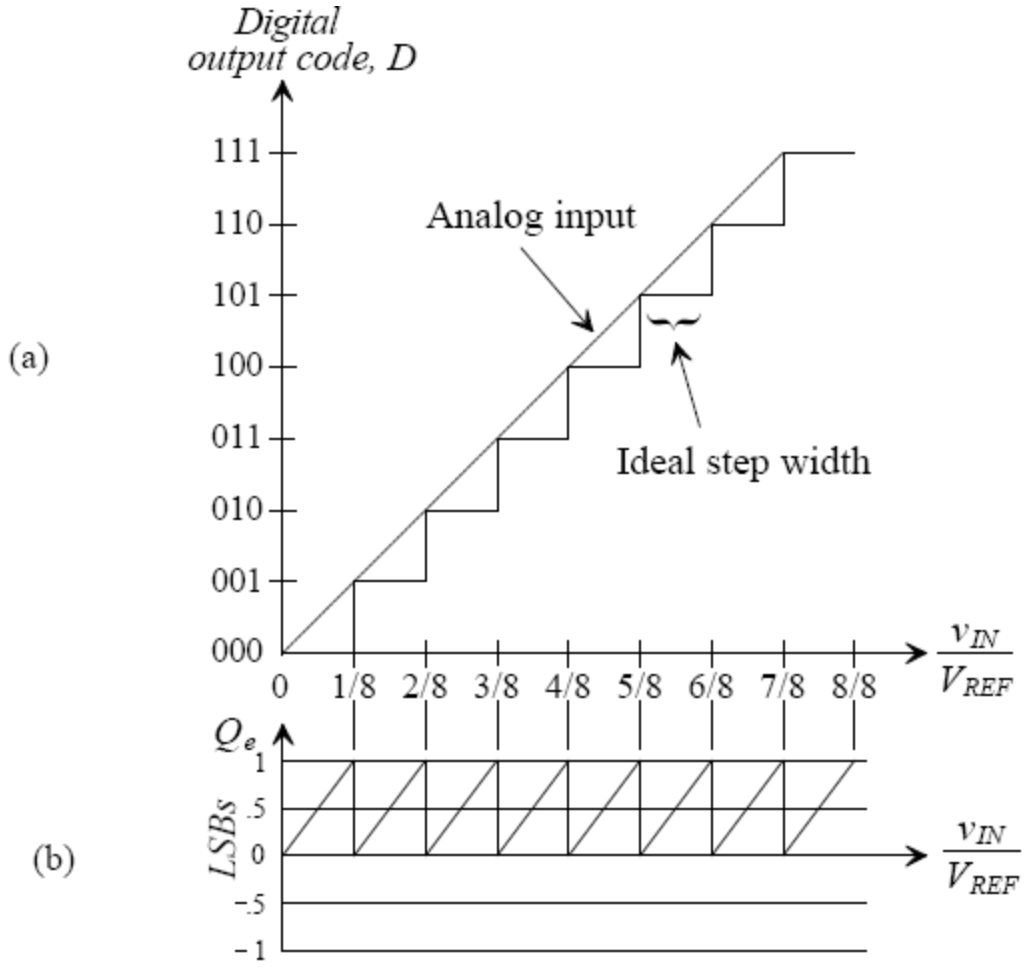

Figure 2.2 Ideal voltage characteristics of a 3-bit ADC

(a) The ideal digital output for a given analog input. The ideal slope of the analog input line is unity. The step widths and heights are ideally equal to one another. (b) The quantization error for a given analog input. As the input approaches a new quantization level, the error increases to a maximum of 1 LSB [1].

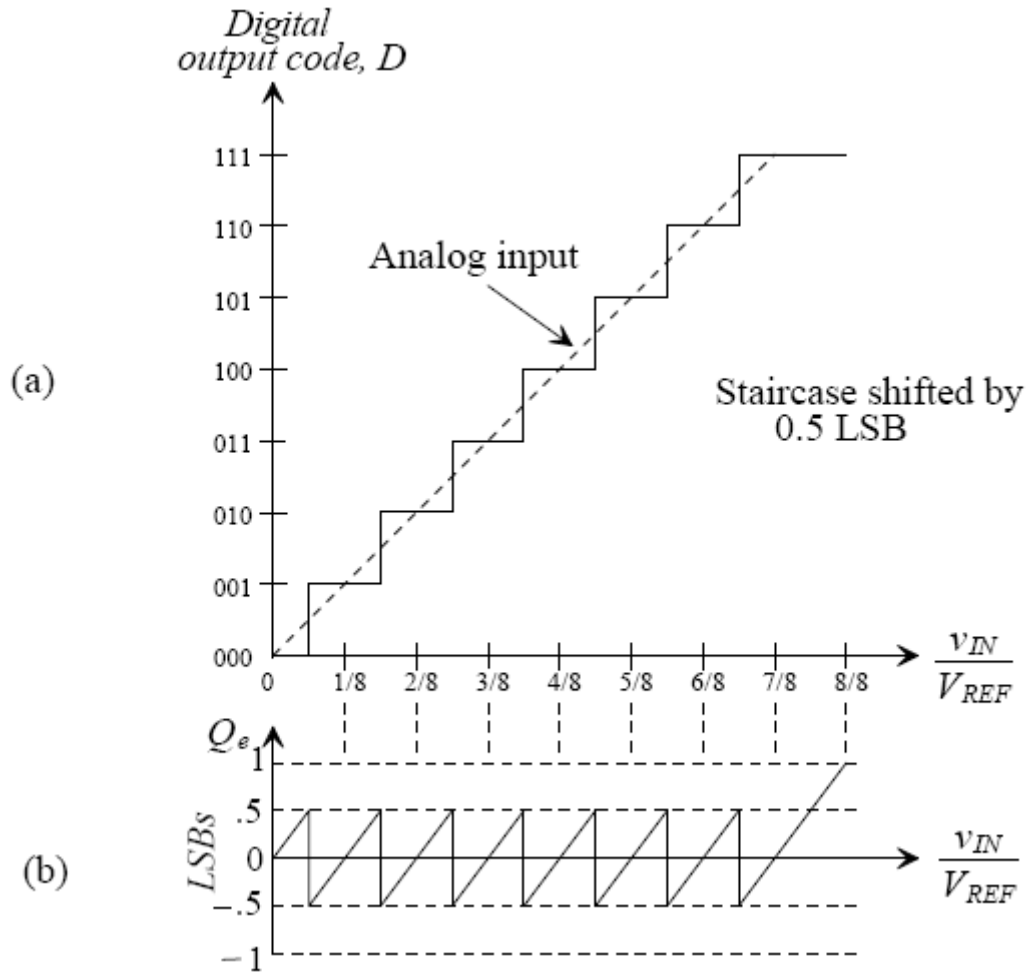

Figure 2.3 Ideal voltage characteristics of a 3-bit ADC with 0.5 LSB offset

(a) The ideal digital output for a given analog input. The ideal slope of the analog input dashed line is unity. The step widths and heights are ideally equal to one another. The staircase is purposely shifted by 0.5 LSB to reduce quantization error and potential implementation problems. (b) The quantization error for a given analog input. As the input approaches a new quantization level, the error increases to a maximum of 0.5 LSB excluding the portion approaching the reference voltage [1].

equal width and is distributed evenly between the reference and ground voltages.

The 12-bit ADC being characterized should have the same voltage characteristic curve, except it should have 2^{12} (or 4096) discrete levels for the staircase. Additionally, the characteristic curve will be centered around an analog voltage of zero volts, because the reference voltage is a differential ±2 V. Figure 2.4 shows the acceptable analog voltage range for the ADC. Note that the intended analog range allows for a ±2 V swing. For a proper analog-to-digital conversion, it is important that the input signal has a DC offset equal to 1.65 V. The height of the steps will depend on the reference voltage level as shown in equation 2.1.

$$Step(Height) = \frac{V_{REF}}{2^{\#Bits}} = \frac{4V}{2^{12}} = 977\mu V \tag{2.1}$$

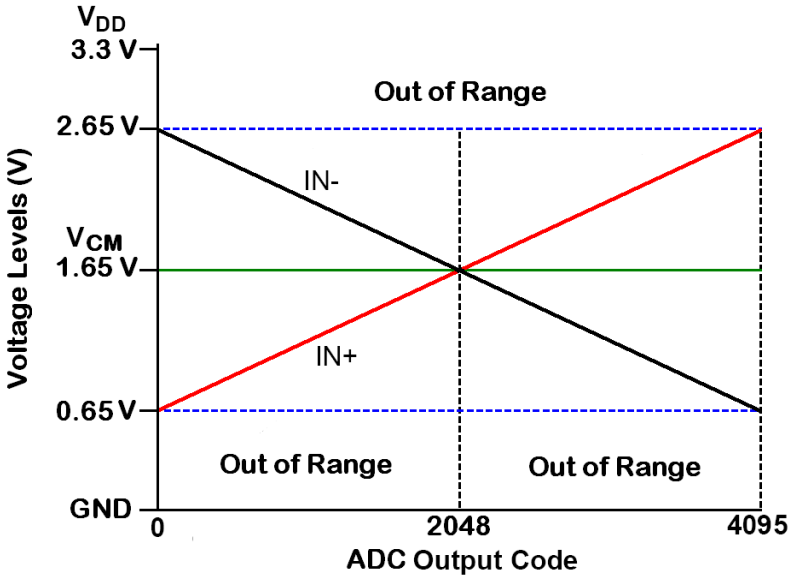

Figure 2.4 Intended analog input voltage range

Plot showing the proper range of input voltages for the 12-bit ADC found on the UT1 Thyatira. [15]

The tested ADC is rated for a differential reference voltage of 4 volts maximum. Thus, if the maximum reference voltage is employed, the width of each step will theoretically be 977μV.

2.3 Non-Ideal Characteristics

The non-ideal characteristics to be discussed are differential nonlinearity (DNL), missing codes, integral nonlinearity (INL), offset error, and gain error. These are the characterization parameters being determined for this thesis.

The first non-ideal characteristic discussed is the DNL of an ADC. DNL, by definition, is the difference between the measured step width and the ideal step width of one LSB, as shown in equation 2.2 [1].

$$DNL = Measured\ Step\ Width - Ideal\ Step\ Width \tag{2.2}$$

If the DNL is greater than zero, then the quantization error of the ADC will become worse than the ideal case. This is caused by the fact that more of the analog voltage range will be interpreted as a single digital level. A missing code is present if the DNL equals negative one. Applying equation 2.2, this proves accurate, because if the measured step width is zero, then the equation will equate to a negative ideal step width or a negative one LSB. Even if an ADC has a step is 2 LSBs wide, or twice the ideal value, it will not guarantee that ADC will have missing codes, although it does produce favorable conditions for missing codes [1]. If an ADC has missing codes, then the effective number of bits decreases from the designed number of bits. Figure 2.5 shows how the DNL will affect the staircase characteristic curve. The wider steps will introduce greater magnitudes of quantization error, because a wider range of analog voltages are

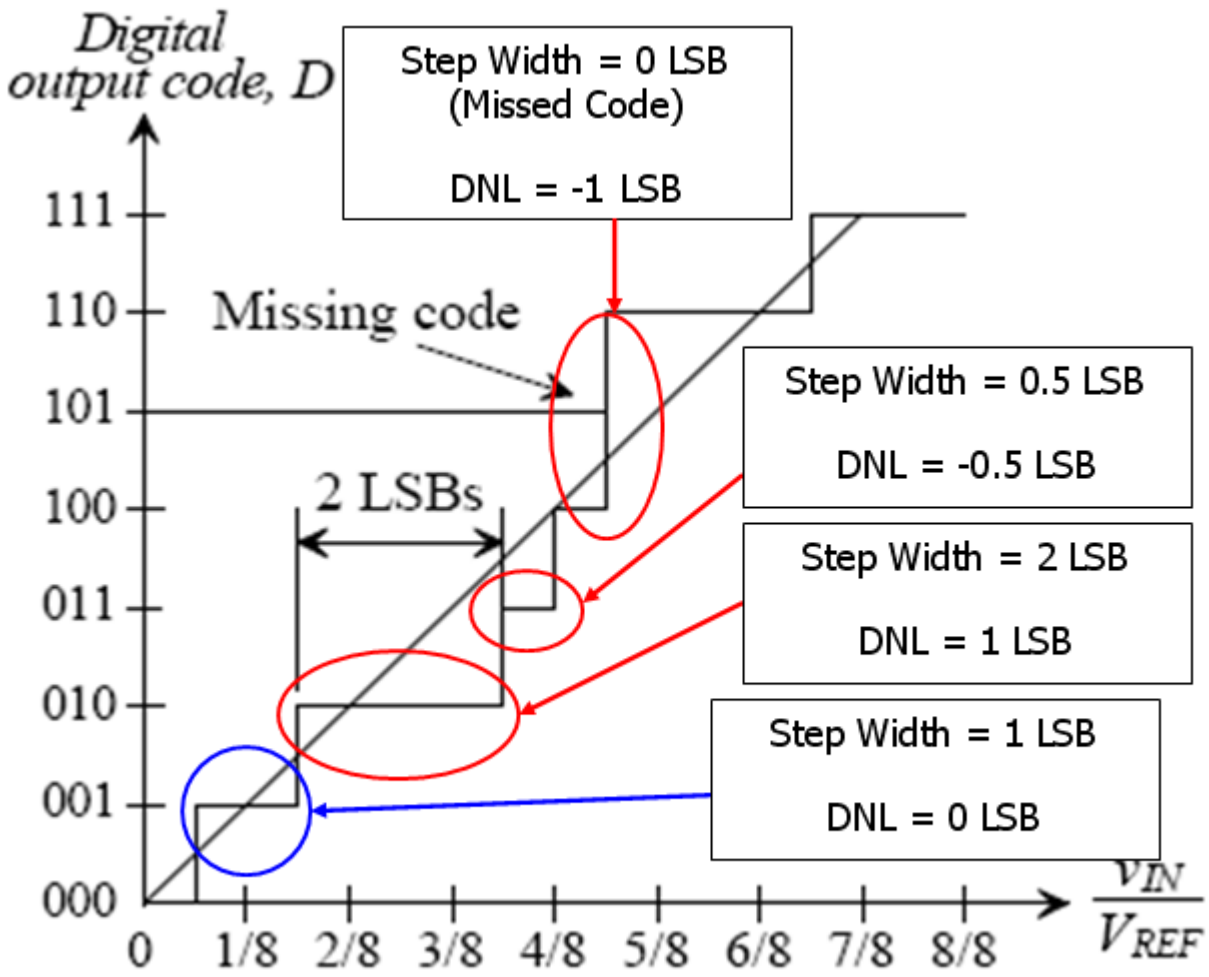

Figure 2.5 Non-ideal voltage characteristics showing DNL

(a) The non-ideal characteristic curve for a 3-bit ADC. This plot shows how the DNL manifests itself in the staircase voltage curve. The wider steps have a positive DNL and the narrower steps have a negative DNL. (b) The quantization error is similar to the ideal case, except the DNL causes the wider steps to generate a larger quantization error [1].

being digitized to the same output level.

Integral nonlinearity (INL) is the next non-ideality discussed. INL is defined as the difference between the measured corner transition point and the best fit line typically defined by the first and last transitional corners. Figure 2.6 shows the affect of INL on the staircase curve.

The final two non-idealities are the offset and gain errors. The offset error is simply the difference between the first transition point and the ideal first transition point, which is half of a LSB. Offset error will cause an initially higher than expected quantization error, but after the first transition the quantization error will return to the expected trend. The y-intercept of the best fit line used to determine the INL of the ADC is equal to the offset error.

The gain error, also called the scale factor error, is the difference between the slope of a best fit line going through the corners of the transitional points of each step and the ideal slope of the staircase curve of unity. Both the offset and gain errors are shown in Figure 2.7. Note how quantization error is affected by the presence of both offset and gain errors. The offset error introduces an initially high quantization error, but settles out to the ideal sawtooth pattern. Conversely, the gain error increases the quantization error for higher code steps.

The above mentioned non-idealities will be considered in the characterization of the 12-bit pipeline ADC for this thesis. The non-idealities amount to a DC characterization of the ADC. Although the ADC will be performing conversions dynamically, the dynamic characteristics of the ADC are not considered because of time restraints and difficulties with the ADC testing. Several dynamic characteristics that could be measured in the future include: variation of DC characteristics over temperature, aperture error, bandwidth, and the signal-to-noise ratio (SNR).

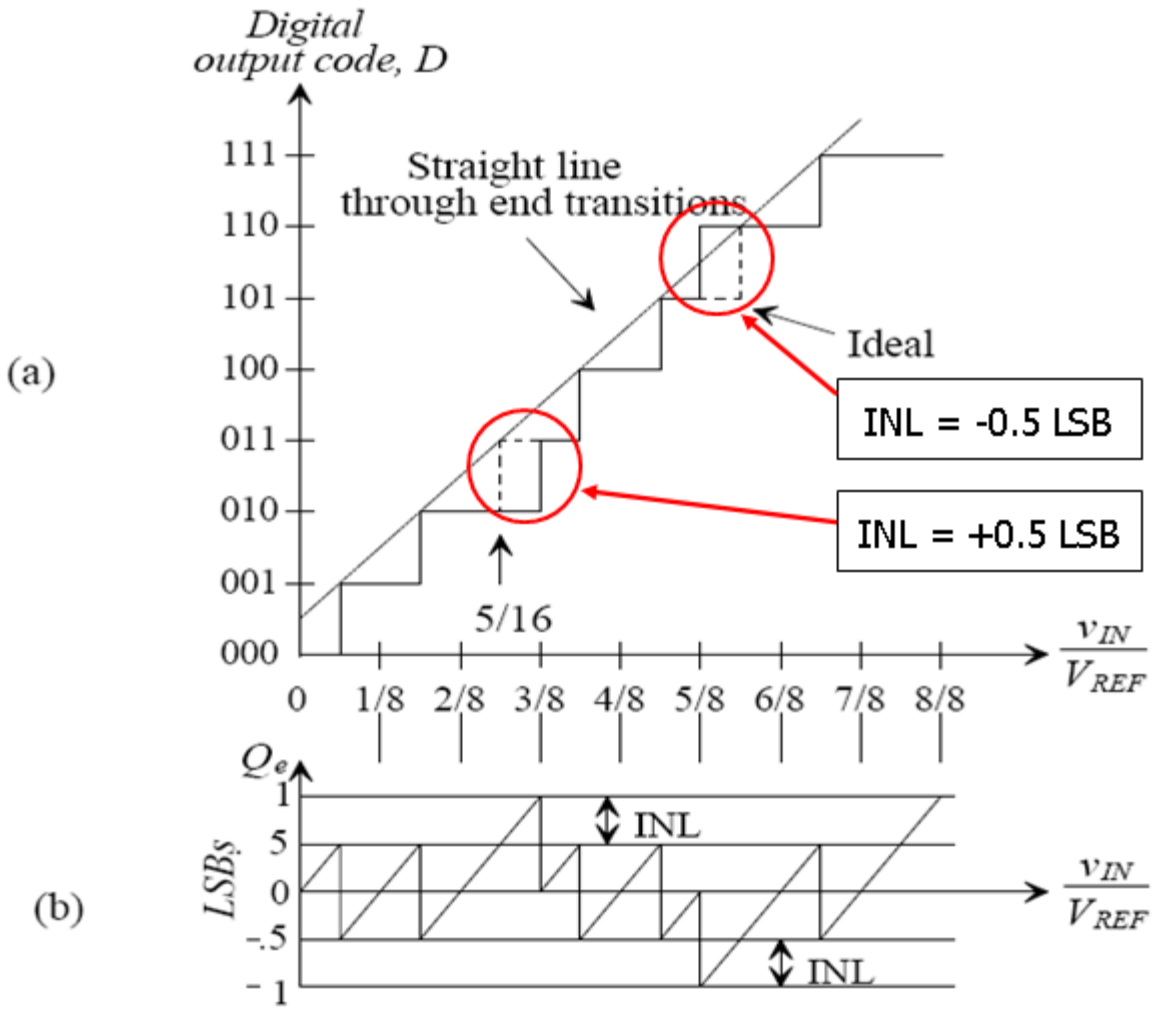

Figure 2.6 Non-ideal voltage characteristics showing INL

(a) The non-ideal characteristic curve for a 3-bit ADC. This plot shows how the INL manifests itself in the staircase voltage curve. (b) The quantization error caused by the INL [1].

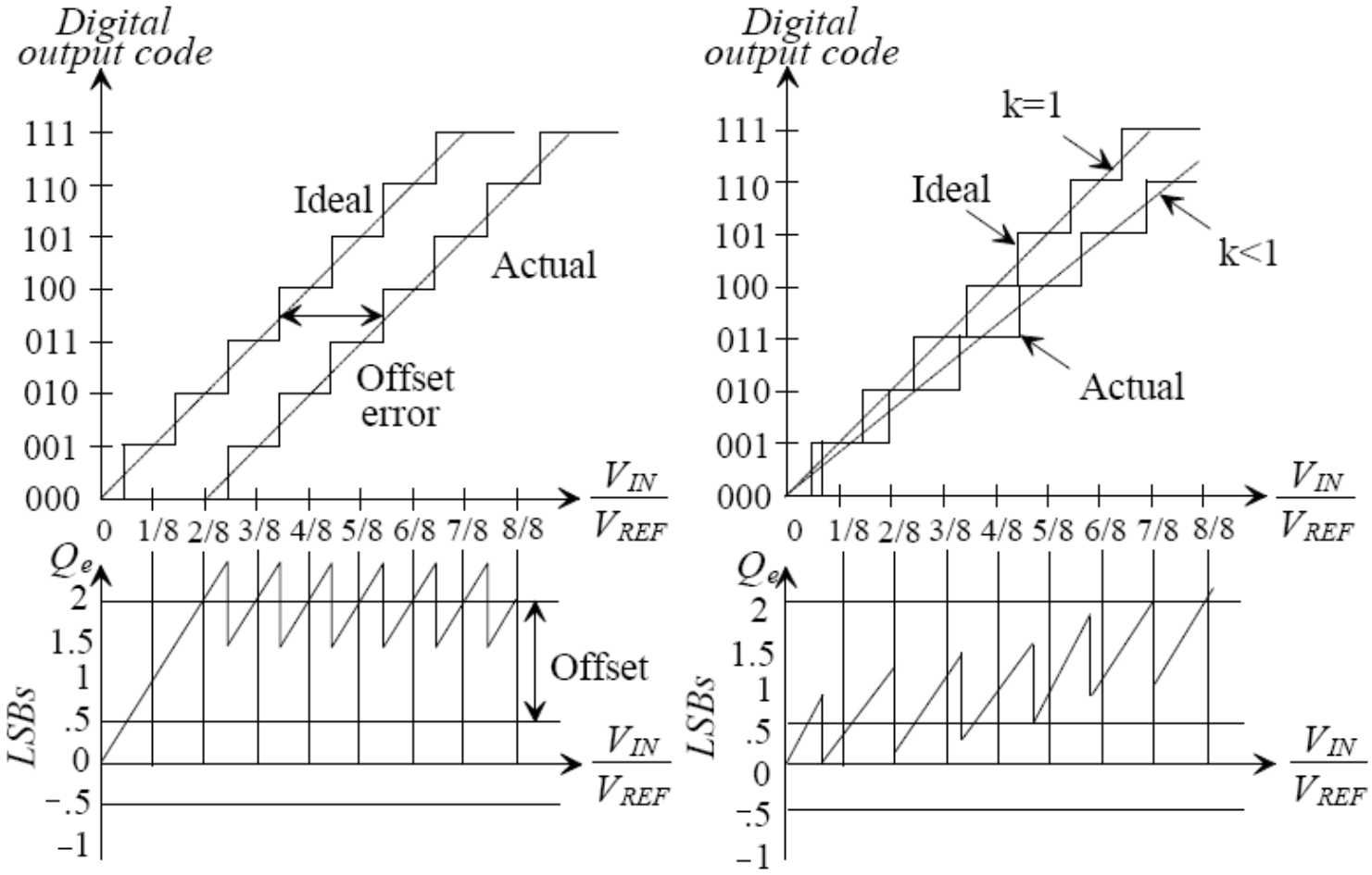

Figure 2.7 Non-ideal voltage characteristics showing offset and gain error

The plot on the left shows the manifestation and effects of the offset error on the ideal ADC characteristic curve. The plot on the right depicts the same for the gain error [1].

Chapter 3 Characterization

3.1 UT1 Thyatira Chip

The UT1 Thyatira chip contains the 12-bit pipeline ADC. The chip also contains a sub one volt bandgap reference circuit and a solitary high speed sample-and-hold circuit. An identical high speed sample-and-hold circuit is also used in the pipeline ADC.

The functionality of the high speed sample-and-hold was verified first, as it is one of the required fundamental circuit blocks the ADC needs for proper functionality. The high level circuit schematic for the S150 high speed sample-and-hold is shown in Figure 3.1. The sample-and-hold modes of the circuit are shown in Figures 3.2 and 3.3, respectively.

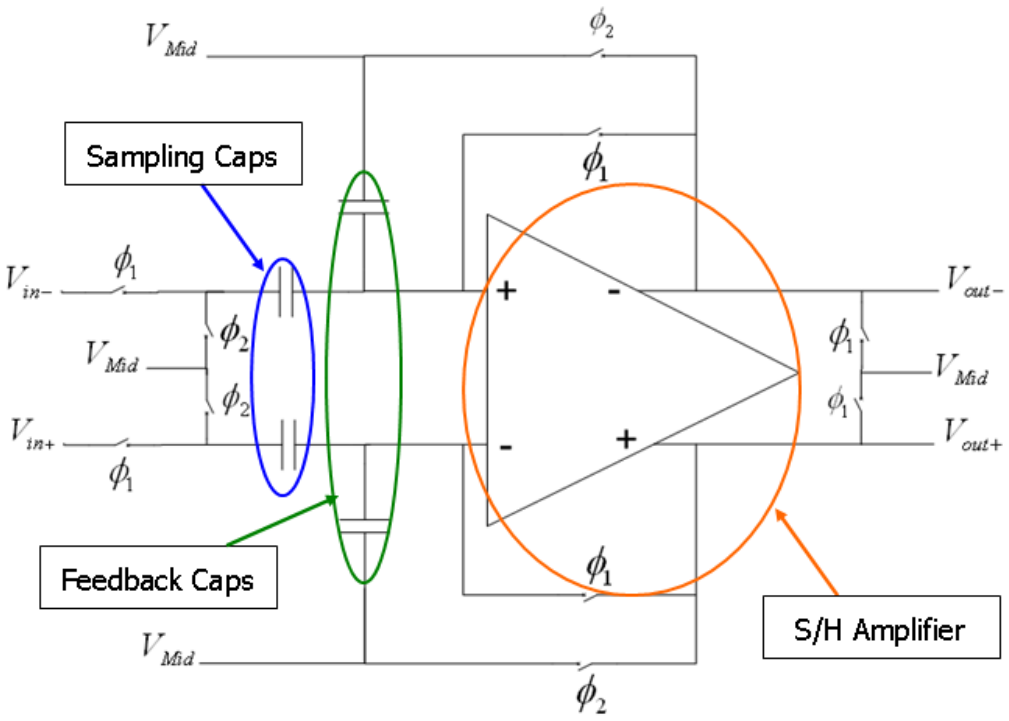

Figure 3.1 High speed sample-and-hold high-level schematic

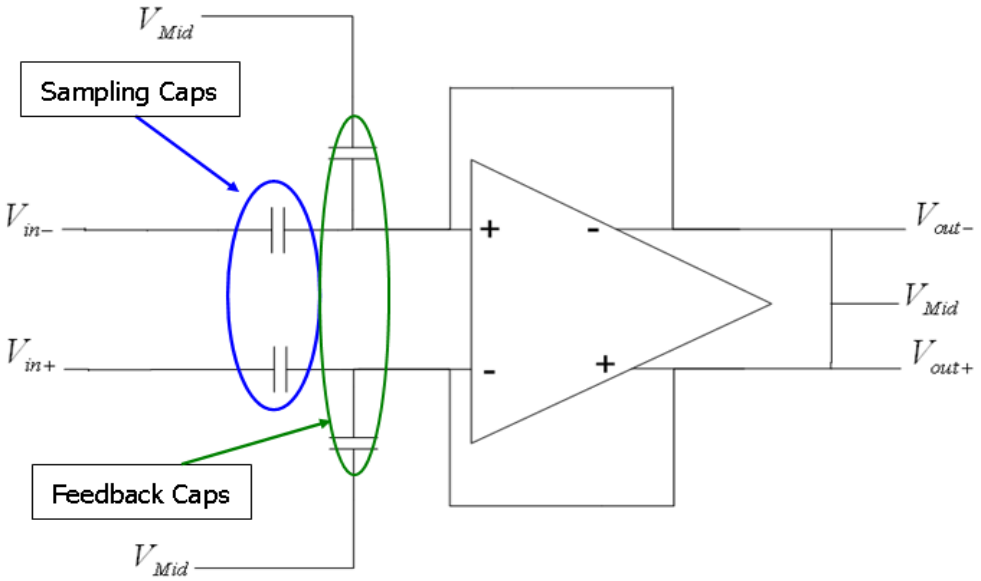

Figure 3.2 Sample mode of sample-and-hold circuit

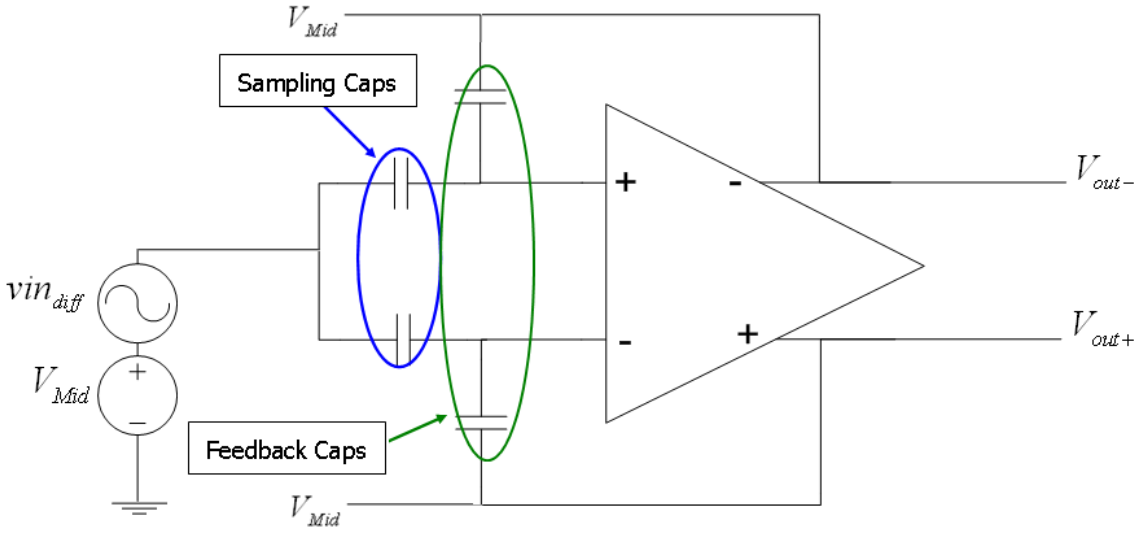

Figure 3.3 Hold mode of sample-and-hold circuit

The switches for the sample-and-hold circuitry have been implemented using three CMOS transmission gates for each switch. The schematic for the transmission gate is shown in Figure 3.4. Two dummy transmission gates half the size of the switch transmission gate are attached to the input and output nodes of the switch. Assuming the clock feedthrough is equally fed to the input and output terminals of the switch, the dummy transmission gates ideally allow an opposite polarity of the clock feedthrough to appear at both nodes canceling the effects of the clock feedthrough.

During the sampling mode of the sample-and-hold circuit, the sampling capacitors connected to the differential inputs charge up to the input voltages, assuming the capacitors have enough time to charge. The slew of the sample-and-hold amplifier will determine how quickly the capacitors are able to charge. The DC offset of the input signal should be set to the V_{Mid} voltage so only the differential input signal is sampled. It is essential for correct sampling that both the input signals have a DC offset equal to V_{Mid}. Otherwise, the sampling capacitors will not charge to the differential input signal, but will instead charge to the differential input signal plus the DC voltage difference between V_{Mid} and the DC offset of the input. During this sampling period, the feedback capacitors are also reset by setting the voltage across both feedback capacitors to zero volts, since both sides of the feedback capacitors are at the same potential. The operational amplifier is a unity gain follower during the sampling time with a common mode input of V_{Mid}.

After the sampling mode, the circuit is in the hold mode of operation. The sampling capacitors are tied together, which sums the sampled signal to form the differential input signal that will be amplified by the sample-and-hold amplifier. The signal vin_{diff} represents the charge

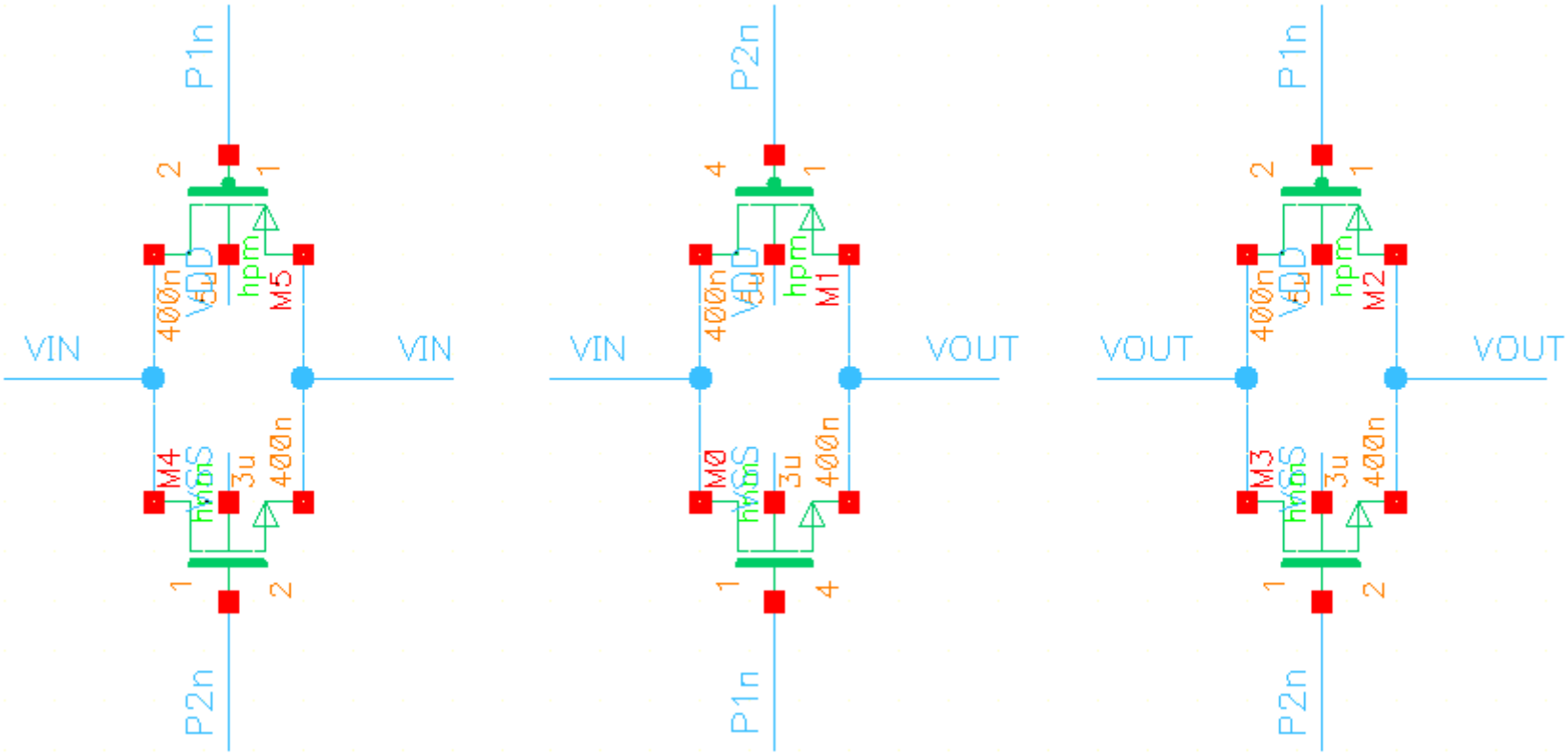

Figure 3.4 Transmission gate implementation for CMOS switches found on UT1 Thyatira

[4]

that accumulated on the sampling capacitors during the sampling mode of operation. The gain of the operational amplifier will depend on the ratio of the sampling and feedback capacitors, as defined in equation 3.1.

$$\frac{vout}{vin_{diff}} = A_F = \left(\frac{Z_F}{Z_S}\right) = \left(\frac{1/sC_F}{1/sC_S}\right) = \left(\frac{C_S}{C_F}\right) \tag{3.1}$$

The impedance of the feedback capacitor, Z_F, divided by the sampling capacitor impedance, Z_S, equals the closed loop gain, A_F, for one of the single ended output voltages. The differential outputs have opposite polarities with the same magnitude. Notice the gain is ideally only dependent on the ratio of the sampling and feedback capacitors, where we are assuming a sufficiently high open loop gain for the operational amplifier. Both feedback paths will provide a negative feedback path for the fully differential operational amplifier. The feedback paths should be identical and matched, because if the paths are different, then the output will exhibit second order harmonic distortion [17].

The outputs of the sample-and-hold circuit will be held at the amplified differential input level sampled if we assume the gain of the operational amplifier is infinite [1]. A finite gain will reduce the held signal slightly.

Other specifications of the operational amplifier will also have an impact on the sample-and-hold circuit performance, as shown in Figure 3.5. The slew rate and phase margin of the operational amplifier are important to the sampling mode of the circuit. During the hold mode of operation, the implementation of the switches is critical. All the switches will introduce some clock feedthrough that will affect the sampled voltage level immediately. This error is

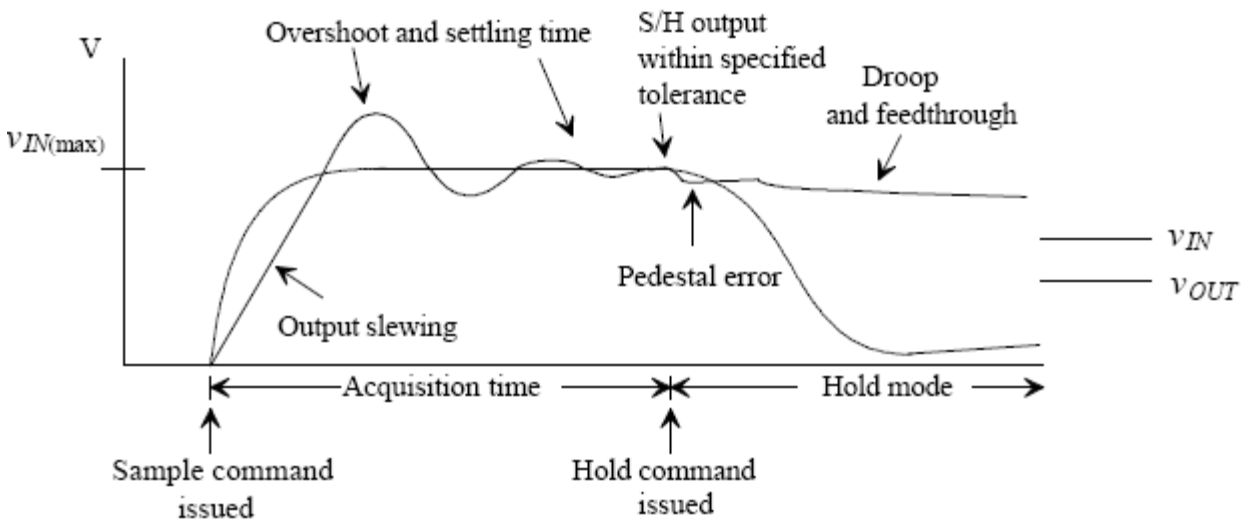

Figure 3.5 Typical output of a sample-and-hold circuit

labeled as pedestal error in Figure 3.5. When the circuit is left in the hold mode for increasing periods of time, the charge stored on the capacitors discharges through the switches, with finite resistance, and through parasitic paths. For this reason, there is a minimum clock frequency at which the sample-and-hold circuit will operate properly. If the clock frequency selected is too low, then the sampled signal could potentially have enough time to fully discharge while being in the hold mode of operation.

With a fundamental understanding of the sample-and-hold circuit, the testing of the high speed sample-and-hold found on the UT1 Thyatira chip commenced. Figure 3.6 shows a 60 hertz "hum" present at the sample-and-hold circuit differential output when no clock signal is supplied. The addition of the clock signal complicates matters further, especially since the designer of the chip used a signal ended clock. Figure 3.7 shows the overwhelming noise level

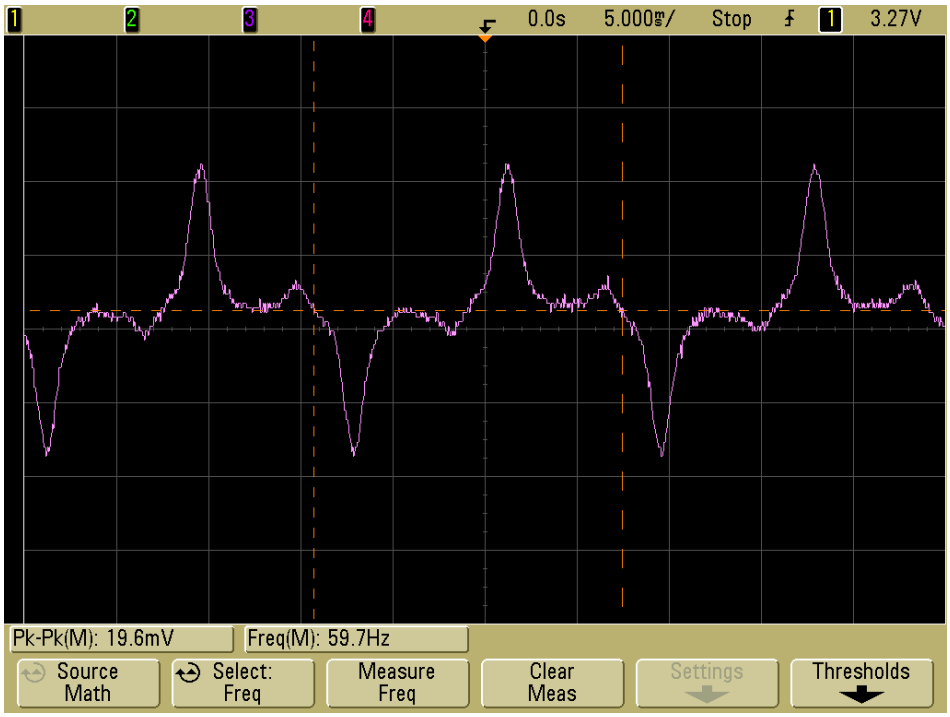

Figure 3.6 60 Hz noise on sample-and-hold differential output (No Clock)

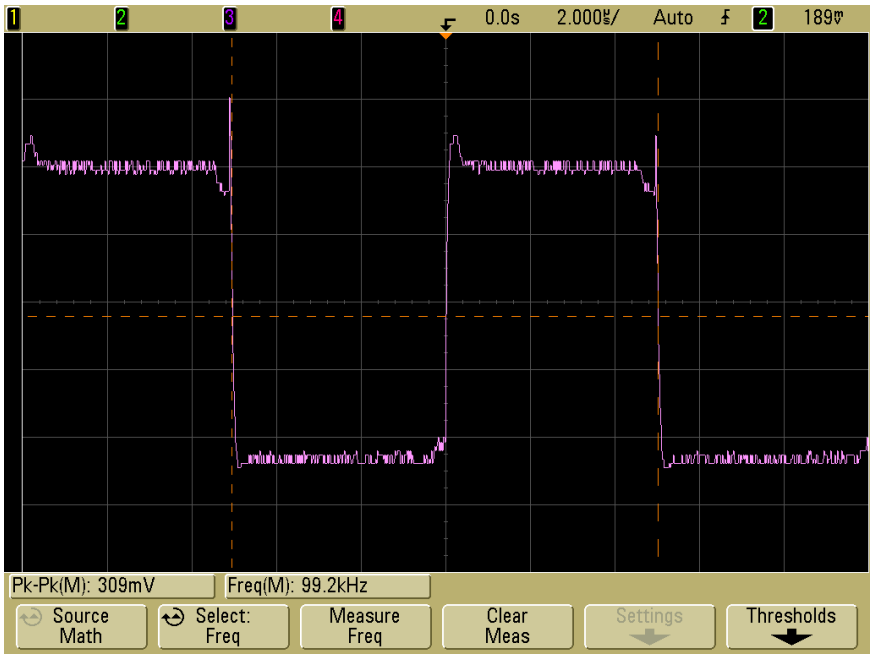

Figure 3.7 Differential output noise of sample-and-hold (Clock of 100 KHz)

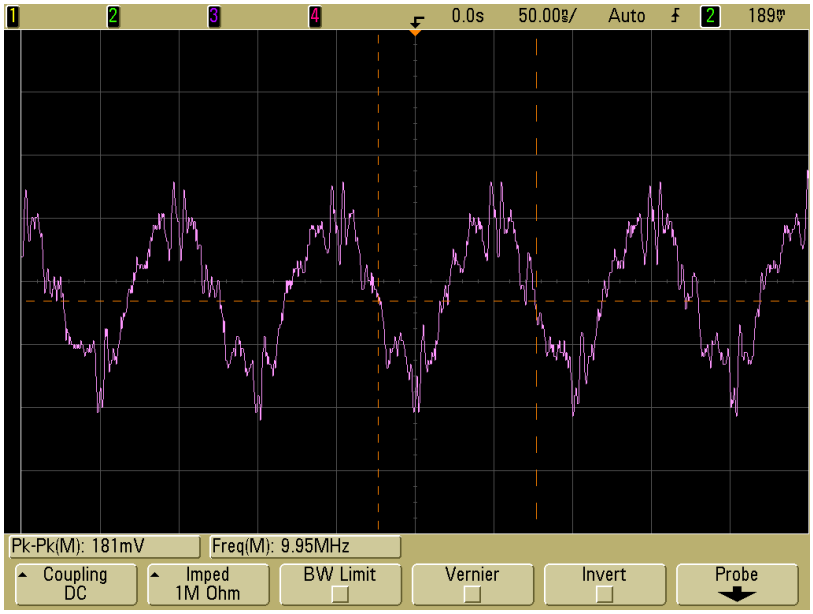

Figure 3.8 Differential output noise of sample-and-hold (Clock of 10 MHz)

introduced by a clock with a frequency of 100 KHz. Figure 3.8 shows the noise introduced by a 10 MHz clock signal.

The noise present during the 100 KHz clock tests are shown to be approximately 10-30 millivolts peak to peak, which is present both in the sample and hold phases of operation. At a clock frequency of 10 MHz, the squarewave output of the sample-and-hold is severely distorted and attenuated. The same input was given for both tests, so the amplitude has been attenuated by nearly a factor of two. The oscilloscope probing capacitance will degrade the performance of the sample-and-hold, especially at higher frequencies of operation. However, the ADC performance also degrades at higher clock frequencies, which suggests the high speed sample-and-hold circuit is not capable of operating at the designed 10 MHz clock frequency without degradation in performance. Previously it was mentioned that a 12-Bit ADC with a reference voltage of 4 volts must be able to discern a little under a millivolt change in the input signal. With the noise level being generated, the ADC output would switch around unpredictably.

The input level to the sample-and-hold should not exceed one volt peak to peak single ended and a two volt peak to peak differential. However, if the nominal input is used, the noise level will overwhelm the conversion of the input signal as shown in Figure 3.9. By doubling the nominal input magnitude to 4 V peak-to-peak (differential), the input signal becomes more visible on the ADC output at the sacrifice of exceeding the ADC reference voltage range, shown in Figure 3.10. For both of these figures, the clock is set for 10 MHz with clock edges of 10 ns. The raw data samples, as shown in Figure 3.10, can be improved by reducing the clock frequency to 1 MHz with clock edges of 50 ns, as shown in Figure 3.11.

As discussed previously, the sample-and-hold is a crucial building block for the pipeline ADC. These early results were not encouraging. Multiple chips were tested to see if the problem was chip specific. Although certain chips out performed others, the results for all chips tested were below expectations.

The ADC is fortunately separate from the sample-and-hold that is probed. This aids in the testing process, because the output of sample-and-hold circuit being used by the ADC should exhibit similar behavior.

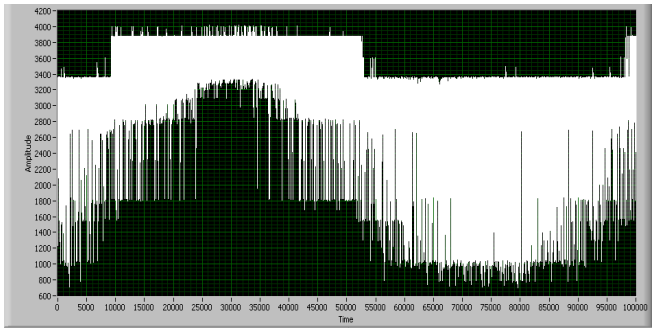

Figure 3.9 Noisy sine output of ADC (2 VPP Diff. Sine & 10 MHz Clock)

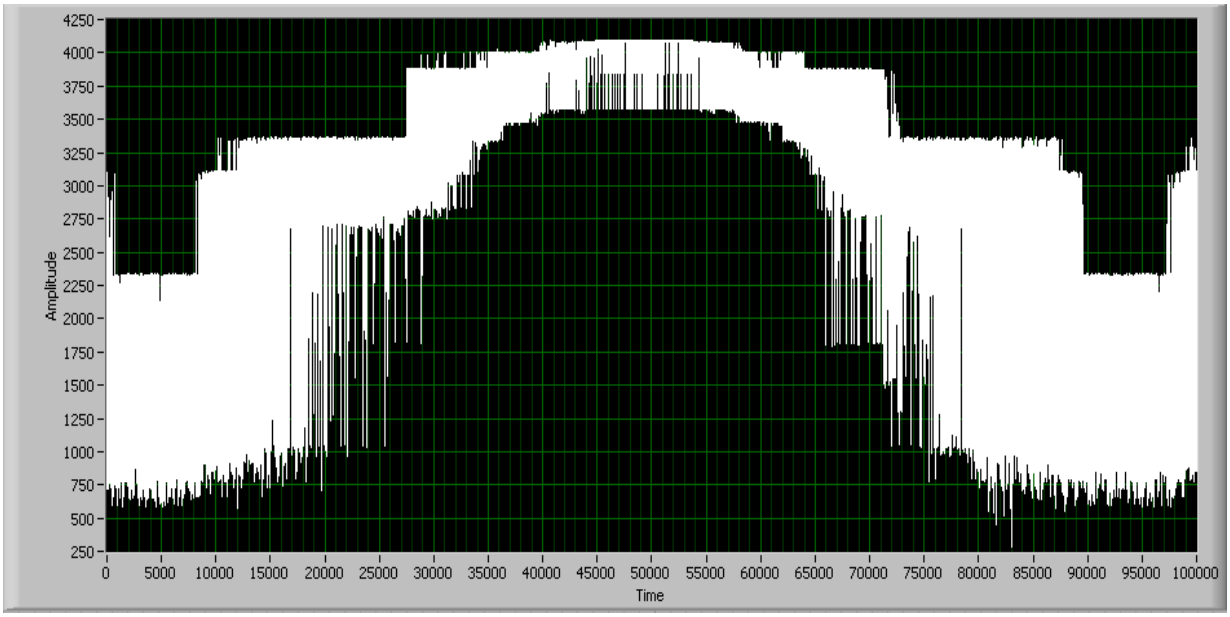

Figure 3.10 Noisy sine output of ADC (4 Diff. VPP Sine & 10 MHz Clock)

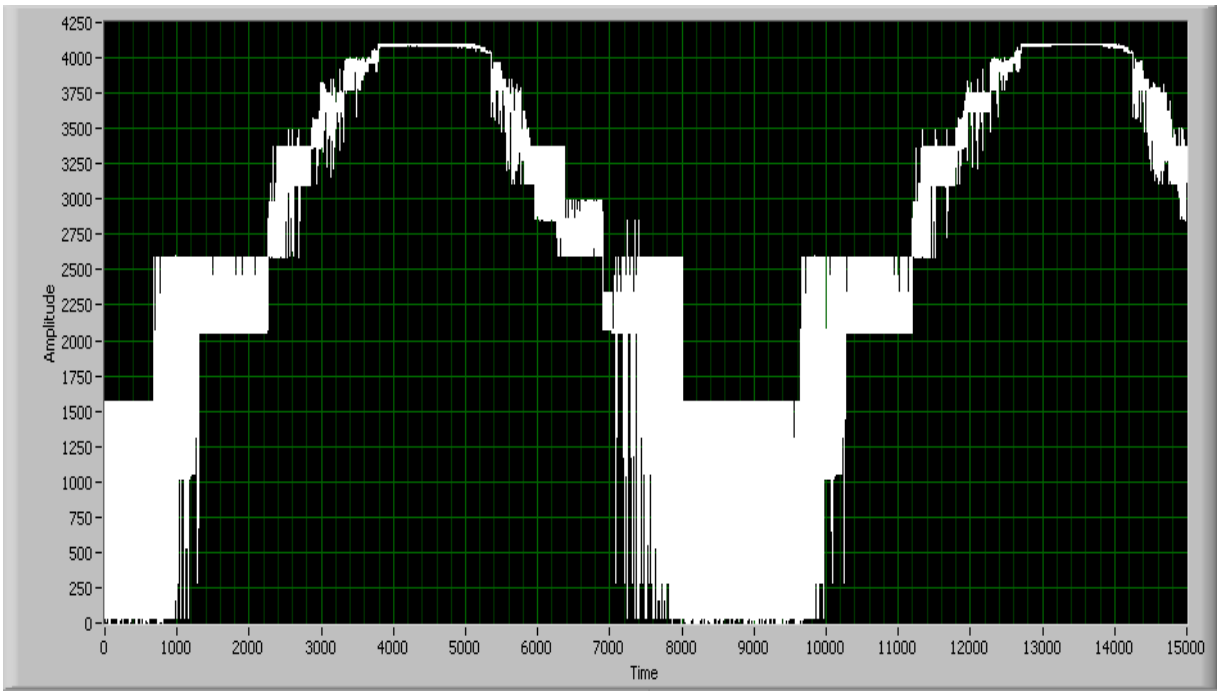

Figure 3.11 Noisy sine output of ADC (4 Diff. VPP Sine & 1 MHz Clock)

3.2 Test Board

The test board was designed by Ross Chun and generously made available for use to characterize the ADC on the UT1 Thyatira chip. A picture of the test board in its entirety can be found in Appendix A of this thesis.

The test board was designed to test the bandgap reference circuit output, the high speed sample-and-hold output, and the ADC outputs. Figure 3.12 shows the portion of the test board responsible for providing all reference and bias voltages. Each 6-pin socket connects to a HA5033 250 MHz video buffer. The reference voltages starting from the left and moving to the right are as follows: VDD_{18} , V_{REFP} , V_{MID} , and V_{REFN} . The VDD_{18} voltage should be adjusted until it is approximately 1.8 V, V_{REFP} should be 2.65 V, V_{MID} should be 1.65 V, and V_{REFN} should be 0.65 V.

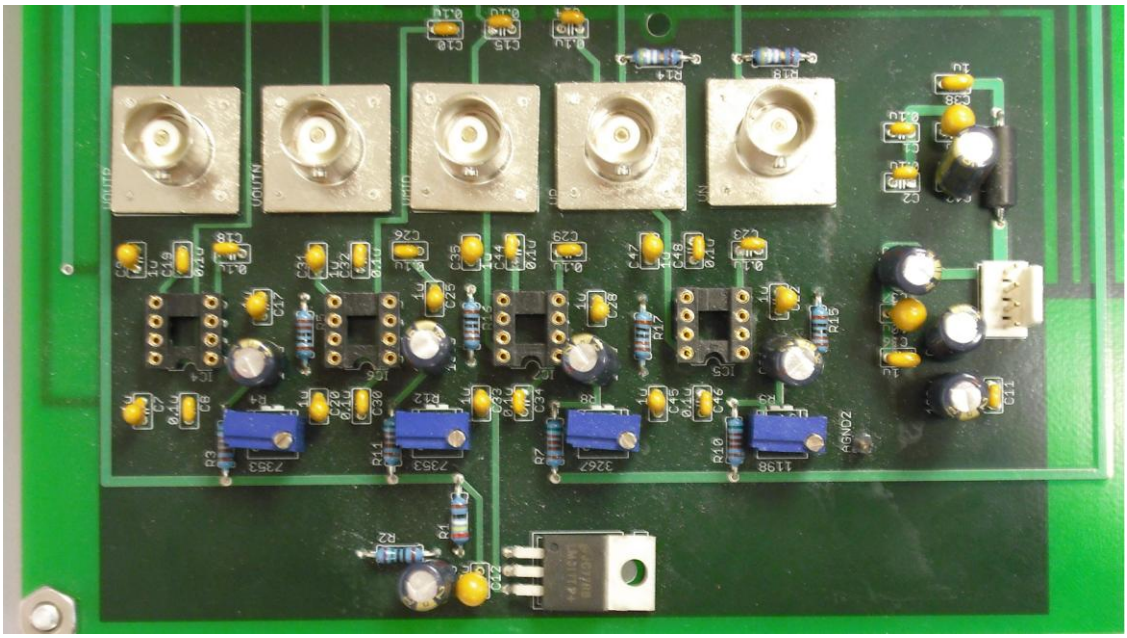

Figure 3.12 Bias circuitry on test board

Each potentiometer permits the adjustment of each bias voltage individually. A potentiometer also resides on the back side of the test board to allow the current bias of the solitary sample-and-hold to be adjusted.

To adjust the current bias for the pipeline ADC, a modification was added to the board. The on-chip current reference was measured as having an output current of approximately 130 µA, while the ideal bias current should be approximately 250 µA. The modification added is simply a potentiometer and resistor in series from the bias current mirror input to ground. The value of the resistor is 2.43 kΩ, so by using Ohm's law the bias current flowing through the resistor can be determined as the potentiometer is adjusted. A switch was also used, so if for any reason the tester wanted to switch back to the on-chip current reference, then it could be by changing the switch position. A 2.2 µF tantalum capacitor was also soldered between the supply rail VDD and the current mirror input bias node to reduce noise.

In hopes of reducing the noise level, an additional BNC connector was soldered to the side of the test board near the BNC that carries the clock signal onto the board. This additional BNC connector brings an inverted clock, or clock bar, onto the chip as well. The presence of the inverted clock assisted marginally, but it is still recommended to connect an inverted clock to the BNC during testing.

The V_{REFP} and V_{REFN} voltages are the differential ADC reference voltages. The ADC reference voltage is equal to the difference between the voltages of V_{REFP} and V_{REFN}. If the input signal equals the difference, then the output of the ADC will be '111111111111' or step 4095. This is the highest output level for a 12-bit ADC. If the input is a negative reference voltage, then the output code of the ADC will be '000000000000' or step 0, which is the lowest output level.

The V_{MID} voltage is the reference voltage used by the comparator in the pipeline ADC architecture and was shown in Figure 2.1 as $\frac{V_{REF}}{2}$.

The three left BNC connectors are important during the testing process. The two on the far left are the differential output of the test sample-and-hold, which is separate from the ADC. The ADC inputs are also connected to the test sample-and-hold. With the use of an oscilloscope, the performance of the sample-and-hold under the available bias conditions and input signal can be shown. If the test sample-and-hold circuit provides an output that does not resemble the input, then a problem exists with either the input signal attributes or the bias voltages. The input signal must have a common mode voltage of approximately 1.65 volts. The middle BNC connection is the common mode voltage V_{MID}. This BNC connection was intended for setting the DC offset of the Audio Precision System Two precision sine generator. However, the DC offset will be attenuated because of the 50 Ω terminations. Therefore, an external power supply was used to generate the necessary DC offset for the input signals. It is important to probe the 50 Ω resistors on the test board to ensure the DC offset is accurate. The far two BNC connections on the right are the differential input for the sample-and-hold, and consequently, the ADC as well.

The next portion of the test board, shown in Figure 3.13, contains the socket necessary to mount the UT1 Thyatira chip onto the test board. The chip is easily mounted by placing the chip in the correct orientation in the socket indentation, then pressing down evenly on all four corners of the socket and gently releasing. On either side of the socket there is a SN54HCT541 line driver. Each line driver is capable of buffering eight digital outputs. The line drivers are

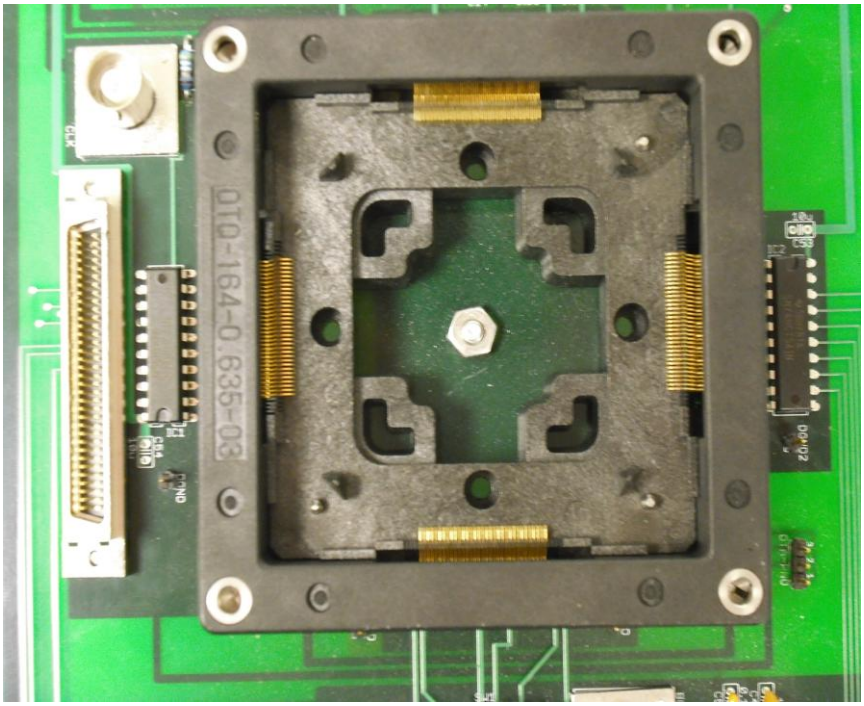

Figure 3.13 UT1 Thyatira chip socket, NI 68-pin peripheral connector, and line drivers

soldered directly to the test board without a socket in order to minimize parasitic capacitances in the signal path.

The clock signal, which is connected through the BNC connector shown, is also directed to the line driver nearest the BNC connector. The clock requires an amplitude equal to the VDD voltage, which is 3.3 V for this chip. The minimum allowable clock amplitude is approximately 1.9 to 2.0 V. The only reason the clock amplitude can be reduced is the presence of clock buffers on the chip that will restore the clock amplitude to 3.3 V.

Depending on the signal generator, an offset voltage may need to be added to help the clock to move from 0.0 V to 3.3 V. The preferable clock generator is The Lecroy Pulse Generator. The Lecroy Pulse Generator conveniently outputs the inverted clock in addition to the clock signal. Also, it requires no additional DC offset, because the low and high voltages can be

explicitly defined. The frequency of the clock should not exceed 10 MHz. Lower frequencies provide optimal measurements.

A total of twelve digital outputs from the 12-bit ADC and the clock are connected to the NI 68-pin connector after being buffered by the line drivers. The clock is connected to port PFI2. The ADC digital outputs, starting from the MSB to the LSB, are connected to lines zero through seven of port zero and lines zero through three of port one. This is important for use in the Labview code.

3.3 Overview of Test Procedure

The test board previously mentioned and discussed in detail was used exclusively throughout the testing of the ADC on the UT1 Thyatira chip. The board was designed and fabricated before work on this thesis began, but additional components and connectors were necessary in order to test the ADC. The most notable additions include the additional inverted clock BNC and the resistive current sink for the PMOS current mirror input.

In order to characterize the ADC for the DNL, INL, offset error, and gain error a differential sinusoidal is required. The differential sinusoidal signal was set for the maximum amplitude of two volts peak-to-peak. Note the input is differential. In order for the input to exhibit the correct amplitude for the ADC to convert, the two sinusoids used for the positive and negative inputs must be exactly 180 degrees out of phase. The two sinusoids were set at a DC offset equal to V_{MID} . The amplitude of each individual sinusoid is equal to one volt peak-to-peak, providing a differential amplitude of two volts peak-to-peak. The same conditions apply to a triangular waveform, if one were used. Different input signal frequency, clock frequency, comparator reference voltage, and input signal DC offset combinations were used in order to

ensure dynamic characteristics were not dominating the characterization process and to achieve the best results possible. Although the clock for the ADC is designed for 10 MHz, the digital outputs of the ADC began to exhibit instability at higher clock frequencies. This is likely because of clock feedthrough from the transmission gates found in the high speed sample-and-hold circuitry, and because the clock is single-ended. As the frequency of the clock increases, the gate to source and gate to drain capacitances associated with the MOSFETs that comprise the transmission gates will reduce in their impedance, allowing for additional clock signal to feed into the signal path.

The most difficult aspect of testing the ADC was optimizing the conditions surrounding the chip. Adjusting the bias voltages and DC offset for the input signals was time consuming and frustrating, especially when having limited knowledge of the inner workings of the chip. After acquiring a basic understanding, the results improved over time. Another issue was the discovery of two pins swapped on the pin-out spreadsheet, the IINPUT and IOUTPUT pins. Testing a non-personal design definitely made the testing process more complicated, however with the continued correspondence with the ADC designer, Mark Hale, the results continued to advance with an improved understanding of the design.

3.4 Labview Code

The Labview code created and employed had the simple purpose of interfacing the test board with a personal computer (PC) so the lab measurements of the 12 digital output bits of the ADC could be collected in a timely manner. Several of the measurements were performed multiple times with each measurement consisting of as many as one million samples, which would be quite an undertaking if performed manually. The interface connection used was the 68-

pin NI 6534 connector. The Labview code responsible for the task of gathering the digital output data is shown in Figure 3.14.

The input amplitude and frequency used in the first frame are directed to a simple VI which is responsible for controlling the Audio Precision System Two precision sinusoidal generator. This portion of the Labview code is only relevant for a sinusoidal input test. If triangular input tests were performed, then two Agilent 33250A 80MHz function generators would need to in sync and used for the differential input.

The DAQmx blocks interface with the NI connector. The first block sets the physical channels for the data, the data type, and how to handle multiple lines. For all tests conducted using this code, the channels were set to "Dev1/port0/line0:7,Dev1/port1/line0:3". All twelve lines were stacked into one channel. The data type selected was digital input. The next DAQmx block controls the timing associated with data collection. The sampling type, sampling rate, and clock source channel are specified. The sampling type used was "Finite Samples". The sampling rate must be equal to the external clock frequency, which was varied between 100 KHz and 10 MHz during the various testing attempts. The physical channel for the clock source was specified as "Dev1/PFI2".

The next DAQmx block begins the task associated with gathering the data at the specified sampling rate from the specified channels.

Moving forward, the next block controls how many samples to read from the channels specified and the format of the data being read. The number of samples was varied during the different tests, but the format of the data remained a 1 channel 16-bit unsigned integer. Multiple samples were taken from each line as indicated by the number of samples variable. The timeout variable is set to "-1", which indicates the code will run as long as necessary to acquire all the

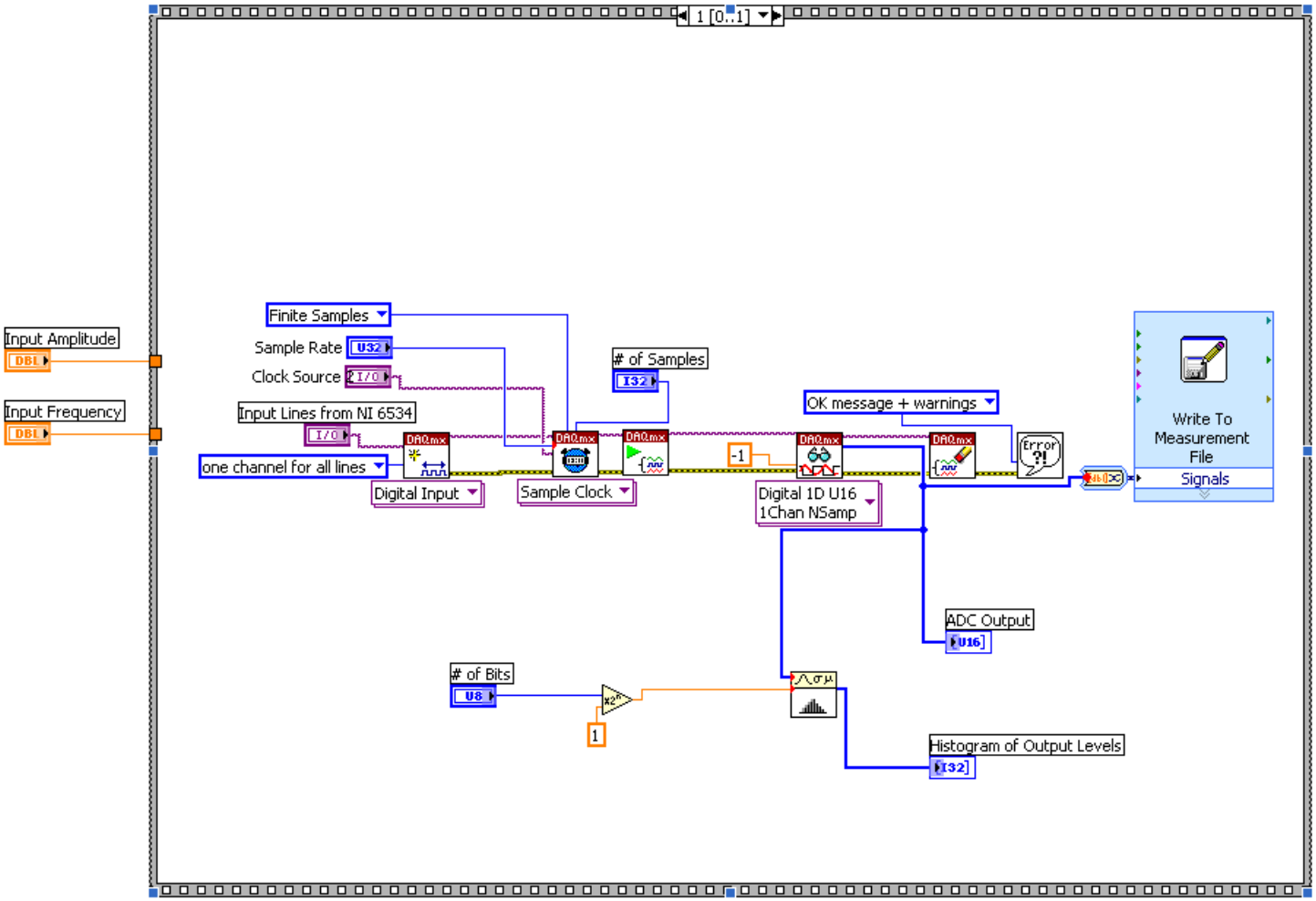

Figure 3.14 Labview code for collecting data from NI 6534 connector

[14]

requested samples.

The final DAQmx block completes the task of gathering the data and communicates any errors that might have occurred during data collection. If an error occurred, then a dialog box will appear with the error code and a possible explanation for the problem. If no error exists, the code will execute, end, and display the raw data results in the form of a waveform and a histogram of the output levels triggered during the test. The most common error is providing the code with the incorrect physical addresses for the data lines and/or the clock source.

The small bit of code at the bottom creates a simple histogram plot designed for an n-bit ADC where the output levels acquired include all output levels. The histogram will depict a misleading picture if the lowest level is not zero or if the highest level is not 4095. This is the reason raw output levels are plotted alongside the histogram plot. The histogram plot will display the lowest triggered output code as 0 and the highest triggered output code as 4095 regardless if they are 0 and 4095. This does not constitute a serious problem, as the data is to be plotted in Matlab regardless.

Finally, all of the data collected is stored in a ".LVM" Labview data file. The file is an ASCII tab delimited data file that will be analyzed using Matlab.

3.5 Matlab Code

The Matlab code was created and utilized to take the digital output raw data collected by Labview and perform computations to uncover the characteristics of the ADC being tested. The code used for determining the characterization parameters and generating the plots in Chapter 4 is found in Appendix B.

3.6 LTspice Simulations (Ideal Components)

Using the free circuit simulator LTspice by Linear Technology, the 12-bit pipeline ADC was first simulated prior to any measurements. This provides a baseline for the best case scenario of the measurements, and to further an understanding of the inner workings of the ADC. Figure 3.15 shows a segment of the schematic used to simulate the 12-bit pipeline ADC architecture. The portion shown between components A12 and E22 is the repeated pipeline architecture stage block. In order to implement a 12-bit ADC, 11 pipelined stages and a final comparator stage where used. R-C delay networks were used between stages to prevent race conditions [1]. The D-flip flops (DFF) synchronize the outputs of the ADC with each other by adding variable delays. Figure 3.16 depicts the results of sweeping the input voltage as a ramp between zero volts and the reference voltage of the ADC, which is two volts for the purpose of the simulation.

The digital output of the 12-bit ADC was fed through an ideal 12-bit DAC in order for the output of the ADC to be directly compared with the analog voltage it is supposed to convert. The schematic for the ideal 12-bit DAC used is shown in Figure 3.17.

Both the 12-bit pipeline ADC and DAC, using ideal components, are based on the examples provided by Jacob Baker on his textbook website cmosedu.com [1]. The examples provided are a 3-bit ADC and 3-bit DAC. However, it was not difficult to extend the concept to a higher number of bits.

The simulation results show the pipeline architecture, implemented using ideal components in LTspice, works as expected apart from a few minor issues.

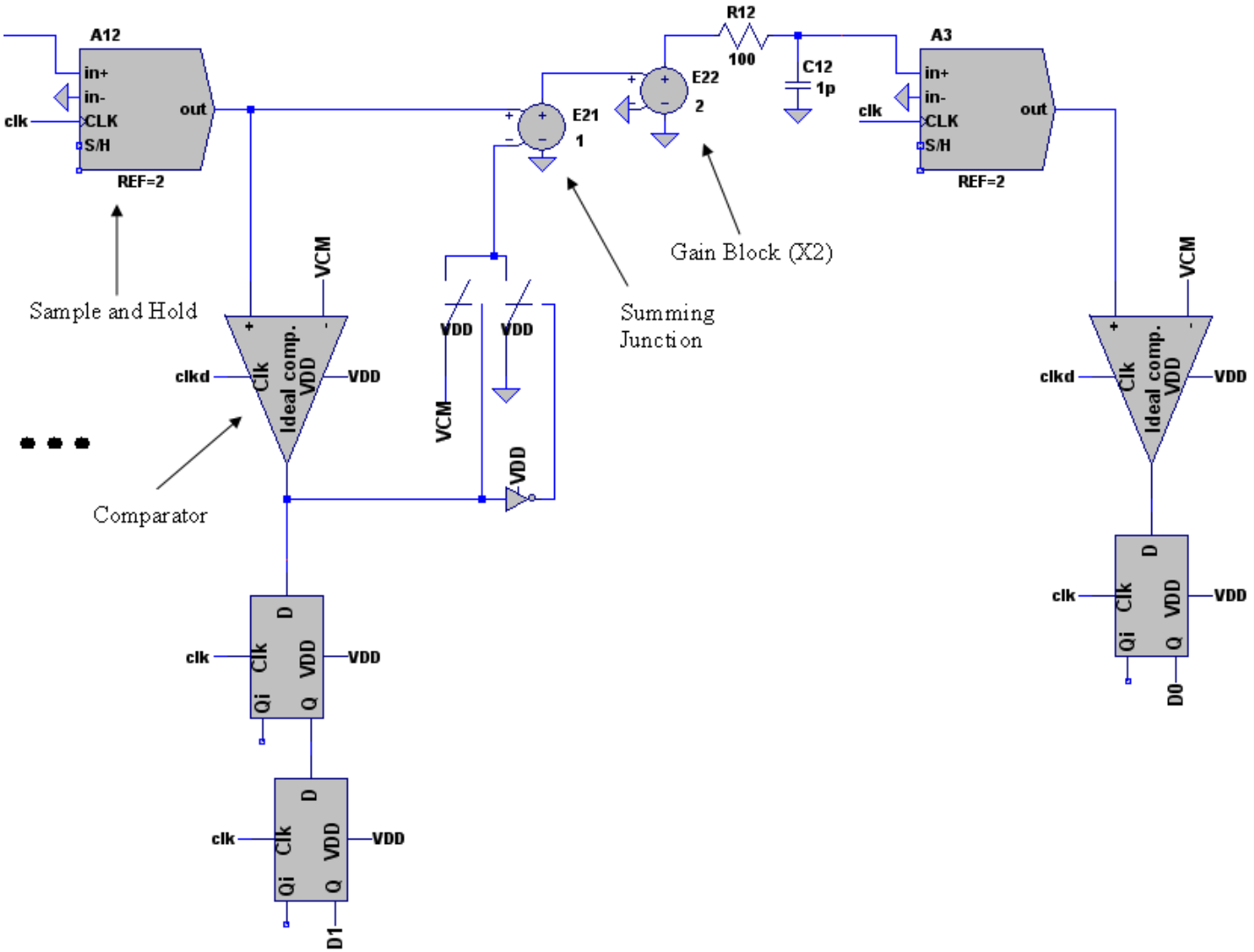

Figure 3.15 LTspice pipeline ADC schematic portion

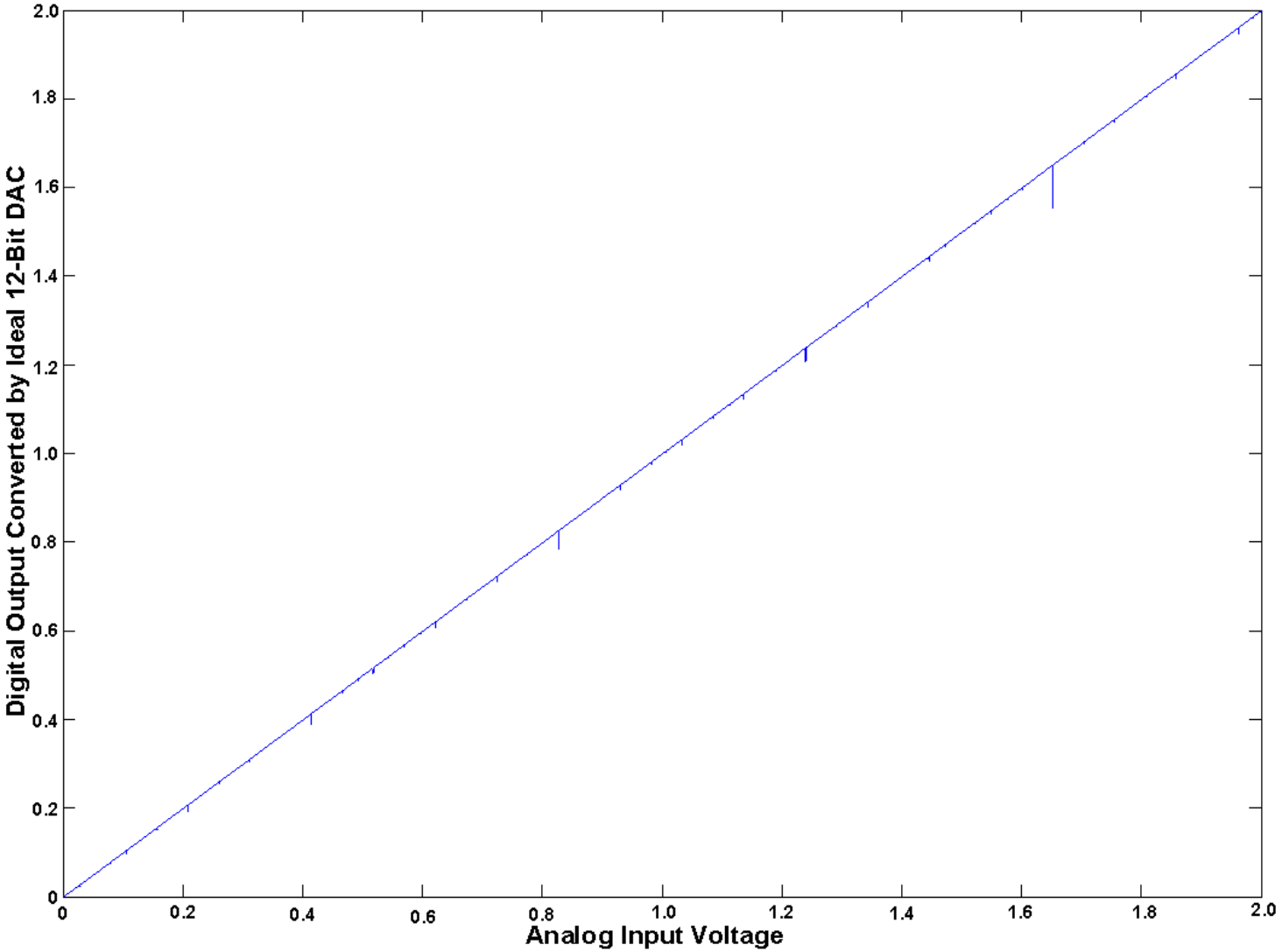

Figure 3.16 Simulated characteristic curve for 12-bit pipeline ADC (Ideal Components)

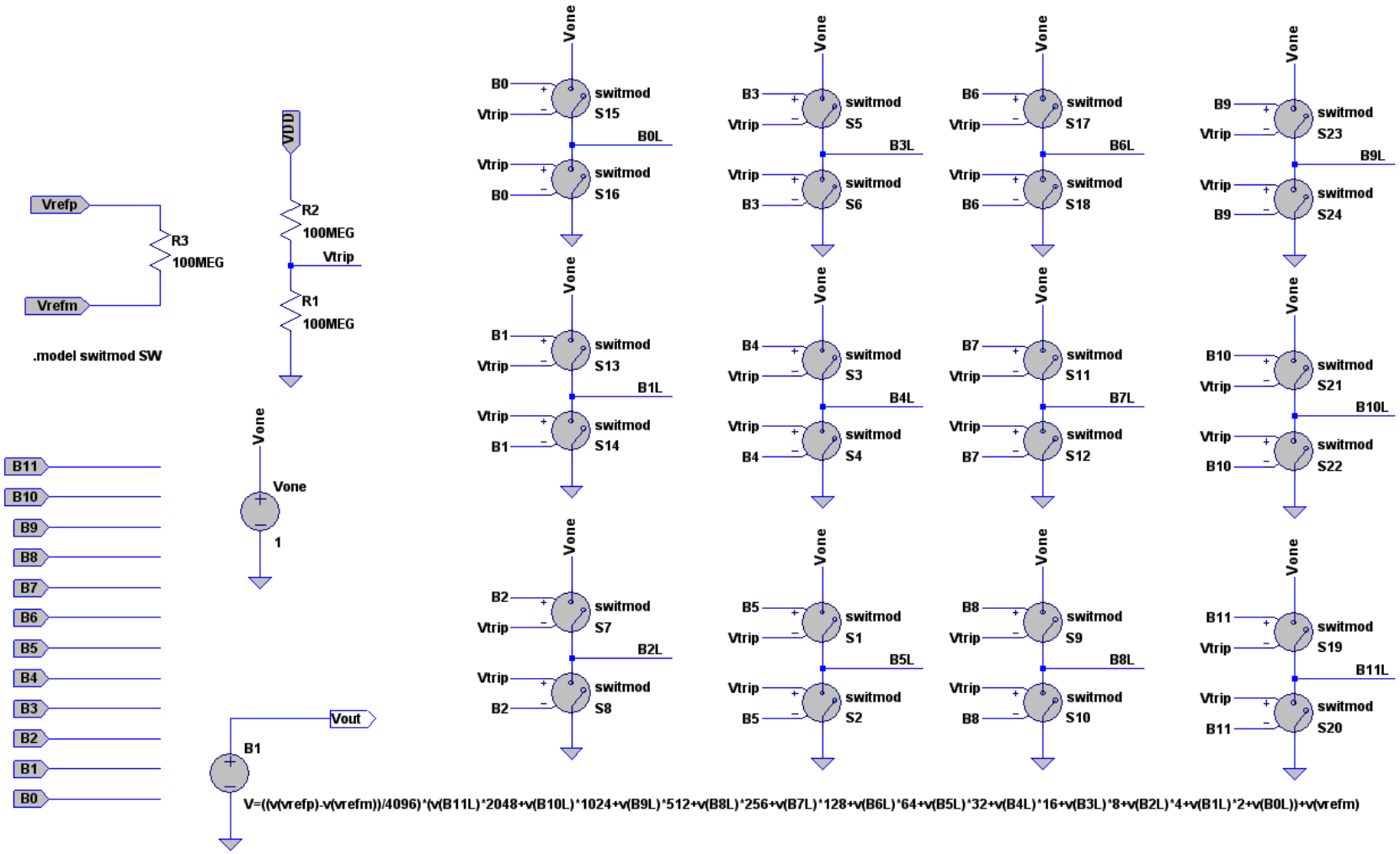

Figure 3.17 LTspice implementation of ideal 12-bit DAC

Figure 3.18 shows a close up of one of these errors, known as monotonic errors, where the output code drops lower for a greater analog input voltage or the output code goes higher for a lower analog input voltage. This type of error will cause multiple analog input voltages to have the same digital output code erroneously.

The simulated pipeline ADC shows primarily ideal results. However, the curve exhibited the prior mentioned monotonic errors and also some instances of DNL and INL greater than 0 LSB.

The cause of the monotonic errors can be found in the ideal voltage characteristic curve for the comparator shown in Figure 3.19. If the input is less than the reference voltage for the comparator then the output goes to ground. Conversely, if the input is greater than the reference voltage for the comparator then the output goes to VDD. The comparator is effectively acting as an ideal single bit ADC. However, if the inputs of the comparator are equal, then the comparator will randomly jump between the two possible output states, because the ideal comparator has infinite gain in this region of operation. This means the transition would happen at precisely the reference voltage as a perfectly vertical line. In reality, this is unachievable and the comparator will have a finite high linear gain. Therefore, at precisely equal inputs the comparator will output an analog voltage which would be midway between the supply rail voltages. This output state would be a digital unknown or ‘X’ region. Fortunately, if the gain of the operational amplifier is large enough, then the presence of noise will provide enough signal level difference in the two inputs for the output to take a ‘0’ or ‘1’ state. Of course, the output will be unstable when the input voltage is near the inverting terminal common mode reference voltage. This instability can cause the comparator to output an erroneous digital level, which will cause a monotonic error in

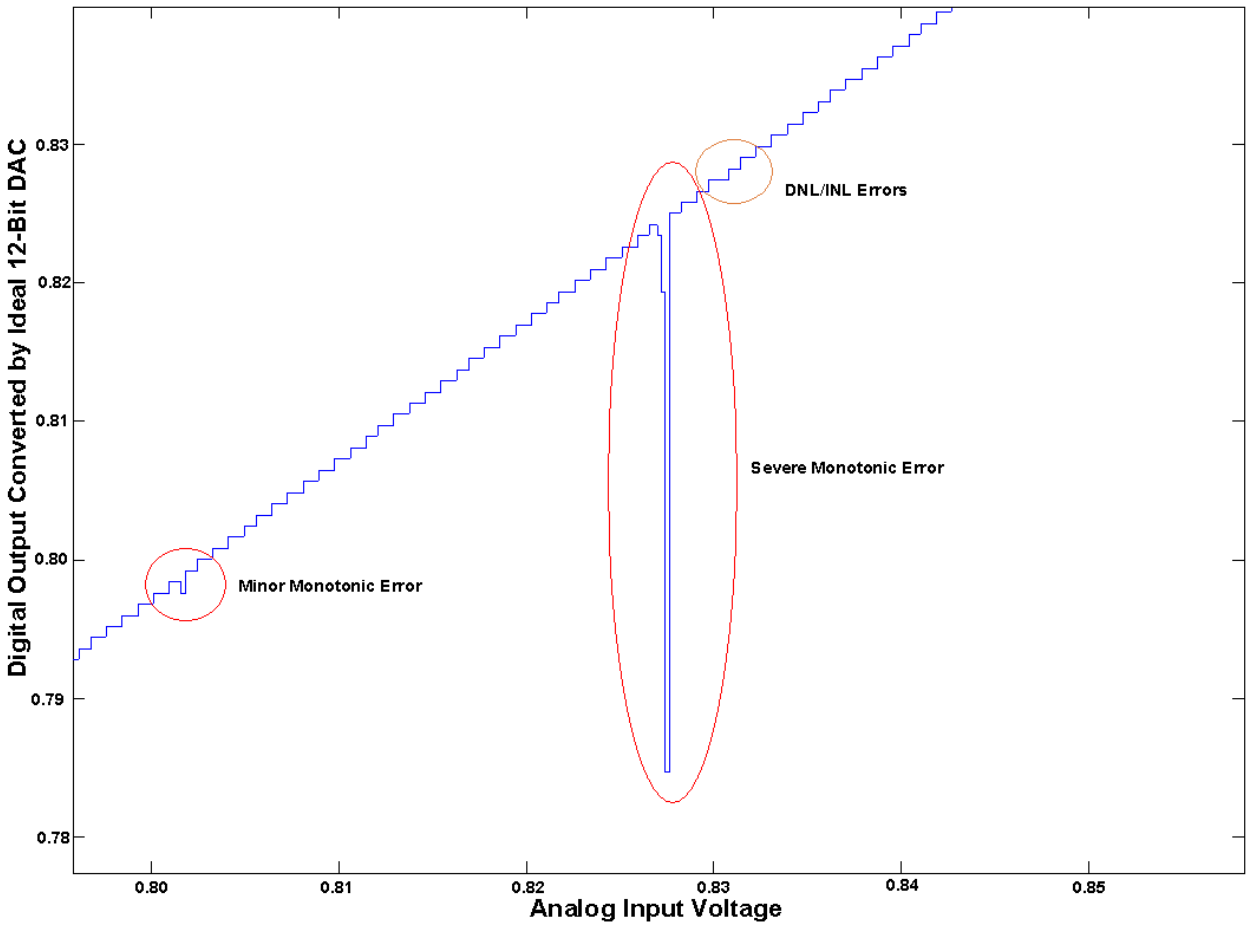

Figure 3.18 Non-idealities found from LTspice simulations

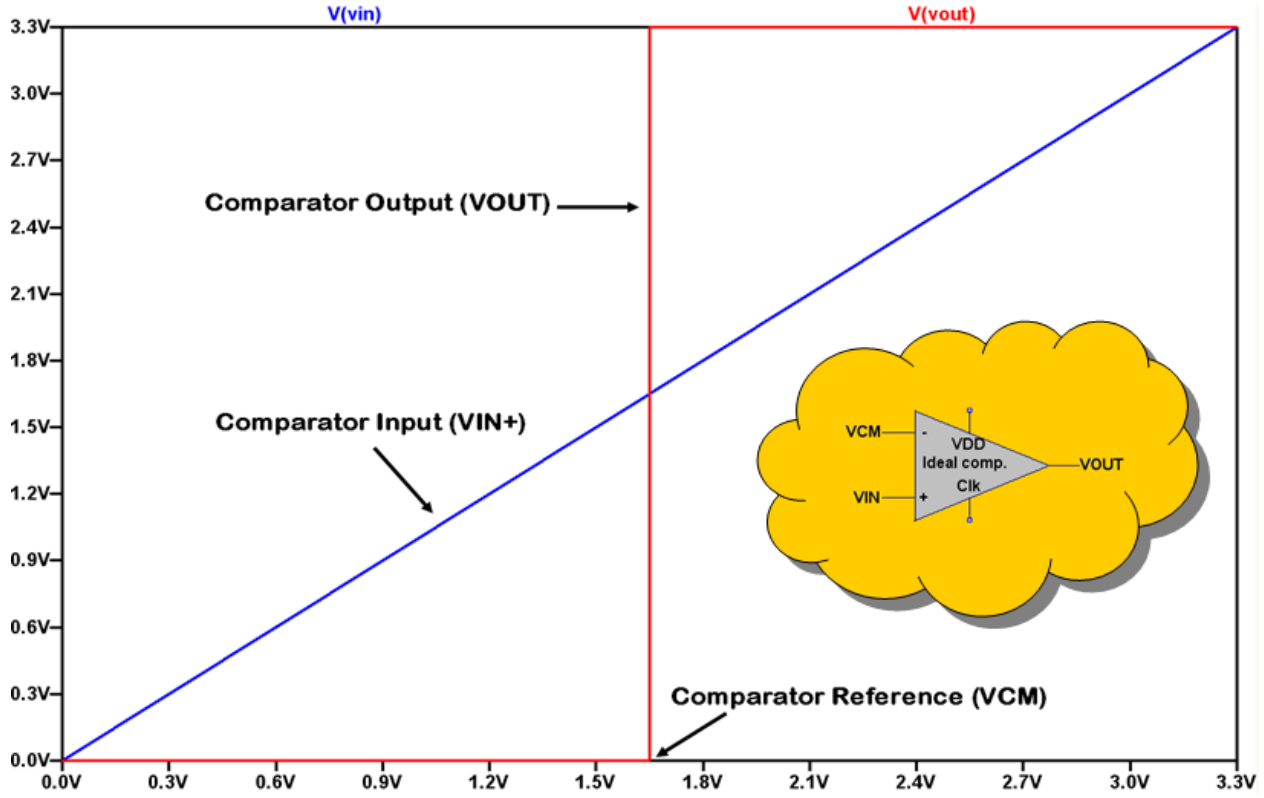

Figure 3.19 LTspice ideal comparator simulation

the output digital level. Depending on which bit the comparator is outputting, the severity of the monotonic error can vary, where the MSB will cause the most severe and the LSB the least. The ideal implementation was also tested for a 100 hertz sinusoidal input. The results of the sinusoidal simulations are shown in Figure 3.20. Notice the same monotonic errors are present in the digitalized sinusoidal input, as expected. Theoretically, they should occur at exactly the same voltages, which they do. The only noticeable difference is on the negative slope of the sinusoid. The monotonic errors are in the reverse direction, so that for a lower voltage the output code is higher than expected as shown in Figure 3.21. Severity is also greatly diminished. This is because the way the simulator is handling the infinite gain region of the ideal operational amplifier being used as a comparator.

Although in a real world application the negative slope could exhibit different characteristic than the positive slope, because of the characteristics of the amplifier being used. Notably, a CMOS amplifier would be expected to have differing slew rates for a positive and negative going signal. The differing rates can cause a comparator implementation to output a specific state near the linear high gain region of operation, depending on the sampling rate. If the sampling rate is sufficiently slow, then the unequal slew rates would not have an influence on a tendency for a specific output.

An example of the LSB falling into this state was shown in Figure 3.18 where a minor monotonic error was noted. The LSB at that specific voltage went to the ground potential instead of VDD because of the incoming voltage to the final stage being equal to the comparator reference voltage. If the same situation occurs at higher bits, the resulting impact on the final conversion is more severe, as noted in Figure 3.18. Note that in Figure 3.16 the most

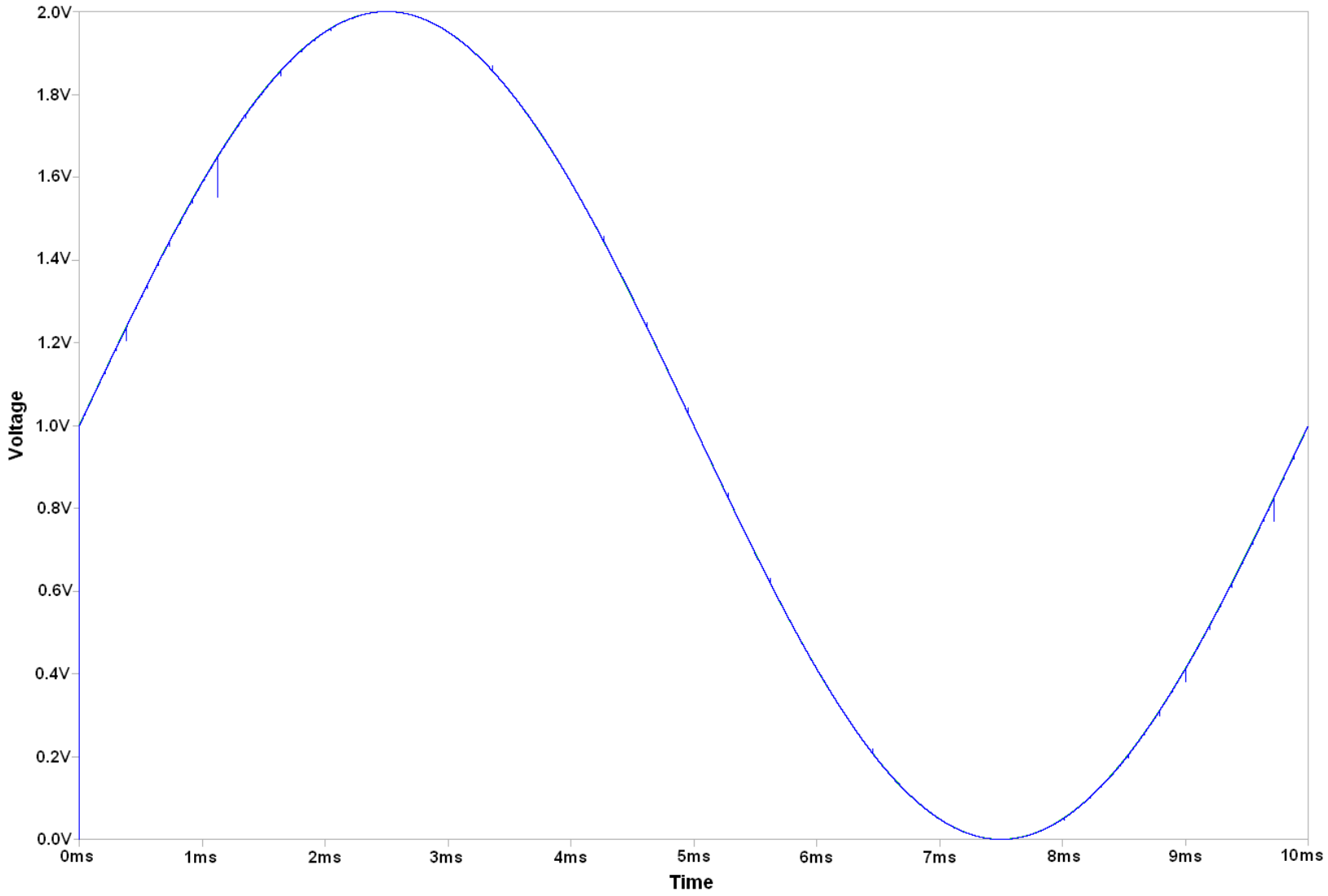

Figure 3.20 LTspice sinusoidal simulation of 12-bit pipeline ADC

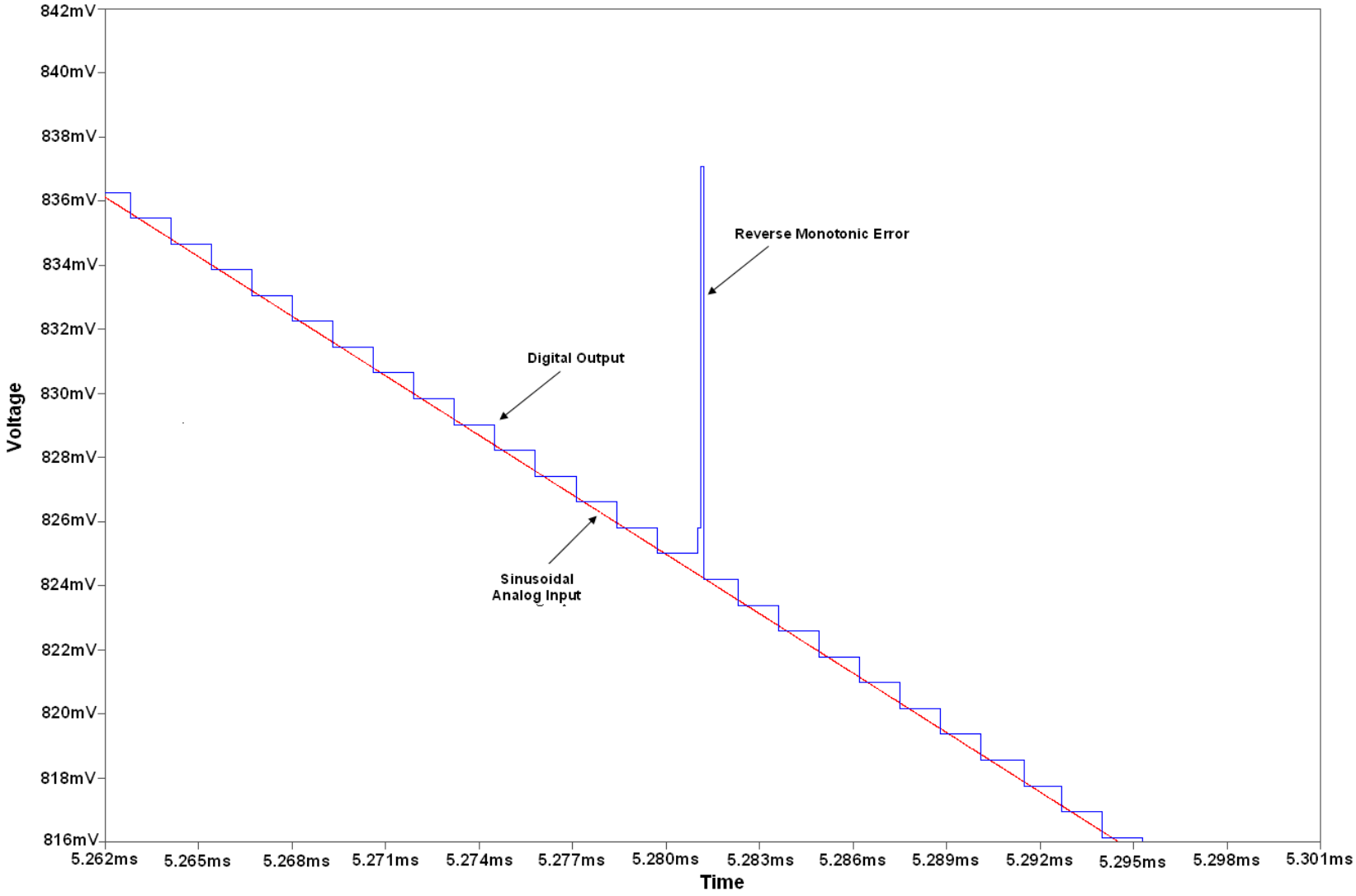

Figure 3.21 Non-ideal characteristics of negative slope from LTspice sine simulations

severe monotonic error occurs at precisely where the input voltage is equal to the comparator reference voltage, which is 1.65 volts. Also notice that the monotonic errors shown in Figure 3.16 occur at voltages defined by equation 3.2.

$$Monotonic\ Error\ Voltage(x) = \frac{VCM}{2^{x-1}} = \frac{1.65}{2^{x-1}} \quad (x = 1,2,3,..., n) \tag{3.2}$$

In order to determine the input voltage to the ADC that will potentially trigger a monotonic error in stage x of the pipeline ADC, where x is equal to 1 for the MSB stage and the number of bits n for the LSB stage, the common mode comparator reference voltage needs to be divided by 2 raised to the $(x-1)$ power. However, equation 3.2 will only identify the fundamental monotonic error voltages. Integer multiples of the fundamental voltages can also trigger monotonic errors. Figure 3.16 demonstrates both statements to be true. Figure 3.22 illustrates an example of a monotonic error triggered on both the first and second stages of an ADC.

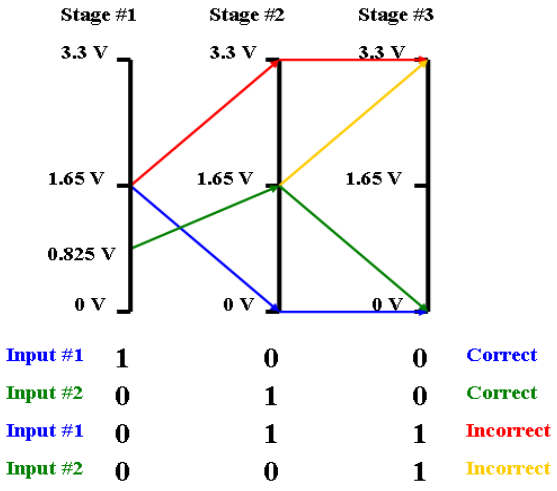

Figure 3.22 Monotonic error conversion example

3.7 Low Pass Filter Design

Earlier during sample-and-hold testing, the presence of 60 hertz noise found at the output of the sample-and-hold circuit was noted as having a peak to peak amplitude of near 20 millivolts. Figure 3.23 shows the results of measuring the VDD supply pin directly. The 60 hertz noise is clearly visible with an amplitude of approximately 50 millivolts peak to peak. In addition to the 60 hertz noise, the supply rail is plagued by a staggering amount of high frequency noise with a maximum measured amplitude of nearly 400 millivolts peak to peak. Clearly the supply rail is not sufficiently filtered.

The ideal situation is to attain a 3.3 V DC voltage for VDD. In order to come closer to achieving this goal, a well designed low pass filter (LPF) needs to be implemented.

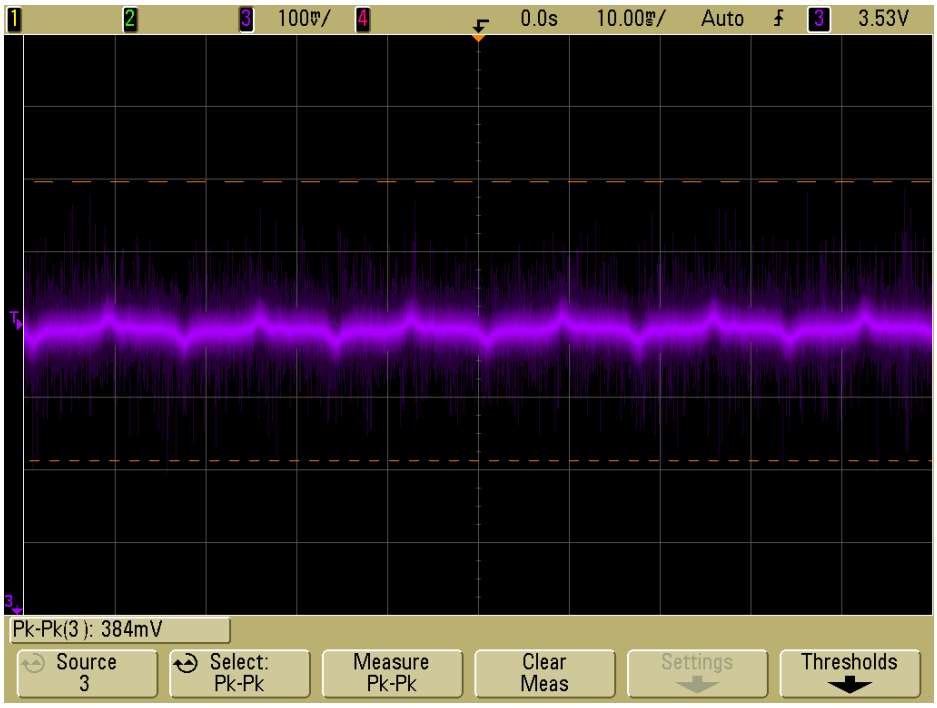

Figure 3.23 Noise on the VDD supply rail

One of the simplest implementations of a LPF is shown in Figure 3.24. The resistor R2 is the measured load resistance and not an actual component in the filter. The AC source V1 is inputting 25 mV peak, or 50 mV peak to peak, into the filter. Finally, the resistor R1 and capacitor C1 make up the simple R-C filter. With the component values shown, Figure 3.25 shows the gain of the network versus frequency. The gain at 60 Hz would translate into the 50 mV peak-to-peak noise signal being reduced to 1.33 mV peak-to-peak. However, the R-C filter will also attenuate VDD. With a VDD of 3.3 volts, the output level would be 3.19 volts. The drop is not significant enough to be a serious problem, but there is a simple addition that can be added to this simple R-C network to mitigate the DC voltage drop.

Figure 3.26 shows the addition of an operational amplifier to the R-C network. The operational amplifier is connected in a buffer configuration, such that the input impedance of the operational amplifier becomes the new load resistance for the R-C network. The input impedance of the JFET input stage operational amplifier being used is on the order of 10^{12} Ω. The resistor R1 is negligibly small compared to the operational amplifier's input resistance, therefore the DC signal attenuation will be negligible as a result. The results shown in Figure 3.27 verify the

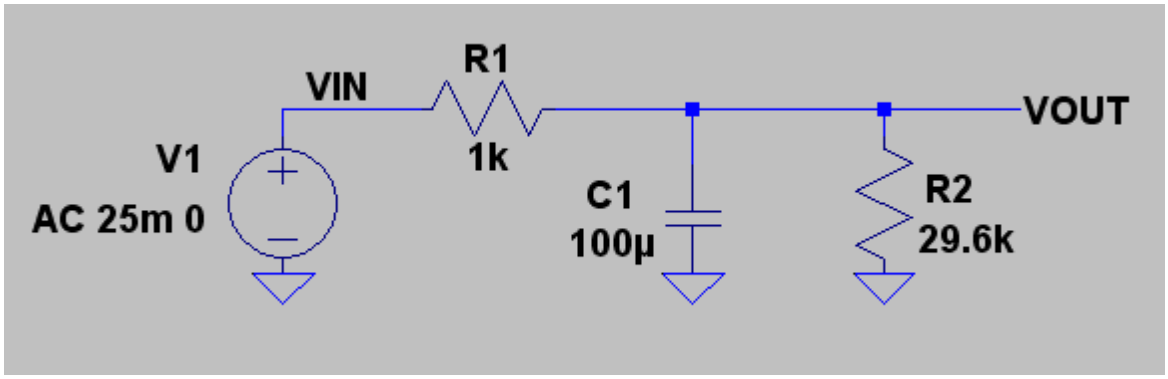

Figure 3.24 R-C LPF schematic

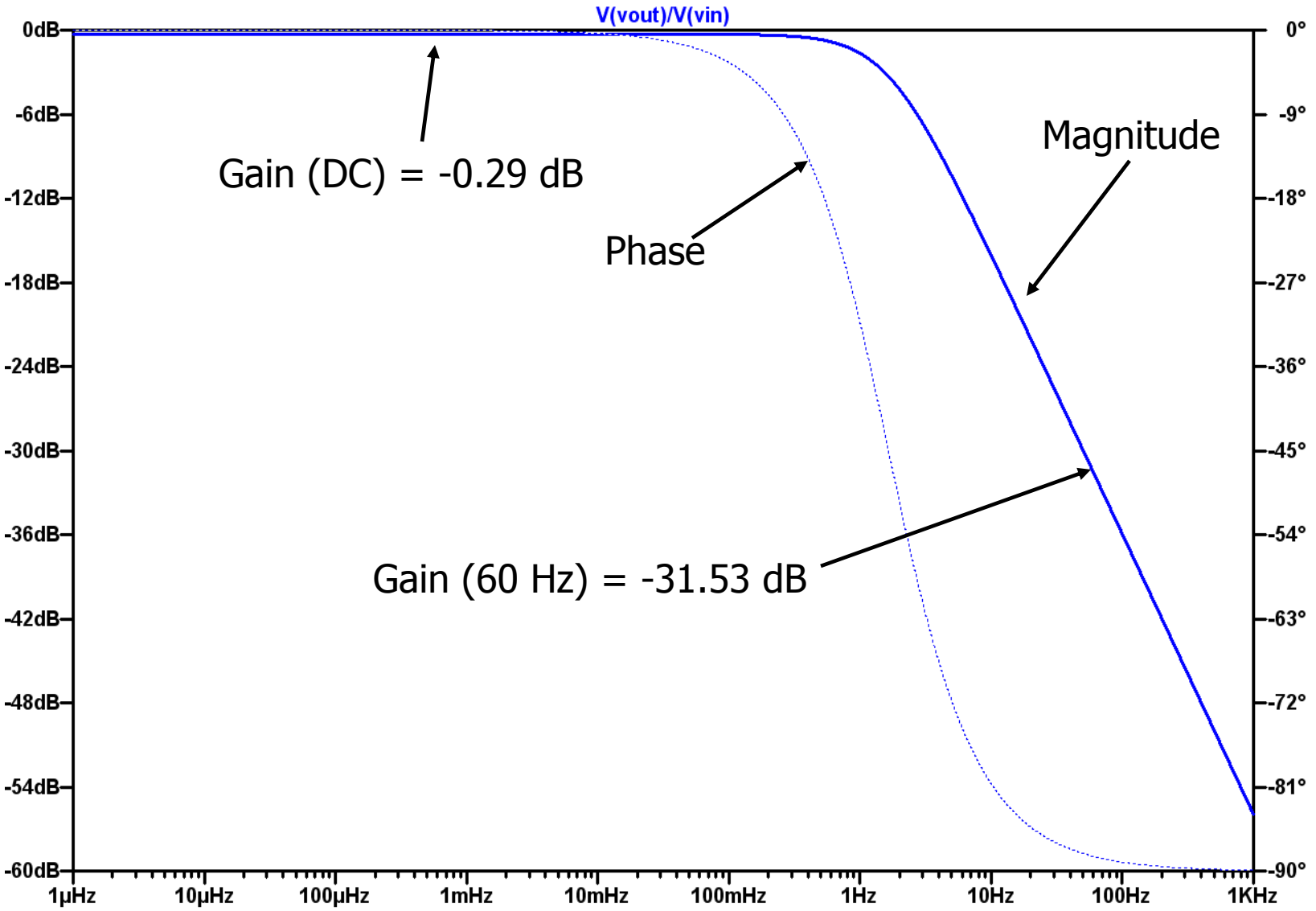

Figure 3.25 Simulation results for simple R-C filter gain (R =1kΩ & C = 100µF)

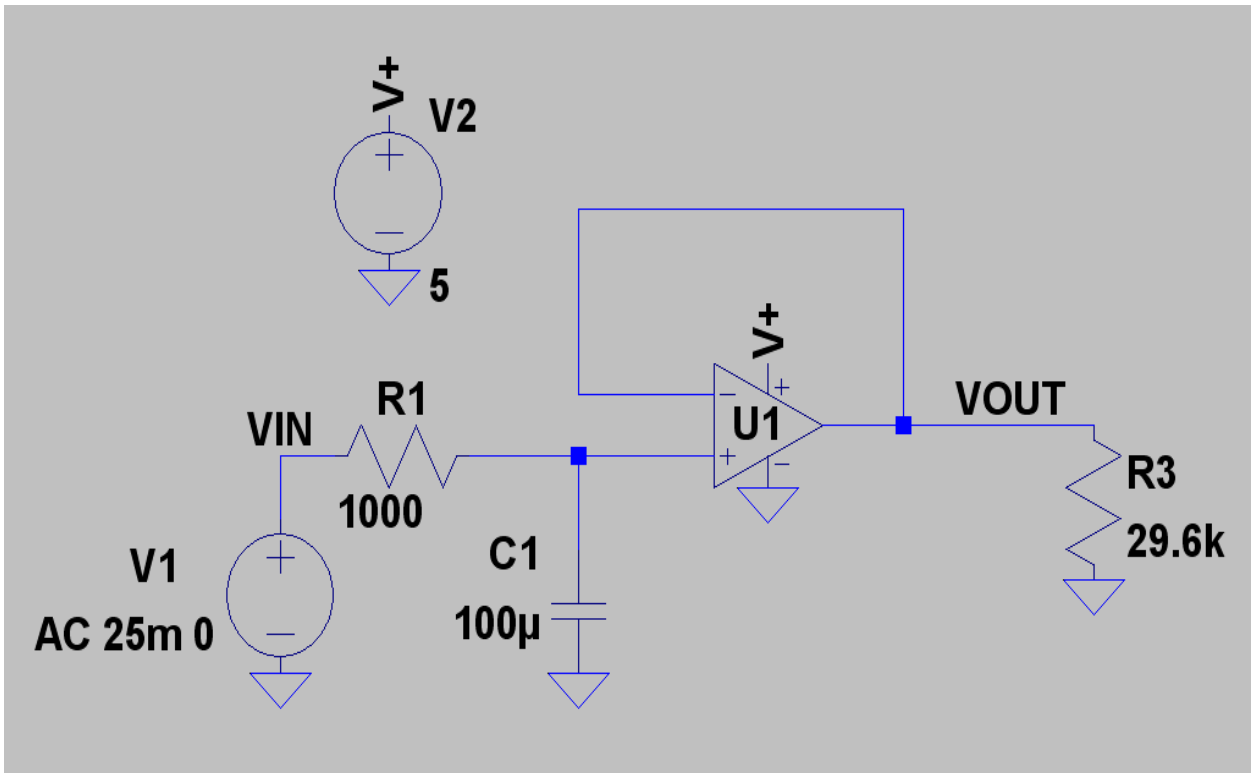

Figure 3.26 R-C LPF with buffered output schematic

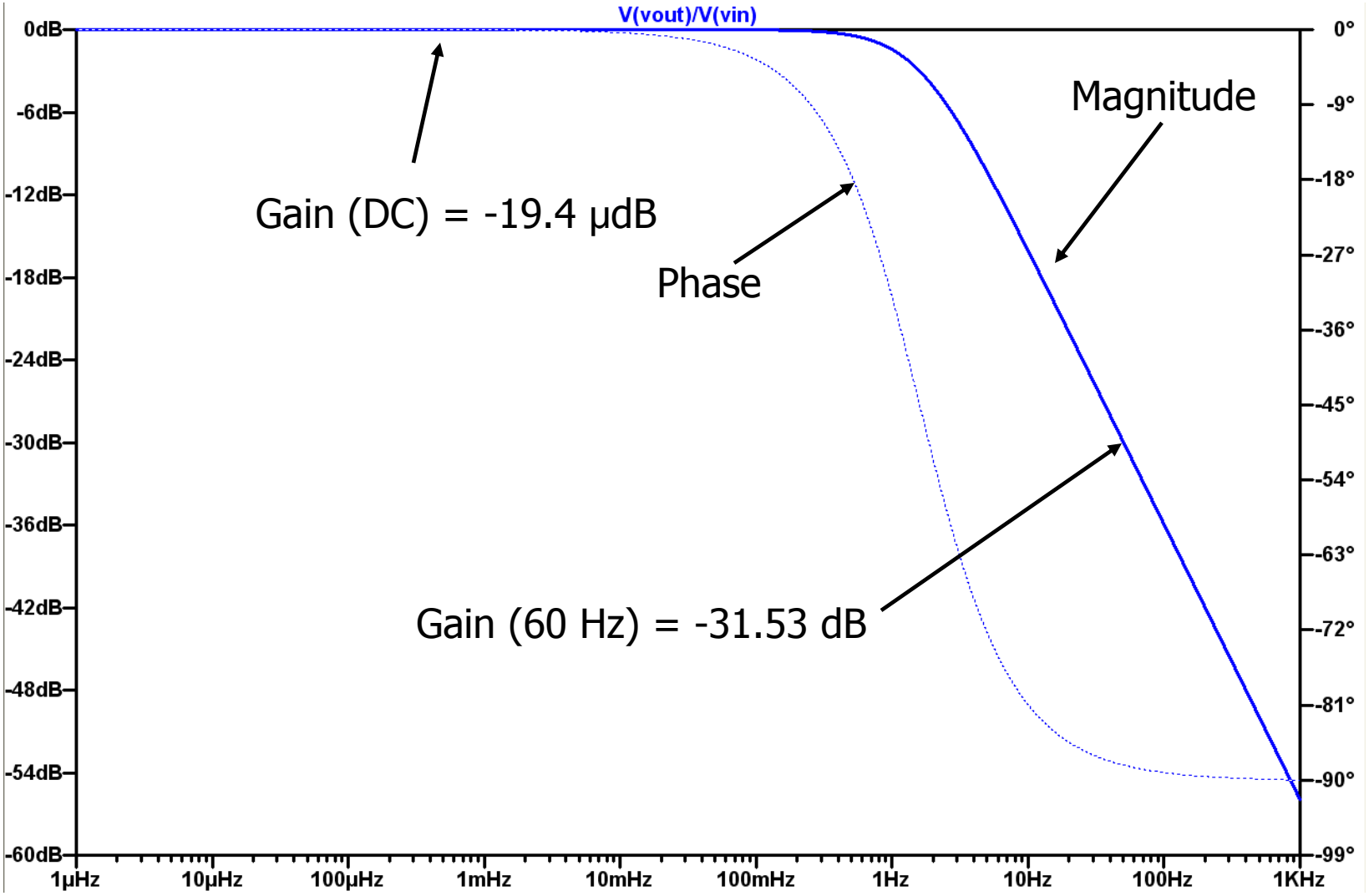

Figure 3.27 Simulation results for simple R-C filter gain with buffered output (R = 1kΩ & C = 100µF)

addition of the operational amplifier buffer significantly reduces the DC attenuation and leaves the 60 hertz attenuation unchanged.

So far the filters shown will bring the 60 hertz "hum" down to a magnitude of approximately 1.33 mV peak-to-peak. The performance on the buffered filter can be further improved in one of two ways. The first method increases the value of either R1 or C1. Since the operational amplifier input resistance is practically infinite, the resistor value can easily be increased without the additional board space a larger capacitor would require. Figure 3.28 shows the simulation results when R1 is set to 38 kΩ. The 60 hertz response dramatically improves, while the DC response only slightly degrades. Also the bandwidth of the filter, as defined by equation 3.3, reduces significantly.

$$BW = f_{-3dB} = \frac{1}{2\pi R_1 C_1} \tag{3.3}$$

Figure 3.29 shows the alternative to simply increasing component values. Instead of scaling the component values, the R-C is cascaded into a R-C ladder network. Figure 3.30 shows the simulation results for a 2 stage R-C ladder network with an output buffer. The multiple stage results show less DC attenuation than the prior method along with identical results at 60 hertz. The main difference between the two methods is that the multi-stage method will introduce a double pole at the same cutoff frequency as a single stage response. Therefore, the slope of the gain after the cutoff frequency is -40 dB per decade. The single stage with scaled components simply shifts the cutoff frequency to a lower frequency, but the slope of the gain

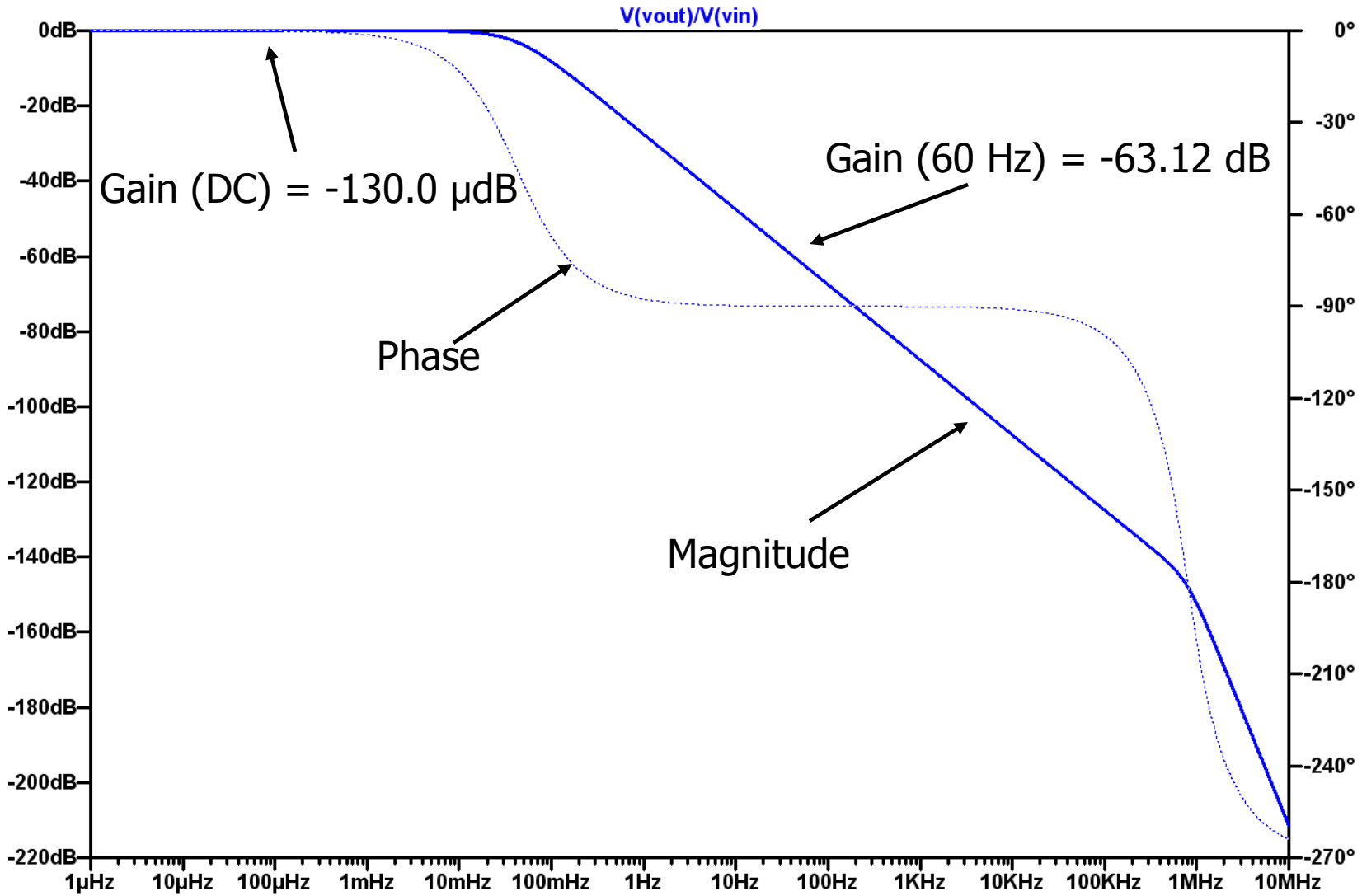

Figure 3.28 Simulation results for simple R-C filter gain with buffered output (R = 38kΩ & C = 100µF)

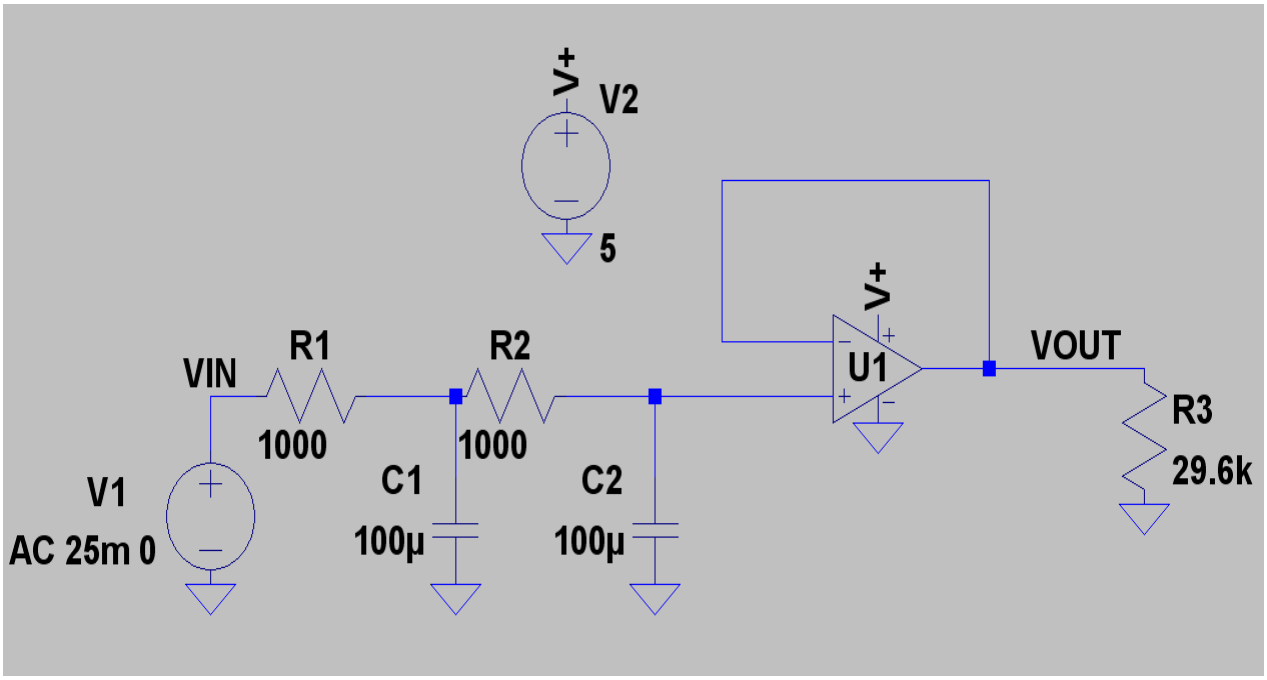

Figure 3.29 Two stage R-C LPF with buffered output schematic

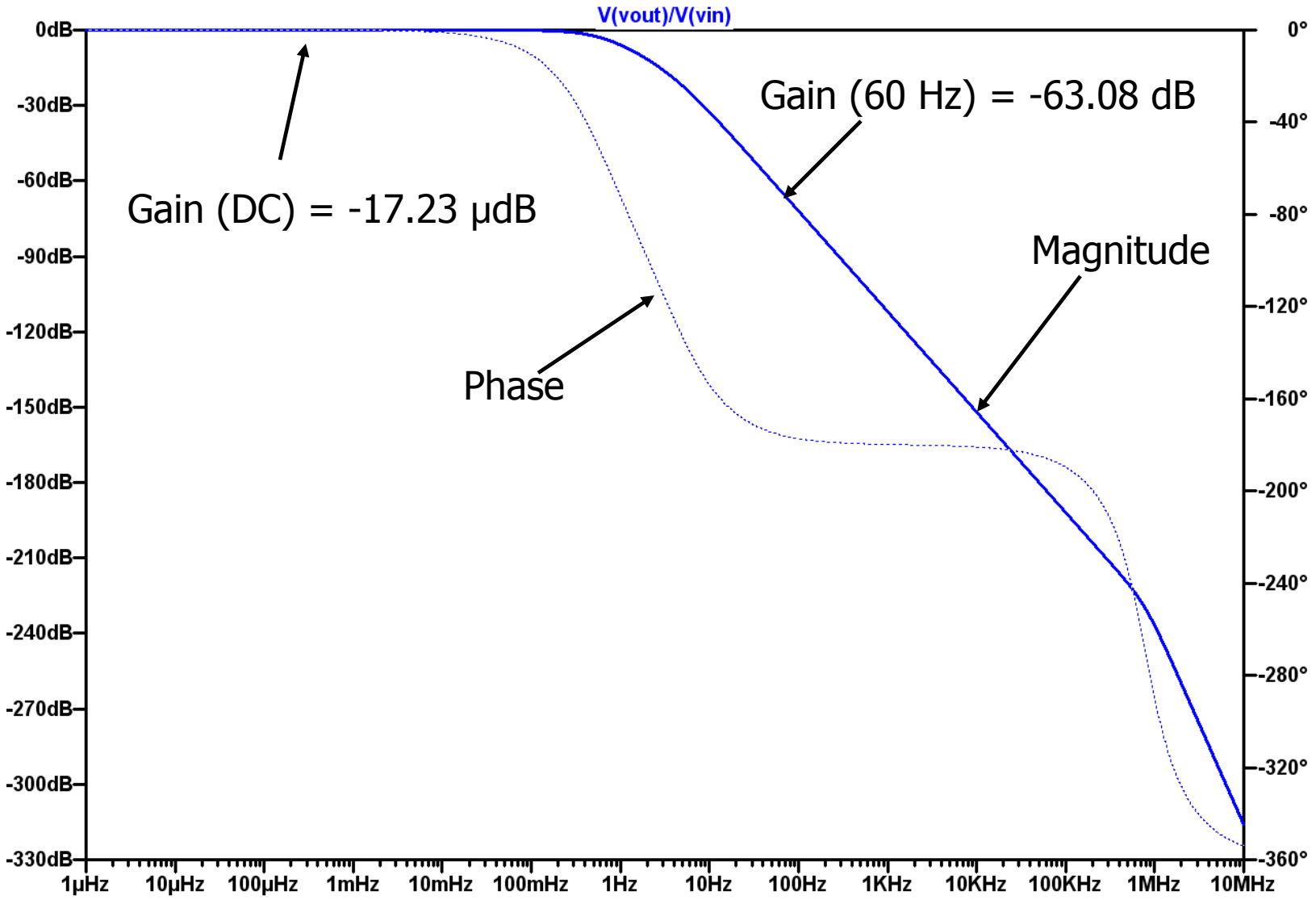

Figure 3.30 Simulation results for two stage R-C filter gain with buffered output (R = 1kΩ & C = 100µF)

after the cutoff frequency is -20 dB per decade. Scaling the components proves beneficial if the cutoff frequency is not low enough. However, the multiple stage technique proves useful in providing a sharper roll off from the cutoff frequency, but it does take up more board space.

There is a hidden danger in the active LPF circuit with the operational amplifier buffer. The supply pins of the buffer could introduce the same 60 hertz noise the filter is trying to eliminate. Although the operational amplifier's power supply rejection ratio (PSRR) will help mitigate this effect, the power supply pins should be filtered with bypass capacitors as close to the operational amplifier pins as possible. The operational amplifier will be using a single ended power supply, so only one power pin is bypassed.

3.8 Implemented Low Pass Filter Results

The final schematic of the LPF implemented is shown in Figure 3.31. The simulation results for the implemented filter are shown in Figure 3.32. The implemented filter took advantage of both component scaling and adding an additional R-C stage. Every filtered node includes an electrolytic, tantalum, and ceramic capacitor to achieve good frequency response. The simulation results show that the configuration will marginally affect the DC voltage and severely attenuate any noise found on the supply rail.

Figure 3.33 shows an oscilloscope measurement of the filter's effectiveness. The filter reduces the noise level by an order of magnitude. Therefore the implemented filter only achieves -10 dB attenuation, as contrasted with the simulated -104.73 dB. There are two fundamental reasons why this is the case. First, the model used for the operational amplifier in the simulator is generic. Even if the model were specific to the TL082CP, the model would need to be at the transistor level in order to best demonstrate the effects of a varying supply voltage.

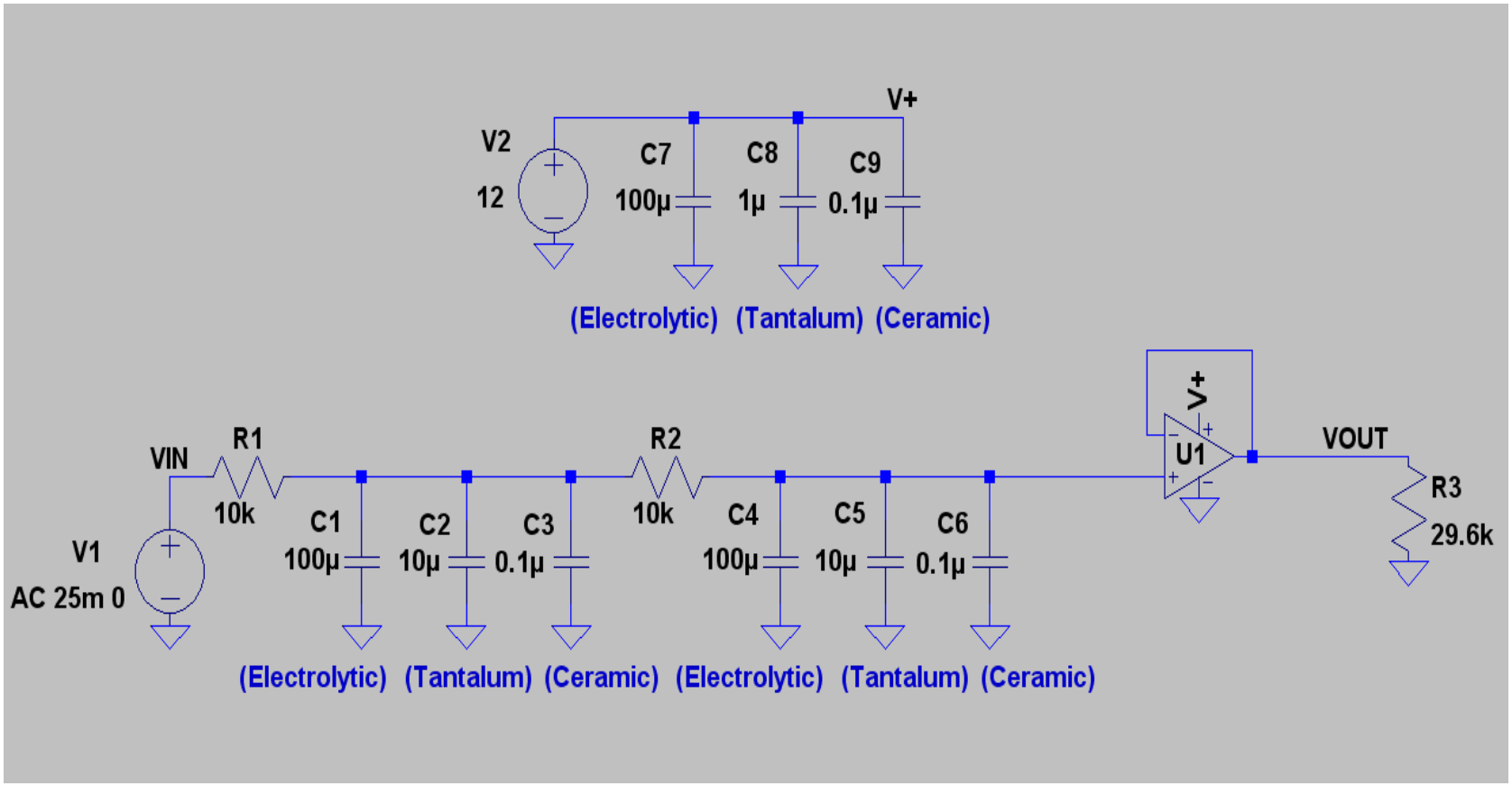

Figure 3.31 Implemented LPF schematic

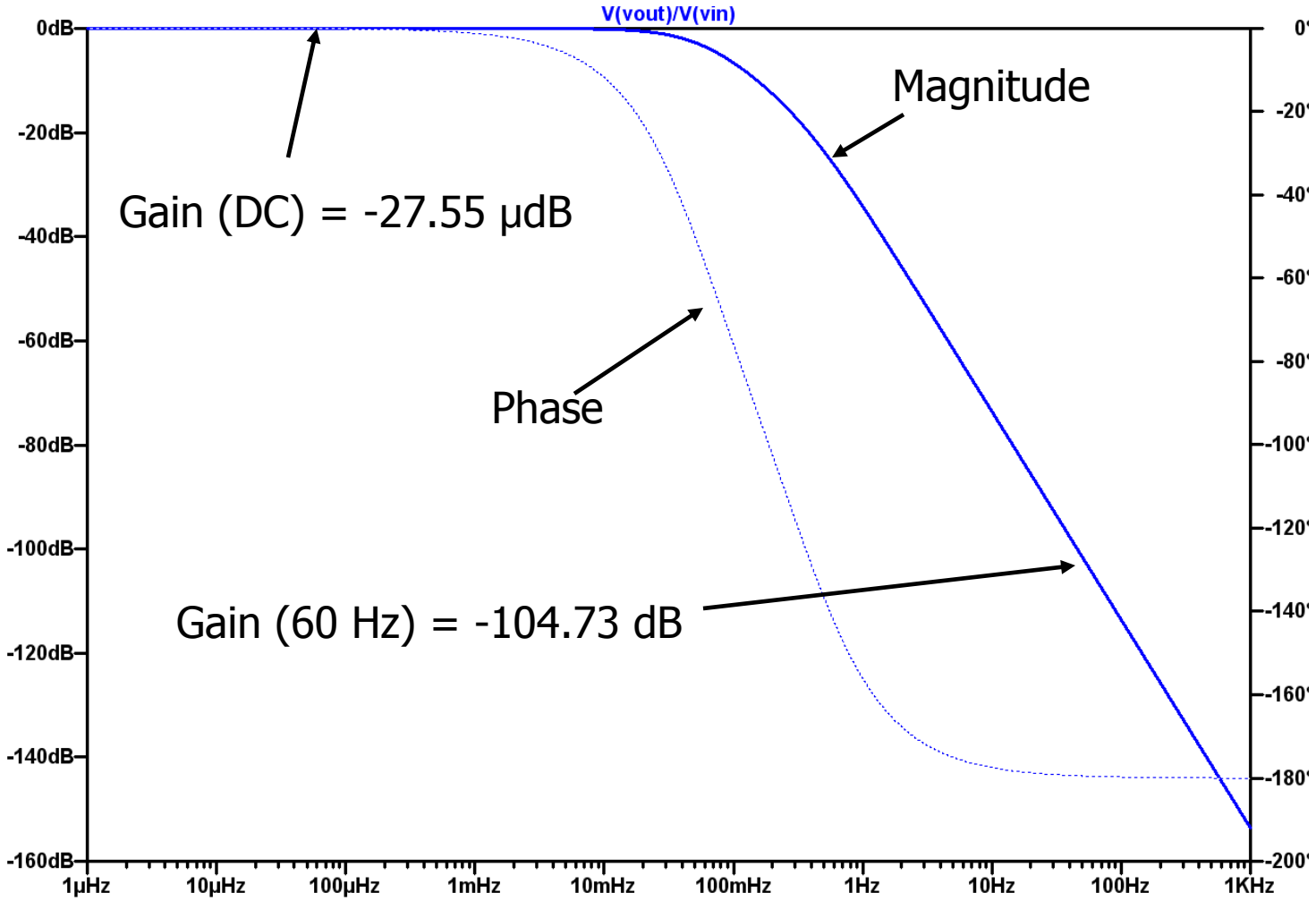

Figure 3.32 Implemented filter gain simulation results

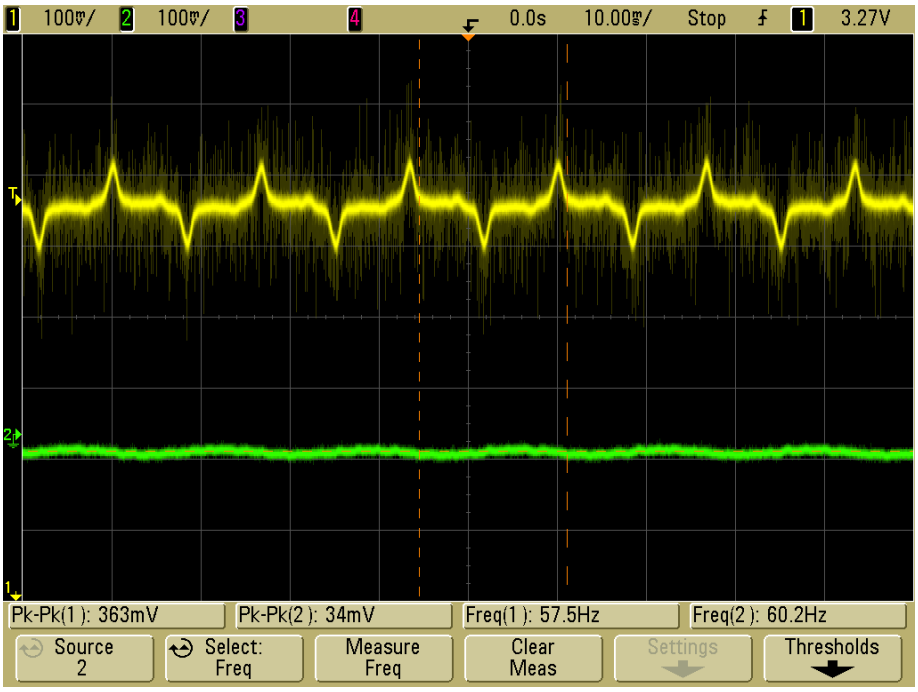

Figure 3.33 Measurements of LPF input (Yellow) and output (Green)

Secondly, the environment has a noise floor that is present throughout the UT1 Thyatira chip, test board, implemented filter, and even the oscilloscope measuring the filter. Regardless, the filter works sufficiently. This can be demonstrated by re-measuring the sample-and-hold output voltage. Figure 3.34 shows the re-measurements of the sample-and-hold circuit output with no clock signal or input signal supplied. The yellow signal is the positive output, the green signal the negative output, and the purple signal the differential output. Compare the new results with Figure 3.6, which was measured before the addition of the filter. The differential output has improved by nearly a factor of 14. A sinusoidal input was used to test the sample-and-hold again, which is shown in Figure 3.35. The sample-and-hold circuit functionality has been improved by the filtering of the supply rail.

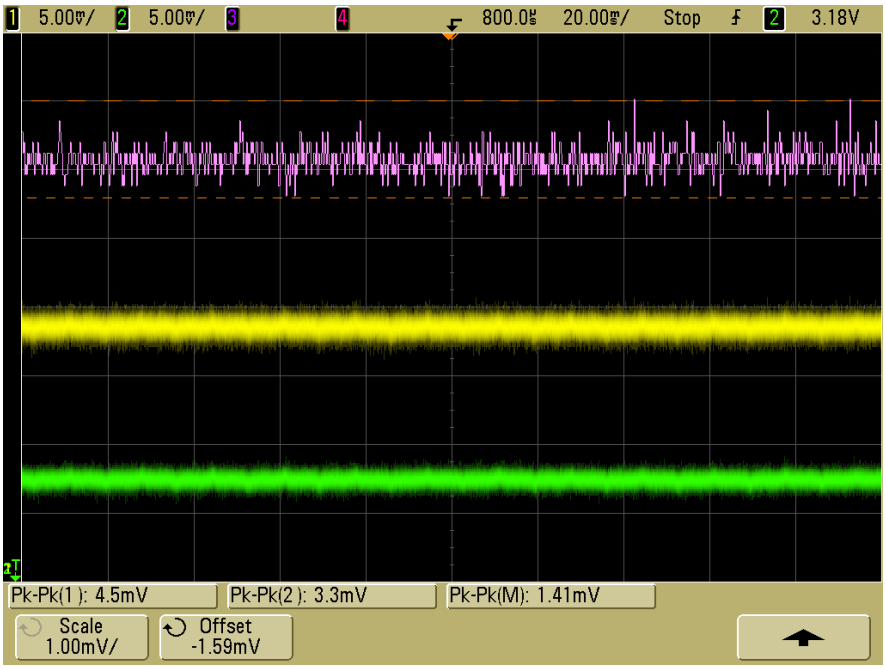

Figure 3.34 Sample-and-hold output with no input/clock (Filtered VDD)

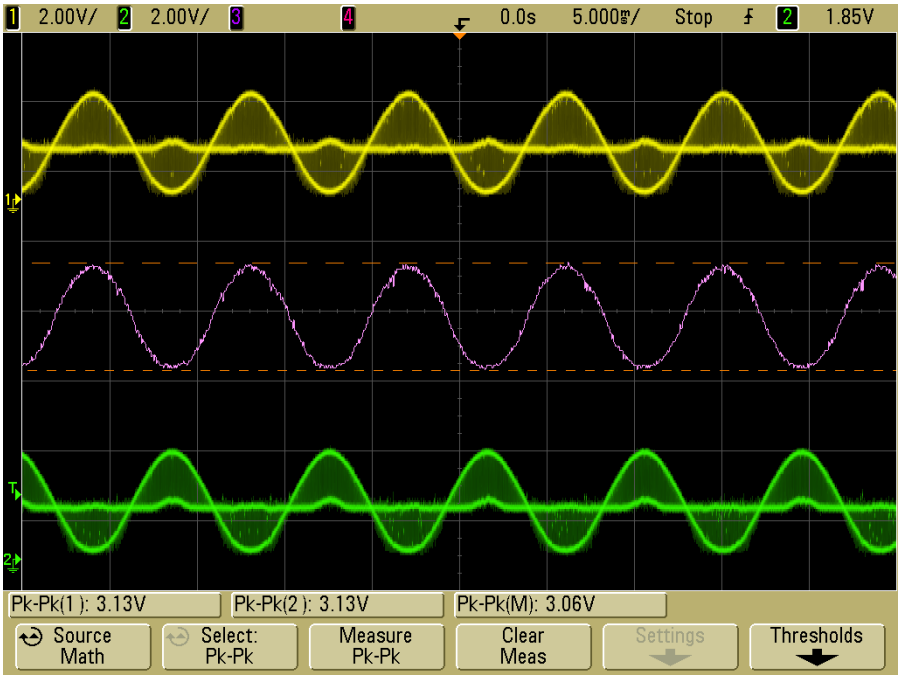

Figure 3.35 Sinusoidal output of sample-and-hold (Filtered VDD)

Chapter 4 Results and Discussion

As mentioned earlier, the ADC was only characterized for its DC characteristics which include the DNL, INL, gain error, and offset error.

The testing required the use of a full range sinusoidal input. A full range sinusoid means the waveform is centered on the ADC characteristic curve with a DC offset equal to half the ADC's reference voltage and the amplitude is sufficient to trigger all code levels. Typically the sinusoid is given an amplitude that slightly exceeds the ADC's range to ensure that all code levels get exposure. Upwards of 131,000 samples were retrieved from the ADC for each test. Using the gathered samples, a histogram was produced that showed how often the code levels were triggered. The upper and lower code extremes were discarded, as theoretically these output levels have infinite width. This is sensible because if the input is out-of-range, then the ADC will default to one of these outputs, assuming the out-of-range voltage does not damage the ADC.

The DC characteristics of the ADC can be determined from the histogram plot by understanding that the number of hits for a specific code level is proportional to the code level width [2]. Prior to discussing the more complicated sinusoidal formulas, the formulas used for the ramp input are discussed first. In order to identify the characterization parameters, the number of code hits H(x) must be defined by the histogram. Next, the average number of hits is defined, shown by equation 4.1 [2].

$$H_{AVG} = \frac{1}{2^n - 2} \sum_{x=1}^{2^n-2} H(x) \tag{4.1}$$

Notice the first and last codes are omitted from the average. The omitted codes provide a misleading amount of coverage because the step width is undefined at the extremes. Thus they are omitted to prevent skewed results. This is especially true for a sinusoidal input where the voltage lingers around the extremes for greater periods of time than it remains at the voltages between the extremes. Equation 4.2 [2] can be used to compute the width of each code's step in units of LSBs.

$$Code\ Width(x) = \frac{H(x)}{H_{AVG}} \text{ (LSB)} \tag{4.2}$$

Once the width of each step is known relative to an LSB, the next step is to determine the average LSB for the ADC experimental using equation 4.3 [2], where V_{UE} and V_{LE} are the upper most transition and lower most transition voltages respectively.

$$V_{LSB} = \frac{V_{UE} - V_{LE}}{2^n - 2} \tag{4.3}$$

The accuracy associated with the characterization using the histogram method is inversely proportional to the average number of code level hits [2]. Another complication with the histogram test is that results can change over time. It is difficult to get a histogram characterization to produce consistent results [2].

All equations up to this point only work accurately for a relatively slow ramp input. Since a sinusoidal input is used, equations suitable for a sinusoidal input need be discussed. A perfect

sinusoidal wave will provide more exposure to the higher and lower level codes than the middle codes. For this reason, new equations based on the ideal distribution of levels triggered by a sinusoidal input need to be utilized instead of using the simple averaging equation. First the DC offset and amplitude of the input sinusoid, as seen by the ADC, can be calculated from the histogram results using equations 4.4 and 4.5, respectively [2].

$$Offset = \left(\frac{C_2 - C_1}{C_2 + C_1} \right) \left(2^{n-1} - 1 \right) \text{ (LSB)} \tag{4.4}$$

$$Amplitude(Peak) = \frac{2^{n-1} - 1 - Offset}{C_1} \text{ (LSB)} \tag{4.5}$$

For all equations, n is the number of bits for the tested ADC, which in this case would be 12. C_1 and C_2 are defined by equations 4.6 and 4.7, respectively [2].

$$C_1 = \cos\left(\pi \frac{H(2^n - 1)}{N_S} \right) \tag{4.6}$$

$$C_2 = \cos\left(\pi \frac{H(0)}{N_S} \right) \tag{4.7}$$

In both equations 4.6 and 4.7, N_S is the total number of samples taken and includes the end codes as well [2]. The rule of thumb that should be followed is to have at least 32 samples for each output code level as shown in equation 4.8 [2].

$$Samples\ (Minimum) = (32)(2^n) = (32)(2^{12}) = 131072 \tag{4.8}$$

Therefore all characterization testing should retrieve at least 131072 samples to achieve reliable results. However, for a sinusoidal input the lower and upper extreme codes will have more exposure; therefore, a larger amount of samples than this minimum should be acquired to ensure that the middle codes will also achieve the minimum 32 sample exposure for acceptable results.

In order to determine the width of each digital output code level with a histogram generated by a sinusoidal input, equations 4.9 and 4.10 need to be used in lieu of equations 4.1 and 4.2 [2].

$$H_{Sine}(x) = \frac{N_S}{\pi}\left[\sin^{-1}\left(\frac{x+1-2^{2-1}-Offset}{Amplitude(Peak)}\right) - \sin^{-1}\left(\frac{x-2^{2-1}-Offset}{Amplitude(Peak)}\right)\right] \tag{4.9}$$

$$Code\ Width(x) = \frac{H(x)}{H_{Sine}(x)}\ \text{(LSB)} \tag{4.10}$$

Equation 4.9 provides the probable number of hits for a specified output level for an ideal ADC, but not the exact number. Note the probable value should not be expected to be an integer value [2].

The best waveform collected to date from the ADC is shown in Figure 4.1. Notice the noise is greater closer to the zero code. Unfortunately the waveform also does not extend to all code levels. The waveform never descends to code zero or ascends to code 4,095. If the amplitude and DC offset were adjusted to correct for this, then the results degenerate by displaying more noise than signal.

The raw data histogram is shown in Figure 4.2. It is encouraging to note that the histogram does exhibit a general "bathtub shape", as it should. However, there are numerous missed codes, not even including the range of codes that were not extended to by the input signal. The normalized histogram is shown in Figure 4.3. An ideal ADC would have a completely flat normalized histogram with a value of 1 LSB across all codes. However, this is not the case with these results. In some places the code widths are close to 1 LSB, whereas in other places the code widths are drastically wider than 1 LSB. The widest step is nearly 46 LSBs.

Figure 4.4 reveals the DNL for the ADC. The only reason the DNL graph looks similar to the shape of the normalized histogram is because of the outrageously wide steps. Had the normalized histogram been more acceptable, the DNL graph would not go beyond ±0.5 LSB. As shown in Figure 4.5, there are portions of the DNL curve that are within the tolerable range. However, Figure 4.5 also depicts where the DNL reveals missing codes.

Figure 4.6 shows the measured curve characteristic of the ADC plotted alongside the best fit line the ADC curve should have followed. Needless to say, the measured ADC characteristic

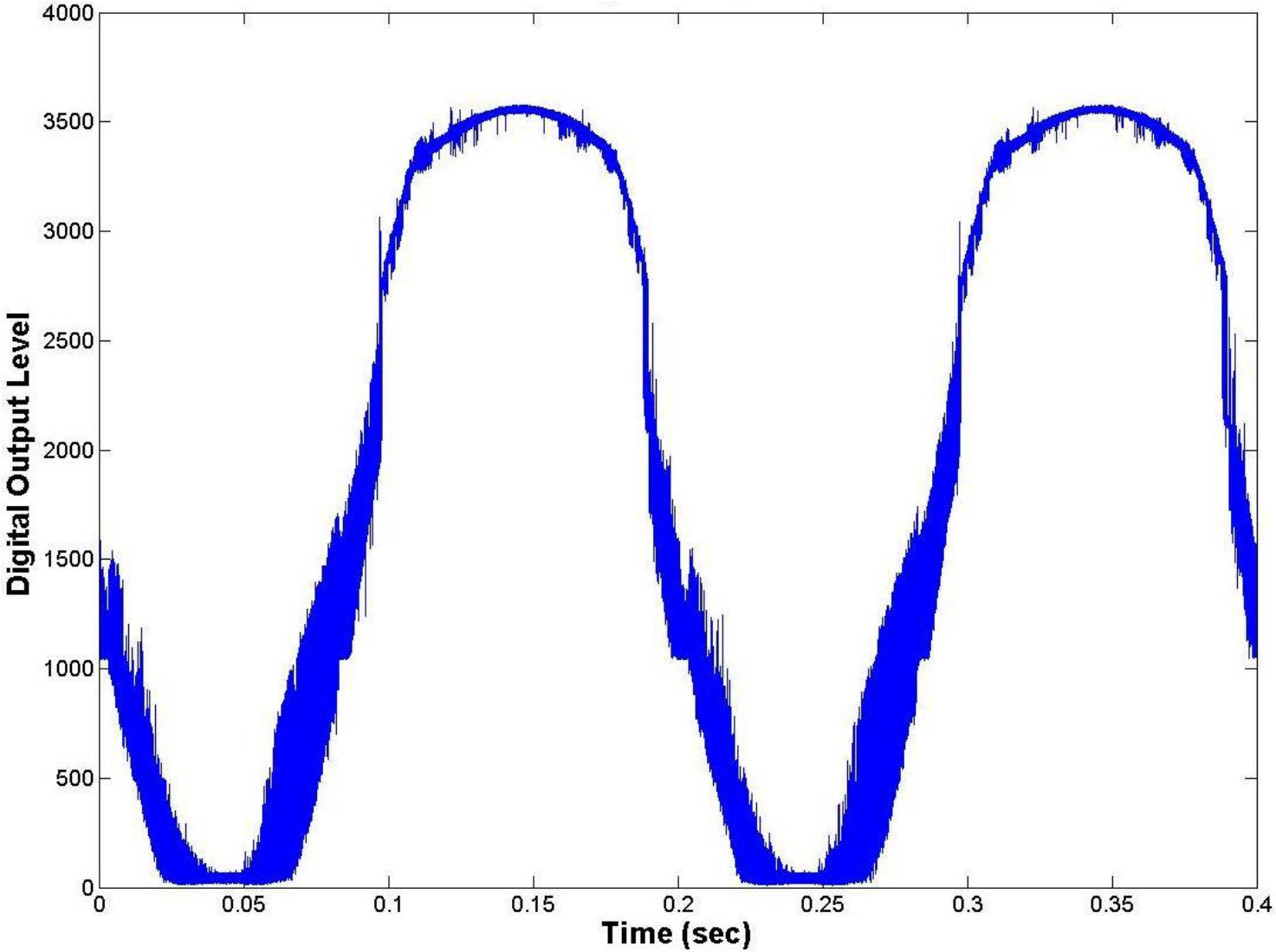

Figure 4.1 Measured ADC output waveform (Noisy Supply)

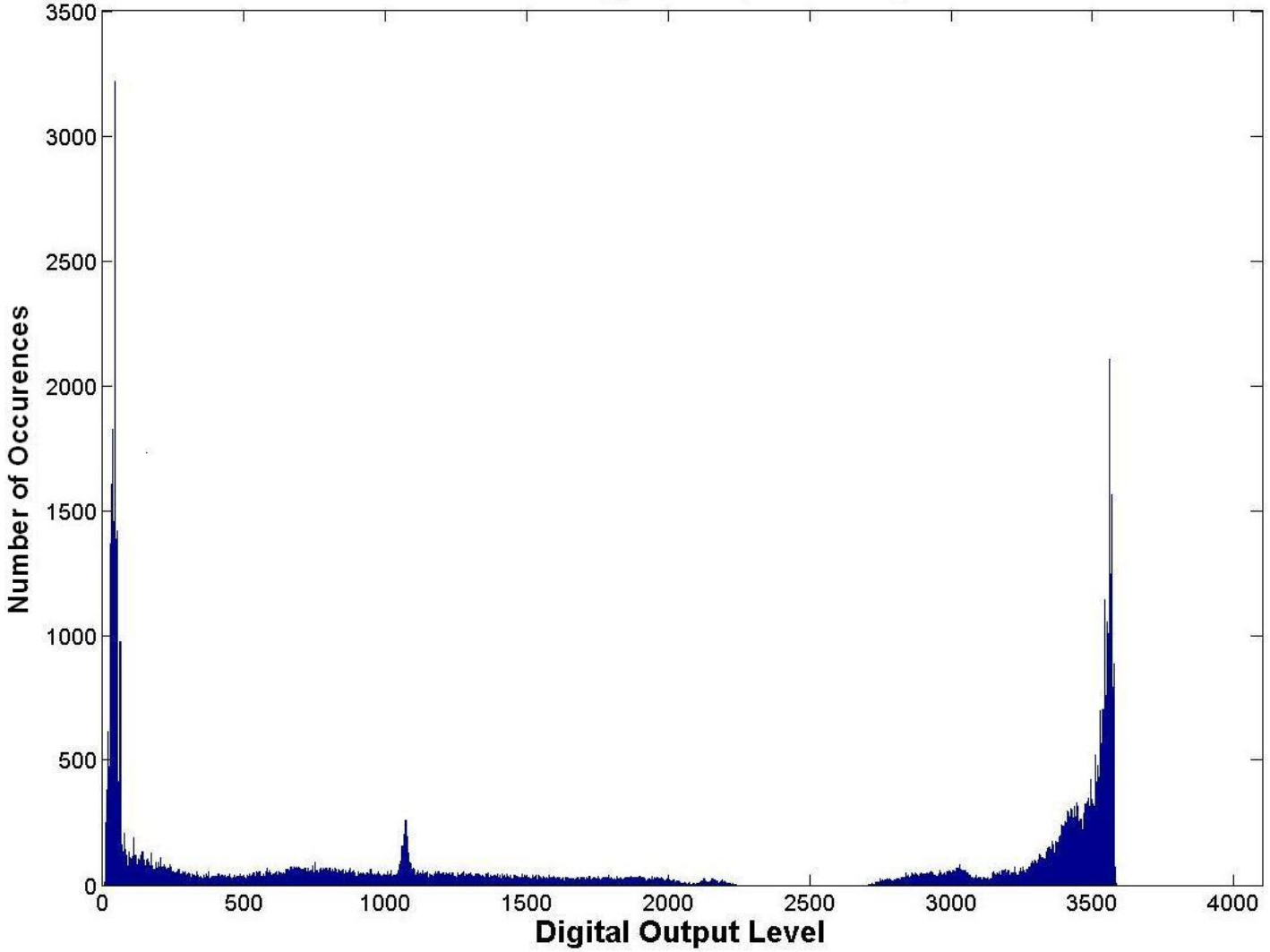

Figure 4.2 Measured raw ADC output data histogram (Noisy Supply)

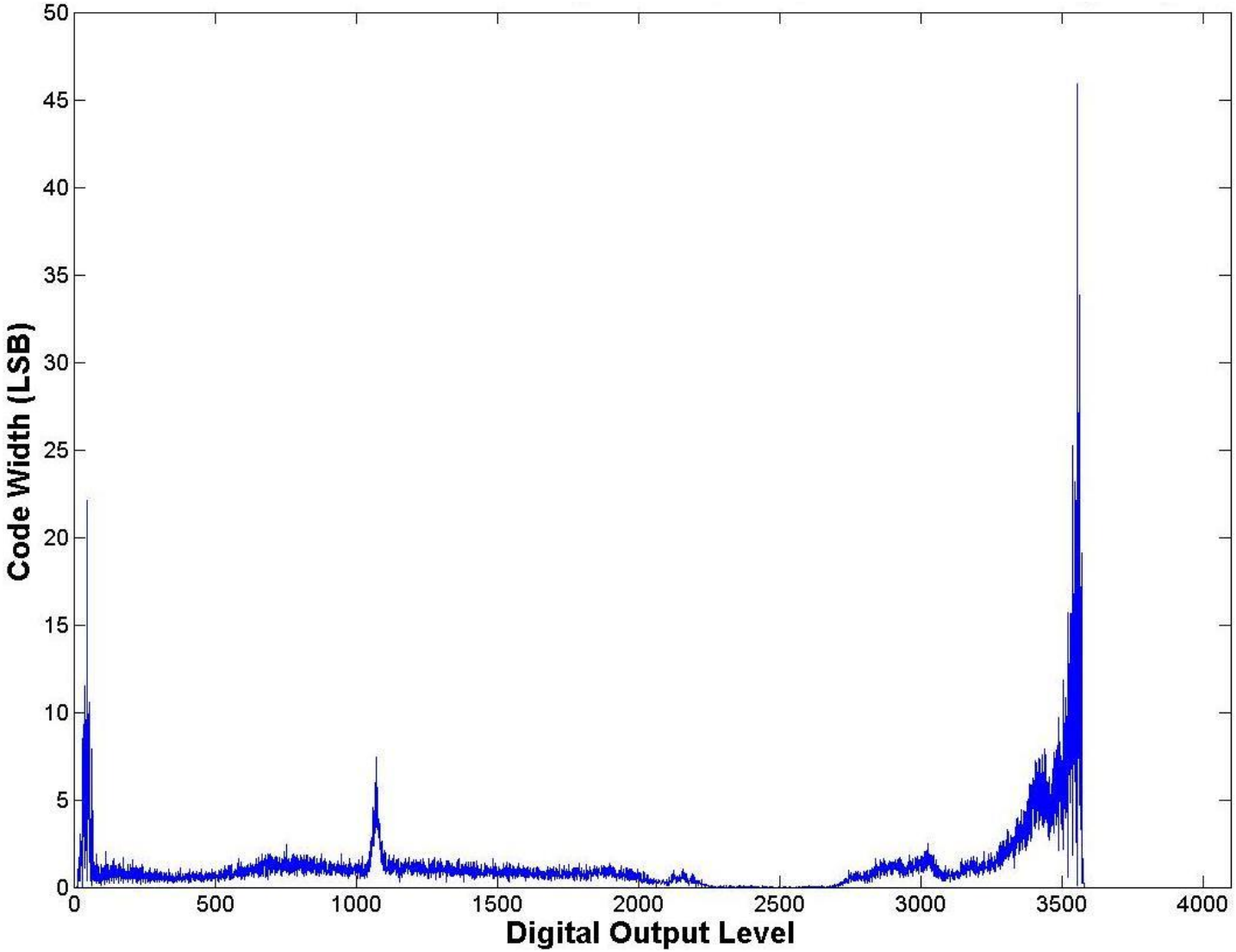

Figure 4.3 Normalized histogram showing code step widths (Noisy Supply)

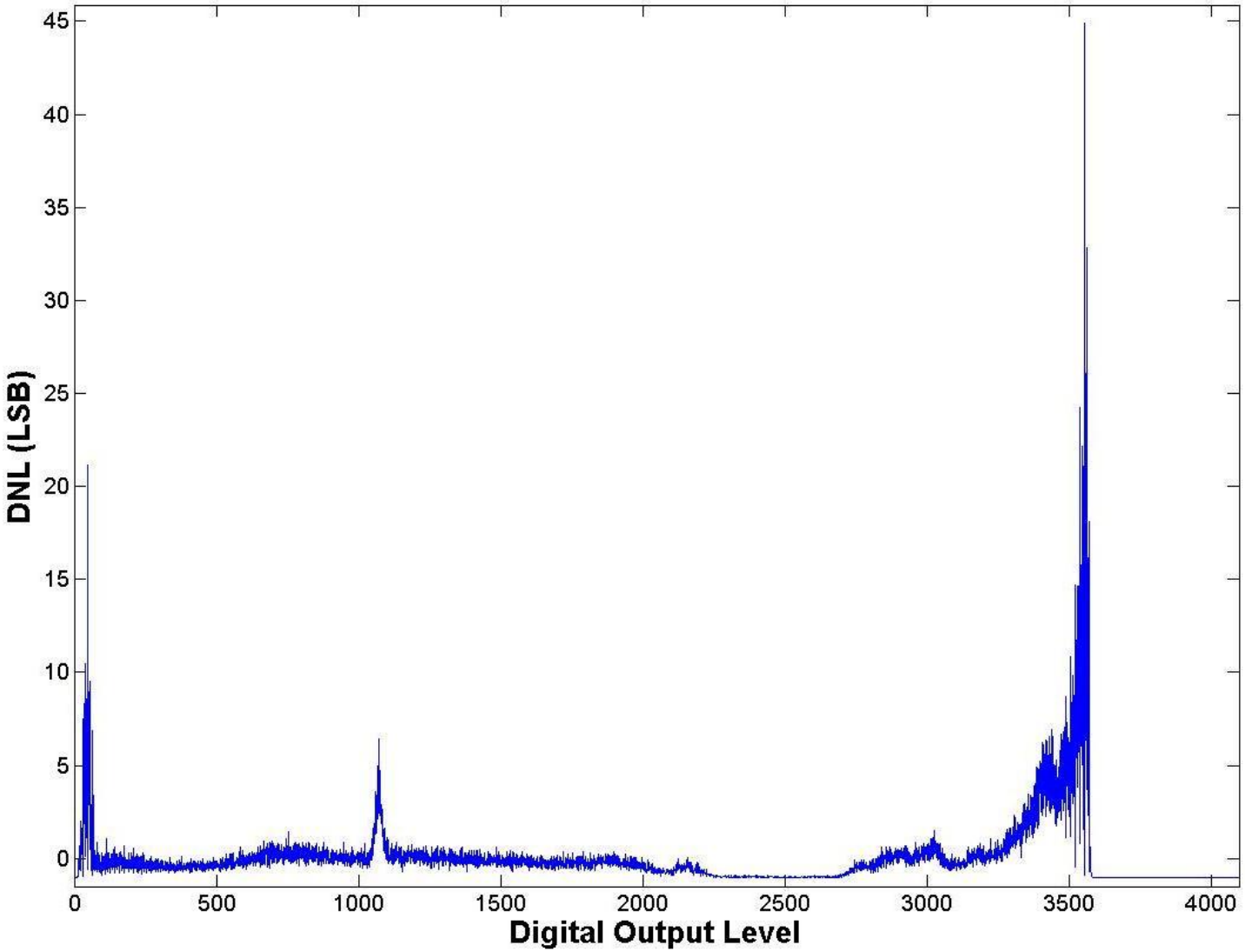

Figure 4.4 Measured DNL curve (Noisy Supply)

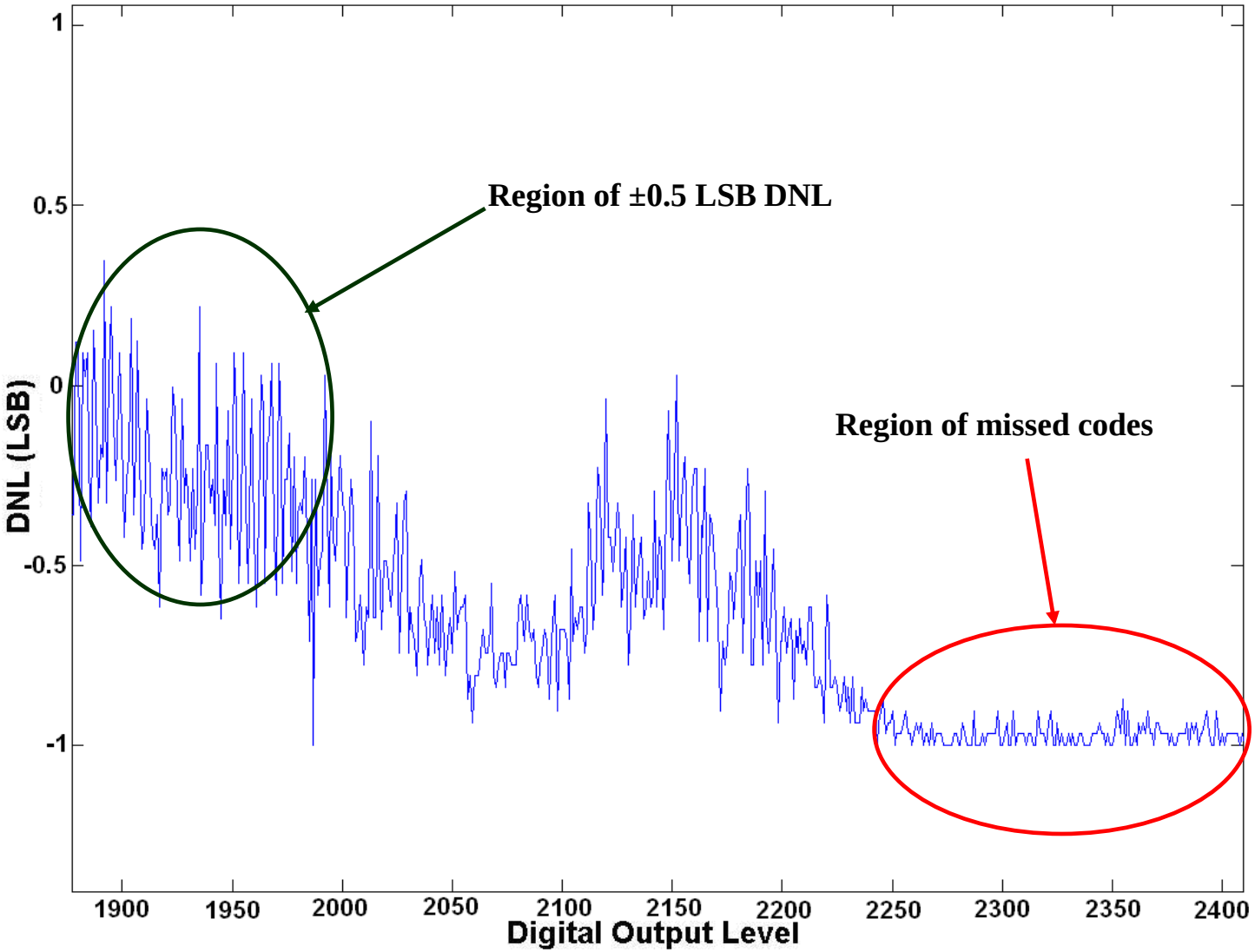

Figure 4.5 Close-up of DNL curve showing missed codes (Noisy Supply)

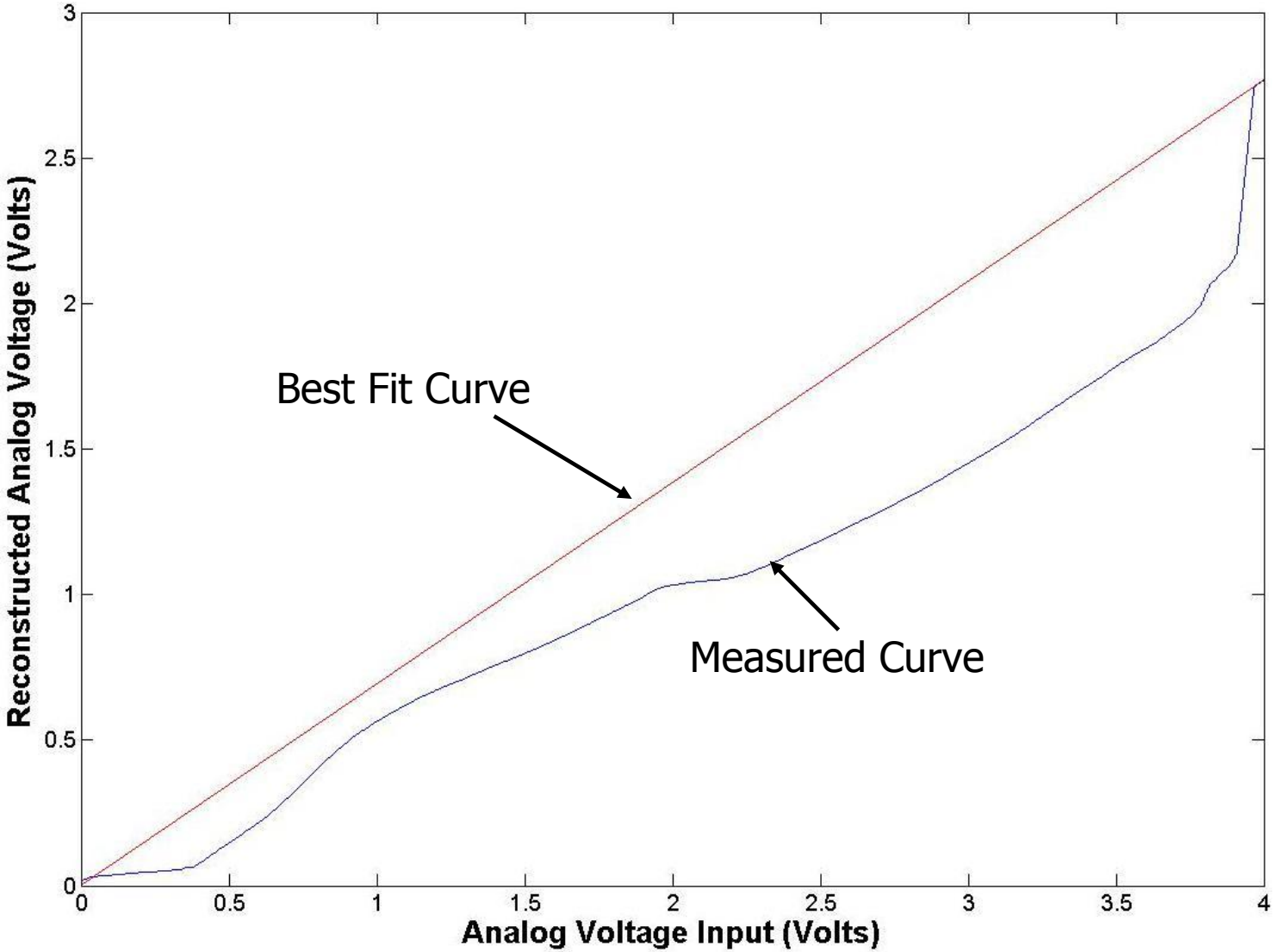

Figure 4.6 Measured voltage characteristic curve and best fit line (Noisy Supply)

diverges greatly from the best fit line. This will, of course, translate to an enormous INL as shown in Figure 4.7.

Using the best fit line, the DC offset error is determined to be 0.4237 LSB or 414 μV and the gain error is determined to be -0.17, meaning the slope is 0.83 instead of the ideal case of unity.

The results shown so far were gathered with a noisy supply rail. Some new results were gathered after the supply rail had been filtered by the LPF mentioned earlier. Figure 4.8 shows the re-measured waveform. Notice the new waveform has brief regions where the ADC is functioning properly. During the testing process, these regions only appeared periodically. A majority of the ADC output is still noisy. It is encouraging to see improvement though. Figures 4.9, 4.10, 4.11, 4.12, and 4.13 show the remaining new characteristic plots. The results remain less than satisfying, however the ADC is working better with a filtered supply rail.

With the supply rail filtered, the question arises as to why the results continue to disappoint. The sample-and-hold is functioning properly, and the supply voltage is filtered. The only portion of the pipeline ADC that has gone untested individually is the comparator found in each stage performing a coarse 1-bit conversion. Figure 4.14 shows the comparator reference voltage. Somewhere either on the test board or the UT1 Thyatira chip the sample-and-hold circuitry is coupling with the comparator reference voltage. The resulting reference voltage for the comparators changes every clock cycle. An example of the resulting impact on the final conversion is shown in Figure 4.15, which uses the measured comparator reference voltage from Figure 4.14. The time varying comparator reference will destroy the linearity of the ADC and produce mistaken output levels.

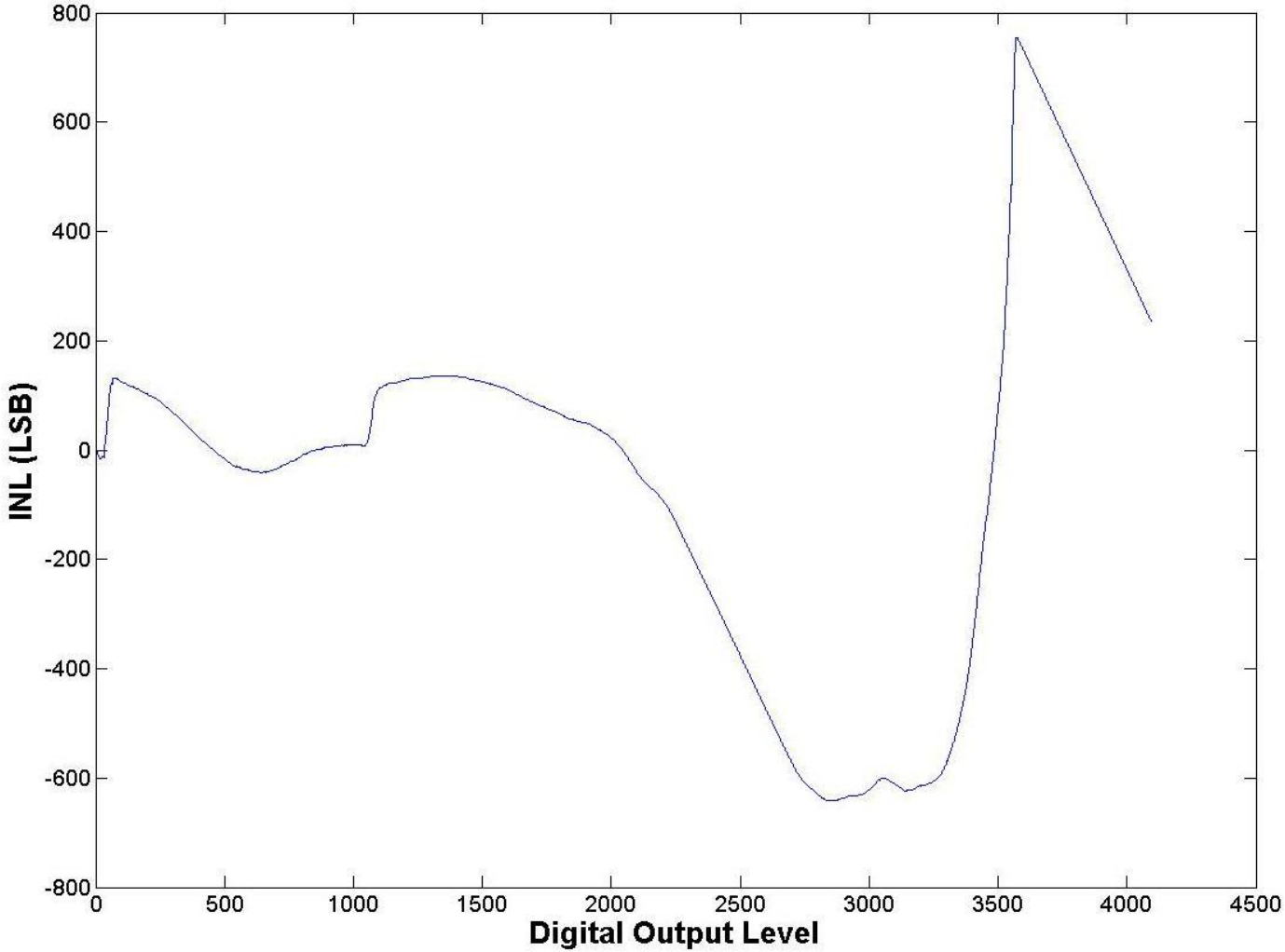

Figure 4.7 Measure INL curve (Noisy Supply)

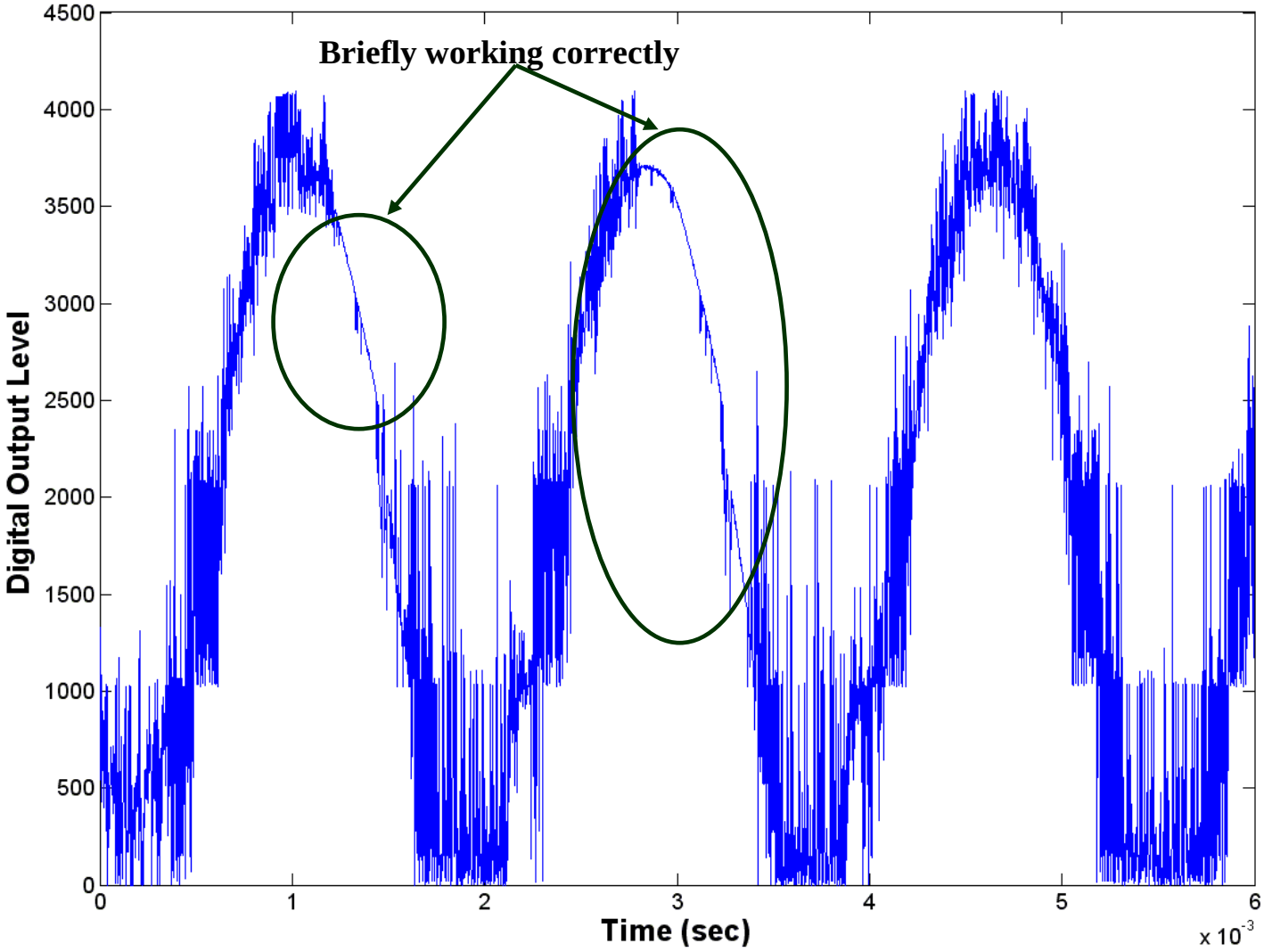

Figure 4.8 Measured ADC output waveform (Filtered Supply)

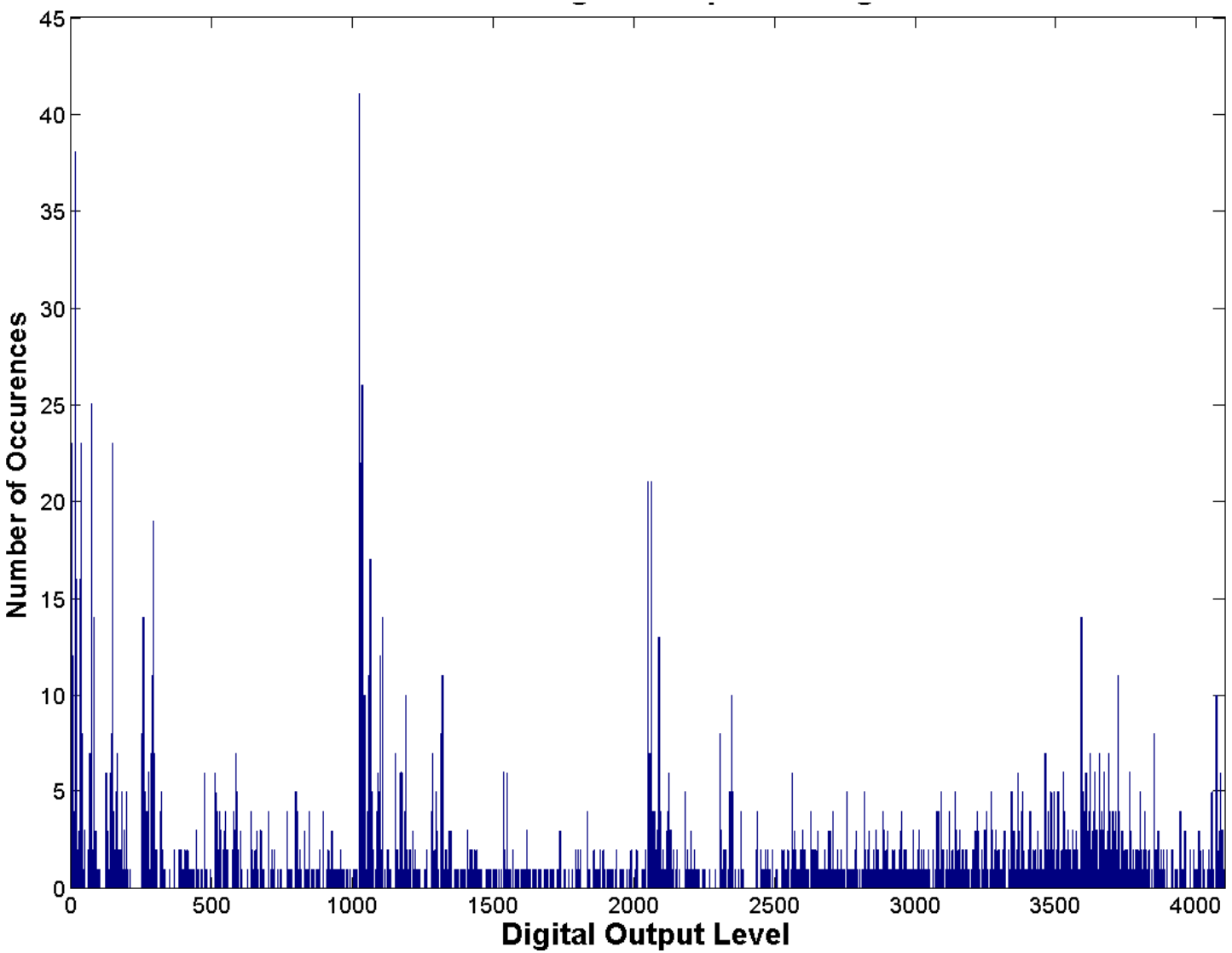

Figure 4.9 Measured raw ADC output data histogram (Filtered Supply)

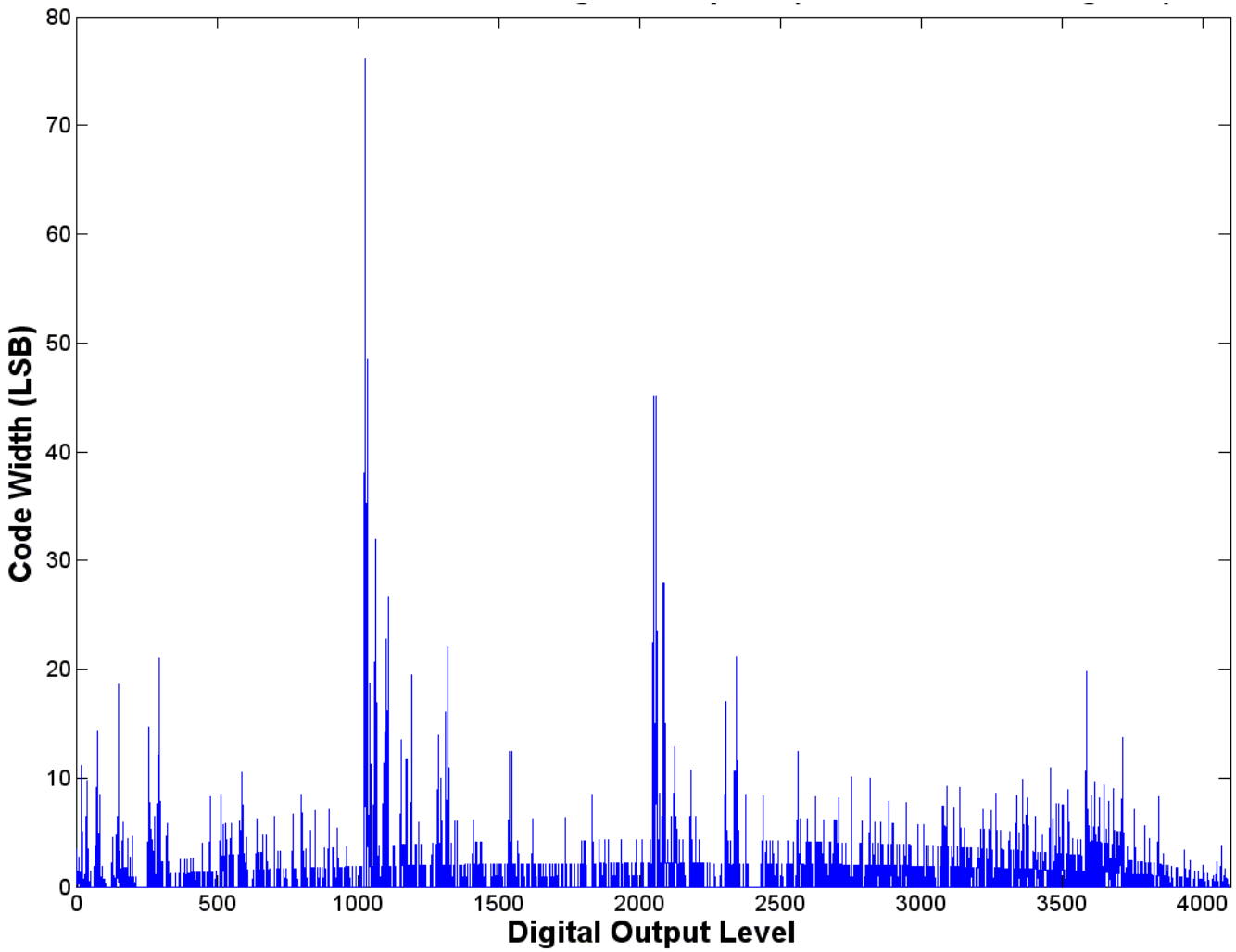

Figure 4.10 Normalized histogram showing code step widths (Filtered Supply)

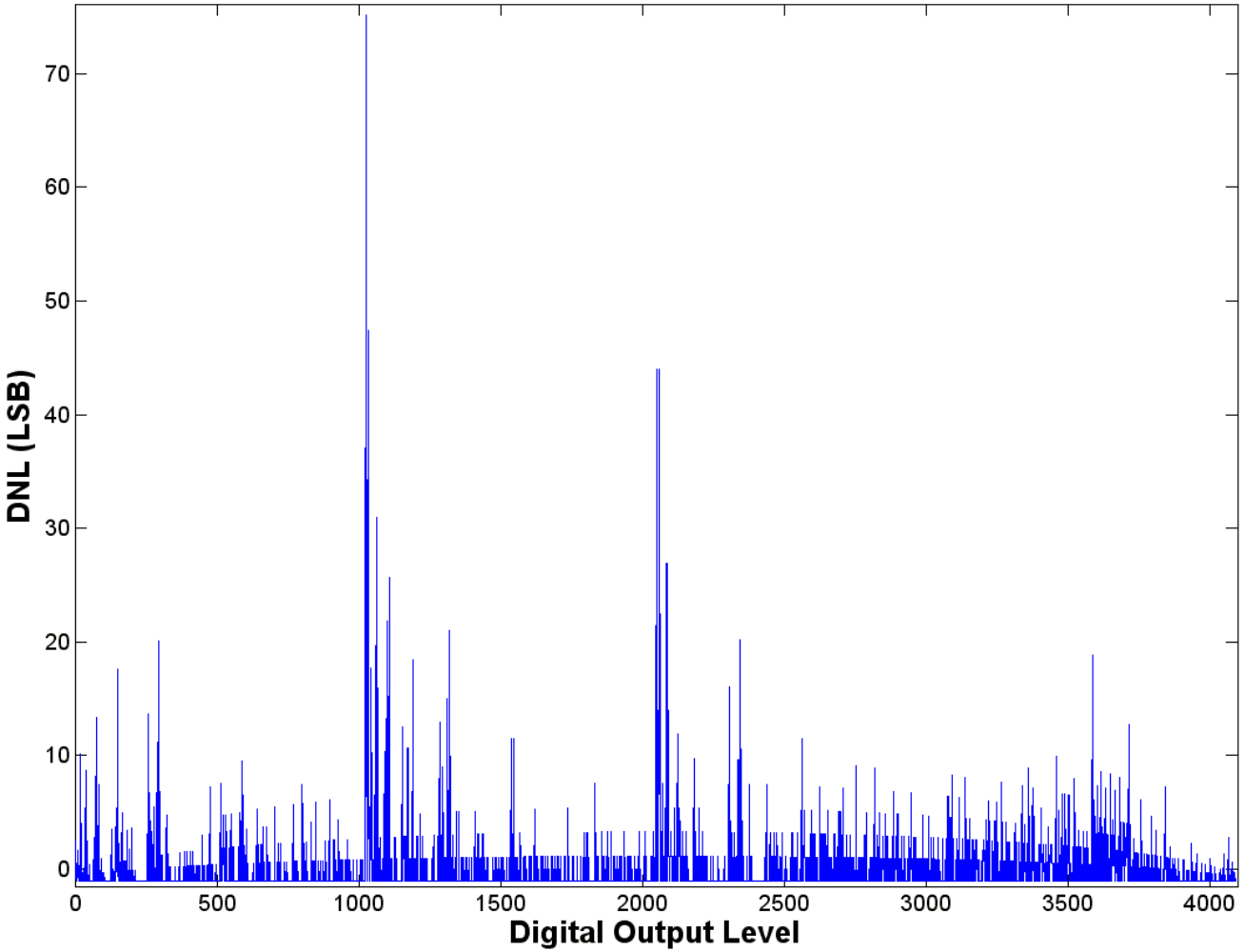

Figure 4.11 Measured DNL curve (Filtered Supply)

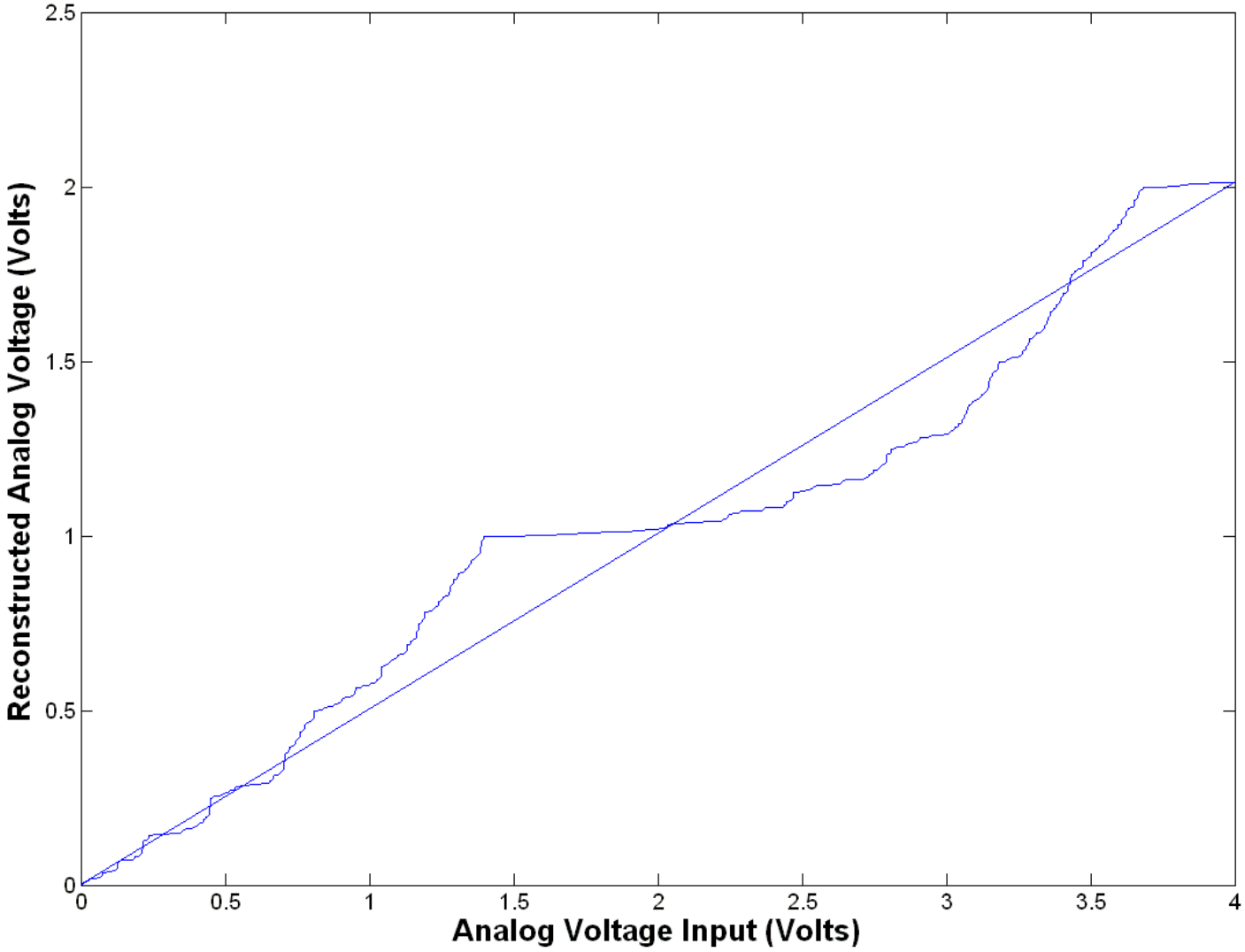

Figure 4.12 Measured voltage characteristic curve and best fit line (Filtered Supply)

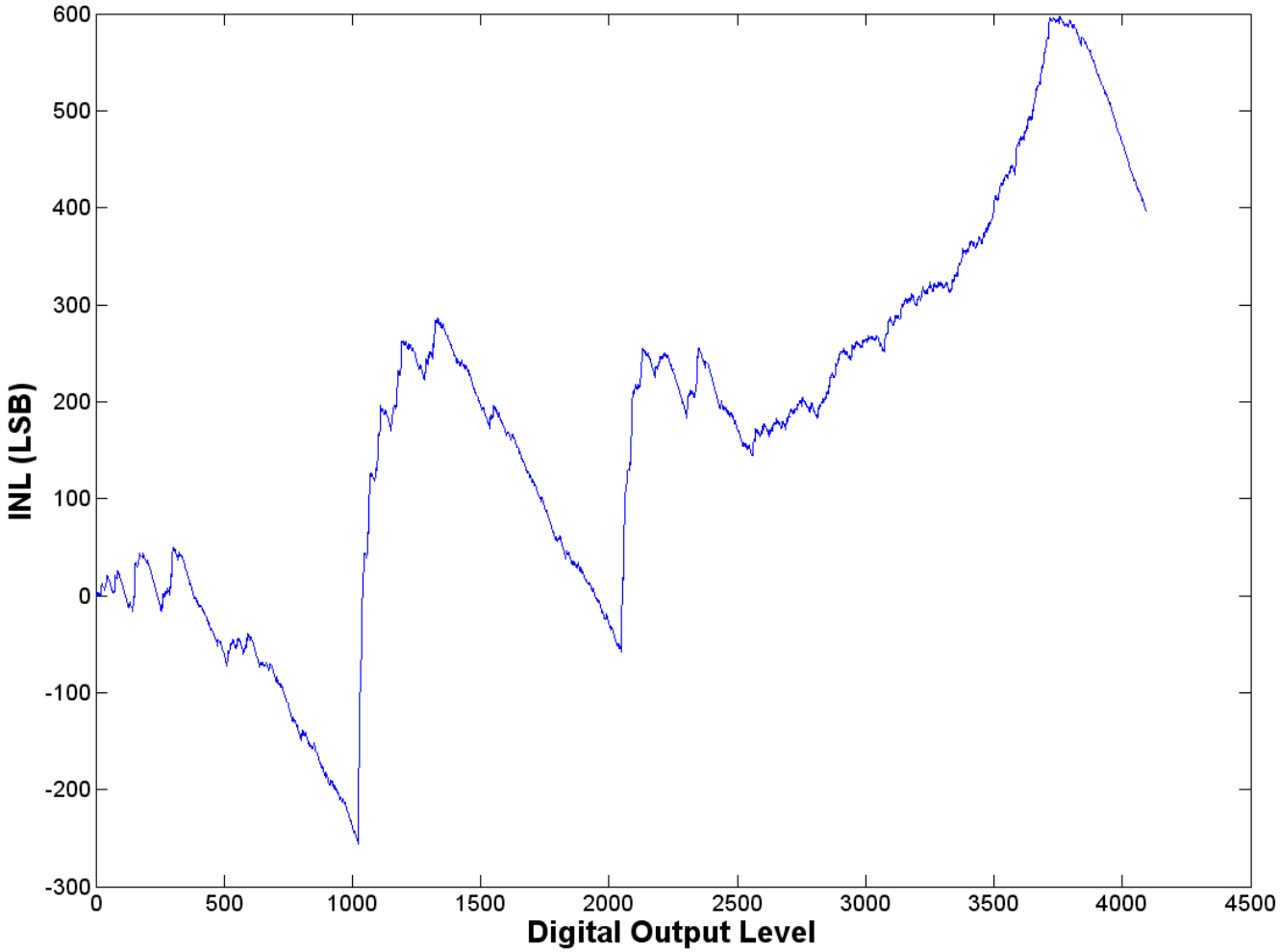

Figure 4.13 Measure INL curve (Filtered Supply)

Figure 4.14 Comparator reference voltage Vmid

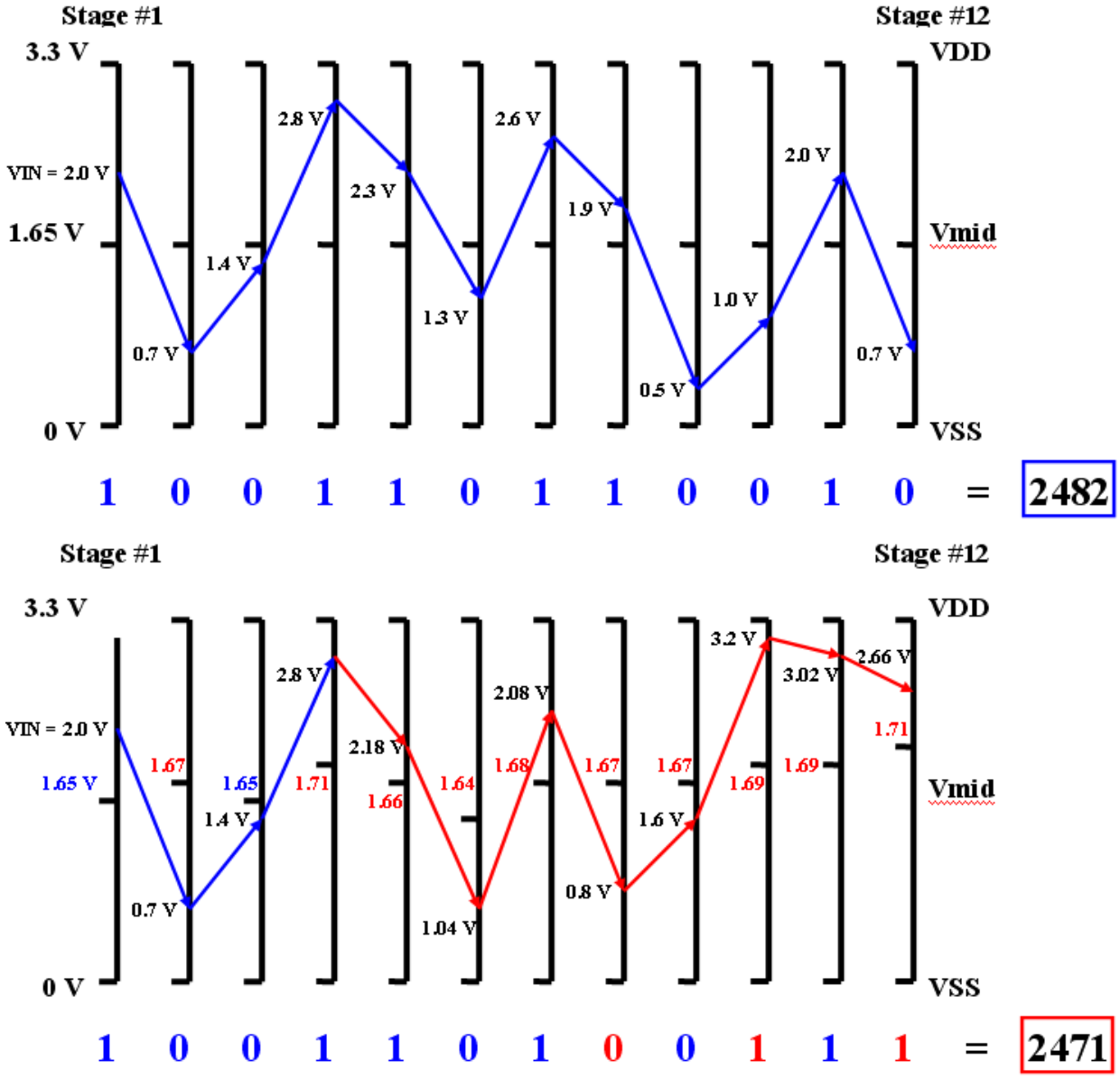

Figure 4.15 Conversion error due to time varying comparator reference voltage

Chapter 5 Conclusions and Recommendations

Throughout the process of attempting to characterize the ADC, multiple difficulties have been encountered and overcome. These difficulties included learning how to operate the test board, interface the NI connector with the test board through Labview, manipulate the raw data into meaningful characteristics, and attempt to gain a better understanding of the pipeline ADC architecture in general and specific to the ADC tested.

There is no question it is a far simpler task for the designer to test his/her own circuit, than it is for someone unfamiliar with the design to test it without a firm background on the specifics of its implementation. The Cadence schematic and layout for the chip aided in mitigating this difficulty, but no substitute exits for having the intimate knowledge of the circuit the designer acquires through iteration.

The end results of this characterization are less than satisfying. The hope for better results continued to be met with the grim reality that the results had reached an optimal point given the current chip and test board. Even though additional time was invested in an attempt to obtain more accurate data, the results remained unchanged or became worse than the results shown in Chapter 4.

The chip, test board, or possibly even both may be at fault for the results. Throughout the testing process, problems were encountered relating to both. For example, the chip brings a single ended clock onto the chip, which will inject a considerable amount of noise into the substrate of the chip. Additionally, the on-chip current bias circuit's output was incorrect. The output remained fairly consistent from chip-to-chip with a current of 130 μA instead of the design value of 250 μA.

Board related issues also existed. The test board originally had no connector for the inverted clock. In addition, the line driver's outputs do not completely settle out if the clock frequency is in the neighborhood of the nominal clock frequency of 10 MHz. It is recommended that if any future testing is performed, a new test board should be designed. The new test board should place the BNC connections for the clock and inverted clock signals symmetrically. Also, superior filtering techniques should be implemented for the biasing voltages and more care taken in the connection of analog and digital supply rails. Finally, it is recommended that the new test board include a superior current biasing scheme, which can be switched to the current mirror input pin.

List of References

[1] R. Jacob Baker, et al., *CMOS Circuit Design, Layout, and Simulation,* IEEE Press, 2008. ISBN 978-0-470-22941-5.

[2] Mark Burns and Gordon W. Roberts, *An Introduction to Mixed-Signal IC Test and Measurement*, Oxford University Press, 2001. ISBN 978-0-19-514016-3.

[3] Mark Ferriss and Joshua Kang, *A 10 bit 100MHz pipeline ADC*, University of Michigan, 2004.

[4] Personal correspondence with Mark Hale (ADC).

[5] Personal correspondence with Ross Chun (Test Board).

[6] Hae-Seung Lee, *A 12-b 600 ks/s Digitally Self-Calibrated Pipelined Algorithmic ADC*, IEEE Journal of Solid-State Circuits, Vol. 29, No. 4, April 1994.

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[9] Stephen H. Lewis and Paul R. Gray, *A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter*. IEEE Journal of Solid-State Circuits, Vol. sc-22, No. 6, December 1987.

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[13] Dong-Young Chang and Un-Ku Moon, *A 1.4V 10-bit 25-MS/s Pipelined ADC Using Opamp-Reset Switching Technique*. IEEE Journal of Solid-State Circuits, Vol. 38, No. 8, August 2003.

[14] Personal correspondence with Neena Nambiar (NI 6534 LabView Code).

[15] Craig L. King, *Differential ADC Biasing Techniques, Tips, and* Tricks. Microchip AN842 Application Note, 2002.

[16] NI 6534 User Manual for Traditional NI-DAQ. February 2005.

[17] Bruce Carter, *Fully Differential Op Amps Made Easy*. Texas Instruments Application Report SLOA099, May 2002.

Appendices

Appendix A – Test Board

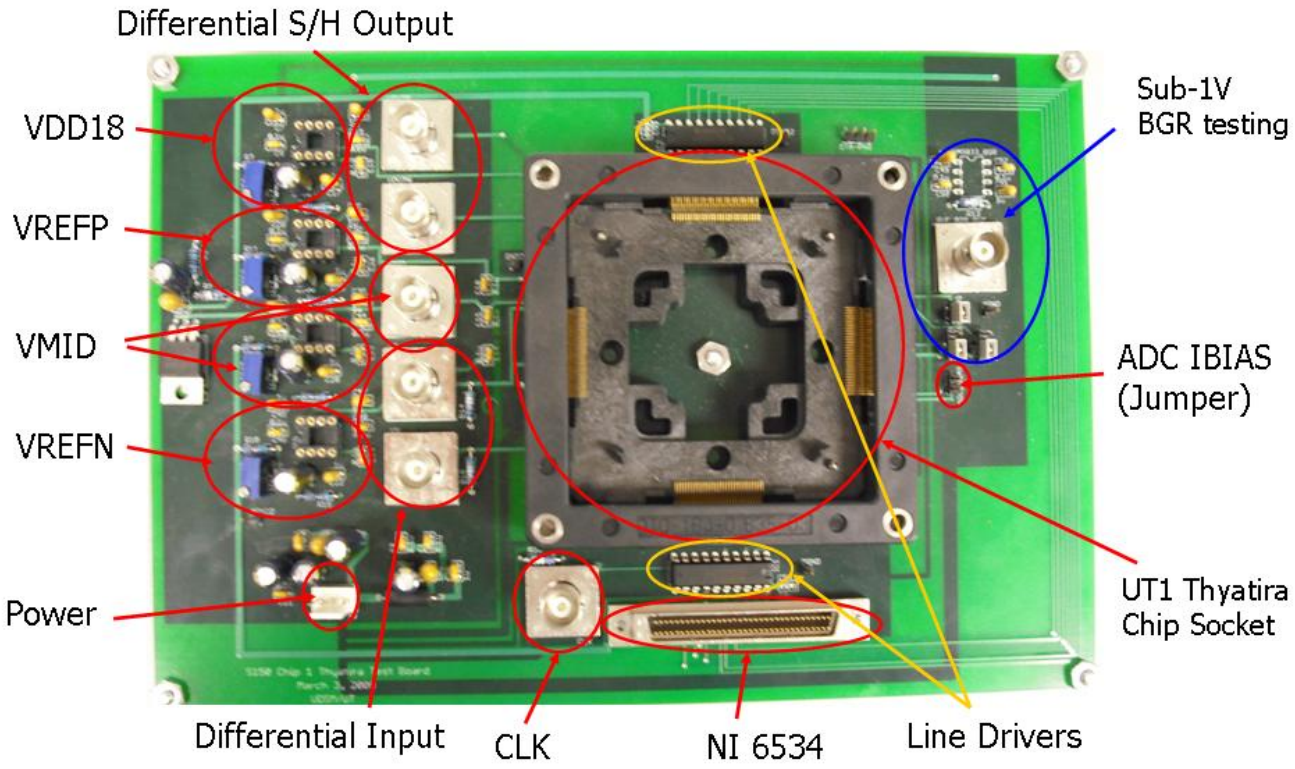

Figure A.1 Picture of entire test board designed by Ross Chun

Appendix B – Matlab Code

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%% Labview Data Analysis %%
%% Sine Histogram ONLY   %%
%% By Saeed R. Ghezawi   %%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%
% Initialization %
%%%%%%%%%%%%%%%%%%

%Clear Matlab memory
clear;

%Clear command window
clc;

%Clear all figures
close all;

%Number of bits
n = 12;

%ADC reference voltage
VREF = 4;

%LSB size (Volts)
VLSB = VREF./2^n;

%Clock frequency (hertz)
clk_hz = 500e3;

%Number of output levels
num_lvl = 2^n;

%Maximum output code
max_out = 2^n - 1;

%File with data
filename = 'ugly_sine_1MHZ_111FIN_2VPP.lvm';

%Tab delimited file
delim = '\t';

%Header ends on line 21 (Of LVM file)
header = 21;

%%%%%%%%%%%%%%
% Read Data %
%%%%%%%%%%%%%%
temp = importdata(filename,delim,header);

%Digital output data (Measured ADC data)
dout = temp.data(:,2);

%Clean up memory (No longer needed information)
clear temp filename delim header;

%%%%%%%%%%%%%%%%%%
% Plot Waveform %
%%%%%%%%%%%%%%%%%%

%Declare time vector
time = 0:(1/clk_hz):((1/clk_hz)*length(dout));
```

```
%Plot waveform
figure(1);
axes('Parent',1,'FontSize',14);
plot(time(1,1:length(dout)),dout);
title('12-bit ADC Digital Output Waveform','FontSize',22,'FontWeight','bold');
xlabel('Time (sec)','FontSize',20,'FontWeight','bold');
ylabel('Digital Output Level','FontSize',20,'FontWeight','bold');

%%%%%%%%%%%%%%%%%%
% Plot Histogram %
%%%%%%%%%%%%%%%%%%
figure(2);
axes('Parent',2,'FontSize',14);
bins = 0:max_out;
[count,code] = hist(dout,bins);
hist(dout,bins)
xlim ([0 max_out]);
title('12-bit ADC Digital Output Histogram','FontSize',22,'FontWeight','bold');
xlabel('Digital Output Level','FontSize',20,'FontWeight','bold');
ylabel('# of Occurences','FontSize',20,'FontWeight','bold');

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%   Characterization Computations   %
% For Differential Sinusoidal Input %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%Number of samples
NS = length(dout);

%Formula constants
C1 = cos(pi * count(num_lvl)/NS);
C2 = cos(pi * count(1)/NS);

%Sine offset and amplitude calculations (Seen by ADC)
offset = ((C2 - C1) / (C2 + C1)) * (2^(n-1)-1);
amplitude = (2^(n-1)-1 - offset) / C1;

%Expected distribution (Excluding Code 0 and Code 4095)
HSINE = (NS/pi) * (asin(((1:2^n-2)+ 1 - 2^(n-1) - offset) / amplitude ) ...
    - asin(((1:2^n-2) - 2^(n-1) - offset) / amplitude));

%Measured code widths (Note: code_width(1) is code width of '1' not '0')
code_width = count(2:length(count)-1) ./ HSINE;

%Plot Normalized Histogram (Measured code widths)
figure(3);
axes('Parent',3,'FontSize',14);
plot(code_width);
xlim ([0 max_out]);
title('Measured Code Width of Digital Outputs (Normalized
Histogram)','FontSize',22,'FontWeight','bold')
xlabel('Digital Output Level','FontSize',20,'FontWeight','bold')
ylabel('Code Width (LSB)','FontSize',20,'FontWeight','bold')

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Differential Nonlinearity (DNL) %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%Calculate DNL assuming ideal width is 1 LSB
DNL = code_width - 1;

%Plot DNL
figure(4);
axes('Parent',4,'FontSize',14);
plot(DNL);
xlim ([0 max_out]);
ylim([-1.5,max(DNL)+1]);
title('DNL for 12-Bit ADC','FontSize',22,'FontWeight','bold')
```

```
xlabel('Digital Output Level','FontSize',20,'FontWeight','bold')
ylabel('DNL (LSB)','FontSize',20,'FontWeight','bold')

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Construct Characteristic Curve %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%Lowest output triggered (Ideally 0)
start_bit = min(dout);

%Highest output triggered (Ideally 4095)
stop_bit = max(dout);

%Current digital voltage level (Ideal DAC)
vout = 0;

%Assume 0.5 LSB offset
corner = 0.5 * VLSB;

%Characteristic curve
curve = 0;

%Analog input voltage
ain = 0;

%Analog voltage step
step = 100e-6;

%Define Analog input
ain = 0:step:VREF;

%Next transition
next = 1;

%Define measured transitional corners (Assuming 0.5 LSB offset)
for j = 1:length(code_width)
   corner = [corner corner(j)+code_width(j)*VLSB];
end

%Define characteristic curve
for i = 1:length(ain)
    if(ain(i) < corner(next))
        curve = [curve vout];
    elseif (ain(i) >= corner(next))
        if (next == 1)
            first = i;
        end
        last = i;
        if (next < 4095)
            next = next + 1;
        end
        vout = vout + VLSB;
    end
    curve = [curve vout];
end

%Plot characteristic curve
figure(5);
axes('Parent',5,'FontSize',14);
plot(ain,curve(1:length(ain)));
title('12-Bit ADC Characteristic Curve','FontSize',22,'FontWeight','bold')
xlabel('Analog Voltage Input (Volts)','FontSize',20,'FontWeight','bold')
ylabel('Reconstructed Analog Voltage (Volts)','FontSize',20,'FontWeight','bold')

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% DC Offset and Gain Errors %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%Determine linear best fit (Between first and last transitional corners)
```

```
coff = polyfit([ain(first),ain(last)],[curve(first),curve(last)],1);
hold on;
best_fit = coff(1) * ain  + coff(2) + VLSB;
plot(ain,best_fit);
hold off;

%Determine gain error
gain_error = coff(1) - 1

%Determine offset error
offset_error = -coff(2)/VLSB

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Integral Nonlinearity (INL) %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%Define ideal corners
ideal_corner = 0.5:1:(2^n-2);

INL = (corner(1:length(ideal_corner))/VLSB - ideal_corner);
figure(6)
axes('Parent',6,'FontSize',14);
plot(INL);
title('INL for 12-Bit ADC','FontSize',22,'FontWeight','bold')
xlabel('Digital Output Level','FontSize',20,'FontWeight','bold')
ylabel('INL (LSB)','FontSize',20,'FontWeight','bold')
```

Appendix C – NI 6534 Pinout

Figure C.1 NI 6534 connector pinout

[16]

Table C.1 NI 6534 Pinout usage and explanation

Pin Numbers	Signal Name	Signal Type	Description (Signal Connection)
2, 9	PFI <2..3> (REQ <1..2>)	Control	Request lines – Control line used to indicated when data is available (Clock)
3, 8	PFI <6..7> (ACK <1..2>)	Control	Acknowledge lines – Not used
4, 7	PFI <0..1> (STOPTRIG <1..2>)	Control	Stop triggers – Not used
5, 6	PFI <4..5> (PCLK <1..2>)	Control	Peripheral clock lines – Not used
10, 44, 45, 12, 13, 47, 48, 15	P0 <0..7> (DIOA <0..7>)	Data	Port 0 (A) – Bidirectional data lines (D12 – D5)
16, 17, 21, 22, 51-54	P1 <0..7> (DIOB <0..7>)	Data	Port 1 (B) – Bidirectional data lines (D4 – D1)
23, 57, 58, 25, 26, 60, 61, 28	P2 <0..7> (DIOC <0..7>)	Data	Port 2 (C) - Not used
29, 63, 64, 31, 32, 66, 67, 34	P3 <0..7> (DIOD <0..7>)	Data	Port 3 (D) - Not used
40	CRTL PULL (CPULL)	Bias Selection	Control pull up/down selection – Connected to ground so that control lines are pulled down when they are not being driven
38	DATA PULL (DPULL)	Bias Selection	Data pull up/down selection – Connected to ground so that data lines are pulled down when they are not being driven
1	+5 V (+5 V)	Power	5 volt supply - Not used
11, 14, 18, 20, 24, 27 30, 36, 37, 39, 41, 42, 46, 49, 50, 55, 59, 62, 65, 68	D GND (GND)	Power	Ground reference
19, 35, 43, 56	R GND (R GND)	Power	Reserved ground

[16]

Appendix D – Thyatira Pinout

Table D.1 Pinout for UT1 Thyatira

Package (Pin #)	Buffer Place (Layout)	Signal Name	Signal Level	Signal Direction
1	-	VSS	0 V	IN/OUT
2	L015	VSS	0 V	IN/OUT
3	L014	Vn	0.65 – 2.65 V	IN
4	L013	Vp	0.65 – 2.65 V	IN
5	L010	VDD18	1.8 V	IN/OUT
6	L009	Vrefp	2.65 V	IN
7	L008	Vrefn	0.65 V	IN
8	L007	Vmid	1.65 V	IN
9	L006	NO CONNECT	-	-
10	L005	NO CONNECT	-	-
11	L004	NO CONNECT	-	-
12	-	UNUSED PIN	-	-
13	L003	NO CONNECT	-	-
14	-	UNUSED PIN	-	-
15	-	UNUSED PIN	-	-
16	-	UNUSED PIN	-	-
17	-	VDD33	3.3 V	IN/OUT
18	-	VSS	0 V	IN/OUT
19	-	UNUSED PIN	-	-
20	-	UNUSED PIN	-	-
21	B003	DVSS	0 V	IN/OUT
22	B005	NO CONNECT	-	-
23	B004	DVSS	0 V	IN/OUT
24	B006	NO CONNECT	-	-
25	B007	NO CONNECT	-	-
26	B008	NO CONNECT	-	-
27	B009	NO CONNECT	-	-
28	B010	NO CONNECT	-	-
29	B011	VDD18	1.8 V	IN/OUT
30	B014	D1	0 – 3.3 V	OUT
31	B015	NO CONNECT	-	-
32	B016	NO CONNECT	-	-
33	B017	NO CONNECT	-	-
34	-	VDD33	3.3 V	IN/OUT
35	B018	NO CONNECT	-	-
36	B019	D2	0 – 3.3 V	OUT

Table D.1 Continued

Package (Pin #)	Buffer Place (Layout)	Signal Name	Signal Level	Signal Direction
37	B020	NO CONNECT	-	-
38	B021	NO CONNECT	-	-
39	B024	VDD18	1.8 V	IN/OUT
40	B025	D3	0 – 3.3 V	OUT
41	B026	NO CONNECT	-	-
42	B027	NO CONNECT	-	-
43	B028	D4	0 – 3.3 V	OUT
44	B030	DVDD33	3.3 V	IN/OUT
45	B029	DVSS	0 V	IN/OUT
46	B032	NO CONNECT	-	-
47	B031	D5	0 – 3.3 V	OUT
48	-	UNUSED PIN	-	-
49	-	UNUSED PIN	-	-
50	-	VSS	0 V	IN/OUT
51	-	VDD33	3.3 V	IN/OUT
52	-	UNUSED PIN	-	-
53	-	UNUSED PIN	-	-
54	-	UNUSED PIN	-	-
55	-	UNUSED PIN	-	-
56	R004	NO CONNECT	-	-
57	R003	NO CONNECT	-	-
58	R005	NO CONNECT	-	-
59	R006	NO CONNECT	-	-
60	R007	NO CONNECT	-	-
61	R008	NO CONNECT	-	-
62	R009	NO CONNECT	-	-
63	R010	VDD18	1.8 V	IN/OUT
64	R013	Iinput	1.8 V	IN
65	R014	IN1_R014	3.3 V	IN
66	R015	VSS	0 V	IN/OUT
67	-	VSS	0 V	IN/OUT
68	R016	VSS	0 V	IN/OUT
69	R017	VDD33	3.3 V	IN/OUT
70	R018	VDD33	3.3 V	IN/OUT
71	R021	VDD18	1.8 V	IN/OUT
72	R022	Ioutput	1.8 V	OUT
73	R023	NO CONNECT	-	-
74	R024	NO CONNECT	-	-
75	R025	NO CONNECT	-	-

Table D.1 Continued

Package (Pin #)	Buffer Place (Layout)	Signal Name	Signal Level	Signal Direction
76	R026	NO CONNECT	-	-
77	R027	NO CONNECT	-	-
78	R029	NO CONNECT	-	-
79	R028	NO CONNECT	-	-
80	-	UNUSED PIN	-	-
81	-	UNUSED PIN	-	-
82	-	UNUSED PIN	-	-
83	-	VDD33	3.3 V	IN/OUT
84	-	VSS	0 V	IN/OUT
85	-	UNUSED PIN	-	-
86	-	UNUSED PIN	-	-
87	T031	NO CONNECT	-	-
88	T032	NO CONNECT	-	-
89	T029	DVSS	0 V	IN/OUT
90	T030	DVDD33	3.3 V	IN/OUT
91	T028	NO CONNECT	-	-
92	T027	NO CONNECT	-	-
93	T026	NO CONNECT	-	-
94	T025	D6	0 – 3.3 V	OUT
95	T024	VDD18	1.8 V	IN/OUT
96	T021	NO CONNECT	-	-
97	T020	D7	0 – 3.3 V	OUT
98	T019	NO CONNECT	-	-
99	T018	NO CONNECT	-	-
100	-	VDD33	3.3 V	IN/OUT
101	T017	D8	0 – 3.3 V	OUT
102	T016	NO CONNECT	-	-
103	T015	NO CONNECT	-	-
104	T014	D9	0 – 3.3 V	OUT
105	T011	VDD18	1.8 V	IN/OUT
106	T010	D10	0 – 3.3 V	OUT
107	T009	D12	0 – 3.3 V	OUT
108	T008	D11	0 – 3.3 V	OUT
109	T007	NO CONNECT	-	-
110	T006	NO CONNECT	-	-
111	T004	DVDD33	3.3 V	IN/OUT
112	T005	NO CONNECT	-	-
113	T003	DVSS	0 V	IN/OUT
114	-	UNUSED PIN	-	-

Table D.1 Continued

Package (Pin #)	Buffer Place (Layout)	Signal Name	Signal Level	Signal Direction
115	-	UNUSED PIN	-	-
116	-	VSS	0 V	IN/OUT
117	-	VDD33	3.3 V	IN/OUT
118	-	UNUSED PIN	-	-
119	-	UNUSED PIN	-	-
120	L029	NO CONNECT	-	-
121	-	UNUSED PIN	-	-
122	L028	NO CONNECT	-	-
123	L027	NO CONNECT	-	-
124	L026	NO CONNECT	-	-
125	L025	NO CONNECT	-	-
126	L024	NO CONNECT	-	-
127	L023	CLKB	0 – 3.3 V	IN
128	L022	CLK	0 – 3.3 V	IN
129	L021	VDD18	1.8 V	IN/OUT
130	L018	VDD33	3.3 V	IN/OUT
131	L017	VDD33	3.3 V	IN/OUT
132	L016	VSS	0 V	IN/OUT

Pinout information gathered from excel spreadsheet prepared by Mark Hale [4]

Vita

Saeed Ramzi Ghezawi was born in Amman, Jordan on April 27, 1986. He grew up in Knoxville, Tennessee where he graduated from Farragut High School in 2004. In 2008, he graduated Summa Cum Laude from the University of Tennessee, Knoxville with a Bachelor of Science degree in Electrical Engineering. Afterwards, he immediately entered graduate school to work towards a Master of Science in Electrical Engineering at the University of Tennessee under the guidance of Dr. Benjamin J. Blalock.