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Thesis for the Degree of Doctor

Electrical Characterization and Modeling of Low Dimensional Nanostructure FET

by

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Electrical Characterization and Modeling of Low Dimensional Nanostructure FET

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The journey is the reward.

- Steve Jobs

English Abstract

At the beginning of this thesis, basic and advanced device fabrication process which I have experienced during study such as top-down and bottom-up approach for the nanoscale device fabrication technique have been described. Especially, lithography technology has been focused because it is base of the modern device fabrication. For the advanced device structure, etching technique has been investigated in detail.

The characterization of FET has been introduced. For the practical consideration in the advanced FET, several parameter extraction techniques have been introduced such as Y-function, split C-V etc.

FinFET is one of promising alternatives against conventional planar devices. Problem of FinFET is surface roughness. During the fabrication, the etching process induces surface roughness on the sidewall surfaces. Surface roughness of channel decreases the effective mobility by surface roughness scattering. With the low temperature measurement and mobility analysis, drain current through sidewall and top surface was separated. From the separated currents, effective mobilities were extracted in each temperature conditions. As temperature lowering, mobility behaviors from the transport on each surface have different temperature dependence. Especially, in n-type FinFET, the sidewall mobility has stronger degradation in high gate electric field compare to top surface. Quantification of surface roughness was also compared between sidewall and top surface. Low temperature measurement is nondestructive characterization method. Therefore this study can be a proper surface roughness measurement technique for the performance optimization of FinFET.

As another quasi-1 D nanowire structure device, 3D stacked SiGe nanowire has been introduced. Important of strain engineering has been known for the effective mobility booster. The limitation of dopant diffusion by strain has been shown. Without strain, SiGe nanowire FET showed huge short channel effect. Subthreshold current was bigger than strained SiGe channel. Temperature dependent mobility behavior in short channel unstrained device was completely different from the other cases. Impurity scattering was dominant in short channel unstrained SiGe nanowire FET. Thus, it could be concluded that the strain engineering is not necessary only for the mobility booster but also short channel effect immunity.

Junctionless FET is very recently developed device compare to the others. Like as JFET, junctionless FET has volume conduction. Thus, it is less affected by interface states.

Junctionless FET also has good short channel effect immunity because off-state of junctionless FET is dominated pinch-off of channel depletion. For this, junctionless FET should have thin body thickness. Therefore, multi gate nanowire structure is proper to make junctionless FET.

Because of the surface area to volume ratio, quasi-1D nanowire structure is good for the sensor application. Nanowire structure has been investigated as a sensor. Using numerical simulation, generation-recombination noise property was considered in nanowire sensor. Even though the surface area to volume ration is enhanced in the nanowire channel, device has sensing limitation by noise. The generation-recombination noise depended on the channel geometry. As a design tool of nanowire sensor, noise simulation should be carried out to escape from the noise limitation in advance.

The basic principles of device simulation have been discussed. Finite difference method and Monte Carlo simulation technique have been introduced for the comprehension of device simulation. Practical device simulation data have been shown for examples such as FinFET, strongly disordered 1D channel, OLED and E-paper.

Contents

1. Overview of Semiconductor Device Trends 1
1.1 Economical Consideration: Market Trend Overview 3
1.2 Device Scaling 5
1.3 Short Channel Effects 7
1.3.1 Threshold Voltage Shift, Punchthrough and Drain-induced Barrier Lowering 8
1.3.2 Velocity Saturation 10
1.3.3 Hot Carrier Effects 12
1.4 Challenges to Overcome Short Channel Effects 12
1.4.1 High-k and Metal Gate 12
1.4.2 Silicon on Insulator 14
1.4.3 Multi Gate and Pseudo 1D Structure 16
1.5 Conclusion 18
References 19
2. Nano-device Fabrication Technology 21
2.1 Introduction 23
2.2 Top-down and Bottom-up 24
2.2.1 Bottom-up approach 24
2.2.2 Top-down approach 26
2.2.3 Conclusion: Convergence of Top-down and Bottom-up 37
2.3 Conclusion 38
References 39
3. Characterization and Parameter Extraction of FET 43
3.1 Introduction 45
3.2 Basic MOSFET Operation 46
3.2.1 Linear Regime (at Small V_D) 46
3.2.2 Saturation Regime (at high V_D) 46
3.2.3 Transfer characteristics: Threshold Voltage and Subthreshold Swing 47
3.2.4 Mobility 50
3.2.5 Low Frequency Noise 55
3.3 Characterization and Parameter Extraction Technique 58

3.3.1 Series Resistance 58
3.3.2 Effective Channel Geometry 59
3.3.3 Y-function Method 60
3.3.4 Split C-V 62
3.4 Conclusion 63
References 64
4. Transport of Quasi-1D nanostructure FET 67
4.1 FinFET – Surface Roughness Scattering 70
4.1.1 FinFET overview 70
4.1.2 Experimental Conditions: Device Fabrication and Measurement 75
4.1.3 Threshold Voltage 76
4.1.4 Surface Current Separation Technique 77
4.1.5 Temperature Dependence of FinFET Effective Mobility 81
4.1.6 Quantification of the Surface Roughness Scattering Effect 85
4.1.7 Conclusion 87
4.2 SiGe Nanowire FET – Phonon Scattering and Impurity Scattering 89
4.2.1 Device overview: Strain Engineering 89
4.2.2 Experimental Conditions: Device Fabrication and Measurement 91
4.2.3 Short Channel Effects in SiGe Nanowire FET 92
4.2.4 Analysis of Transport Mechanism 95
4.2.5 Conclusion 102
4.3 Junctionless Transistor – Volume Conduction and Reduced Short Channel Effects 104
4.3.1 Device Overview 104
4.3.2 Transport of Junctionless Transistor 105
4.3.3 Conclusion 109
4.4 Si Nanowire Sensor – Low Frequency Noise and Sensing Limitation 111
4.4.1 Overview: Nanowire for Sensor Application 111
4.4.2 Simulation Environment and Conditions. 112
4.4.3 Sensitivity Estimation: Numerical Simulation and Analytical Model 113
4.4.4 Low Frequency Noise in Nanowire Sensor 115
4.4.5 Conclusion 118
References 119
5. Device Simulation 125
5.1 Overview: Types of Simulation 127

5.2 Simulation of Quasi 1D Nanowire Devices 129
5.2.1 Finite Difference Method 129
5.2.2 Simulations in Specific 1D Systems: Variable Range Hopping in Disordered System.. 131
5.2.3 Practical Device Simulation 133
5.3 Other Device Simulations: OLED and E-paper 134
5.3.1 Monte Carlo Method 134
5.3.2 Device Simulations: OLED and E-paper 136
5.4 Conclusion 138
References 140
Conclusion 141
Appendix 145
Appendix 1: Physical Constants 146
Appendix 2: General Properties of Si, Ge and SiGe 147
Appendix 3: E-beam Lithography Pattern Design Program using Mathematica 150
Appendix 4: Fundamental Vacuum System 155
Appendix 5: Publication List 158
국문 초록 159

1. Overview of Semiconductor Device Trends

1. Overview of Semiconductor Device Trends

1.1 Economical Consideration: Market Trend Overview

1.2 Device Scaling

1.3 Short Channel Effects

- 1.3.1 Threshold Voltage Shift, Punchthrough and Drain-induced Barrier Lowering
- 1.3.2 Velocity Saturation
- 1.3.3 Hot Carrier Effects

1.4 Challenges to Overcome Short Channel Effects

- 1.4.1 High-k and Metal Gate
- 1.4.2 Silicon on Insulator
- 1.4.3 Multi Gate and Pseudo 1D Structure

1.5 Conclusion

Chapter 1
Overview of Semiconductor Device Trends

1.1 Economical Consideration: Market Trend Overview

Currently, the appearance of smart devices such as smartphone, tablet PC changes semiconductor market trends.

The origin of smart devices was IBM Simon which was released in 1993 as a world first smart device as a convergence between mobile phone and PC [1]. It included a schedule manager, address book, world clock, fax, games and calculator etc. With evolutions, smart devices have been continuing like personal digital assistant, iPhone and Galaxy Tab etc. Especially after iPhone and Android smartphone has been released in the market, numerous smart applications which use simple user interface, global positioning system (GPS), motion sensors and Wi-Fi etc., play a role as a bridge between human and smart devices.

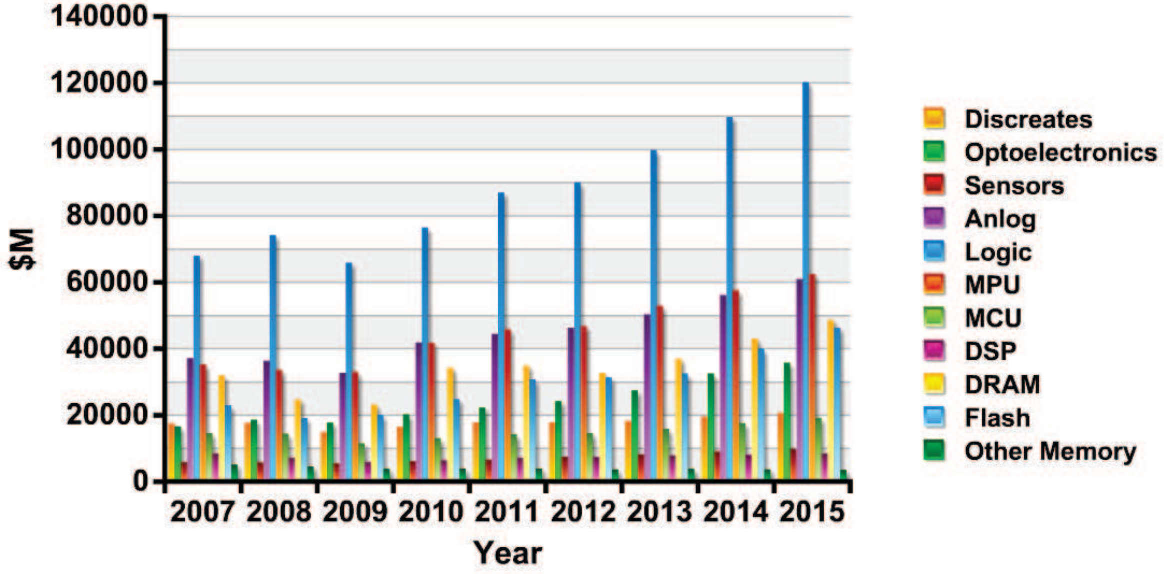


Figure 1.1 : Worldwide semiconductor revenue forecast by product type [2].

The harmonious combination between application and hardware has created the exponential market explosion of smart devices. The markets of smartphone and tablet PC have been forecasted as 49% and 162% growth in 2011 comparing with 2010 [3, 4].

According to the increased demand of smart devices, semiconductor memory market trends are changing for instance from PC DRAM to mobile DRAM and from HDD to NAND flash memory. For example, the market share of mobile DRAM in DRAM market will be growing up to 7.1% in 2011 comparing with 5.5% in 2010 and the total growth rate will be over 100% [5]. To be applied in mobile devices, mobile DRAM should be cost effective with high device density and developed as high performance and low power consumption.

Non-memory (representatively system IC) device market vends are also changing due to the enlargement of smart device market.

Centering around application processor (AP) for smart device, system IC market is growing up. Marching in step with this trend, strategic industrial feature ‘fab-less company’ has appeared. (Table 1.1) The fabless company means a semiconductor vendor which design, test and selling the chips without semiconductor manufacturing facilities. It relies on the other foundries for the fabrication of chips. The memory devices need the integrated device manufacturer, whereas non-memory device need a capability to correspond with requests of customer through the small quantity batch production. Thus the fabless companies which focus on the chip design are promising business core for the non-memory device.

2010 Rank	Company	Headquarters	2010 ($M)
1	Qualcomm	U.S.	7204
2	Broadcom	U.S.	6589
3	AMD	U.S.	6494
4	Marvell	U.S.	3592
5	MediaTek	Taiwan	3590
6	Nvidia	U.S.	3575
7	Xilinx	U.S.	2311
8	Altera	U.S.	1954
9	LSI Corp.	U.S.	1616
10	Avago	U.S.	1187

Table 1.1 : 2010 top 20 fabless IC suppliers [6].

Although the fabless company is one of the recent trend in non-memory devices, the research and development of device scaling down and advanced transistor technology such as finFETs, gate-all around (GAA) nanowire is still very important to improve the fabrication yield, low power consumption and the device performance, etc.

1.2 Device Scaling

As device dimensions reduced, it becomes difficult to carry out device fabrications. For instance, the integrated circuit becomes denser and more complicated as devices scale down. Thus, problems occur in lithography, interconnects and processing.

Device Scaling down to the small dimension is required to increase device performance such as enhanced switching speed and decreased power consumption. As an example, circuit delay time τ can be reduced as a function of gate length L because τ is given as:

	MOSFET Device and Circuit Parameters	**Multiplicative Factor**
Scaling Assumption	Device Dimensions (t_{ox}, L, W)	$1/\alpha$
	Doping Concentration (N_a, N_d)	α
	Voltage (V_D)	$1/\alpha$
Derived Scaling Behavior of Device Parameters	Electric Field (E)	1
	Depletion-layer Width (w_d)	$1/\alpha$
	Capacitance ($C= \varepsilon A/t_{ox}$)	$1/\alpha$
	Inversion-layer Charge density (Q_i)	1
	Carrier Velocity	1
	Drain Current in Drift Region (I_D)	$1/\alpha$
	Circuit delay time (τ)	$1/\alpha$
	Power dissipation ($P=I_DV_D$)	$1/\alpha^2$
	Circuit density	α^2
	Power Density (P/A)	1

Table 1.2 : Scaling parameters from constant-field scaling [7].

$$\tau = \frac{C_G V_D}{I_D} \ , \tag{1.1}$$

where I_D is the drain current, C_G the gate capacitance and V_D the drain voltage. With same V_D, the decrease of C_G or the increase of I_D reduces circuit delay time. The drain current I_D is inversely proportional to the gate length L, thus the reduction of L decreases τ. Like as τ, circuit density is proportional to the L^2 (Table 1.2). Moreover, power dissipation per circuit decreases by a factor of L^2 which is related to the reduction of the device heating problem.

The potential contours are parallel to the gate insulator and channel interface in long channel device. Thus, if the channel is long enough, the carriers are distributed along the channel surface. However, as gate length decreases, the potential distribution is changed. Aligned potential distributions are dispersed to the direction of body and induce uncontrolled device operation.

The scaling law of MOSFET transistor has followed constant-field scaling. In the constant-field scaling, the electric field is constantly maintained as device is scaled down. To keep the constant electric field, the lateral and perpendicular dimensions (for the constant electric field maintenance of both directions), operating voltage bias and doping concentration have to be changed with scaling factor α. The unchanged electric field pattern is necessary to maintain gate control and short channel behavior. As shown in Table 1.2, the thinner gate oxide thickness (decreased by α) is also needed to make gate oxide field constant. Channel doping level has to be increased by α to reduce the depletion width w_d to prohibit punch-through breakdown.

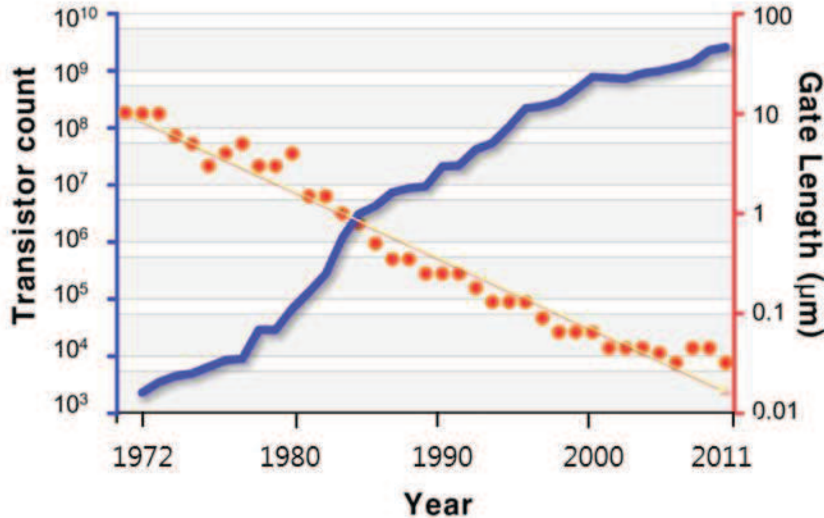


Figure 1.2 : Number of transistor and gate length versus per year (Microprocessor).

Intel co-founder Gordon Moore states that the number of transistor on a chip will be double about every two years, which is well known as Moore's law. For over about 40 years, Moore's law has driven the industry (Fig. 1.2). It seems to work so far. However device dimension has almost reached the end of the scaling limit. Currently 32 nm process node has been used in mass production. According to the Moore's law, several nm of gate length which is physical limitation of MOSFET will be used in several years. Thus, the new concept of device scaling is necessary to continue the device yield and performance enhancement beyond Moore's law.

Lots of alternative device concept has been researched such as multi gate structure, strained channel and junctionless transistor [8-10]. In 2011, Intel has demonstrated that tri-gate transistor will be adopted in 22 nm microprocessor named Ivy Bridge as world first high volume chip using 3D transistor [11]. It will be the first practical case that the conventional device concept molts.

1.3 Short Channel Effects

Device scaling causes unintended effects of device performance. These effects can be categorized according to the different sources [12];

- Electric field profile changes as two dimensional
  1. Drain-induced barrier lowering
  2. Mobility reduction by gate-induced surface field
- Electric field strength becomes very high in the channel
  1. Velocity saturation
  2. Impact ionization near drain
  3. Gate oxide charging
  4. Parasitic bipolar effect
- Physical separation between the source and the drain decreases.
  1. Punchthrough
  2. Channel length modulation

Some of them have similar result even though they have different physics. Moreover, sometimes, it is too ambiguous to separate each phenomenon. Thus, here simply classified short channel effects will be investigated for the clear comprehension.

1.3.1 Threshold Voltage Shift, Punchthrough and Drain-induced Barrier Lowering

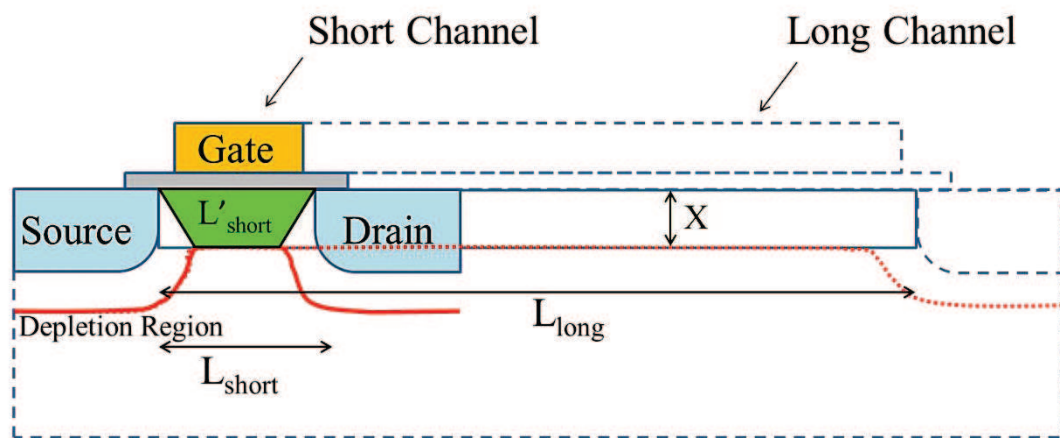


Figure 1.3 : Yau charge sharing model for the short channel device.

For a long channel device, V_G completely control depleting the semiconductor channel. However in short channel devices, part of channel depletion is under the control of source and drain bias. As the channel length shortens, the close proximity of the source and drain region occurs the fraction of the depletion charge in the channel. In other words, both the gate and source–drain voltages share control of the charge density below the gate. This effect is described by the charge-sharing model (Fig. 1.3) [13]. As a result, the channel can be depleted with lower gate voltage in short channel device. Thus, V_{th} becomes lower.

With the substrate doping concentration N_b, the bulk (depletion) charge per unit area Q_b in the depletion region under the gate could be approximated as rectangular thus $|Q_b|=qN_bW_d$ with depletion width W_d by V_G [13]. In this approximation, the charges near the source and drain, which terminate the built-in field from the junction edges, are neglected. The depletion region from the source and drain are overlapped with the channel charge. In long channel devices, this part is negligible comparing with the area of effective device channel. However, in short channel device, this overlapped part cannot be neglected anymore and the previous approximation does not work. With the consideration of overlapped parts, the shape of the depletion charge cross-section can be described as trapezoid and Q_b can be calculated as [14, 15]:

$$Q_b = q N_b W_d \left(\frac{L'_{short} + L_{short}}{2 L_{short}} \right). \tag{1.2}$$

The variation of V_{th} due to the short channel effect is:

$$\Delta V_{th} = \frac{Q_{b,\, longchannel} - Q_{b,\, shortchannel}}{C_{ox}} = \frac{Q_{b,\, longchannel}}{C_{ox}} \frac{W_j}{L} \left(\sqrt{1 + \frac{2W_d}{W_j}} - 1 \right), \tag{1.3}$$

where W_j is the junction depth in channel from the source and drain. From this equation, the decrease of channel length increases threshold shift. As we described previously, depletion charge can be formed easily with small L. Thus, V_{th} becomes lower in short channel. According to this relationship, parameters to avoid V_{th} variation due to the short channel effect can be known as following. 1. The reduction of gate oxide thickness; thin oxide thickness increase C_{ox} thus ΔV_{th} can be decreased. 2. The increase of substrate doping N_b; it decreases W_d and ΔV_{th}. 3. The steep junction depth; the reduction of W_j decreases ΔV_{th}.

When the depletion region around the drain extends to the source in short channel device, two depletion layers can merge into a single depletion region as shown in Fig. 1.4 [15, 16]. The depletion region of the drain is mainly affected by the drain bias V_D [17]. Punchthrough occurs when V_D affects the formation of inversion layer. Punchthrough leads to the rapid increase of drain current with V_D increase and the weak gate control.

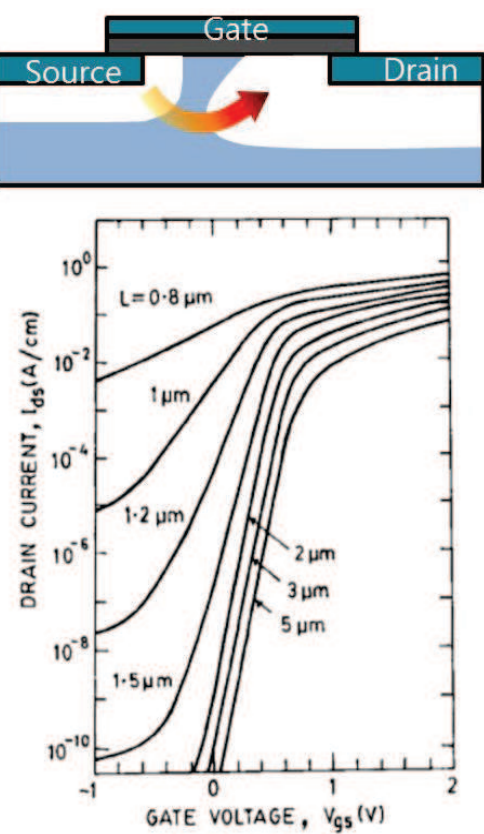


Figure 1.4 : (Above) Schematic of punchthrough. (Below) Calculated subthreshold characteristics V_{DS}=2V, V_{SB}=0 V [15].

There is similar but different consideration. This potential barrier is confirmed by the built-in potential of the source and channel p-n junction [17]. On the other hand, for a short channel device, V_{DS} lowers the potential barrier between source and channel, which is named drain-induced barrier lowering (DIBL) as shown in Fig. 1.5.

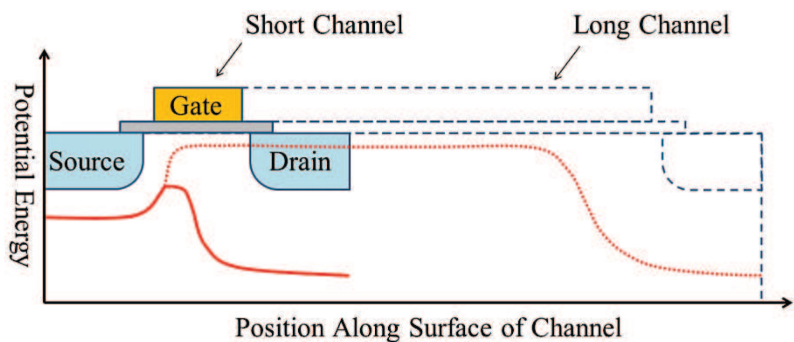


Figure 1.5 : Drain-induced barrier lowering in short channel device. Drain is biased and it pulls down the potential energy around drain.

This effect limits the maximum operation voltage of device [18]. To avoid DIBL, the enhancement of gate control or the separation of merged depletion region is needed. Thus, increase of substrate doping level, delta doping into the substrate and pocket or halo implant has been used in typical planar devices [19-21].

1.3.2 Velocity Saturation

In a short channel, electron transport is governed by the combined effects of electric field E and scattering with the lattice, impurity atoms and other carriers. At low electric field, this results in a mean velocity proportional to the electric field. [14]:

$$v_d = \mu E \ (cm/s) \,. \tag{1.4}$$

The constant μ is called carrier mobility and v_d the drift velocity.

However, due to the energy dependence of scattering relaxation time, its linear relationship is not valid at high electric field. The field dependence of drift velocity is then described by [22]:

$$v_d = \frac{\mu E}{1 + E/E_c} \text{ for } E < E_c \qquad \text{and} \tag{1.5}$$

$$v_d = v_{sat} \text{ for } E > E_c. \tag{1.6}$$

The dividing factor E_c named as critical field, is approximately 10^6 V/m (10^4 V/cm) for the silicon as shown in Fig. 1.6. When E is above E_c, carrier velocity is saturated to v_{sat}. This consideration changes the drain current I_D in nonlinear region from:

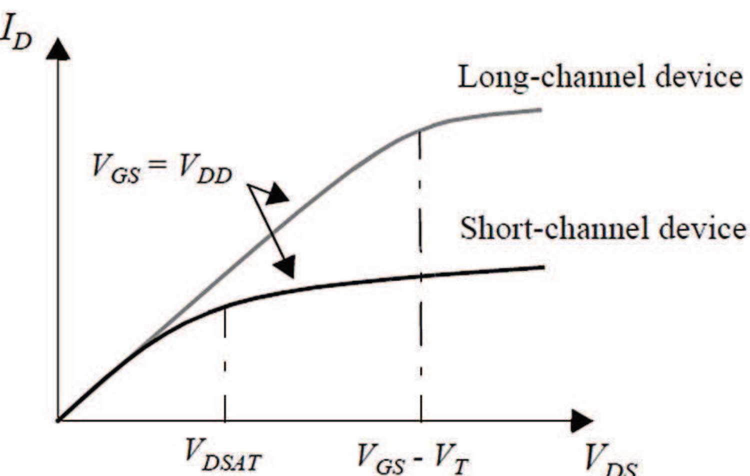


Figure 1.6 : Short channel effect by velocity saturation.

$$I_D = \mu C_{ox} \frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{{V_{DS}}^2}{2}\right] \quad \text{to} \tag{1.7}$$

$$I_D = k(V_{DS})\mu Cox \frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{{V_{DS}}^2}{2}\right], \text{where} \tag{1.8}$$

$$k(V_{DS}) = \frac{1}{1 + (V_{DS}/E_C\, L)}. \tag{1.9}$$

For the large value of L, k approaches 1. However for the short channel, k is smaller than 1 and I_D will be decreased by velocity saturation.

The short channel model can be simplified with the assumption of abrupt constant velocity at E_c.

$$v_d = v_{sat} = \mu E_c \qquad \text{for } E > E_c \quad \text{and} \tag{1.10}$$

$$V_{DSAT} = L E_c = \frac{L v_{sat}}{\mu}, \quad \text{thus} \tag{1.11}$$

$$I_{DSAT} = v_{SAT}\, Cox\, W\left[(V_{GS} - V_{th}) - \frac{V_{DSAT}}{2}\right]. \tag{1.12}$$

Comparing with the quadratic V_{GS} behavior in long channel devices, the linear behavior in short channel device has been proved empirically as shown in Fig. 1.7. Recently, 30nm devices has been used and the scaling down will be continued. In the case of a transistor which has 30 nm gate length, the effective electric field between source and drain is:

$$\frac{V_{DS}}{L} = \frac{0.5V}{30\,nm} = 1.6 \cdot 10^4\ V/cm \ , \tag{1.13}$$

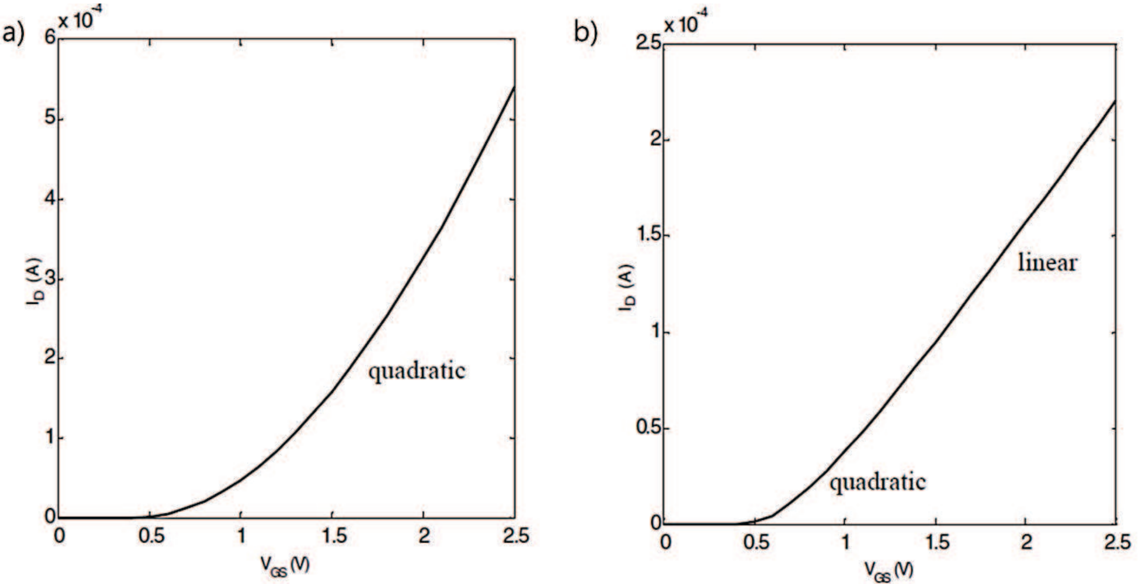


Figure 1.7 : I_D-V_G characteristic for long (L=10 μm) and short (L=0.25 μm) channel at V_D =1.5 V [23].

with 0.5 V V_{DS}. At 0.5V, it is already reached about 10^4 V/cm which is enough value to cause the velocity saturation of the carrier in the channel of the device.

1.3.3 Hot Carrier Effects

If carriers gain very high kinetic energy due to the strong electric field, it can be hot carriers. Hot carrier effect can be classified as [24]: 1) drain avalanche hot carrier injection, 2) channel hot carrier injection, 3) substrate hot electron injection, 4) secondary generated hot electron injection.

At high drain voltage bias, carriers are accelerated by high electric field near the drain. With stress conditions with high V_D and lower V_G, drain avalanche hot carrier injection occurs. When accelerated carriers are injected into the depletion region of drain, electron-hole pairs are generated, which is also called as impact ionization. Generated hot electrons and holes are injected into the gate oxide or flow out as a bulk current. Normally it happens at $V_D > 2V_G$.

Without electron-hole pair generation, accelerated channel hot carriers can be directly injected into the gate oxide by high V_G. It causes gate leakage current, interface and oxide degradation. It can occur around $V_G = V_D$.

From the high positive or negative bias at the substrate, substrate hot carrier injection occurs. In this condition, carriers optically or electrically generated in the substrate (bulk body) injected into the gate oxide and body. These injected carriers cause gate leakages and substrate current

1.4 Challenges to Overcome Short Channel Effects

In this chapter, advanced MOSFET technologies will be introduced. Advanced MOSFET technologies have been researched to overcome short channel effects and to enhance the device performances. They can be categorized as gate stack, silicon on insulator (SOI), channel engineering. There are several parts in channel engineering: channel structure, material and strain engineering. In the case of strain engineering, it will be detailed in chapter 4.2.1.

1.4.1 High-k and Metal Gate

As shown in table 2 (Ch. 1.2), the thickness of gate oxide should be decreased to maintain proper electric field according to the device scaling down. ITRS referred to sub 1 nm effective oxide thickness gate stacks are required at the roadmap in 2009 [25]. When the SiO_2 reaches thickness

below 1 nm, it causes the gate leakage problem due to the quantum mechanical tunneling [26]. Thus, as gate insulator, SiO_2 should be replaced with higher permittivity (high-k) dielectric material. With high-k dielectric layer, effective oxide thickness can be expressed as following:

$$EOT = \frac{k_{SiO2}}{k_{high-k}} = 3.9\frac{t_{high-k}}{k_{high-k}}, \qquad (1.14)$$

where k_{SiO_2} and $k_{high\text{-}k}$ are the dielectric constant of SiO_2 and high-k material, and $t_{high\text{-}k}$ the physical thickness of high-k dielectric layer. For instance, with a dielectric constant of 20 and 5 nm physical thickness, effective oxide thickness of 1 nm SiO_2 can be replaced. According to quantum mechanics, tunneling probability increases exponentially as a function of the barrier (gate dielectric layer in this case) thickness [27]. Thus, increased dielectric thickness can avoid tunneling induced gate leakage (Fig. 1.9).

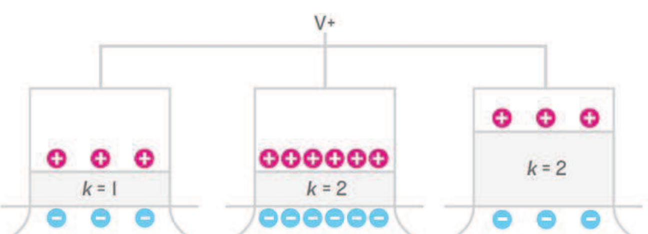


Figure 1.8 : Schematics of high-k gate dielectric. If one gate oxide has twice k of another, a given voltage will draw twice charge into the transistor channel. Or, the same amount of charge will accumulate, if the higher-k dielectric is made twice as thick [26].

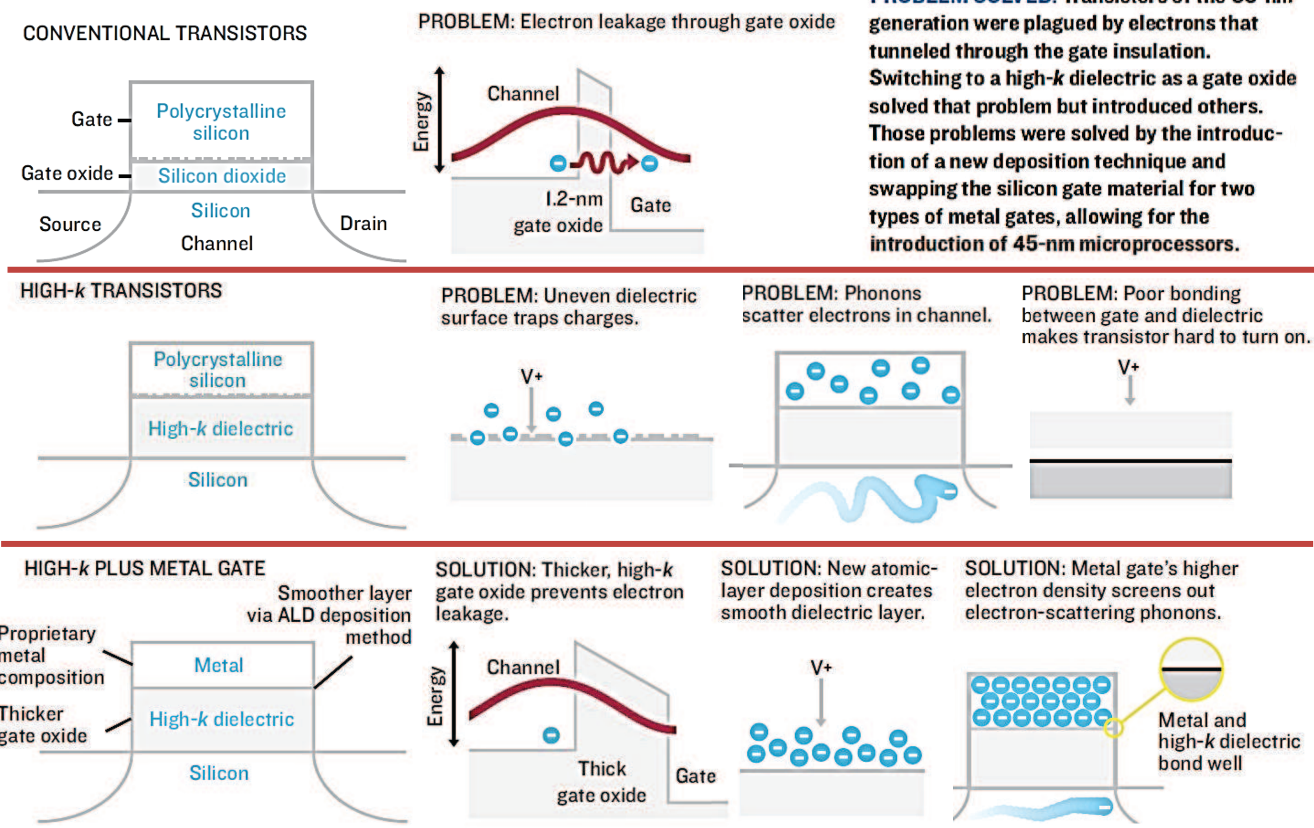


Figure 1.9 : High-k and metal gate for the solution of gate dielectric thinning and phonon scattering [26].

To select high-*k* material as a gate dielectric, several properties should be additionally considered such as semiconductor/gate dielectric band offset, thermodynamic stability, interface quality, film morphology, gate metal compatibility, process compatibility and reliability [28]. Hafnium based dielectric material such as HfO_2 and HfSiO, is one of promising materials for the high-*k* dielectric. From 45 nm process technology, Intel has been using hafnium based gate dielectric [29]. Comparing to 65 nm poly-Si/SiON structure, the gate leakage current of 45 nm metal/high-k gate stacked transistor was 1000 times reduced in PMOS and 25 times reduced in NMOS.

However, high-*k* gate dielectric has problems [27]. The quality of interface between high-*k* and poly-silicon gate is very poor so that the oxygen vacancy in the dielectric layer induce Fermi level pinning which causes high threshold voltages of device operation. Additionally, dipoles in the high-*k* dielectric vibrate like taut rubbers and induce strong vibrations in the lattice of Si channel. This surface phonon scattering in high-k is a primary source of mobility degradation.

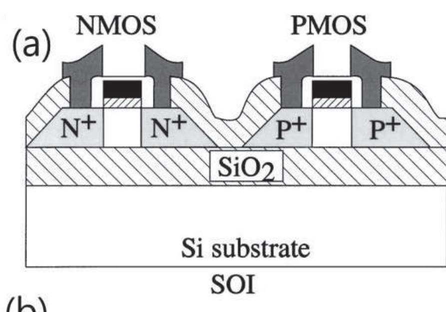
Significantly increased electrons in metal gate electrode can screen the dipole vibrations in high-*k* dielectric [27]. Thus surface phonon scattering is reduced. Moreover, the quality of interface can be improved and Fermi level pinning is reduced.

The use of high-*k* and metal gate stack requires the correct work function matching for both PMOS and NMOS for the higher device performance.

1.4.2 Silicon on Insulator

Silicon on insulator (SOI) is sandwiched silicon-oxide layer-silicon substrate. As shown in Fig. 1.10, the entire transistor is completely isolated from other transistors and back substrate by buried oxide (BOX) [30]. Vertically isolated device layer is protected from parasitic effects. Leakage current, radiation induced photocurrent and latch-up etc. can be induced in bulky substrate. SOI wafer reduce junction surface, leakage current and junction capacitance.

SOI wafer can be fabricated by several methods. Separated by implantation of oxygen (SIMOX) method uses oxygen ion beam implantation [31]. After thermal annealing, buried SiO_2 layer is formed into the Si wafer.



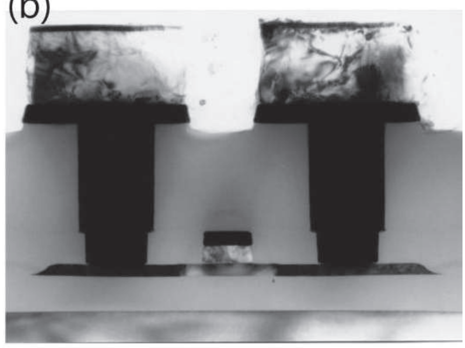


Figure 1.10 : Schematic architecture and TEM cross-section image of planar SOI MOSFET [29].

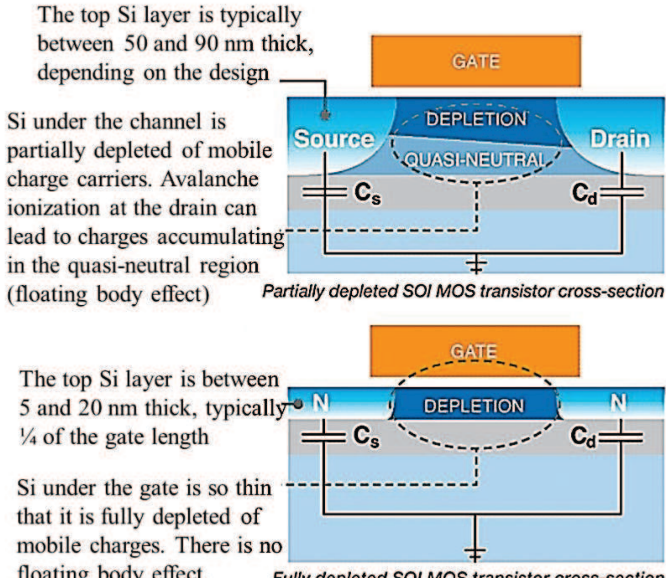


Figure 1.11 : Comparison between PD SOI and FD SOI [33].

ELTRAN process uses epitaxial layer grown on the porous Si [32]. After transfer using wafer bonding technique, it is separated to handle wafer. Smart Cut method developed by Soitec [33] utilizes hydrogen ion implantation as an atomic scalpel which cuts through the crystalline lattice. Clean and uniform transfer of thin film Si layer can be achieved by Smart Cut method.

According to the thickness of SOI wafer, it can be classified as partially depleted SOI (PD SOI) and fully depleted SOI (FD SOI) (shown in Fig. 1.11) [34].

PD SOI has relatively thick (t_{si} > 45 nm) device layer. In PD SOI, top gate and back gate (handle substrate) are decoupled due to the thickness of device layer. The depletion charge in the channel does not extend from the channel surface to the device layer / BOX interface. Thick enough device layer has floating body. PD SOI wafer has several problems from floating body effects [30]. Majority carriers can be collected in the neutral region of PD SOI MOSFET. When impact ionization trigger collected majority carriers, excess current and low frequency noise can be induced. Floating body also induce transient variation of body potential and threshold voltage.

FD SOI has thin body below 45 nm (typically below 20 nm). Due to its extremely small thickness, the whole body is depleted and the depletion charge is constant. The excellent coupling between gate voltage and channel inversion improves drain current, subthreshold swing and gate response time. Back gate is also more effective than PD SOI therefore threshold voltage control is possible using back gate bias. Floating body effects are strongly reduced in FD SOI devices.

However, there are issues to overcome of course. Low thermal conductivity of BOX induce Self-heating problem in FD SOI device. In saturation region, device temperature increases and current is lowered because of self-heating. Defect coupling is also a problem in FD SOI. The presence of defects at the device interface highly affects performance degradation. Carrier transport affected by defect scattering reduces effective mobility.

Even though SOI technology has few disadvantages, it obviously leads higher performances of device operation. To minimize short channel effects, SOI technology is one of the

promising alternatives with multi gate and nanowire structure which is following next chapter.

1.4.3 Multi Gate and Pseudo 1D Structure

Multi gate structure shown in Fig. 1.12 has been developed to enhance the immunity to short channel effects of classical single planar gate devices. Even in the SOI FETs, the body thickness t_{si} should be scaled down up to $L_{eff}/5$ for the good control of the short channel effects [35]. Due to the limitation of the process, it is very difficult to be uniform all over a SOI wafer. This variation makes the fluctuation of the device performances in nano-scale transistors [36, 37].

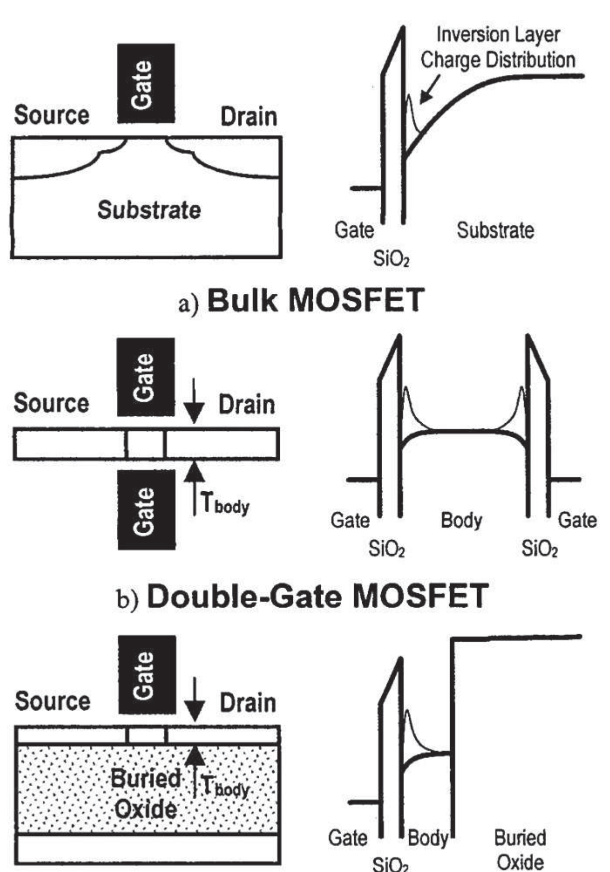


Figure 1.12 : Device structure and energy band diagram of standard single gate bulk MOSFET, double gate MOSFET and ultra-thin body MOSFETs. In standard single gate bulk MOSFET, the body far from the gate is difficult to control [32]

In the case of double gate, two systematic gates make inversion layers on both interfaces between the silicon layer and gates. Double gate FET can be fabricated both being planar and vertical. Gate electrodes are located at the side of vertical fin which has w_{si} as a fin width in the vertical double gate FET and at the top and bottom of the channel in the planar double gate FET. While t_{si} should be smaller than $L_{eff}/5$ in planar SOI transistor, w_{si} should be scaled down up to $L_{eff}/2$ [38]. Thus the gate control is enhanced without channel dopants. The absence of dopant induce no depletion charge (Q_{depl}=0). Effective gate electric field E_{eff} (vertical electric field in channel) consists of linear combination between Q_{depl} and Q_{inv}. A reduction of E_{eff} yields a higher carrier mobility scince the limitation due to the impurity scattering diminishes. It can also reduce interface scattering between Si layer and gate insulator and direct tunneling into the gate dielectric.

In this point of view, the electrostatic control of the gate electrodes can be enhanced by the

increased number of gates. Intel has announced that the next generation CPU platform named Ivy Bridge will be 22 nm manufacturing process instead of 32 nm process of Sandy Bridge. Ivy Bridge will use tri-gate finFET to solve the problem of short channel effects. It will bring lower power consumption and high clock speed due to the advantage of scaling down. Intel expects that 22 nm process finFET will be 37 % faster than current 32 nm process and will save the 50 % of active power.

Beyond the tri-gate finFET, Gate-All-Around (GAA) will be the optimized gate structure in 3D multi gate MOSFETs. GAA FET has gate electrodes wrapped around the channel region. Extremely narrow nanowire channel body has pseudo-1D channel structure. The short channel effect immunity of nanowire FET can be quantitatively analyzed by using natural length λ which can be derived from Poisson's equation (Table 1.3) [39].

Single Gate	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{si} t_{ox}}$
Double Gate	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{ox}} t_{si} t_{ox}}$
Triple Gate	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{3\varepsilon_{ox}} t_{si} t_{ox}}$
Gate-All-Around	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{8\varepsilon_{ox}} t_{si}^2 \ln\left(1 + \frac{2\,t_{ox}}{t_{si}}\right) + \frac{t_{si}^2}{16}}$

Table 1.3 : Natural length of devices depending on different gate structures [39].

The natural length is the length of the channel region controlled by the drain. It means that the smaller λ, the smaller short channel effect can be driven in given device structures. To be free of short channel effects, λ should be at least 5 times shorter than the effective gate length. From the equation of λ with single, double and triple gates, it can be simply guessed that approximately the value of λ can be estimated by division with the square root of gates number. Because the smaller λ can reduce the short channel effects, the device has good immunity from increased gate number.

Moreover, from these equations, it should be notable that the reduction of t_{ox} decreases short channel effects as it was discussed in previous section. Decreasing t_{ox} has a limitation due to the tunneling current leakages below 1.5 nm gate oxide thickness. Thus high-k gate dielectric can effectively reduce λ. The effect of t_{si} thinning is also essential to decrease λ and short channel effects. A quantum confinement induced by t_{si} reduction enhances the volume

inversion effect and yield the increase of V_{th}. However, ultra-thin body raises the mobility degradation even though the reduction of t_{si} can decrease short channel effects [40]. Thus, the optimization of the device scaling in the GAA MOSFET is still necessary to improve device performances.

1.5 Conclusion

In this chapter, recent trends and issues of semiconductor devices are investigated. Because the information technology is dramatically improved, the requirements of device such as smart phone and tablet PC have been exponentially increased. Coming up to these requirements and the fabrication cost down, semiconductor industries have been researching and developing device technologies.

Focused on the field effect transistors, a simple but the most critical issue is device scaling. While device scaling down increases device performances and decreases fabrication cost, it induces unintended short channel effects which affect performance degradation.

To overcome short channel effects, many technologies have been studied. High-k / metal gate stack helps as an alternative to gate oxide thinning. SOI technology has been introduced as substrate engineering. Even though SOI wafer is more expensive than conventional substrates, it obviously decreases short channel effects. For channel engineering, multi gate structure has been studied. Multi gate structure has better gate control.

As device dimension shrunk, recent device structures are converging toward the one dimensional structures like FinFETs or nanowire FETs. Based on this introduction, several topics will be discussed for the transport in quasi-1D nanostructure FETs. In chapter 2, device fabrication technology will be introduced based on my experience during study. In chapter 3, characterization techniques will follow. Transport in quasi-1D nanostructure FET (main topic of this thesis) will be discussed in chapter 4. In chapter 5, device simulation technique will be mentioned. As appendices, physical parameters and material properties of Si and SiGe which were used in my study are attached. Additionally, the development of e-beam lithography pattern generator and basic vacuum technology is supplemented.

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2. Nano-device Fabrication Technology

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2.1 Introduction

2.2 Top-down and Bottom-up

2.2.1 Bottom-up approach

2.2.2 Top-down approach

2.2.2.1 Photolithography

2.2.2.2 Electron Beam Lithography

2.2.2.3 Immersion Lithography

2.2.2.4 Wet Etching

2.2.2.4 Dry Etching

2.2.3 Convergence of Top-down and Bottom-up approach

2.3 Conclusion

Chapter 2 Nano-device Fabrication Technology

2.1 Introduction

As the size of the device is scaled down, fabrication process has been aggressively researched and developed. The limitations of the device fabrication instruments have been successfully overcome yet. Most of device fabrication is based on the CMOS fabrication process. Selective patterning with lithography technology has been making various device structures. Film deposition and etching technology build or carve the target materials for the intended structure.

Currently the geometry of device has been changed. The channel geometry of FET has become 3D structure compared to the previous planar device structures. The improvement of micro (or nano)-electromechanical systems (MEMs or NEMs) also makes the micro-nanostructure possible to be more complicated. Additionally the boundary line of the research field is getting ambiguous. For example, in the bio-medical engineering, nanostructure patterning is necessary to make bio sensors or chemical sensors. Thus the nano-scale device fabrication technology is not limited to the electrical engineering nowadays.

In this chapter, two main schemes of fabrication technology, (top-down and bottom-up) will be delineated. Principles of each fabrication process and the instruments which were used during the study will be described.

2.2 Top-down and Bottom-up

The concept of top-down and bottom-up approach was introduced by Foresight Institute in 1989.

It has been used to help people understand the differences between conventional manufacturing (the mass-production of large non-atomically precise objects) and molecular manufacturing (the mass production of large atomically precise objects). Currently nanotechnology has been researched and developed in both top-down and bottom-up field.

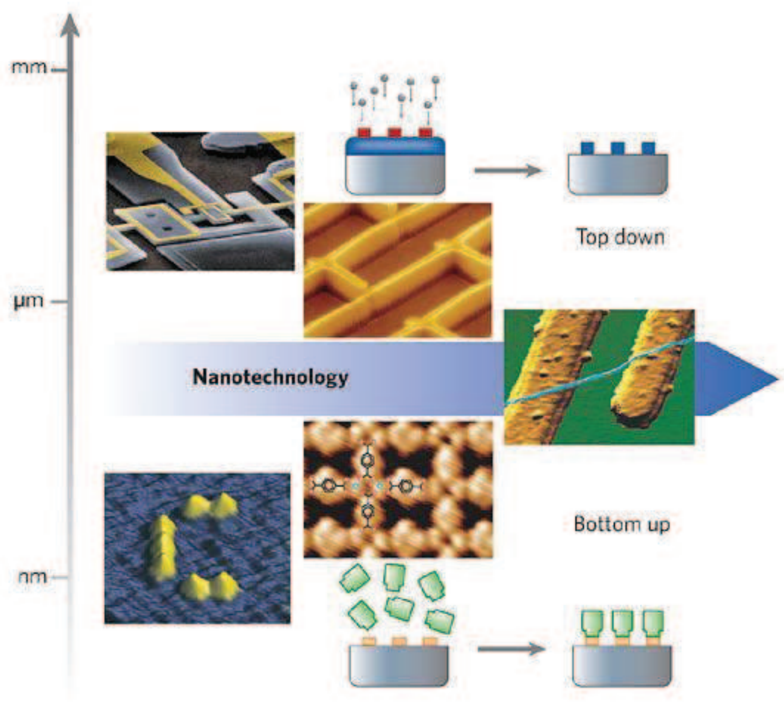

Figure 2.1 : Comparison between top-down and bottom-up approach [1].

2.2.1 Bottom-up approach

In nanotechnology, the bottom-up approach is the method to build up the nano-scale structure using molecular engineering such as self-organized growth and self-assembly.

To grow up nanowire structure, Vapor-Liquid-Solid (VLS) growth is widely used [2, 3]. As shown in Fig. 2.2, this method use metal nanoparticles or a metal pattern as a catalyst. From the gas flow support materials (for example, Si) and it is dissolved into the metal catalyst which is in the liquid phase at high temperature. Three phases exist in this process; vapor phase of gas flow, liquid phase of the catalyst and solid states of the growing structure (nanowire). The size of the synthesized structure depends on catalyst size.

In the case of thermal evaporation Oxide-Assisted Growth (OAG), no metal catalyst is needed during the process [3, 4]. There is no metal contamination. Thus the final products of OGA have good quality. The yield and the growth rate of the final products are high due to the reduction of the pre- and post-treatment process.

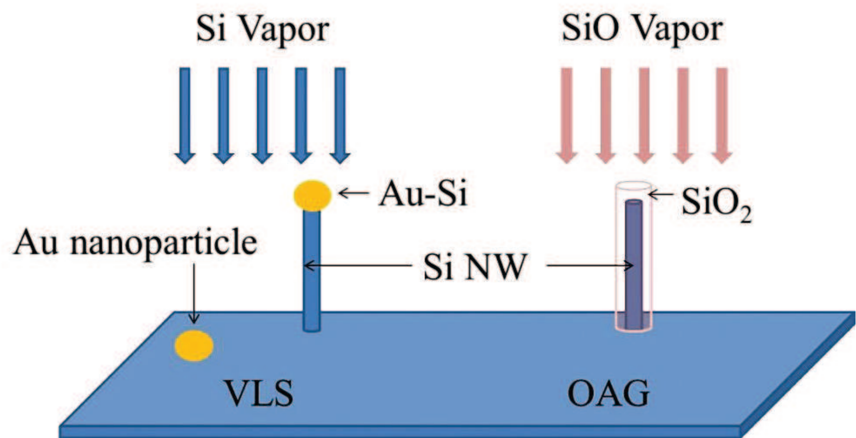

Figure 2.2 : Difference between VLS and OAG.

The laser ablation method is also used to synthesize nanowire structure [5]. In a furnace with high temperature, a heated target is ablated by a laser beam. The evaporated molecule is transported by inert gas and deposited as nanowires. This method has high yield and high purity.

In addition, there are other methods to synthesize nano-structure such as Molecular-Beam Epitaxy (MBE), and solution-phased synthesis (sol-gel method) [6, 7].

The device fabrication using bottom-up approach faced hard tasks in the view point of device integration for mass production. Highly integrated arrays with controlled orientation and spatial position are necessary to introduce nanowire into the mass production [8]. Nowadays this problem is getting solved through continuous challenge of research. Since the beginning of study, the electrophoresis has been used to align nanowire and nanotubes. However, it could not be available in mass production but for single device fabrication at academic level due to the difficulty of fine control for the moment [9]. Shear flow has also

been used. Passing nanowire suspension through microfluidic channel, well ordered nanowire array device fabrications have been shown [10]. Alignment can be controlled by flow rate and the size of nanowire can be limited by the diameter of microfluidic channel. However, there is no commercial device by using bottom-up approach yet. To be applied to the commercial product, the problems originally from the randomness of bottom-up fabrication process have to be solved.

2.2.2 Top-down approach

The top-down methods start from bulk structure while the bottom-up start from building up atomic structure. Conventional CMOS fabrication technology is based on the top-down approach. Previously the size of nanowires (or the width of fins) fabricated by top-down approach was not really 'nano' scale because the diameter or width of nanowire depends on the resolution of lithography. Alongside the improvement of the lithography technology, nanowire device can be fabricated with several nanometer diameters [11, 12] and eventually it can be called quasi-1D nanostructure. In academic research e-beam lithography has been used to fabricate quasi-1D nanostructure but it is not suitable for mass production. To be close to mass production, other advanced lithography technologies are aggressively challenged. Not only lithography but also etching is very important for the fabrication of quasi-1D nanostructure. For quasi-1D nanostructure, the uniform isotropic etching is necessary. Especially, when dimension reach 10 nm range, surface roughness becomes critical. Surface roughness affects device structure and quality. The carrier transport of quasi-1D nanostructure device is directly affected by device structure. In this chapter, various CMOS fabrication technologies will be covered. Advanced lithography technologies and etching techniques will be introduced and the results of top-down fabricated quasi-1D nanostructure will be shown.

2.2.2.1 Photolithography

In the IC industry, photolithography is the most widely used technique to transfer the pattern from mask onto the target. Photolithography is matured rapidly and continuously improved associated with the challenges of IC integration.

Basically, photolithography needs a mask for the pattern transfer. An optically flat glass or quartz plate is used as a mask base. The metallic pattern covers the mask base to block the transfer of light. Chrome is widely used for the metallic pattern layer. Laser beam or electron beam lithography is used to define tiny patterns. For the smallest feature size, a phase shift mask can be used to take advantage of the interference by the difference of phase. For example, Intel has used the alternating phase shift mask for below 65 nm process [13-15]. Currently, leading edge photo masks have 4~5 times shrunken pattern than the final chip pattern. This kind of mask has been used with stepper (Fig. 2.3). In stepper, the wafer stage is rapidly stepped under the optical column from position to position until exposure is fully achieved [16].

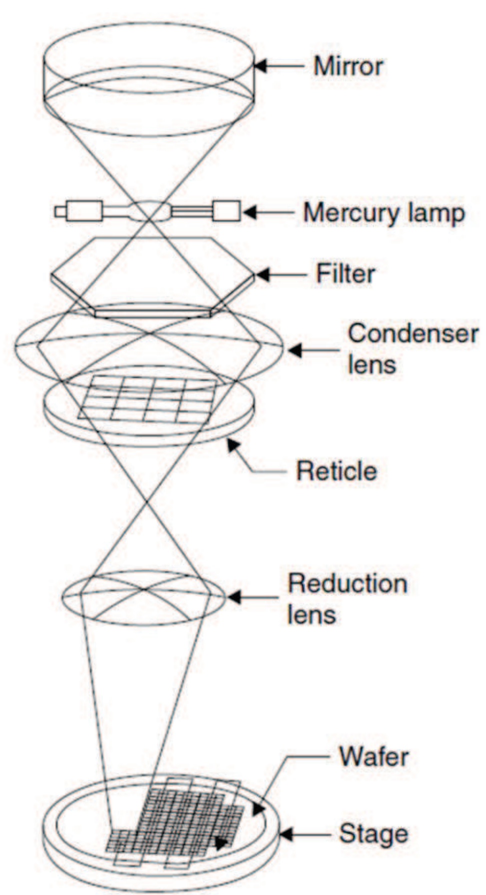

Figure 2.3 : Stepper system for photolithography [15] .

Usual photolithography process is as following: 1. Cleaning wafer; standard wafer cleaning named RCA clean is necessary for wafer preparation before the resist coating. RCA clean includes organic clean, oxide strip and ionic clean [17]. 2. Photoresist coating; basically the photoresist consists of a polymer, a sensitizer (photo active compound) and a solvent [18]. 3. Soft baking; the soft baking removes solvent and stress. 4. Exposure. 5. Development. According to the desired process, post-baking can be added after exposure process. There are two types of photoresist ‘positive’ and ‘negative’. Positive photoresist is the most common photoresist. The exposed area will be developed and then filled with metal or etched. Negative photoresist is widely used as etching mask. The exposed negative photoresist is not soluble in the developer. Thus only unexposed layer will be removed. After all the other post-exposure process including metallization or etching, photoresist is removed from the substrate by resist remover (wet process) or oxygen plasma ashing (dry process).

2.2.2.2 Electron Beam Lithography

Electron Beam (E-beam) Lithography offers higher patterning resolution than the photo lithography. It is based on the wave nature of electrons. According to the de Broglie equation,

$$\lambda = \frac{h}{p} \quad , \tag{2.1}$$

where λ is de Broglie wave length, h Plank's constant and p the relative momentum of the electron. From the kinetic energy of the electron, accelerated electron velocity in the electric field is,

$$v = \sqrt{\frac{2E_k}{m_0}} = \sqrt{\frac{2qU}{m_0}} \tag{2.2}$$

because $E_k = \frac{1}{2} m_0 v^2$,

$F = qE$ and $F = \frac{dU}{dx}$,

where E_k is the kinetic energy of electron, v the electron velocity, q the elementary charge, U the electric potential. SEM is typically used with the acceleration voltage of 10 kV and electron is accelerated about 20 % of the light speed. In the case of TEM, 200 kV is normally used and the speed of electron is about 70 % of the light speed. From de Broglie equation, λ can be described as:

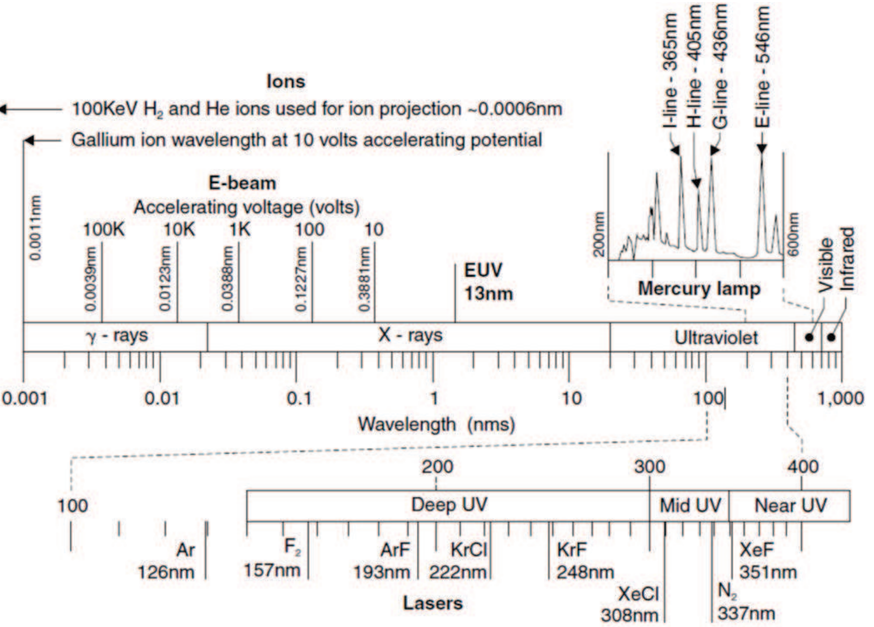

Figure 2.4 : Exposure source and wavelength [15].

$$\lambda = \frac{h}{p} = \frac{h}{m_0 v} = \frac{h}{\sqrt{2m_0 qU}} \ . \tag{2.3}$$

However, the speed of accelerated electron is close to the light one. Thus, relative expression should be used as following:

$$\lambda = \frac{h}{\sqrt{2m_0 qU}} \frac{1}{\sqrt{1 + \frac{qU}{2m_0 c^2}}} \tag{2.4}$$

c is the speed of light. In 10 kV SEM, λ is about 12 pm even while the wavelength of X-ray is 100 pm order.

E-beam lithography doesn't need masks. Electron beam directly draws the pattern on the sample surface. Thus it is helpful to produce various patterns without wasting the cost of photo masks. However the direct drawing makes the process slower than photo lithography. E-beam lithography is not suitable for mass production yet because of its throughput. However, it is commonly used for the fabrication of advanced nanostructure.

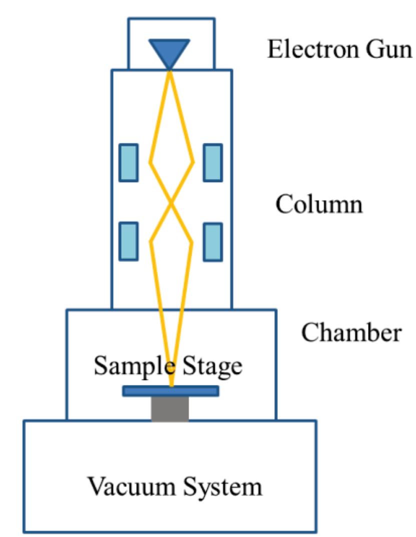

Figure 2.5 : E-beam lithography system

E-beam lithography can be carried out from following systems as shown in Fig. 2.5.

A) An electron gun makes electron. There are two types (thermionic and field emission) of electron source. In thermionic source, electrons are emitted by heating the source material such as W or LaB_6. LaB_6 source has higher brightness and longer life time than W while W source does not need high vacuum condition like LaB_6. In field emission source, a biased sharp tip emits electrons with high electric field. Field emission type has better resolution and brightness than thermal type. However, Field emission source need ultrahigh vacuum condition and extremely expensive cost.

B) An electron column focuses the electron beam. It is designed to make the definite beam diameter or beam shape. Focusing and defocusing lenses and apertures are equipped in the electron column to control it. There is beam blanker to switch the beam on and off.

C) Sample stage control the spot position to draw the pattern properly. Because the deflection system can only address a field of hundreds of micron, it is necessary to move the sample under the beam. An interferometer measures the position of the stage and about several nanometer accuracy can be achieved.

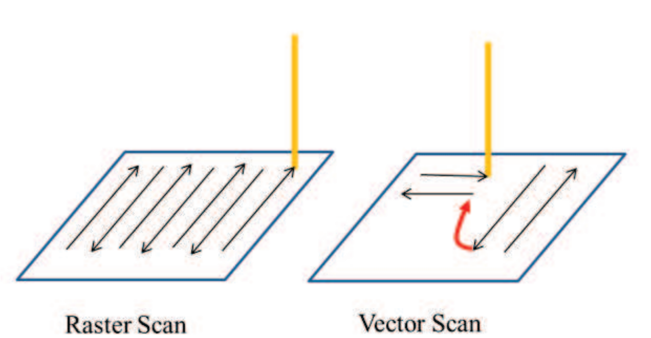

Figure 2.6 : Schematics of raster scan mode and vector scan mode.

Whole system should be under high vacuum to form the electron beam and

strongly shielded by electromagnetic field and external vibrations to control definite beam condition and position.

To draw the pattern, pattern files have to be prepared by Computer-aided Design (CAD) tool or others. Normally Graphic Database System II (GDSII) format is used to design patterns but ACSII format can be available. In the case of ASCII, protocols could be different depending on the instruments company. With pattern filed, electron beam or stage moves on the proper position of design and beam blanker switch to draw it. There are two different drawing schemes (raster scan and vector scan, shown in Fig. 2.6). In raster scan, every points of the design addressed by sample stage and deflection system and beam blanker switch the e-beam according to the structure. In vector scan, points which have structures are only addressed so that exposure time is shorter than raster scan mode.

Time to expose is defined by following relationship.

$$T \cdot I = D \cdot A, \tag{2.5}$$

where T is the exposure time, I the beam current, D the area dose and A the area exposed. According to this relationship, D can be determined as $D = T \cdot I / A$.

Accelerated electrons lose their energy by scattering with the surface. When patterns are close enough, scattered electrons are overlapped and proximity effects appeared. It depends on the pattern size, pattern shape, resist thickness, acceleration voltage and exposure dose. Proximity effects can be controlled by proximity correction programming.

2.2.2.3 Immersion Lithography

As it mentioned in previous part, the throughput of E-beam lithography is not suitable for mass production. Immersion lithography is a promising photolithography alternative resolution enhancement technology. Immersion lithography uses a liquid medium between final lens and the wafer surface instead of air gap in usual photolithography. The refractive index of liquid medium, bigger than 1, is used. For example, the refractive index of water used in immersion lithography with 193 nm wavelength ultraviolet light is 1.44 at room temperature.

The resolution of minimum feature size (R) and the depth of focus (DOF) in photo lithography is according to the Rayleigh resolution limit (or called angular resolution limit) [19, 20].

$$R = k_1 \frac{\lambda}{NA} = k_1 \frac{\lambda}{n \sin\theta} = k_1 \frac{\lambda / n}{\sin\theta} \tag{2.6}$$

$$DOF = k_2 \frac{\lambda}{n\sin^2\theta} = k_2 \frac{\lambda/n}{\sin^2\theta} = k_1 \frac{\lambda n}{NA^2} \quad (2.7)$$

NA is the lens numerical aperture, n the refractive index, k_1, k_2 the process factor from engineering experiences.

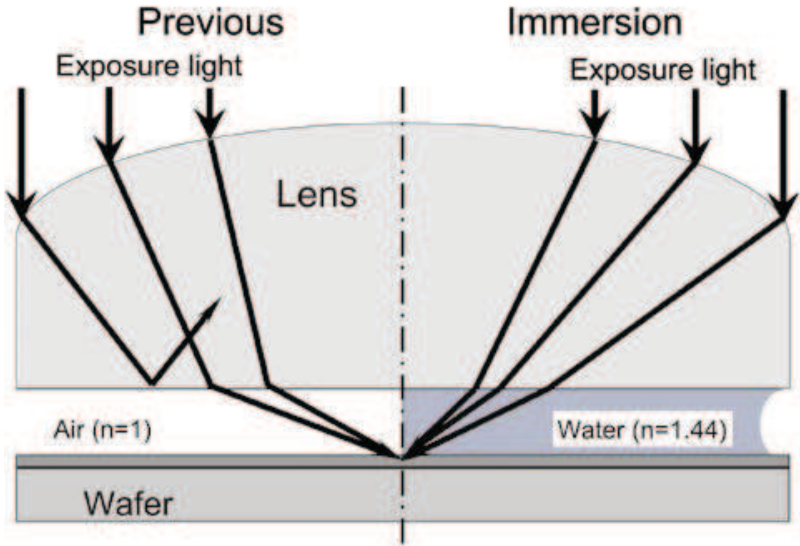

Figure 2.7 : Difference between previous photo lithography and immersion lithography [21].

To enhance the resolution, the reduction of λ or increase of NA is needed. In the DOF point of view, increase of NA makes small DOF and the manufacture of huge microscope is impractical [22]. Thus λ has to be mainly decreased.

With air medium, the resolution of ArF light source lithography (193 nm) can be calculated as:

$$R = k_1 \frac{\lambda}{NA} = 0.25 \frac{193}{0.93} = 52\,nm\,. \quad (2.8)$$

It is not enough to arrive at 45 nm process which is popular nowadays. However, using the liquid medium as shown in Fig. 2.7, effective wavelength can be reduced as:

$$R = k_1 \frac{\lambda/n}{NA} = 0.25 \frac{1.44}{0.93} = 35\,nm\,. \quad (2.9)$$

Light Soruce	Medium	n	λ/n
ArF (Dry)	Air	1	193 nm
F_2 (Dry)	N_2	1	157 nm
ArF (Wet)	H_2O	1.44	134 nm
ArF (Wet)	High-index Fluid	1.64	118 nm
F_2 (Wet)	Perfluoropolyether	1.37	115 nm

Table 2.1 : Effective wavelength a variety of lithography technology [23]

The molecular fluorine (F_2) excimer LASER lithography (157 nm) is also possible to decrease effective wave length but there are lots of problems due to its expensive cost, light absorption in lens and hard pellicle etc. Thus currently ArF immersion lithography has been widely researched and developed.

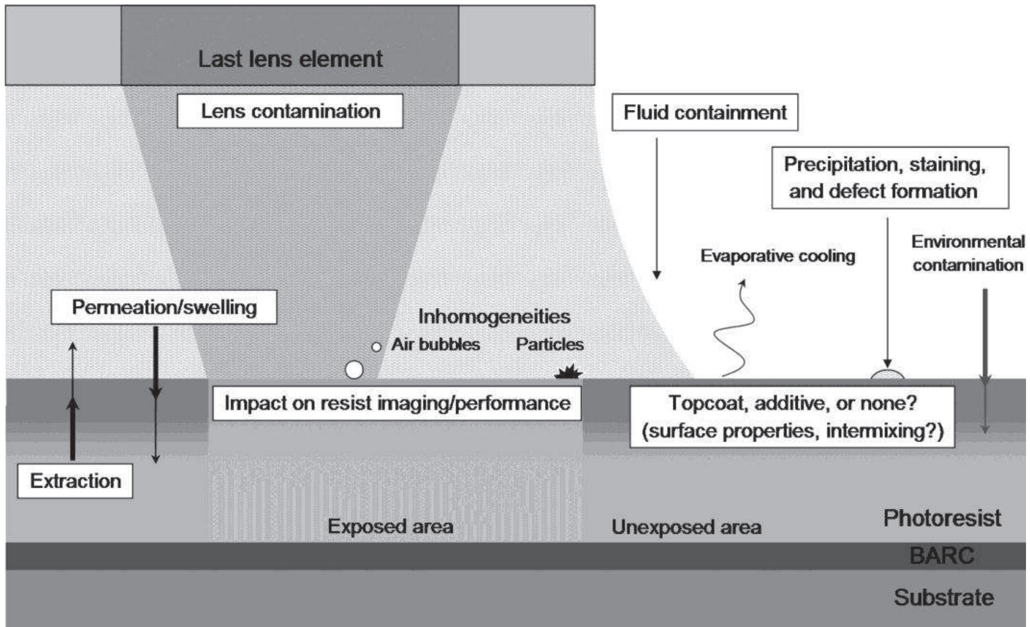

Figure 2.8 : Interactions between liquid medium and photoresist in immersion lithography [23].

However, there are several issues to optimize immersion lithography technology. The interaction between photoresist and water is the most representative problem (Fig. 2.8). For example, water can penetrate photoresist and the component of photoresist can be dissolved into water [24]. The lens can be contaminated by liquid medium. After exposure, the formation of air bubbles [25, 26], particles [27, 28], watermark defect by residue of the liquid medium [29, 30], bridging [31, 32], resist swelling [30] and drying strain [33, 34] can also be created.

The residual bubble can be reduced by additional super-hydrophobic top-coating layer. It prevents direct contact between water and photoresist. For the transparency with ArF light source, cyclic fluorine or acrylate material can be used. Moreover, top-coatless photo resist has been developed to reduce cost and process time [35, 36]. There is no big difference in the basic properties from the photoresist of ArF but it includes original functions of top-coating layer.

2.2.2.4 Wet Etching

An etching process is necessary to remove material from bare or pre-patterned substrate. The etching process is roughly categorized as wet etching and dry etching. For the fabrication of nanowire or the other micro/nano structures, selected regions on the surface of wafer are masked using lithography techniques and uncovered area is removed.

Etching rate (ER) is expressed in nm/min or μ/min and the etching rate of more than 50 nm/min is required for high fabrication throughput [37]. Etching process needs uniformity. Poor etching uniformity enhances surface roughness of nanostructure. Uniformity of etching process can be defined as :

$$U = \frac{ER_{high} - ER_{low}}{ER_{high} + ER_{low}}, \qquad (2.10)$$

where ER_{high} is the maximum etch rate and ER_{low} the minimum etch rate. The geometry of pattern can affect the uniformity of etching rate. Etching selectivity is also important. For selective patterning, the etching mask has to endure during the etching process. It can be described with the mask etching rate versus substrate etching rate.

Wet etching can be orientation-independent (isotropic) or orientation-dependent (anisotropic) depending on etchant. The anisotropy of etching process is defined as following:

$$A = 1 - \frac{ER_L}{ER_V}, \qquad (2.11)$$

where ER_L is the lateral etching rate and ER_V the vertical etching rate. In the case of ideal isotropic etch, A becomes zero and the value of ER_L is same as ER_V. For the isotropic etchant of Si, the mixture of HF, HNO_3 and acetic acid (called HNA) is used. SiO_2 and silicon nitride can be isotropically etched using HF and H_3PO_4 respectively.

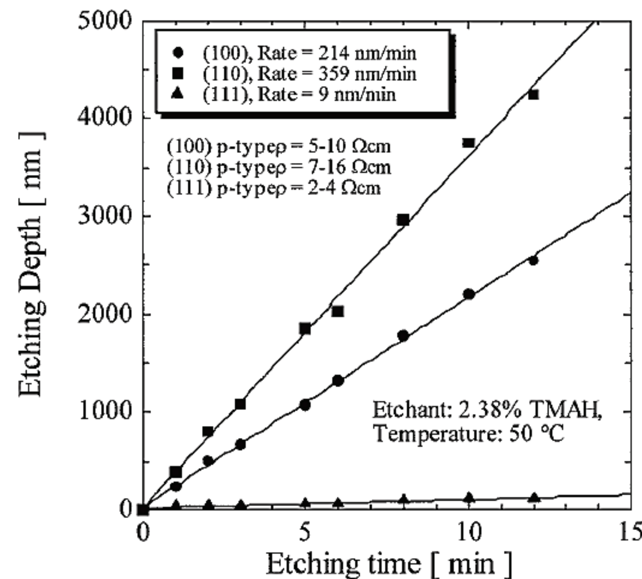

Figure 2.9 : Orientation-dependent etching using TMAH. [38]

Anisotropic etching is based on orientation-dependent etching speed. For example, the etch rate of Si at {111} surface is obviously slower than {110} and {100}. It is caused by crystal surface properties. The differences in surface density of silicon bonds, bonding energy of silicon atoms and

interstitial space on the interface between silicon and silica result in differences in etching rates. From these reasons, the etch rate of Si on {110} surface is several hundred times higher than {111} surface. KOH is one of the most widely used anisotropic etchant for Si. With KOH, the etch rates of {110}:{100}:{111} are in the ratio of 600:400:1. However KOH is corrosive. KOH causes damage to Al and the other metals. Moreover potassium ion is a serious contamination source during the process. Inserted K^+ ions result in device reliability problem. Thus KOH is not used in IC clean room nowadays. Tetramethylammonium hydroxide (TMAH) is another useful Si etchant for anisotropic etching (Fig. 2.9). It does not have any alkali ion. Thus TMAH is suitable for the IC clean room process. Relative etching rates can be reached up to several hundred [38]. For the fabrication of finFET, orientation-dependent etching of (100) SOI wafer using TMAH is emulatively researched as an alternative to dry etching technique.

Wet etching is good for the process of wide surface. Thus it is low cost process. However, there are many problems in the wet etching. Etching rates are varied by shaking condition, temperature and doping concentration. Many etchants are not adaptable for the CMOS process due to the contamination problems. Undercut below etching mask cannot be perfectly solvable which can be critical for the nanostructures.

2.2.2.5 Dry Etching

2.2.2.5.1 Plasma

Dry etching is assisted by plasma (it is also calls plasma assisted etching). The term plasma was coined by American physicist Irving Langmuir. Simply the plasma can be considered as a heavily ionized gas. Plasma is a nearly neutral mixture composed of excited neutral species (radicals), ions and electrons [39]. The degree of ionization is the proportion of atoms which lose or gain electrons, and it is related to the plasma density. Thus plasma has charges at local scale but globally it is neutral.

To induce the plasma, molecules should be excited with a high energy. Using the high energy, the link among atoms can be broken up and ions will be separated. For the general usage, the increase of temperature or an electromagnetic excitation is used to induce plasma. However, the electromagnetic excitation method is used for the dry etching technique. For the excitation, strong RF power source (13.56 MHz) is used.

2.2.2.5.2 Plasma Etching (PE)

Plasma etching is preceded by ionized gas mixture inside a chamber. RF excitation makes the gases ionized in the chamber. A target wafer is located on the ground electrode in the low pressure chamber which has the range from several mTorr to hundreds of mTorr. Induced plasma by RF power directly contacts with the target wafer. The chemical reaction between the plasma and the wafer etches the target wafer. The output products of PE can be highly isotropic etched.

2.2.2.5.3 Reactive Ion Etching (RIE)

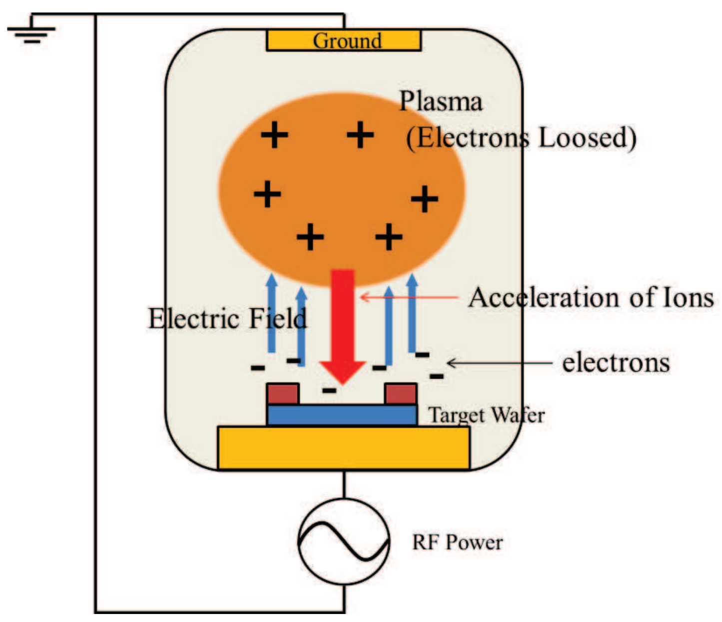

Figure 2.10 : Schematics of the RIE process.

Reactive ion etching is a variation of PE. In RIE, the target wafer is located on the RF power source and the top electrode is connected to the ground as shown in Fig. 2.10. Because the electrons are lighter than positive ions, the target wafer connected to the RF signal is more frequently contacted with electrons. Thus the target wafer is negatively charged by electrons. At the same time, globally neutral plasma changed to positively charged due to the loss of electrons. Polarization of the chamber inside induces the electric field and it accelerates the positive ions toward the target wafer. RIE process is basically combination of chemical and physical etching. The impact of accelerated ion strip away the molecules on the target wafer. It has very low selectivity but is highly anisotropic. In the case of PE, the movements of ions are Brownian random motion. In contrast, in RIE, the direction of ions movements is aligned by induced electric field.

To get the highly anisotropic ratio, target material should have a high capacity to adsorb electrons. Without the electric field due to the charging effect, RIE is similar to PE. Dielectric materials have a poor capacity of electron adsorption comparing to the semiconductors and metals. Thus, normally, dielectric materials are not well suitable for the highly anisotropic etching in RIE.

2.2.2.5.4 Inductively Coupled Plasma – RIE (ICP-RIE) and Bosch Process

Inductively coupled plasma – reactive ion etching (ICP-RIE) is a variation of RIE. As the wafer size is getting larger, the distance between top electrode and the target wafer should be longer to get the uniformly etched output in the RIE system. In this case, higher voltage should be used for the RF source. ICP-RIE chamber is surrounded by inductive coil. The RF coils induces an alternating magnetic field. This alternating magnetic field induces an electric field which smashes the plasma with accelerated electrons. It helps to generate high-density plasma. This is related to the major advantage of ICP-RIE system. It is possible to control almost independently the plasma density and ion energy while an etching process is executed. It is also possible to get more anisotropic patterns, and faster etch rates depending on the parameters of the system. Thus, compared to the RIE, ICP-RIE has several advantages, such as higher etch rate, enhanced vertical profile, clean and low damaged surface [40].

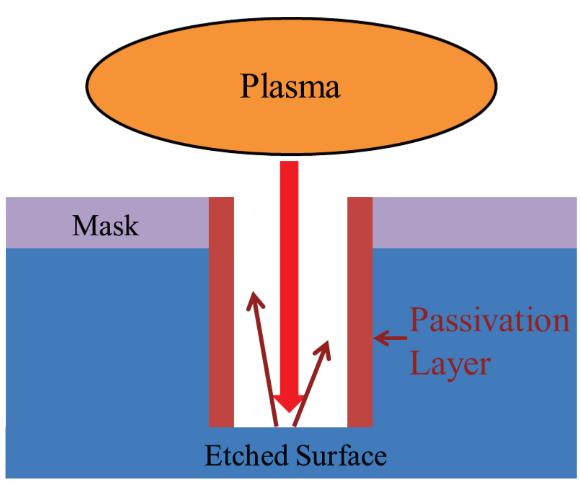

Figure 2.11 : Schematics of Bosch process.

The Bosch process is a patented process developed by Bosch Inc (Fig. 2.11). It is used for a deep etching thus it is called deep RIE (DRIE). In the case of Si, it is difficult to etch anisotropically. The etching with the fluorine based gases, such as CF_4 and SF_6 are basically isotropic. However highly isotropic etching can be achieved using the Bosch process. During etching, it creates a passivation layer on the etched surface. The output of the chemical reaction is re-deposited on the etched surface and it protects the already etched surface during etching. Passivation uses a fluorocarbon process, using gases such as C_4F_8, C_3F_6 or CHF_3. The Bosch process is used to make deep trench and for MEMs fabrication.

2.2.2.5.4 Ion Beam Etching and O_2 Plasma

Ion beam etching (IBE) is pure physical etching. It is sometimes called ion beam milling. Very high energy and neutral gas (normally Ar) are used to make the target wafer etched. IBE is often used to etch metals and the other materials which have poor chemical reactivity.

Because IBE is pure physical etching process, it can etch anything. However it can generate heating problems, physical damages on the substrate. Thus, the selection and the condition of pattern mask are very important.

The wafer stage of IBE is tilted to avoid the re-deposition of etched material. Because IBE has not any chemical reaction, it is not volatile.

O_2 plasma etching is widely used to remove carbon based materials. It is used to remove the residue of the photoresist or the other carbon contamination. As the interest of carbon based device increases, O_2 plasma etching is also used to make the nano-scale pattern of carbon nanotube and graphene [41].

2.2.2.5.5 Application and Issue

As the dimension of the device reduced, the portion of dry etching in the fabrication process is increased. For instance, the dimension of graphene is controlled using RIE and O_2 plasma in academic research [42]. Graphene is 2D structure material but nanoribbon (1D) or nanomesh (1.5D) structure can be fabricated. Dimension modified structure shows improved gate dependency and mobility. FinFET is a good industrial example. To make 3D gate structure, etching process is unavoidable. Especially the quality of etched surface is one of the most important factors for the device performance [43]. Thus to achieve the optimized device performance, clean and uniform surface condition should be defined by improved etching process.

2.2.3 Conclusion: Convergence of Top-down and Bottom-up

Currently the top-down and bottom-up approach are converging. As mentioned in the introduction of this chapter, this phenomenon is related with the convergence of research fields. For example, bottom-up fabricated ZnO nanowire can be applied for the diagnosis of rheumatoid arthritis [44]. In this case, medical science and material engineering are converged. For the mass production and human interface, it should be combined with CMOS process which is top-down. With ZnO nanowire, here is another example of complete top-down/bottom-up converged device (Fig. 2.12). ZnO nanowire network is synthesized on the bottom electrode (top-down) using a sol-gel process (bottom-up) [7]. This device has superior performance as a hydrogen gas sensor due to the porous 3D nanowire network structure.

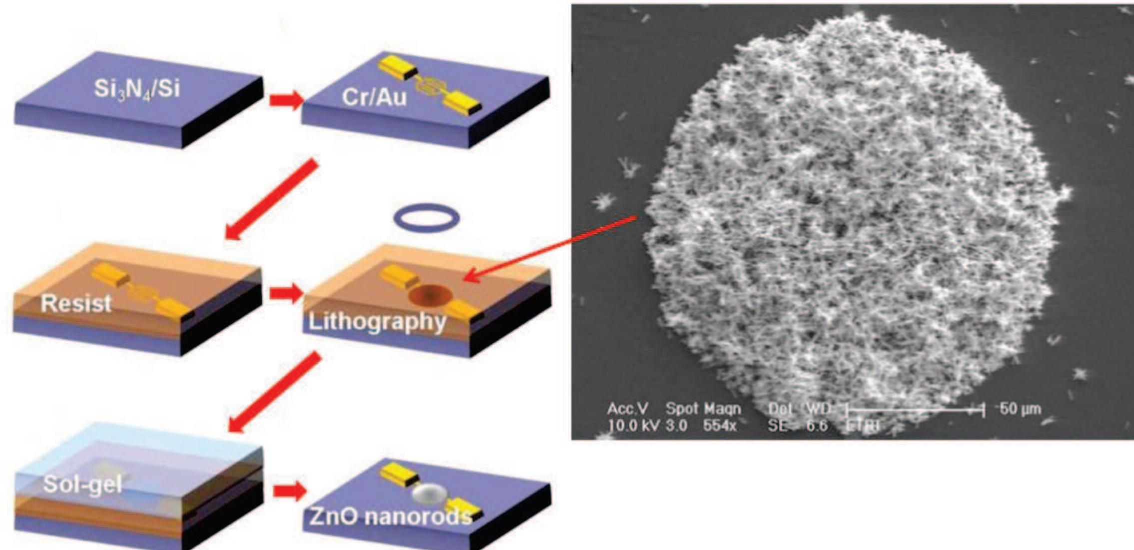

Figure 2.12 : ZnO nanowire network sensor using top-down/bottom-up convergence [7].

As another example, recently graphene nanopore has been studying for the DNA sequencing [45]. Previously, only top-down based SiN membrane was used for the similar concept. However, the appearance of graphene monolayer leads the research of DNA sequencing to the graphene nanopore devices. Because the thickness of graphene is same as one carbon atom, single molecule level detection is possible when the DNA passes through nanopore.

As we can see in the given examples, the convergence of top-down and bottom-up is a recent trend and a solution to overcome the limitation of each fabrication methods.

2.3 Conclusion

In this chapter, various fabrication techniques have been investigated. Bottom-up approach possibly gives cheap solution for mass production because of its self-assembly process. Atomic level feature size can be controlled by bottom-up approach. However, uniformity of device fabrication may not be good because of the randomness of molecular behavior during the process. On the other hand, respectively uniform device quality can be achieved using top-down approach (CMOS compatible process). Most of recent device fabrications are carried out based on lithography technique in top-down approach. However device scaling down using top-down approach almost arrives at the fabrication limitation. To solve this problem and to enhance device performances, convergence of top-down and bottom approach is currently studied. Probably it can be a key of leading next generation fabrication technology.

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3. Characterization and Parameter Extraction of FET

3. Characterization and Parameter Extraction of FET

3.1 Introduction

3.2 Basic MOSFET Operation

3.2.1 Linear Regime (at Small V_D)

3.2.2 Saturation Regime (at high V_D)

3.2.3 Transfer characteristics: V_{th} and Subthreshold Swing

3.2.3.1 Threshold Voltage

3.2.3.2 Subthreshold Swing

3.2.4 Mobility

3.2.4.1 Carrier Scattering

3.2.4.2 Mobility in MOSFET

3.2.4.3 Other mobilities

3.2.5 Noise

3.3 Characterization and Parameter Extraction Technique

3.3.1 Series Resistance

3.3.2 Effective Channel Geometry

3.3.3 Y-function Method

3.3.4 Split C-V

3.4 Conclusion

Chapter 3
Characterization and Analysis of FET

3.1 Introduction

As discussed in chapter 1, scaling down makes the future MOSFET more and more departed from the conventional planar bulk FET such as SiO2 gate dielectric, poly-silicon gate. Many approximated physical phenomena affect MOSFET operation due to the dramatic scaling down. For example, decrease of channel dimension results in surface roughness effects which degrade the effective mobility in the channel transport. Effective gate length becomes important because its portion in the geometrical channel length is relatively increased. Series resistance affects not only drain current but also threshold voltage. Thus, device characterization techniques need to be detailed and improved.

In the development of advanced FET, feedback between device fabrication and characterization is essential for the device optimization. Therefore, accurate parameter extraction is very important in the advanced devices.

In this chapter, basic operation of MOSFET and detail of its characterization will be investigated. Based on the measurement techniques, device parameter extraction will be discussed.

3.2 Basic MOSFET Operation

Here, the basic MOSFET model equation will be shown to support the device parameter extraction later. Chapter 3.2.1 and 3.2.2 will remind us classic MOSFET operations based on long channel device model.

3.2.1 Linear Regime (at Small V_D)

At small drain voltage ($V_D < (V_G - V_{th})$), MOSFET operates in the linear regime. The drain current I_D in the linear regime can be expressed as:

$$I_D = \frac{W}{L} \mu_{eff} C_{ox} (V_G - V_{th}) V_D, \qquad (3.1)$$

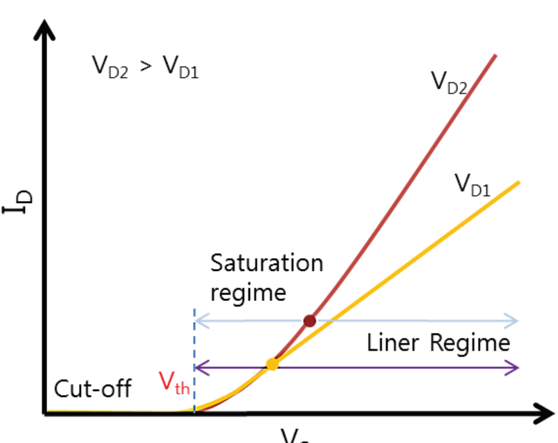

Figure 3.1 : FET operation schemes in transfer (I_D-V_G) characteristics.

where W is the channel width, L the channel length, μ_{eff} the effective mobility and C_{ox} the effective capacitance of gate oxide. In short and narrow channel, the effective gate capacitance includes quantum confinement effect (called dark-space) [1]. From Eq. 3.1, if μ_{eff} is constant, the transconductance g_m can be calculated as:

$$g_m = \left. \frac{\partial I_D}{\partial V_G} \right|_{V_D = Const.} = \frac{W}{L} \mu_{eff} C_{ox} V_D. \qquad (3.2)$$

At linear regime, MOSFET operates as a gate controlled resistance.

3.2.2 Saturation Regime (at high V_D)

After pinch-off ($V_D > (V_G - V_{th})$), the drain current of MOSFET is saturated as:

$$I_D = \frac{W}{2L} \mu_{sat} C_{ox} (V_G - V_{th})^2 \quad \text{and} \qquad (3.3)$$

$$g_m = \frac{W}{L} \mu_{sat} C_{ox} (V_G - V_{th}) = \sqrt{2 \frac{W}{L} \mu_{sat} C_{ox} I_D}, \qquad (3.4)$$

where, μ_{sat} is the carrier mobility in saturation regime. In ideal case, drain current does not increase with increasing drain bias. As channel length scaled down, many parasitic factors result in additional effects which make simple long channel current-voltage model invalid.

3.2.3 Transfer characteristics: Threshold Voltage and Subthreshold Swing

I_D-V_G curve called transfer characteristic is one of the most basic but important properties. From transfer characteristics, many important FET parameters such as threshold voltage, subthreshold swing, drain-induced barrier lowering and mobility can be calculated.

3.2.3.1 Threshold Voltage

Threshold voltage V_{th} is an important FET parameter for the purpose of circuit design. It can be used to extract the other parameters such as channel length / width and series resistance etc. Various definitions exist for V_{th} because transfer characteristic near V_{th} is nonlinear due to sub-threshold current. At high V_G, I_D-V_G curve also can deviate from a straight line because of series resistance and mobility degradation effects.

Linear extrapolation is a common V_{th} extraction method [2]. After finding the point of maximum slope on the I_D-V_G curve from the maximum value of transconductance, linear extrapolation to I_D=0 is carried out from linear fitting to I_D-V_G curve at that point. This method is sensitive to series resistance and mobility degradation because linearity of I_D-V_G can be strongly affected [3, 4].

V_{th} can be calculated in the saturation regime. Taking the square root of both sides, Eq. 3.3 can be changed as:

$$\sqrt{I_D} = \sqrt{\frac{W}{2L}\mu_{sat} C_{ox}}\,(V_G - V_{th})\ . \tag{3.5}$$

With a plot of Eq. 3.5 as a function of V_G, intercept of x-axis (V_G) is V_{th}. For short channel, when I_D is limited by carrier velocity saturation, V_{th} can be easily extrapolated from Eq. 1.11. However, V_{th} is usually extracted from the I_D-V_G curve in linear regime to minimize additional effects induced by high lateral electric field (high V_D). As we discussed in chapter

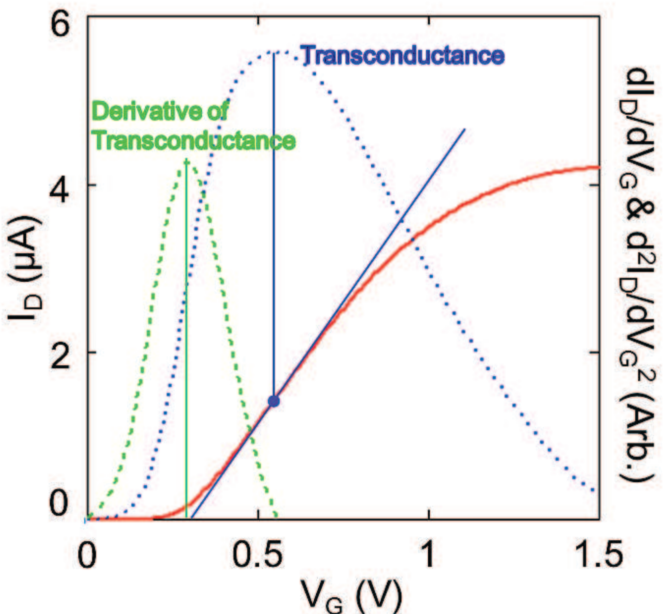

Figure 3.2 V_{th} determination by linear extrapolation method (blue, V_{th}=0.294 V) and transconductance derivative method (green V_{th}=0.28 V). Data was measured at V_D=10 mV.

1.3.4, device performance can be seriously degraded from hot carrier effects.

Transconductance derivative method uses second derivative of I_D-V_G characteristic at low V_D. It is from the ideal MOSFET model, which I_D is 0 at V_G below V_{th} and I_D is proportional at V_G above V_{th} (Eq. 3.1). In this model, the first derivative dI_D / dV_G is a step function so that the second derivative of I_D-V_G is delta function which has infinite value at V_G=V_{th}. Of course, in practical case, the maximum of second derivative value is not infinite. However, it can be available because it is less affected by series resistance and mobility degradation [2, 5].

Besides these methods, there are **constant current method**; if I_D is above setting certain threshold current I_{th} with V_G increase, V_G=V_{th}) and **subthreshold drain current**; using linearity of subthreshold current in the semi-log plot of I_D-V_G, etc.[2] .

3.2.3.2 Subthreshold Swing

The subthreshold swing (SS) is a feature of a current-voltage characteristic in FET. In ideal MOSFET model, drain current is 0 below V_{th}. However, in real device, diode like drain current behavior is observed in subthreshold region. Due to the exponential behavior of subthreshold drain current, it has linearity in the semi-log plot of transfer characteristics.

From the reciprocal semi-log slope of subthreshold drain current, SS can be defined as:

$$SS = \frac{dV_G}{d\log_{10} I_D} = 2.3\left(\frac{dV_G}{d\ln I_D}\right) \quad \text{(V/decade)}. \qquad (3.6)$$

From diode like behavior, subthreshold drain current can be expressed as:

$$I_{DsubV_{th}} = I_0 \exp\left(\frac{q(V_G - V_{th})}{nK_BT}\right)\left(1 - \exp\left(-\frac{qV_D}{K_BT}\right)\right). \tag{3.7}$$

I_0 depends on temperature, device dimension and doping concentration etc. n is related to the ideality of capacitive coupling between the gate stack interfaces. When the interface trap density exists n is:

$$n = 1 + \frac{C_{it}}{C_{ox}} + \frac{C_d}{C_{ox}}, \tag{3.8}$$

where C_{it} is the surface state capacitance and C_d depletion layer capacitance [6]. In the case of FD SOI wafer, C_d becomes 0 because depletion charge Q_d is constant as a function of voltage bias (C=dQ/dV). Using Eq. 3.6 and Eq. 3.7, SS can be approximated as:

$$SS \approx 2.3\frac{K_BT}{q}n. \tag{3.9}$$

K_BT/q is thermal voltage known as 0.02586 mV at room temperature.

For a device to have good turn-on characteristics, SS should be as small as possible; steeper slope has better gate control decreases SS. At room temperature, the minimum value of SS is 60 mV/decade.

The interface trap density D_{it} can be also optained as :

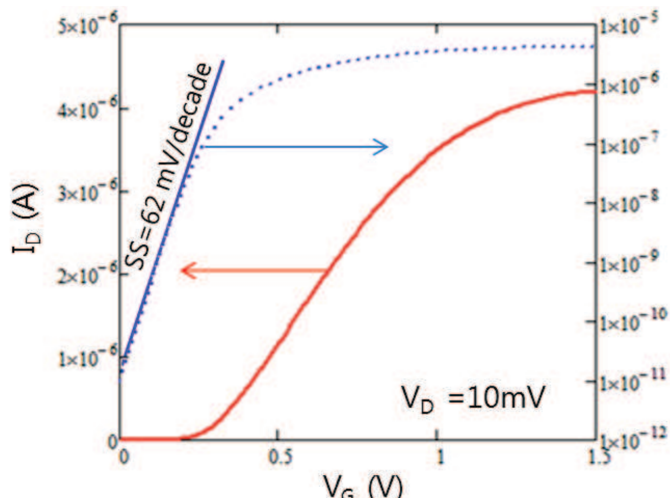

Figure 3.3 : FinFET subthreshold characteristic (Wfin=250 nm and L=1 μm).

$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{q\,SS}{2.3K_BT} - 1\right) - \frac{C_d}{q^2} \ (\text{cm}^{-2}\text{eV}^{-1}). \tag{3.10}$$

For the calculation of D_{it}, accurate value of C_{ox} and C_d is required.

3.2.4 Mobility

Carrier mobility represents how quickly carriers can move in the material. When an electric field E is given across the material, carriers drift with random motion. Due to the randomness, an average velocity named drift velocity v is used for the ensemble movement of a carrier in certain condition. v is proportional to E below velocity saturation;

$$v = \mu \cdot E, \tag{3.11}$$

where μ is the carrier mobility.

3.2.4.1 Carrier Scattering

During transport, carriers lose their energy and momentum as a result of various scattering process. There are many scattering sources including lattice vibrations (phonon), impurity ions, other carriers and surface roughness etc. [7].

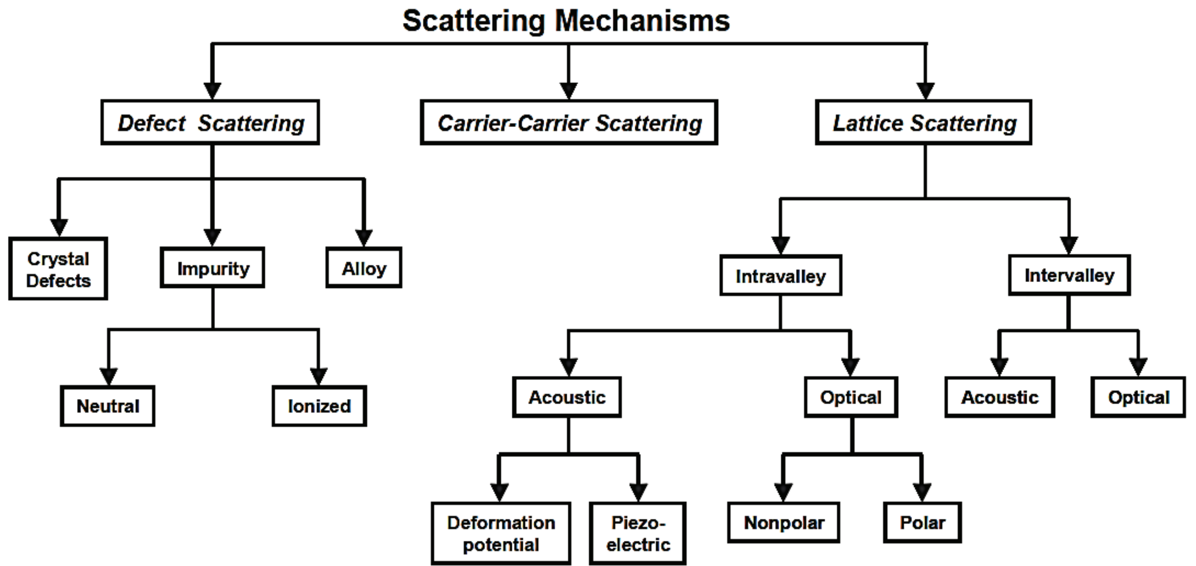

Figure 3.4 : Scattering mechanism in typical semiconductors [7].

Various scattering mechanism can be classified as shown in Fig.3.4. To analyze the mobility characteristics, the important scattering mechanisms need to be identified for the particular device conditions. Defect scattering includes scattering limited by both ionized and neutral impurities and by crystal defects. Carriers are scattered when they encounter the

electric field induced by ionized impurity. Phonon scattering is induced by the deformation potential in covalent semiconductors and by both the deformation potential and by polar interactions in ionic semiconductors [8]. Carrier-carrier scattering occurs by both binary collisions and interactions with the carrier plasma. Free carriers can also affect the other scattering process by screening the perturbing potential [8]. For the high quality, intrinsic and crystalline semiconductors, defect scattering and carrier-carrier scattering scarcely limit carrier transport. In polar semiconductors, carrier transport can be affected by free carrier plasma oscillations coupled by longitudinal optical phonons. As we will see in chapter 4.2.1, intervalley scattering also limit effective carrier mobility. Si consists of several valleys. When a carrier moves from a given valley to one on the opposite side of the same axis, it is called as 'g-type' process. Carrier transport to one of remaining valleys on the same side is also possible, which is named as 'f-type' process. Both intervalley scatterings affect the energy and momentum of carrier [8].

3.2.4.2 Mobility in MOSFET

According to Matthiessen's rule, more than one source of scattering mechanism can be merged as:

$$\frac{1}{\mu}=\frac{1}{\mu_1}+\frac{1}{\mu_2}+\frac{1}{\mu_3}+\ldots, \tag{3.12}$$

where μ_1, μ_2 and μ_3 are mobilities limited by different scattering mechanisms such as phonon or Coulomb etc. Similar to Eq. 3.12, relaxation time of scattering can be expressed as:

$$\frac{1}{\tau}=\frac{1}{\tau_1}+\frac{1}{\tau_2}+\frac{1}{\tau_3}+\ldots \quad . \tag{3.13}$$

τ is average of scattering time and τ_1, τ_2, τ_3 are scattering relaxation times from different scattering mechanisms. In Eq. 3.12 and Eq. 3.13, the smallest scattering mechanism is dominant in the total mobility behavior.

Because each mobility source has different temperature dependences, it can be separated by low temperature measurement. Jeon et al. and Takagi et al. showed the temperature dependence of each scattering mechanism using experimental mobility analysis [9, 10].

At low temperature, the lattice scattering is reduced by phonon freezing;

$$\mu_{ph} \propto T^{-n} N_S^{-1/\gamma}, \qquad (3.14)$$

where T is a temperature, N_S surface charge density and n and γ fitting parameters. Fitting parameter n and γ depends on crystallographic orientation of surface (n is 1~1.5 and γ is 3~6 in Si) [9]. Due to the reduced scattering, mobility limited by phonon scattering increases as temperature goes down.

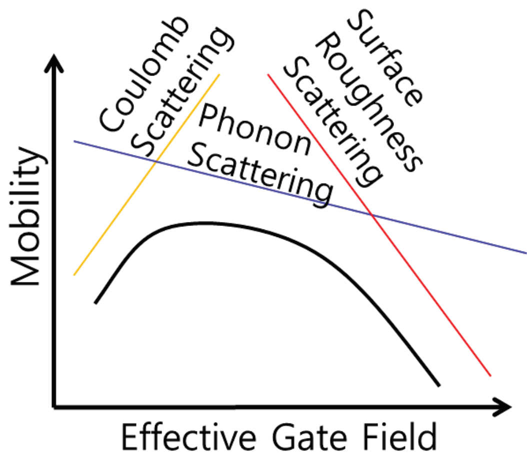

Figure 3.5 : Schematic of Matthiessen's rule and effective gate field (or carrier density).

Coulomb (ionized impurity) scattering has completely different behavior comparing to phonon scattering;

$$\mu_{Coulomb} \propto T N_S^{-\chi}, \qquad (3.15)$$

where χ is empirical fitting parameter which has positive values and changes depending on materials [9]. Lowering temperature makes the thermal motion of carriers slower. Because slow movements of carrier are likely to be scattered strongly by the interaction with a charged ion and carrier, impurity scattering decreases carrier mobility with decreasing temperature.

For the surface roughness scattering and non-ionized impurity scattering, there are no temperature dependences. However in the case of surface roughness scattering, it has power of -2 dependence as a function of effective gate field [11].

Using temperature dependent mobility analysis, dominant scattering mechanism in the carrier transport can be evaluated. For the device performance optimization, this is very important. As device scaled down, dopant fluctuation and surface roughness of the channel structure are much more effective in the device performance. Thus exact diagnosis of scattering mechanism should be carried out with certain devices.

When the given E in the channel exceeds a certain critical value, the mechanism of current saturation changes from channel pinch-off to velocity saturation [1]. As we discussed in chapter 1.3.2, the saturation current is proportional to v_{sat} instead of μ_{eff}. In ultra-short channel devices, this will be more complicated by absence of equilibrium transport. Therefore, mobility is usually extracted in the linear regime with small V_D (normally V_D=10 mV or 50

mV which is about tens ~ hundreds times smaller than maximum V_G).

There are several mobilities in use. However, in MOSFET modeling, three mobilities are widely used for transport analysis.

Field effect mobility μ_{fe} is derived from the transconductance;

$$g_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D=const.}, \tag{3.16}$$

From the relationship of Eq. 3.2, μ_{fe} can be expressed as;

$$\mu_{fe} = \frac{L g_m}{W C_{ox} V_D}. \tag{3.16}$$

Field effect mobility is easy to calculate but it is not valid below threshold voltages ($\mu_{fe} \rightarrow 0$).

Effective mobility μ_{eff} uses drain conductance. From drift-diffusion current, I_D can be;

$$I_D = \frac{\mu_{eff} W Q_n V_D}{L} + \mu_{eff} W \frac{K_B T}{q} \frac{d Q_n}{d x}, \tag{3.17}$$

where Q_n is the mobile channel charge density. If V_D is low enough, the diffusion term of Eq. 3.17 goes 0 because the channel charge becomes more uniform from source to drain. Thus, the first term of Eq. 3.17 remains and μ_{eff} can be estimated as;

$$\mu_{eff} = \frac{L g_d}{W Q_n}, \tag{3.18}$$

and the drain conductance g_d is defined as;

$$g_d = \left.\frac{\partial I_D}{\partial V_D}\right|_{V_G=const.}. \tag{3.19}$$

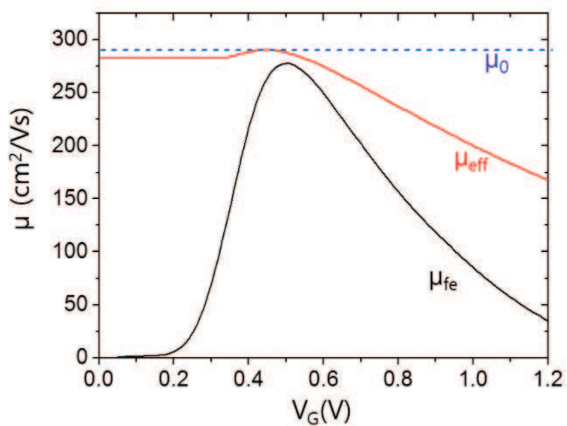

Figure 3.6 : Comparison of different mobilities in FinFET (L=1 μm, W_{fin}=5 nm).

For the calculation of μ_{eff}, Q_n should be defined properly. As a simple approximation, the relationship of $Q_n = C_{ox}(V_G - V_{th})$ is available. Even though the subthreshold channel charge exists, it is available in the strong inversion region due to the term of ($V_G - V_{th}$). Especially, due to the non-linear drain current near V_{th},

μ_{eff} dramatically fall down around V_G=V_{th} [2]. Gate capacitance measurement gives more accurate information of Q_n. Capacitance measurement for the effective mobility will be discussed in chapter 3.3.4.

Because μ_{eff} has the consideration of gate effective field, normally it has higher value than μ_{fe}. If μ_{fe} is used in device modeling, the current and device switching speed will be underestimated.

Low field mobility μ_0 represents the intrinsic carrier mobility. It is upper limits of carrier mobility in a given device structure. Because μ_0 should be considered in low field behavior (relatively small V_G), it is mainly affected by Coulomb scattering and lattice scattering. The calculation of μ_0 will be discussed in chapter 3.3.

3.2.4.3 Other mobilities

Apart from mobilities discussed in chapter 3.2.4.2, there are other important mobility considerations.

Hall mobility is used for the characterization of intrinsic mobility, carrier density and resistivity in certain material. When a magnetic field B is applied perpendicular to the transport direction, the Lorentz force makes electric field and carrier movement shifted according to Fleming's right hand rule. As a result, there is a potential difference called Hall voltage V_H across the sample. Hall mobility is defined as;

$$\mu_H = \frac{|R_H|}{\rho}, \qquad \text{with} \tag{3.20}$$

$$R_H = \frac{dV_H}{BI}. \tag{3.21}$$

Weakness of Hall mobility measurement is that the special sample structure is required [2]. Typical Hall effect measurement needs more than for contacts which called Hall bar. This measurement requires long sample length but short sample width. Thus, conventional MOSFET structure is not proper to Hall effect measurement.

Magnetoresistance mobility can escape from the limitation of complicate sample structure. In the short and very wide sample geometry, Hall potential can be negligible. With a cylindrical symmetry structure called Corbino geometry, Hall potential is so balanced that

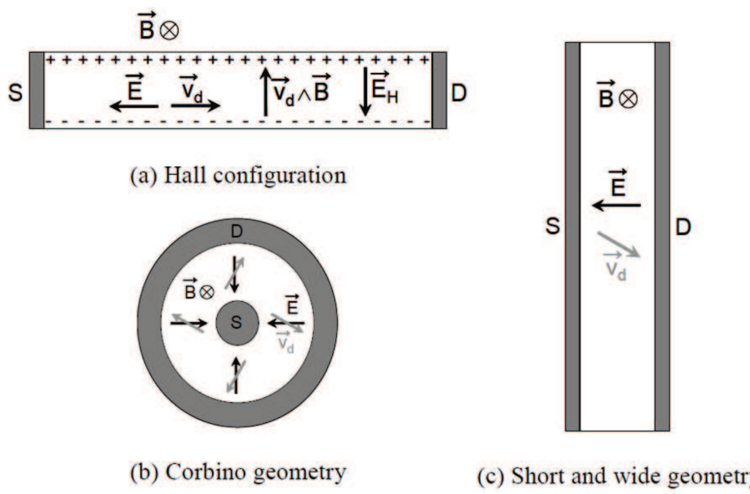

Figure 3.7 : Device geometry configurations for Hall effect (a) and transverse geometric magnetoresistance (b and c) [1].

there is no Hall potential.

Resistivity increases when the sample locates in a magnetic field. This is the physical Magnetoresistance effect (PMR) with the anisotropic conduction, bipolar carrier conduction and energy dependent carrier scattering [2].

Resistance is also increased by magnetic field due to the deviation from the straight line of carrier transport path. This effect named as the geometrical magnetoresistance (GMR) depends on the sample geometry.

Magnetoresistance mobility is estimated as following relationship [1]:

$$\frac{\rho_{(B)} - \rho_{(0)}}{\rho_{(0)}} = \mu_{MR}^2 \cdot B^2 . \tag{3.22}$$

3.2.5 Low Frequency Noise

In device performance, noise is a kind of inevitable elements. On the view point of device operation, noise has to be avoided factor. However, for the device qualification, it can be a useful tool.

There are lots of noise origins. In this chapter, several low frequency noise characteristics will be investigated.

Thermal noise is the most common noise. It is generated by the thermal motion of carriers. Thermal noise is constantly spread throughout the frequency spectrum. Therefore it is called as 'white noise'. Thermal noise caused by Brownian motion of carriers depending on temperature. Thus, even in the absence of a current, thermal noise exist in the device. Thermal noise is given by:

$$S_V = 4K_B T R \quad (\text{or} \quad S_I = \frac{4K_B T}{R}), \tag{3.23}$$

where R is the resistance.

Shot noise occurs when the current flowing across a potential barrier, such as P-N junction, is discontinuous owing to the discrete nature of charge carriers. PSD of shot noise is:

$$S_I = 2qI. \tag{3.24}$$

Shot noise is smaller than thermal noise at room temperature. It is observed at low temperature.

Generation-recombination (GR) noise is induced from trapping / detrapping of carriers during transport. Randomly captured charge can locally fluctuate the carrier mobility, diffusion coefficient, electric field, barrier height and depletion width etc. There are four GR noise origins; 1) free electron – free hole recombination, 2) free electron – free hole generation, 3) electron trapping / detrapping in trap site and 4) hole trapping detrapping in trap site.

PSD of the carrier number fluctuation in GR noise follows as:

$$S_N(f) = \frac{4\left\langle \Delta N_{trap}^2 \right\rangle \tau}{1 + (2\pi \tau f)^2}. \tag{3.24}$$

where $\langle \Delta N_{trap}^2 \rangle$ is the variance of the total number of the interface trap charges and τ the trapping time constant. The interface traps obeying the Poisson's distribution of which the variance is simply equal to the mean value of the total number of the interface trap charge.

Random telegraph signal (RTS) noise is a special case of GR noise. If the number of traps is small, GR noise can be displayed as RTS noise. It has several quantized switching events in time domain. RTS noise is sensitive to bottlenecks of carrier transport (poor contact) and interface states [12].

1/f noise is the common name for the noise described as:

$$S_I = \frac{K I^{\beta}}{f^{\gamma}}, \tag{3.24}$$

where K is a constant and β / γ the current / frequency exponents. 1/f noise is observed in the

low frequency region (less than 10^5 Hz). 1/f noise is mainly interpreted by the carrier number fluctuation (CNF) model and Hooge mobility fluctuation (HMF) model.

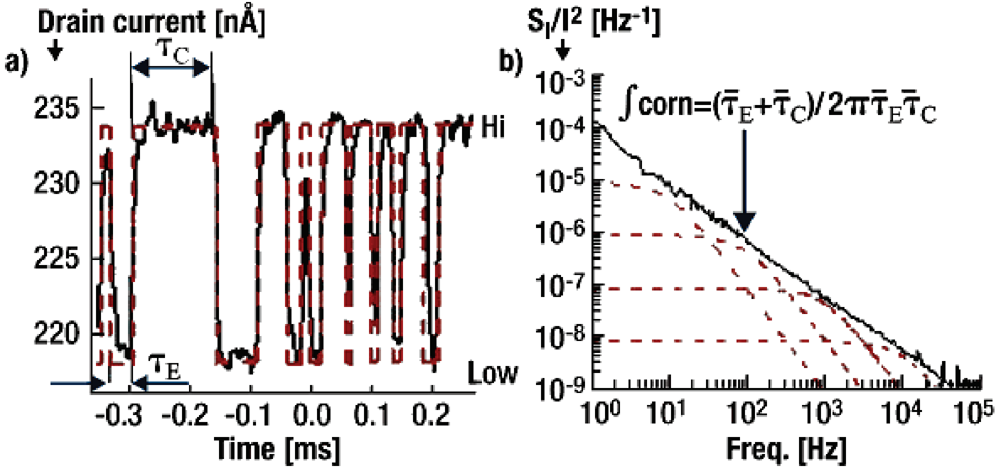

Figure 3.8 : a) Typical two-level RTS signal in a high-*k* MOSFET. b) Schematic noise power density spectra: two-level RTS signal described by a Lorentzian function (dashed line) with its corner frequency, f_{corn}, determined by the average capture and emission times of the trap; superimposition of multiple Lorentzians in a large area device form a 1/f spectrum (solid line). τ_e and τ_c stands for the emission and capture time in the trapping event [12].

CNF model is caused by trapping / detrapping of carrier near the gate oxide / semiconductor channel interface. Due to the carrier number fluctuation by trapping / detrapping, the flat band voltage and current are locally modulated [13]. CNF model can be combined with the correlated mobility fluctuation model (CMF). CNF+CMF model can be described with the normalized drain current noise;

$$\frac{S_{I_D}}{I_D^2} = \left(1 + \alpha\, \mu_{eff}\, C_{ox} \frac{I_D}{g_m}\right) \cdot S_{Vfb} \cdot \left(\frac{g_m}{I_D}\right)^2, \tag{3.25}$$

where α is the Coulomb scattering parameter (V s/C) and S_{Vfb} the flat band voltage PSD. S_{Vfb} is related with the charge fluctuation near interface, which is given as:

$$S_{Vfb} = \frac{q^2 K_B T \lambda N_t}{f W L C_{ox}^2}, \tag{3.26}$$

where λ is the oxide tunneling distance, N_t the volume trap density. CNF model is sensitive to the quality of gate oxide / semiconductor channel interface.

HMF model is originated from the carrier mobility fluctuation induced by phonon scattering.

It is described as [13]:

$$\frac{S_{I_D}}{I_D^2} = \frac{q\alpha_H}{WLQ_i f} \approx \frac{1}{I_D}, \tag{3.26}$$

with α_H is the phenomenological parameter named as Hooge parameter, Q_i the inversion charge density per unit area. Typically, α_H has the range of 10^{-3}~10^{-6} [13].

3.3 Characterization and Parameter Extraction Technique

In chapter 3.3 various parameter extraction techniques will be investigated. Due to the device scaling down, subtle difference between geometrical parameters and physical parameters cannot be negligible. For example, effective channel length and width is different not only from mask design, but also from the physical geometry due to the short channel effect. Mobility attenuation factors can be varied because of surface roughness and impurity fluctuation in small dimension. Thus, proper parameter extraction technique is necessary for the research of advanced device structure.

3.3.1 Series Resistance

In linear regime, FET operates as a gate controlled resistor. The resistance of FET consists of source resistance R_S, channel resistance R_{ch} and drain resistance R_D. As shown in Fig. 3.9, R_S and R_D restrict I_D. Total series resistance R_{SD} can be representative as a superposition of R_S and R_D. R_{SD} is originated from the source and drain contact resistance, the sheet resistance of source and drain and the spreading resistance at the transition from the source diffusion to channel etc. [2]. As device dimension reduced like FinFET and nanowire FET, bottleneck of carrier transport between low dimensional channel and source (or drain) also induce resistance. With the consideration of R_{SD}, total drain conductance g_d can be written as:

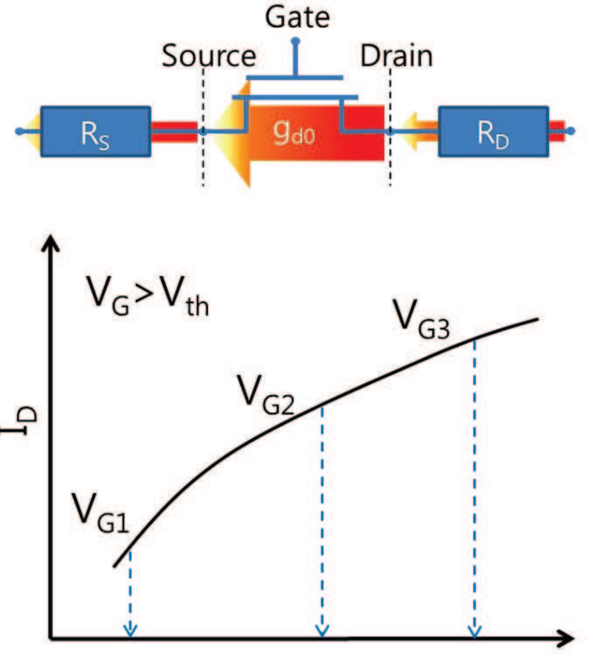

Figure 3.9 : Schematic of series resistance (above) and Hamer's fitting method for parameter extraction.

$$g_d = \frac{1}{R_{SD} + (1/g_{d0})} = \frac{g_{d0}}{1 + R_{SD} g_{d0}}, \quad (3.27)$$

where g_{d0} is the channel conductance. Combining Eq. 3.17 with low field mobility μ_0, g_{d0} can be calculated as:

$$g_{d0} = \frac{\mu_0 W Q_n}{L}, \quad (3.28)$$

Finally, we can achieve I_D considering R_{SD} as:

$$I_D = G_m \frac{V_G - V_{th}}{1 + \theta(V_G - V_{th})} V_D, \quad (3.29)$$

where the mobility attenuation factor θ is $\theta = \theta_0 + G_m R_{SD}$ and G_m the low field transconductance parameter;

$$G_m = \frac{\mu_0 W C_{ox}}{L}. \quad (3.30)$$

For Eq.3.29, Q_n is approximated as $C_{ox}(V_G - V_{th})$. Because there are three unknown variables (G_m, θ and V_{th}), solving three equations (Eq. 3.29) at three different V_G can give the values of unknown parameters as shown in Fig. 3.9. From the linearity of θ, the total series resistance R_{SD} can be extracted [14].

3.3.2 Effective Channel Geometry

As discussed before, the effective channel length becomes more different from the mask defined gate length and physical (geometrical) gate length of device in short channel device. It is from the source and drain junction encroachment under the gate [15]. In highly doped source and drain with steep gradient of doping concentration, the effective channel length is almost same as the physical length. However in lightly doped drain (LDD), the effective channel length is larger than the space between source and drain [2]. Moreover, the effective channel length can be more expended by high gate bias [9, 16]. For the proper device modeling, the effective channel length should be defined. The effective channel length can be

extracted from the capacitance, resistance and transconductance etc. as a function of the mask defined gate length. Linear intercept of x-axis (gate length) represent the difference between mask defined gate length and the effective channel length. As an example, Fig. 3.10 shows the effective channel length extraction with total resistance [16].

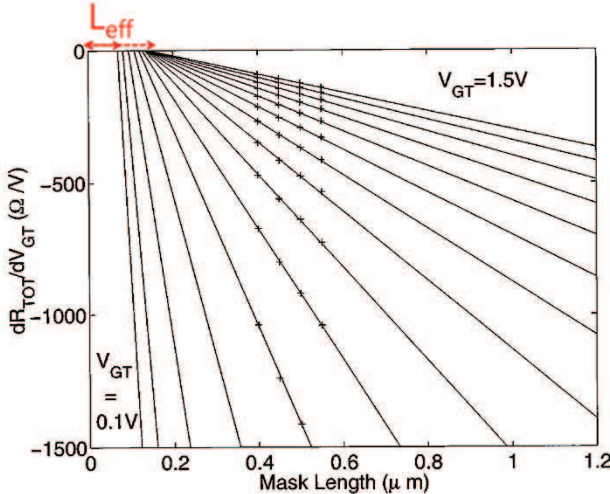

Figure 3.10 : Effective channel length extraction using the derivation of total resistance as a function of gate bias in linear regime [16]. For different V_G ranging from 0.1 to 1.5 V in steps of 0.1 V. V_D = 50 mV.

For the characterization of ultra-short channel device, the effective channel length should be estimated to the exact device modeling.

3.3.3 Y-function Method

Y-function method is a MOSFET parameter extraction technique [17]. Relying on drain current and transconductance transfer characteristics, V_{th}, μ_0 and θ can be extracted.

As we discussed in chapter 3.3.1, series resistance affects device transfer characteristics which makes parameter extraction difficult. Principle of Y-function method is the elimination of series resistance in transfer characteristic model. From Eq. 3.29 and Eq. 3.30, transconductance g_m of MOSFET is:

$$g_m = \frac{W}{L} C_{ox} \frac{\mu_0}{\left(1+\theta\left(V_G - V_{th}\right)\right)^2} V_D . \quad (3.31)$$

Eq. 3.29 and Eq.3.30 has mobility attenuation factor θ. Dividing I_D by square root of g_m eliminates θ;

$$\frac{I_D}{\sqrt{g_m}} = \left(\frac{W}{L} C_{ox} \mu_0 V_D\right)^{1/2} \left(V_G - V_{th}\right). \quad (3.32)$$

According to the linearity of Eq. 3.32, the intercept of x-axis is V_{th}. From the slope of Eq. 3.32, μ_0 can be obtained. Using the transconductance parameter G_m, R_{SD} and L_{eff} also can be estimated.

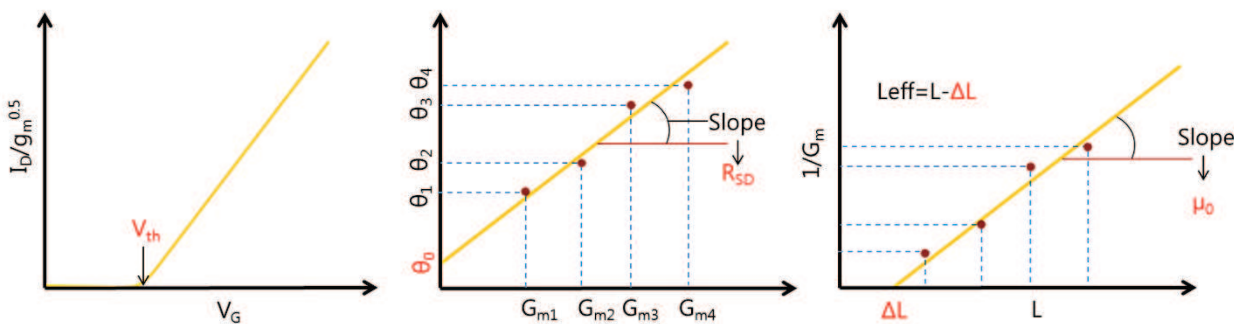

Figure 3.11 : Schematics of parameter extraction. μ_0, θ_0, R_{SD}, L_{eff} can be extracted using linearity of θ - G_m and $1/G_m$ - L plot.

If the device has very low dimensional channel, additional effect such as surface roughness scattering break the linearity of Y-function due to the second order mobility attenuation factor θ_2 [5, 11, 18]. In this case, the model of effective mobility μ_{eff} is changed from:

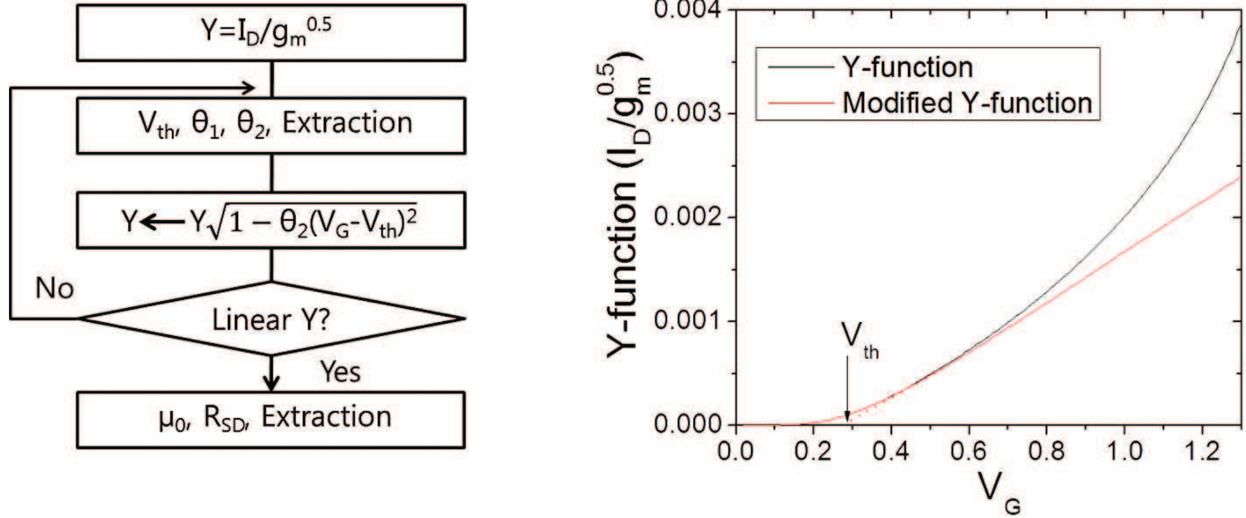

Figure 3.12 : Flow chart of modified Y-function (left) and application to the experimental data (right). Bent Y-function curve become linear after modification.

$$\mu_{eff} = \frac{\mu_0}{1+\theta(V_G - V_{th})} \quad \text{to} \tag{3.33}$$

$$\mu_{eff} = \frac{\mu_0}{1+\theta_1(V_G - V_{th})+\theta_2(V_G - V_{th})^2}, \tag{3.34}$$

where θ_1 and θ_2 are 1st and 2nd order mobility attenuation factor. θ_1 describes impurity scattering and lattice scattering and θ_2 describes surface roughness scattering phenomena.

As shown method in Fig. 3.12, non-linear Y-function can be modified using iteration technique [19]. After making Y-function linear, effective values of V_{th}, R_{SD}, $\mu 0$, θ_1 and θ_2 can be extracted by the methods explained previously.

3.3.4 Split C-V

The capacitance-voltage (C-V) characteristic is one of the important electrical properties. It includes the information of charge in the device. C-V characteristics can be measured using quasi-static C-V or split C-V technique. The difference between two methods is in the applied test frequency.

In quasi-static C-V measurement, test frequency is very low and can be regarded as quasi DC signal. In the case of device which has slow charge response, quasi-static C-V method is useful to characterize its low mobility charge behavior.

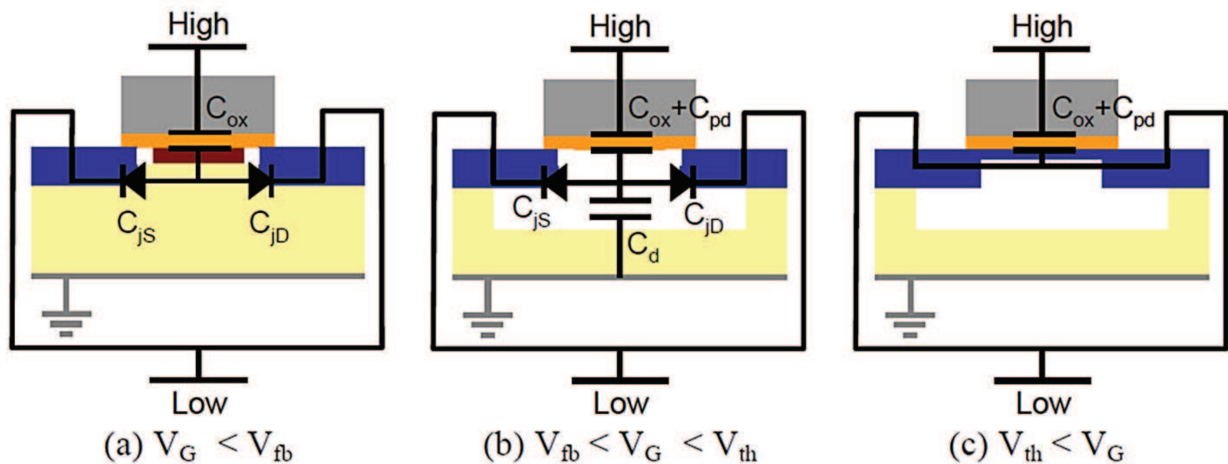

Figure 3.13 : Equivalent circuit for C_{GC} measurement in (a) accumulation, (b) depletion, (c) inversion regime [1].

The split C-V measurement has been developed to study interface states in weal inversion and mobility extraction. It measure capacitance between the gate and source-drain C_{GC} and the capacitance between the gate and the substrate C_{GB}.

C_{GC} can be estimated by measuring AC current on the source and drain. AC input voltage is applied on the gate electrode as shown in Fig 3.13. The inversion charge is obtained by integration of C_{GC} as a function of V_G.

As we discussed in 3.2.4.2 and 3.3.2, effective mobility and effective channel length can be extracted using C_{GC}. For Eq. 3.18, Q_n is

$$Q_n(V_G) = \int_{V_{ACC}}^{V_G} \frac{C_{GC}(V)}{WL_{eff}} dV , \tag{3.35}$$

where V_{ACC} is a gate bias at accumulation region.

In highly scaled devices, the split C-V method has problem induced by parasitic capacitance. For the exact measurement of C_{GC}, effective gate length should be estimated before. Then, under the assumption that C_{GC} is independent of effective channel length, intrinsic capacitance per unit of gate length can be obtained [1]. The difference of gate length should be enough but not too much because too much gate length difference can induce V_{th} mismatch. From this, parasitic capacitance can be eliminated.

3.4 Conclusion

As modern device structures are extremely scaled down, device characterization and exact parameter extraction become more and more important.

Various device characterization and parameter extraction methods have been investigated in this chapter. Based on the basic MOSFET characterization, the principles of threshold voltage, subthreshold swing and carrier mobility estimation have been introduced. For the low dimensional device structures, the series resistance, the mobility attenuation and the gate-channel capacitance characterization have also been studied.

In next chapter, the transport characterization in quasi-1D nanostructure FET is following.

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4. Transport of Quasi-1D nanostructure FET

4. Transport of Quasi-1D nanostructure FET

4.1 FinFET – Surface Roughness Scattering

4.1.1 FinFET overview

4.1.2 Experimental Conditions: Device Fabrication and Measurement

4.1.3 Threshold Voltage

4.1.4 Temperature Dependence of FinFET Effective Mobility

4.1.5 Quantification of the Surface Roughness Scattering Effect

4.1.6 Conclusion

4.2 SiGe Nanowire FET – Phonon Scattering and Impurity Scattering

4.2.1 Device overview: Strain Engineering

4.2.2 Experimental Conditions: Device Fabrication and Measurement

4.2.3 Short Channel Effects in SiGe Nanowire FET

4.2.4 Analysis of Transport Mechanism

4.2.4.1 Temperature Dependence of Effective Mobility in SiGe NW FETs

4.2.4.2 Temperature Dependence of Low-field Mobility in SiGe NW FETs

4.2.4.3 Respective Contribution of Scattering Mechanism

4.2.4.4 Role of Strain: Boron Out-diffusion from S/D Regions

4.2.5 Conclusion

4.3 Junctionless Transistor

– Volume Conduction and Reduced Short Channel Effects

4.3.1 Device Overview

4.3.1.1 Junction Gate Field Effect Transistor (JFET)

4.3.1.2 Junctionless Nanowire FET

4.3.2 Transport of Junctionless Transistor

4.3.3 Conclusion

4.4 Si Nanowire Sensor

– Low Frequency Noise and Sensing Limitation

4.4.1 Overview: Nanowire for Sensor Application

4.4.2 Simulation Environment and Conditions.

4.4.3 Sensitivity Estimation: Numerical Simulation and Analytical Model

4.4.4 Low Frequency Noise in Nanowire Sensor

4.4.5 Conclusion

Chapter 4

Transport of Quasi-1D nanostructure FET

4.1 FinFET – Surface Roughness Scattering

4.1.1 FinFET overview

In order to overcome the short channel effects induced by scaling down, the first improvement consists in reducing body thickness, using fully depleted SOI devices. Multiple gate operation still enhances gate control and allows loosening the constraints on oxide and body thicknesses [1, 2]. To this end, FinFET architecture has been proposed in this respect. The term of FinFET was used to describe a non-planar double gate FET based on the earlier fully depleted lean-channel transistor (DELTA) [5]. Depending on the authors, it can be called tri-gate or omega-gate etc. but in this paper all of fin-based transistor will be defined as FinFET. The FinFET has the advantages of featuring no buried electrode and of offering excellent robustness to short channel effects [6]. Fin width plays the same role as body thickness, and steep subthreshold slope, low body coefficient and high switching speed can be obtained, making this architecture very attractive for future technological nodes. However, the limitations of some specific fabrication modules such as fin patterning, gate stack or junction conformality are still an issue for technology optimization [7-10].

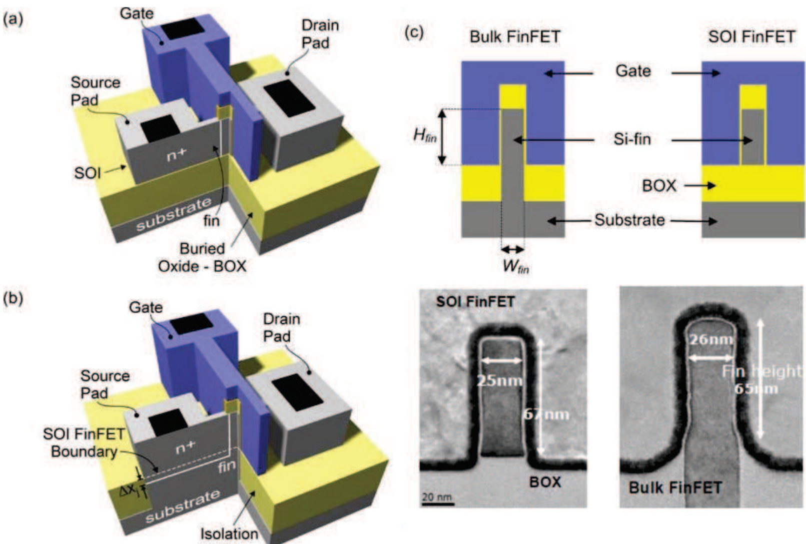


Figure 4.1.1 : SOI FinFET and bulk FinFET. Bird's eye view (a) SOI and (b) bulk FinFET. (c) Cross-sections [3, 4]

Currently FinFET has two trends which are 'Bulk FinFET' and 'SOI FinFET'. Bulk FinFET

use two schemes for the electrical isolation of each device, which are junction isolation and material isolation.

The junction isolated bulk FinFET uses a high dose junction implantation at the base of the fin. The junction barrier electrically isolates devices. In the case of material isolation, the grown oxide from the oxide trench isolation across the bottom of the fin similar to the local oxidation of silicon (LOCOS) process. Comparing to the SOI FinFET, the main advantage of bulk FinFET is that the bulk CMOS technology is available and the wafer cost is cheaper than SOI wafer. However the fabrication process of material isolated bulk FinFET has more complexity.

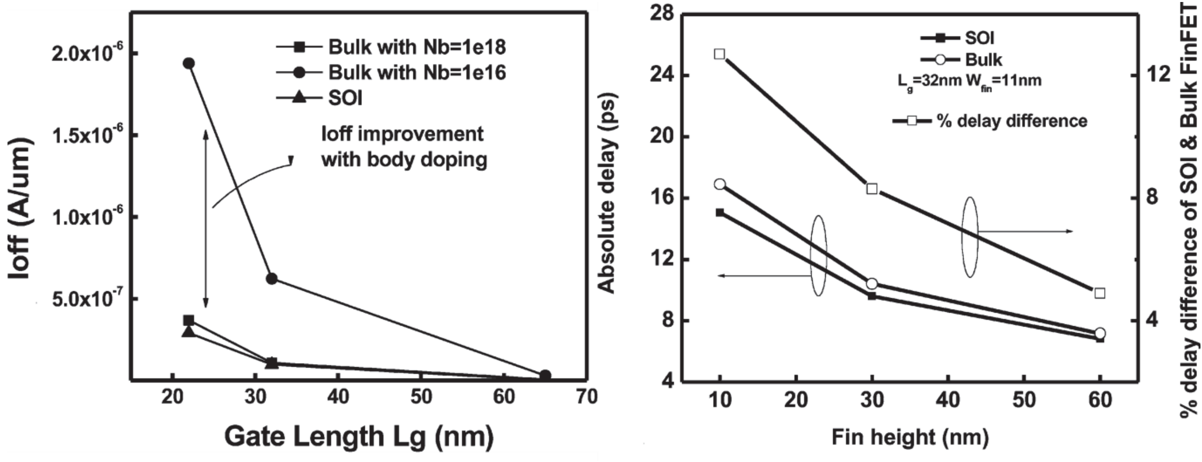


Figure 4.1.2 : Comparisons of leakage (left) and delay (right) [11].

The SOI FinFET is fabricated on the device layer of SOI wafer directly. Due to the BOX layer, it does not need to make additional isolation which means that the fabrication process is less complex than the bulk FinFET. The SOI FinFET has better performances comparing to the bulk FinFET. Gate leakage is smaller. AC performance is higher (smaller parasitic capacitance and smaller delay). However, these differences are just several percentages of themselves. For example, the parasitic capacitance of SOI is below 5~6 % less than the bulk [11]. As seen in Fig. 4.1.2, the height of fin affects the performance of FinFET. Thus the geometry optimization is necessary.

The cost of SOI wafer is approximately 4 times higher than bulk [12]. However the bulk FinFET needs 6~8 additional process step. Front-end-of-line (FEOL) process requires 140% higher cost in bulk FinFET [12]. Still the debate of wafer cost/process complexity is on-going. In the case of bulk FinFET, positioning of the junction. Because of the absence of BOX layer, source and drain junctions are deeper than the height of fin. It causes the degradation of short

channel effect control and the bulk punch-through

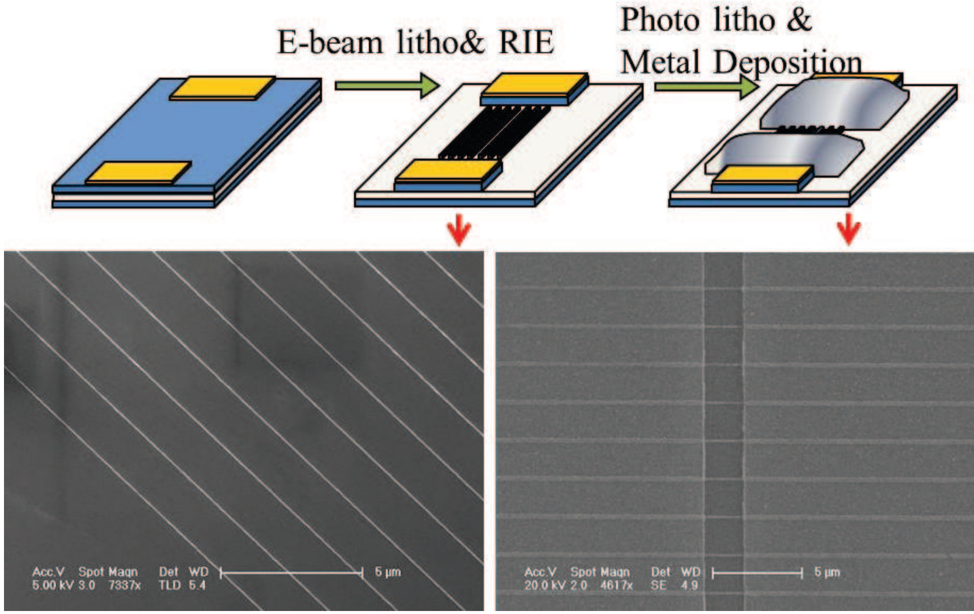
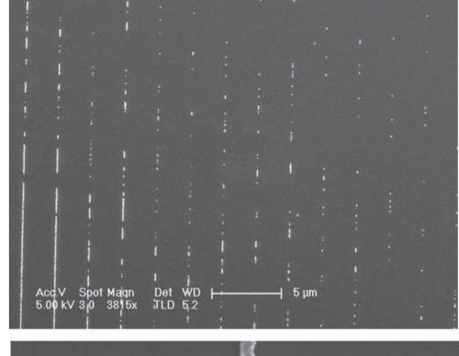


Figure 4.1.3 : Bottom gate FinFET fabricated by E-beam lithography. Fabrication process (top) and SEM images of each process (bottom).

Thus, halo implantation and channel doping is necessary [4]. However it increases the process complexity and the random doping fluctuation which reduce the benefit of the FinFET structure. For the mass production, the immersion lithography or the other advanced patterning technology such as spacer technology [13]. However, e-beam lithography is widely used in the academic research due to the fabrication cost. During this Ph.D. Study, most of FinFET experiments were carried out with the devices from the IMEC which are fabricated by immersion lithography. But some of FinFET were fabricated using e-beam lithography in Korean Research Institute of Standard and Science (KRISS). Fig 4.1.3 and 4.1.5 show the SEM images and DC characteristics of FinFET fabricated in KRISS. Using (100) p-type SOI wafer, simple e-beam lithography was carried out to make Cr metal mask. Using field emission scanning electron microscopy (FEI Sirion 400 FESEM) and Raith



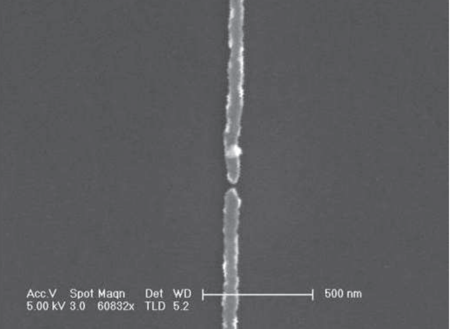


Figure 4.1.4 : Failed pattern due to the wrong e-beam lithography and etching conditions.

Elphy quantum software, 35 nm width line patterns were drawn on the spin coated PMMA C2 e-beam resist (ER). Thickness of ER was about 100nm and only line dose was used at 30KV. After e-beam lithography, 1:3 methylisobutylketone (MIBK) to isopropylalcohol (IPA) solution was used for the developer. 20 nm of Cr was deposited on the pattern using e-beam evaporator and lifted off in the PG remover. ICP-RIE was used to etch Si device layer of the SOI wafer. CF_4 100 sccm, Ar 50 sccm, 40 mTorr pressure, 500/50W ICP/Bais power and 120s etching time were used. Fin patterning is very sensitive with the fabrication conditions of e-beam lithography and ICP-RIE. Even with same conditions, if different instruments are used, the feature of fin pattern is completely changed. Thus well-defined fabrication condition is required.

After etching, Cr mask was etched by CR7-SK chrome etchant. Finally, photolithography process was carried out to make source, drain contact with Al. Due to the contact between Si channel and metal, fabricated device does not work properly. Thus rapid thermal annealing (RTA) process should be done during 5 minutes at 350 ˚C. Because it used only back gate with 200 nm BOX, the DC characteristics are not good enough to use the CMOS circuits. However, it can be good to apply for the sensor application in academic research.

The electrical or morphological interface quality of a FinFET related to the fin pattern and gate stack is one of the most important factors to optimize the device performance. For the sake of illustration, the numerical simulation of tri-gate fin architecture, similar to the experimental one is helpful as shown in Fig. 4.1.6. The concentration profiles across the fin, taken at half fin height, have been drawn as a function of gate bias for a 20 nm wide n-type FinFET (Fig. 4.1.6 (c)). As can be seen, most of the electrons concentrate near the surface of the fin structure. In the other words, the fin surface quality is a critical feature to enhance the mobility and, in turn, the current of FinFET device. However, in order to obtain a tight control of their geometry, the fins are normally patterned using RIE techniques, which are liable to induce some damages and increase surface roughness (SR)

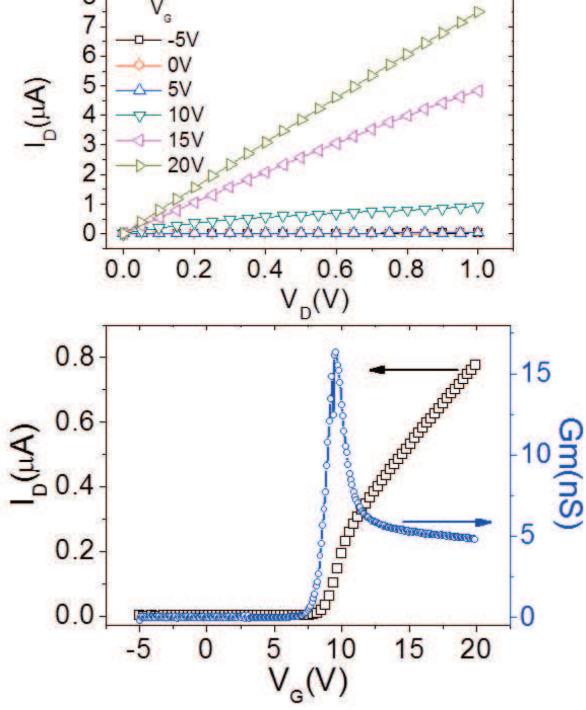


Figure 4.1.5 : DC characteristics of bottom gate FinFET fabricated by e-beam lithography.

at the sidewalls while the top surface is protected by the masking layer. Therefore, there is a risk that surface roughness scattering, which generally appears at high electron concentration, can limit the mobility and even decrease the drive current [14, 15]. Experimental techniques that allow quantification of the influence of SR in the fabricated device are therefore very important for technology optimization. Techniques that physically characterize interface roughness, using TEM or AFM, are destructive and cannot be used extensively for such a goal [16, 17]. Moreover, since the expected impact of roughness on device performance results from a degradation of transport properties, direct extraction from a mobility analysis brings more direct information for technology optimization.

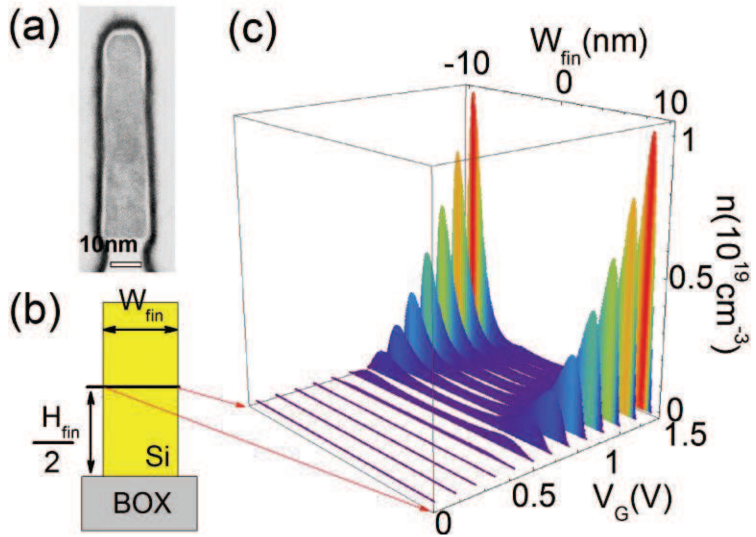


Figure 4.1.6 : (a) TEM cross-section of a 10 nm wide fin corresponding to the tri-gate FinFET technology characterized in this paper. Scale bar is 10 nm. (b) Cross-section of the tri-gate FinFET structure simulated for illustration. (c) Electron concentration, in linear scale, along a cross-section taken at half fin height for 20 nm fin width. The different curves correspond to increasing gate voltage. Most of the inversion charge lies very close to the interfaces.

In this chapter, the detail of an experimental method that provides a quantitative evaluation of surface roughness contribution will be shown. It is based on the detailed analysis of the static characteristics dependence with temperature and fin width.

Assuming that the only other scattering mechanism to be considered is phonon scattering, which can be considered as frozen at sufficiently low temperature, SR mobility is sometimes extracted as the low temperature mobility (30 K) [18]. Our method is rather exploiting a range of temperature (from 77 K to 350 K here) in order to identify the contributions of all the dominant scattering mechanisms. This technique has recently been demonstrated to allow quantitative extraction of SR mobility, with good correlation to the results of AFM studies, in NMOS transistors [19].

This technique is coupled with a decorrelation of sidewalls and top surface channels, based on the linear width dependence of drain current, and as function of temperature. This linear dependence has been shown to allow independent extraction of the sidewall and top interface mobility in tri-gate FinFETs at room temperature, using effective mobility extraction from I-

V curves associated to each type of channel [19, 20]. A similar dependence has been noticed for the gate to channel capacitance which is used for the alternative split C-V extraction of the mobility [21]. However, based on this, it could be concluded that the top surface contributed to less than 4% in their 10 nm fins and that it was therefore possible to use their narrower fins as good representative to extract sidewalls transport parameters. It was not used to decorrelate the two interfaces and no information was given about the transport properties for the top channel. In addition, the narrowest fins may be subject to coupling effects between the two facing sidewalls and may therefore not give a perfect image of sidewall conduction in wider fins. Particularly, the electrical or morphological interface quality related to the fin pattern and gate stack is one of the most important factors to optimize the device performance.

4.1.2 Experimental Conditions: Device Fabrication and Measurement

The FinFETs used in this study were fabricated on standard SOI wafers with 145 nm buried oxide thickness at IMEC (Leuven). The fabrication process has been described in [22]. It includes no intentional strain boosters. An undoped channel, with background boron doping of 10^{15} cm^{-3}, was used to avoid impurity scattering and to reach higher mobility. As a gate insulator, HfSiO was deposited by metal-organic chemical vapor deposition (MOCVD) with an equivalent gate oxide thickness of 1.7 nm.

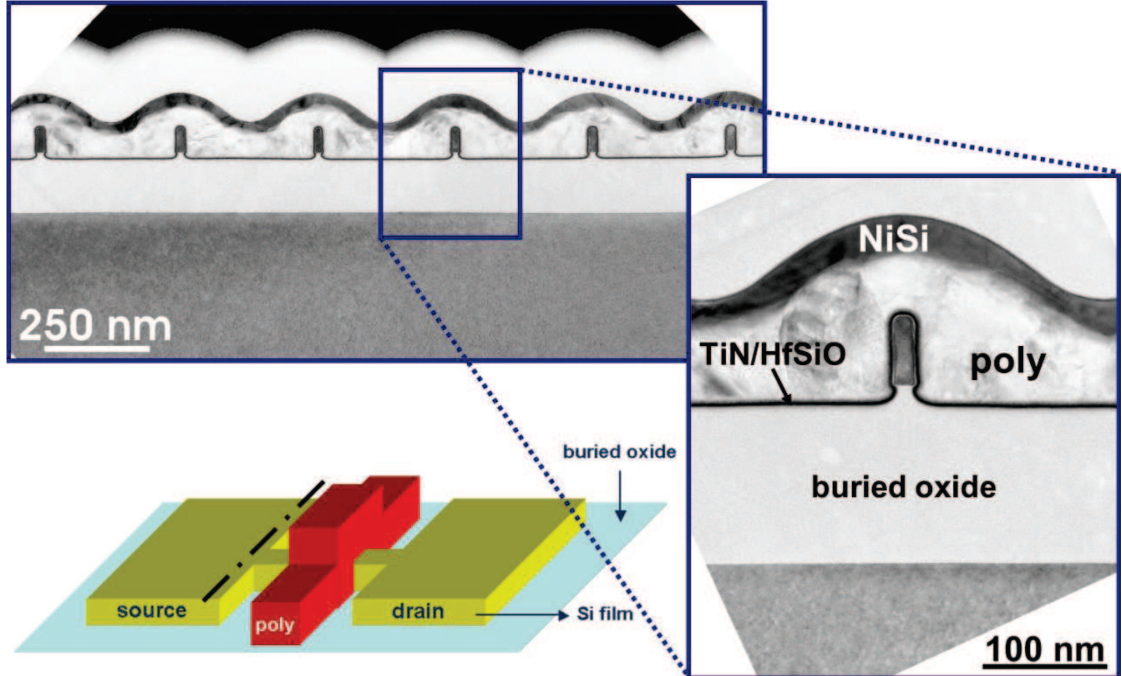


Figure 4.1.7 : Cross-section images of SOI FinFET. Devices are supported by IMEC.

For the gate metallization, TiN layer was deposited by physical vapor deposition (PVD). It was capped with a 100 nm polysilicon layer. The distance between the gate and the source/drain pads, heavily doped to about 2×10^{20} cm^{-3}, was 0.2 μm. The spacer width was about 50 nm with a doping concentration of 5×10^{19} cm^{-3}. The fin height H_{fin} was kept constant at 65 nm and the fin width W_{fin} was varied from 10 to 1000 nm. Fig. 4.1.7 shows the TEM cross-section of a FinFET with multi-fins. The devices show a tri-gate architecture with a very conformal gate stack. In this experiment, fixed and rather long gate length (L=1 μm) was used to avoid any short channel effect. For this gate length, series resistance can be neglected.

The static I_D-V_G characteristics were measured using an HP 4155A semiconductor parameter analyzer. All FinFET devices were measured in the linear operation regime with V_D=10mV to avoid self-heating effect. Low temperature measurements were carried out at wafer level with SussMicroTec LT probe station in the temperature range from 77K to 350K. Measurements were repeated on devices from different chips (≈3-4) on the same wafer and show very little dispersion.

4.1.3 Threshold Voltage

The threshold voltage V_{th} has been extracted from the modified Y-function method. In Fig. 4.1.8 (a), Y-function modification is shown. The intrinsic Y-function ($Y=I_D/g_m^{0.5}$) of measurement data have nonlinear behavior because the devices have the strong effect of the mobility degradation parameters. Using the iterative modification of $Y_{new}=Y\cdot(1-\theta_2(V_G-V_{th})^2)^{0.5}$, Y_{new} has the linearity and adapted to extract the parameters. Fig. 4.1.8 (b) shows the temperature dependence measured for n-type and p-type devices. The curves feature only weak dependence with fin width. As expected, the absolute value of V_{th} decreases when temperature increases. The slope of $V_{th}(T)$ can be used to extract the doping concentration in the channel. Indeed, the threshold voltage is the linear combination of the flat band voltage, Fermi surface potential and the potential derived from the depletion charge.

The Fermi surface potential ϕ_B has the most significant temperature dependence. Indeed, dϕ_B/dT is strongly negative because dn_i/dT exponentially increases as a function of T as follows [23, 24]:

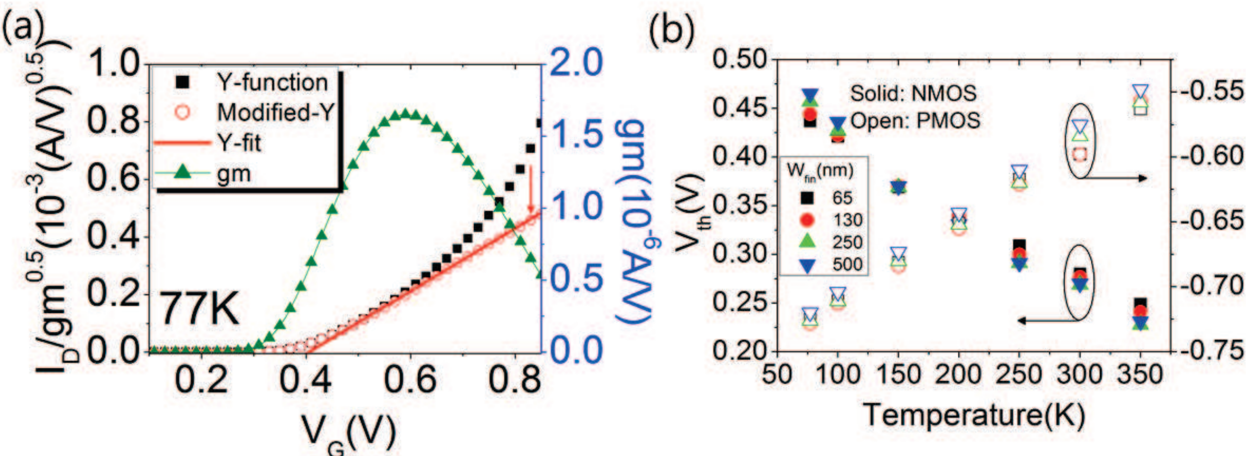


Figure 4.1.8 : (a) Modified Y-function technique. Nonlinearity of intrinsic Y-function (black square) is modified using iteration (red circle). (b) V_{th} as a function of temperature for W_{fin} values ranging from 65 to 500 nm. The absolute value of V_{th} increases at low temperature.

$$\frac{d\phi_B}{dT} = \frac{k}{q}\left(\ln\left(\frac{N}{n_i}\right) - 2\frac{T}{n_i}\frac{\partial n_i}{\partial T}\right), \tag{4.1.1}$$

with

$$n_i \propto T^{1.5}\exp\left(\frac{-E_g}{2k_B T}\right), \tag{4.1.2}$$

where k_B is the Boltzmann constant, q the elementary charge, N the doping concentration, n_i the intrinsic carrier density, and T the temperature. Thus, V_{th} decreases when temperature increases. The measured dV_{th}/dT is equal to 0.52mV/K in both p-type and n-type. From this value, the residual channel doping concentration is estimated around $10^{17}cm^{-3}$.

4.1.4 Surface Current Separation Technique

Fig. 4.1.9 shows typical I_D-V_G characteristics for n- and p-channel devices measured at room and liquid nitrogen temperatures, with various fin width values. As usual, the drain current I_D is larger at low temperature because of the increase in mobility due to phonon freezing.

Here it should be noted that the slope of the I_D-V_G curves (the transconductance) in high inversion was found much smaller at 77K than at room temperature (Fig. 4.1.9 (c), (d)). In NMOS transistors, the drain current even decreases at high gate voltage (above 1.3V).

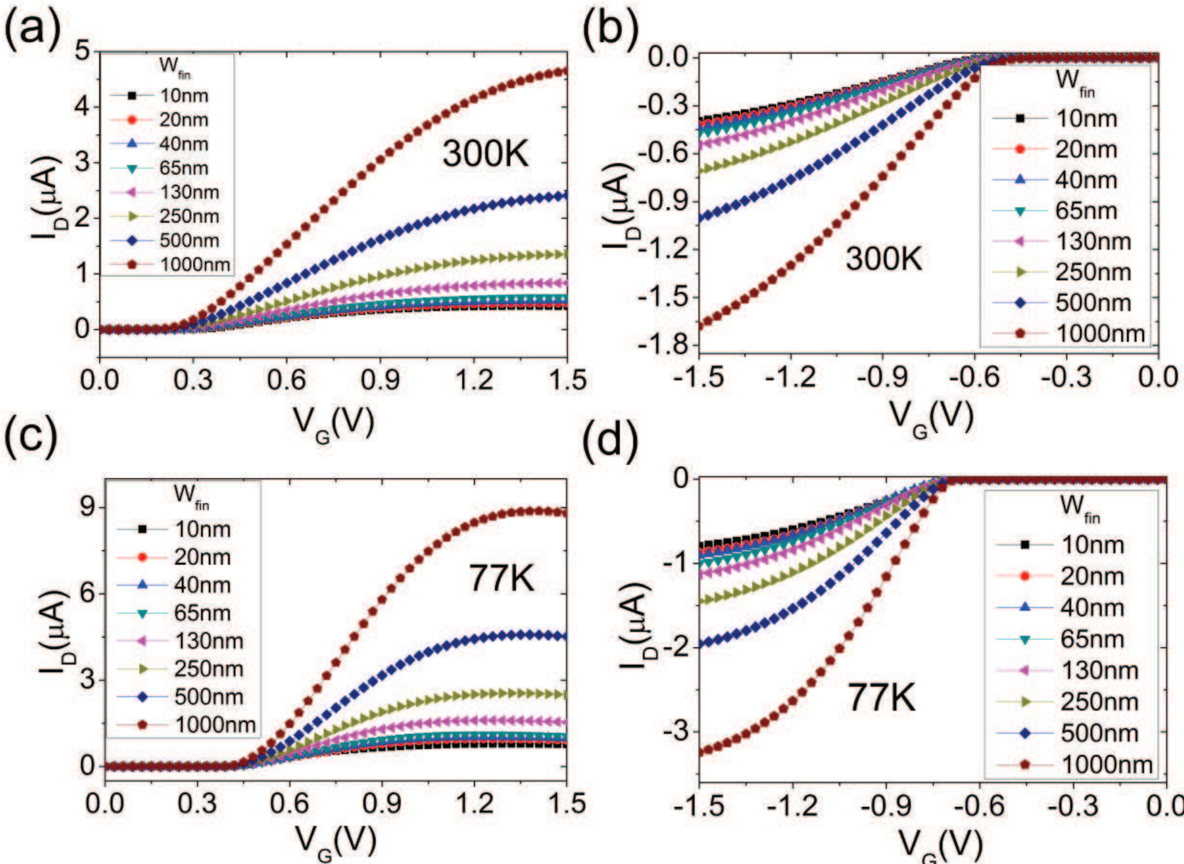


Figure 4.1.9 : FinFET I_D-V_G characteristics with various W_{fin} values; (a) NMOS at 300K, (b) PMOS at 300K, (c) NMOS at 77K and (d) PMOS at 77K. As expected, threshold voltages increase at low temperature compared to room temperature. At low temperature, the drain currents are visibly degraded at high gate bias voltage in NMOS FinFETs while the degradation is not as severe in PMOS FinFETs.

This decrease in I_D, which induces a negative transconductance, could stem from surface roughness scattering or from lattice self-heating [15, 25, 26]. However, self-heating can be ruled out here, due to the very low V_D value used during measurements (V_D = 10m V). Thus, the surface roughness scattering is mainly responsible for the drain current decrease at high gate drive bias. It is the purpose of this paper to understand whether all the interfaces contribute equally or not, and which is then the roughest interface. The first step is to separate the top and sidewall channels.

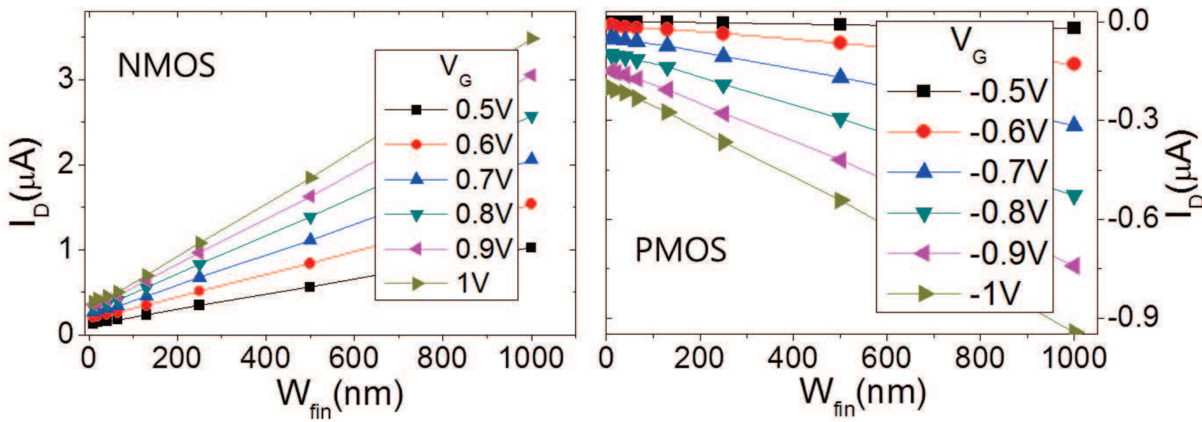


Figure 4.1.10 : I_D-W_{fin} for the top/sidewall current separation with NMOS (left) and PMOS (right) FinFET at 300K. From the linearity, the sidewall current is extracted at W_{fin}= 0.

The inversion channel of the FinFET was formed along the surface of the fin, except at the bottom surface because it faces the BOX and the back substrate, which was grounded in this experiment. Thus the current mainly flowed along the top and sidewall surfaces.

Transport characteristics along top surface and sidewalls can be split by linear extrapolation of the current versus fin width, using a simple mathematical technique [18, 20]. At fixed gate bias, the drain current varied indeed linearly with fin width, as can be seen from Fig. 4.1.10. From the linear extrapolation at W_{fin}=0, the y-axis intercept provides the current I_{Dside} that flows along the sidewalls, with an equivalent gate width equal to $2{\cdot}H_{fin}$. The top surface current I_{Dtop} can be deduced by:

$$I_{Dtop} = I_D - I_{Dside} \quad . \tag{4.1.3}$$

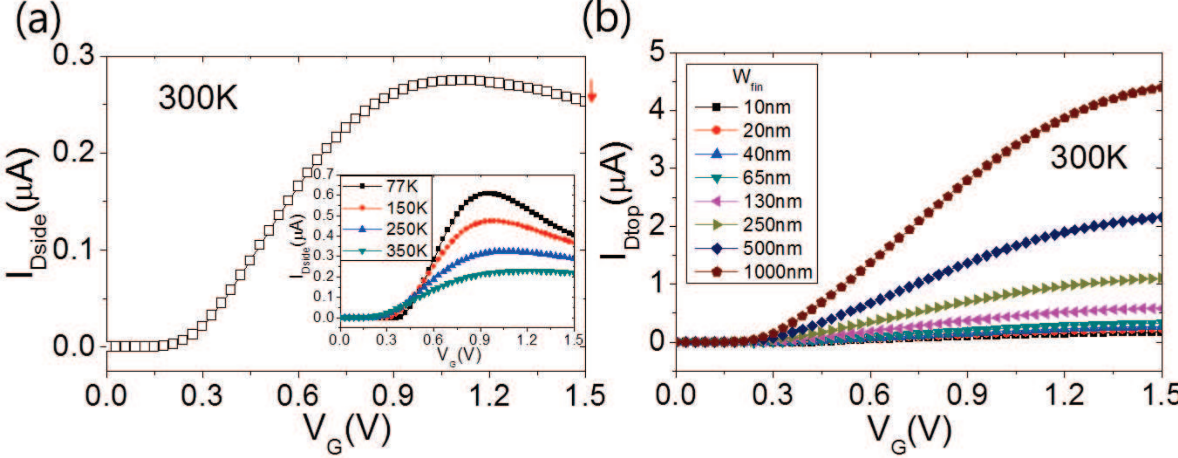


Figure 4.1.11 : Separated (a) sidewall and (b) top surface current in NMOS FinFET at 300K. Decreasing temperature increases the current degradation of sidewall at high gate bias ((a) inset).

This splitting technique was used for every temperature and every gate voltage. It should be noticed here that it is important to use a fixed gate voltage in order to account for potential differences in the threshold voltage associated to each interface. A small deviation from linearity can be observed only for n-type FinFETs, with fin widths narrower than 130 nm, and gate voltage larger than 0.9 V. This may be due to some coupling effects between the two facing sidewalls in the narrowest fins. However, thanks to the wide range of W_{fin} values used for the extrapolation, this deviation plays a negligible role and the sidewall current that is extracted using this method is free from any coupling effect. It does not represent the real current that flows in an extremely narrow fin, but rather the current that flows along the sidewalls of larger fins, which is exactly the information that we want to obtain. This is an advantage of the extrapolation method compared to methods which use the narrow fin devices as representative of the sidewall current in larger fins, as assumed for instance in [21].

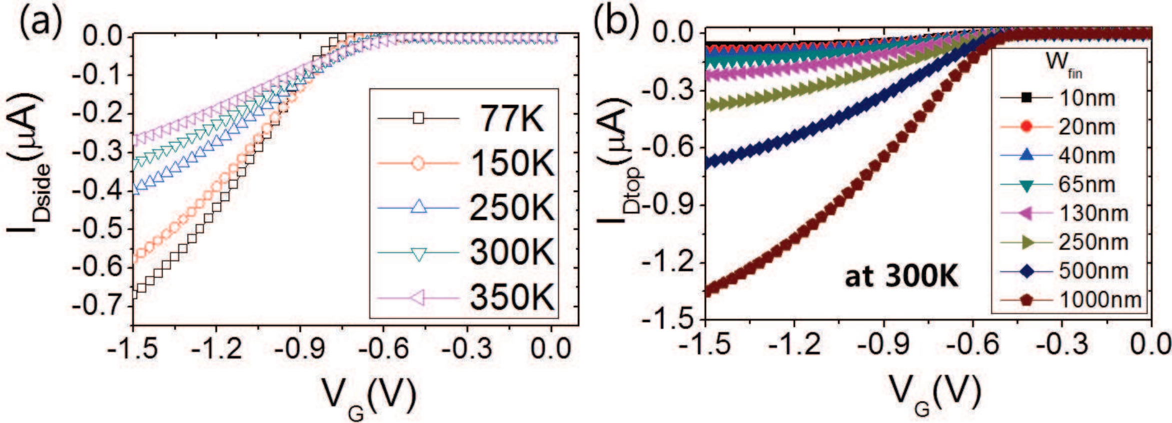


Figure 4.1.12 : Sidewall current of PMOS with temperature variation. Compared to the top surface current (b), the sidewall current (a) does not decrease at high gate bias.

Fig. 4.1.11 shows the result of this splitting for the n-type FinFETs: the sidewall current, which is the extrapolated current at zero fin width, is the same for all the n-type devices (Fig. 4.1.11 (a)), while the top channel current, is proportional to fin width (Fig. 4.1.11 (b)).

It should be noted that the sidewall current decreases at high gate bias even at 300K. In contrast, the top surface current does not decrease at 300K. According to previous discussion, this suggests that surface roughness scattering is affecting carrier transport on the sidewalls more strongly than on the top. The effect was even stronger at low temperature, with a strong decrease of sidewall current at high field in NMOS FinFETs (inset in Fig. 4.1.11 (a)), while no such degradation was observed, neither for top surface conduction in NMOS FinFETs (not shown here) or for sidewall and top surface conduction in PMOS FinFETs (Fig. 4.1.12).

4.1.5 Temperature Dependence of FinFET Effective Mobility

A temperature dependent measurement was used to further analyze the role of surface roughness at the two interfaces. For mobility extraction, several techniques are available [27]. The split C-V technique was not applicable here, due to very small device area. Therefore, effective mobility μ_{eff} was extracted for each interface using the following equation:

$$\mu_{eff} = \frac{L}{W\, C_{ox}\,(V_G - V_{th})\, V_D} I_D \quad , \tag{4.1.4}$$

where L is the channel length, W the channel width, C_{ox} the gate oxide capacitance per unit area and I_D the current. W and I were set to W_{fin} and I_{Dtop} for the effective mobility of the top channel, and to $2 \cdot H_{fin}$ and I_{Dside} for the effective mobility of the sidewall channel, μ_{efftop} and $\mu_{effside}$ respectively. For each mobility extaction, V_{thside} / V_{thtop} extracted from I_{Dside} / I_{Dtop} were adopted as V_{th} in Eq. (4.1.4). Gate oxide capacitance per unit area was measured using a large area dedicated test structure.

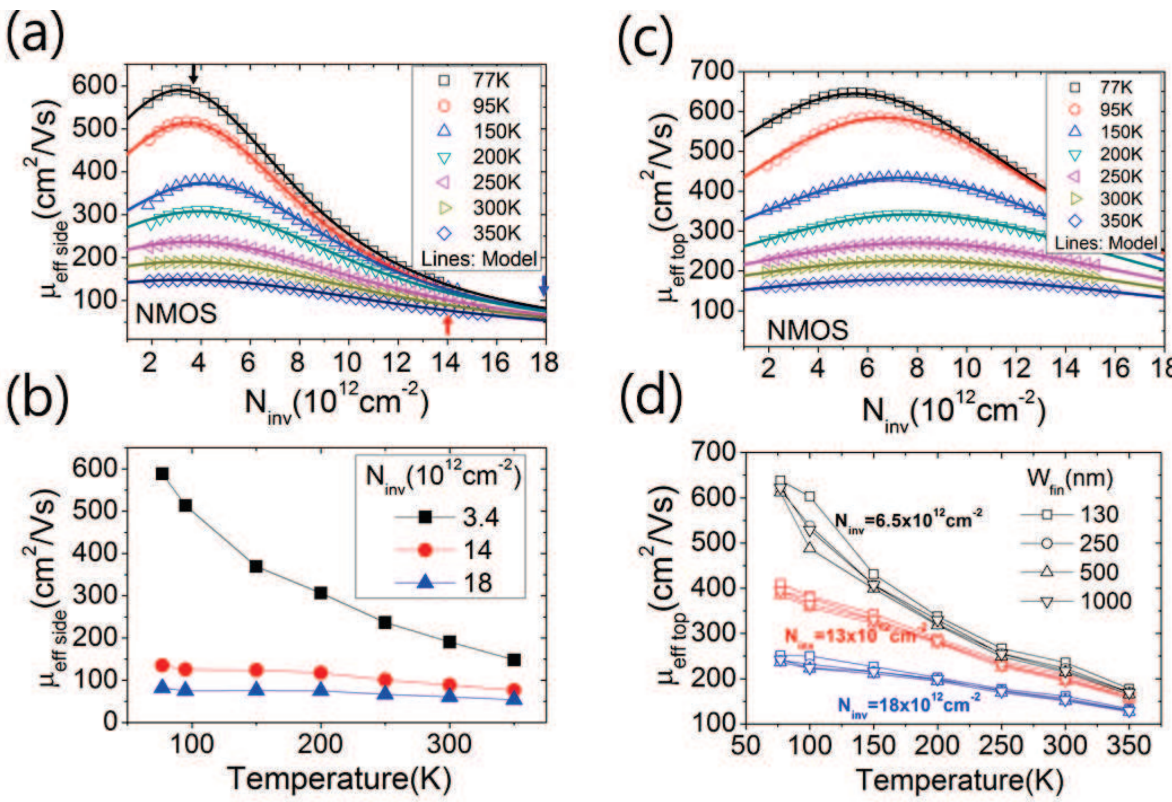


Figure 4.1.13 : (a) Sidewall mobility of NMOS with temperature variation. Low temperature induces strong mobility degradation at high electric field. (b) Sidewall mobility at fixed N_{inv} indicated colored arrow at (a). (c) Top surface mobility of NMOS. Mobility degradation at high N_{inv} shows less decrease compared to the sidewall case. (d) Top surface mobility at fixed N_{inv} (same as (b)).

Fig. 4.1.13 show the inversion charge and temperature variations of $\mu_{effside}$ and μ_{efftop} for NMOS FinFETs with W_{fin}=130 nm. The carrier density in the inversion channel, N_{inv}, was calculated using the strong inversion approximation $N_{inv} \approx C_{ox} (V_G-V_{th})/q$.

To fit the experimental data, the following empirical equation was used for μ_{eff} [15]:

$$\mu_{eff} = \frac{\mu_0}{1+\theta_1(V_G - V_{th}) + \theta_2(V_G - V_{th})^2} , \tag{4.1.5}$$

where μ_0 is the low field mobility, θ_1 and θ_2 are the mobility degradation parameters which describe mobility degradation at high transverse effective field. The θ_2 correlates to surface roughness scattering, while θ_1 includes phonon scattering dependence with gate voltage (due to changes in the overlap integrals) as well as Coulomb scattering. It should be noted that in the presence of significant Coulomb scattering, θ_1 can be found negative [28, 29]. It is the case here. As can be seen from Fig. 4.1.13, the empirical model of Eq. (4.1.5) fits the measured data very well. Depending on the temperature, μ_0 (cm^2/Vs) of sidewall current was changed from 122 (350 K) to 423 (77 K) in NMOS and from 80 (350 K) to 339 (77 K). The θ_1 (V^{-1}) of sidewall current increased from -0.419 (350 K) to -1.667 (77K) in NMOS but currents in the case of PMOS it did not have tendency. The average value of θ_1 (V^{-1}) in PMOS has 0.8 for sidewall and 0.3 for top surface.

To further analyze the results, it is useful to remember that the different scattering mechanisms that dominate carrier transport show very different dependences as a function of temperature and effective field. Generally, the effective mobility in inversion layers is composed of three mobility terms corresponding to the main scattering mechanisms i.e. Coulomb, phonon and surface roughness, and sometimes neutral defects scattering [30]. It has been shown that the phonon limited could be expressed as [31]:

$$\mu_{ph} \propto T^{-n} \cdot N_{inv}^{-1/\gamma} , \tag{4.1.6}$$

At low temperature or high inversion density, when most carriers are in the first sub-band level, n and γ are equal to 1 and 3, respectively. When intervalley and interband scattering can occur, these parameters take larger values in the range 1-1.75 and 3-6, respectively, depending on crystalline orientation of the conduction plane. In both cases, the phonon scattering limited mobility is rapidly increasing as temperature decreases and depends weakly on N_{inv}. The limitation by Coulomb scattering is especially important at relatively low temperature, around 100K and below. In this range, it can be modelled as [31]:

$$\mu_C \propto T^{-1}\ N_{inv}^{\chi}\ , \tag{4.1.7}$$

where χ is in the range 1.6-2, according to the respective contributions of channel doping and oxide charges. In this temperature range, the increase of temperature induces Coulomb scattering rate increase due to screening effect. On the other hand, at higher temperature, increased kinetic energy reduces scattering effect. Thus μ_C is proportional to T. Finally, the surface roughness scattering limited mobility μ_{SR} can be described as follows [32-34]:

$$\mu_{SR} \propto \frac{E_{eff}^{\ -\alpha}}{\Delta^2\ \lambda^2}\ , \tag{4.1.8}$$

where Δ is the rms value of the surface roughness, λ its correlation length, E_{eff} the effective field, which is proportional to N_{inv} in this case and the exponent α is ranging between about 1 and 2, depending on carrier type and surface roughness statistical properties [32, 33]. According to Eq. (4.1.8), μ_{SR} should be independent of temperature, while the two other mechanisms depend on it. It also shows the strongest degradation for high N_{inv} values. These considerations allow identification of the dominant scattering mechanisms according to inversion charge and temperature range.

Fig. 4.1.13 (a) and (b) show the inversion charge dependence of sidewall mobility for temperature values ranging from 77 to 350K. In order to keep the picture clear, the top surface mobility is shown for one fin width value only (130 nm). It should be noted first that the extracted $\mu_{eff}(N_{inv})$ curve shows a positive slope, typical of Coulomb scattering, at low inversion charge. This contribution of Coulomb scattering is even more visible at low temperature, where it becomes the dominant scattering mechanism in weak inversion, due to phonon freezing. It should be noted also that the sidewall mobility decreases dramatically in strong inversion (N_{inv}>5x10^{12} cm^{-2}) as compared to the mobility of the top surface, indicating a stronger influence of surface roughness scattering.

The temperature dependence of sidewall and top surface mobility for given values of N_{inv} is shown in Fig. 4.1.13 (b) and (d), respectively. In Fig. 4.1.13 (d), we show the top mobility extracted for several fin width values, ranging from 130 nm to 1 μm. It can be checked that the fin width dependence is indeed small, validating the linear extrapolation procedure. We found experimentally that $\mu_{effside}$ did not depend significantly on temperature for high N_{inv} (red circles and blue triangles). Indeed, because of the -2 power law of E_{eff} in Eq. (4.1.8), μ_{SR} is becoming dominant in strong inversion. This allows us to conclude that, in our devices, μ_{eff} is indeed dominated by surface scattering in this regime. For low N_{inv}, $\mu_{effside}$ includes

contributions from Coulomb and phonon scatterings. That is the reason why $\mu_{effside}$ shows enhanced temperature dependence at low N_{inv}. Especially, the negative slope of the mobility versus temperature indicates that the phonon scattering limited mobility still plays a role. In the case of the top surface (Fig. 4.1.13 (d)), μ_{efftop} decreases for increasing temperatures, even at high N_{inv}. This means that surface roughness scattering is not the dominating scattering mechanism at the top surface while it does on the sidewalls, which are thus suspected to be rougher. Moreover this larger surface roughness scattering effect reduces the peak mobility $\mu_{effside}$ compared to μ_{efftop} ($\mu_{effside}$=600 cm^2/Vs and μ_{efftop}=650 cm^2/Vs at 77K).

Fig. 4.1.14 shows the results obtained for the mobility of PMOS FinFETs along top surface and sidewalls. In contrast to the results obtained for NMOS, the $\mu_{effside}$ value obtained for PMOS does not show any decrease as a function of N_{inv}. As compared to NMOS, $\mu_{effside}$ always decreases with temperature (Fig. 4.1.14 (b)), indicating that the effective mobility along the sidewalls of PMOS FinFETs is not fully dominated by surface roughness scattering. This does not mean that the surface roughness is physically different in NMOS and PMOS FinFETs. Only its influence on the mobility is different.

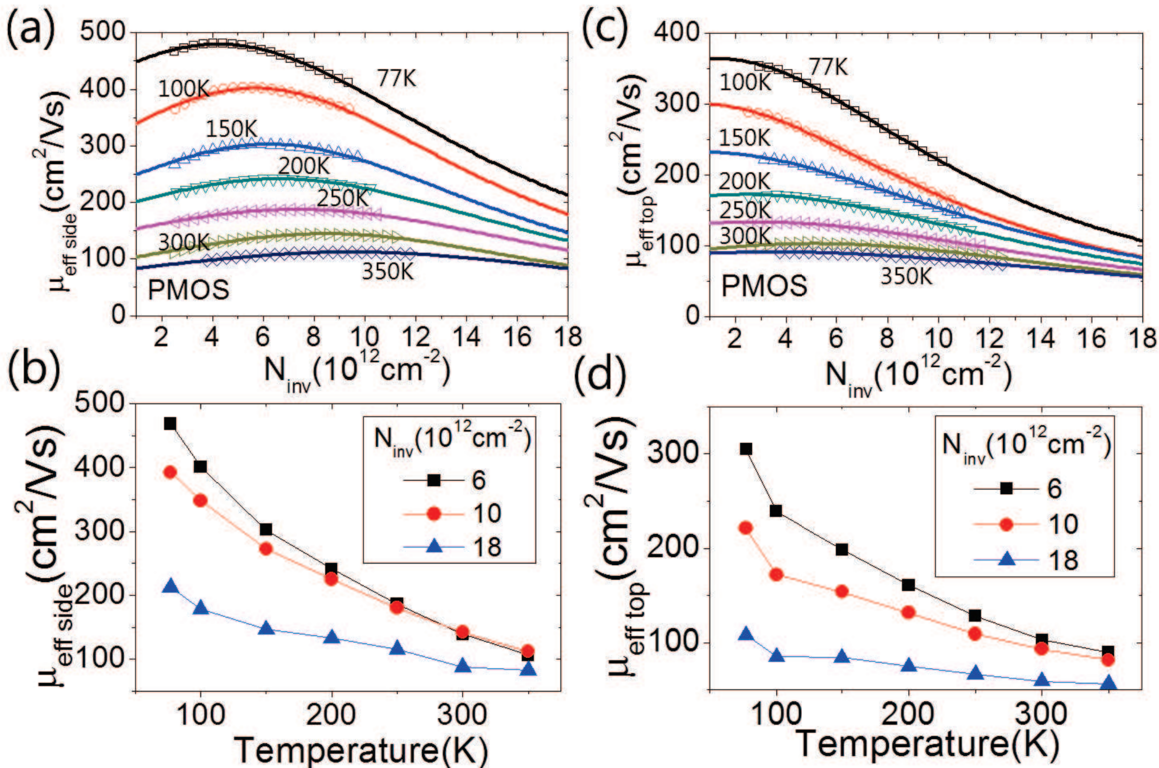


Figure 4.1.14 : Separated effective mobility of PMOS finFET (a), (b) sidewall and (c), (d) top surface.

It has been shown previously, by simulation of surface roughness scattering in bulk MOSFETs, that hole mobility can show a different dependence with effective field, because

their wave vector at the Fermi energy, k_F, takes higher values than that of electrons, and both types of carriers are not sensitive to the same part of the surface roughness statistical distribution [35].

Finally, it should also be noted that the peak value extracted for $\mu_{effside}$ is higher than that of μ_{efftop} in the PMOS FinFETs. For example, $\mu_{effside}$ is 490 cm^2/Vs while μ_{efftop} is 355 cm^2/Vs at 77K. This feature is consistent with the different orientation of the (110) sidewalls and (100) top surface. Indeed, it has been reported that the anisotropy of the effective mass due to surface orientation results in an enhancement of the effective mobility of holes [36-39].

4.1.6 Quantification of the Surface Roughness Scattering Effect

In order to quantify the contribution of surface roughness scattering to the top surface and sidewall current components, the surface roughness mobility degradation factor θ_2 was directly extracted from fitting of mobility data using Eq. (4.1.5). Because both the low field mobility and the effective field dependent scattering mechanisms depend on temperature, θ_2 should be normalized by μ_0. The correct parameter to quantify the influence of SR on mobility is thus θ_2/μ_0. The θ_2 parameter cannot be used as such since it depends on temperature (Fig. 4.1.15), even though surface roughness scattering does not. The SR limited mobility parameter, θ_2/μ_0, can also be extracted from the derivation of the reciprocal effective mobility [19]:

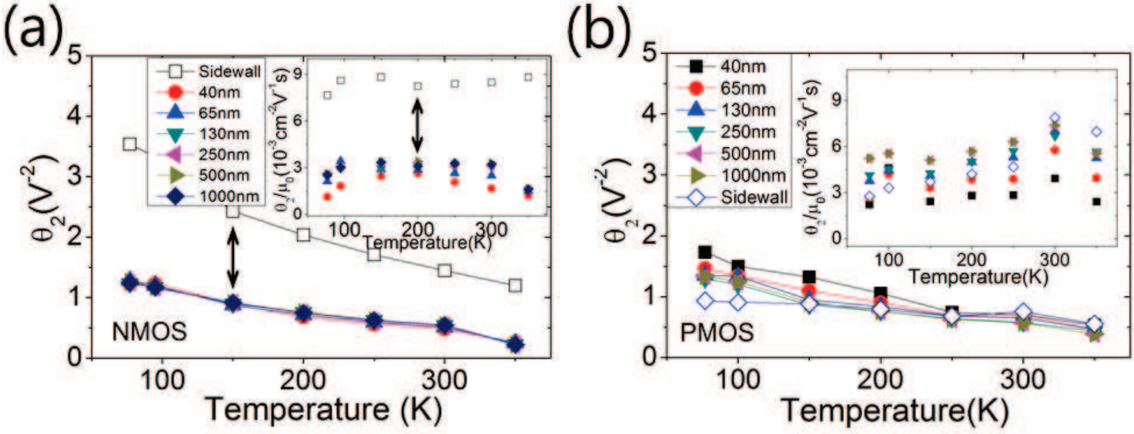


Figure 4.1.15 : Mobility degradation parameter θ_2 versus temperature (a) NMOS and (b) PMOS. Surface roughness scattering parameter θ_2/μ_0 is obviously distinguishable in NMOS sidewall (inset).

$$D_{eff} = \frac{d(1/\mu_{eff})}{dV_G} = \frac{\theta_1 + 2\theta_2(V_G - V_{th})}{\mu_0} \quad (4.1.9)$$

According to this equation, the SR mobility parameter θ_2/μ_0 can be obtained from half the slope of the D_{eff} versus V_G curve. The θ_2/μ_0 values, extracted from the direct fitting with Eq. (4.1.5) and calculated by Eq. (4.1.9), are nearly the same as shown in the inset of Fig. 4.1.15. As can be seen, the SR mobility parameter θ_2/μ_0 is almost independent of temperature. In the case of NMOS FinFETs, the θ_2/μ_0 values extracted for the top surface are around 3 $cm^{-2}V^{-1}s$ independent of W_{fin}, whereas the values at the sidewalls are found much larger, typically around 9 $cm^{-2}V^{-1}s$ (the inset of Fig. 4.1.15 (a)). Therefore, the surface roughness scattering is about 3 times higher on the sidewall than at the top surface. This corresponds to an enhancement of the geometrical factor $\Delta\cdot\lambda$, which characterizes surface roughness, by about 1.7 times for the sidewalls as compared to the top surface.

In contrast to the NMOS finFETs, θ_2/μ_0 for the PMOS does not separate among the sidewall and top surfaces, indicating that, as in bulk structures, holes are much less sensitive to surface roughness.

The contributions of the surface roughness scattering in the total effective mobility can be calculated as following:

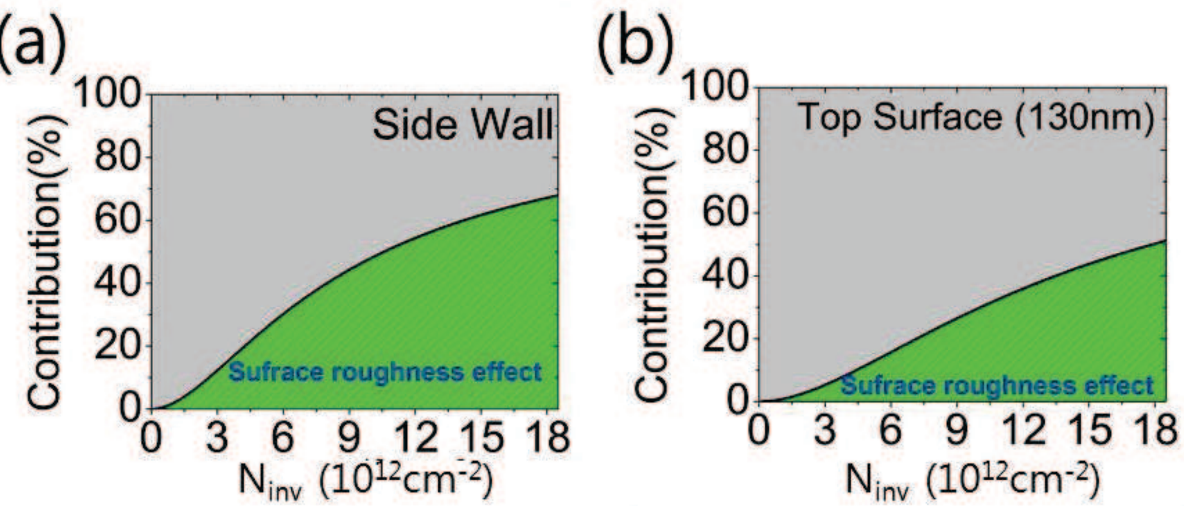


Figure 4.1.16 : Contribution of surface roughness mobility in total effective mobility.

$$P_{SR} = \frac{\left|\frac{\theta_2 (Vg - Vth)^2}{\mu_0}\right|}{\frac{1}{\mu_0} + \left|\frac{\theta_1 (Vg - Vth)}{\mu_0}\right| + \left|\frac{\theta_2 (Vg - Vth)^2}{\mu_0}\right|}, \qquad (4.1.10)$$

where P_{SR} is the surface roughness scattering probability.

Comparing to the top surface, the contribution of the surface roughness scattering at the sidewall is much higher. At the $1.8 \cdot 10^{13}$ cm^{-2} of N_{inv}, the mobility of sidewall is affected up to 70%. However, 50% of surface scattering mobility effect is observed on the top surface.

4.1.7 Conclusion

In this chapter, n-type and p-type triple-gate FinFETs have been experimentally studied by means of low temperature measurements. A simple method to split the drain current into its components associated to conduction along either the top surface or the sidewalls has been carried out by measuring devices with different fin widths.

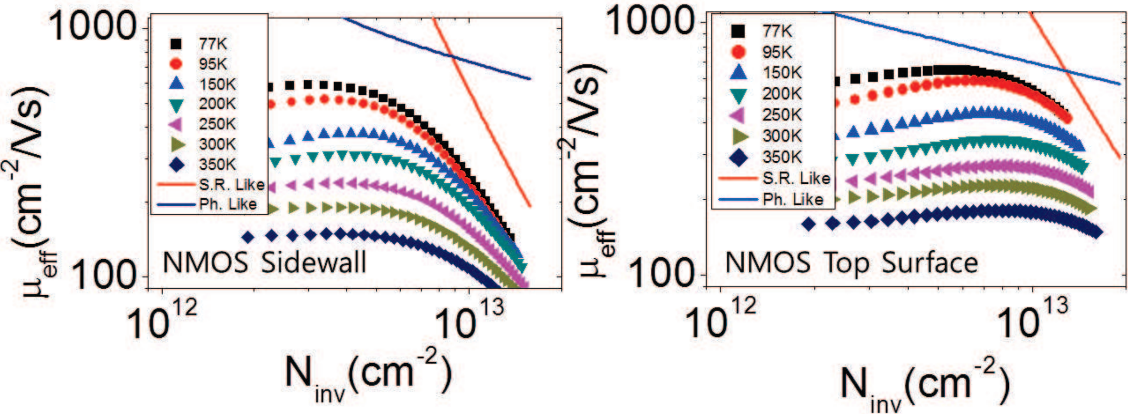


Figure 4.1.17 : Effective mobility of each surface in FinFET and general mobility behavior of phonon scattering and surface roughness scattering.

The sidewall and the top surface mobilities have been estimated in a wide range of temperature from each surface current component extracted by the linear extrapolation technique. The low temperature experiments enhance the relative importance of surface roughness scattering because the other scattering mechanisms become less effective. In n-type FinFETs, it was found that the sidewall mobility was strongly degraded at high inversion charge as compared to the top surface.

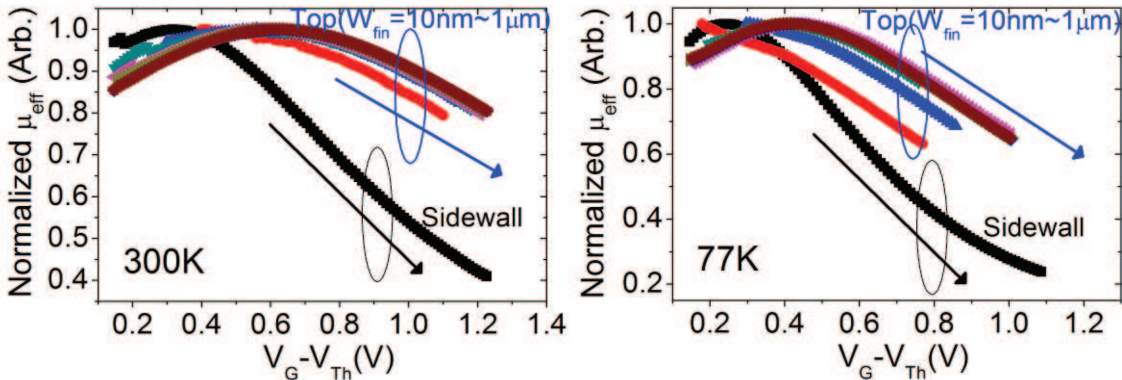


Figure 4.1.18 : Normalized mobility behaviors of NMOS sidewall and top surfaces at 300 K (left) and 77 K (right).

Effective mobility behavior for FinFET sidewall has completely different from the top surfaces as shown in Fig. 4.1.18.

To quantify this effect, the surface roughness scattering parameter θ_2/μ_0 was extracted. In n-type FinFETs, the surface roughness scattering rate associated to sidewalls was found to be 3 times higher than for the top surface. In contrast, SR scattering was less effective for holes so that SR scattering is not the only process involved, even in strong inversion, and no clear difference can be made between both interfaces. SR scattering is the main cause of mobility degradation at the sidewalls of n-type FinFET. It suggests that improvement of the etching process and adequate post treatments should allow further performance optimization.

4.2 SiGe Nanowire FET
– Phonon Scattering and Impurity Scattering

4.2.1 Device overview: Strain Engineering

The down scaling of metal oxide semiconductor field effect transistors (MOSFETs) has been continued for several decades for the purpose of higher integration, faster operating speed and smaller power consumption [40]. Gate length (L) is now reaching the 10 nm range. However, down-scaling is becoming more and more challenging due to performance limitations that arise from carrier velocity saturation, high-field effects such as impact ionization, or short channel effects of electrostatic origin such as drain-induced barrier lowering (DIBL), threshold voltage shift, subthreshold slope degradation and punchthrough. Due to their high immunity against short channel effects, Silicon-on-Insulator (SOI) based gate-all-around (GAA) nanowire FETs, with a metal/high-κ dielectric gate stack, have been suggested as excellent candidates for future technology nodes [1, 41, 42]. Besides, in conventional Si CMOS technology, p-type MOSFETs show a smaller mobility compared to n-type MOSFETs, due to differences in the band structure, and especially to the larger effective mass of holes compared to that of electrons.

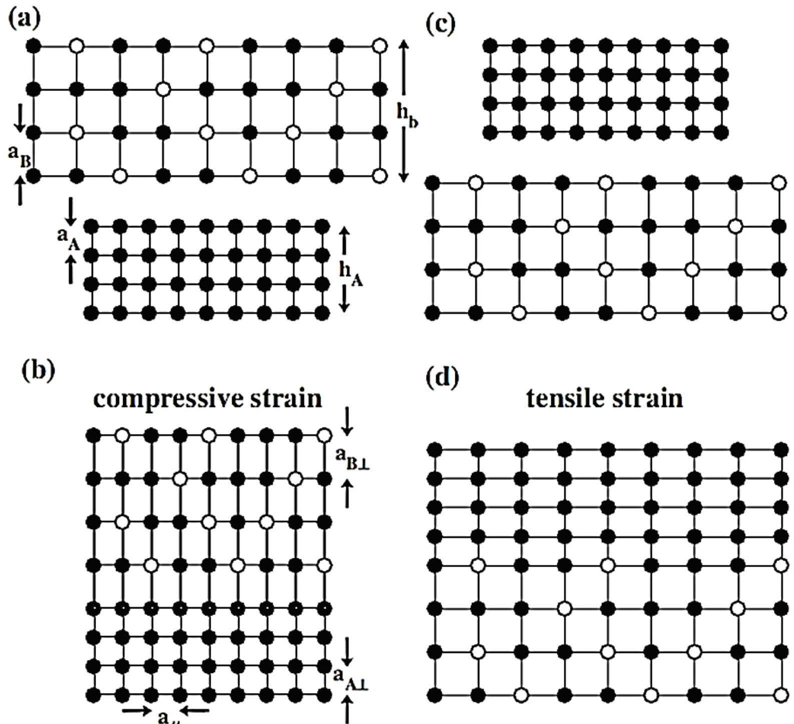


Figure 4.2.1 : Schematics of strained Si/SiGe hetero-structures. (a) and (c) Bulk lattices of SiGe and Si. (b) and (d) compressive strained and tensile strained hetero-structures [43].

To increase hole mobility, strain engineering has been studied aggressively [41, 43].

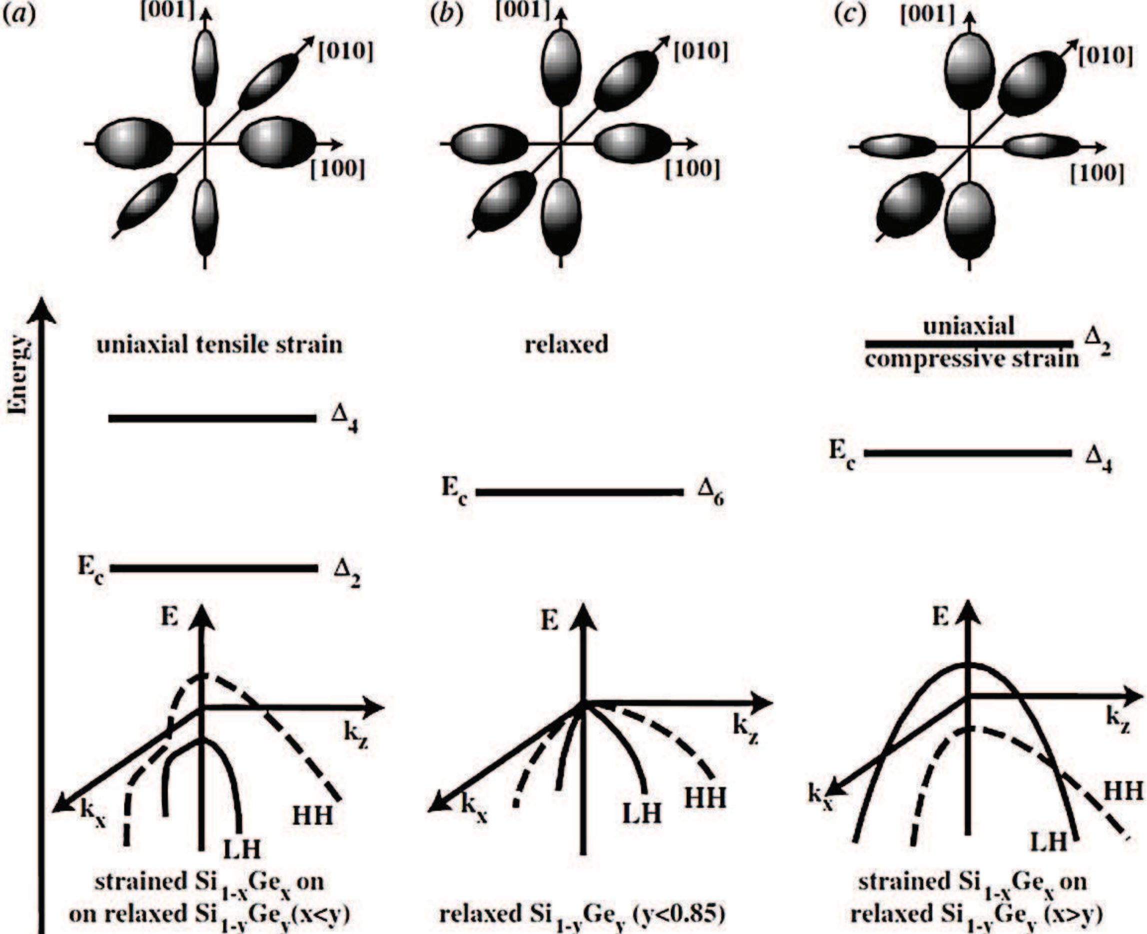


Figure 4.2.2 : The conduction band, valley structure and valence band splitting of (a) uniaxial tensile strained silicon or $Si_{1-x}Ge_x$ grown on a (100) $Si_{1-y}Ge_y$ virtual substrate with $x < y$, (b) bulk silicon and relaxed (100) $Si_{1-x}Ge_x$ with $x < 0.85$ and (c) uniaxial compressively strained (100) $Si_{1-x}Ge_x$ grown on a $Si_{1-y}Ge_y$ virtual substrate with $x > y$ [43].

For example, hetero-structure can be used to improve hole mobility. The lattice constant of SiGe is larger than the Si. In planar device, replacing the silicon source and drain with SiGe (embedded SiGe source/drain), compresses the Si channel and improves hole mobility with uniaxial strain. Increased Ge concentration makes larger lattice constant so that higher strain and higher mobility can be achieved. However strain cannot be increased infinitely. Solid state systems tend to be the lowest (stable) energy state. Lattice dislocations can be happened to reduce the energy state at the Si/SiGe interface. Increased Ge concentration not only makes the strain but also the dislocation and it limits the mobility enhancements.

Biaxial strain engineering is for the wafer level while uniaxial strain is applied to the individual devices. For the bulk device level, biaxial strain can be obtained by the growth of SiGe on the standard Si wafer or vice versa depending on which material is used.

With the improvement of SOI wafer technologies, strained SOI wafers are developed. Biaxial strained SOI wafer can be made similar to the bulk strained Si/SiGe wafers. The biaxial strained wafer has smaller hole mobility enhancement and larger V_{th} shift than uniaxial strained wafer [44]. However, smaller fabrication cost and the device roadmap based on the SOI technology make biaxial strained devices more attractive for the mass production.

Both uniaxial and biaxial strain engineering modifies the energy band structure because atoms in the strained lattice have different location. Manipulated energy band structure has two major properties which are effective mass change and the band split. Effective mass is depending on the radius of curvature of energy band structure in k space. Uniaxial c-strained Si has lighter hole effective mass than unstrained. Thus the effective mobility of PMOS is enhanced. Also the band split reduces the inter-band scattering. Reduced scattering improves the effective mobility.

In this chapter, compressively-strained (c-strained) SiGe MOSFETs will be demonstrated for hole mobility enhancement. A GAA device architecture associated to compressively strained SiGe nanowires is thus ideally suited for the PMOS transistor of future CMOS nodes. The purpose of this chapter is to study *short channel effects and transport mechanisms in p-type SiGe nanowire FETs , in order* to *analyze the influence of strain* on these effects and to *understand how this influence depends on gate length*. Both strained and unstrained SiGe channels will be compared.

4.2.2 Experimental Conditions: Device Fabrication and Measurement

3D stacked p-type SiGe nanowire FETs, with high-κ/metal gate stacks (HK/MG), were fabricated at LETI-CEA on a silicon-on-insulator (SOI) substrate [41]. Both a typical SOI (100) wafer and a tensile strained (1.3 GPa) SOI (100) wafer were used to form c-strained and the unstrained SiGe nanowires, respectively. The mains steps are as follows. First, $Si/Si_{0.8}Ge_{0.2}$ superlattices were epitaxially grown on each wafer by reduced pressure-chemical vapor deposition. In order to obtain narrow channels, hybrid deep ultra-violet/electron-beam lithography and resist trimming were combined. Cavities were patterned by means of an anisotropic dry plasma etching before isotropic removal of the Si layers. Nanowire lengths ranged from 40 to 600 nm. To achieve higher mobility, a 2nm thick Si capping layer was

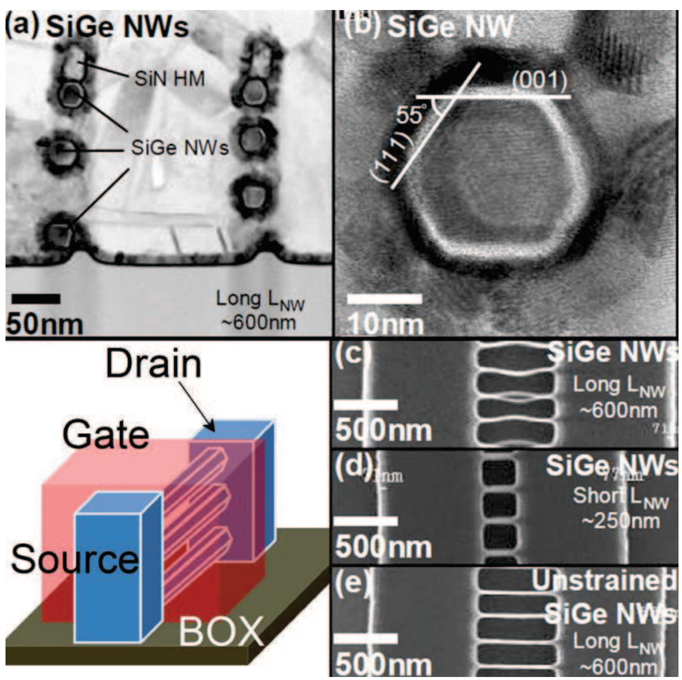


Figure 4.2.3 : (a) Cross-sectional TEM image of 3D stacked c-strained SiGe NW FETs. (b) Zoomed image of c-strained SiGe NW. Top-view of (c) c-strained SiGe NW with L=600 nm, (d) c-strained NW with L=250 nm and (e) unstrained SiGe NW with L=600 nm [41].

epitaxially grown at 650 °C on the SiGe nanowire surface. Then, an HfO_2 (3 nm)/TiN (10 nm)/Poly-Si gate stack was deposited as HK/MG. The cross-sectional shape was hexagonal as shown in Fig. 4.2.3. A SiO_2-like interfacial layer (T_{IL}: 1.5~2 nm) was also grown due to a non-optimized thermal process. After gate patterning, the source and drain contact regions were implanted and activated. A 10^{20} cm^{-3} boron doping concentration was achieved. After vertical spacers formation, the source/drain contacts were silicided. Finally, the fabrication ended with a standard back-end of line process. As shown in Fig. 4.2.3 (c), (d) and (e), only c-strained long channel nanowires are bent. Details about the fabrication process can be found in [41].

Static characteristics were measured using an HP 4155A semiconductor parameter analyzer and a SussMicroTec 200 mm low temperature probe station for temperatures ranging from 77K to 300 K.

4.2.3 Short Channel Effects in SiGe Nanowire FET

Fig. 4.2.4 compares the transfer characteristics (I_D plots against V_G at constant V_D) of the strained and unstrained SiGe p-type MOSFETs, for short (L = 40 nm) and long (L = 600 nm) channel lengths, respectively. The devices were biased in the linear regime of operation with a small drain voltage (V_D), fixed at 10 mV, and a gate voltage varying from 0.3 V to - 2 V. Both for long and short channel devices, the c-strained SiGe nanowires demonstrate larger drain current after turn on than their unstrained counterparts.

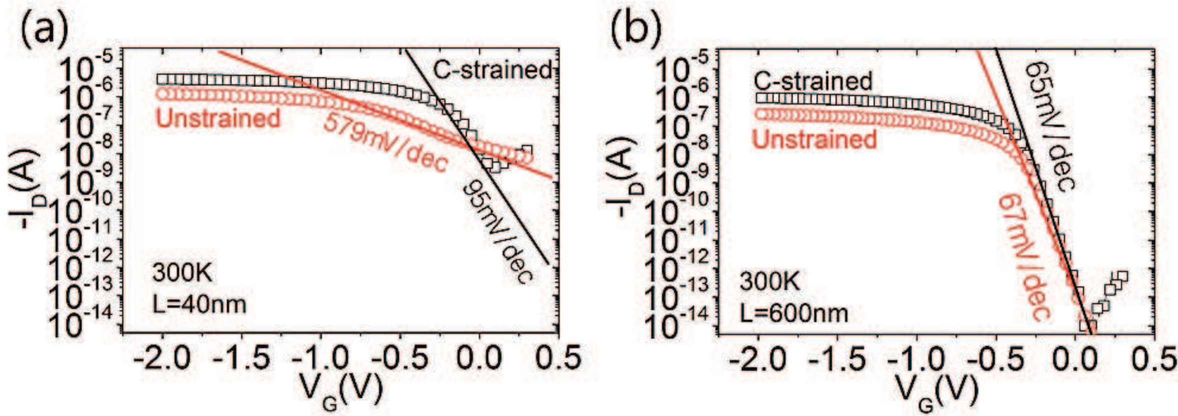


Figure 4.2.4 : I_D-V_G characteristics of SiGe nanowire FETs. C-strained and unstrained devices are compared in short channel (a) and relatively long channel (b). In short channel, unstrained device shows weak gate-channel control.

Following its definition [45], the subthreshold swing (SS) was extracted using (Eq. 3.6).

At room temperature, long channel devices displayed similar values of SS, with 67 mV/dec for unstrained SiGe nanowires and 65 mV/dec for c-strained SiGe nanowires. Both values are close to the ideal value at room temperature, which is about 60 mV/dec. In contrast, short channel effects could be observed for the 40 nm long devices. They were limited in the c-strained SiGe devices, with a SS value below 100 mV/dec, while they reached extremely large values, around 580 mV/dec, in the unstrained devices.

Threshold voltage (V_{th}) was extracted by Y-function method [46]. The method takes benefit from the fact that inversion drain current and transconductance (g_m) are related by the following relationship:

$$Y = \frac{I_D}{\sqrt{g_m}} = \left(\frac{W}{L} C_{ox} \mu_0 V_D\right)^{1/2} (V_G - V_{th}), \tag{4.2.1}$$

where C_{ox} is the gate oxide capacitance, μ_0 the low field mobility and V_D the drain bias. It includes only μ_0, geometrical parameters, gate capacitance and bias voltages. μ_0 and V_{th} can be directly extracted by a linear fitting and extrapolation of $I_D/\sqrt{g_m}$ against V_G. Importantly, the presence of series resistance does not affect in this relationship, which is a strong advantage of Y-function method.

The temperature dependence of V_{th} was estimated (Fig. 4.2.5), which can be exploited to

extract the doping level in the channel. Indeed, due to the small thickness of the silicon body, the devices under study belong to the fully-depleted SOI family and V_{th} temperature dependence is thus obeying the following law [47]:

$$\frac{dV_{th}}{dT} \approx \frac{d\phi}{dT} = -\frac{k_B}{q}\left(\ln\left(\frac{N}{n_i}\right) - 2T\frac{T}{n_i}\frac{\partial n_i}{\partial T}\right) \tag{4.2.2}$$

$$\text{with} \quad \phi = -\frac{k_B T}{q}\ln\left(\frac{N}{n_i}\right), \tag{4.2.3}$$

where ϕ is the Fermi surface potential, k_B Boltzman constant, T the temperature, q the elementary charge, N the channel doping concentration and n_i the intrinsic carrier density. Because $\partial n_i/\partial T$ is exponentially increasing with T [23], theory implies that $d\phi/dT$ is positive. So was the measured dV_{th}/dT, as verified in Fig. 4.2.5.

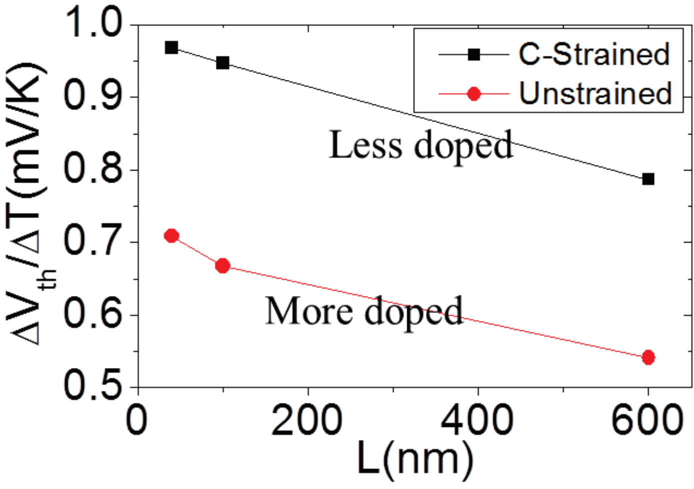


Figure 4.2.5 : Differences of threshold voltage according to the temperature. In each same length condition, unstrained SiGe nanowire FETs have lower dV_{th}/dT values.

For a given gate length, we found that dV_{th}/dT was smaller for unstrained SiGe nanowire than for c-strained ones. At this stage, it should be noted that the higher the doping concentration, the smaller dV_{th}/dT. The ratio between the channel doping concentrations in the two types of devices was calculated from:

$$\left.\frac{dV_{th}}{dT}\right|_{C-strained} - \left.\frac{dV_{th}}{dT}\right|_{Unstrained} \cong -\frac{k_B}{q}\ln\left(\frac{N_{C-strained}}{N_{Unstrained}}\right), \tag{4.2.4}$$

therefore,

$$\frac{N_{Unstrained}}{N_{C-strained}} = \frac{q}{k_B} \cdot \exp\left(\left.\frac{dV_{th}}{dT}\right|_{C-strained} - \left.\frac{dV_{th}}{dT}\right|_{Unstrained} \right). \tag{4.2.5}$$

Based on the values measured for the 100 nm gate length, $N_{Unstrained}/N_{C\text{-}strained}$ amounted to 25.75. Therefore, it was concluded that the unstrained SiGe nanowire channel was approximately 25 times more doped than the c-strained one, although the fabrication process was the same. We will come back to the conclusion later in the paper in the view of transport parameter analysis.

4.2.4 Analysis of Transport Mechanism

4.2.4.1 Temperature Dependence of Effective Mobility in SiGe NW FETs

Based on the conventional transfer characteristic model, the effective mobility (μ_{eff}) can be expressed as:

$$\mu_{eff} = \frac{L}{W\,Q_{inv}} I_D, \tag{4.2.6}$$

where Q_{inv} is the inversion charge, L is the gate length, W the channel width. The effective mobility was plotted against the inversion charge density Q_{inv}, which was evaluated using the strong inversion approximation,

$$Q_{inv} \cong C_{ox}(V_G - V_{th}). \tag{4.2.7}$$

Figure 4.2.6 illustrates the μ_{eff} dependence with $N_{inv}= Q_{inv}/q$. These curves were obtained for both unstrained and c-strained devices, with short and long channel lengths, for temperatures ranging from 77 K to 300 K. With c-strained channels, long and short devices behaved similarly, with an increase of effective mobility as temperature decreases. Such a behavior is indicative of a phonon scattering dominated transport. Indeed, due to phonon freezing, phonon scattering is the only scattering mechanism that results in strong temperature dependence, with an increase of mobility at low temperature. Long channel unstrained nanowires behave similarly. For long channels, c-strained SiGe nanowire FETs display 3.5 times higher mobility than unstrained nanowire FETs under the same temperature conditions. This was convinced with theoretical explanation which states that strain is responsible for a

degeneracy lifting of the light and heavy holes valence bands which results in lighter conduction mass and less inter-valley scattering.

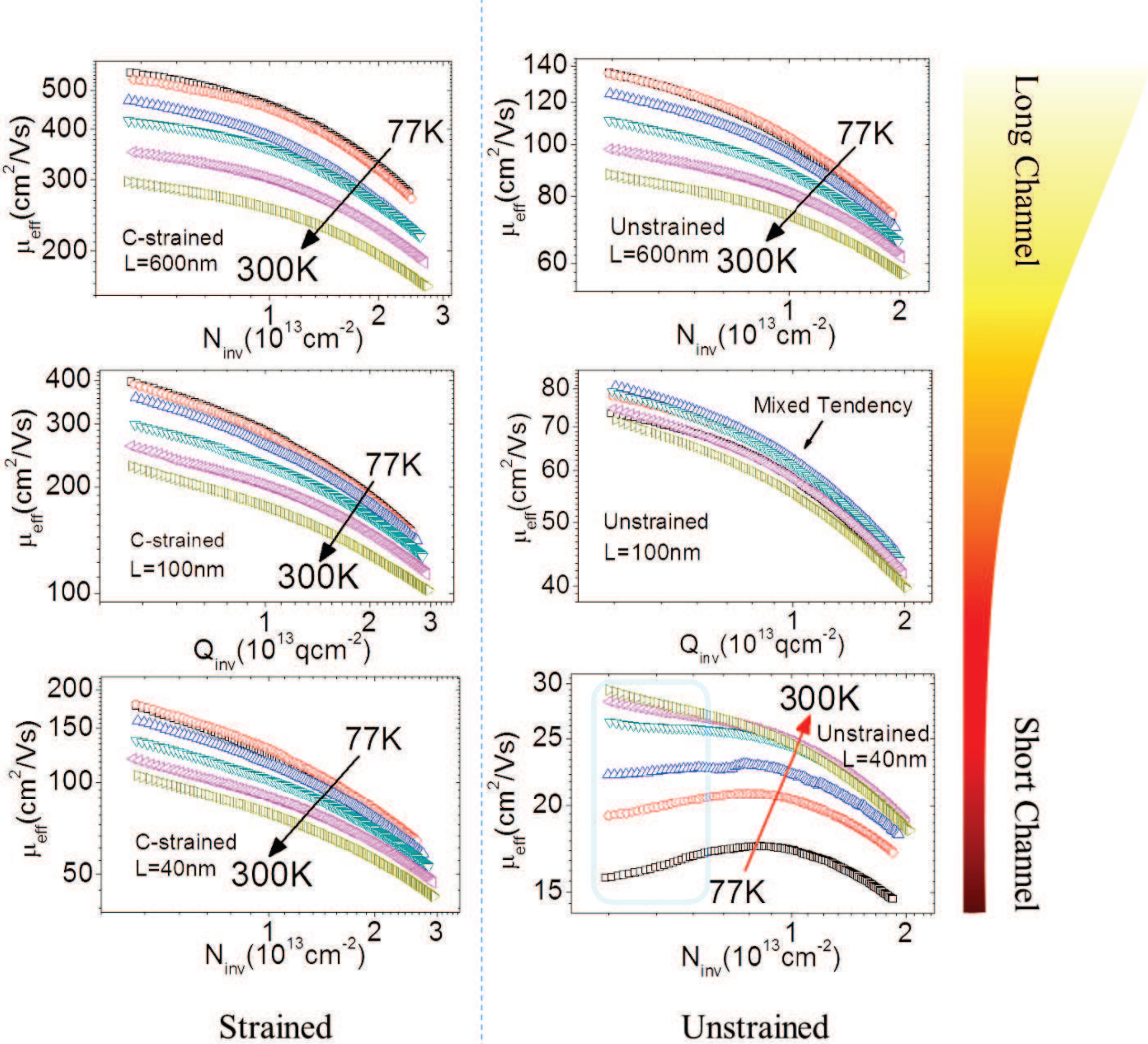


Figure 4.2.6 : Effective mobility of c-strained (left) and unstrained (right) devices. Specially, temperature dependent behavior of short channel unstrained device (bottom right) is completely different from the others.

The most striking results concerned short channel unstrained devices, which featured a fully opposite temperature dependence compared to other three cases. For these devices, effective mobility decreased at low temperature, especially at low inversion charge. Such dependence is typical of Coulomb scattering dominated transport. In addition, even at room temperature, where the influence of phonon scattering is still present, the effective mobility extracted for short devices is improved by about 6.5 times in the c-strained devices with respect to the unstrained ones. This is more than what we found for longer devices, for which a factor 3.5

had been obtained. From all these results, it was concluded that strain was influencing transport also by another mechanism than the sole change in the valence band and its resulting effect on mobility.

4.2.4.2 Temperature Dependence of Low-field Mobility in SiGe NW FETs

In order to go beyond these qualitative conclusions, a more precise mobility extraction than from Eq. 4.2.6 has to be performed. The split C-V technique [48, 49] could not be used here due to the small size of the devices under study. Instead, the low field mobility μ_0 was extracted from effective mobility model. This model assumes that effective mobility follows the usual E_{eff} dependence:

$$\mu_{eff} = \frac{\mu_0}{1+\theta_1\left(V_G - V_{th}\right)}, \tag{4.2.8}$$

where θ_1 is the first-order attenuation factor. Here, it was not necessary to include a second-order attenuation factor [50, 51].

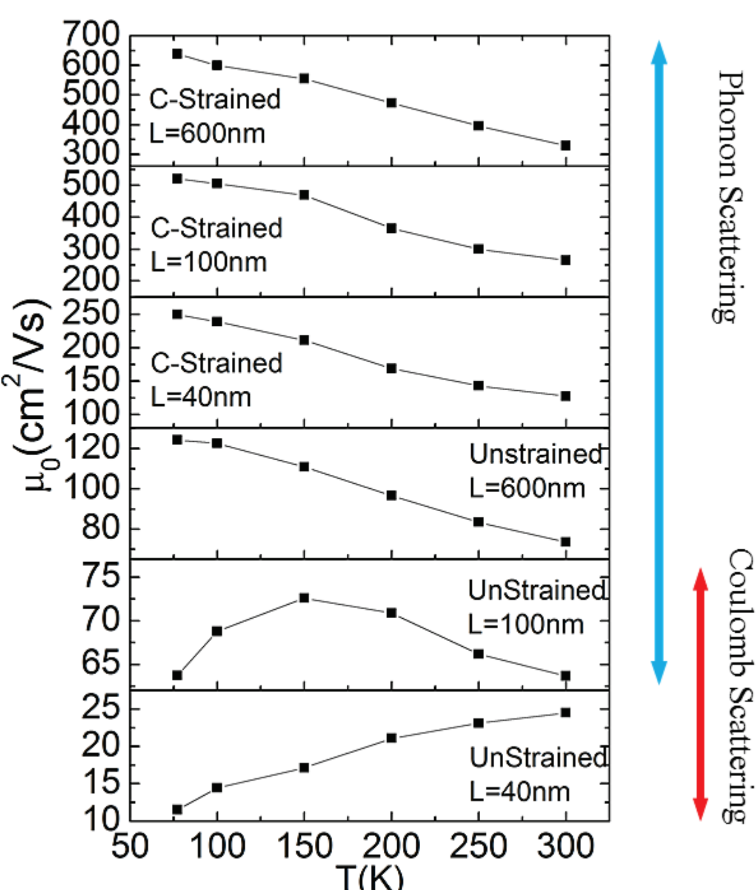


Figure 4.2.7 : Temperature dependence of low field mobilities. Coulomb and phonon scattering appear simultaneously as Matthiessen's rule in 100nm unstrained device.

Figure 4.2.7 displays the temperature dependence of the low-field mobility as a function of strain and gate length. The same trend was found as for μ_{eff}. Low field mobility decreased as temperature was increased for both all the c-strained devices and the longest channel (L = 600 nm) unstrained devices, while the opposite trend was obtained for the shortest channel unstrained devices. These two opposite temperature dependencies were compared to what is expected for phonon and Coulomb scattering, respectively. Phonon

scattering mobility μ_{Phonon} is expected to depend on temperature and effective field as:

$$\mu_{Phonon} \propto T^{-n} E_{eff}^{-1/3}, \quad (4.2.9)$$

where n is an empirical fitting parameter and E_{eff} the effective electric field [31]. Curve fitting of $\mu_0(T)$ for the c-strained and longest unstrained devices resulted in n = 1.75, which falls in the expected range for Si MOSFETs, depending on crystal orientation [32]. In contrast, Coulomb scattering mobility $\mu_{Coulomb}$ is linearly dependent on temperature [31], and follows the following law:

$$\mu_{Coulomb} \propto T Q_{inv}^{-1}, \quad (4.2.10)$$

which fitted quite well the experimental μ_0 (T) curve for the shortest unstrained devices. Therefore, it was concluded that phonon scattering was the dominant mechanism in c-strained and long unstrained devices, while Coulomb scattering dominated transport in the shortest unstrained devices. For unstrained devices with intermediate gate length (L = 100 nm), both mechanisms were present and dominated in turn according to the temperature range. For unstrained devices, the respective contributions of phonon and Coulomb scattering to low-field mobility was thus evolving as gate length was decreased.

4.2.4.3 Respective Contribution of Scattering Mechanism

In this third step of the analysis, focus was put on scattering by defects, with the aims of extracting their contribution to the total mobility and probing the variation of this contribution with gate length. To do so, all the main scattering mechanisms that can contribute to carrier transport in the channel - namely phonon, Coulomb, and neutral impurity scattering mechanisms- were taken into account together. Surface roughness scattering did not need to be accounted for, as long as only low-field mobility was concerned here.

Neutral impurity scattering is usually considered as temperature independent [52, 53]. It can result from the scattering with some lattice defects, which induce a local variation of the band structure while remaining neutral. Inactive doping atoms which can be found in heavily doped layers are an example of such defects. Other examples are point defects, such as silicon interstitial atoms. Point defects are known to be generated during source and drain implantations and to diffuse laterally towards the channel during the subsequent thermal annealing steps [54-56]. These point defects can diffuse as such, or as neutral clusters of point defects and doping atoms, leaving neutral defects in the channel at the end of the annealing

steps. They play a role as well in the diffusion of doping atoms out of the source and drain regions during anneals. Therefore, a certain amount of charged defects - such as ionized doping atoms - can also be injected in the channel. In the following, neutral defects and Coulomb centers will be considered together as defects arising from the source/drain implantation and annealing process steps and the aim of this paragraph is to evaluate their combined contribution to the low-field mobility.

The total mobility was obtained using Matthiessen's rule:

$$\mu_0 = \left(\frac{1}{\mu_{Coulomb}} + \frac{1}{\mu_{Phonon}} + \frac{1}{\mu_{Neutral}} \right)^{-1}, \qquad (4.2.11)$$

where

$$\mu_{Coulomb} = \alpha \cdot T\, Q_{inv}^{-1}$$

$$\mu_{Phonon} = \beta \cdot T^{-n} E_{eff}^{-1/3}$$

$$\mu_{Neutral} = \gamma$$

Each term follows different temperature dependences so that the contribution of each scattering mechanism can be extracted by fitting Eq. 4.2.11 to the experimental μ_0 (T) curves. Especially, the contribution of scattering by source/drain induced defects, which will be referred to as impurity scattering in the rest of the text, was extracted as:

$$Contribution(\%) = \frac{\frac{\alpha}{T/300} + \gamma}{\frac{\alpha}{T/300} + \beta (T/300)^n + \gamma} \cdot 100\,. \qquad (4.2.12)$$

	α (Vs/cm^2)	β (Vs/cm^2)	γ (Vs/cm^2)
C-strained (600 nm)	0	4.4x10^{-3}	3.6 x10^{-3}
C-strained (100 nm)	7.3x10^{-5}	2.4 x10^{-3}	1.4 x10^{-3}
C-strained (40 nm)	8.4x10^{-5}	1.8 x10^{-3}	1.1 x10^{-3}
Unstrained (600 nm)	15.8x10^{-3}	0.5x10^{-3}	24.3x10^{-3}
Unstrained (100 nm)	1.5x10^{-3}	4.9x10^{-3}	9.5 x10^{-3}
Unstrained (40 nm)	0.16x10^{-3}	6.8x10^{-3}	6.7 x10^{-3}

Table 4.2.1 : Fitting parameter of Eq. 4.2.12 used for Fig. 4.2.8

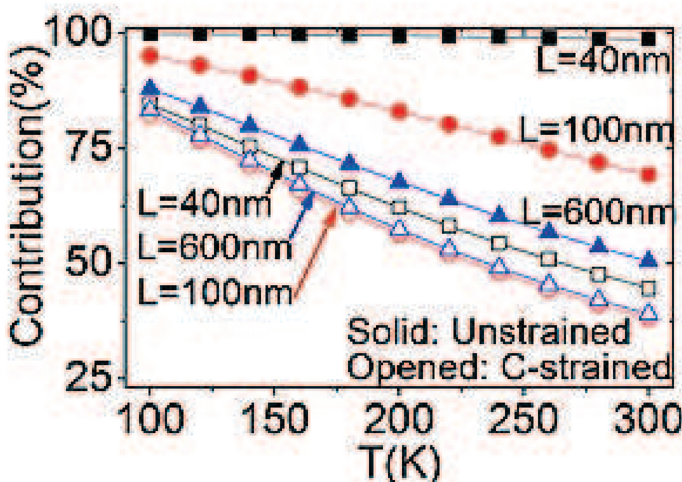


Figure 4.2.8 : Contributions of impurity scattering in each devices. Compared to c-strained devices, mobilities are strongly affected by impurity scattering in unstrained devices.

Table 1 summarizes the values of the parameters α, β and γ which were obtained from the fitting procedure, while Fig. 4.2.8 illustrates the resulting contribution of impurity scattering. All three c-strained devices displayed a similar trend, with similar contribution of impurity scattering. A very small increase of impurity scattering contribution by a few percent could only be observed in the shortest devices (L = 40 nm) This contribution increases as temperature decreases, but rather as a consequence of phonon freezing and of the resulting fading out of phonon scattering contribution to the total. In unstrained devices impurity scattering is globally larger than in c-strained devices. More importantly, impurity scattering contribution increased drastically at short gate length, until reaching 98 % of the total in 40 nm long channel devices.

4.2.4.4 Role of Strain: Boron Out-diffusion from S/D Regions

All these results could be understood consistently by assuming a *smaller point-defect assisted boron out-diffusion* from the highly doped source and drain contact regions during annealing steps *in the c-strained nanowires*. Low-frequency noise measurements, which have been performed on the same devices as those studied here, have also been found consistent with such an assumption [57]. Although our devices were SiGe nanowires subjected to uniaxial strain, this assumption would also be consistent with previous results obtained for biaxially strained SiGe films. For such layers, and although the exact physical mechanisms

may not be fully elucidated, it has been shown that a compressive strain was effective in reducing boron diffusion in SiGe, and induced a decrease of boron diffusion activation energy [58-61]. Here, they would explain the differences observed in device resistance to short-channel effects as well as in the extracted values for average channel doping or mobility.

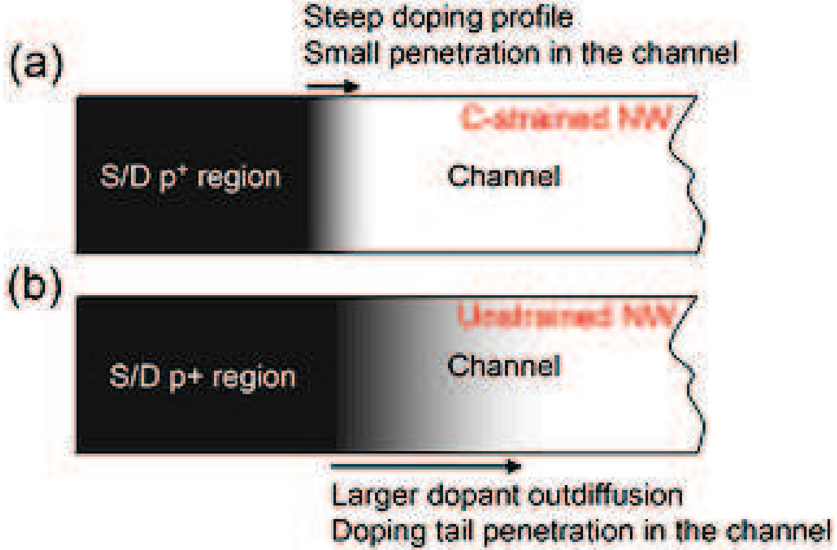


Figure 4.2.9 : Schematics of boron diffusion in SiGe nanowire FETs. B diffusion is retarded by strain so that short channel unstrained nanowire strongly affected by impurity scattering (a) for C-strained and (b) for un-strained device. In long channel devices, diffused B less affects in unstrained nanowire because diffusion length is relatively shorter than gate length.

From the results, it was concluded that boron out-diffusion created a disturbed region around the source/drain regions. While it remains negligible in c-strained devices, it represented most of the channel length in the shortest unstrained devices (Fig. 4.2.9). As a result, unstrained devices suffered from shorter effective channel length and larger short channel effects. Indeed, large subthreshold slope and channel punchthrough were observed in the subthreshold region of the shortest devices (Fig. 4.2.4 (a)). Moreover, the stronger dopant out-diffusion was also consistent with a larger average channel doping level in unstrained devices, as extracted from dV_{th}/dT. Finally B out-diffusion was associated to an increase of the neutral and charged scattering centers that degraded transport near the source-drain regions and even in the whole channel for the shortest devices.

4.2.5 Conclusion

SiGe nanowire architectures are among the most promising alternatives for future p-type MOSFETs generations. In addition, compressively strained SiGe is known as a very efficient performance booster, since it contributes to decreasing the holes effective mass and to reducing phonon scattering. In this chapter, it has been studied that the characterization of short channel effects and transport mechanisms in such devices, focusing on the influence of a compressive strain along the channel direction. Based on mobility extraction techniques and detailed analysis of mobility dependence against gate overdrive and operation temperature, the scattering processes that govern transport were identified and their respective contributions quantified. For long channel devices, phonon scattering was dominant and played the major role in improving mobility in c-strained devices.

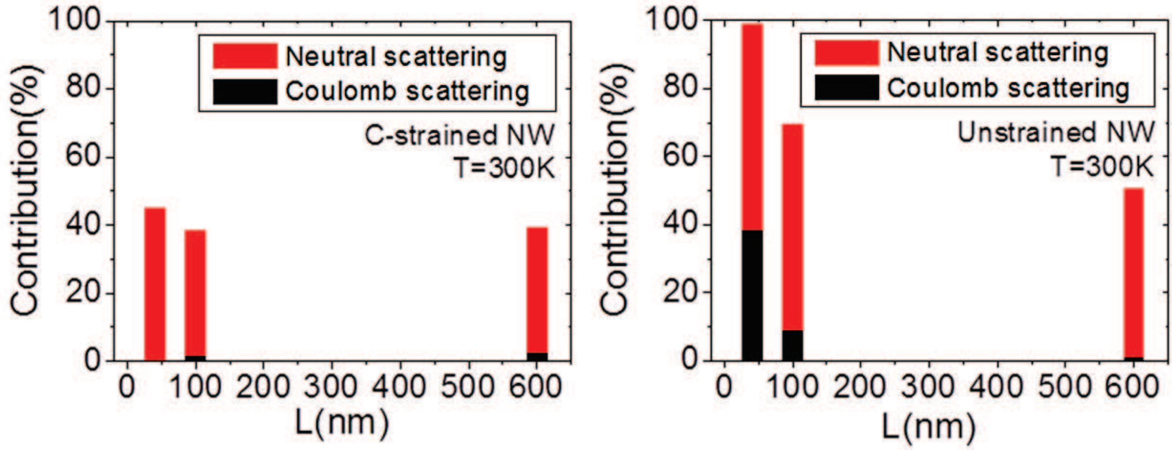


Figure 4.2.10 : Impurity Contribution of μ_0. Coulomb scattering in unstrained NW is much higher than c-strained NW.

However, it was found that impurity scattering was also playing a critical role in short channel devices. It could even be the dominant mechanism (98%) in unstrained devices at low temperature, while it brought a much smaller contribution in c-strained devices. This scattering originated from the presence of boron atoms, out-diffused from source and drain regions towards the channel during process, creating a kind of defective region with a high density of Coulomb and neutral centers in the vicinity of the source and drain regions. The impact of this defective region on the extracted mobility is all the more important as its extension is large compared to channel length. Results clearly show that compressive strain has a beneficial effect in reducing boron out-diffusion in SiGe nanowires. Therefore, beyond its expected influence in improving mobility due to band structure and phonon scattering

modifications, compressive strain is also beneficial because of its effect on process induced mechanisms and especially dopant diffusion. The latter effect increases the mobility advantage of c-strained p-type SiGe NW-MOSFETs compared to their unstrained counterparts. It also improves their resistance to short channel effects.

4.3 Junctionless Transistor – Volume Conduction and Reduced Short Channel Effects

4.3.1 Device Overview

4.3.1.1 Junction Gate Field Effect Transistor (JFET)

Before talking about junctionless transistor, we have to remind about junction gate field effect transistor (JFET). JFET has a doped semiconductor channel. Different from enhancement mode FET, channel is doped by same polarity as operating mode (p-doped for PMOS, n-doped for NMOS). The gate is also doped by opposite type of channel doping. The name of JFET is derived from the P-N junction at the gate-channel interface.

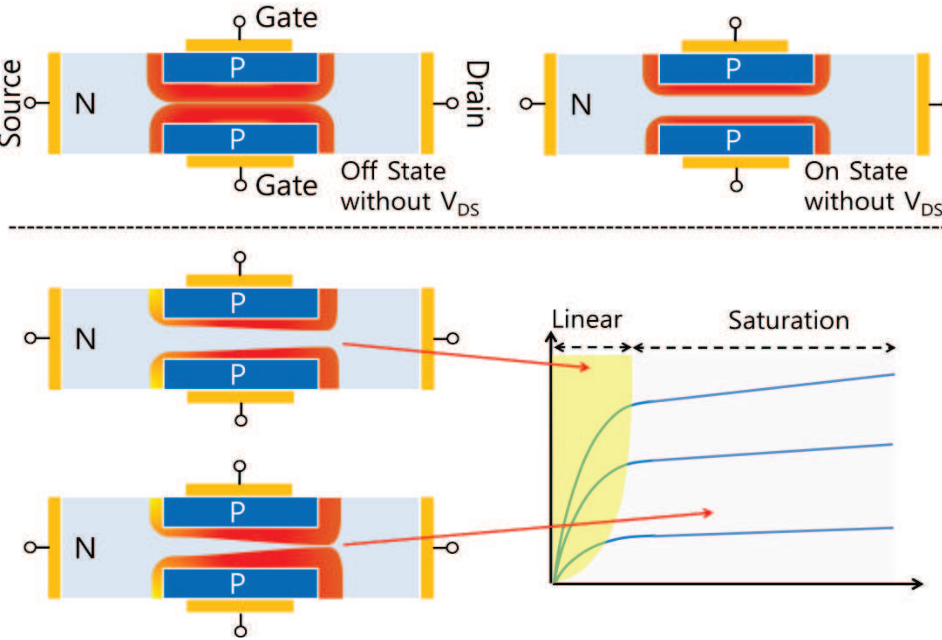


Figure 4.3.1 : Schematics of JFET device operation.

JFET is depletion mode transistor because the channel conducts with when V_G=0V. With a reverse bias the depletion width increases so that the channel conduction is interrupted. The channel conduction is similar to a resistor for the on-states with low V_{DS} (ohmic region). When the channel is pinched off by high V_{DS}, the conduction is limited by the drifted carrier and becomes a constant current. JFET has volume conduction. Differently from the surface conduction of conventional MOSFET, most of bulk is available for the conduction. Thus JFET has higher transconductance and lower noise than MOSFET.

4.3.1.2 Junctionless Nanowire FET

Based on the multi gate structure, junctionless FET (JLess FET) is recently studied for a new device concept to overcome short channel effects [62]. Meaning of 'junction' in JLess FET is different from JFET. Traditional MOSFETs are fabricated as a sandwich structure with $n^+ p\ n^+$ for NMOS and $p^+ n\ p^+$ for PMOS. In this case, current flows through the inversion channel between source and drain. Accumulation mode MOSFETs consist of n^+nn^+ for NMOS and p^+pp^+ for PMOS. However, in the case of accumulation mode MOSFET, channel has a high resistance due to the lightly doped channel region. High gate bias should be applied to drive an accumulation layer for the conduction channel.

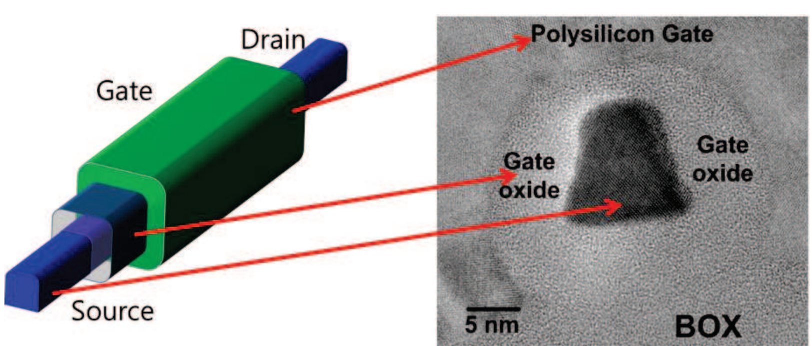


Figure 4.3.2 : Cross-section of JLess FET [63].

Basic structure of JLess FET is similar to the accumulation mode MOSFET. However, JLess FET has heavily doped channel (N^+ for n-channel device). Thus, JLess FET has no junction at the interface between channel and source / drain region. Device operation of JLess FET is rather similar to the JFET than accumulation mode MOSFETs. Depletion region formed by gate field limits the current flow in JLess FET. The most important fabrication issue of JLess FET is the formation of thin and narrow enough semiconductor layer to allow for full depletion of carriers when the device is off states. Thus, JLess FET has a nanowire structure as shown in Fig. 4.3.2 [63].

4.3.2 Transport of Junctionless Transistor

As we discussed, carrier transport of JLess FET is different from conventional MOSFETs. Apart from the operation modes, carrier transport of MOSFET is near channel surface.

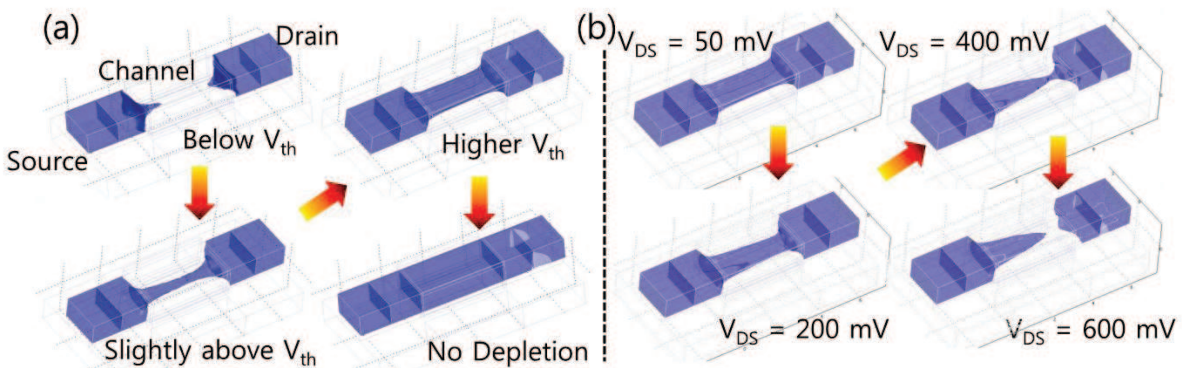


Figure 4.3.3 : Electron concentration contour plots in an n-type JLess FET [62, 64]. (a) Increased gate bias reduces depletion regions. (b) Drain bias increase the depletion region in the channel between gate and drain. Device operation scheme is same to JFET in Fig. 4.1.1.

The conduction channel of MOSFET is formed as very thin layer squeezed along the semiconductor / gate oxide interface by the electric field induced from the gate electrode [62]. During the transport, carriers can be trapped in the oxide or at the semiconductor interface. Carriers also can be scattered by surface roughness of channel interface as shown in the case of FinFET (chapter 4.1). As the device dimension decreases, carrier transport is more affected by surface roughness scattering. Both charge trapping and surface roughness scattering degrades carrier mobility and current.

Comparing to the MOSFETs, the biggest difference of JLess FET is volume conduction. In Fig. 4.3.3, carrier concentration of JLess FET is shown. When V_G is lower than V_{th}, the conduction channel of JLess FET is depleted by the difference of work function (Fig. 4.3.3 (a)). As V_G increased, the depletion region around the channel is reduced because forward biased gate-channel cancel out internal electric field of depletion region. It can operate as a gate controlled resistor. If the gate is fully opened, there is no depletion region in the channel. However it cannot gives infinite drain current. As shown in Fig. 4.3.3 (b), the depletion region increases in the channel between the drain-gate when V_{DS} is increased. Because of increased V_{DS}, potential difference between the gate and the drain decreases and the field effects induced by gate is canceled out. If the conduction channel is pinched off by depletion region near the drain, current becomes constant (saturation region). This operation scheme is very similar to JFET's one.

Carrier transport by volume conduction has advantages. The carrier transport of JLess FET is far from the semiconductor interface. As gate bias increased, conduction channel is formed from the inside to the outside channel. Thus, carrier trapping and surface roughness scattering is less than MOSFETs.

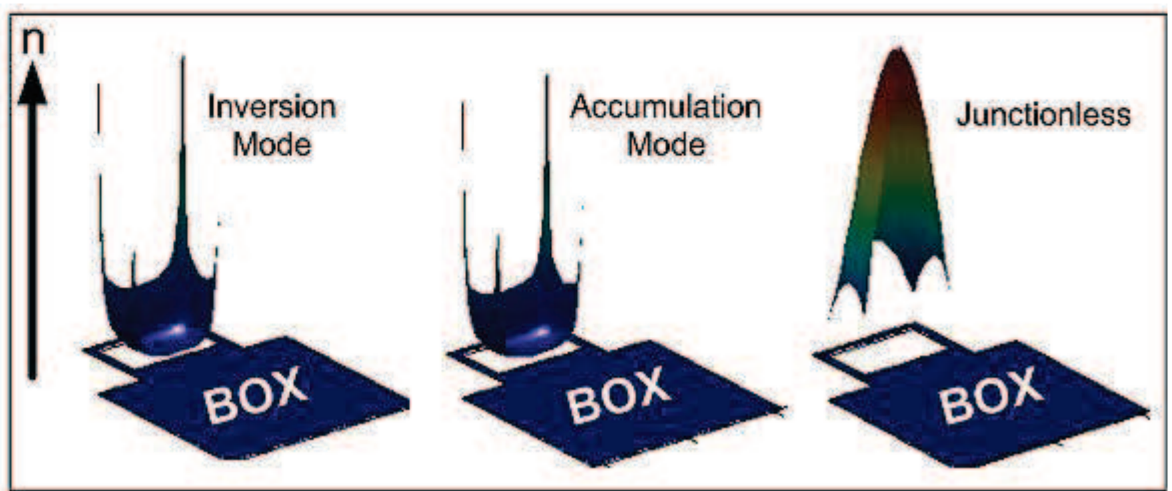


Figure 4.3.4 : Electron concentration profile above threshold in inversion mode MOSFET, accumulation mode MOSFET and JLess FET [64].

Jang et al. show that the volume trap density of JLess FET is in the range from 6×10^{16} to 3×10^{17} $cm^{-3}eV^{-1}$ from the low frequency noise measurement [65]. This value is similar to the volume trap density in typical bulk MOSFETs but much smaller than High-*k* MOSFET's (from 10^{19} to 10^{20} $cm^{-3}eV^{-1}$). Nazarov et al. characterize random telegraph noise (RTN) of JLess MOSFETs [66]. Smaller relative RTN amplitude in the current of JLess FET than in inversion-mode MOSFETs was observed. The average capture time of JLess FET into the trap in the gate insulator is longer than inversion mode MOSFETs due to the difference between volume and surface inversion conduction.

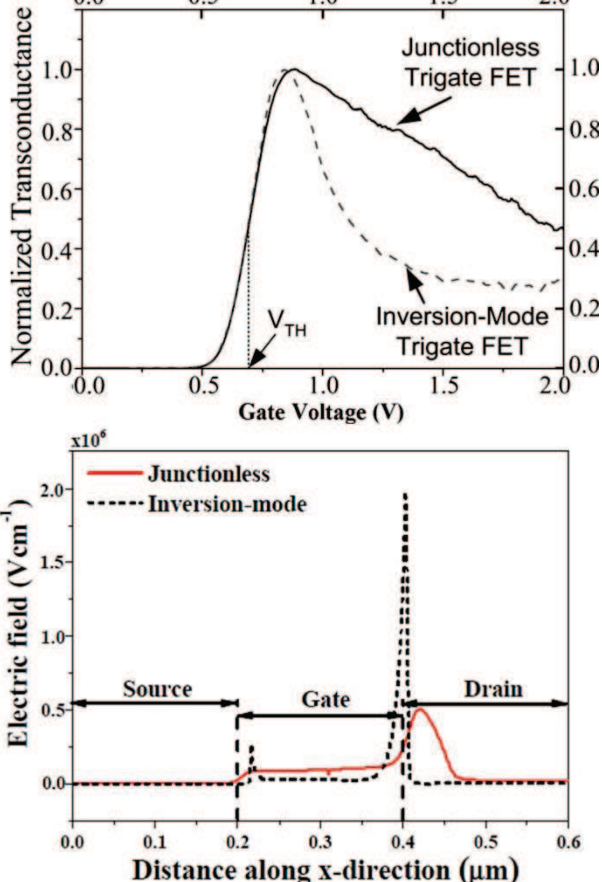


Figure 4.3.5 : (a) Normalized transconductance in inversion mode MOSFET and JLess FET [63]. (b) Simulation of electric field from source to drain [67].

As described in the definition of JLess FET, no junction interface exists between source / drain and channel. Drain current is purely blocked by that the depletion region pinches off heavily doped conduction channel. Thus drain potential drop is found 'inside' the drain [67, 68]. JLess FET has lower peak and

wider width of transversal electric field than inversion mode MOSFETs. Thus, impact ionization takes place in the drain region while it takes place in the channel near the drain in the inversion mode MOSFETs. V_{DS} to make sharp subthreshold swing is efficiently reduced in the JLess FET comparing to the inversion mode MOSFETs.

In the inversion mode or accumulation MOSFETs, the majority carrier concentration in the channel is peaked at the highest electric field region because higher gate electric field attracts more majority carriers. However in the case of JLess FET, the peak carrier concentration is at the lowest electric field region. The field is not quite equal to zero but much higher than inversion mode MOSFETs [63]. The mobility in the inversion mode MOSFETs at the high gate electric field decrease rapidly. In contrast, the decrease of mobility in JLess is much smaller because the carrier transport of JLess FET is less affected by longitudinal gate electric field. Thus JLess FET has an advantage in the current driven at the high gate electric field.

However, JLess FET has controvertible issues. For example, mobility in JLess FET is reduced by ionized impurity scattering [69]. Carrier effective mobility largely decreases as a function of channel doping concentration. Beyond the doping concentration of 10^{19}cm^{-3}, mobility degradation is not significant as below. However, the effective mobility of JLess FET is definitely lower than inversion mode MOSFETs as shown in Fig. 4.3.6 [69].

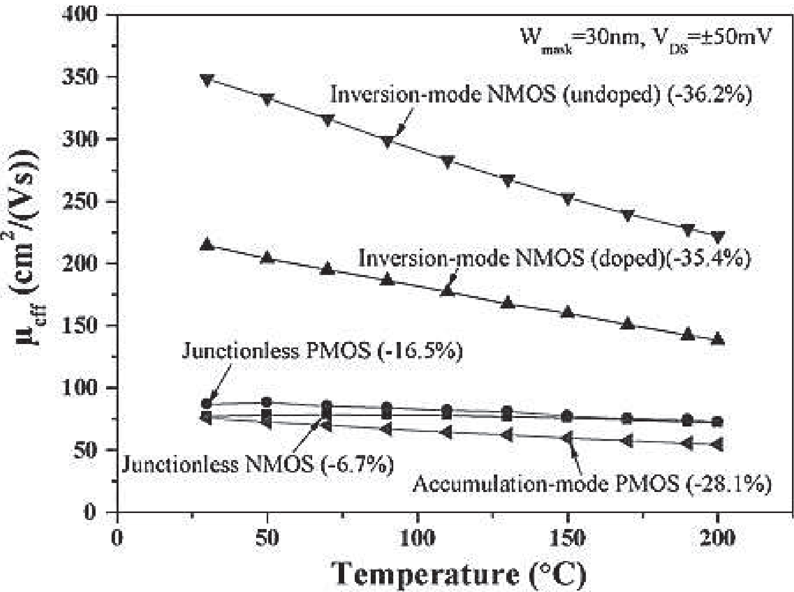


Figure 4.3.6 : Comparison of effective mobility in heavily doped JLess FETs and in the other tri-gate MOSFETs with doped and undoped channel conditions. [69].

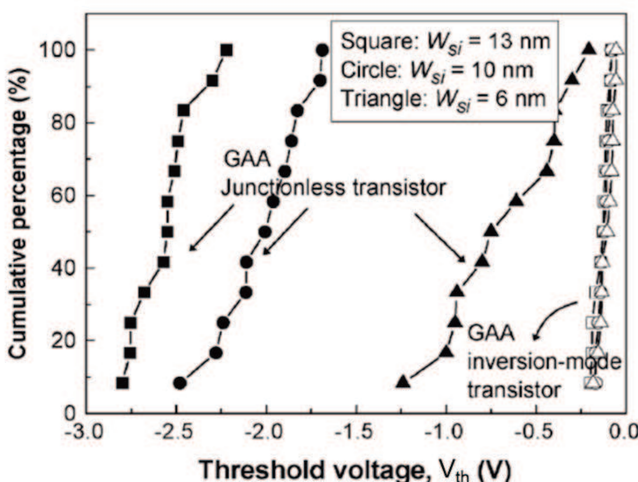


Figure 4.3.7 V_{th} distribution according to the channel width of JLess FETs. Comparing to inversion mode MOSFETs, Vth is largely varied depending on the channel width [70].

V_{th} of JLess FET depends on nanowire width. In the case of inversion mode GAA MOSFETs, there are two trends in the relationship between V_{th} and channel width [70]. When the channel is doped below 10^{19} cm^{-3}, V_{th} is not sensitive to the doping concentration. Additionally, if the channel width becomes thinner, the gate which surrounds the channel has better control of the channel potential and short channel effects and V_{th} is increased. However, when the channel is heavily doped above 10^{19} cm^{-3}, V_{th} increases with the increase of channel width and fluctuation of V_{th} becomes sensitive to the difference of the channel width. Because the JLess FET has heavily doped channel, V_{th} of JLess FET has sensitive channel width dependence.

4.3.3 Conclusion

As a solution of overcoming short channel effects, JLess FET was investigated in this chapter. Differently from inversion or accumulation mode MOSFETs, the device operation of JLess FET is close to JFET. From the volume conduction in the carrier transport, JLess FET has lots of advantages such as: (1) JLess FET is easier to manufacture; (2) it has reduced short-channel effects, drain-induced barrier lowering and subthreshold swing degradation with aggressive scaling down of feature size.; (3) it is expected to have a reduced degradation in carrier mobility at the high gate bias due to the reduced gate electric field; (4) it relax the requirements reducing gate dielectric

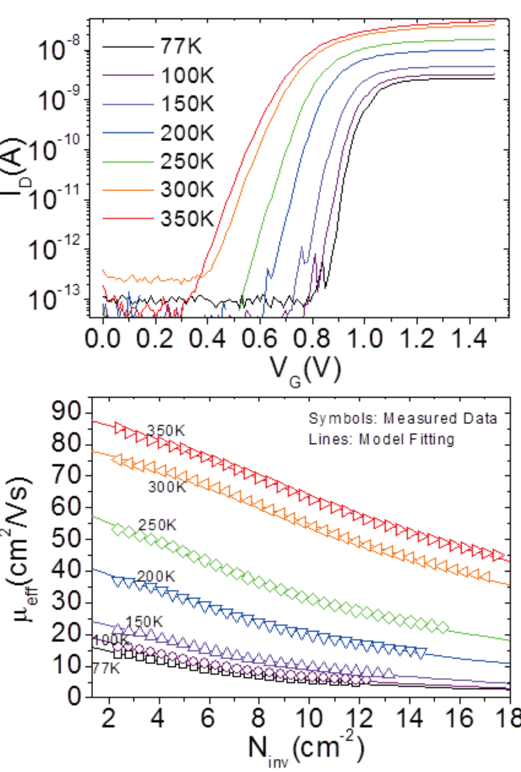


Figure 4.3.8 : I_D-V_G characteristics of JLess FET (up) and effective mobility depending on temperature. Impurity scattering behavior is shown in effective mobility.

thicknesses, competitively with inversion or accumulation mode MOSFETs [71]. However, many other open issues also remain. Effective mobility should be improved. Because JLess FET has heavily doped channel, impurity scattering mainly limits effective mobility. JLess FET is also sensitive to the channel geometry. The variability of V_{th} is one of the further works to be solved.

As a new device concept, JLess FET is very interesting and promising research topic in the device physics.

4.4 Si Nanowire Sensor – Low Frequency Noise and Sensing Limitation

4.4.1 Overview: Nanowire for Sensor Application

Currently nano materials are attracting more interest for their practical applications based on the advantages of their small dimension. Among them, silicon nanowires have the advantage, that Si is a well understood material based on its longstanding use in semiconductor technology. Silicon nanowires can be fabricated either by the bottom-up [72, 73] or top-down approaches [74-76].

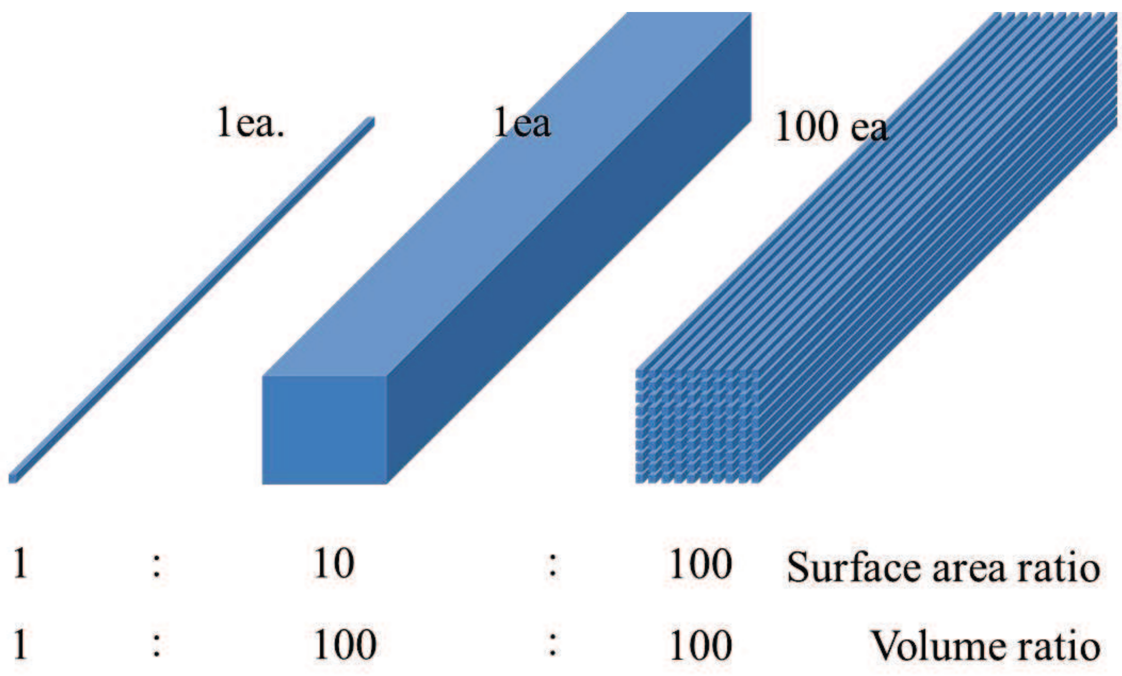


Figure 4.4.1 : Surface area and Volume ratio of nanowire. As scale down, surface area in the same volume is increased.

In recent years, many research papers about silicon nanowire-based chemical or biosensors have been published [77-80]. For instance, among many other examples, Lieber's group reported on functionalized nanowires that could detect cancer biomarkers [81]. Electrically addressable integrated nanowire sensor chips have been developed and showing a great possibility for the mass production. Device modeling, prior to the fabrication, can save time and experimental trial-and-errors by providing a starting design that can be better optimized in terms of sensing performance. The modeling and the simulation of nanowire sensors have

been the subject of many recent publications, with detailed account of the role of electrostatic mechanisms on the sensitivity [82-85]. However, to the best of our knowledge, noise issues have not been discussed, while the low-frequency noise associated to trapping-detrapping of carriers (i.e. generation-recombination, G-R) in the nanowire can put a severe limit to the sensitivity, due to the SNR (Signal to Noise Ratio) degradation it induces.

It is the aim of this chapter to discuss the trade-off between the sensitivity and the SNR in nanowire sensors. This imposes to use the same modeling framework for both issues. This framework was chosen simple enough to allow a fast evaluation of the design trends, but complete enough to include the main effects.

4.4.2 Simulation Environment and Conditions.

The sensitivity of the nanowire was first calculated as a function of the geometrical design of the nanowire (dimensions and doping level) and was compared to a simple analytical model. Compared to most previous approaches, the thickness of the passivation oxide layer and the field effect mobility degradation were taken into account.

For the sake of analytical calculation, the external charge attached around the silicon nanowire was assumed homogeneous. The conductance variation and the charge sensitivity of the silicon nanowire sensor were obtained by solving Poisson equation across a two-dimensional section of the nanowire and coupling it to the Drift-Diffusion equation. This was done numerically using FlexPDE 5. FlexPDE 5 is the software solving partial differential equations with a finite element method. An external homogeneous charge density N_{ext} (cm^{-2}), surrounding the passivation layer of silicon dioxide was used for simplification.

The conductance of the nanowire was calculated for the various geometries of silicon nanowire (length L, radius r_{si}) with nominal values of doping concentration ($N_d=10^{18}$ cm^{-3}) and the thickness of the silicon oxide layer (t_{ox}=2nm) at room temperature (T=300K). The results for the n-type silicon nanowires can be applied to the p-type in the same way with the proper choice of carrier mobility with a reversed sign. All the simulations were assumed at room temperature (300K).

4.4.3 Sensitivity Estimation: Numerical Simulation and Analytical Model

In the simulation, the carrier mobility has been considered either as constant throughout the nanowire section (solid lines in Fig. 4.4.2) or degraded by the radial electric field E_r induced by the external charge (doted lines in Fig. 4.4.2). We used the standard equation of the mobility degradation $\mu=\mu_0/(1+E_r/E_c)$, where μ_0 is the low field mobility and E_c a critical field ($\approx 10^5$V/cm for silicon devices) [86]. Figure 4.4.2 (a) shows the normalized conductance change ($\Delta G/G_0$), as a function of the adsorbed charge density N_{ext} (cm^{-2}) at the surface of nanowires depending on the radius of nanowires. As expected, the conductance change increases with a positive N_{ext} values as n-type silicon nanowire due to a stronger accumulation of majority carrier in the n-type silicon nanowires. On the contrary, for negative N_{ext} values, the conductance change is negligible owing to the formation of the inversion regime where the hole charge dominates.

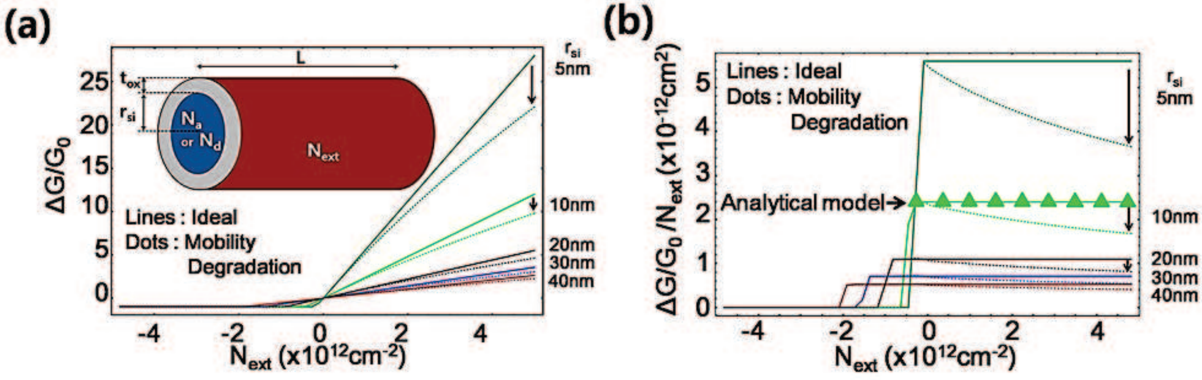


Figure 4.4.2 : (a) Normalized conductance variation ($\Delta G/G_0$) for the constant mobility or the mobility degradation. The inset shows the schematic geometry of the silicon nanowire sensor. The external charge, added by target molecules, is represented by a uniform charge areal density N_{ext} (cm^{-2}). (b) Sensitivity of the silicon nanowire sensor. Solid lines and dotted lines show the numerical simulation results. Triangles are obtained from the analytic model of Eq. (4.4.4) when r_{si}=10nm and t_{ox}=2nm.

It is important to note that we define the sensitivity of the nanowire sensor as the ratio between the conductance change $\Delta G/G_0$ (the output) and the external density of charge N_{ext} (the input). Figure 4.4.2 (b) clearly indicates that the sensitivity can be enhanced in the close-to-neutrality and the accumulation regions of the operation with a smaller cross section nanowire. This means that both p-type and n-type silicon nanowires are required for probing the positive and the negative external charges with a high sensitivity. It should be noted that the mobility degradation at high field i.e. large external charge densities will reduce the

nanowire sensitivity of nanowire sensors and, in turn, alter the linear response of the charge sensor, which can explain the nonlinear sensitivity reported in the previous literatures [79, 83, 87].

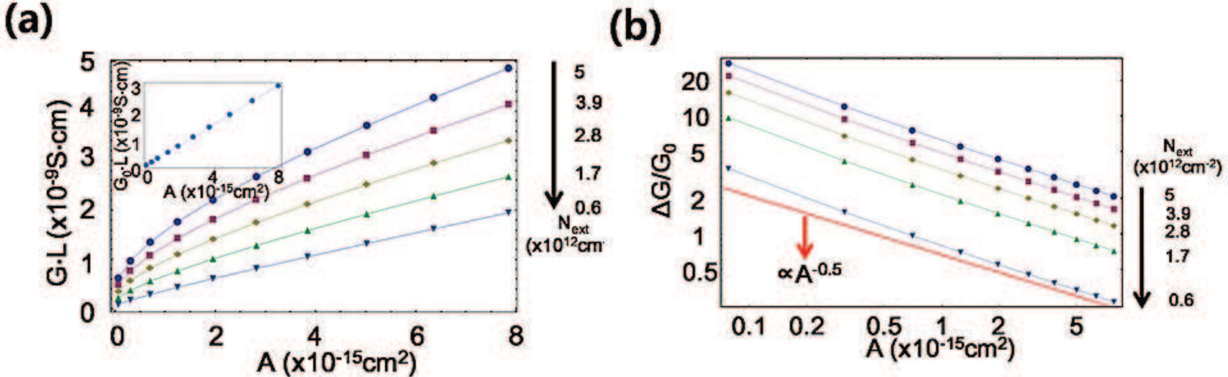


Figure 4.4.3 : (a) Conductance nonlinearly depending on the cross section area (A) of the silicon nanowire. On the other hand, the initial conductance G_0 is proportional to A. (Inset) (b) $\Delta G/G_0$ variation as a function of nanowire area A. Deviation from the general $A^{-0.5}$ trend is noticeable, attributed to the influence of t_{ox}.

Figure 4.4.3 plots the conductance G·L and the normalized conductance $\Delta G/G_0$, as a function of the cross-section area A. $\Delta G/G_0$ varies almost following $1/A^{0.5}$ except for the small areas below 10^{-15} cm^2 as in Fig. 4.4.3 (b). In order to interpret these simulation results, we have derived an analytical model of the conductance of silicon nanowires as following. The nominal conductance of the silicon nanowire will be given under the charge neutrality condition:

$$G_0 = \frac{q\mu}{L^2}\pi r_{si}^{\ 2} N_d L = \frac{q\mu N}{L^2}\ , \tag{4.4.1}$$

where q is the electric unit charge ($1.6\text{x}10^{-19}$ C), N_d the doping concentration of the silicon nanowire (cm^{-3}), N the total number of carriers in the nanowire. By considering the global charge neutrality in the structure, the absolute change of charge induced by the total external charge on the carrier number in the nanowire is given by

$$\Delta N = 2\pi (r_{si} + t_{ox}) N_{ext} L\ . \tag{4.4.2}$$

Assuming a constant mobility in the 1st order, the conductance change reads:

$$\Delta G = \frac{q\mu}{L^2}\Delta N\ , \tag{4.4.3}$$

yielding,

$$\left.\frac{\Delta G}{G_0}\right|_{ext} = \frac{2(r_{si}+t_{ox})N_{ext}}{r_{si}^2 N_d} \quad . \tag{4.4.4}$$

Equation 4.4.4 explains the sensitivity plot depending on the square root of the cross-section area of the nanowire for $r_{si}>>t_{ox}$ (Fig. 4.4.2 (b) and Fig. 4.4.3 (b)), whereas it should increase as 1/A for very small cross-section. Equation 4.4.4 also indicates that the reduction of the doping concentration can increase the nanowire sensitivity, enabling the optimized design of the nanowire sensor.

4.4.4 Low Frequency Noise in Nanowire Sensor

The sensitivity of nanowire sensor can be limited by the low frequency noise arising from the random trapping-detrapping (G-R) of carriers into traps, of areal density N_{it} (cm^{-2}), located at the Si/SiO_2 interface [88, 89]. The random fluctuations of the number of the total interface charges, N_{trap}, give rise to random fluctuations in carrier number, resulting in the conductance fluctuation of nanowires. This might limit the sensitivity of the detection. The power spectral density (PSD) associated with charge traps at the interface can be written as: [90, 91]

$$S_{Ntrap}(f) = \frac{4\langle \Delta N_{trap}^2 \rangle \tau}{1+(2\pi\tau f)^2} \ , \tag{4.4.5}$$

where $<\Delta N_{trap}^2>$ is the variance of the total number of the interface trap charges and τ the trapping time constant. For the interface traps obeying the distribution of Poisson's law [90, 91], the variance is simply equal to the mean value of the total number of the interface trap charge:

$$\langle \Delta N_{trap}^2 \rangle = \int_0^\infty df \ S_{Ntrap}(f) = \langle N_{trap} \rangle = 2\pi r_{si} N_{it} L \ . \tag{4.4.6}$$

The condition of global charge neutrality, i.e. $\Delta N = \Delta N_{trap}$, enables the PSD and the total variance of the conductance to be derived from Eqs (3)-(6) as,

$$S_G(f) = \frac{q^2\mu^2}{L^4} S_{Ntrap}(f) \tag{4.4.7}$$

and

$$\left.\frac{\langle \Delta G^2 \rangle}{{G_0}^2}\right|_{Noise} = \frac{2N_{it}}{\pi {r_{si}}^3 {N_d}^2 L} \,. \tag{4.4.8}$$

To guarantee the charge detection, the conductance variation due to the external charge must be higher than its random fluctuation due to the trapping-detrapping noise i.e.

$$\left.\frac{\Delta G}{G_0}\right|_{ext} > \sqrt{\left.\frac{\langle \Delta G^2 \rangle}{{G_0}^2}\right|_{Noise}} \,. \tag{4.4.9}$$

Equations 4.4.8 and 4.4.9 allow the definition of the sensitivity threshold for detecting the external charges, N_{ext_th} as:

$$N_{ext_th} = \frac{1}{r_{si} + t_{ox}} \sqrt{\frac{N_{it} r_{si}}{2\pi L}} \,. \tag{4.4.10}$$

It should be noted that the charge detection threshold N_{ext_th} depends on geometrical parameters and on the interface trap density N_{it}, but is independent of doping concentration.

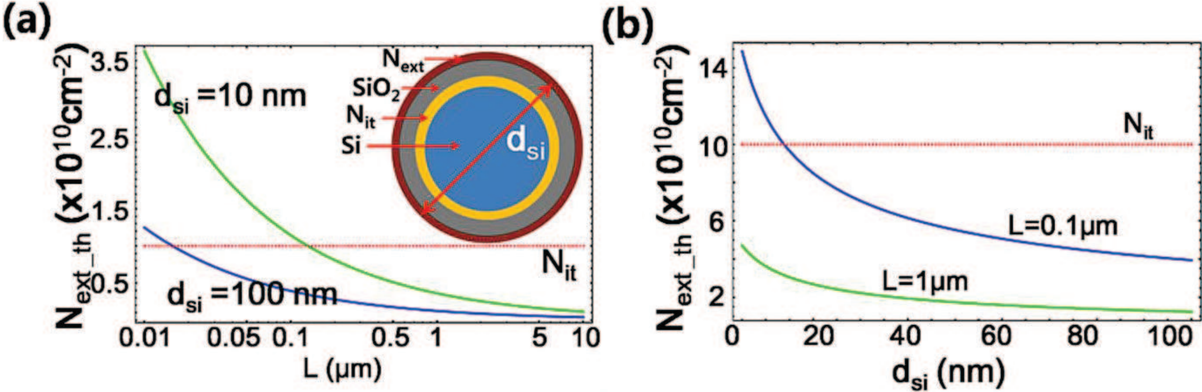


Figure 4.4.4 : Sensing threshold density as a function of (a) the length L and (b) the diameter d_{si} of the silicon nanowire; the other parameter being set to be constant value. In order to be detectable, the external charge density must be higher than the sensing threshold density.

Figure 4.4.4 shows the geometric dependence of the sensing threshold N_{ext_th} for a given interface trap density $N_{it}=10^{10}$ cm^{-2}. As can be seen, N_{ext_th} decreases typically as the square root of diameter d_{si} and the length L of the silicon nanowire, indicating that the low frequency

noise limitation can be overcome by scaling up the active area of the sensor, $2\pi(r_{si}+t_{ox})L$. This could be achieved by increasing the diameter or the length of the nanowire, but at the expense of sensor sensitivity and of nominal nanowire conductance G_0. The only remaining parameter of the nanowire sensor for the optimization is then the doping concentration, which can be chosen for a tradeoff between sensitivity and nominal conductance values. In addition, it is worth noting that an external charge density lower than N_{it} can be detected, because the fluctuations of the interface trap scales as the square root of N_{it} in Eq. 4.4.10.

The detection limit of a single external charge can also be addressed using Eqs 4.4.1 and 4.4.3. To this end, one can calculate the conductance change due to one elementary charge variation i.e. ΔN=1, yielding,

$$\left.\frac{\Delta G}{G_0}\right|_{single} = \frac{1}{\pi r_{si}^2 N_d L}. \qquad (4.4.11)$$

To be detectable over the trapping noise fluctuations, this initial conductance should be larger than the square root of the conductance variance (Eq. 4.4.9), which leads, after simplification, to the condition: $N_{it}<1/(2\pi r_{si}L)$. Interestingly, this means that the detection of a single external charge is only possible if the interface trap density N_{it} is sufficiently low i.e. lower in average than one trap per active surface of the nanowire.

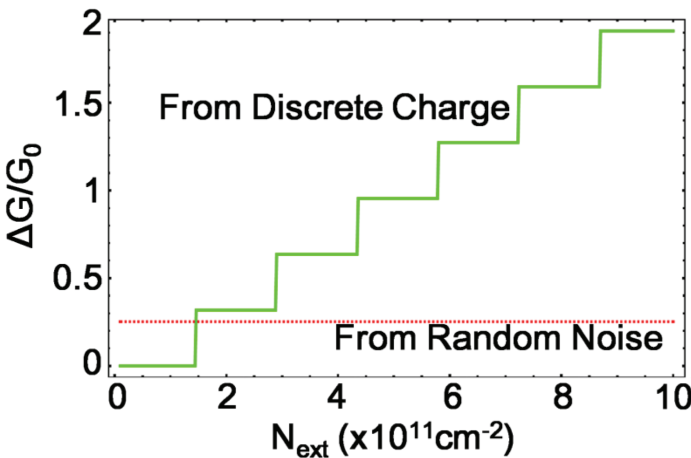


Figure 4.4.5 : $\Delta G/G_0$ variation from the discrete charge detection and the random noise fluctuation. The charge which makes the variation below 2.5 cannot be sensed.

As an illustration of single charge detection, the conductance variation has been evaluated with Eq. 4.4.4 for integer values of $\Delta N = 2\pi(r_{si}+t_{ox})N_{ext}L$ after setting the nanowire parameters: L=0.1μm, d_{si} =20 nm, t_{ox} =1 nm, N_d = 10^{17} cm^{-3} and N_{it} = 10^{10} cm^{-2} (see Fig.

4.4.5). For this geometry, one single charge corresponds to a step in the external charge density, $N_{extSingle}$=1.32x10^{10} cm^{-2}, and, to a conductance change $\Delta G/G_0$ of 0.32. The random noise detection limit for the conductance is given by 0.25, indicating the possibility of the detection of a single charge variation. In other words, the detection is possible because once averaged over the nanowire area, a single charge yields a charge density $N_{extSingle}$ larger than the interface trap density N_{it}.

4.4.5 Conclusion

In summary, by means of simulation and analytical calculation, the charge sensitivity of silicon nanowire sensors was evaluated as well as their detection limit due to the low frequency trapping noise. Not only from the extrinsic noise, but also intrinsic noise can be a limitation of sensor performance. The principle and the limitation of single charge detection have also been discussed in this chapter. It depends on the fabrication condition and geometrical parameters. Thus in the same process condition, device simulation should be performed before the fabrication to avoid the limiting sensor by intrinsic low frequency noise. The engineering of the sensitive nanowire sensor can be possible by tuning the doping concentration and the diameter of nanowire.

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5. Device Simulation

5. Device Simulation

5.1 Overview: Types of Simulation

5.2 Simulation of Quasi 1D Nanowire Devices

5.2.1 Finite Difference Method

5.2.2 Simulations in Specific 1D Systems:
Variable Range Hopping in Disordered System

5.2.3 Practical Device Simulation

5.3 Other Device Simulations: OLED and E-paper

5.3.1 Monte Carlo Method

5.3.2 Device Simulations: OLED and E-paper

5.4 Conclusion

Chapter 5

Device Simulation

5.1 Overview: Types of Simulation

During several tens of years, semiconductor devices have been enormously innovated. Not only for the feature size, but the type of semiconductor devices also enlarge. As time goes by, various device structures require more complicated manufacturing processes. Cost of experiment is increasing as process equipment becomes more expensive. Thus a pure trial-and-error approach to the optimization of device performance becomes time consuming and expensive. For a practical alternative, a computer simulation becomes an essential tool for the device engineering. In electrical engineering technology computer aided design (TCAD) and electronic design automation (EDA or ECAD) are the most widely used simulation tools. TCAD models semiconductor fabrication and device operation.

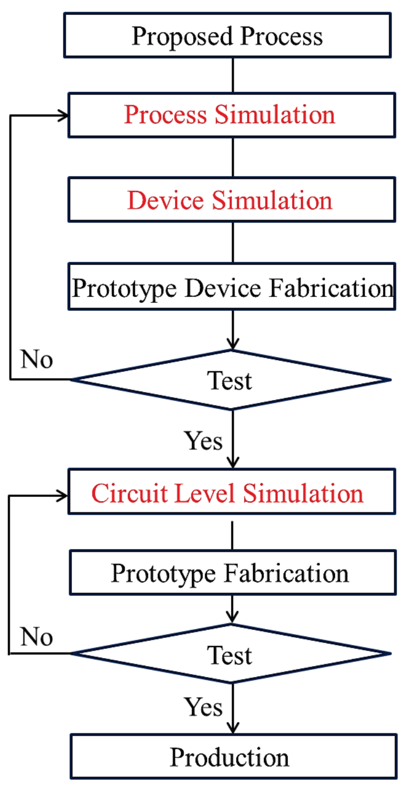


Figure 5.1 : Device fabrication flow.

ATHENA serviced by SILVACO is a famous process TCAD simulator [1]. Process simulator supports virtual fabrication of device according to the given process flow. For considerable parameters, it includes most of fabrication process such as material growth, oxidation, diffusion, etching and metal deposition etc. Depends on the simulator 1D cross-section, 2D or 3D structure can be fabricated and compared. Process simulation is necessary to reduce the cost of development and the period of process development and to enhance the yield.

As an example of device TCAD simulator, Sentaurus Device serviced by SYNOPSYS can

Approach	Model	Improvements
Semi-classical approach	Compact models	Appropriate for circuit design
	Drift-Diffusion equations	Good for devices down to 0.5 μm, include μ(**E**)
	Hydrodynamic equations	Velocity overshoot effect can be treated properly
	Boltzmann transport equation Monte Carlo/CA methods	Accurate up to the classical limits
Quantum approaches	Quantum hydrodynamics	Keep all classical hydrodynamic features + quantum corrections
	Quantum Monte Carlo/CA methods	Keep all classical features + quantum corrections
	Quantum-kinetic equation (Liouville, Wigner-Boltzmann)	Accurate up to single particle description
	Green's functions method	Includes correlations in both space and time domain
	Direct solution of the *n*-body Schrödinger equation	Can be solved only for small number of particles

Figure 5.2 : Hierarchy of transport models [4].

make simulations of electrical, thermal and optical characteristics of devices [2]. Process simulation supports the first step in overall simulation. It can provide the detailed physical structure and the dopant profile of device before device simulation. Thus the output of process TCAD is usually available for the starting point of device TCAD. Using device TCAD, device performances for the prototype device can be estimated. It can supplement experimental data with deep physical insight and shorten development time. Coupling of process and device TCAD enhance the ability to optimize the device performance and process sequences.

Simulation Program with Integrated Circuit Emphasis (SPICE) simulation is indispensible for the device integration. SPICE used for the designing electronic systems like integrated circuits and printed circuit boards. EDA support not only the design but also the circuit simulations. DC/AC, transfer curve, noise etc. can be analyzed using EDA tools.

All of simulation requires models. In the process simulations, physical models of diffusion, oxidation, ion implantation, thin film deposition and etching etc. are necessary. For example, Deal-Grove model is used for the oxidation. In the device simulations, lots of models exist depending on the device structures, materials and the output which we want to observe. At the beginning of semiconductor industry, simple analytical models based on the drift-diffusion model were used to estimate the device transport characteristics [3]. It includes simplified doping profiles and device geometry [4]. However, nowadays drift-diffusion model is not enough because the scaled down device require quantum physics to estimate their properties. Thus other models such as quantum Monte Carlo method or Green's function method have been studied to overcome the limitation of drift-diffusion model.

In this chapter, device simulation of quasi 1D nanowire structures and other devices will be

shown. Simulation examples of Si nanowire, FinFET, OLED, E-paper will be introduced.

5.2 Simulation of Quasi 1D Nanowire Devices

5.2.1 Finite Difference Method

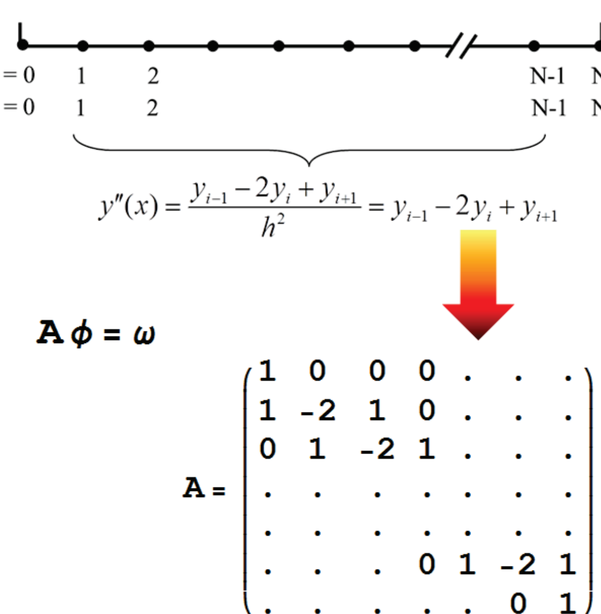


Figure 5.3 : Simplified 1D 2nd order differentiation.

Lots of simulation models such as Poisson's equation or Schrödinger equation are based on partial differential equations. Solving a partial differential equation can be carried out using numerical analysis. Analytical solution is difficult to find in the complex system so that the simple approximation and numerical method is necessary to reduce the running time of simulation and hardware resource. To understand numerical method easily, let's guess an 1D continuous system which has a certain model *f(x)*. Then, divide the continuous 1D system by finite number of N. Discreteness of system is the first approximation of finite difference method. From this approximation, differential equation can be changed to 'difference' equation. According to the definition, 2nd order differentiation can be written as:

$$f'' = \frac{f'_{i+1} - f'_i}{x_{i+1} - x_i} = \left(\frac{f_{i+1} - f_i}{x_{i+1} - x_i} - \frac{f_i - f_{i-1}}{x_{i+1} - x_i} \right) \Big/ \left(x_{i+1} - x_i \right) = \frac{f_{i+1} - 2f_i + f_{i-1}}{\left(x_{i+1} - x_i \right)^2}, \quad (5.1)$$

where i is index of 1D discrete coordinate. Especially, when the distance between discrete x is 1, it can be simplified as $f_{i+1}-2f_i+f_{i-1}$. Eventually, this system can be described as a linear algebra matrix.

Now previous method can be applied in 2D system. Let's see how to solve Poisson's Equation using this method. Poisson's equation is 2nd order differential equation describing the relationship between the electric potential (or field) and charge in closed system. It can be

written as :

$$\nabla \cdot E = \nabla^2 V = -\frac{\rho}{\varepsilon}, \tag{5.2}$$

where E is the electric field, V the electric potential, ρ the charge density and ε the permittivity. From Eq. 5.1, 1D Poisson's equation can be described as :

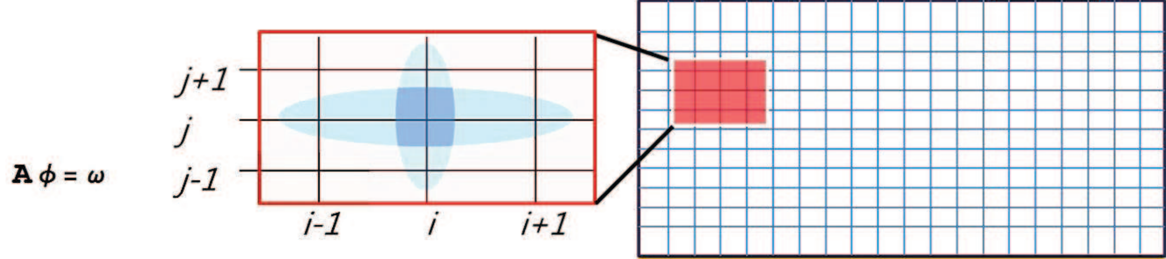
$$\frac{V_{i+1} - 2V_i + V_{i-1}}{\Delta x^2} = -\frac{\rho_i}{\varepsilon}. \tag{5.3}$$

With the geometrical index (i, j) and Eq. 5.3, Poisson's equation in 2D system is:

$$\frac{V_{i+1,j} - 2V_{i,j} + V_{i-1,j}}{\Delta x^2} + \frac{V_{i,j+1} - 2V_{i,j} + V_{i,j-1}}{\Delta y^2} = -\frac{\rho_{i,j}}{\varepsilon}. \tag{5.4}$$

If the difference of distance in x and y axis is same (it will be described as Δ), Eq.5.4 can be:

$$\frac{1}{4}\left(V_{i+1,j} + V_{i-1,j} + V_{i,j+1} + V_{i,j-1} - \frac{\rho_{i,j}}{\varepsilon}\Delta^2 \right) = V_{i,j} \tag{5.5}$$



$$A = \begin{pmatrix} T & B & 0 & 0 & \cdot & \cdot & \cdot \\ B & T & B & 0 & \cdot & \cdot & \cdot \\ 0 & B & T & B & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & 0 & T & B \\ \cdot & \cdot & \cdot & \cdot & 0 & B & T \end{pmatrix} \quad T = \begin{pmatrix} -4 & 0 & 0 & 0 & \cdot & \cdot & \cdot \\ 1 & -4 & 1 & 0 & \cdot & \cdot & \cdot \\ 0 & 1 & -4 & 1 & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & 0 & 1 & -4 & 1 \\ \cdot & \cdot & \cdot & \cdot & \cdot & 0 & 1 \end{pmatrix}, \quad B = \begin{pmatrix} 1 & 0 & 0 & 0 & \cdot & \cdot & \cdot \\ 0 & 1 & 0 & 0 & \cdot & \cdot & \cdot \\ 0 & 0 & 1 & 0 & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & 0 & 1 & 0 \\ \cdot & \cdot & \cdot & \cdot & 0 & 0 & 1 \end{pmatrix}$$

Figure 5.4 : 2D system and 2nd order differential equation matrix.

The meaning of Eq. 5.5 is that $V_{i,j}$ is related to the average of values of neighbor. Finally differential equation becomes eigenvector problem. Using Gauss-Seidel method or successive over-relaxation method results in fast convergence for the solution in the iterative process [5].

From these approach, the electric field, potential, charge distribution can be estimated in a given system. As we can see in the previous paragraph, properties are calculated according to the variations and values at neighbor nodes. For the simulation, grid generation is one of the most important tasks.

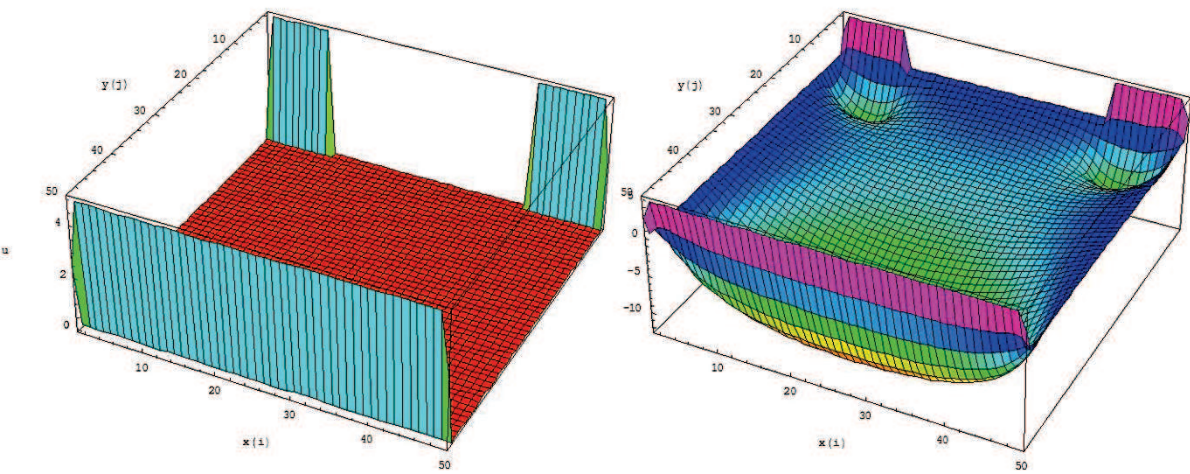


Figure 5.5 : Example of Potential distribution simulation. 2D system in Fig. 5.4 was used. Simulation was carried out using Mathematica 6.

The grid should be fine enough to reflect interests of neighbors. The grid spacing depends on the geometrical properties of devices. Non-uniformly spaced grids are used in most of practical simulations. Near the edges of device or junction interfaces, the grid should be dense for the precise calculation. However as a trade-off of calculation accuracy, simulation time is increased because the increase of the matrix dimension makes the calculation difficult. Depending on the simulator, the grid is refined in regions where the parameters change rapidly. It can make the effective simulation which save the running time and give enough accuracy.

5.2.2 Simulations in Specific 1D Systems: Variable Range Hopping in Disordered System

For an example of simulation, the conduction of 1D system with localized states in low temperature was calculated. Currently many semiconductor industries have been developing the device on the transparent substrate such as glass or flexible polymer [6, 7]. In this case the fabrication of single crystalline device is very difficult. Thus amorphous Si and organic materials have been studied for alternatives of single crystalline on the glass or flexible

polymer substrate. At the grain boundary of non-single crystalline materials, localized states exist.

Variable range hopping (or Mott variable range hopping) is a model which describes the conduction of strongly disordered system in low temperature [8]. The probability of hopping with optimum hopping distance r between two states is [9]:

$$P \approx \exp\left(-2\frac{r}{a} - \frac{\Delta E}{k_B T}\right), \tag{5.6}$$

where a is the localization length, k_B the Boltzmann constant and ΔE is the activation energy.

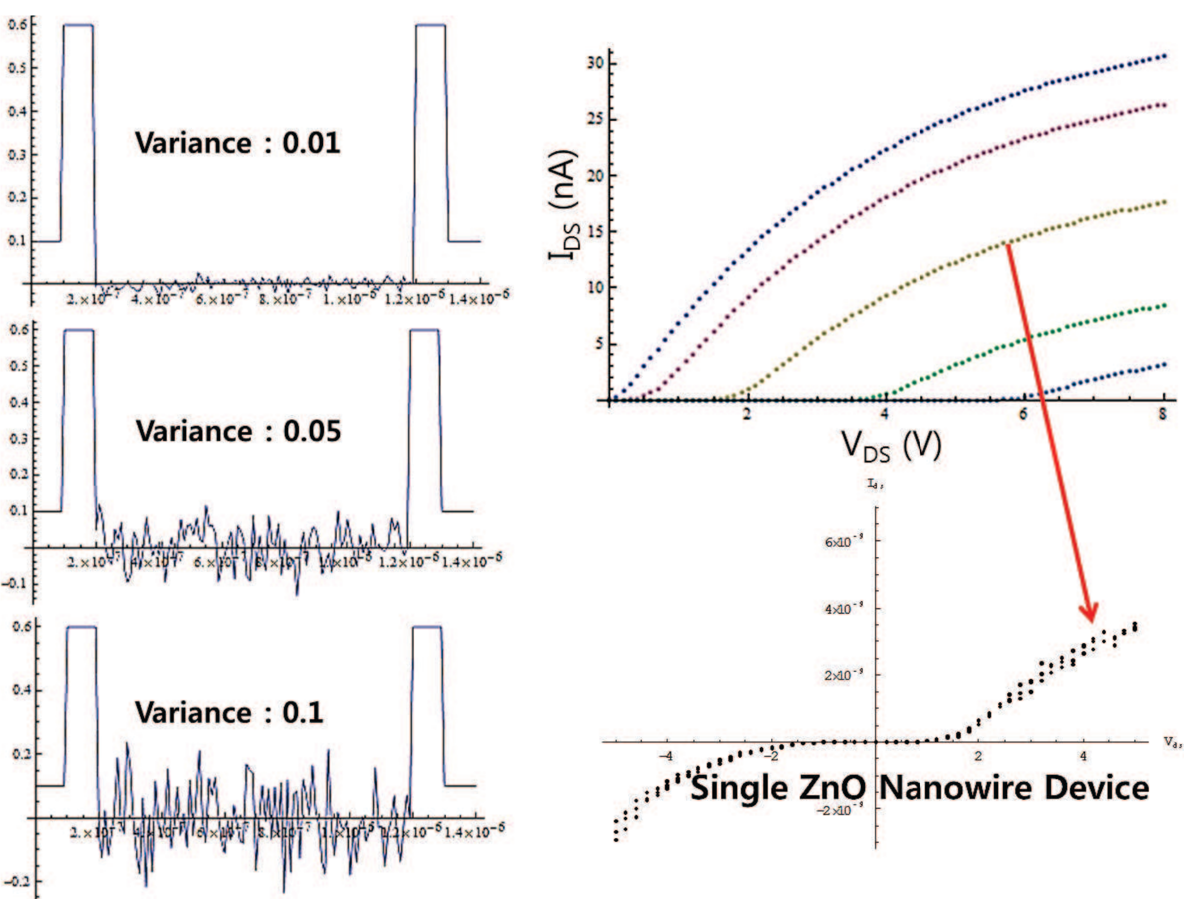


Figure 5.6 : Random energy states in the double barrier problem (left). Gaussian random was used. Shape of estimated current is similar to the nanowire device I-V characteristic.

When the hopping distance is further, carriers have low probability for the hopping event. This is same for the energy states. Lower energy difference between two states gives higher hopping probability. These schemes are available with following calculation process 1) initialization: the definition of 1D disordered system, 2) calculation of transfer matrix and 3)

iteration for the probability calculation. Simple 1D disordered structure was defined in the simulation. For the randomness of disordered energy states, variance of channel energy state was given for the variable with Gaussian random distribution.

From 1D numerical analysis explained in previous section, the hopping probability was calculated. When drain bias V_{DS}, is given, energy band diagram is changed. From the changed band diagram, hopping probability is changed. Injected carriers hop forward and back and arrived carriers in drain region are counted to calculate current.

This simulation gives a clue of the transport of nanowire structure. Previously, bottom-up grown nanowire structure has been explained using back-to-back diode model which considers only contact barriers [10, 11]. However, with variable range hopping model, device simulation with channel disorder becomes possible.

5.2.3 Practical Device Simulation

As we discussed before, device dimension becomes shrunken close to 1D structure. Currently, lots of nanowire devices are developed and studied for the alternative of planar devices. Device simulation of these devices gives us the considerable parameters and device operation scheme.

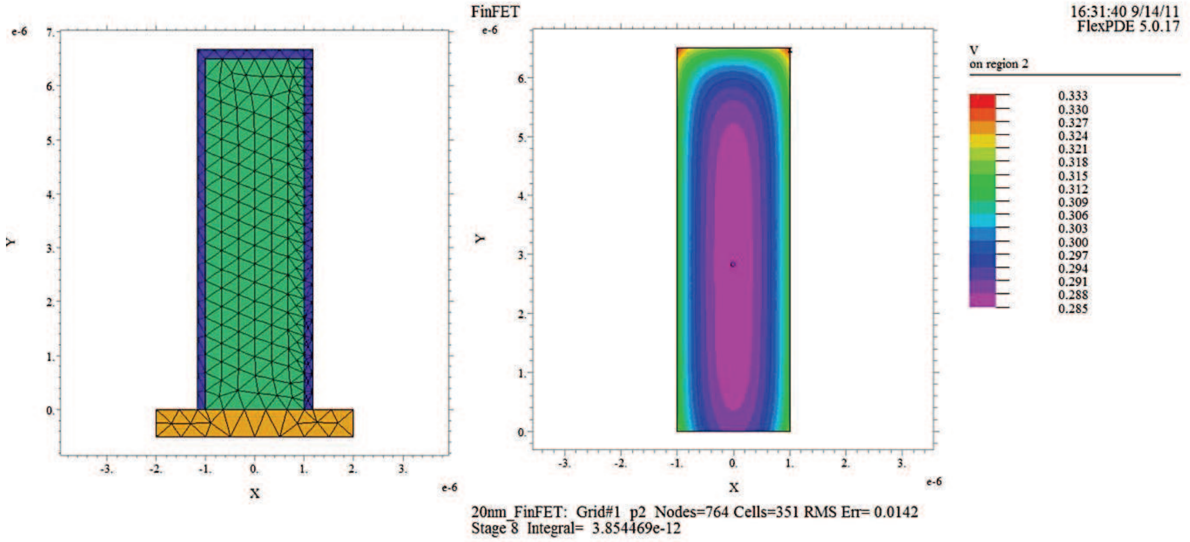


Figure 5.7 : Grid structure for FinFET simulation (left) and simulated potential distribution at V_G=0.4 V (right).

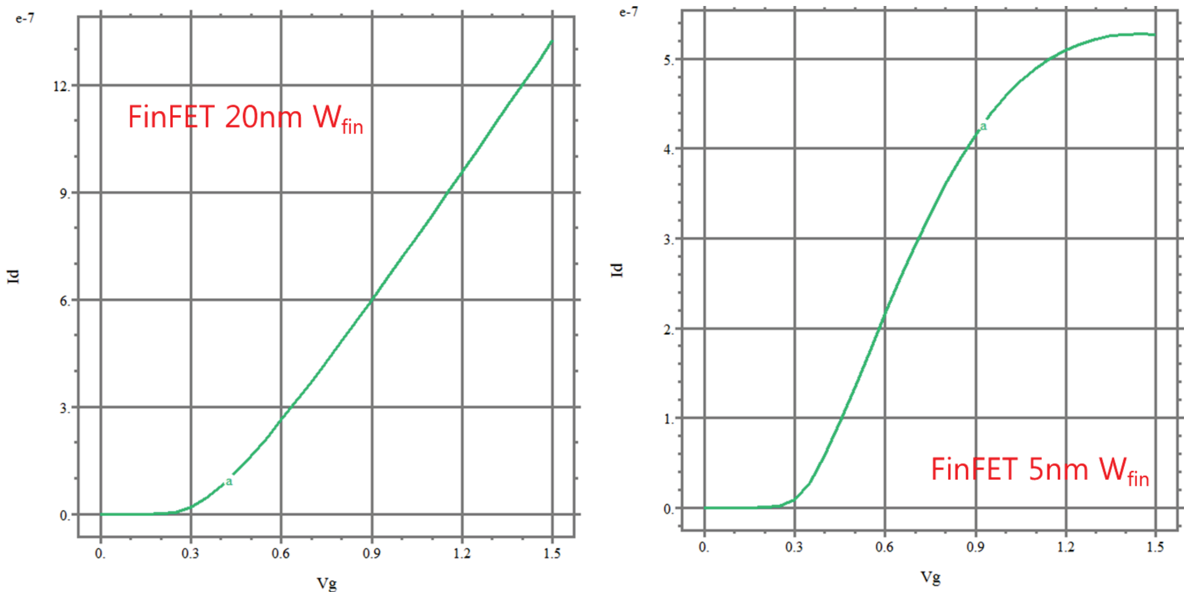


Figure 5.8 : I_D-V_G characteristic Comparison of FinFETs. 5 nm W_{fin} show current degradation at high gate bias (right) while 20 nm Wfin has linear I_D-V_G behavior.

Mobility analysis of FinFET has been discussed in chapter 4.1. For the study of FinFET, FlexPDE was used. Design of SOI FinFET fabricated by IMEC was similarly programmed in the software as shown in Fig. 5.7. Surface roughness scattering factor was considered as a variable for the mobility model [12]. Without surface roughness consideration, I_D-V_G characteristic does not have any current degradation. Before the simulation, the result of measurement shows the current degradation at high gate bias with narrow FinFET. With the assumption of surface roughness scattering effect, simulation shows the evidence of its effect.

5.3 Other Device Simulations: OLED and E-paper

5.3.1 Monte Carlo Method

Monte Carlo methods rely on repeated random sampling to estimate simulation results. Different from the deterministic model, Monte Carlo method is stochastic model. In the deterministic model, it is possible to find analytical solutions. However, there are lots of cases impossible to find solution. Especially, Monte Carlo simulation is useful for the system with many coupled degrees of freedom. Carrier transport or random particle collision problem is thus suitable for the Monte Carlo Simulation[13, 14].

For simple understanding, let's calculate π with Monte Carlo method. Someone throw darts randomly in the square including a circle (target) fully inside.

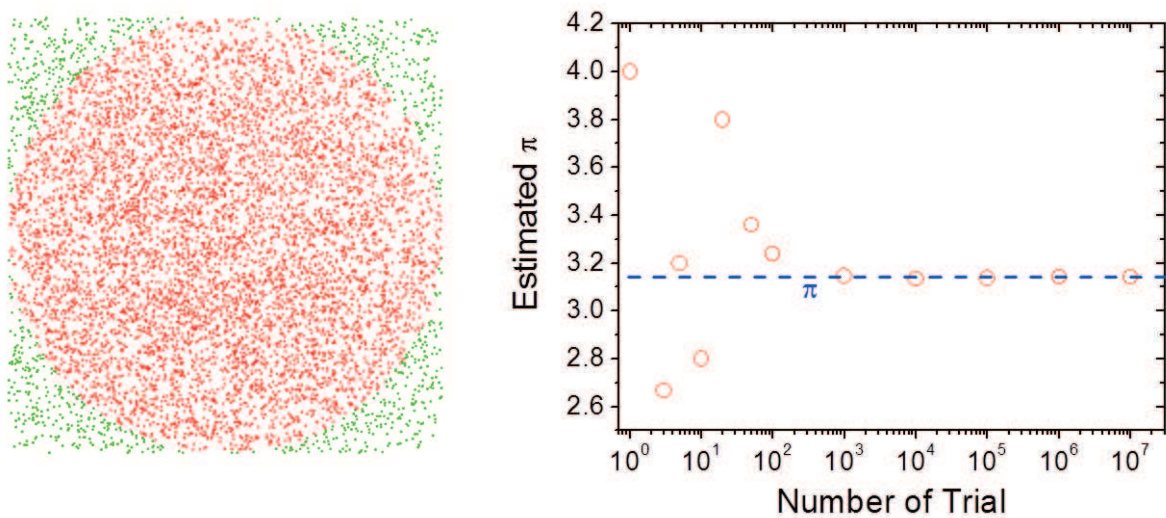


Figure 5.9 : Calculation of π using Monte Carlo method. Ratio between numbers of red darts to total darts is the ratio of area (left). More trial can achieve more accurate value (right).

If his throwing is completely random, darts will be uniformly distributed in the square. Some of them will be inside circle and others will be out of circle (but inside square). Thus the ratio of circle area / square area is the number of dart in the circle / in the square. It can be simply rearranged as:

$$\frac{N^\circ\ Dart\ \ in\ the\ circle}{N^\circ\ Dart\ \ in\ the\ square} = \frac{\pi r^2}{4r^2} = \frac{\pi}{4}, \tag{5.7}$$

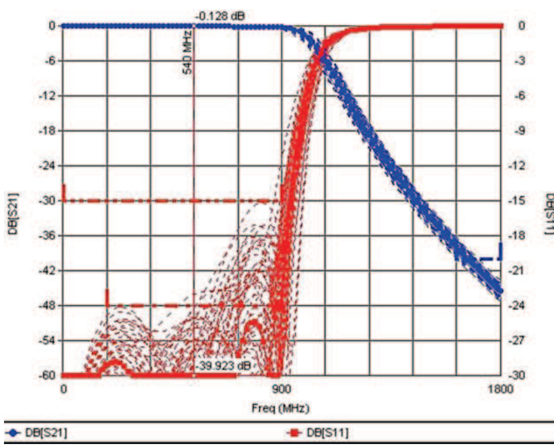


Figure 5.10 : Spice simulation of RF low pass filter using Monte Carlo simulation.

where r is the radius of circle. Thus without any analytical calculation, π can be calculated from the ratio of dart inside / outside of circle in the square. If the trial is increased, more accurate value π can be obtained as shown in Fig. 5.9. Like this example, Monte Carlo method can avoid complicated calculation and give realistic results when the system includes randomness. In circuit fabrication, it is impossible to make exactly same devices because the performance of device

components cannot be definitely same even in the same fabrication condition. Thus, all of circuits should be designed with the tolerances. In this case, the errors of each device parameters are random factors. The analytical simulation cannot consider these random factors in the complex circuit simulation. Monte Carlo simulation can give the realistic simulation results for the tolerance simulation of designed circuit.

5.3.2 Device Simulations: OLED and E-paper

Monte Carlo simulations of organic light emitting display (OLED) and electronic paper (E-paper) have been done for the optimization of device structure. For alternatives of liquid crystal display (LCD), research of OLED and E-paper has been being carried out [15, 16]. Especially in mobile devices, OLED occupies huge portion of market because it does not need back light module. OLED has several issues. For example, life time of OLED has been a research topic due to respectively shorter lifetime than other displays [17]. Basically OLED consists of organic materials. Thus performance of OLED can be degraded easily by other factors such as oxidation, contamination and high electric field. To enhance the life time of OLED, proper materials, device design and operating algorithm is necessary.

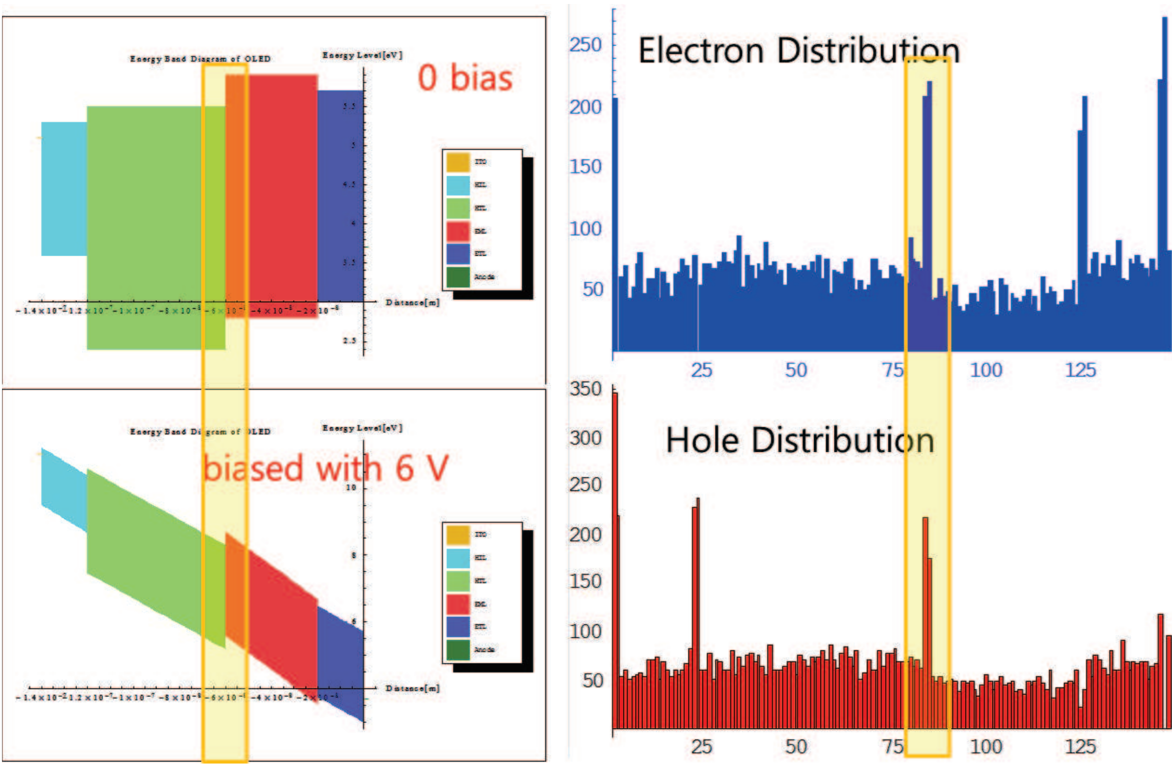


Figure 5.11 : Carrier transport simulation of OLED using Monte Carlo method. For efficient light emission, most of carriers should be accumulated in the region highlighted with yellow.

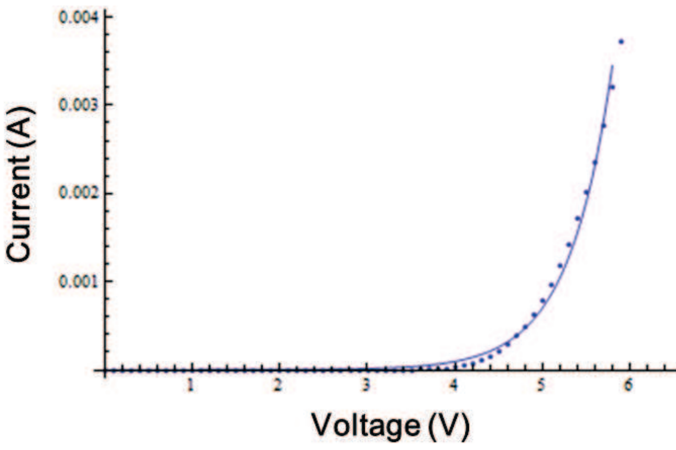
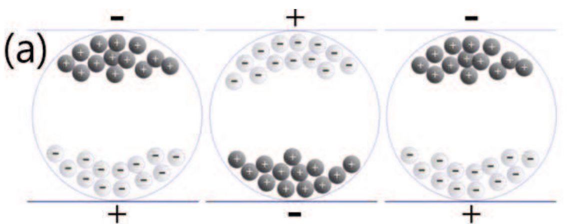


Figure 5.12 : I-V characteristic of OLED. Measured (dots) data is fitted by simulated (line) one.

Optimized device design needs proper thicknesses of each material layers such as anode, hole injection layer (HIL), hole transport layer (HTL), emission material layer (EML), electron transport layers (ETL), electron injection layer (EIL) and cathode. For the emission efficiency, most carriers should recombine in the EML. As shown in Fig. 5.11, energy barriers at material interfaces accumulate holes and electrons and it affect total transport characteristics. I-V characteristic was estimated from counting carriers as a function of given bias (Fig. 5.12).

E-paper use electrophoretic display to form visible images [18]. By rearranging charged pigment particle, it shows colored or white images. To rearrange the charged particles, transparent electrode covers the top of cell. E-paper doesn't need to be turned on continuously to display image. Once charged particles are rearranged, it can be remained without external power. It makes E-paper felt like real paper. Because E-paper does not use light emission, it also has been issued on the viewpoints of good legibility and readability and response time.



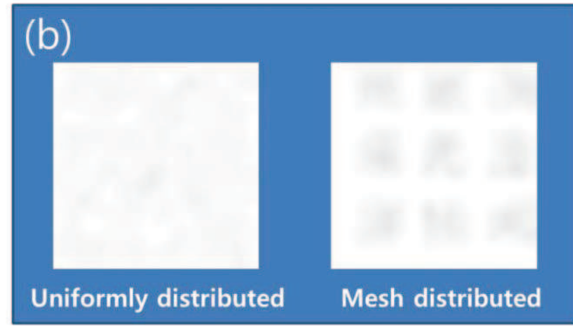


Figure 5.13 : (a) Operation scheme of E-ink [18]. (b) Contrast manipulation using mesh electrode structure.

To enhance the legibility and readability, the contrast control can be useful. Increased bias can strongly rearrange charged particles but power consumption will be increased. Electric field can be manipulated by the shape of top electrode. Mesh shape of electrodes gather the grid of charged particles at the top of the cell. In this case the aggregated particle can give enhanced contrast.

Before Monte Carlo methods, electric field and potential distribution were calculated using numerical analysis. As described in Ch. 5.2.1, Poisson's equation has been calculated to be the basis of the Monte Carlo simulation because

the movement of particle is affected by electric field.

Figure 5.14 : Potential and electric field distribution of unit cell. 6 electrodes (left) and 3 electrodes (right) are shown in this example.

Various fabrication conditions, for instance distance of electrode, amounts of charge in the particle and number of charges are considered as variables of the simulation. Stronger electric fields are confined in the cell when the number of electrode is increase and the electrode gap decreased. It reduces the flight time of the charged particle. When the charge of particle increases, particles are more affected by electric field and it reduces the response time. However, increased charge, particle number and electric field can make more collision among particles and it can increase the response time of E-paper.

To optimize the performance of E-paper, fabrication conditions and device geometry should be firstly defined. Monte Carlo simulation can be a useful tool for the device optimization in E-book production.

5.4 Conclusion

In chapter 5, various simulations are investigated. Usages of process simulation and device simulation and the importance of proper modeling were introduced. In the device development level, process simulation and device simulation can be complementary.

Finite difference method is one of the basic (but powerful) tools for the simulation. Using computational calculation, partial differential equation such as Poisson's equation can be

solved. Electric field, potential, carrier distribution can be calculated so that the device characteristics also can be estimated.

Monte Carlo simulation is based on the randomness of the simulation parameters. It can be useful in the case of that the analytical solution is difficult to find. Due to the randomness, Monte Carlo method may give more realistic simulation results.

To be an optimized device, device characterizations and simulation should be simultaneously carried out in the research. It can give the way to improve device performances.

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Chapter 6 Conclusion

Evolution of smart device and innovation of information induce the requirements of electronic devices. Various device features appear according to such kind of requirements.

The increase of modern device requirement enhances the development of field effect transistor. During tens of years, one of the major trends in FET has been channel length scaling down. However, device scaling down looks like arriving almost the end. Industry fabricates nanoscale devices using 22 nm process. As device dimension decreased, there are lots of unwanted phenomena represented as short channel effect.

To avoid the short channel effect such as threshold voltage variation, drain-induced barrier lowering punchthrough, velocity saturation and hot carrier effect, lots of technologies have been developed. As an example, multi gate structure has been researched to have better gate control about channel. For the better control and immunity of short channel effect, device channel structure has been achieved at almost 1D nanostructure such as FinFET, 3D stacked nanowire and junctionless FET etc. Due to the change of device structure in advanced FET, many physical factors neglected in bulk scale arise again.

In this thesis, basic and advanced device fabrication process which I have experienced during study has been shown in chapter 2. We have been discussed top-down and bottom-up approach for the nanoscale device fabrication technique. Especially, lithography technology has been focused because it is base of the modern device fabrication. For the advanced device structure, etching technique has been investigated in detail.

Because of the extremely scaled down device structure, device characterization becomes more complicated. In chapter 3, characterization of FET has been introduced. Based on the simple MOSFET operation model, we have discussed how to define series resistance, carrier mobility, threshold voltage. For the practical consideration in the advanced FET, several parameter extraction techniques have been introduced such as Y-function, split C-V etc.

In chapter 4, some kind of quasi-1D nanowire structure devices have been discussed based on previous chapters. FinFET is one of promising alternatives against conventional planar devices. Problem of FinFET is surface roughness. During the fabrication, the etching process induces surface roughness on the sidewall surfaces. Surface roughness of channel decreases the effective mobility by surface roughness scattering. With the low temperature measurement and mobility analysis, drain current through sidewall and top surface was

separated. From the separated currents, effective mobilities were extracted in each temperature conditions. As temperature lowering, mobility behaviors from the transport on each surface have different temperature dependence. Especially, in n-type FinFET, the sidewall mobility has stronger degradation in high gate electric field compare to top surface. Quantification of surface roughness was also compared between sidewall and top surface. Low temperature measurement is nondestructive characterization method. Therefore this study can be a proper surface roughness measurement technique for the performance optimization of FinFET.

As another quasi-1D nanowire structure devices, 3D stacked SiGe nanowire has been introduced in chapter 4.2. Important of strain engineering has been known for the effective mobility booster. In chapter 4.2, the limitation of dopant diffusion by strain has been shown. Without strain, SiGe nanowire FET showed huge short channel effect. Subthreshold current was bigger than strained SiGe channel. Temperature dependent mobility behavior in short channel unstrained device was completely different from the other cases. Impurity scattering was dominant in short channel unstrained SiGe nanowire FET. Thus, it could be concluded that the strain engineering is not necessary only for the mobility booster but also short channel effect immunity.

As described in chapter 4.3, Junctionless FET is very recently developed device compare to the others. Like as JFET, junctionless FET has volume conduction. Thus, it is less affected by interface states. Junctionless FET also has good short channel effect immunity because off-state of junctionless FET is dominated pinch-off of channel depletion. For this, junctionless FET should have thin body thickness. Therefore, multi gate nanowire structure is proper to make junctionless FET.

Because of the surface area to volume ratio, quasi-1D nanowire structure is good for the sensor application. In chapter 4.4, nanowire structure has been investigated as a sensor. Using numerical simulation, generation-recombination noise property was considered in nanowire sensor. Even though the surface area to volume ration is enhanced in the nanowire channel, device has sensing limitation by noise. The generation-recombination noise depended on the channel geometry. As a design tool of nanowire sensor, noise simulation should be carried out to escape from the noise limitation in advance.

Characterization should have a model to explain the device physics. Without this model, device operation cannot be properly explained. Thus, device simulation with physical model is necessary to explain why the device operates and to predict how it will operate. In chapter 5, the basic principles of device simulation have been discussed. Finite difference method and Monte Carlo simulation technique have been introduced for the comprehension of device

simulation. Practical device simulation data have been shown for examples such as FinFET, strongly disordered 1D channel, OLED and E-paper.

Through this thesis, we have traveled from the device fabrication to modeling. At the beginning of this chapter, I said “device scaling down looks like arriving almost the end”. Sometimes it sounds like that there is no field to improve in transistor engineering. However, as we have seen in this thesis, there are plenty works to do in all around of transistor research. I hope that studies in this thesis contribute to the small part in semiconductor device research.

Appendix

Appendix 1: Physical Constants

Appendix 2: General Properties of Si, Ge and SiGe

Appendix 3: E-beam Lithography Pattern Design Program using Mathematica

Appendix 4: Fundamental Vacuum System

Appendix 5: Publication List

Appendix 1: Physical Constants

q	Electronic charge	1.602×10^{-19} C
m_0	Electron mass in free space	9.109×10^{-31} kg
m_p	Proton rest mass	1.673×10^{-31} kg
c	Speed of light in vacuum	2.998×10^{8} m/s
ε_0	Permittivity of vacuum	8.854×10^{-14} F/cm
k_B	Boltzmann's constant	1.381×10^{-23} J/K
		8.617×10^{-5} eV/K
h	Planck's constant	6.625×10^{-34} J s
		4.135×10^{-15} eV s
K_T ($K_B T$)	Thermal energy	0.02586 eV (T = 27 °C)
		0.02526 eV (T = 20 °C)

Appendix 2: General Properties of Si, Ge and SiGe

List of physical properties about Si, Ge, and SiGe [1].

<table>
<tr><th colspan="2">Properties</th><th>Si</th><th>$Si_{0.75}Ge_{0.25}$</th><th>$Si_{0.5}Ge_{0.5}$</th><th>$Si_{0.25}Ge_{0.75}$</th><th>Ge</th></tr>
<tr><td colspan="2">Atoms/cm3</td><td>5.0×10^{22}</td><td>4.805×10^{22}</td><td>4.61×10^{22}</td><td>4.415×10^{22}</td><td>4.42×10^{22}</td></tr>
<tr><td colspan="2">Atomic weight</td><td>28.09</td><td>39.2175</td><td>50.345</td><td>61.4725</td><td>72.6</td></tr>
<tr><td colspan="2">Breakdown field (V/cm)</td><td>$\sim 3 \times 10^5$</td><td>2.5×10^5</td><td>2×10^5</td><td>1.5×10^5</td><td>$\sim 10^5$</td></tr>
<tr><td colspan="2">Crystal Structure</td><td>Diamond</td><td>Diamond</td><td>Diamond</td><td>Diamond</td><td>Diamond</td></tr>
<tr><td colspan="2">Density (g/cm3)</td><td>2.328</td><td>3.078</td><td>3.827</td><td>4.577</td><td>5.3267</td></tr>
<tr><td colspan="2">Dielectric constant</td><td>11.9</td><td>12.925</td><td>13.95</td><td>14.975</td><td>16</td></tr>
<tr><td colspan="2">Effective density of States in conduction band, N_c (cm^{-3})</td><td>2.8×10^{19}</td><td>-</td><td>-</td><td>-</td><td>1.04×10^{19}</td></tr>
<tr><td colspan="2">Effective density of States in valence band, N_v (cm^{-3})</td><td>1.04×10^{19}</td><td>-</td><td>-</td><td>-</td><td>6.0×10^{18}</td></tr>
<tr><td rowspan="4">Effective Mass, m/ m^0</td><td rowspan="2">Electrons</td><td>m_l= 0.98</td><td>-</td><td>-</td><td>-</td><td>m_l= 1.64</td></tr>
<tr><td>m_t= 0.19</td><td>-</td><td>-</td><td>-</td><td>m_t= 0.082</td></tr>
<tr><td rowspan="2">Holes</td><td>$m_{l\,h}$= 0.16</td><td>-</td><td>-</td><td>-</td><td>$m_{l\,h}$= 0.044</td></tr>
<tr><td>$m_{h\,h}$= 0.49</td><td>-</td><td>-</td><td>-</td><td>$m_{h\,h}$= 0.28</td></tr>
<tr><td colspan="2">Electron affinity</td><td>4.05</td><td>4.0375</td><td>4.025</td><td>4.0125</td><td>4</td></tr>
<tr><td colspan="2">Minimum Indirect Energy Gap (eV) at 300K</td><td>1.12</td><td>1.05</td><td>0.945</td><td>0.804</td><td>0.66</td></tr>
<tr><td colspan="2">Minimum Direct Energy Gap (eV)</td><td>3.4</td><td>3.1</td><td>2.5</td><td>1.6</td><td>0.7</td></tr>
</table>

Intrinsic carrier concentration (cm^{-3})	1.45×10^{10}	0.6×10^{13}	1.2×10^{13}	1.8×10^{13}	2.4×10^{13}
Intrinsic Debye length (μm)	24	18.17	12.34	6.51	0.68
Intrinsic resistivity (Ω-cm)	2.3×10^{5}	1.725×10^{5}	1.15×10^{5}	$.575 \times 10^{5}$	47
Lattice Constant (A)	5.4310	5.4825	5.5373	5.5960	5.6575
Linear coefficient of thermal expansion, ΔL/LΔT (°C^{-1})	2.6×10^{-6}	3.4×10^{-6}	4.2×10^{-6}	5.0×10^{-6}	5.8×10^{-6}
Melting point (°C)	1415	1295.5	1176	1056.5	937
Minority carrier lifetime (s)	2.5×10^{-3}	2.125×10^{-3}	1.75×10^{-3}	1.375×10^{-3}	10^{-3}
Mobility (drift) (cm^2/V s)	1500(electron)	2100(electron)	7700(electron)	3300(electron)	3900(electron)
	450(hole)	812.5(hole)	1175(hole)	1537.5(hole)	1900(hole)
Optical – phonon energy (eV)	0.063	-	-	-	0.037
Phonon mean free path λ0(Å)	76 (electron)	-	-	-	105
	55 (hole)				
Specific heat (J/g °C)	0.7	.6025	.505	.4075	0.31
Thermal conductivity at 300 K (W/cm °C)	1.5	.085	.083	.11	0.6
Thermal diffusivity (cm^2/s)	0.9	.765	.63	0.495	0.36
Vapor pressure	1 at 1650°C	1 at 1570°C	1 at 1490°C	1 at 1410°C	1 at 1330°C

(Pa)	10^{-6} at 900°C	10^{-6} at 865°C	10^{-6} at 830°C	10^{-6} at 795	10^{-6} at 760°C

Reference

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Appendix 3: E-beam Lithography Pattern Design Program using Mathematica

Unlike using photo mask in photo lithography, E-beam lithography use pattern file. The Pattern file includes structure generated by the software like CAD [1]. There are several advantages of conventional CAD tool. For instance, it is quite popular and easy so that there are common source of introduction and help. Also, there are lots of functions to make design easy. However, conventional CAD tool cannot import another images for drawing background. In the case of top-down approach, align-keys could be enough to make definite alignment but for the bottom-up approach, sample image is necessary for the background to make exact position. For example, let's think about the back gate ZnO nanowire FET on the SiO_2 substrate. After synthesizing ZnO nanowire, it should be well dispersed on the SiO_2 substrate. The SiO_2 substrate already has pre-patterned contact pads and aligns keys. We will draw electrode structure to make contact on edges of ZnO nanowire. How can we know where the ZnO wire is? To know the position ZnO nanowire, we need images on the substrate using optical microscope or AFM (in the case of target is very small). This image should include align-keys to define the relative position of ZnO nanowire. Thus for the electrode design, substrate image which includes the target and align-key is needed as back-ground image.

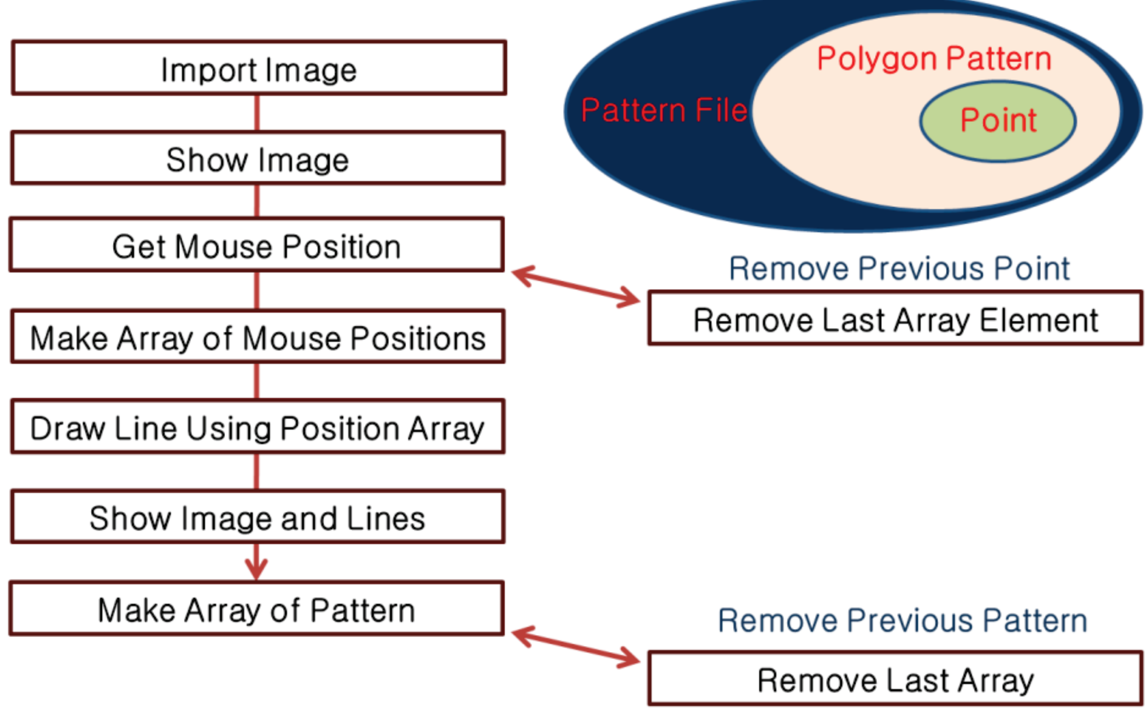

Figure A.1 : Main process of E-beam lithography pattern design program.

To make it easier, pattern design tool has been developed using Mathematica 7 [2]. Mathematica has dynamic module and manipulation function after the version of 7. Especially manipulation function is very helpful to make user interfaces. It gives immediate access to changeable variables with powerful interactive capabilities.

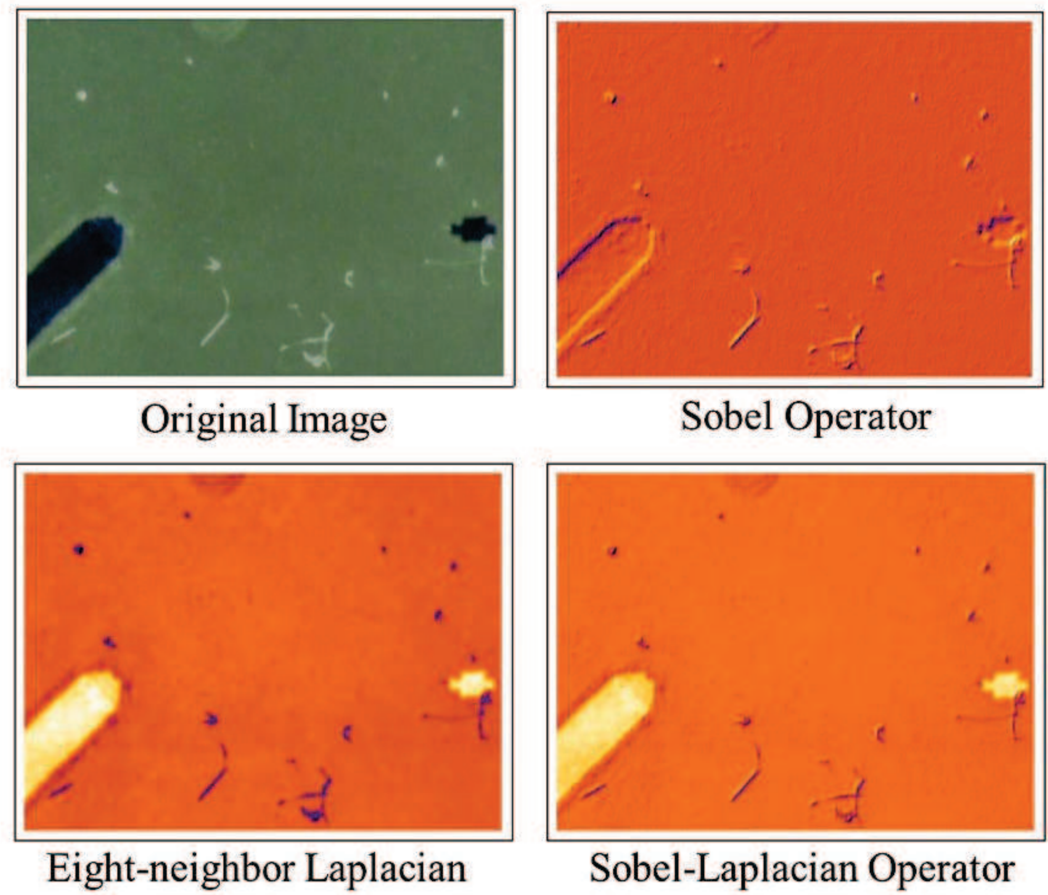

Figure A.2 : Original image and different outputs of image processing.

This design tool works as following:

A) Import Image

As we mentioned before, for the drawing with exact position, sample images is necessary. The function of **Import** gives access to the external data files. **Import[“file”]** imports data from a file. For example, **Import[“ZnO.jpg”, “Data”]** means that ZnO.jpg file will be called and returned as numerical data.

B) Image Processing

The image of optical microscopy does not have enough magnification to see nanostructure. Even though ZnO nanowire has the length of several micrometers, the shape of nanowire can be blurred in the picture. To enhance hazy shape of nanowire, image processing algorithms are added in the program. Sobel operator and eight-neighbor Laplacian operator were used to

make edge detection [3]. Sobel and Laplacian operators are differentiation operators. It makes differences from neighbors and gives the information of changing value. In this tool, root mean square average of Sobel and Laplacian operator were used. Output image is similar to AFM images. It has obvious separation between the target nanowire and others, which help easier patterning.

C) Alignment

Before drawing structures on the imported background image, position alignment has to be carried out. Every sample has different (X, Y) positions. To draw structure easily in such different systems, another coordinate system (U, V) is needed. For example, if the (X, Y) vector is translated to (U, V), a pattern in (U, V) coordinate can be available in all same shape of pre-patterned contact pads and align-markers even with different (X, Y) positions. An affine transform algorithm was used to translate vector coordinates [4, 5]. The affine transform is the most common transform used in image processing technique. Using simple linear algebra, the relationship between real position (X, Y) and imaginary position (U, V) can be expressed as following:

$$\begin{pmatrix} U \\ V \\ 1 \end{pmatrix} = \begin{pmatrix} aX & bY & c \\ pX & qY & r \\ 0 & 0 & 1 \end{pmatrix} = \begin{pmatrix} a & b & c \\ p & q & r \\ 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} X \\ Y \\ 1 \end{pmatrix} = M_{affine} \begin{pmatrix} X \\ Y \\ 1 \end{pmatrix},$$

where M_{affine} is the affine matrix.

In the affine matrix, we have 6 variables (a, b, c, p, q, r). Thus, at least 3 points of (X, Y) are necessary to solve these equations (to create 6 equations).

After M_{affine} is defined, all of patterns in (U, V) coordinate can be transformed to (X, Y) coordinate using M_{affine}^{-1}. It makes alignment between (U, V) and (X, Y).

D) Structure Drawing

After alignment, structure can be drawn. Using the function of **Mouseposition**, (U, V) vectors are taken on the background image. Each (U, V) vectors are appended one after another. Each polygon structure can be separated with protocols. For instance, in ELPHY Quantum system [6], the number set {1, 100, 1} is used to distinguish the start and the end of each polygon.

E) Save File

Completed structure has to be saved. In this tool, ASCII [7] code used to save patterns. *.asc is used for file extension.

With these functions, customized drawing tool has been developed. During the patterning, seeing and checking the sample images give comfortable and exact design of each structure.

Practically, using this tool, 100 nm pattern size has been made by e-beam lithography in ELPHY Quantum system.

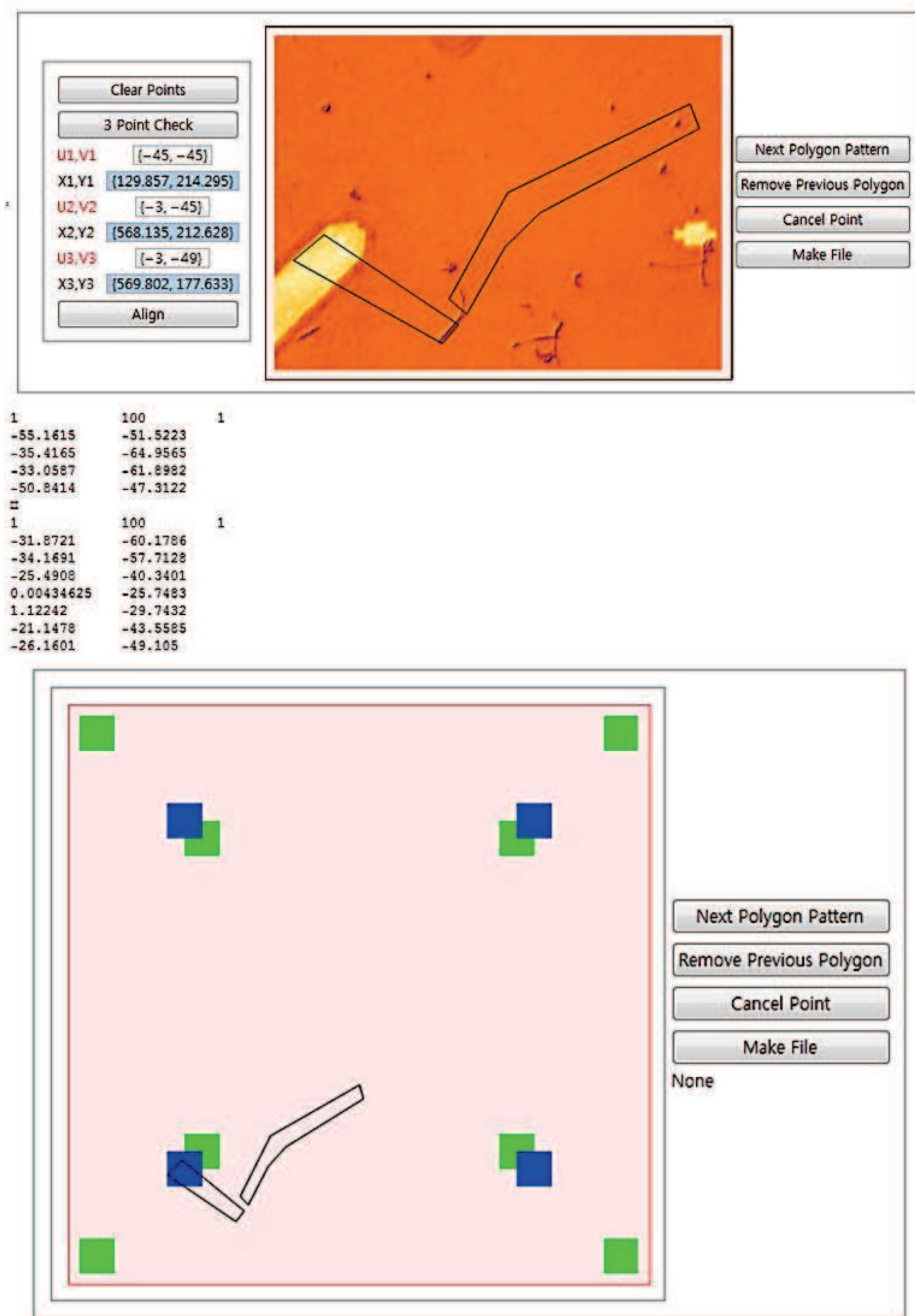

Figure A.3 : Screen shot of pattern design program using Mathematica 7.

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Appendix 4: Fundamental Vacuum System

Vacuum systems have been not only widely used in the device fabrication but also in the measurement systems. Why vacuum is needed? When a system needs to be clean or need some special circumstance, vacuum is necessary. In the device fabrication process, 10 ppm (part per million) of boron make the electrical conductance 1000 times higher. It is as same as the probability of the encounter with hydrogen in the ambient air. Unintended surface oxidation should be also avoided. Native oxide can be formed on the exposed surface during the process. If the device, such as unpassivated OTFT or OLED, is weak against the oxidation for example, it should be kept in the vacuum desiccator. For the low temperature measurements, vacuum condition is necessary to remove water molecules. If water molecules remain, it will be frozen below 273 K and disturb contact probing for the electrical measurements.

There are several units for the degree of vacuum but Torr and Pa (Pascal, N/m^2) are the most popular. One atmospheric pressure is 760 Torr and 1 Torr is 133.3 Pa. It is easy to remember if we approximate 1 Torr is about 100Pa. According to the degree of vacuum, three vacuum statuses, low vacuum, high vacuum and ultrahigh vacuum, are defined. Low vacuum (or called rough vacuum) is the range of $760 \sim 10^{-3}$ Torr [1]. In the low vacuum, the number of vapor molecule is larger than the number of molecule attached inside the chamber. It is used for the distillation, the sputtering, LPCVD (low pressure chemical vapor deposition) and the plasma process etc. High vacuum is the range of $10^{-3} \sim 10^{-7}$ Torr and ultrahigh vacuum is the range of below 10^{-8} Torr [1]. In these cases, the mean free path of the vapor molecule is longer than the chamber length. Thus the molecule collision with chamber is frequent than with other molecules. High vacuum and ultrahigh vacuum is used in the ion implantation, e-beam evaporation and SEM etc. Sometimes people define medium vacuum or extremely high vacuum depending on the usages.

The selection of proper pump in the vacuum system is very important. No pump can go to hi vacuum or ultrahigh vacuum directly because each pump has own operation pumping range. Thus, various combinations are used in the vacuum systems.

For the low vacuum, rotary pump and dry pump are most widely used. Rotary pump compress the gas to the higher pressure than atmospheric pressure and exhaust outside [2]. Pump module is in the oil. This oil is used for the cooling, lubrication and sealing etc. Thus oil should be cleanly maintained. If the pump operates with low pressure, the oil vapor tends to flow back into the vacuum chamber. It can be the contamination source during the process. Dry pump works without pump oil [2]. Like the engine, it includes pistons which compress and remove the gas. Thus dry pump is suitable at the extremely high clean process.

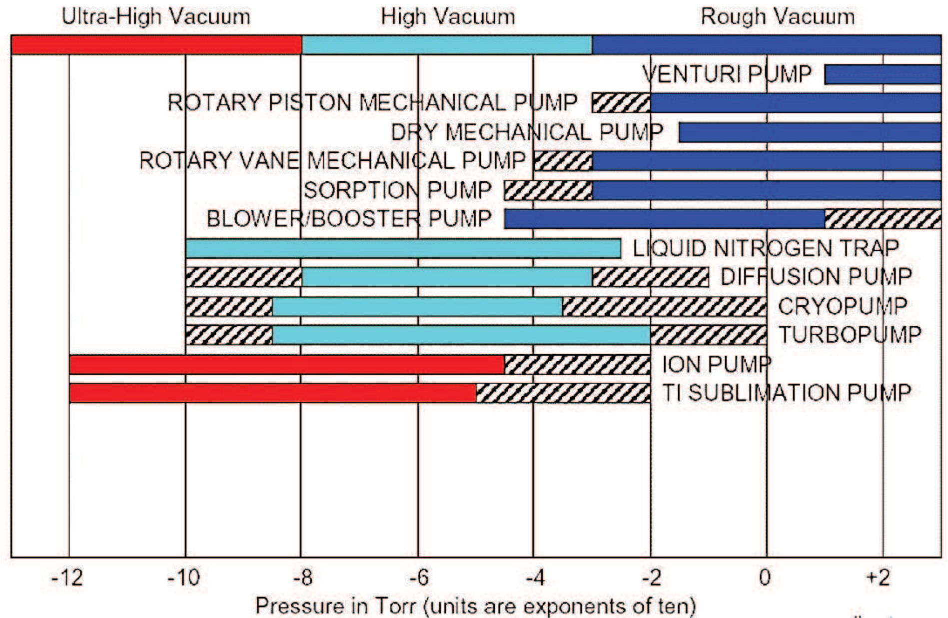

Figure A.4 : Vacuum pump pressure range [3].

For high and ultrahigh vacuum, diffusion pump, turbo molecular pump and Cryopump is widely used. Most of high vacuum pump cannot work at the atmospheric pressure but below 10^{-3} Torr after removing most of gas [3]. Diffusion pump uses heated oil. The oil is heated up to boiling point. The vapor of oil is sprayed by jet nozzle. When accelerated oil vapor heat the pump body which is cooled by water, oil vapor is condensed and flow down. The air in the chamber collides with this fast and heavy oil vapor and compressed. Compressed gas goes out through fore line. Diffusion pump is cheap and easy to control. It has high throughput. However, the pump oil back-streaming and the contamination of chamber can be happened. On the other hand, turbo molecular pump does not use the pump oil [3]. Turbo molecular pump is purely mechanical pump. It includes rotors and stators which have wings. Stator is fixed while rotors spin from 9000 rpm to 90000 rpm. Instead of the pump oil, gas molecule collides with the rotors and condensed. Turbo molecular pump is clean system but it is expensive to install and noisy because of high rpm. The operation mechanism of Cryopump is very different from the others. Cryopump cool down gas and frozen gas removed from the chamber [3]. Cryopump consists of He compressor, cold head and pump body. It is closed loop refrigeration system. Turbo molecular pump does not use the pump oil and actuation part so that it is very clean and silent. However, it needs extra pure He and periodic regeneration. Thus maintenance is expensive.

Apart from introduced pumps, there are many pump system such as sorption pump, Venturi pump and blow/booster pump for low vacuum and ion pump, titanium sublimation pump and non-evaporable getter pump for ultrahigh vacuum. However, they are not introduced in this chapter because they are not widely used in the conventional semiconductor process.

To get the high quality and yield rate of the fabrication, vacuum system should be well defined in the instruments. Maintenance of vacuum system is also important for the process.

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Appendix 5: Publication List

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[3] D. Jang, **J. W. Lee**, K. Tachi, L. Montes, T. Ernst, G. T. Kim, and G. Ghibaudo, **"Low-frequency noise in strained SiGe core-shell nanowire p-channel field effect transistors"** *Appl. Phys. Lett.,* vol. 97, Aug 2010.

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[6] **J. W. Lee,** D. Jang, M. Mouis, G. T. Kim, T. Chiarella, T. Hoffmann and G. Ghibaudo, **"Experimental Analysis of Surface Roughness Scattering in FinFET Devices"** Proceeding of ESSDERC 2010 **(Young Scientist Award),**

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[10] **J. W. Lee**, M. Mouis, D. Jang, K. Tachi, G. T. Kim, T. Ernst, G. Ghibaudo, **"Short Channel Mobility Analysis of SiGe Nanowire pFETs: Origins of the Strain Induced Performance Improvement"** Solid State Electronics **(submitted)**

국문 초록

미국 벨 연구소에서 최초의 트랜지스터가 제작된 이후, 전계 효과 트랜지스터 (field effect transistor,이하 FET)는 현대사회의 급격한 정보화 혁명에 영향을 미쳤다. 쏟아지는 많은 양의 새로운 정보들을 처리하기 위하여 퍼스널 컴퓨터에서 최근 스마트폰과 같은 모바일 기기까지 다양한 형태의 장비들이 등장하였고 자연스레 더 작고, 더 좋은 성능을 지닌 전자소자가 필요로 하게 되었다.

더 빠르고 더 작으면서도 더 좋은 성능을 갖기 위하여 FET는 채널길이가 짧아지는 형태로 발전하게 되었고, 2011년 인텔이 22나노 공정을 이용한 FET를 발표함으로써 채널의 길이는 이제 양자역학을 고려해야만 하는 나노미터 수준으로 작아지게 되었다.

이러한 채널 길이의 감소는 FET의 문턱전압을 높이거나 게이트 전압이 문턱전압을 넘지 않았는데도 원치 않는 전류가 흐르는 드레인 전류 누설, 게이트 절연막이 얇아짐으로써 생기는 게이트 전류 누설 등의 다양한 부작용을 가지고 있다.

이러한 숏 채널 이펙트 (short channel effect, 이하 SCE)를 방지하고 소자의 성능을 극대화하기 위해 새로운 채널 물질 및 소자 구조 등에 대한 연구가 진행되고 있다. 그 한 예시로 다중 게이트 구조는 채널에 대한 더 나은 게이트 컨트롤을 위하여 활발한 연구가 진행되고 있으며, FinFET, 3D 적층형 SiGe나노선 FET, 정션리스 트랜지스터와 같은 형태의 다중 게이트 구조 소자에 대한 연구 결과가 발표되고 있다. 이러한 소자는 짧은 채널 길이를 가짐과 동시에 채널 폭 또한 매우 작아져 1차원 형태의 나노선 구조를 갖는다.

이 논문은 학위과정 동안 경험해본 다양한 소자의 측정 및 모델링에 대해 다루고 있다.

제 1장에서는 반도체 소자의 시장 동향 및 기술 트랜드에 대해 다루고 있다. 점점 짧아지는 FET의 채널 길이에 따른 SCE에 대한 설명과 이를 극복하기 위한 최신 기술들을 간략히 소개한다.

제 2장에서는 소자 제작을 위해 필수적인 기술들에 대해 서술하고 있다. 나노 스케일의 소자를 제작하기 위해 필요한 기본적인 리소그래피 장비에서부터 에칭장비까지 학위과정 동안 사용했던 다양한 장비들을 소개하고 장비가 동작하기 위한 이론적 기반과 각 장비의 세부 특징을 다루고 있다.

제 3장에서는 FET의 특성을 분석하고 파라미터를 추출하는 방법에 대해서 이야기하고 있다. 간단한 MOSFET 동작 모델을 기반으로 일련의 컨택저항, 캐리어 이동도, 문턱전압 등을 정의하는 방법에 대해 논의한다. 또한 Y-펑션, CV 측정 등 실질적으로 많이 쓰이게 되는 FET소자에 대한, 여러 파라미터 추출 기법에 대해 알아본다.

제 4 장에서는 유사 1D nanowire 구조 소자의 특성에 대해 논의한다. 이전 장들에서 이야기 했던 내용들을 바탕으로 실제 소자를 측정하고 분석 한 내용들을 담았다.

제 4장의 시작에서는 FinFET에 대해 다루고 있다. 기존의 평면형태 FET에 대한 대안으

로 대두되는 FinFET 제작하는 과정중의 에칭 프로세스에 의해 측벽 표면이 거칠어지게 되는데 이러한 거칠기는 캐리어를 산란시켜 캐리어 이동도를 낮추게 된다. 저온 실험을 이용한 캐리어 이동도 분석으로부터 측벽과 소자 윗벽에 대한 정성적 차이를 알아보고, 이를 통해 표면의 거칠기를 정량적으로 분석하는 방법을 설명한다.

다음으로 SiGe 나노선 FET에 있어서 strain의 효과에 대한 내용을 다룬다. 실리콘에서 P 타입 소자가 N 타입에 비해 상대적으로 작은 캐리어 이동도를 갖는 문제를 해결하기 위해 SiGe이 채널 물질의 대안으로 연구되고 있다. 특히 strain의 방향에 따른 캐리어 이동도의 증가가 위 문제에 대한 해결책 중 하나로 제시됨에 따라 strain이 가해진 SiGe 나노선 FET의 연구가 활발히 진행중에 있다. Strain이 가해진 소자와 그렇지 않은 소자의 비교에 따른 SiGe 채널 내에서의 strain 영향을 알아보고 앞으로 새로운 소자에 대해 고려해야 할 점에 대해 논의한다.로

다음으로 이어지는 정션리스 소자 부분에서는 대안 소자로 떠오르는 완전히 새로운 형태의 소자인 정션리스 소자에 대해 알아보고 이 소자가 갖고 있는 장점과 단점을 현상학적으로 분석하고 앞으로 이어질 정션리스 소자 연구에 있어서 우리가 고려해야 할 부분들에 대한 논의를 한다.

마지막으로 나노선 FET 센서에 대한 논의가 이어진다. 전기화학적 게이팅을 이용한 센서로서의 나노선 특성을 시뮬레이션을 통해 예측해본다. 특히 나노선 자체가 내재적으로 가지고 있는 내부 노이즈로부터 센서를 설계할 때 우리가 꼭 고려해야 할 파라미터들에 대해 새로운 수학적 모델을 제시하고 센서 설계를 위한 지표를 제시한다.

제 5장에서는 소자 시뮬레이션 및 모델링에 대해 이야기한다. 공부하는 동안 사용했던 다양한 시뮬레이션 기법에 대해 이론적 배경을 설명하고 실제 적용 예를 통해 소자 시뮬레이션의 기초에 대해 알아본다. 수치해석법 및 몬테카를로 시뮬레이션이 시뮬레이션의 이해를 돕기 위해 설명되었고 FinFET, OLED 및 전자종이 등에 대한 적용 예를 보여준다.

이와 같이 본 논문은 소자 제작 기술에서부터 측정 및 분석과 시뮬레이션을 통한 소자 모델링까지 다양한 분야를 아울러 학위 기간 중에 배우고 경험했던 내용들에 대해 다루고 있다.